FABRICATION AND CHARACTERIZATION OF POLYMER BASED METAL-OXIDE-SEMICONDUCTOR AND NON-VOLATILE MEMORY DEVICES

A Dissertation presented to the Faculty of the Graduate School

University of Missouri

In Partial Fulfillment

of the Requirements for the Degree

Doctor of Philosophy

---

by

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December 2009

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FABRICATION AND CHARACTERIZATION OF POLYMER BASED METAL-OXIDE-SEMICONDUCTOR AND NON-VOLATILE MEMORY DEVICES

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ACKNOWLEDGEMENTS

I sincerely thank Prof. Shubhra Gangopadhyay, my doctoral committee chair and research advisor, for giving me lots of opportunity to work within her research group on this very interesting project, and for providing excellent guidance and advice throughout my time in her group. Without Dr. Shubhra's ever present guidance, my work would have in no way been possible. I will be eternally grateful to her.

I also sincerely thank my co-advisor, Prof. Suchi Guha for her time and continuous effort in helping me to complete organic electronics work. I would also like to graciously thank the other two doctoral committee members, Prof. Naz Islam and Prof. Gregory Triplett.

It would have been nearly impossible for me to reach this point without the help, support and creative diversions provided by all of my current group members: Dr. Venu, Dr. Joseph, David, Bala, Sangho, and all my colleagues. I would like to thank my previous group members for providing useful discussion and assistance in the early stages of my work: Dr. Maruf, Dr. Arif, Dr. Othman, and Rama. I am also thankful to my many friends who supported me through difficulties I encountered during my research and life in U.S.A.

Last but not least, I wish to dedicate this work to my loving parents and all of my brothers and sisters. Their lifelong support and caring has been instrumental in my life. Thank you all.

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ABSTRACT

Organic field-effect transistors (FETs) have been widely investigated due to their potential applications in low cost, large area, and flexible electronics. Despite the rapid progress in organic FETs there are still obstacles- high density of defect in organic semiconductor and poor interface between dielectric and organic semiconductor, which leads to relatively high operating voltage.

Due to the large bandgap, polyfluorenes are very promising organic semiconductor for blue emitting display application. The electrical characteristics of ethyl-hexyl substituted polyfluorene (PF2/6) devices rely on the type and quality of polymer semiconductor and dielectric. Trapped and interfacial charges have significant impact on the performance of polymer light-emitting diodes and FETs resulting in delay time of electroluminescence at low voltages and voltage instability. Electrical measurement allows the extraction of material parameters, such as doping density, mobility, and interface states density.

In this dissertation, detailed charge transport characteristics of PF2/6 using hybrid metal-oxide-semiconductor (MOS) structures are presented. Capacitance-voltage and conductance-voltage measurements give insight into the presence of distribution of trap charges at the dielectric/polymer semiconductor interface and bulk of polymer. By thermal annealing of PF2/6 film to a semicrystalline phase, the device characteristics such as field-effect mobility as well as the interface properties of dielectric/(PF2/6) are significantly improved.

Charge storage characteristics of MOS structure containing size tunable sub-2 nm Pt nanoparticles between Al_2O_3 tunneling and capping oxide layers were studied. Significantly different amounts of memory window were obtained with the different size of Pt nanoparticles embedded in the MOS structure and reached a maximum of 4.3 V using 1.14 nm Pt nanoparticles, which corresponds to the largest particle density and optimum interparticle distance obtained in our particle deposition method. Satisfactory long term non-volatility was attained in a low electric field due to the Coulomb blockade and quantum confinement effects in ~1 nm Pt nanoparticle. These properties are very promising in view of device application. Further, our metal nanoparticle formation at room temperature is integrated to polymer dielectric and semiconductor to produce polymer-based non-volatile memory.

Chapter 1. Introduction

The discovery of electrical conduction in organic solids dates back nearly 100 years with the observation of photoconductivity and the study of the dark conductivity in anthracene crystals [1]. In 1977, the first highly conducting polymer, chemically and electrochemically doped polyacetylene, was discovered by A. J. Heeger, H. Shirakawa, and Alan G. MacDiarmid, which won them a Nobel Prize in Chemistry in 2000 [2]. This remarkable observation opened up an entire new field called organic electronics, and a new range of applications for conducting and semiconducting organic materials. Organic electronics generally refers to electronic devices and systems that are based on organic semiconductors, particularly conjugated polymers, and generally it is applied to three main technological areas: organic light-emitting devices (OLEDs), organic photovoltaic solar cells, and organic electronic circuits based on organic thin film field effect transistors (OTFTs or OFETs).

One of the key advantages is the ease by which polymer based devices can be made. The main procedure used in building such devices is spincoating of a polymer solution on a given substrate. For the industry it is possible to compete and win over more traditional technologies since it is relatively easy and cost effective process to fabricate devices compared with the conventional Si-based microelectronics. And by utilizing flexible substrate we can even roll or bend the devices, which can be a flexible rollup display for the future [3].

Until now, remarkable progress has been made in the development of organic electronic devices. The performance of the best organic materials now rivals that of the amorphous silicon thin film transistors (TFTs) commonly used as the pixel-switching elements in active matrix flat-panel displays. Organic TFTs combine the electrical properties of organic semiconductors with the properties typical of plastics: low cost, versatility of chemical synthesis, ease of processing, and flexibility. Organic memory device is another form factor to be used in future flexible electronics.

The dissertation is divided into seven chapters dealing with different aspects of organic and memory devices. Chapter 2 reviews the basic background in organic semiconductors and provides a theoretical description of charge transport in organic semiconductors at the molecular level. Understanding the influence of molecular parameters on charge transport and its structure-property relationship are extremely important in designing new organic semiconductors and devices. In addition, this chapter gives the necessary additional background in physical electronics that is needed for a discussion of electronic devices from metal-oxide-semiconductor (MOS) capacitors to non-volatile memory devices.

Chapter 3 describes the impact of Al_2O_3 on the capacitance characteristics of polyfluorene-based MOS structures. Polymer MOS structures are the two terminal analogues of polymer thin film transistors sharing the same basic layer structure. Electrical characterizations such as capacitance-voltage (C-V) and capacitance-frequency (C-F) measurements in these devices yield information about doping of polymer semiconductor, trapped charges, and trapping process in these devices. Those quantities are critical to evaluate the interfacial trap states between dielectric and polymer

semiconductor. Detailed analysis of the polymer semiconductor/Al_2O_3 interfacial properties using C-V and conductance-voltage (G-V) techniques is presented.

Chapter 4 focuses on the influence of thermal annealing of polyfluorene-based MOS structure on the interface properties. The experimental details and methodologies were described and followed by structure and morphology of the polymer semiconductor, polyfluorene. Results and discussion of C-V and G-V measurements including the Schottky-Mott analysis as well as a detailed analysis of the interface trap densities are discussed.

Chapter 5 provides sub-2 nm size tunable Pt nanoparticles embedded MOS non-volatile memory device on thin Al_2O_3 tunneling and control oxide layers and shows different amount of charging density according to the size and density of nanoparticles. Its endurance and retention characteristics also demonstrated.

This dissertation concludes with chapter 6, where the major conclusions derived from the work of this dissertation. Several ideas regarding possible future work and directions are also briefly discussed in the concluding chapter.

Chapter 2. Theory

2.1. Organic Semiconductor

In recent years, the use of organic semiconductors have become very attractive for building electronic and optoelectronic devices such as active matrix displays, photovoltaic cells, and organic integrated circuits due to their low cost solution processing [4]. Although there have been significant improvements in organic semiconductor-based electronic and optoelectronic devices, there are still many open issues that need to be fully addressed before commercialization of such devices can begin. A few of them include low carrier mobility and stability in organic semiconductor compared with their inorganic counterparts and interface traps which can dramatically impact the electronic properties of organic semiconductor and the operation of organic devices [5]. The development of a suitable device structure and self-organized high quality organic semiconductor thin films as well as the structure-property relationship of these organic materials are critical issues for enhancing the performance of organic semiconductor devices.

2.1.1. Charge Transport

The development of the field of organic electronics has benefited from the unique set of characteristics offered by π-conjugated polymers. The charge transport properties in conjugated materials critically depend on the packing of the chains and degree of order

in the solid state [6] as well as on the density of impurities and structural defects [7]. As a result, the measured mobility values can largely vary as a function of sample quality [8].

Organic semiconductors operate under conduction mechanisms that are vastly different from inorganic semiconductors such as silicon. Semiconductors based on organic molecular components are mainly composed of hydrogen, carbon, and oxygen. Unlike inorganic semiconductors that are crystalline with band-like charge transport, organic semiconductors are amorphous or polycrystalline in which the charge transport occurs through hopping of charges between delocalized molecular orbitals. Organic molecules are weakly bonded to each other through weak van der Waals bonds [9]. Within each semiconducting organic molecule are chains of alternating single and double bonds. By definition, these are conjugated molecules, which results in electrons residing within π-orbitals orthogonal to the plane of the molecule. When multiple molecules are placed in close proximity, overlapping of the π-orbitals occur, enabling the transport of electrons between molecules. As a result, the degree of molecular packing can play an important role in the ease of electron transport. The common thread within the charge transport theory in organic semiconductor is that the overlapping π-orbitals form delocalized states, resulting in the formation of a highest occupied molecular orbital (HOMO) energy band and a lowest unoccupied molecular orbital (LUMO) energy band. In devices, these bands act similarly to the valance and conduction bands of inorganic semiconductor.

In highly purified organic crystals band transport is observed, rendering room temperature mobilities in the range of 1 to 10 cm^2/Vs. In the other extreme, electron-hopping transport is observed in amorphous polymer films. Since hopping (phonon-

assisted tunneling) is thermally activated process, the mobility of these devices is generally dependent on temperature and electric field. Although the exact dependence of the mobility on the electric field depends on the properties of the material, it has been found experimentally in conjugated polymers that the Poole–Frenkel (PF) model in Equation 2.1, often fits the experimental data quite well

$$\mu(E) = \mu_0 \exp(\gamma\sqrt{E}) \tag{2.1}$$

where E is the electric field, and μ_0 and γ are material and temperature dependent parameters [10].

When a positive voltage is applied to the gate, negative charges are induced at the source [11]. For example, as can be seen in Figure 2.1, the LUMO level of pentacene is far away from the Fermi level of gold, so there is a substantial energy barrier for electrons and electron injection is very unlikely. Accordingly, no current passes through the pentacene layer and the small current essentially comes from leaks through the dielectric. In contrast, when the gate voltage is reversed to negative, holes are easily injected because the Fermi level is close to the HOMO level and the barrier height is low. A conducting channel forms at the dielectric-semiconductor interface and charge carriers can easily be driven from source. Because holes are more easily injected than electrons, pentacene is said to be p-type. Note that this concept differs from that of doping in conventional semiconductors. Symmetrically, an organic semiconductor is said to be n-type when electron injection is easier than hole injection, which occurs when the LUMO is closer to the Fermi level than the HOMO. Note that in the terminology of organic light-

emitting diodes, these two classes of materials are often designated ‘‘hole transport’’ (or hole-injecting) and ‘‘electron transport’’ (or electron-injecting) materials.

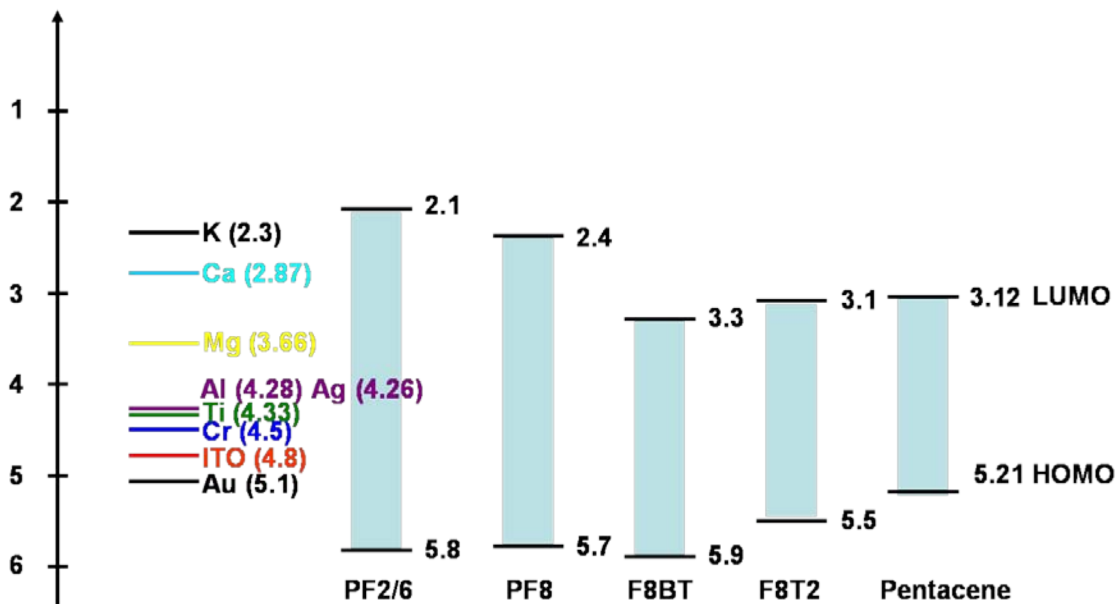


Figure 2.1: Energy scheme of the various metal-organic semiconductor interfaces.

2.1.2. Organic Materials

Organic semiconductors are traditionally classified as polymers or small molecules. An important difference between the two classes of materials lies in the way how they are processed to form thin films. Whereas small molecules are usually deposited from the gas phase by sublimation or evaporation, conjugated polymers can only be processed from solution such as by spincoating or printing techniques. Additionally, a number of low molecular materials can be grown as single crystals allowing intrinsic electronic properties to be studied on such model systems. The

controlled growth of highly ordered thin films either by vacuum deposition or solution processing is still subject of ongoing research, but will be crucial for many applications.

The former have the advantage of being amenable to specific deposition techniques that have been developed for conventional polymers. Their performance is still orders of magnitude lower than that of small molecules. However, encouraging performance has been reported with the latter, although high performance requires high ordering, particularly in the vicinity of the dielectric-semiconductor interface [12]. The importance of high ordering has been recently confirmed by measurements on single crystal devices [13].

1. Polymer

Two polymers are used for most work dealing with polymer-based TFTs- polyfluorene [14, 15] and poly(3-hexylthiophene) (P3HT) [16, 17]. We will only deal with the latter, which affords the highest mobility in currently demonstrated conjugated polymer devices. After pioneering work by Sirringhaus *et al*. [18] on spincoated P3HT, it is now well established that the performance of polymer TFTs critically depends on the chemical and structural ordering of the chains at the dielectric-polymer semiconductor interface. High order first relies on the regio-regularity of the polymer chains; that is, the percentage of regio-regular head-to-tail attachment of the alkyl side chains to the beta position of the thiophene rings [11]. High regio-regularity is not sufficient, however. Two orientations are observed, one with the thiophene rings flat on the surface and the other with the chain edge-on [15]. High mobility, up to 0.1 cm^2/Vs was only found with the latter arrangement. More recently it has been shown that the mobility can be slightly

increased if the film is applied by dip coating instead of spincoating. This is closely related to the limited time available for chain alignment forced by the rapid drying of solvent [19]. However, choosing a high boiling point solvent is another key to improve the field effect mobility with high on-off ratio [20]. Therefore, it must be remarked that the factors affecting orientation and crystallinity of the polymer chains on the substrate are not fully understood.

2. Small Molecule

Pentacene is the material most used for preparation of p-type organic TFTs based on small molecules. The highest reported mobility is up to 6 cm^2/Vs [21]. Major improvements have been achieved by modification of the dielectric-semiconductor interface. Most devices are grown by vapor deposition on silicon oxide. Because of the different physical and chemical nature of both materials, their association may lead to highly disordered interfaces, thus leading to poor performance. Heating the substrate [22] and depositing pentacene thin films at a low rate [23] leads to better organization of pentacene molecules. Choosing a proper gate dielectric is an important way to get high efficient pentacene field effect transistors (FETs) [24]. A better alternative, however, consists in covering the surface of the oxide with an organic self-assembled monolayer before vapor deposition. Thus, octadecyltrichlorosilane (OTS) [25] gave good results with pentacene on SiO_2. An alternative route is to use a polymer dielectric [26] or self-assembled monolayer gate dielectric [27], which resulted in high performance pentacene FETs.

3. N-type Semiconductor

A small number of n-type organic materials in which the conduction is due to the negatively charged carriers have been investigated, including fullerene C_{60} [28], fluorocarbon-substituted thiophene oligomers [29], naphthalene and perylene derivatives [30], etc. The compounds with the highest electron mobility are currently fullerene C_{60}. A major problem with these n-type organic semiconductors is their high sensitivity to ambient conditions, especially oxygen and moisture. Recently, a small number of air-stable n-type compounds have been reported. A prominent aspect that promotes the search for air stable, high mobility n-type organic semiconductors is the possibility of access to organic complementary logic circuitry. Making circuits that combine n-channel and p-channel transistors has many advantages such as high robustness, low power consumption, and low noise [31]. A new concept has recently emerged in the field of organic TFTs, that of ambipolar materials, which can be defined as materials that change type depending on the nature of the contact used to inject charges [32]. Ideally, an ambipolar semiconductor would have a low ionization potential and high electron affinity.

2.2. Properties of the Metal-Oxide-Semiconductor (MOS) Capacitor

2.2.1. Ideal MOS Capacitor

The MOS capacitor is the stack forming the gate in a metal-oxide-semiconductor-field-effect-transistor (MOSFET). The metal provides an electrode at which the voltage can be fixed, and the resulting three components, MOS system is useful in understanding several important integrated circuit structures like MOSFET. The discussion of the MOS system will greatly help us to understand the physical electronics that underlie operation of the MOSFET. Bias applied to the metal contact sweeps the MOS structure through accumulation, depletion, and inversion by controlling the build-up of majority and minority carriers in the semiconductor near the oxide through the field effect. The simulated energy band diagram of the ideal MOS system in thermal equilibrium condition is shown in Figure 2.2. Here, titanium, e-beam grown Al_2O_3, and p-type Si containing N_A of 10^{16} cm^{-3} form an MOS system. The drawing of energy band diagram and next charge distribution analysis were performed with the use of the energy band diagram program software [33].

Some terms in the system will now be defined. E_c and E_v are the conduction and valance band, respectively. Eg is the bandgap of semiconductor, E_F is the Fermi level, E_{Fi} is the intrinsic Fermi level of the semiconductor, and χ_s is the electron affinity of semiconductor. φ_s represents the surface potential and is an important term in describing the state of the MOS stack. φ_f is the distance the Fermi energy from the intrinsic Fermi energy and is dependent on the doping of the semiconductor [34]. Finally, φ_m denotes the work function of metal electrode.

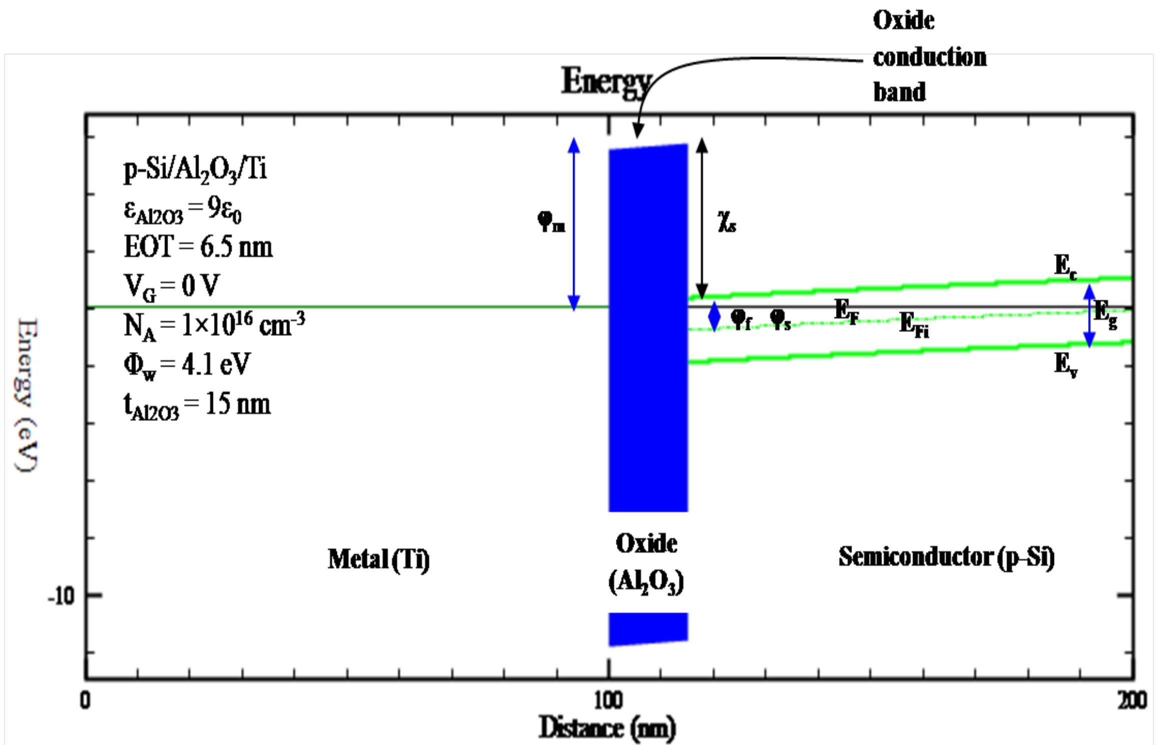
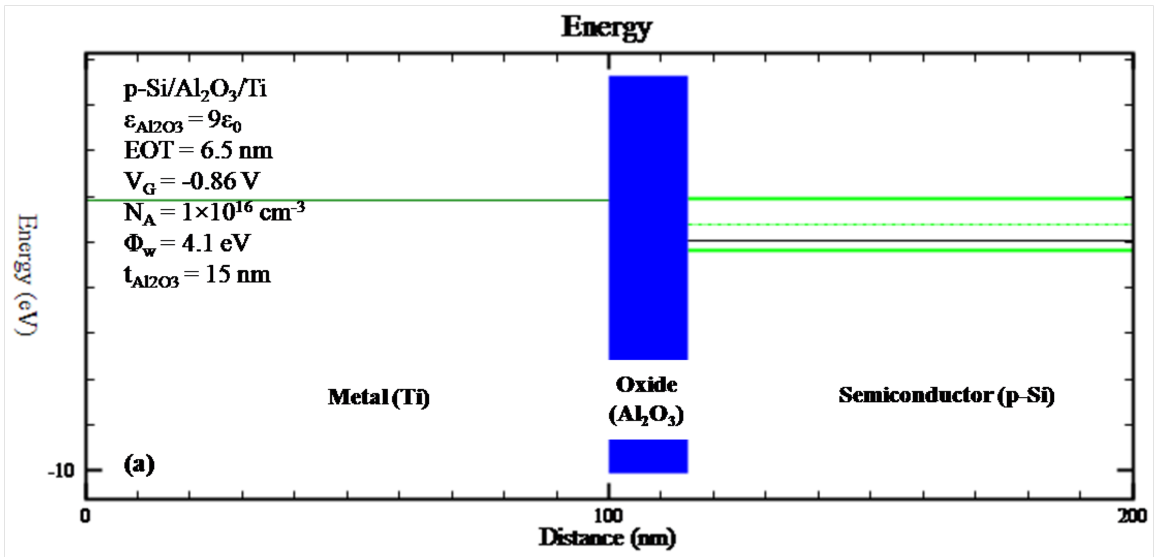
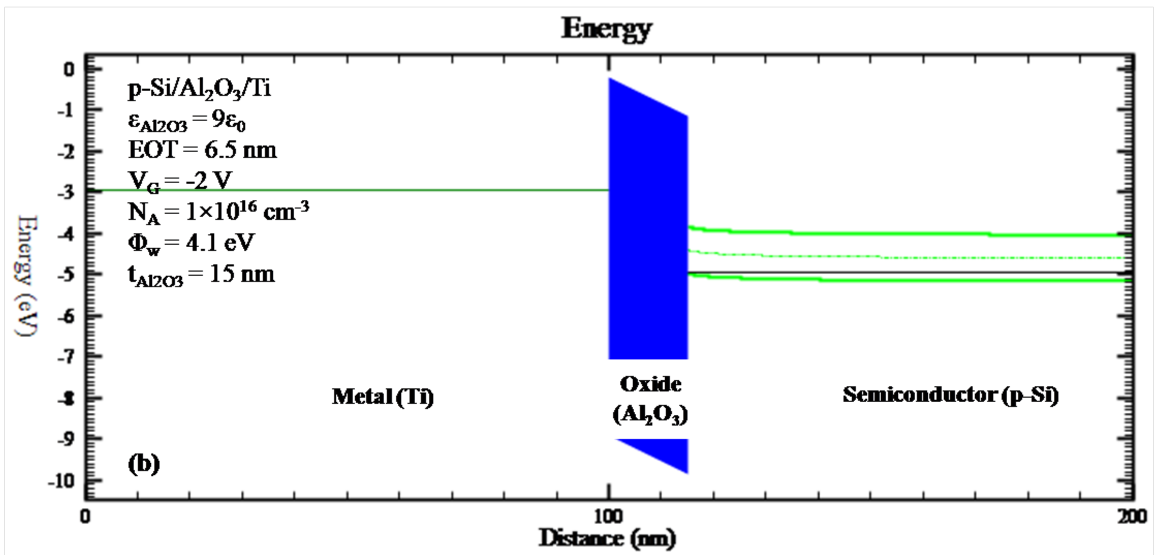


Figure 2.2: Simulated energy band diagram of the ideal p-Si/Al_2O_3/Ti MOS system in thermal equilibrium condition.

A brief discussion on the three modes of operation for a MOS device will now be presented. In *accumulation*, a sufficiently negative charge applied to the gate for a p-type semiconductor results in the attraction of majority carriers to the region directly beneath the field oxide. This maintains the reverse bias between the gate and drain and gate and source, thereby inhibiting conduction from gate to source. As the bias becomes increasingly more positive (negative for a n-type semiconductor), the majority carriers are repelled away from the surface resulting in the establishment of a *depletion* region underneath the oxide. As a result of band bending, the intrinsic Fermi level moves toward the Fermi level. When the bias is strongly positive (or negative for a n-type semiconductor), minority carriers from the semiconductor bulk enter the region just below the oxide and form an *inversion* region. This inversion layer comprised of the minority carriers in the gate semiconductor is of the same polarity as the majority carriers in the drain and source semiconductor. Thus, a conducting channel is formed from the source to drain. The intrinsic Fermi level at inversion is below the Fermi level (in the case of a p-type semiconductor). When intrinsic Fermi level is slightly below the Fermi level at the surface, the electron density in the inversion layer is low and the MOS system is said to be biased in the *weak inversion* region. On the other hand, when the electron density in the inversion layer is greater than hole density in the bulk, and the system is in the *strong inversion* region. [34] Energy band diagrams in the various regions are illustrated in the Figure 2.3 (a-d).


Energy
p-Si/Al2O3/Ti
εAl2O3 = 9ε0
EOT = 6.5 nm
VG = -0.86 V
NA = 1×10^16 cm^-3
Φw = 4.1 eV
tAl2O3 = 15 nm
Energy (eV)
Metal (Ti)
Oxide
(Al2O3)
Semiconductor (p-Si)
(a)
-10
0
100
200
Distance (nm)


Energy
p-Si/Al2O3/Ti
εAl2O3 = 9ε0
EOT = 6.5 nm
VG = -2 V
NA = 1×10^16 cm^-3
Φw = 4.1 eV
tAl2O3 = 15 nm
Energy (eV)
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
Metal (Ti)
Oxide
(Al2O3)
Semiconductor (p-Si)
(b)
0
100
200
Distance (nm)

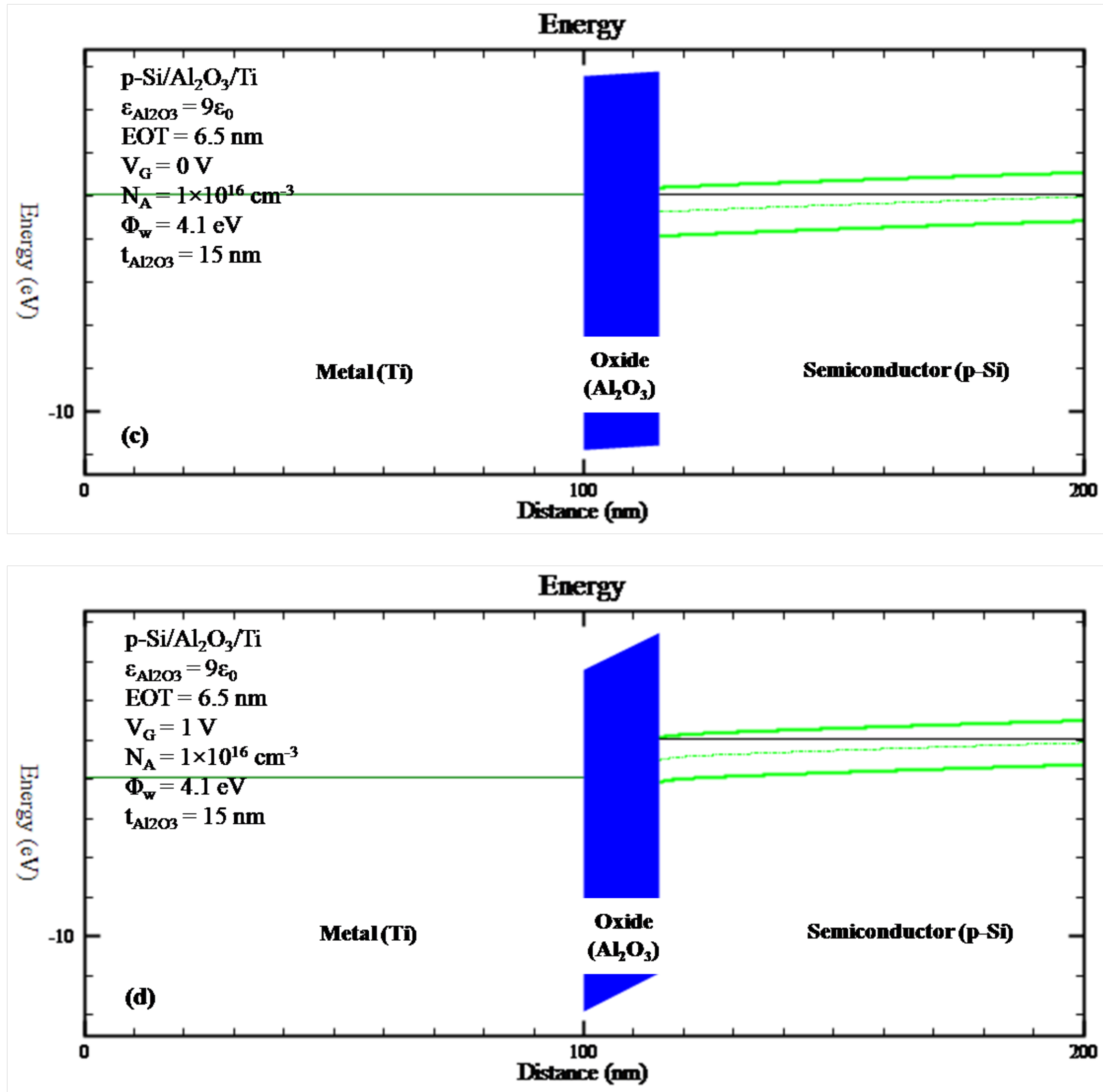


Figure 2.3: Simulated energy band diagram of a MOS system at (a) flatband, (b) accumulation, (c) depletion, and (d) inversion. The system is p-Si/Al_2O_3/Ti.

By definition, the surface potential determines which region of operation a MOS device is in. When φ_s, which is a function of the applied gate bias, is zero, the device is at the flatband condition with a corresponding flatband voltage, V_{FB}. When $\varphi_s = \varphi_f$, the semiconductor near the oxide effectively has the carrier concentrations of intrinsic Si and the device is at midgap. Here, the semiconductor Fermi level position at the oxide interface is equal to the intrinsic Fermi level position. For strong inversion, φ_s must equal twice φ_f. When this occurs, the inversion layer has a minority carrier concentration equal to the majority carrier concentration in the semiconductor far from the interface. That is, the inversion layer has minority carriers of opposite polarity, but equal concentration to the majority carriers in the semiconductor bulk.

We now define V_{FB} and the threshold voltage, V_T. The following derivations are for a p-type semiconductor. Voltage across the gate, V_G, at zero applied bias (in equilibrium), is [35]

$$V_G = V_{OX} + \phi_S + \phi_{ms} \tag{2.2}$$

where V_{OX} is the voltage across the oxide. φ_s is defined as

$$\phi_S = \chi + \frac{E_g}{2q} + \phi_f \tag{2.3}$$

The work function difference between the semiconductor and the gate metal, φ_{ms}, is

$$\phi_{ms} = \phi_m - \phi_s \tag{2.4}$$

If we define Q_i as the net effective fixed charge per unit area in the oxide very near the interface and knowing there is no net charge in the semiconductor, for charge neutrality, we must have

$$Q_i + Q_m^{'} = 0 \tag{2.5}$$

Here, Q_m' is the charge density on the metal. By the definition of capacitance

$$V_{OX} = \frac{Q'_m}{C_{OX}} \tag{2.6}$$

C_{ox} is the oxide capacitance per unit area. By substitution, the flatband voltage is

$$V_{FB} = V_G = \frac{-Q_i}{C_{OX}} + \phi_{ms} \tag{2.7}$$

The threshold voltage is now similarly defined. As mentioned earlier, V_T is the voltage at which the surface potential is equal to twice φ_f. To establish this condition, the charge in the depletion region must be offset in addition to the flatband criteria. Depletion charge density is below and the charge distribution at threshold is shown in Figure 2.4.

$$|Q_D(\max)| = qN_A x_{dT} \tag{2.8}$$

This is a rather straightforward concept as the depletion region charge density per unit area is simply the unit electronic charge times N_A (the doping density of the p-type semiconductor) times the depletion region depth, x_{dT}. q is the electronic charge. From these conditions, the threshold voltage for a p-type semiconductor is

$$V_T = V_G = \frac{|Q_D(\max)|}{C_{OX}} - \frac{Q_i}{C_{OX}} + \phi_{ms} + 2\phi_f \quad (2.9)$$

The charge distribution at threshold is shown in Figure 2.5.

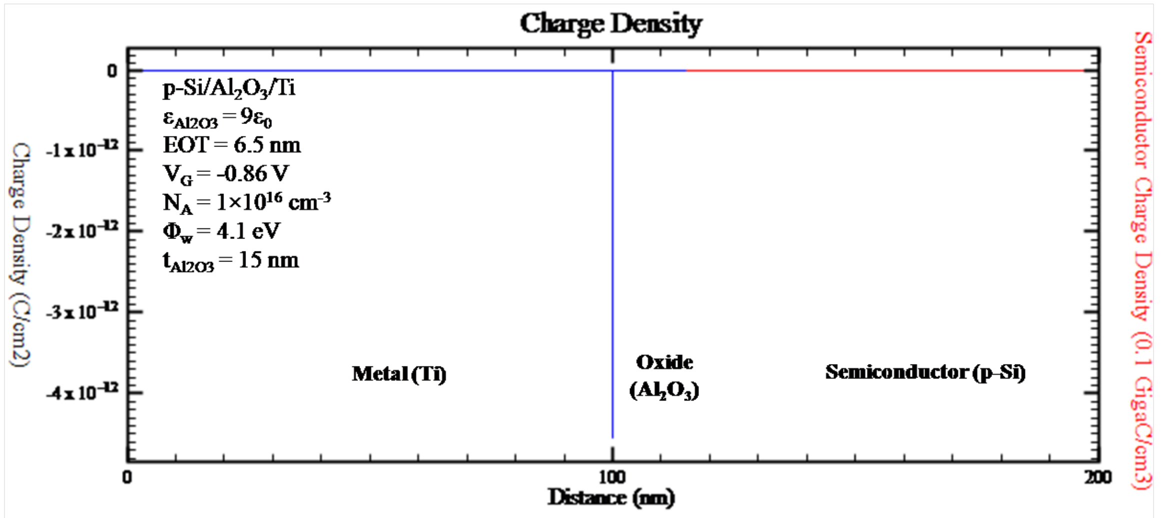


Figure 2.4: Charge distribution in a MOS system at flatband condition.

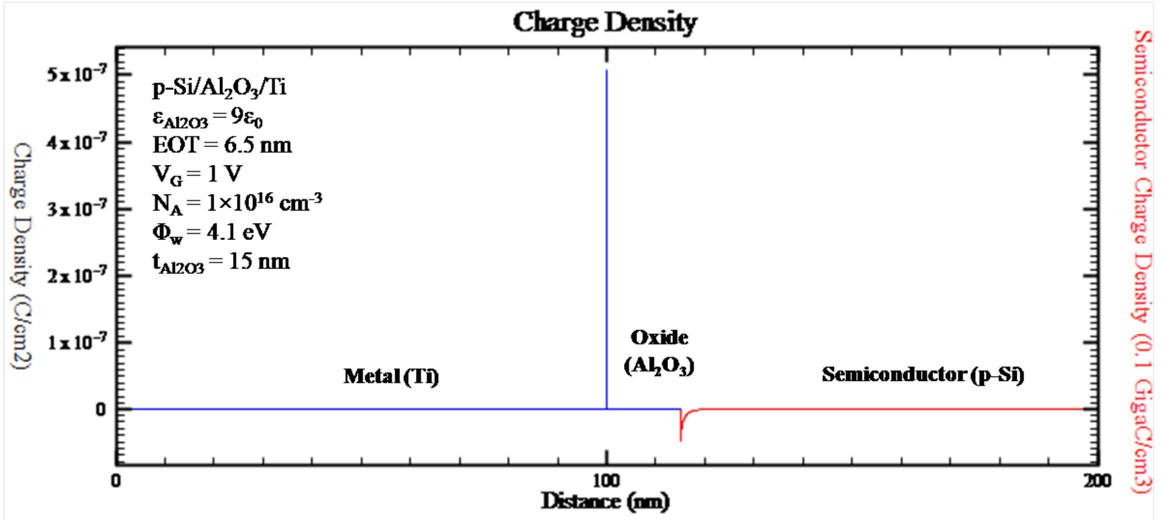


Figure 2.5: Charge distribution in a MOS system at the inversion threshold.

2.2.2. Capacitance of the MOS structure

Devices produced in a MOS fabrication facility are constantly monitored to track the amount and type of oxide charges they contain. In the case of the MOS system, C-V measurement and analysis techniques are standard tools in the diagnosis and monitoring of technology under development or in production. C-V test results offer a wealth of device and process information, including bulk and interface charges. Many MOS device parameters, such as oxide thickness, flatband voltage, threshold voltage, etc., can also be extracted from the C-V data [36]. In this section, we discuss the basic physics behind MOS C-V behavior assuming that the MOS system is ideal and that there are no charges in the oxide or traps at the oxide-semiconductor interface.

The small signal capacitance (per unit area) of a two terminal device is defined as the derivative of the charge Q on the terminals with respect to the voltage V across them,

$$C = \frac{dQ}{dV} \tag{2.10}$$

The free electrons in the metal and the majority carriers in the semiconductor, both being characterized by very small dielectric relaxation times, cannot respond as quickly to a changing voltage, and the associated capacitance can essentially depend on the frequency of the changing applied voltage. One general practical way to implement this is to apply a small AC voltage signal (mV range) to the device under test (DUT), and then measure the resulting current. Integrate the currents over time to derive charge Q and then calculate capacitance from charge Q and voltage. C-V measurements in a semiconductor device are made using two simultaneous voltage sources: an applied AC voltage signal and a DC voltage that is swept in time. The magnitude and frequency of the AC voltage are fixed,

but the magnitude of the DC voltage is swept in time. The purpose of the DC voltage bias is to allow sampling of the material at different depths in the device. The AC voltage bias provides the small signal bias so the capacitance measurement can be performed at a given depth in the device [36].

The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. Figure 2.6 illustrates a high frequency C-V curve for a p−type semiconductor substrate. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

In accumulation state, electrostatic forces from the gate voltage pull the excess holes at the semiconductor surface very close to the oxide. The oxide capacitance is measured in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the C-V curve is almost flat. This is where the oxide thickness can also be extracted from the oxide capacitance. Thus, the capacitance per unit area in accumulation (C_{ox}) approaches

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.11}$$

where ε_{ox} is the dielectric constant of oxide, t_{ox} is the oxide thickness, respectively. However, for a very thin oxide, the slope of the C-V curve does not flatten in accumulation and the measured oxide capacitance differs from the actual oxide capacitance [37].

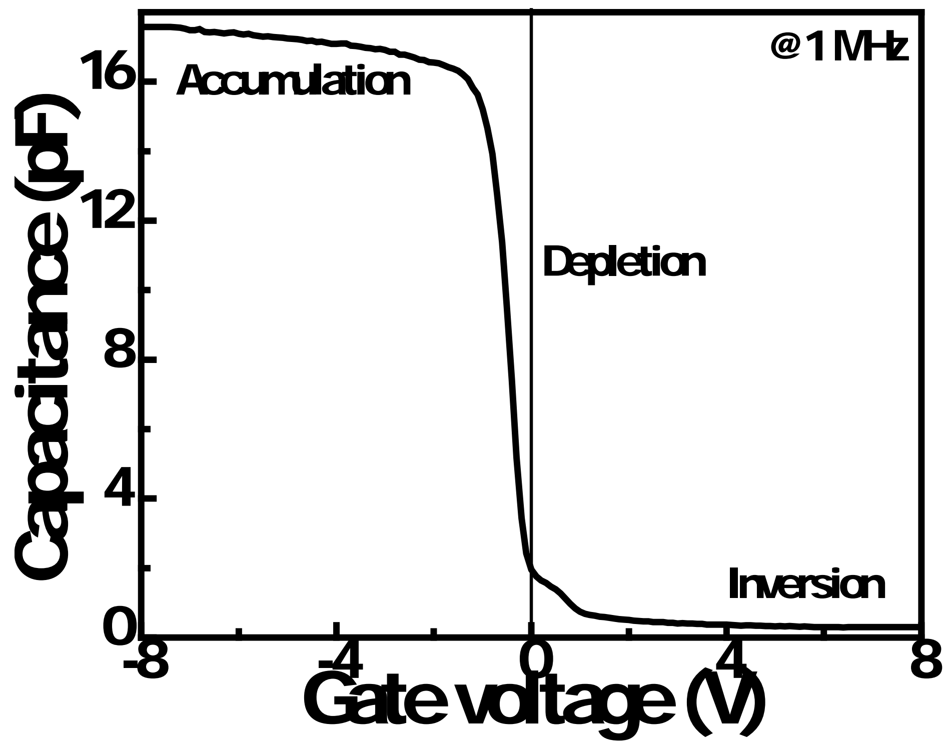


Figure 2.6: C-V curve of p-Si/Al_2O_3 (15 nm)/Ti MOS capacitor measured at 1 MHz.

When the gate voltage approaches the flatband voltage, the surface accumulation vanishes, and the capacitance decreases as the Debye length at the surface increases. It is important to define flatband capacitance, C_{FB}, as the capacitance measured when the gate voltage is flatband voltage and can be express as

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_s}} \tag{2.12}$$

where L_D is the extrinsic Debye length and ε_s is the dielectric constant of semiconductor. L_D is calculated as below,

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 N_A}} \tag{2.13}$$

where k is Boltzmann constant and T is absolute temperature.

The depletion region of the C-V curve, where the capacitance changes rapidly with the gate voltage, contributes to a depletion capacitance and further separating the effective capacitor plates. The total measured capacitance now becomes in series connection of the oxide capacitance and the depletion layer capacitance, and as a result, the measured overall capacitance decreases. The depletion region starts at a voltage defined by the flatband voltage. The capacitance decreases till the depletion width reaches a maximum and inversion sets in. The effective value of capacitance is now given by

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s}} \tag{2.14}$$

where C_s is the capacitance across the depletion region.

In the inversion region, the value of the capacitance depends on whether the measurements are conducted at low frequency (0.01 to ~1 Hz) or at high frequency (~1 MHz), where “low” and “high” are with respect to the generation-recombination rate of the minority carriers in the inversion layer. When measured at high frequency, the relatively sluggish generation-recombination process will not be able to supply minority carriers in response to the applied AC signal. The number of minority carriers in the inversion layer therefore remains fixed at DC value. On the other hand, if the measurement frequency is low, minority carriers can be generated in response to the applied AC signal and hence the capacitance increases [35]. At strong inversion, the minority carriers become more significant and hence the capacitance is only due to the inversion capacitance.

Practically, given modern MOS capacitors with their long carrier lifetimes and low carrier generation rates, even probing frequencies as lows as 1 Hz, the practical limit in bridge-type measurements will produce high frequency type characteristics. Thus, indirect means such as the quasi-static technique must be employed if low frequency C-V measurement is required. In the quasi-static technique a slow liner voltage ramp is applied to the gate and the current into the gate is monitored as a function of gate voltage [38].

2.2.3. Non-ideal Effects

The theory presented to this point has not considered an important characteristic of the oxide-semiconductor system, the influence of charges within the oxide and at the oxide-semiconductor interface. The presence of these charges is unavoidable in practical system and a real MOS system usually deviates from theoretical behavior as the result of oxide charges and interface trapped charge. Interface trapped charge will be discussed in greater detail in the next chapter.

Oxide charges fall into one of three categories: oxide fixed charge, oxide trapped charge, and mobile ions [39]. Fixed charge, Q_f, is independent of oxide thickness as it is located very near the oxide-semiconductor interface (within 30 Å), but entirely within the oxide. It is not dependent on the semiconductor doping, but is dependent on the crystalline orientation and the condition of oxide deposition and annealing. A positive Q_f results in a negative V_{FB} shift and a negative Q_f results in a positive V_{FB} shift. This can be more clearly explained considering charge neutrality. If a negative bias is applied at the gate, then this charge must be compensated by positive charge somewhere along the MOS stack. Ideally, when Q_f is 0, this charge is compensated entirely by donors in the semiconductor. However if a positive fixed charge is present, then this will partially compensate some of the negative gate charge [35]. This reduces the number of donors in the semiconductor that are required to compensate the charge at the gate and thus reduces the depletion region width. A narrower depletion region raises overall MOS capacitance (since the MOS capacitance is the series combination of the oxide and depletion capacitances), producing a positive C-V shift. The opposite is the case for negative fixed charge. The flatband voltage shift due to fixed charges is given as follows

$$\Delta V_f = \frac{Q_f}{C_{OX}} \tag{2.15}$$

Oxide trapped charges, Q_t, are electrically neutral sites distributed throughout the oxide that can be charged with the introduction of electrons or holes. Charge can become trapped in the oxide during device operation even if not introduced during device fabrication. Energetic radiation also produces electron-hole pairs in the oxide and some of these electrons or holes are subsequently trapped in the oxide. These sites are usually caused by defects in the oxide bulk. They also cause a voltage shift as follows

$$\Delta V_t = \frac{Q_t}{C_{OX}} \tag{2.16}$$

Here, Q_t is the effective bulk oxide trapped charge density per unit area present at the interface. Usually, the presence of charged traps in the bulk dielectric causes the high frequency C-V plot to shift in parallel to the ideal curve. The shift in flatband voltage, called hysteresis, is used in Equation 2.16 to calculate the trapped charges in the dielectric, Q_t.

Mobile charges are typically alkali ions such as sodium and potassium [40]. They are unintentionally introduced during device fabrication as the result of contamination. Unlike the trapped and fixed charges, which are located at a single site, mobile ions move about within the oxide. This results in a bias and bias sweep direction dependent voltage shift or hysteresis. Similar to the localized charges, the voltage shift is given by

$$\Delta V_m = \frac{Q_m}{C_{OX}} \tag{2.17}$$

Again, it should be noted that Q_m is the mobile charge density per unit area. A widely used technique to measure the mobile charge density in the oxide the "bias-temperature" test, in which a field is applied across the structure at an elevated temperature to move the mobile ions and changes their effect on flatband voltage; the C-V curve is subsequently measured at room temperature. The high temperature bias is then applied in the opposite direction, followed by another C-V measurement at room temperature. The hysteresis of the C-V curves indicates the amount of mobile oxide charges [34].

The total flatband voltage shift due to oxide charges is the sum of these three individual voltage shifts.

$$\Delta V_{FB} = \Delta V_f + \Delta V_t + \Delta V_m \tag{2.18}$$

Therefore, the total flatband voltage shift is

$$\Delta V_{FB} = -\frac{Q_f + Q_t + Q_m}{C_{OX}} + \phi_{ms} \tag{2.19}$$

This is simply an expansion on Equation 2.7. Overall, various sources of charges in the oxide and at the interface are shown in Figure 2.7.

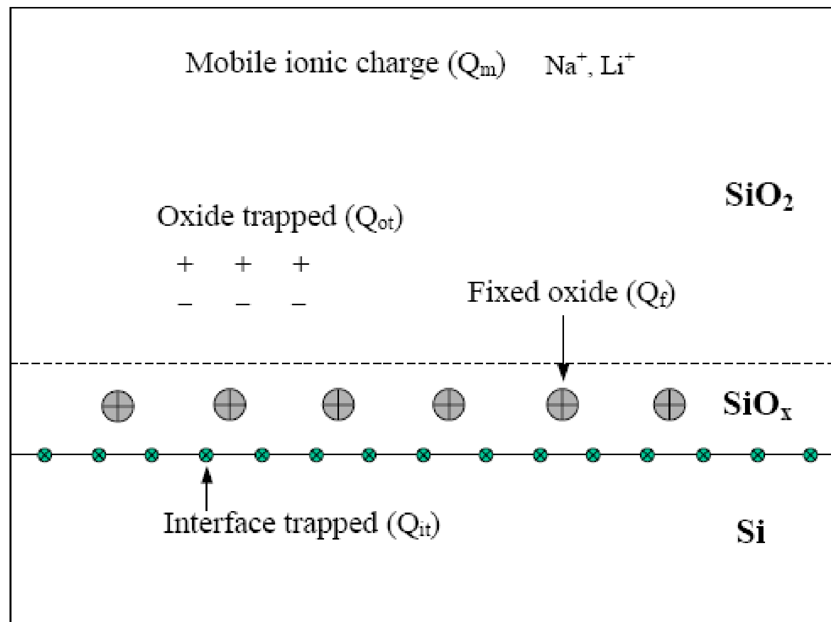


Figure 2.7: Definitions of charge densities (C/cm^2) associated with thermally oxidized silicon [41].

2.2.4. Analysis of Interface Trap States

Interface trap states arise from the abrupt termination of the crystalline Si lattice. The trap charge is a quantity Q_{it}. Q_{it} are states existing within the bandgap of Si. It was shown that this charge is directly related to surface density of Si atoms (~10^{15} cm^{-2} on Si (100)) with measurements on clean Si surfaces in an ultra high vacuum environment [42]. Typically, dielectric deposition on the Si surface and annealing satisfies most of the charge, thereby reducing this state density by several orders of magnitude, typically to the 10^{10}-10^{12} eV/cm^2 range. States are either donors or acceptors. Since interface traps are located in the semiconductor bandgap at the oxide-semiconductor interface, their position relative to the Fermi level is affected by band bending. By varying the bias, trap occupancy as governed by the Fermi-Dirac probability function, can be altered. This is also schematically illustrated in Figure 2.8.

When an small AC signal (~30 mV) is superimposed onto the DC bias, the traps very near the Fermi level will be forced to change occupancy as the Fermi level oscillates above and below these trap levels. While the band structure itself can respond instantaneously to this varying bias, the interface traps cannot. There is a lag between the time the Fermi level crosses below an occupied trap and the time at which that trap actually empties. This charge storing characteristic results in a capacitance, C_{it}, measured in parallel with the depletion capacitance. There is a time constant associated with this lag. Also, the filling and emptying of traps with carriers results an energy loss, which must be supplied by the measuring instrument and is observed as a parallel conductance,

G_p [49]. Other factors such as series resistance and leakage can also contribute to energy loss and care should be taken to either correct for or eliminate them.

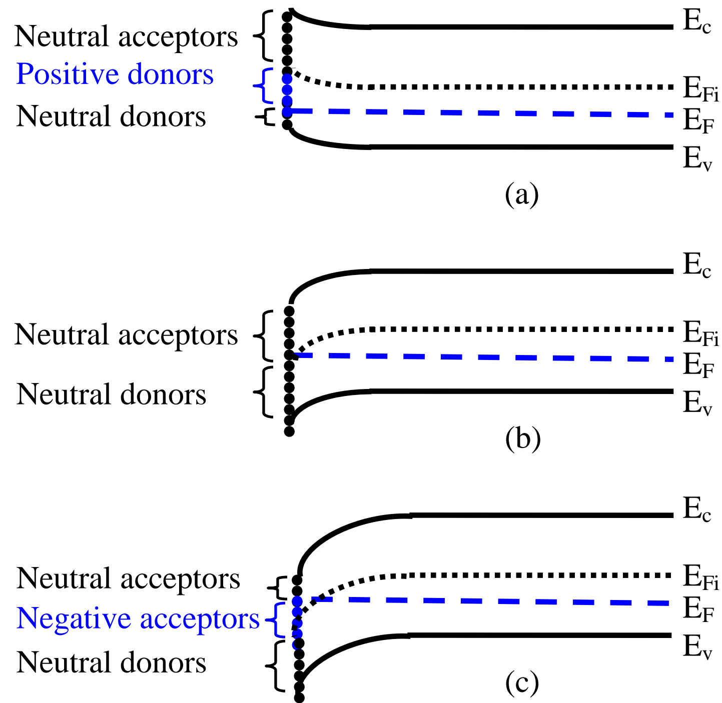


Figure 2.8: Interface trap occupancy relative to the Fermi level at (a) accumulation, (b) midgap, and (c) inversion.

Several different techniques have been developed to quantitatively measure the interface trap density. These includes the Terman and Lehovec methods [43, , and 45], where the measured high frequency C-V curve of the MOS capacitor is compared with the corresponding theoretical C-V curve calculated for the same capacitor assuming that the MOS system is ideal. Interface traps also could be calculated using the fact that interface trap cause an offset in between low and high frequency C-V plots. This offset can be utilized to calculate interface trap density from the measured high frequency capacitance and low frequency capacitance at a certain gate bias [46]. Further information regarding the use of above-mentioned and other methods is referred to the appropriate text [47].

For the work presented here, the conductance method proposed by Nicollian *et al.* was used which is described in this chapter [48, 49]. Among several techniques available for estimating the interface trap density (D_{it}), the conductance technique involving point-by-point determination of interface trap density throughout the depletion region gives reliable D_{it} values. The loss is dominated by majority carrier transitions at the traps and there is a small signal frequency at which it is comparable to the majority carrier transition time constant. The conductive response of the interface traps is directly related to the trap time constants as proposed by Nicollian and Goetzberger and can be used to reveal the trap density as well as the time constants.

When a group of traps have linked capacitances and capture resistances, they behave as one trap of one energy level, yielding the single time constant (STC) model. The equivalent circuit of this model is as follows,

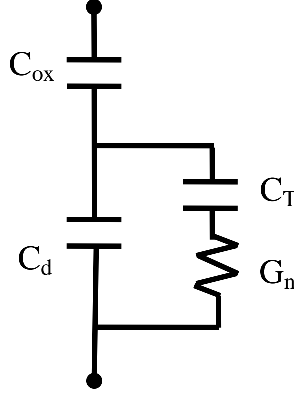


Figure 2.9: Equivalent circuit for STC model. Note the device is in depletion. The series combination of C_T and G_n forms the trap admittance Y_{it}.

The admittance of the STC traps, Y_{it}, is given by

$$Y_{it} = \frac{\omega^2 \tau C_{it}}{1+\omega^2\tau^2} + j\frac{\omega C_{it}}{1+\omega^2\tau^2} \tag{2.20}$$

which is of the general form

$$Y_{it} = G_p + j\omega C_p \tag{2.21}$$

According to the STC model the equivalent parallel conductance of a single level interface state characterized by the time constant τ can be written as

$$\frac{G_p}{\omega} = \frac{qD_{it}\omega\tau}{(1+\omega^2\tau^2)} \tag{2.22}$$

where τ is the time constant of the interface state and G_p/ω is maximized for $\omega\tau = 1$ in the STC model. The usual Si/SiO_2 MOS device shows excellent agreement with the above equation in the bias region corresponding to weak inversion of the silicon surface.

When the interface traps have energy levels so closely spaced across the bandgap that they are a virtually continuous distribution, it gives rise to the continuum of states model.

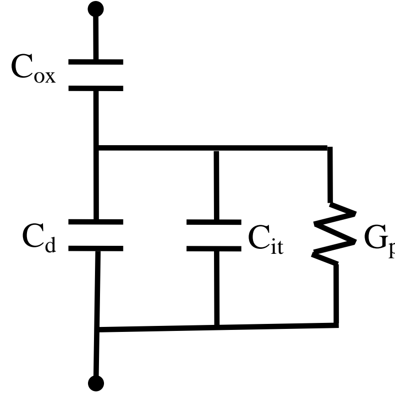


Figure 2.10: Equivalent circuit for continuum of states model. Note again the device is in depletion.

The admittance of the continuum of states model is

$$Y_{it} = \frac{C_{it}}{2\tau}\ln(1+\omega^2\tau^2) + j\frac{C_{it}}{\tau}\tan^{-1}(\omega\tau) \tag{2.23}$$

From this for the continuum of states model

$$\frac{G_p}{\omega} = \frac{qD_{it}\ln(1+\omega^2\tau^2)}{2\omega\tau} \tag{2.24}$$

G_p/ω is maximized for $\omega\tau = 1.98$ in the continuum of states model and for the depletion region, Si/SiO_2 device exhibits large dispersion of time constants.

The measured capacitance and conductance are used to extract G_p in the depletion region as given by

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.25}$$

To calculate D_{it} using G_p, two models either STC model or the continuum of states model is used to fit the experimental data. At each fixed bias, the maximum value of G_p/ω is plotted against frequency, and the peak maximum and the corresponding frequency are recorded. These values are then re-substituted into the Equations 2.22 and 2.24 to evaluate D_{it} and to generate the theoretical G_p/ω versus frequency plots. A complete derivation of both of these models is presented in [49].

To effectively perform C-V and G-V analysis, the data must typically be corrected for the presence of series resistance, R_s. The rise in conductance in the accumulation region and the loss of peak for the higher frequency curves is due to presence of high series resistance effects masking the losses due to interface traps [50]. If the measured admittance across the probe terminals is

$$Y_{ma} = G_{ma} + j\omega C_{ma} \tag{2.26}$$

The $_{ma}$ subscript denotes measured in accumulation. Then, the inverse of the admittance is the impedance, Z_{ma}, of which the real part is the resistance, R_s. The set of equations for corrected capacitance, C_c, and conductance, G_c, at a particular frequency measured across the terminals of the MOS capacitor are given by are as follows

$$R_s = \frac{G_{ma}}{G^2{}_{ma} + \omega^2 C^2{}_{ma}}$$

$$a = G_m - (G^2{}_m + \omega^2 C^2{}_m)R_s$$

$$C_c = \frac{(G^2{}_m + \omega^2 C^2{}_m)C_m}{a^2 + \omega^2 C^2{}_m}$$

$$G_c = \frac{(G^2{}_m + \omega^2 C^2{}_m)a}{a^2 + \omega^2 C^2{}_m} \quad (2.27)$$

R_s is found using the accumulation capacitance and conductance values at 1 MHz and this value is thereafter used as a constant at all lower frequencies. It is typically less than 1 kΩ for low doped substrates and can be less than 100 Ω for heavily doped substrates.

2.3. Non-volatile Memory

Memory can be split into two main categories: volatile and non-volatile. Volatile memory loses any data as soon as the system is turned off and thus it requires constant power to remain viable. Most types of random access memory (RAM) fall into this category. Non-volatile memory does not lose its data when the system or device is turned off. A non-volatile memory device is a MOS transistor that has a source, a drain, an access or a control gate, and a floating gate. It is structurally different from a standard MOSFET in an existence of floating gate, which is electrically isolated, or "floating". Non-volatile memories are sub-divided into two main classes: floating gate and charge-trapping. Important classes of non-volatile memory storage elements using the MOSFET structure are floating gate MOS devices first proposed by Kahng and Sze [51]. In this memory, electrons were transferred from the floating gate to the substrate by tunneling through a 3 nm thin SiO_2 layer. Tunneling is the process by which a non-volatile memory can be either erased or programmed and is usually dominant in thin oxides of thicknesses less than 12 nm. Storage of the charge on the floating gate allows the threshold voltage to be electrically altered between a low and a high value to represent logic 0 and 1, respectively.

In floating gate memory devices, charge or data is stored in the floating gate and is retained when the power is removed. All floating gate memories have the same generic cell structure. They consist of a stacked gate MOS transistor as shown in Figure 2.11. The first gate is the floating gate that is buried within the gate oxide and the inter-polysilicon dielectric (IPD) beneath the control gate. The IPD isolates the floating gate and can be oxide or oxide-nitride-oxide (ONO). The second gate is the control gate which is the

external gate of the memory transistor. A floating gate device is at the heart of erasable-programmable read-only memories (EPROM). EPROMs that are electrically erasable are known as EEPROMs, and flash memory is a derivative of EEPROMs.

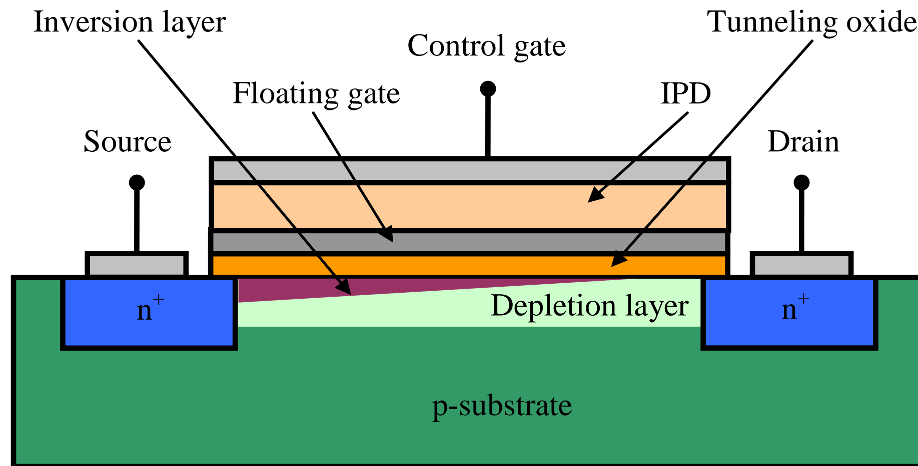


Figure 2.11: Floating gate device. The lower gate is the floating gate and the upper gate is the control gate. IPD is the inter polysilicon dielectric.

The working principle behind EEPROM is charge stored in the floating gate alters the threshold voltage of the transistor. In a manner similar to how oxide charges produce a C-V curve shift in MOSFET devices, charges on the floating gate alter the turn on characteristics of the floating gate device. The charging, storage, and erase band diagrams are shown in Figure 2.12.

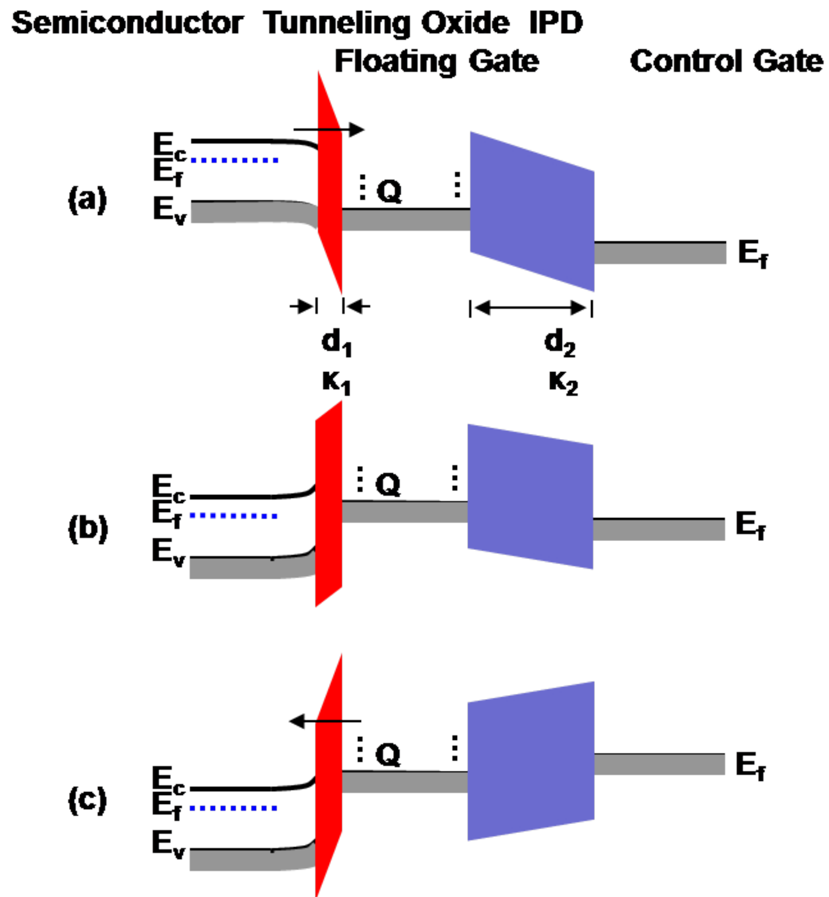


Figure 2.12: Floating gate structure in (a) charging, (b) storage, and (c) discharging.

Under thermal equilibrium conditions, the floating gate is isolated from both the control gate and the substrate by the dielectrics. However, when a large bias is applied to the control gate, the two insulating layers will undergo band bending. The thinner tunneling oxide will undergo more severe band bending and charges in substrate can tunnel through the very thin tunneling oxide and be trapped by the floating gate which is the discrete nanoparticle in our case. The mechanism is the Fowler-Nordheim (F-N) tunneling described as follows [52]. From the Schrödinger equation, we know that there is a finite probability that a particle can tunnel through a non-infinite barrier. As the barrier width decreases, the probability of a particle penetrating it rises exponentially. In sufficiently thin oxides (below 15 Å), direct quantum mechanical tunneling through the barrier can occur. Also, under oxide band bending, electrons can more readily penetrate a barrier giving rise to F-N tunneling or field emission. F-N tunneling can occur even in thicker oxides under sufficient band bending. Direct and F-N tunneling are similar in nature, with the basic difference being that direct tunneling occurs through the trapezoidal barrier and F-N tunneling occurs through the upper triangular barrier. In conventional MOSFETs, both tunneling mechanisms can greatly increase oxide leakage currents. Figure 2.13 shows both tunneling mechanisms.

Because the oxide layer above the floating gate is thicker (such that tunneling is not prominent), the charges remain trapped at the floating gate, increasing the threshold voltage. The device can now be “read” by checking its threshold voltage. To erase the device, the gate bias is reversed, thereby allowing charge trapped on the gate to tunnel back into the substrate, restoring the threshold voltage to the lower state.

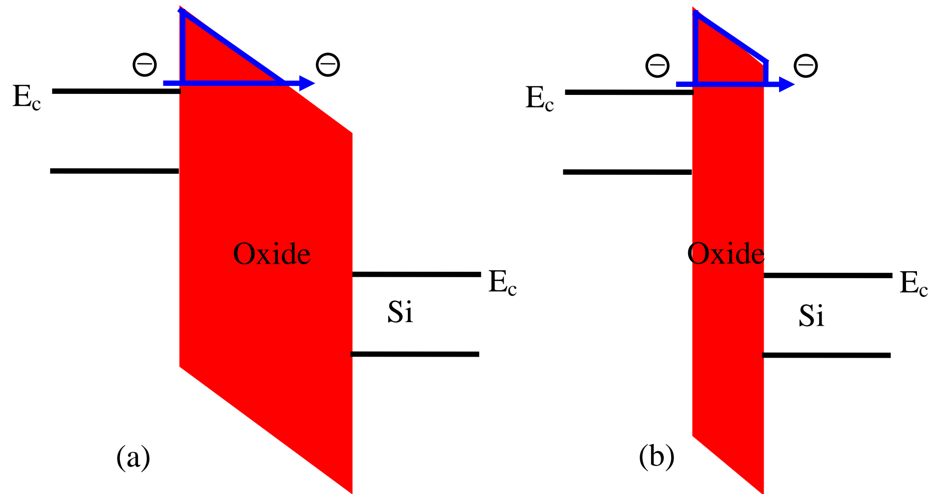


Figure 2.13: Tunneling mechanisms through a MOS oxide. (a) Fowler-Nordheim tunneling and (b) direct tunneling.

Tunneling oxide selection is largely dictated by the band offsets and leakage properties of the material. High-*k* dielectrics are of interest in floating gate memory devices. Here, the lower band offsets of high-*k* oxides such as Al_2O_3 or HfO_2 can actually be advantageous as it allows for lower operating voltages and thicker tunneling oxides, reducing leakage currents [53]. Consequently, such devices can be programmed using lower voltages, at faster speeds and retain the data for longer periods of time. Interesting multi-layer dielectrics comprised of oxides with different dielectric constants and bandgaps have even been proposed to tune the program/erase (P/E) characteristics of the tunneling oxide [54]. Moreover, the trade-off between P/E speeds and data retention is still an important issue in the application of the floating gate non-volatile memory. One promising way to solve this issue is through bandgap engineering of the tunnel oxide with an asymmetric barrier which typically consists of doubly stacked dielectric layers with a high barrier adjacent to the substrate and a low barrier to the floating gate [55].

Unfortunately, some drawbacks may still exist. Take the two layer tunnel oxide of HfO_2/SiO_2, for example. Due to the relatively low barrier height and easily crystallized structure of HfO_2, its ability to suppress leakage by either thermionic emission or grain boundary conduction would be low. In contrast, if the high barrier oxide of Al_2O_3 in amorphous structure was used instead of HfO_2, a good charge retaining could be obtained, but the tunneling efficiency will be decreased substantially as the overall barrier profile is too high to induce a F-N tunneling at a moderate voltage. In order to solve this problem, there are lots of researches going on about bandgap engineering of tunnel oxide with a multi-stacked concave barrier, from which the effective thickness of the tunneling barrier can be greatly reduced under a moderate bias, while a thick and high barrier is retained for charge retention.

2.4. Characterization Tools

2.4.1. Ellipsometry

All film thickness measurements were done ex-situ with a J. A. Woollam variable angle spectroscopic ellipsometer (V.A.S.E). Ellipsometer is a non-destructive, but a very sensitive optical measurement technique that uses polarized light to characterize thin films, surfaces, and material microstructure. Linearly polarized, monochromatic light incident on a surface is reflected and elliptically polarized. The incident light on a thin film is either reflected off the film surface or is refracted into the film and undergoes internal reflections within the film before being absorbed by the substrate or emerging from the film. By measuring the polarization change, properties of the film including thickness and refractive index can be extracted.

Many simple samples may be characterized by ellipsometric measurement as a single wavelength. However, variable angle spectroscopic measurements provide much more information about the sample, and also provide the ability to acquire data in spectral regions where the measured data are most sensitive to the model parameters which are to be determined [56]. Our ellipsometry tool, V.A.S.E, is a versatile ellipsometer for research on all types of materials and it combines high accuracy and precision with a wide spectral range up to 193 to 2500 nm. Variable wavelength and angle of incidence allow flexible measurement capabilities from generalized ellipsometry to reflection and transmission ellipsometry.

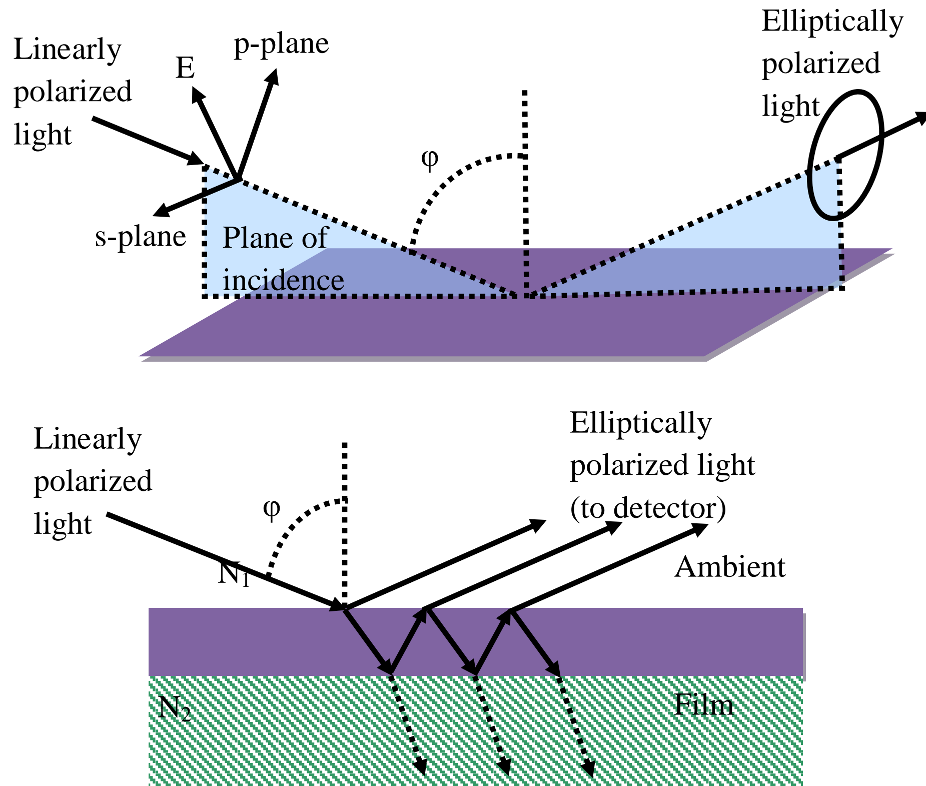


Figure 2.14: Geometry of ellipsometer measurement.

The general setup of an ellipsometer is shown in Figure 2.14. Ellipsometer is an optical instrument used to measure polarization states changes upon reflection. An ellipsometer consists of several optical components that come with many different set of configurations. All ellipsometer configurations consist of four basic optical device elements: light source, polarizer, analyzer, and detector. The direction parallel to the plane of incidence is the p-plane and the direction normal to it is the s-plane. N is the complex index of refraction and is equal to n + jk, where n is the index of refraction and k is the extinction coefficient. N varies for each material and is wavelength dependent. If

the two Fresnel reflection coefficients (the ratios of incident and reflected light) in the p and s directions are r_p and r_s, then

$$\frac{r_p}{r_s} = \rho = \tan(\Psi)e^{j\Delta} \tag{2.28}$$

where tan Ψ is the amplitude ratio ($|r_p|/|r_s|$) and Δ is the phase difference ($\delta_p - \delta_s$). V.A.S.E. does not measure the individual Fresnel coefficients, but rather the ratio ρ. A model is then used to fit the experimental Ψ and Δ values to those of known materials and/or Cauchy layers. Recursive methods are used to determine the model parameters (n, k, and thickness) for each layer. For material layers, the refractive indexes (and extinction coefficients) at various wavelengths are known and the thickness is determined. In a Cauchy layer the wavelength dependent refractive index is of the form as below

$$n(\lambda) = n_0 + \frac{n_1}{\lambda^2} + \frac{n_2}{\lambda^4} \tag{2.29}$$

where n_0, n_1, and n_2 are known as Cauchy coefficients. n_0 is the constant that dominates $n(\lambda)$ for long wavelengths, n_1 controls the curvature of $n(\lambda)$ in the middle of the visible spectrum, and n_2 influences $n(\lambda)$ to a greater extent in shorter wavelengths. The parameters n_0, n_1, n_2 and thickness of the film are used to calculate Ψ and Δ values. It is used in cases where the film is of unknown type. The coefficients (n_0, n_1, and n_2) are varied and thus both the refractive index and thickness are solved for simultaneously. A graded Cauchy layer used for depth profiles is comprised of multiple discrete Cauchy layers, each with its own refractive index and thickness.

Many films can be described with as Cauchy relationship for the longer wavelength region, but cannot be described adequately in the lower visible or UV region. Usually, the ellipsometer data taken with polymer films is fitted with one or several oscillators to more closely emanate the experimental data.

2.4.2. Electrical Characterization

An inductance-capacitance-resistance (LCR) meter and sourcemeter were utilized for all electrical measurements of devices. The HP 4284A LCR meter is capable of measuring two parameters simultaneously including C-V and G-V. It can provide a ±42 V DC bias and an AC small signal frequency ranging from 20 Hz to 1 MHz. Note that we have checked dissipation factor before C-V measurement to ensure that the overall quality of dielectric stack is satisfied with the requirement ($D < 0.1$). In addition, successful measurements require compensating for stray capacitance and measuring at equilibrium conditions, which is described as below.

C−V measurements on a MOS capacitor are typically performed on a wafer using a prober. The LCR meter is designed to be connected to the prober via interconnect cables and adaptors. This cabling will add stray capacitance to the measurements. To correct for stray capacitance, the LCR meter has a built-in tool for offset correction: the corrections for OPEN or SHORT depending on the impedance of DUT.

MOS capacitor takes time to become fully charged after a voltage step is applied. C−V measurement data should only be recorded after the device is fully charged. This condition is called the equilibrium condition. Therefore, to allow the MOS capacitor to reach equilibrium, first allow a sufficient hold time to enable the MOS capacitor to

charge up, and second, allow a sufficient sweep delay time before recording the capacitance after each voltage step of a voltage sweep [36].

The Keithley 2400 sourcemeter is capable of a ±200 V DC bias and can source or sink 1 A, up to a maximum of 20 W. It was used for all medium level current-voltage (I-V) measurements. HP 4145A semiconductor parameter analyzer is used to measure low level current measurements below 1 pA of all organic MOS devices. It can provide a ±42 V DC bias and support 4 source-measure units (SMUs) and 2 voltage and current sources, respectively. The illustration of the experimental set-up along with a device under test is shown in Figure 2.15.

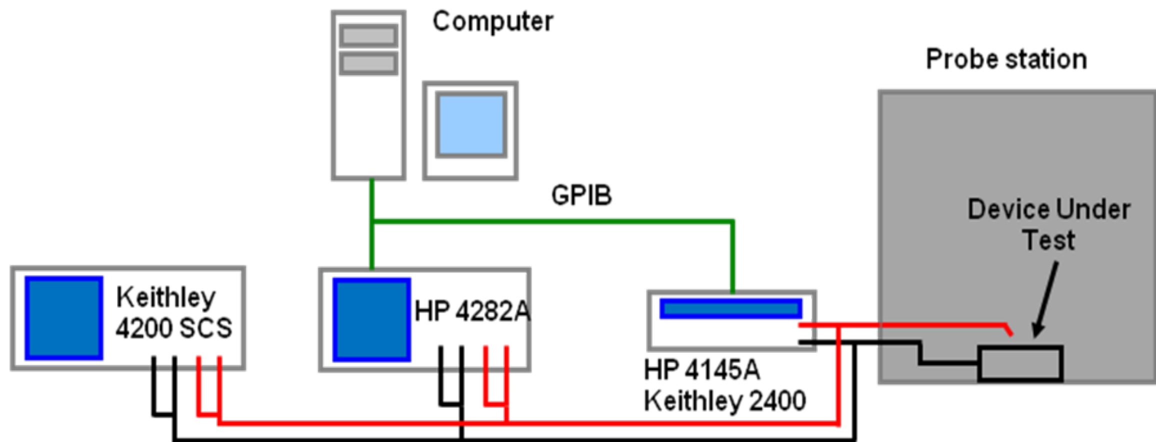


Figure 2.15: Experimental set-up and device structure under test.

The probe station is kept inside the light tight enclosure (LTE) to prevent measurements from external light and electromagnetic waves. The probe station consists of micromanipulators that can move probes in three axes and a linear translation stage positioned on a portable air table to lower the vibration. The shielded/guarded cables and

wires are connected from the probe station to the equipments. For the devices with a backside common gate, the samples are connected by a gate chuck connected to a source meter by shielded coaxial cables. All measurements and data acquisition are automated using customized National Instruments LabView® codes running on a computer via GPIB interface control.

Lastly, Keithley 4200 Semiconductor Characterization System (SCS) is used to fully characterize non-volatile Flash memory devices such as memory window, endurance, retention, and P/E transient characteristics. The Keithley 4200 SCS system with connected to Signatone WL210E probe station via all triaxial cables can also measure sub-femto ampere measurement resolution with added module and allows characterizing both standard and exotic devices in ultra low level phenomena. In addition, the Keithley 4200-CVU Integrated C-V Option speeds and simplifies the process of making C-V measurements, offering users the advantages of intuitive point-and-click setup, complete cabling, and built-in element models, taking the guesswork out of obtaining valid C-V measurements. The software incorporates C-V tests, which include a variety of complex formulas for extracting common C-V parameters. The 4200 SCS can also bring together I-V, C-V, and pulse testing capabilities in one easy-to-use tool that can support all of our lab's characterization, modeling, and reliability testing needs [36].

Chapter 3. C-V Characterization of PF-based MOS Structure

3.1. Introduction

Polyfluorenes (PFs) have emerged as attractive alternatives to other conjugated polymers for applications in light-emitting displays [57] and thin film transistors [58] due to efficient blue emission, relatively high charge carrier mobility [15], and excellent chemical and thermal stability [59]. Polyfluorene derivatives utilize solubilizing side chain substituents to mould the explicit molecular level properties [60]. These side chains give rise to a rich array of mesomorphic behavior with the appearance of the liquid crystalline phase (LCP). The LCP renders facile uniaxial orientation resulting in polarized light emission [61, 62] and increase in mobility when utilized in thin film transistors [15]. Recently, dioctyl substituted bithiophene fluorene copolymer (F8T2) transistors have been shown to be very promising with relatively high mobility and good air stability at the interface with a polymer dielectric [63].

The quality of an interface between a dielectric and a semiconducting polymer determines the performance of polymer FETs. In particular, trapped and interfacial charges have significant impact on the performance of organic light-emitting diodes (LEDs) and FETs resulting in voltage instability and delay time of electroluminescence at low operation voltages. Early organic electronic devices have utilized hybrid structures; inorganic materials such as a thermally grown SiO_2 gate dielectric on a degenerately-doped silicon substrate were combined with a semiconducting polymer [64]. Many recent works focus on organic dielectrics to form a high quality interface with organic

semiconductor [65] or to have a specific role such as a one carrier (hole or electron) device or an inversely doped (*n*-doped) semiconducting polymer. The importance of an interface for practical device operation and applications is demonstrated in a recent publication by Chua *et al*. [66]. Typically most of organic FETs show p-type conduction; however, recently it was shown that the usage of an appropriate hydroxyl-free gate dielectric yields n-channel FET conduction in many conjugated polymers. Chua *et al*. have shown that electrons are more mobile in organic FETs than previously accepted; in PF copolymers the parallel electron mobilities are one of the highest: 10^{-3} ~ 10^{-2} cm^2/Vs. Additionally, this n-type behavior largely depends upon the choice of the gate dielectric, which controls trapping of electrons usually happened at surface groups, such as silanol groups at the semiconductor-dielectric interface in the case of commonly used SiO_2 gate dielectric. The role of the gate dielectric has most commonly been regarded as the layer affecting semiconductor morphology. Furthermore, this opens up new opportunities for organic complementary metal-oxide-semiconductor (CMOS) circuits.

Technology roadmaps predict less than 2 nm equivalent gate oxide thickness (EOT) for sub-0.10 μm CMOS devices. Within these dimensions, SiO_2 has relatively large gate leakage current and reliability issues because of which recent efforts have focused on high-*k* gate dielectrics [67]. Among these high-*k* materials, Al_2O_3 has attracted considerable attention due to its low leakage characteristics [68, 69]. Although the bandgap of Al_2O_3 (Eg~8.8 eV) is similar to that of SiO_2, its dielectric constant (k = 8.4 ~ 12) is two to three times larger than that of SiO_2. The relatively large Eg of Al_2O_3 provides compatibility with a wide range of semiconductors. It has been recently shown that in polymer FETs high-*k* dielectrics result in device operation at low voltages. The

oxide capacitance increases due to its higher dielectric constant resulting in a reduction of the threshold voltage and lower power dissipation. In addition, high-*k* dielectric materials can partially compensate for the relatively low carrier mobility of semiconducting polymer [70], and further enhance the switching speed of FETs [71].

Trapped and interfacial charges have significant impact on the performance of organic LEDs and FETs resulting in voltage instability and delay time of electroluminescence at low voltages [5]. In recent years, MOS structures based upon organic polymers such as P3HT [72, 73] and poly (3,3´´´-dialkyl-quaterthiophene) (PQT) [74] have been analyzed. Throughout the work, it is well understood that interfaces are key to efficiently operate organic devices, but our understanding of their electronic properties is still rudimentary. In this chapter, the impact of Al_2O_3 on the capacitance-voltage characteristics of polymer-based MOS structures is investigated. MOS structure were fabricated one of a derivative of the PF family, poly[bis(2-ethyl)hexylfluorene] (PF2/6), as the active semiconductor layer. To our knowledge this is the first time MOS structures are fabricated using PF polymer with Al_2O_3 layer as the gate dielectric. A detailed analysis of (PF2/6)/Al_2O_3 interfacial properties using C-V and G-V techniques is discussed.

3.2. Experiment

3.2.1. Cleaning

p^+-Si (100) wafers with resistivity of 0.001-0.005 Ω-cm were cleaned using a modified Shiraki process [75, 76]. This method is known to chemically remove organics and the native oxide in a series of steps involving the growth and etching of oxide layers. Further, the final step results in an atomically flat, hydrogen terminated surface that is reasonably resistant to the re-growth of a native oxide exposure to air for a period of a few hours. All chemicals were semiconductor grade products from Sigma Aldrich/Riedel-de Haër. The following table details the cleaning procedure used for all samples in this dissertation.

Step	Procedure
1	10 min. HNO_3 dip at 90 °C followed by DI water rinse (thick oxide growth)
2	1 min. HF:H_2O (1:5) dip followed by DI water rinse (oxide etch)
3	10 min. HCl:H_2O_2:H_2O (3:1:1) dip at 90 °C followed by DI water rinse (thin oxide growth)
4	1 min. HF:methanol (1:3) dip without DI water rinse (oxide etch and passivation)
5	Drying under nitrogen

Table 3.1: Silicon substrate cleaning procedure.

3.2.2. Al_2O_3 Deposition

The Al_2O_3 film (of thickness ~250 nm) was deposited using electron-beam (e-beam) evaporation on p^+-Si. Immediately following cleaning and drying, the samples were transferred to a Kurt J. Lesker (KJLC) AXXIS e-beam deposition system. This computer controlled e-beam system is designed to facilitate multiple deposition techniques and co-deposited films efficiently with a Telemark TT-6 e-beam power supply and multi pocket source. The configuration of the table top AXXIS system is shown in Figure 3.1. In this system, we have only main process chamber without being connected to loadlock chamber.

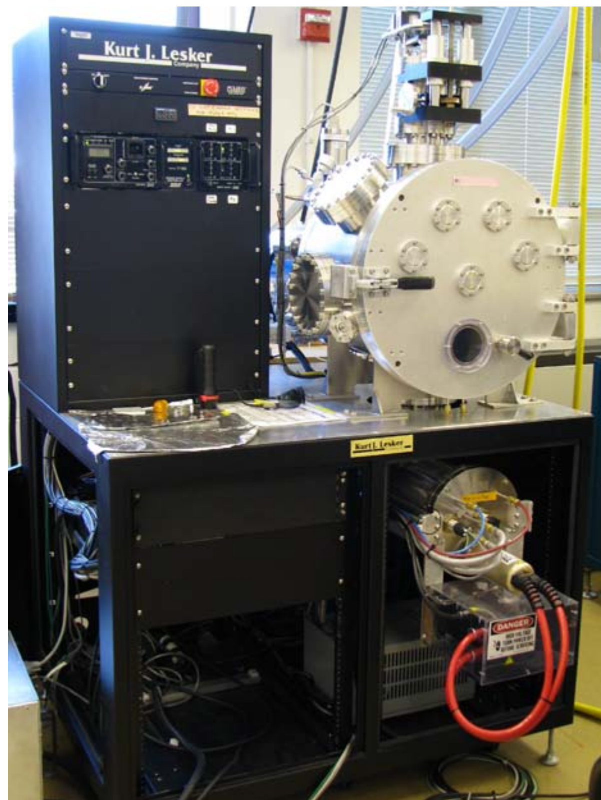


Figure 3.1: KJLC's computer controlled AXXIS e-beam system.

A customized Ti substrate holder was used to tightly secure the samples. The process chamber was then pumped down to a base pressure of 1×10^{-7} torr, first with a roughing pump and then a CryoTorr cryogenic pump. Oxygen backfill was then applied by flowing oxygen at the rate of 4 sccm from a nozzle placed closely near the substrate holder. The working pressure was held ~$4\text{-}5\times10^{-5}$ torr during the film deposition. The pressure of the oxygen reactive gas has an influence on properties of the film including refractive index. [77] After establishing an oxygen ambient, the substrate was then rotated at 20 rpm and heated to 50 °C to promote uniform adhesion of the evaporated Al_2O_3 into the substrate.

The evaporation source materials were Al_2O_3 pellets (1.5 to 4 mm pieces, 99.99 % purity) from KJLC placed in graphite crucibles. First, a thin layer of Al_2O_3 of the desired thickness was deposited at ~0.5 Å/s. Deposition rate and thickness were monitored with a 6 MHz Au QCM crystal sensor and computer controlled Sigma SQS-242 software. After reaching the target thickness, turn off the oxygen valve and samples were annealed *in-situ* under hydrogen ambient, which has been shown to improve the electrical properties of thin films deposited on Si [78]. The process chamber was first pumped back down to a high vacuum (better than 1×10^{-6} torr). The cryogenic pump valve was then throttled and a flowing hydrogen ambient was formed at 45-50 sccm and a pressure of $4\text{-}5\times10^{-4}$ torr. The samples were then annealed at 250-300 °C for 45 min.

3.2.3. Spincoating and Metallization

The PF2/6 used in this work has M_n = 88, 000 g/mol and M_w = 130, 000 g/mol; its synthesis is reported elsewhere [79] and chemical structure is shown in Figure 3.2.

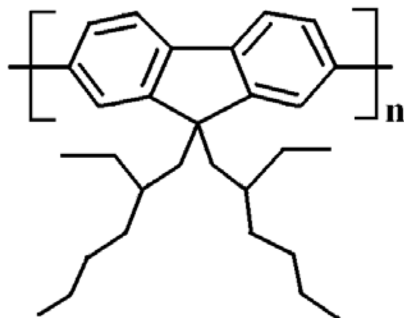


Figure 3.2: Chemical structure of poly[bis(2-ethyl)hexylfluorene] (PF2/6).

The Al_2O_3 substrate was cleaned with ultra-sonication of 10 min acetone, 10 min methanol, and rinsed with isopropanol, and followed by flowing dry N_2 gas. The PF2/6 film (of thickness ~105 nm) was prepared by spincoating onto the Al_2O_3 layer from a toluene solution under N_2 atmosphere inside the MBraun glove box as shown in Figure 3.3. Since the device performances based on organic semiconductor are extremely sensitive to the environmental conditions such as oxygen and moisture, this sensitivity of organic semiconductors towards exposition to oxygen and moisture is a strong limiting factor in the proper operation of organic device. The right positioned box is equipped with a Direct 1000 spincoater and a small water cooled oven that goes up to 350 °C for baking and heat treatment. The left positioned glove box is equipped with a thermal

evaporator for the deposition of small organic molecules and metals. The two boxes are connected via an antechamber with translation rails and a loading gate.

The spincoater is inserted in the bottom plate of the glove box. The PF2/6 solution was at first prepared with a concentration of 10 mg/ml of toluene solvent. The solution was then filtered once with a 0.45 μm PTFE filter. Approximately 6-8 drops of PF2/6 from a pipette was then spincoated on the area of the device with spin rotations of 250 rpm for 1 s; 500 rpm for 1 s; and 2500 rpm for 30 s. After baking the PF2/6 films at 60 °C for 20 min, the samples were transferred to a thermal evaporator for the top Al contact. The Al deposition procedure using thermal evaporation involves selecting a tungsten boat for loading Al pellets and then increasing the current driven through that boat slowly while monitoring the thickness through Sigma SQC-222 external monitor. When a steady deposition rate of 0.1-0.3 nm/s was achieved, the substrate shutter was opened to start deposition. When desired thickness was achieved, the shutter was closed, and the source current was shut off [80].

The final structure fabricated was p^+-Si/Al_2O_3/(PF2/6)/Al and the device size was determined by scanning electron microscopy (SEM) as 2.2×10^{-3} cm^2. Additionally, we also prepared a control sample: Al_2O_3/p-Si with resistivity of the p-type Si ~50 Ω-cm. The aim of comparison between organic and control samples is to figure out which layer contributes to the trap charges in either Al_2O_3 layer or interface between Al_2O_3 and PF2/6. As found in next chapter, the low hysteresis for the control sample compared to the PF2/6 MOS structure indicates that the PF2/6 layer itself is responsible for large hysteresis. In addition, p-si substrates acts as semiconductor in the control sample while p^+-Si substrate is used for the bottom gate. Because of the good vacuum under the probe station chuck,

unpolished back side, a metal back contact was not used. Electrical characterization of the MOS structures was performed at room temperature in the Micromanipulator probe station. C-V and G-V were carried out at frequencies ranging from 10 kHz to 1 MHz and C-F measurement from 20 Hz to 1 MHz using a HP 4284A LCR meter. For the C-V measurements the devices were biased from -25 to 10 V with voltage step of 0.175 V, held at 1 s, then reverse biased for hysteresis measurement. The C-V and G-V curves were corrected for the possible presence of series resistance (R_S) [49].

Figure 3.3: MBraun glove box system with two boxes [80].

3.3. Discussion

The capacitance of a MOS can be changed by accumulating, depleting, and inverting charges in the semiconductor at the interface with the dielectric. A negative potential causes holes to be accumulated at the dielectric/semiconductor interface forming a thin layer which behaves like a parallel plate capacitor. When the semiconductor layer is depleted, the capacitance falls owing to the formation of a depletion region at the dielectric/semiconductor interface. When the gate bias is increased sufficiently to invert the surface, an inversion layer is created and the value of the capacitance strongly depends on the applied frequency. This last inversion layer is typically not observed in polymer semiconductor which is also confirmed by theory [81]; the very long relaxation time of the minority carriers precludes the presence of the polymer inversion at practical time scales at the laboratory. Chua *et al*. [66] discussed another important reason why the inversion phenomenon is hard to see in polymer semiconductor. They convinced that the trapping of electrons at the dielectric/semiconductor interface is indeed the culprit, and they relate this trapping to electronegative hydroxyl (OH) groups in the dielectric material. When the organic FET is fabricated using materials that are free of hydroxyl groups, uninhibited electron transport is indeed observed. Chua *et al*. conclude that if the trapping of electrons by electronegative groups in the dielectric layer could be avoided, then n-channel behavior would be easily seen in a broad range of semiconductors.

Figure 3.4 shows a sample C-V curve of the PF2/6-based MOS structure at 10 kHz frequency; all C-V measurements show hysteresis in the measured range of frequencies. The p-type nature of PF2/6 is clearly seen from the C-V curve: high

capacitance is measured in the accumulation region at negative bias voltage and low capacitance is observed in the depletion region at positive bias voltage. The depletion layer acts as a capacitance in series with the dielectric capacitance. In general, π-conjugated polymers can be regarded as p-type semiconductors since they can stabilize chemically/photo-chemically generated mobile radical-cations (positive polarons) [82]. Further, we do not observe any inversion charge carrier layer at the polymer semiconductor-dielectric interface similar to the work by Zhao *et al*.[74]

With the hysteresis (Δ= 7.7 V) observed at 10 kHz in PF2/6 MOS structure, we estimate the trap charges (N_t) in PF2/6 as 4.4×10^{11} cm^{-2}, using the relation,

$$N_t = \frac{C_{OX}\Delta}{q} \tag{3.1}$$

The oxide charge density in Al_2O_3 (control sample) is 1.88×10^{10} cm^{-2}. The low hysteresis (Δ ~0.12 V) for the control sample, as shown in the inset of Figure 3.4, compared to the PF2/6 MOS structure indicates that the PF2/6 layer itself is responsible for this large hysteresis. Brown *et al*. [83] have attributed such a hysteresis in P3HT-based MOS structures to slow trapping (relaxation) of induced charge carriers or due to migration of low-mobility dopant ions towards the accumulation layer. Additionally, the hysteresis direction reveals the nature of charge injection. Counterclockwise loop of the hysteresis in the C-V curve of PF2/6 MOS structure indicates a positive carrier injection into the PF2/6 layer with subsequent trapping [39].

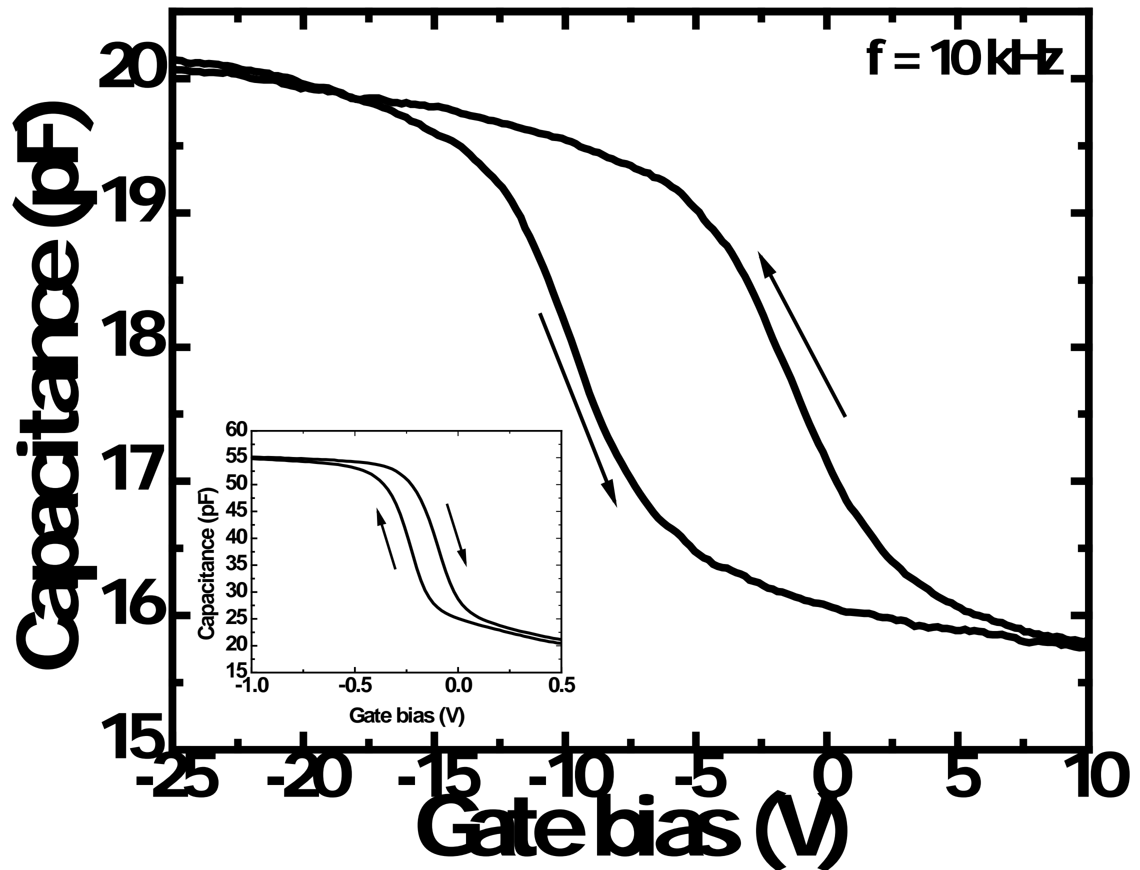


Figure 3.4: C-V characteristics of p^+-Si/Al_2O_3/(PF2/6)/Al MOS structure at a frequency of 10 kHz. The arrows indicate the sweep direction of the gate bias voltage. The inset shows the C-V curve for the control sample: p-Si/Al_2O_3/Al.

In the control sample on the other hand, where p-Si is the semiconductor layer, the hysteresis loop is clockwise indicating a negative carrier injection into the PF2/6 semiconductor layer.

Frequency dependence of the C-V curves in the forward (-25 to 10 V) direction are shown in Figure 3.5 for five different frequencies. The exact nature of the frequency dispersion in the accumulation region is still not clear. Since frequency dispersion in the depletion region is negligible one can look at the separate regions for possible explanations of frequency dispersion. The C-V curves have been corrected for the series resistance which obviously does not remove the dispersion. We fabricated Al/(PF2/6)/Al structures and found no appreciable dielectric loss over the entire frequency region. Further, the leakage current density is also found to be small comparable of one of typical dielectric.

Frequency dispersion in the accumulation region most probably arises from a different response of the trapped and mobile charges at the interface region and bulk. This dependence can be directly related to the long relaxation time in organic materials. The shallow states respond to voltages at high frequencies since the capture and emission of charges in these states have small time constants, while deep states with long time constants are localized and thus do not respond to voltages at high frequency [74]. Lower values of the capacitance at higher frequencies suggest mobile charges at lower frequencies might not respond at higher frequencies, behaving more like trapped charges. Frequency dispersion in the transition region between C_{max} and C_{min} is due to the presence of interface trap states in the bandgap of PF2/6.

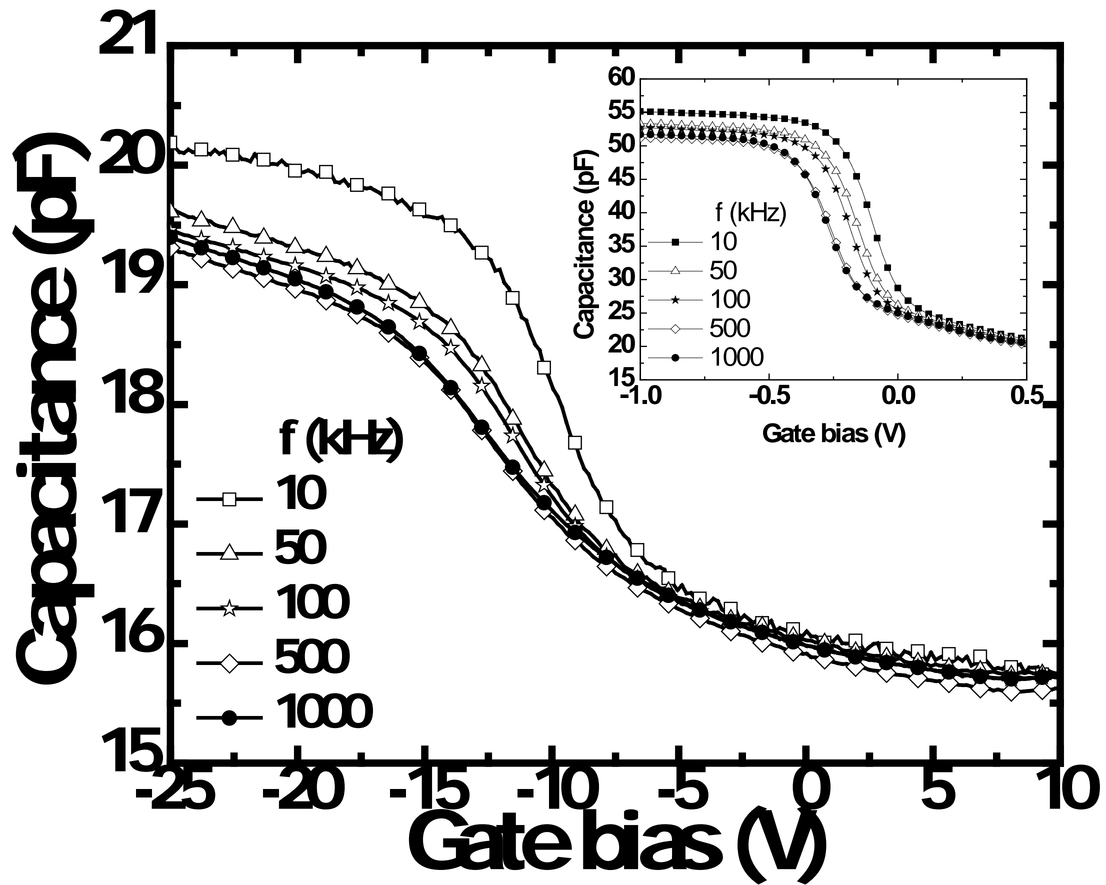


Figure 3.5: Frequency dependence of the C-V curves for the device in Figure 3.4. The inset exhibits the frequency dependent C-V curves of the control sample.

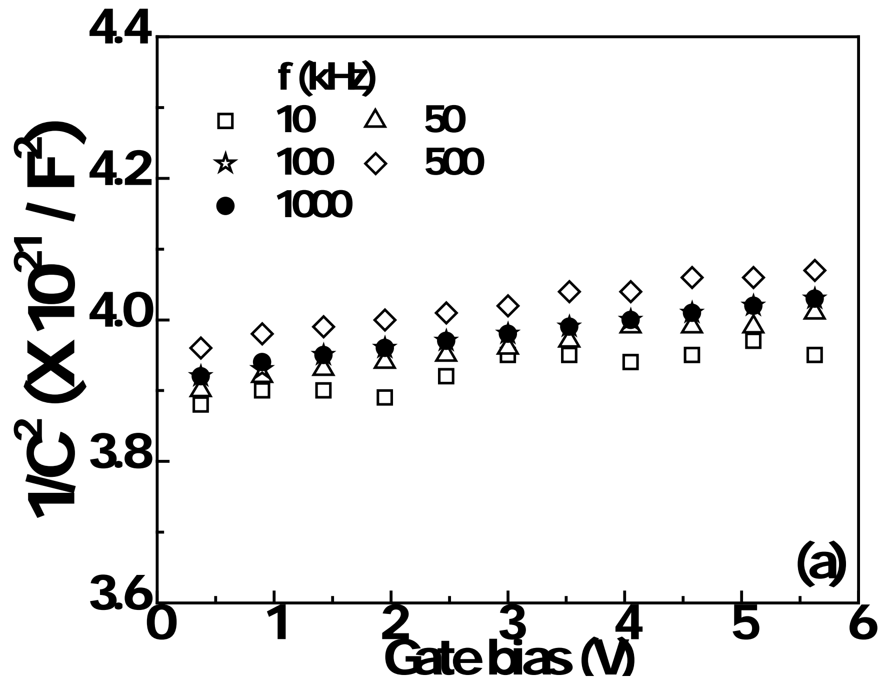
The capacitance due to interface traps acts in parallel to the transition layer capacitance and is a function of the applied signal frequency [39]. As a result, the total capacitance in the transition region increases with decreasing frequency resulting in a shift of flatband voltage with frequency.

We point out that frequency dispersion in the accumulation region in our devices with Al_2O_3 as the gate dielectric is significantly small compared to SiO_2 gate dielectric-based P3HT MOS structures [73]. This clearly shows that our e-beam deposited Al_2O_3 forms a good interface with the polymer layer. For a comparison, frequency dependence of the control sample is shown as an inset in Figure 3.5. Small frequency dispersion in the depletion region indicates that interface traps are small. Thus, the p^+-Si/Al_2O_3 interface may further influence the shape of the C-V curve.

According to the standard Schottky-Mott analysis [39] we can extract the doping density in the depletion region (or more pertinently the concentration of localized charges) from the relationship:

$$\frac{\partial(\frac{1}{C^2})}{\partial V_g} = \frac{2}{q\varepsilon_0\varepsilon_{semi}N_A A^2} \tag{3.2}$$

where C is the capacitance in the depletion region, V_g is the gate bias, ε_0 is the dielectric constant of vacuum, ε_{semi} is the relative dielectric constant of the semiconductor, A is the area of device, and N_A is the doping density or the concentration of localized charges which react slowly to respond to the testing frequency [74]. Using the data of Figure 3.5 we plot $1/C^2$ vs. gate bias at the depletion region, as shown in Figure 3.6.



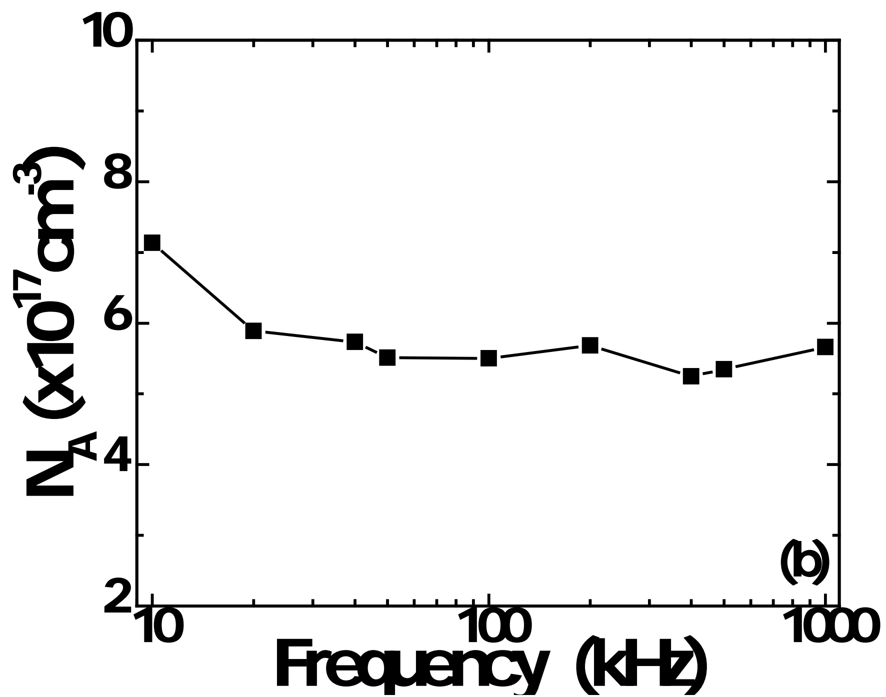


Figure 3.6: (a) $1/C^2$ vs. gate bias voltage for five different frequencies in the deep depletion region (b) Frequency dependence of N_A from p^+-Si/Al_2O_3/(PF2/6)/Al MOS device.

It is more appropriate to consider the depletion region here to obtain the bulk doping density within the polymer layer. ε_{semi} was measured from the capacitance value of an Al/(PF2/6 105 nm)/Al structure as 2.66. At 20 kHz, N_A is estimated to be 5.7×10^{17} cm^{-3} and remains a constant beyond this frequency. Thus, we can say that unintentional doping density is not independent of sweep frequency. However, due to the presence of strong noise at lower frequency in the device, we could not measure C-V characteristics below 10 kHz. Thus, we cannot say or estimate the capacitance behavior in the range of low frequency. One drawback in using the Schottky-Mott analysis is that the N_A values may be overestimated due to the presence of interface states, which stretch the C-V plot [39], and the long relaxation time in π-conjugated polymers [84].

C-F curve at a constant bias voltage of -25 V, which is in the accumulation region, is shown in Figure 3.7. From the Zhao *et al*. [74], if the frequency of the electric field is increased too much, then even the charges with a short relaxation time constant cannot come up with the electric field and the measured capacitance decreases. Thus, some of the carriers at low frequencies become trapped at higher frequencies. Beyond 10 kHz there is a sharp decrease indicating an onset of the transition frequency (f_c). Here $f_c = 10$ kHz at room temperature, which is relatively lower than conventional Si-based MOS structure biased in the accumulation region. f_c, which is the inverse of the bulk relaxation time (τ), is related to unintentional doping concentration (N_A) and the perpendicular mobility ($\mu_\perp$) [73], which is given by

$$\tau = \frac{1}{2\pi f_c} = \frac{\varepsilon_0 \varepsilon_{semi}}{q N_A \mu_\perp} \qquad (3.3)$$

The resulting perpendicular mobility of charge carriers is ~1.3×10^{-7} cm^2 $V^{-1}s^{-1}$ at room temperature. This mobility is comparable to the mobility obtained from space-charge limited currents (SCLCs) measurement from [85].

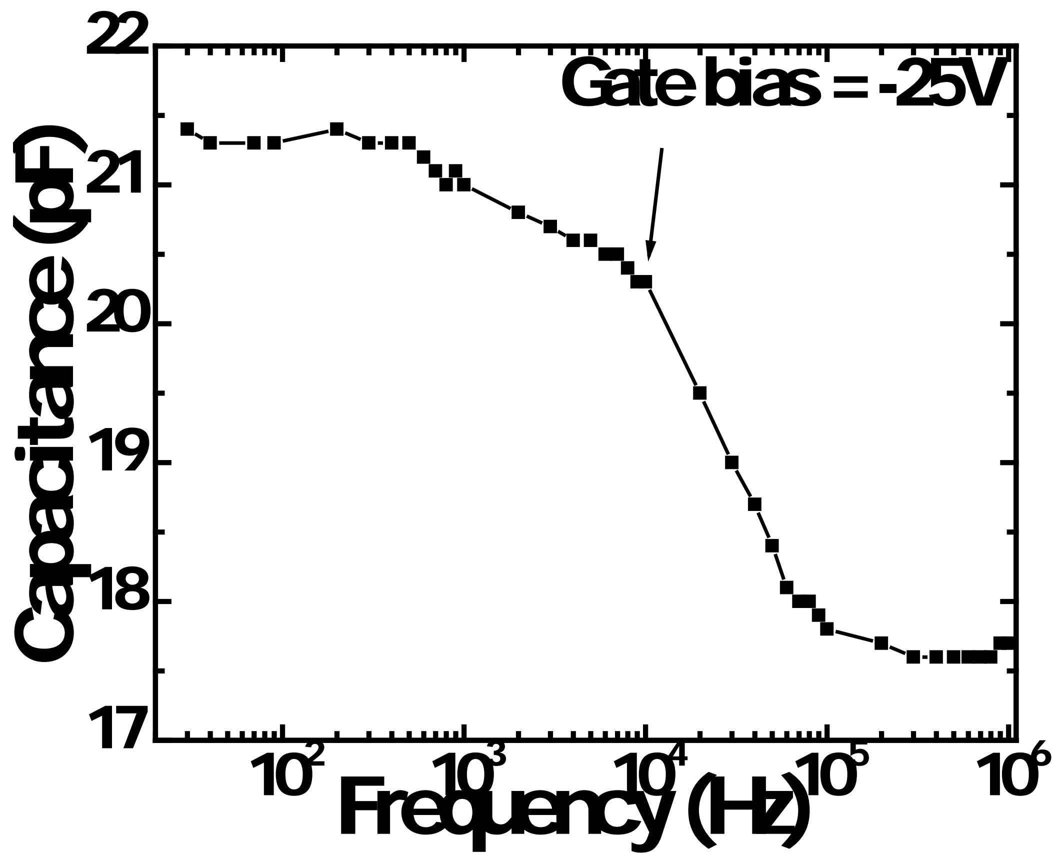


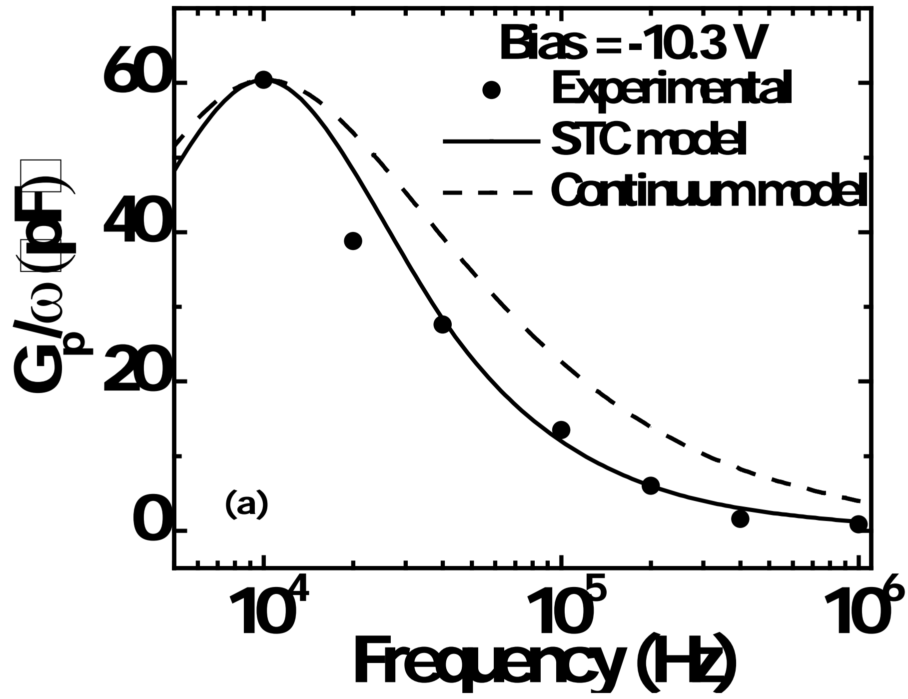
Figure 3.7: Capacitance vs. frequency of p^+-Si/Al_2O_3/(PF2/6)/Al in the accumulation region at -25 V.

Interface trapped charges (referred to as interface states) give rise to energy levels that are confined to the semiconductor/dielectric interface. With the application of a voltage the interface states relative to the fixed Fermi level move within the conduction or valence bands. A change of charge in the interface trap occurs when it crosses the Fermi level [39]. This change alters the MOS capacitance. For the calculation of interface state density (D_{it}), conductance measurements which was described at chapter 2.2.4 were performed as a function of frequency for a given gate bias. A conductance peak is observed in G-V curve because of the AC loss due to the capture and emission of carriers by the interface states. From the measured capacitance and conductance, the equivalent parallel conductance (G_p) at different biases is extracted and a series of extraction was studied followed by the described procedure at chapter 2.2.4.

Although there have been considerable on-going work with fabrication and characterization of polymer MOS structures [70, 74, 92], there is a little work on the analysis of polymer semiconductor/dielectric interface trap states. To our knowledge, this work is one of the first which looks at their interface trap states and leads better understanding of polymer semiconductor/dielectric interfaces.

Figure 3.8 (a) shows G_p/ω vs. frequency at a bias of -10.3 V and that best fitting was obtained if the single time constant model is assumed. We observed the same type of behavior at all values of gate bias in the depletion region. Figure 3.8 (b) displays D_{it} vs. gate voltage as determined by the conductance method. The D_{it} value of PF2/6 MOS structure at the flatband voltage is ~7.7×10^{11} $eV^{-1}cm^{-2}$. This is similar to the density of interface traps measured at P3HT-based MOS structures [72]. Single time constant of interface trap levels, as observed in the depletion region, is probably caused due to

chemical inhomogeneity at the dielectric/semiconductor interface [49]. The inhomogeneity is caused by stretched, bent or broken bonds between the Al_2O_3 and the PF2/6 semiconductor surface. Such a chemical disorder gives rise to potential pockets on a non-equipotential interface where the band bending is altered [50]. It also be noted that the single constant time behavior of interface traps at PF2/6 and Al_2O_3 interface is somewhat different with the exponential behavior of trap states in bulk PF2/6 polymer [85]. Overall, the total AC loss is small and a first order calculation yields D_{it} values that are reasonable from a device point of view in organic MOS devices.



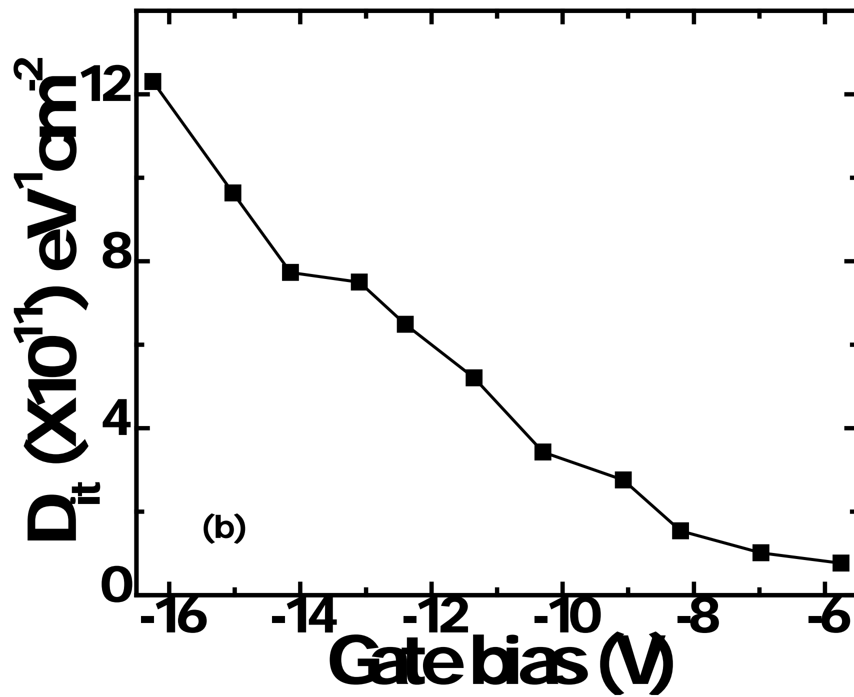


Figure 3.8: (a) The equivalent parallel conductance vs. frequency at a gate bias of -10.3 V. (b) Interface state density vs. gate bias voltage.

Chapter 4. Thermal Annealing of PF-based MOS Structure

4.1. Introduction

In this chapter, the effect of thermal cycling on a semiconducting polymer, PF2/6, is investigated using a MOS structure by means of C-V and G-V measurements.

PFs are attractive due to their facile processing characteristics, allowing uniaxial chain orientation which result in linearly polarized emission [61]. Almost all PFs are characterized by side chains substituted at the bridging carbon that can cause a rich array of mesomorphic behavior with the appearance of the nematic-liquid crystalline (*n-LC*) phase. PF2/6, in particular, has an unusual structure-property relationship: despite the molecular-level disorder that is inherent due to two possible enantiomers and limited number of isomers, thermally annealed PF2/6 films exhibit an ordered hexagonal phase. The PF2/6 chains self consistently average to a five-fold helix. These soft, hairy-rod brushlike polymers further self organize into a three chain unit cell [86], which yields a well ordered semicrystalline hexagonal phase with coherence lengths exceeding 50 nm [60].

Along with the change of crystal structure of PF2/6 films, there is added benefit from the thermal annealing of PF2/6 based device. By transforming the amorphous PF2/6 films to a semicrystalline phase, the interface properties of (PF2/6)/Al_2O_3 can be significantly improved compared to the as-grown polymer in MOS structures discussed in a previous chapter. Detailed analysis of the data following the Nicollian and Goetzberger [48] methodology clearly demonstrates the role of interface traps and the

influence of thermal annealing on device performance, which are vital requirements for the fabrication of PF2/6-based LEDs and FETs. Additionally, the change in unintentional doping concentrations upon annealing stems from the unique crystalline structure that PF2/6 adopts. Although we do not infer the values of mobilities from this work, I-V measurements from PF2/6-based LED structures demonstrate that the perpendicular mobilities are enhanced by more than an order of magnitude in annealed films [85].

Finally, a brief section about fabricating and characterizing of pentacene FET will be present. As a prelude for the preparation of organic non-volatile memory with incorporation of discrete nanoparticle as a charge storage medium, we are needed to develop organic FET structure before driving to the nanoparticle embedded non-volatile memory.

4.2. Experiment

Polymer MOS structure were fabricated with PF2/6 as the electronically active polymer semiconductor layer and Al_2O_3 as an inorganic dielectric layer grown on p^+-Si. Highly *p*-doped (100) silicon wafers employed as the bottom gate electrode, with resistivity of 0.001-0.005 Ω-cm, were etched via the modified Shiraki process [75, 76] prior to the Al_2O_3 film growth. This method is found to be superior in surface passivation by terminating the silicon surface with hydrogen atoms more completely than the conventional RCA cleaning technique. After drying under nitrogen, a KJLC AXXIS e-beam system was utilized to first deposit the Al back-side contact (100 nm) on p^+-Si substrate. A 250 nm thick Al_2O_3 film was then grown, using Al_2O_3 pellets as source material, by e-beam evaporation onto the p^+-Si. The detailed process of Al_2O_3 deposition was described at chapter 3.2.2.

After organic cleaning of p^+-Si/Al_2O_3 substrates in an ultrasonic bath with acetone, methanol, and isopropyl alcohol, the PF2/6 films were prepared by spincoating onto the Al_2O_3 layer, at a speed of 2500 rpm, from a toluene solution (10 mg/ml) that was first filtered through a 0.45 μm filter. The thickness of the film was measured as ~60 nm. After spincoating, the PF2/6 films were baked at 50 °C for 20 min to remove any residual traces of the solvents used. The samples were then immediately loaded into a thermal evaporator for the top Al contact which was evaporated through a shadow mask. The three processes: spincoating, baking, and evaporation were performed in a nitrogen filled glove box system (from MBraun) with oxygen and water levels below 1 ppm. The cross-sectional device configuration fabricated was Al/p^+-Si/Al_2O_3/(PF2/6)/Al as shown in Figure 4.1, and the device area was determined by SEM to be 4.9×10^{-4} cm^2.

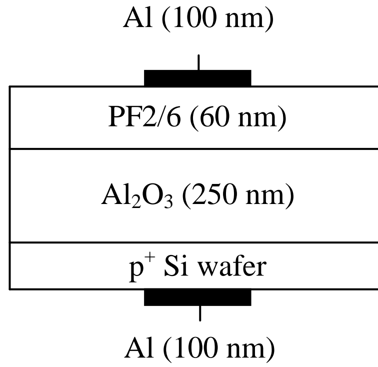


Figure 4.1: Schematic diagram of the configuration of Al/p$^+$-Si/Al_2O_3/(PF2/6)/Al polymer MOS structure.

Thermal cycling of PF2/6 films was done prior to the evaporation of the top Al contact. After spincoating the PF2/6 layer on top of Al/p$^+$-Si/Al_2O_3 substrate, the samples were transferred to a high vacuum (10^{-7} torr) annealing chamber to prevent the possible doping of the silicon substrate due to the long duration of the thermal treatment. Since PF2/6 shows a very slow crystallization process, the samples were first raised slowly to 80 °C (close to T_g) and held for 10-15 hrs. This was followed by raising the temperature close to the *n-LC* phase temperature of the polymer (150 °C) at 2 °C/min. The samples were then cooled back to room temperature at 1 °C/min, after which the top contacts were evaporated for the MOS structures. We further checked the C-V characteristics of a control sample (p-Si/Al_2O_3/Al) that was annealed under the same conditions to ensure that the changes observed in our PF2/6-based MOS structures are not due to the changes between the silicon and Al_2O_3 interface.

Electrical measurements of the polymer MOS structures were carried out at room temperature in air using a Micromanipulator probe station under dark ambient. C-V and

G-V dependence of the devices were achieved over a frequency range from 1 kHz to 1 MHz using a HP 4284 LCR meter which is controlled by a computer program written in LabView®. For the C-V measurements the devices were biased from -15 to 40 V by varying the sweep rates from 0.055 to 11 V/s. Since the wide bandgap semiconducting polymer shows a deep depletion capacitance, by decreasing the sweeping time a deep depletion capacitance in the C-V curve may be obtained (shown in chapter 4.3.2). We allowed optimal holding times to achieve thermal equilibrium since the polymer MOS cannot adequately recover from deep depletion for short holding times. This was followed by reverse biasing for hysteresis measurements. For the best high-frequency fit, R_S was found to be 191 Ω for an as-grown sample and 130 Ω for an annealed sample, respectively.

4.3. Discussion

4.3.1. Structure and Morphology

Depending on the forming conditions, PF2/6 may be glassy or semicrystalline at room temperature, with a nominal glass transition temperature (T_g) for the amorphous component at 80 °C and a crystalline to *n-LC* phase transition just above 160 °C. Work by Tanto *et al*. [60] shows that bulk PF2/6 (powder) has some resemblance to the hexagonal phase at the onset and at T_g there is a distinct structural evolution to the hexagonal phase. Upon cooling the polymer from its *n*-LC phase the X-ray diffraction (XRD) pattern shows sharp Bragg peaks indicative of improved long-range order. To ascertain whether these features are observed in thin PF2/6 films cast from toluene (that are used in our MOS structures), we measured the atomic force microscopy (AFM) images from two films: one as-grown and the second thermally annealed samples (with the same conditions that we used in our MOS structures).

For the AFM studies, PF2/6 films were spincoated on silicon wafers, which were cleaned using procedures described elsewhere [87]. The concentration of the PF2/6 solutions and the recipe for spincoating were the same as used in our MOS structures (described in Chapter 4.2). A detail of the annealing process is also described in Chapter 4.2. The AFM measurement was performed with a Nanoscope IIIa (Veeco Instruments) operating in the tapping mode. Commercial ultra-sharp, rectangular silicon cantilevers made by Micromasch ($250 \times 35 \times 1.7\ \mu m^3$) were used having a nominal spring constant of ~0.35 N/m and a resonance frequency of ~33 kHz. We simultaneously recorded AFM topography and phase images with certain scan rate to have optimal resolution images. Figure 4.2 shows the topography and phase images of the as-grown (a,b) and annealed

samples (c,d). The annealed sample clearly shows an increase in the particle size with an average particle footprint area of ~10^4 nm^2. The rms roughness of the two samples for 1μm×1μm area increased from ~1.4 nm in the as-grown sample to ~2.9 nm in the annealed sample. Since annealing promotes crystallization to an ordered hexagonal phase and its coherence length is in excess of 50 nm [60], each grain in the image most probably reflects a single domain of PF2/6 with a loss of coherence about halfway across each domain due to disorder effects. We point out that since our processing temperature reached only 150 ºC, the annealed film may not have fully crystallized.

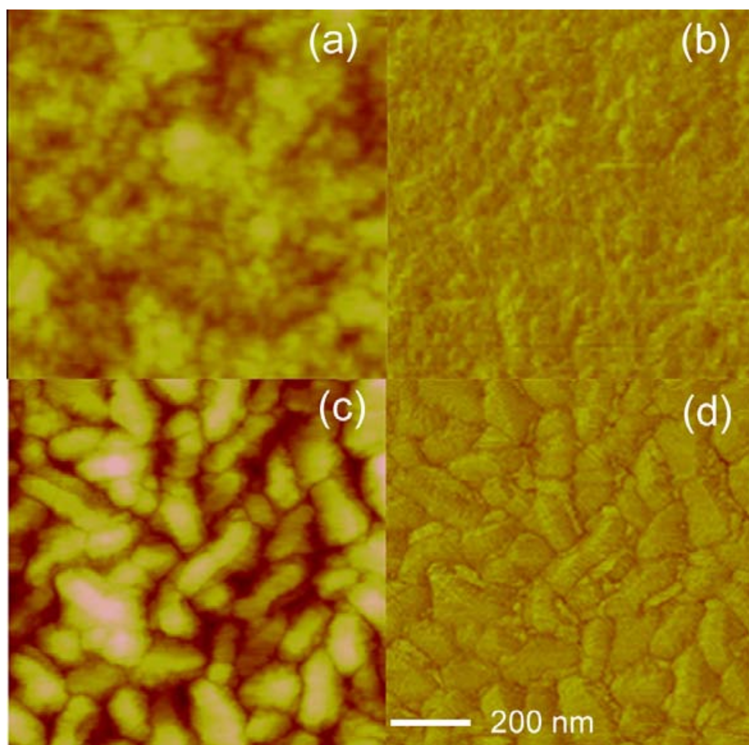


Figure 4.2: AFM topography and phase images of PF2/6 deposited on Si wafers before and after annealing. (a) Topography image of the as-deposited sample; (b) phase image of the as-deposited sample; (c) topography image of the annealed sample, and (d) phase image of the annealed sample.

4.3.2. Schottky-Mott Analysis

Previous efforts to investigating the interface trap density at the interface between organic semiconductor and inorganic dielectric can extend to the thermal annealing study of PF2/6. Figure 4.3 exhibits a typical C-V curve with hysteresis at 10 kHz (top) and 1 MHz (bottom) of both as-grown and annealed samples. Although these plots are shown for two frequencies, similar measurements were performed for a range of frequencies; the magnitude of the hysteresis for both samples was independent of the applied frequency at room temperature but dependent on the sweeping rate as discussed in next chapter. For consistency, we checked that the results presented here represent typical data measured from more than five MOS structures. The shape of the C-V curves for both samples reveals typical *p*-type behavior of the PF2/6 MOS structure. This is inferred from a higher capacitance in the accumulation region at negative bias (with the maximum capacitance being given by the dielectric capacitance) and a lower capacitance value in the depletion region at positive bias (with minimum capacitance produced by the series sum of dielectric capacitance and the capacitance associated with the maximum depletion layer).

Typically, the bias sweep from negative to positive voltage and in the reverse direction display the same amount of hysteresis. Brown *et al*. [83] have attributed such a hysteresis in P3HT-based MOS structures to slow carrier trapping (relaxation) or to the migration of low-mobility dopant ions towards the accumulation layer. Recently Lindner *et al*. [88] have shown by detailed numerical simulations that the origin of the hysteresis in organic devices is a combination of mobile species and trap recharging.

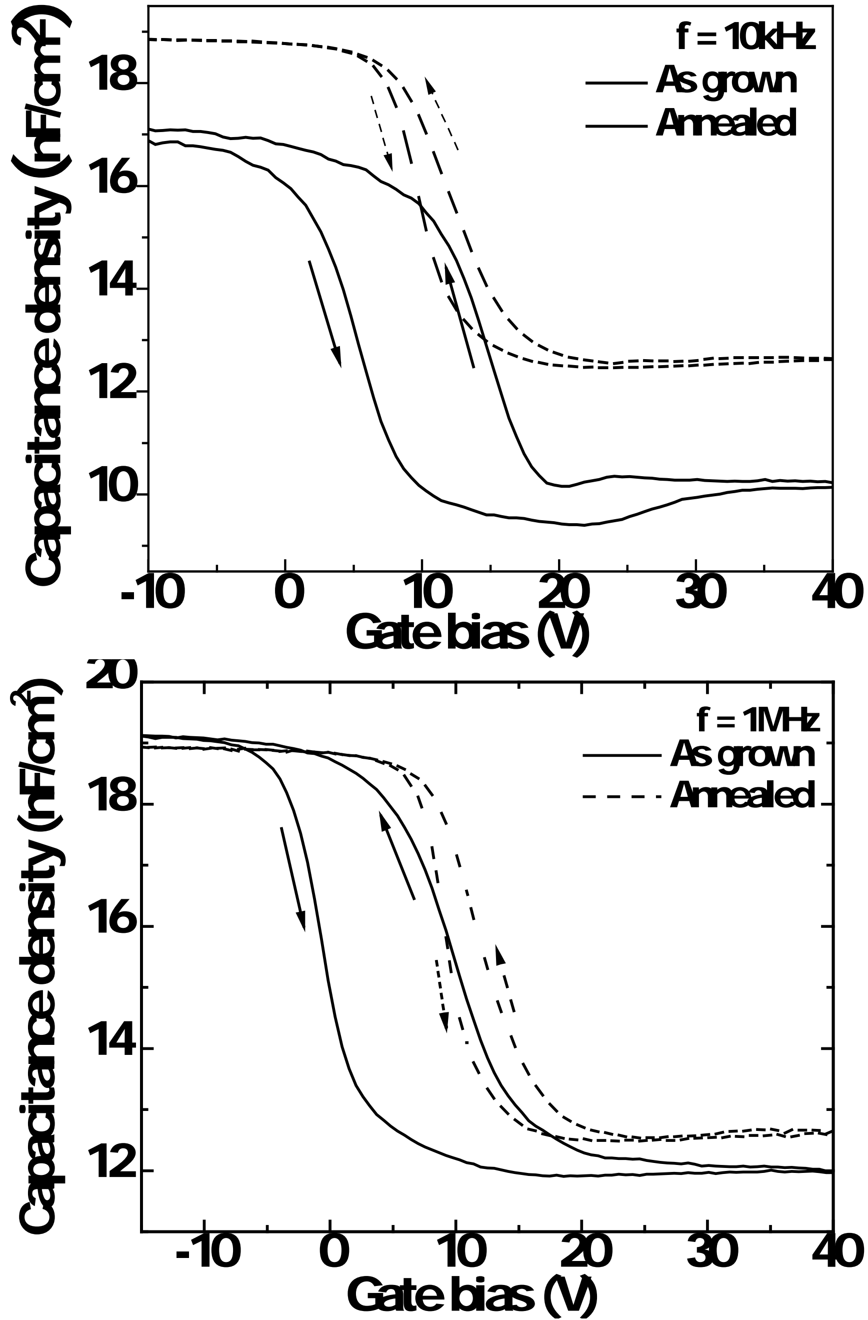


Figure 4.3: Hysteresis curves of both the as-grown sample (solid line) and annealed sample (dashed line) at constant frequency of 10 kHz (top) and 1 MHz (bottom) with sweeping rate of 55 mV/s, respectively. The arrows indicate the sweep direction of the gate bias voltage.

Thus, in our case, the hysteresis and related phenomena originate from charge trapping at or near the interface between the polymer semiconductor and the gate dielectric as well as from ambient oxygen and moisture due to the measurement in air. The counterclockwise nature of hysteresis is usually attributed to a positive carrier injection into the semiconducting PF2/6 layer with subsequent charge trapping [39]. The nature of the observed hysteresis is the same for the as-grown and annealed samples, albeit greatly reduced in the latter.

In comparing the as-grown with the annealed PF2/6-based MOS structures, there are two important features to be noted in the C-V characteristics. First, the shape of C-V curves is similar in both samples although the accumulation and depletion capacitance values are changed after thermal annealing: a slight decrease in the accumulation capacitance and a slight enhancement of the depletion capacitance is seen for the annealed sample. Most probably this arises from the Si/Al_2O_3 interface; a similar change is seen in our control sample. Second, at 1 MHz, annealing the polymer films substantially reduces the hysteresis from 9 V (as seen for the as-grown sample) to 3 V. We measured the thickness and the dielectric constant of PF2/6 films cast on bare Si and PF2/6 films sandwiched between Al/(PF2/6)/Al structures for both as-grown and annealed films. No changes in the thickness and the dielectric constant ($k = 2.6 \pm 0.1$) are seen before and after thermal annealing. This suggests that the crystalline domains in the PF2/6 layer (after annealing) fill up the open trap charge centers, decreasing charge migration in the film and resulting in a reduction of the hysteresis.

By using the relationship from Equation 3.1, we find that N_t decreases from 1.1×10^{12} cm^{-2} in the as-grown sample to 3.5×10^{11} cm^{-2} in the annealed sample. These values

maybe overestimated due to the unexpected mobile ions. To ensure that the above results originate from annealing (crystallization) of the PF2/6 film and not from the dielectric, we checked the hysteresis from two control samples (p-Si/Al_2O_3/Al), one as-grown and the other annealed under the same conditions as our annealed polymer MOS structures. There are virtually no changes in the hysteresis of the C-V curves in the two samples. [Δ is 0.4 V in as-grown and 0.35 V in annealed]. This is not surprising since 150 °C is a relatively low temperature for modification of the structural properties of Al_2O_3. Hence, we conclude that the decrease in N_t in the annealed sample is an effect of the crystallization of the PF2/6 layer.

Typical frequency dependence of the C-V curves for both the samples measured at selected frequencies is shown in Figure 4.4 in the forward (-15 to 40 V) direction with a slow sweeping rate (55 mV/s). The C-V curves of the annealed sample are characterized with a relatively steeper transition region from the maximum capacitance to minimum capacitance compared to the as-grown sample. The positively shifted V_{FB} with annealing indicates the creation of negative charges in the oxide layer. These charges consist of trapped charges in the Al_2O_3 layer that most probably diffuses from the PF2/6 film on the application of a high gate voltage. The negligible variation of V_{FB} shift with annealing in our control samples indicates that these charges are not from bulk Si or Si/Al_2O_3 interface. Since a large V_{FB} shift is the origin of a large threshold voltage in FET structures, we attempted to reduce the V_{FB} shift upon annealing of the polymer, using a surface treatment of the Al_2O_3 using organic self-assembled monolayer [89] or in-situ H_2 annealing.

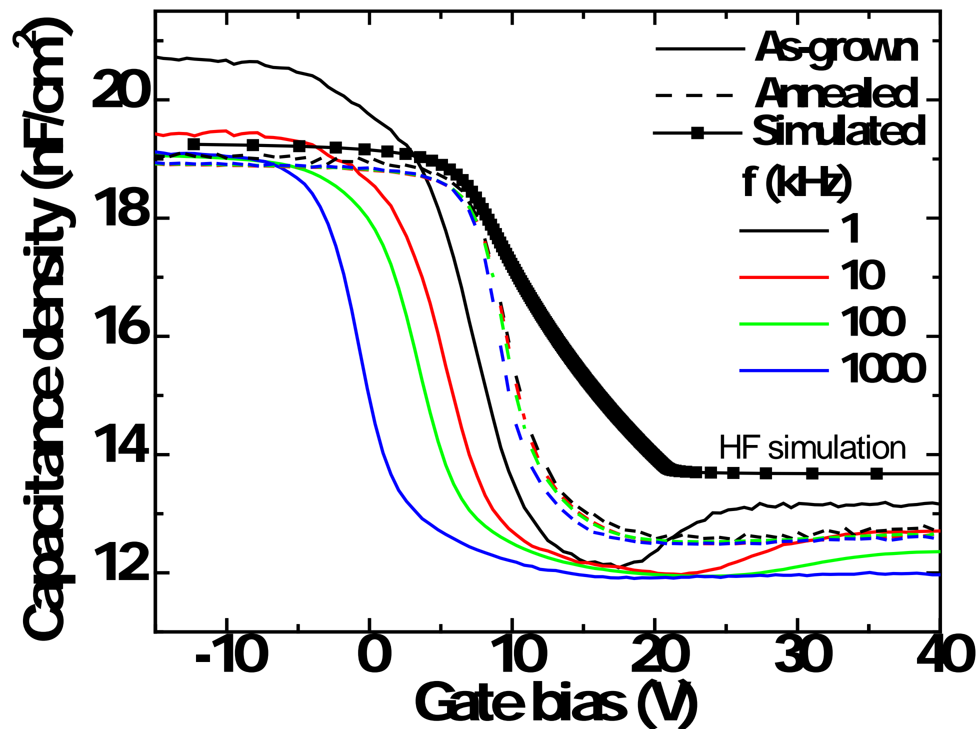


Figure 4.4: Frequency dependence of the C-V characteristics of the as-grown sample (solid line) and annealed sample (dashed line). Simulated C-V curve marked with frequencies shown are 1, 10, 100 kHz and 1 MHz right to left, respectively.

The frequency dispersion in the accumulation region is greater for the as-grown sample compared to the annealed one. The origin of the frequency dispersion in this region is most probably due to a different response of trapped and mobile charges between the interface region and bulk, which can be directly related to the long lifetimes and low carrier generation rates for carriers in disordered organic semiconductors [72]. Detailed reasons for frequency dispersion in the accumulation region of as-grown samples were discussed in Chapter 3.3. The transition region in the as-grown sample also shows a large frequency dispersion, which arises from a large number of interface traps in this sample compared with the annealed film. This is discussed in more detail in the chapter 4.3.3. We point out that in our previous work the C-V measurements were done using a fast sweep and the frequency dispersion in the deep depletion region was negligible [90].

Slower sweep rates result in induced traps in the dielectric or dielectric/semiconductor interface of the as-grown sample, which result in larger hysteresis (discussed later with Figure 4.5). This sample shows an increasing depletion capacitance below 100 kHz (Figure 4.4). These enhanced values result from a combination of the capacitance associated with induced traps and single time constant traps (discussed in chapter 4.3.3) that reside at the polymer-dielectric interface. Thus, there is a trade-off in using slower sweep rates in disordered organic MOS structures: although the C-V curve is far from the deep depletion capacitance, the hysteresis increases. The annealed sample, on the other hand, does not show any increased capacitance in the depletion region due to fewer traps in the dielectric and at the dielectric/semiconductor interface.

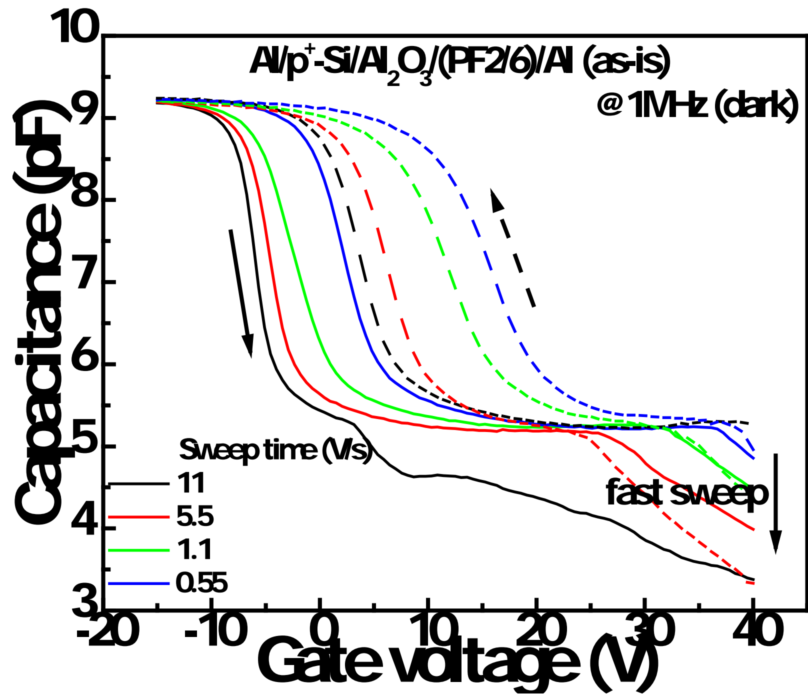
One thing needs to be mentioned in the Figure 4.4 is the creation of inversion layer of polymer semiconductor or not. In polymer MOS structures the inversion charge generation time is much slower compared to the applied high frequency in the C-V measurements. This implies that the polymer MOS does not have enough time to generate minority carriers to form an inversion layer and as a result the depletion region reaches a maximum depth where the high frequency capacitance still relies on the majority carrier position and distribution. To obtain further insight into the nature of the capacitance (whether it is true depletion or inversion), we simulated a high frequency C-V curve as shown by the black squares in Figure 4.4. The simulations were carried out at infinite frequency assuming that the oxide thickness is much greater than the maximum depletion width. With the intrinsic carrier concentration n_i calculated from the effective density of states: $N_C = 10^{19}$ cm^{-3}, $N_V = 4\times 10^{21}$ cm^{-3}, [85] energy gap $E_G = 2.8$ eV, doping density = 8.8×10^{17} cm^{-3} at 1 kHz, and $V_{FB} = 6$ V from the experimental C-V curve, we simulated the high frequency C-V curve using exact-charge analysis [38]. Since the minimum capacitance of the annealed sample in our experimental data is lower than the simulated one, it is clear that PF2/6 MOS structure does not reach the inversion region and shows a depletion capacitance for positive gate bias. This is also verified by theoretical work that due to extraordinarily low minority carrier generation rates inversion would not be observable at practical time scales [88].

One of the usual phenomenons of organic MOS is deep depletion capacitance. Deep depletion occurs in a MOS capacitor when measuring the high frequency capacitance while sweeping the gate voltage “quickly”. Quickly means that the gate voltage must be changed fast enough so that the structure is not in thermal equilibrium.

One then observes that, when sweeping voltage from flatband to threshold and beyond, the inversion layer is not or only partially formed. This occurs since the generation of minority carriers cannot keep up with the amount of needed time to form the full inversion layer. The depletion layer therefore keeps increasing beyond its maximum thermal equilibrium value, resulting in a capacitance which further decreases with voltage [91].

The time required to reach thermal equilibrium can be estimated by taking the ratio of the total charge in the inversion layer to the thermal generation rate of minority carriers. A complete analysis should include both the surface generation rate as well as generation in the depletion layer and the quasi-neutral region. A good approximation is obtained by considering only the generation rate in the depletion region and the quasi-neutral region. [38]

Figure 4.5 shows the C-V curves of as-grown (a) and annealed (b) PF2/6 MOS structure depending on various sweeping speeds at 1 MHz. It was observed that a fast sweeping rate of C-V measurements show a deep depletion capacitance at both samples due to the long relaxation time of carriers in the polymer. However, we observe flat deletion capacitance in both samples when sweeping times are enough long. Note that applying optimal holding time after sweeping from accumulation to depletion is required to get thermal equilibrium status in polymer MOS structure.



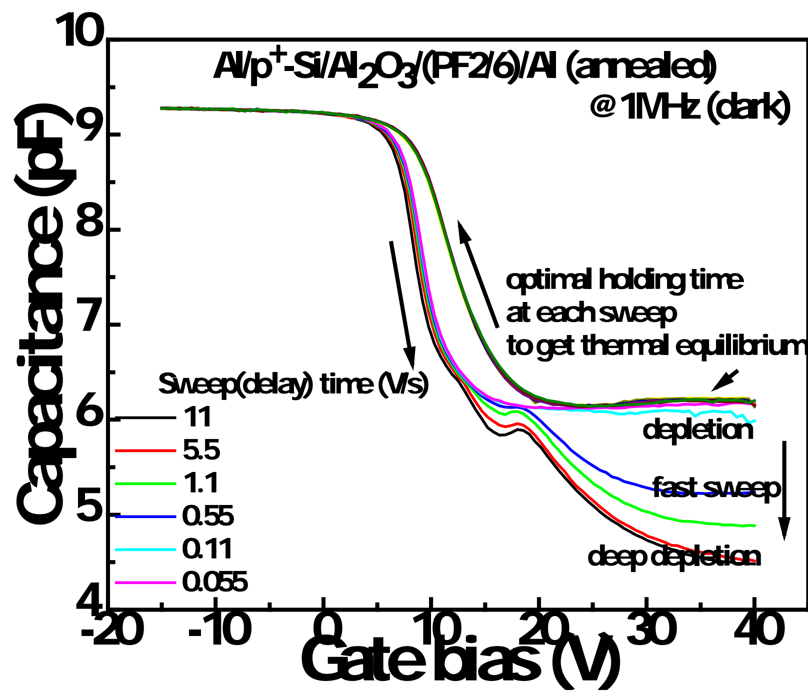


Figure 4.5: (a) C-V curve of different sweeping speeds of as-grown PF2/6 based MOS structure (b) C-V curve of different sweeping speeds of thermally annealed PF2/6 based MOS structure.

Overall, compared to the as-grown sample, the annealed sample shows a reduced hysteresis, very small frequency dispersion in the depletion region, and a reduced stretching of the C-V curve about the voltage axis (Figures 4.3 and 4.4). These characteristics can be attributed to a reduced interface trap density indicating a better interface quality between Al_2O_3 and PF2/6 as discussed in chapter 4.3.3.

A closer inspection of the C-V curves suggests charge carrier localization in the bulk of the polymer. As a first step, we extract the unintentional doping density from a plot of $1/C^2$ vs. V as shown in Figure. 4.6. This is derived from the standard Schottky-Mott analysis [39] where the doping concentration in a *p*-type semiconductor. We use the depletion region at 1 MHz sample frequency for the plots. The slopes correspond to the localized doping concentration. The slopes of $1/C^2$ vs. V are slightly different for the as-grown and the annealed sample. Using the dielectric constant of PF2/6 as 2.6, and the slopes from Figure 4.4 by adopting Equation 3.2, N_A for the as-grown and the annealed samples are $4.3 \times 10^{17}\,cm^{-3}$ and $9.1 \times 10^{17}\,cm^{-3}$ at 1 MHz, respectively. N_A as a function of the frequency is plotted for both samples in Figure 4.7. The *p*-type nature of PF2/6 arises most probably from structural and oxygen-induced defects that can stabilize mobile radical cations [82]. At lower frequencies we do observe an increase in N_A by a factor of 4. The slight enhancement of N_A maybe related to the morphological changes in the polymer film upon annealing; thermal cycling of PF2/6 results in a closed-pack formation of the polymer chains where the side chains are nested pairwise.

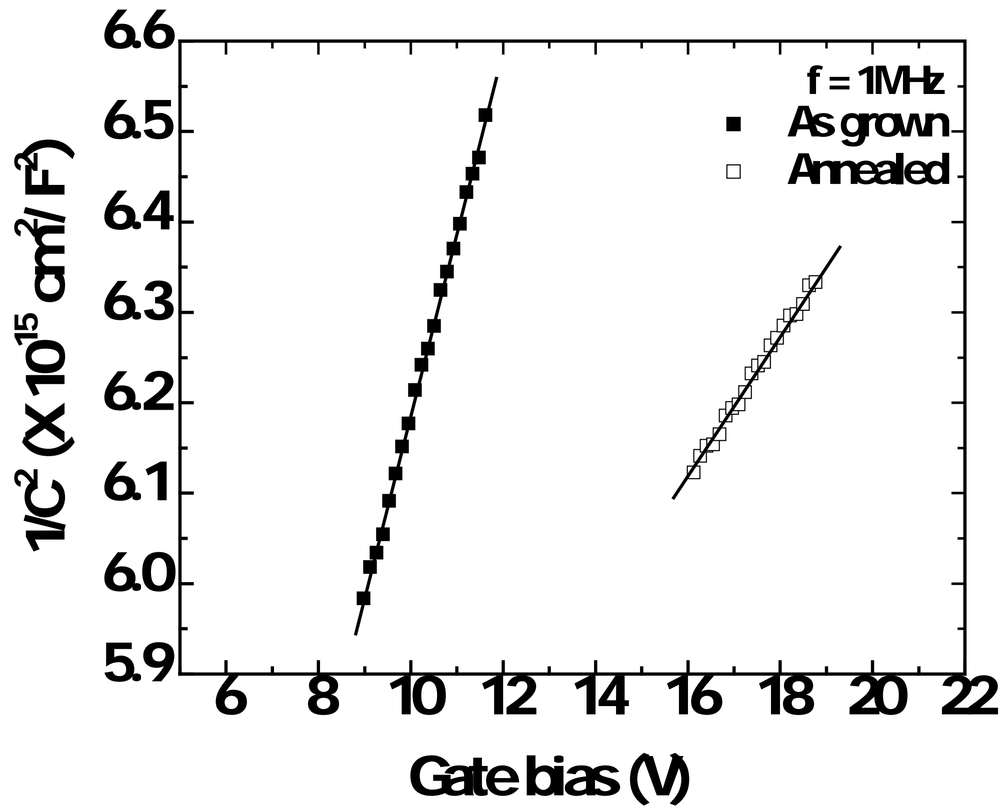


Figure 4.6: $1/C^2$ versus gate bias voltage curves of as-grown and annealed samples at test frequency of 1 MHz, derived from the depletion region C-V curves in Figure 4.4.

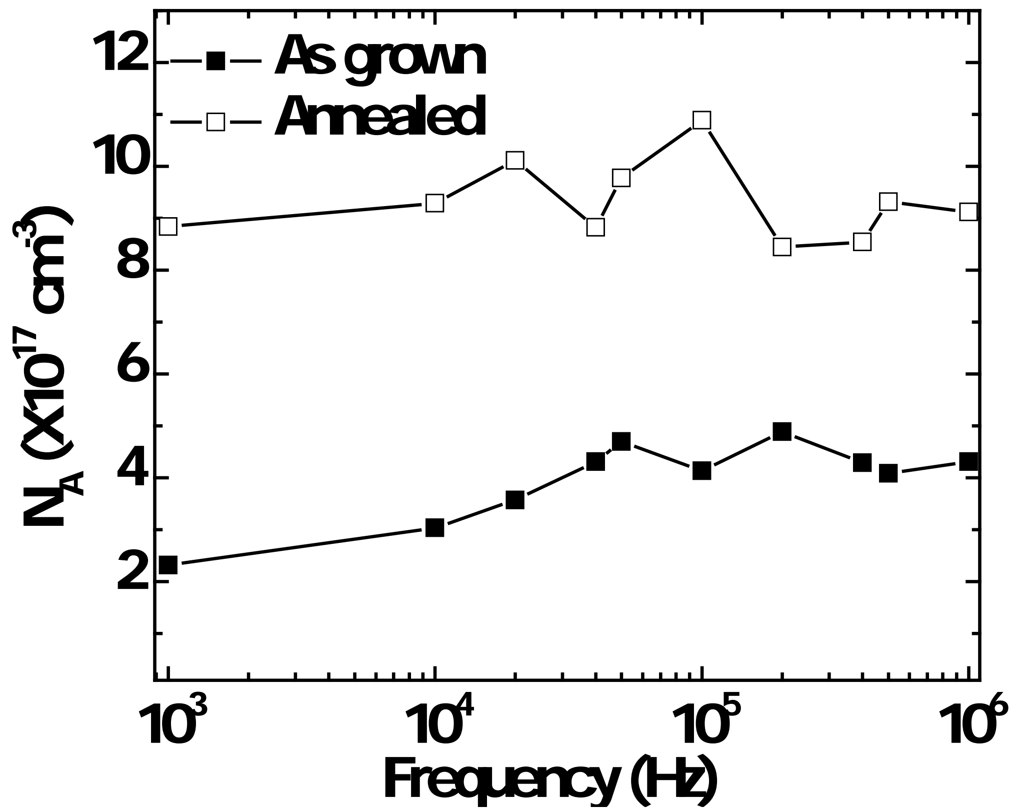


Figure 4.7: Extracted doping density (N_A) plotted as a function of measured frequency in the as-grown sample and the annealed one.

However, the exact mechanism is still not understood since the thicknesses of the films remain almost the same before and after annealing. The number of dopants most probably remains unchanged upon annealing but a volume contraction of the semicrystalline phase results in a slight enhancement of the doping densities. Annealing also results in an enhancement of the charge carrier mobility perpendicular to the dielectric as in the recent work by Grecu *et al*. [92]. This has been independently verified by determining the hole mobilities from PF2/6-based LED structures using I-V characteristics under space charge limited conduction; the carrier mobilities are enhanced by more than an order of magnitude [85].

4.3.3. Interface Trap States

A polymer MOS structure can be described by a series capacitance of the dielectric and depletion layer of the semiconductor as schematically shown in Figure 4.8.

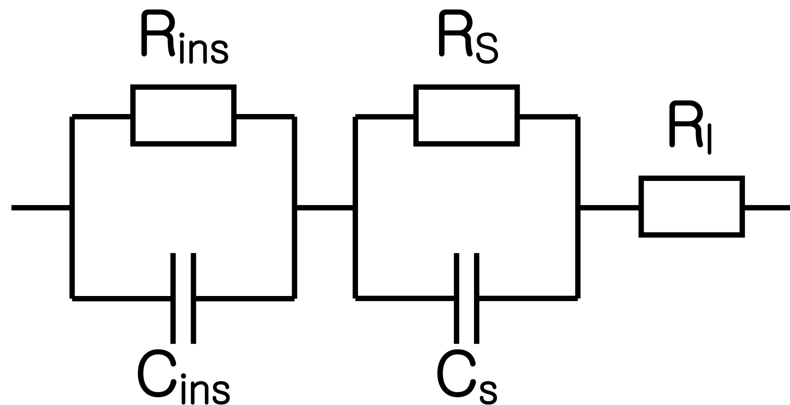
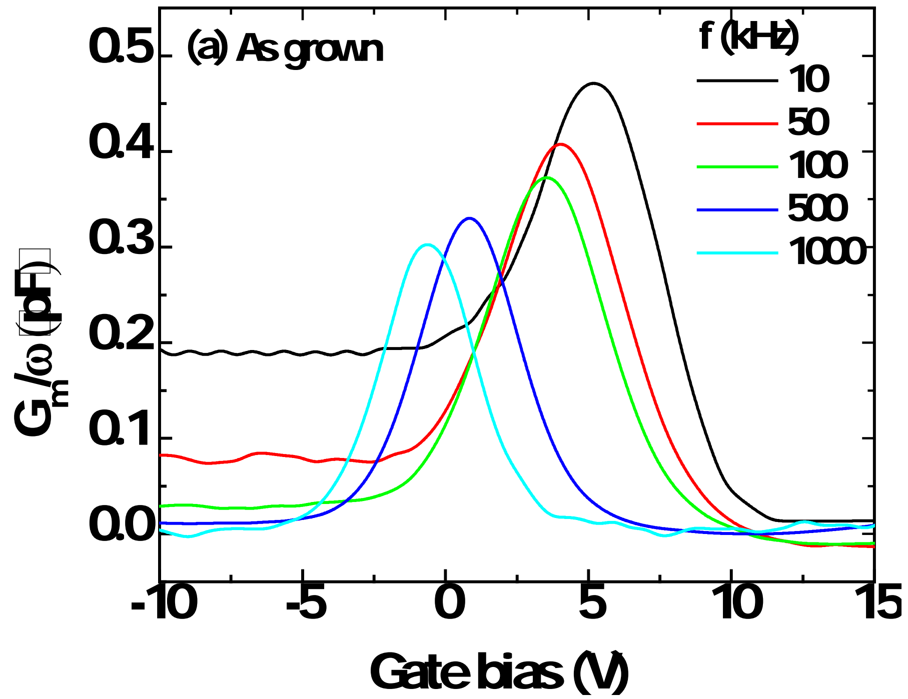


Figure 4.8: Equivalent circuit model of resistors and capacitors for contacts, semiconductor and dielectric.

The appropriate equivalent circuit is modeled as the connection in series of the dielectric (R_{ins}, C_{ins}), semiconductor (R_s, C_s), and small contact resistance associated with the electrodes (R_l). This is the simplest model; for a full description of the dielectric response of polymer MOS structures models taking into account the time constant dispersion in bulk polymer should be considered [93]. Since this work compares the semiconductor/dielectric interfacial properties of two samples, we use the simple circuit model shown in Figure 4.8, assuming that the correction terms are the same for both samples.

Figure 4.9 (a) and (b) shows the measured loss of conductance per angular frequency (G_m/ω) as a function of the gate bias for five selected frequencies. Distinct conductance peaks are observed for both samples because of the AC loss due to the capture and emission of carriers by the interface traps. The peak of the G_m/ω vs. V curve shifts negatively with increasing frequency, which is consistent with the shift of the flatband voltage of the corresponding C-V curves. The height of the loss peak denotes the number of interface traps at a given frequency [69]. Since the loss peak height of the annealed sample (Figure 4.9 (b)) is substantially reduced compared to the as-grown sample, it suggests a reduction in the interface traps. Also, the stretch of G_m/ω vs. V profiles for the as-grown sample reflects the stretching of C-V curves, seen in Figure 4.4. The rise in conductance in the accumulation region for the as-grown sample is due to the presence of high series resistance effects.



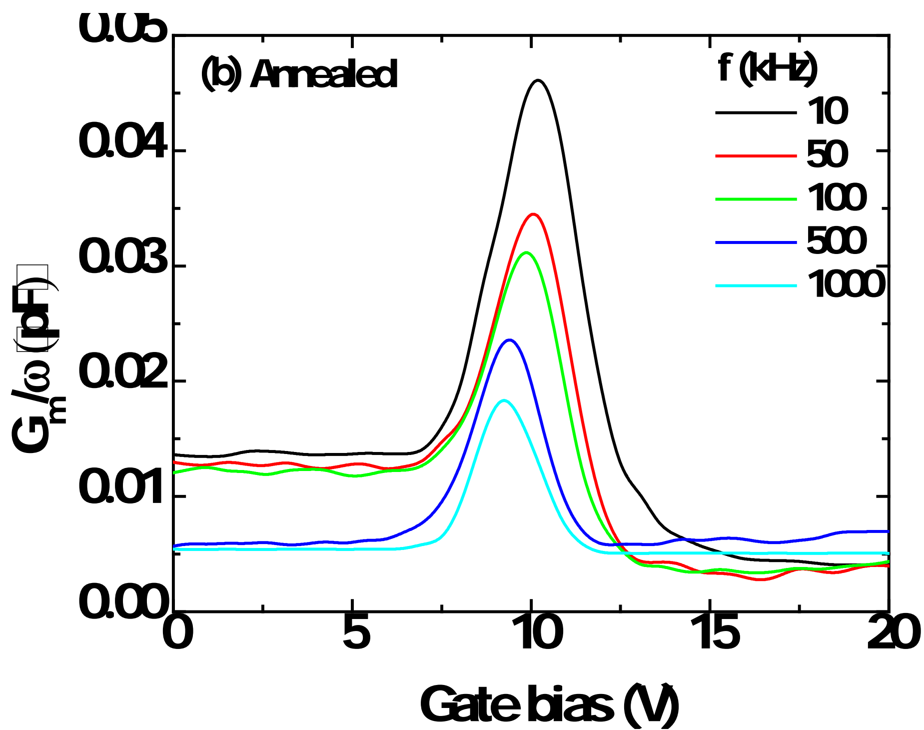


Figure 4.9: Frequency dependence of the measured conductance loss (G_m/ω) as a function of gate bias voltage for (a) as-grown and (b) annealed samples.

To investigate the effect of annealing on the interface, we focused on the interface trap charges. We have utilized the method proposed by Nicollian and Goetzberger [48, 49] to calculate the equivalent parallel conductance (G_p) offered by interface states from the measured capacitance and conductance as descried earlier in chapter 2.2.4. Figure 4.10 represents G_p/ω versus frequency for the as-grown and annealed PF2/6 MOS structures at biases of -1 V and 8 V flatband voltages, respectively. The continuous lines (bold and dotted) denote the theoretical curves generated using Equations 2.22 and 2.24. The filled circles represent the experimental data. The equivalent parallel capacitance versus frequency agrees well with the single time constant model (indicated by solid lines) over the entire range of gate biases for both samples which is also consistent with figure 3.8 (a).

Finally, the calculated D_{it} values versus gate bias are plotted for the as-grown and annealed sample in Figure 4.11. Thermal annealing improves the quality of interface between (PF2/6)/Al_2O_3 layer as identified by a significant reduction of the interface trap density from ~3.9 × 10^{12} $eV^{-1}cm^{-2}$ to ~3.3 × 10^{11} $eV^{-1}cm^{-2}$ at the flatband voltage. The lower value of D_{it} for the annealed sample is in agreement with the small frequency dispersion shown in Figure 4.4. Thus, thermal cycling of PF2/6 from its *n-LC* phase to room temperature results in large crystalline domains reducing the interface trap densities at the (PF2/6)/Al_2O_3 interface.

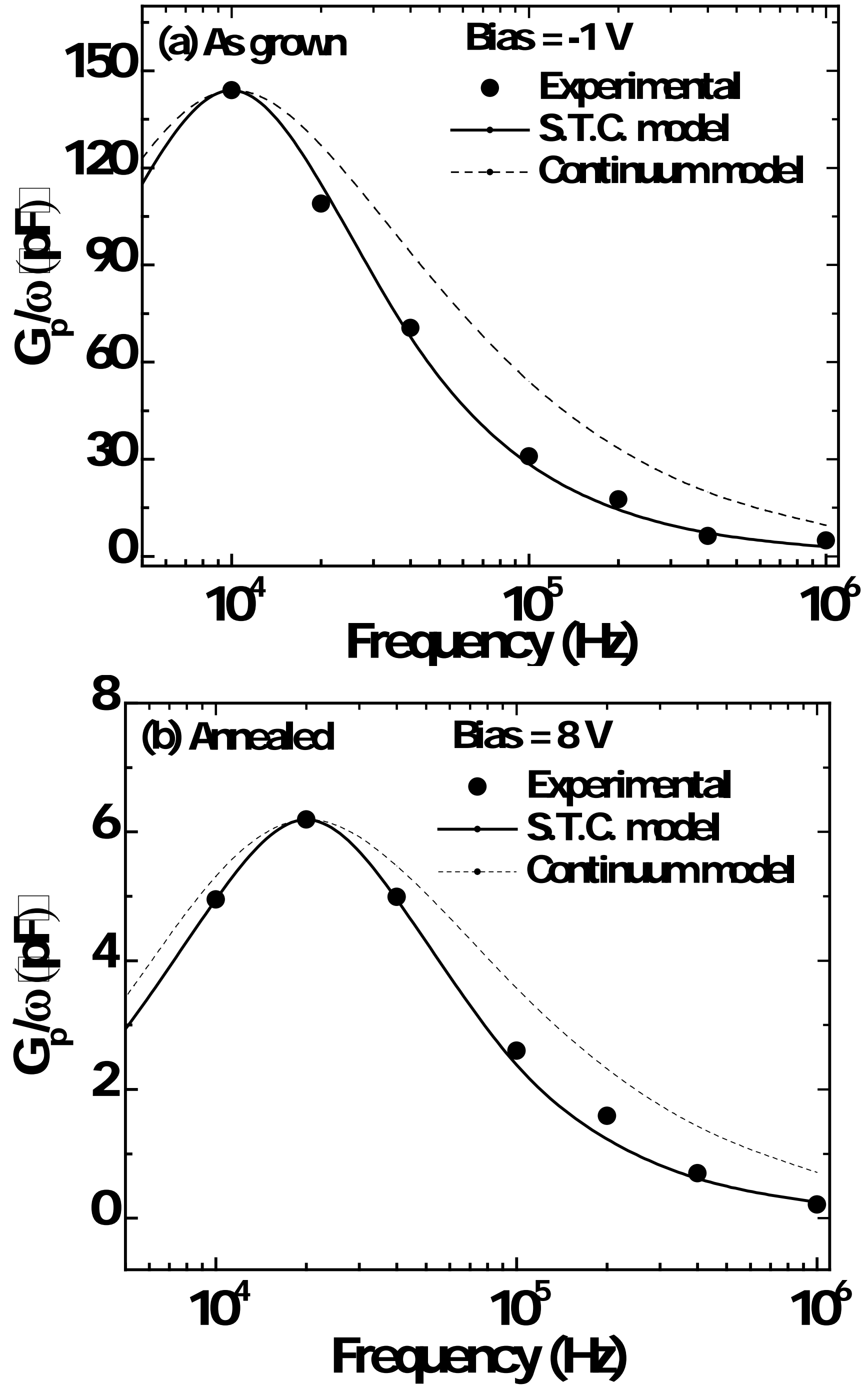


Figure 4.10: Equivalent parallel conductance (G_p/ω) versus frequency at a fixed bias of -1 V for (a) the as-grown sample, and at 8 V for the (b) annealed sample. Both curves match the single-time constant model.

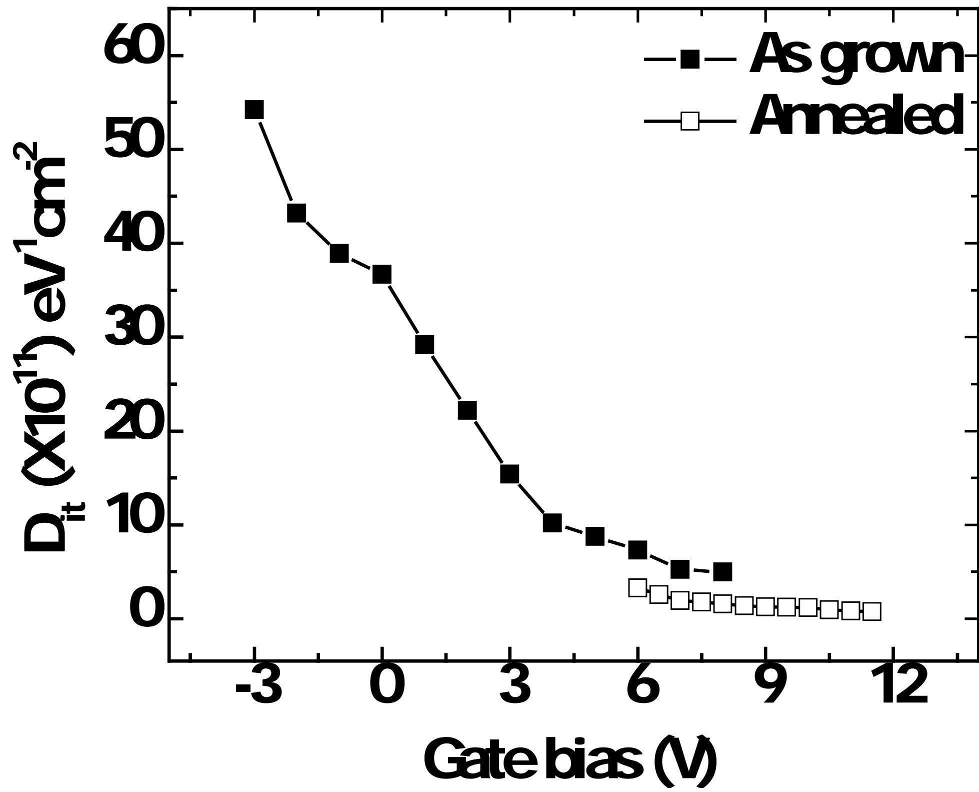


Figure 4.11: Plot of the interface state density (D_{it}) as a function of the gate bias voltage as determined by the conductance method for as-grown and annealed samples.

4.4. Pentacene Field Effect Transistor

There have been tremendous efforts from various researchers about improving device performance of pentacene FETs, especially focus on enhancing field effect mobility and switching speed. Among thin film transistors with an organic semiconductor as the active channel, those fabricated with pentacene have allowed the highest performance. Mobilities up to 1.5 cm^2/Vs and threshold voltages comparables to those obtained with hydrogenated amorphous silicon have been reported by several laboratories [94, 95]. Up to now, the hole mobility of pentacene thin film is continuously improved with great success on chemical synthesis of pentacene and surface treatment of high-*k* inorganic dielectric using self assembled monolayer [96] or use of low-*k* polymer onto high-*k* dielectric to prevent from energetic disorder due to polar dielectric interfaces of high-*k* dielectrics [97].

Pentacene FET using conventional SiO_2 (200 nm) dielectric on heavily doped p-Si wafer which was purchased from Silicon Quest International was fabricated and measured. Cleaned heavily doped Si was used as the substrate and the bottom gate electrode. Here, we have chosen SiO_2 rather than Al_2O_3 because we want to develop simple process and a sample organic FET structure so that we have a capability to further fabricate and characterize metal nanoparticle embedded organic non-volatile memory device. To fabricate pentacene FETs with top contact geometry, 40 nm thick pentacene (sublimed grade, ≥99.9 % trace metals basis, Sigma-Aldrich) active layers were thermally deposited through shadow masks onto SiO_2 gate dielectrics at 70 °C, at a deposition rate of 0.3 Å/s by using the thermal evaporation method at 10^{-6} mbar inside the glove box. Pentacene was used without any further purification. The second shadow mask for

patterning the source and drain electrodes was set in a glove box without exposure to air. The FET was completed by deposition of a 100 nm thick Au layer for source and drain electrodes. The channel length (L) and width (W) were varied from 50 to 250 μm and from 500 to 2500 μm, respectively. Electrical characteristics of the pentacene FETs were measured in air using HP 4145A semiconductor parameter analyzer.

Output and transfer characteristics of pentacene FETs are shown in Figure 4.12. All devices exhibited good linear/saturation behavior in this range of operating voltage, which is a typical of transistor devices. Transfer characteristics also show a plot for the prepared device of the square root of drain current (I_D) in the saturation region at drain voltage (V_D) = -40 V as a function of the gate voltage $V_{G.}$ According to theory [39], above the threshold this plot should yield a straight line with a slope proportional to the mobility, and with an intercept equal to the threshold voltage. By using a linear fit of the plot of transfer characteristics in semilog scale, the threshold voltage in the saturation region were determined as a -3V, which is comparable value of pentacene FET using SiO_2 gate dielectric. The right axis of transfer curve also shows the gate leakage current (I_s) as low as 10^{-10} A. We realized that without patterning pentacene region which is not overlapped in source and drain, there is a significant gate leakage current at 0 V.

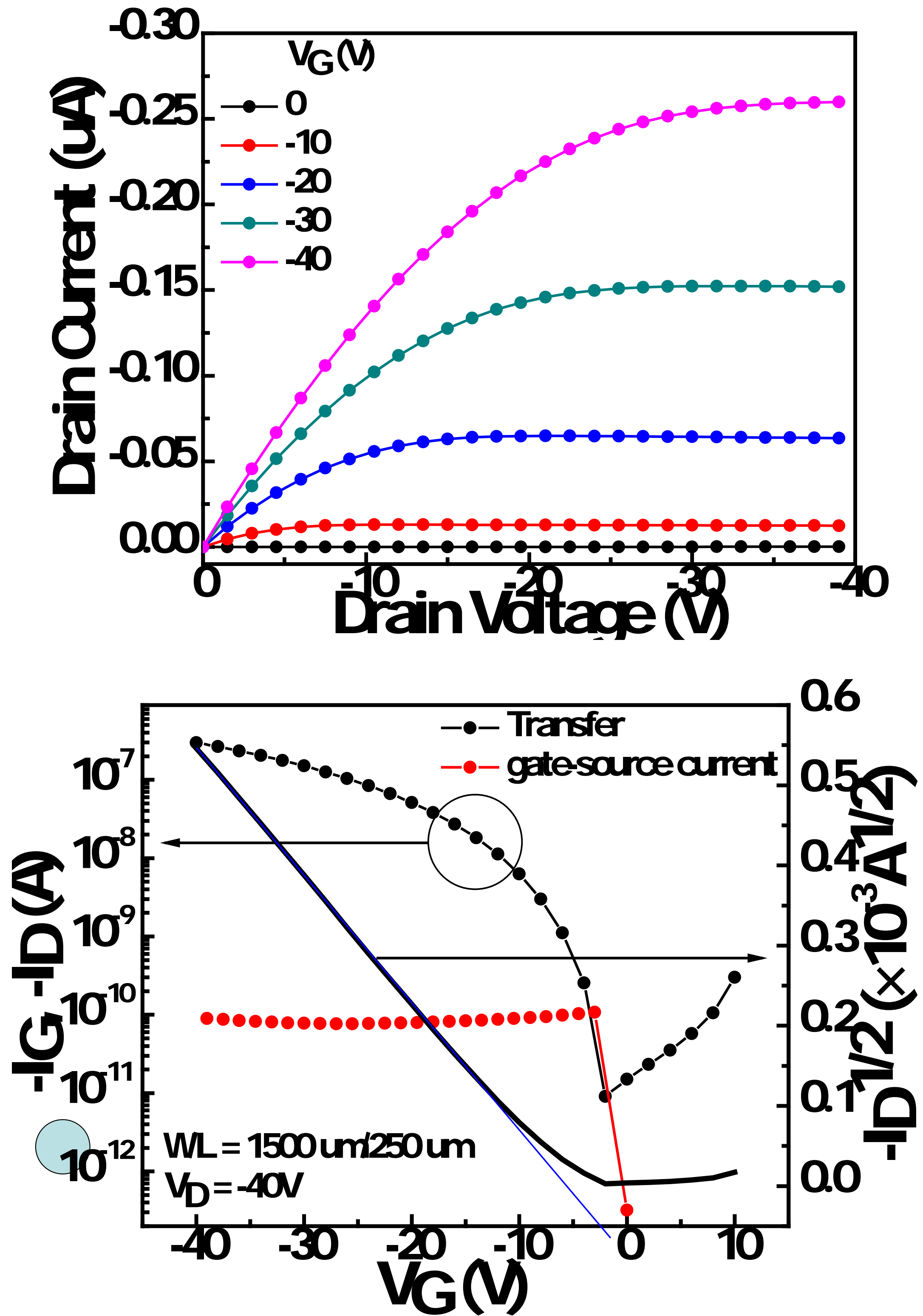


Figure 4.12: Output (top) and transfer (bottom) characteristics of pentacene FET.

Pentacene morphology also affects the performance of FET due to the grain size and degree of crystallinity in pentacene which results in a formation of grain boundary [98]. AFM images were scanned using Agilent 5500 AFM/SPM Microscope. In AC mode non-contact high-resolution silicon tips were used, ~293 kHz resonant frequency, amplitude set point 1.5 to 2 V. Morphology was significantly changed onto different substrates from hydrophilic (SiO_2) to hydrophobic (Tetraethyl orthosilicate, TEOS) due to surface energy matching. Similar surface energy suggests that it may be possible to develop more efficient transistor channels by better matching the surface energies of the gate dielectric and the organic semiconductor [99]. Overall, these works will be a basis for developing metal nanoparticle embedded organic non-volatile Flash memory device.

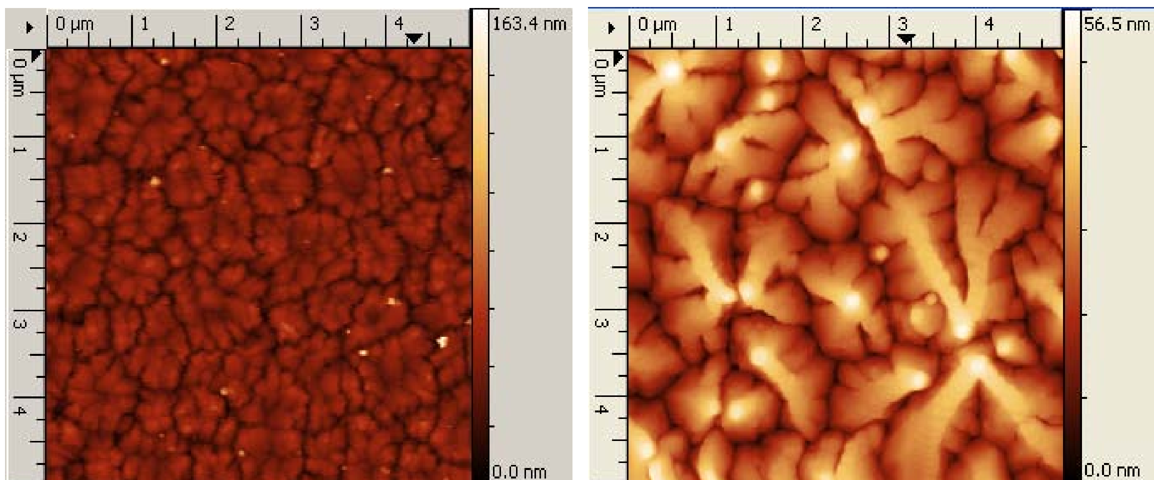


Figure 4.13: AFM images of pentacene onto SiO_2 (left) and TEOS (right) surfaces.

Chapter 5. Pt Nanoparticle Embedded Non-volatile Memory

5.1. Introduction

Non-volatile memory is an essential part of numerous electronic applications. Non-volatile memories using conventional charge storage mechanisms are based on a combination of a structure and a memory element, generally a continuous polycrystalline silicon floating gate. Although a huge commercial success, conventional floating gate devices face serious obstacles due to further downscaling of tunneling oxide thickness [100]. Each material that may address these obstacles offers benefits and limitations. A silicon-oxide-nitride-oxide-silicon (SONOS) type non-volatile memory device suffers from increased stress induced leakage current (SILC) and SiN defects which adversely affect the retention and reliability of scaling [101]. However, discrete charge storage offers better stability and retention characteristics than a continuous charge trap layer due to the lateral electrical isolation of each node. Discrete nanoparticles offer localized charge storage which eliminates the complications of downscaling in SONOS. It allows for 2 bit storage per cell due to asymmetry in read/write of bits which leads to local storage and to multiple bit cells. In addition, nanoparticle embedded memories are characterized by excellent immunity to SILC and oxide defects due to the distributed nature of the charge storage in the nanoparticle layer [102].

Semiconductor nanoparticles have been chosen for developing non-volatile memory device due to an easy formation of nanoparticles. Recently, it has been known that metal nanoparticle embedded non-volatile memory devices are very attractive

because metal has larger work functions and higher density of states than a semiconductor [103, 104] and it is easy to tune the barrier height for carrier injection due to numerous choices of metal [105]. In addition, metal nanoparticles are advantageous compared to semiconductor nanoparticles with regard to scaling down. The bandgap of semiconductor nanoparticles is increased compared to bulk materials due to carrier confinement, which reduces the depth of the potential well of nanoparticles and brings about degraded retention characteristics [106]. When metal nanoparticle is integrated with high-*k* dielectrics for non-volatile memory application, and then it enables EOT scaling aggressively and thus exhibits smaller operating voltage, faster P/E speeds, better data endurance, and long retention characteristics [107]. Nanoparticle of size smaller than 2 nm has the added benefit of the Coulomb blockade effect [108]. This quantum confinement of charge enhances the retention characteristics of a non-volatile memory device [109]. Thus, metal nanoparticles below 2 nm hold the most promise.

Various approaches for the formation of nanoparticle or nanocrystals have been demonstrated. Most techniques, however, suffer from limitations in size uniformity, control of density, and thermal stability. Pt nanoparticle has been used as charge storage cites due to high work function, good thermal stability, and chemical inertness of Pt. There are several ways to form metal nanoparticles using physical vapor deposition. Specific to Pt nanoparticles, two commonly used nanoparticle formation processes include: first, a thermal dewetting process using high temperature rapid thermal annealing (RTA) treatment, which produces 2.2 nm [110] and 4 nm Pt nanoparticles [111], respectively. This technique does not satisfy a low thermal budget and the particle distributions are broad. A second process is direct 5 nm non-spherical shape growth [112],

which shows inability to control uniform and spherical shaped nanoparticles smaller than 5 nm. Recently, we have conducted research on metal nanoparticles formation using sputtering deposition without subsequent high temperature annealing [113]. The simplicity of the direct sputter deposition technique and its compatibility to standard CMOS processes makes the approach highly attractive for use in non-volatile memory devices. In this direct deposition method, the average size of the nanoparticles is simply controlled by varying deposition time with constant deposition pressure, power, and gas flow rate at room temperature. This technique produces uniformly distributed spherical Pt nanoparticles with mean diameters between 0.5 and 2 nm, having high particle density $>10^{12}$ cm^{-2}, and maintaining a necessary interparticle distance. Shrinking nanoparticle size is an important step to realize high density nanoparticle memory design. More importantly, this process is relatively simple and highly repeatable, making it a good candidate for fabrication of non-volatile Flash memory device. Our major motivation for sub-2 nm size tunable metal nanoparticle together with high particle density is for better controllability of different memory capability of scaled non-volatile memory devices followed by different requirements in various applications [114].

In this chapter, size tunable sub-2 nm Pt nanoparticles embedded MOS stacks utilizing thin Al_2O_3 tunneling and control oxide layers is discussed. These devices show different amounts of charging density due to the varied particle size and density. Double Pt nanoparticle layers embedded non-volatile memory shows enhanced memory window compared with single layer device. Finally, its endurance and retention characteristics are demonstrated.

5.2. Experiment

Modified Shiraki [75, 76] cleaned low doped p (100) silicon was used to fabricate MOS capacitors. Initially, e-beam was utilized to deposit a 4.3 nm tunneling Al_2O_3 layer, which its deposition process is described at Chapter 3.2.2. The same thickness of tunneling Al_2O_3 layer was deposited on carbon film grids for TEM analysis. The nanoparticle deposition processes are performed through a computer controlled sputtering system called AJA International ATC 2000-V magnetron sputtering system. The system is a versatile coating tool that can be built in a wide variety of configurations to satisfy almost any requirement. The configuration of ATC 2000-V sputtering system is shown in Figure 5.1.

Followed by tunneling Al_2O_3 layer deposition, samples were immediately transferred to the main chamber of the sputtering system by using loadlock chamber to deposit Pt nanoparticles onto the tunneling oxide with the following deposition times: 5, 10, 20, 30, and 45 s after 15 min of preheating 2 inch Pt target at 90 W (KJLC). The base pressure of main chamber was 1×10^{-7} torr. Precise time of deposition was controlled via shutter valve timing. A deposition power of 30 W RF was used with a working pressure of 4 mTorr and 10 sccm of Ar gas flown at room temperature [113]. The purpose was to determine the best range of deposition times for tunable particle size and density while maintaining spherical shape. More detailed process and its growth mechanisms about forming nanoparticles were described in David *et al*. [113]. The distance between Pt target and substrate plays an important role to determine the size and density of Pt nanoparticle. We used our possible minimum distance to have short working distance to form uniform nanoparticle.

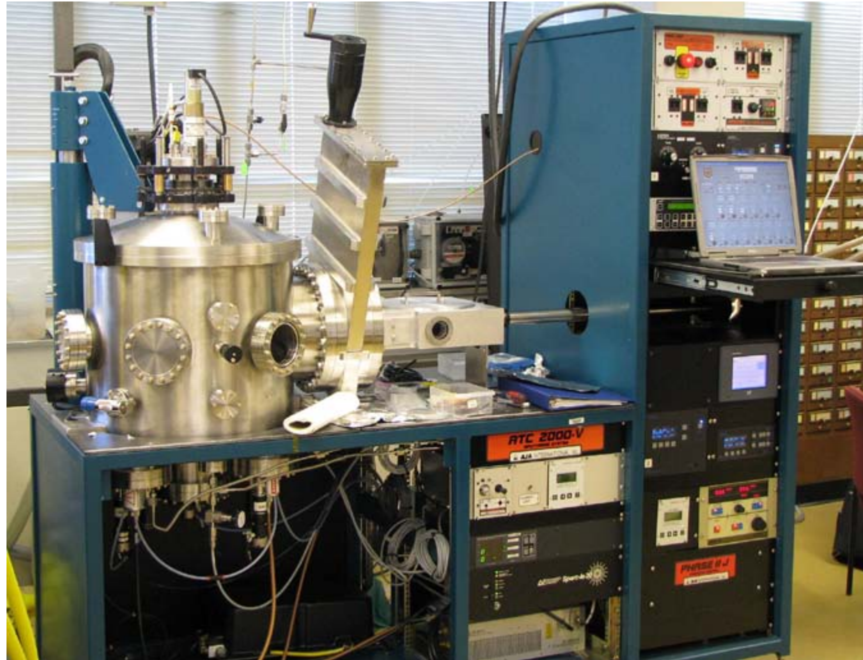


Figure 5.1: AJA's computer controlled ATC 2000-V sputtering system.

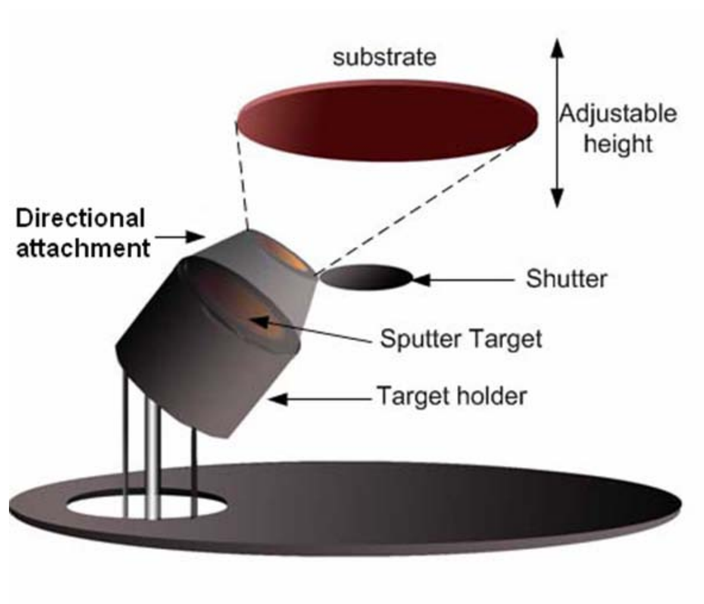


Figure 5.2: Schematic diagram of main chamber of the sputtering system.

Samples were again transferred to the e-beam system for 14 nm Al_2O_3 control oxide deposition and subsequent *in-situ* H_2 gas annealing at 260 °C for 45 min. E-beam grown 4 nm interdielectric Al_2O_3 is used to make double layer Pt nanoparticles embedded MOS stack with incorporation of 2nd Pt nanoparticle layer. Here, a relatively thick control oxide is utilized to minimize any charge injection from the top electrode. Finally, e-beam evaporated 250 nm Ti electrodes of 4.42×10^{-5} cm^2 were deposited onto the control oxide under the both based and working pressure of below 10^{-7} torr to avoid oxidation of Ti during evaporation. The samples were held in a stainless steel holder. A specially designed molybdenum shadow mask with 500, 250, 150 and 75 μm diameter apertures was used to pattern the top contacts. A control sample without embedded Pt nanoparticles was also prepared by the same process to verify that the memory effect is solely from trapped charges at the nanoparticles, and not from defects in the Al_2O_3 [115]. Final device structure is shown in Figure 5.3.

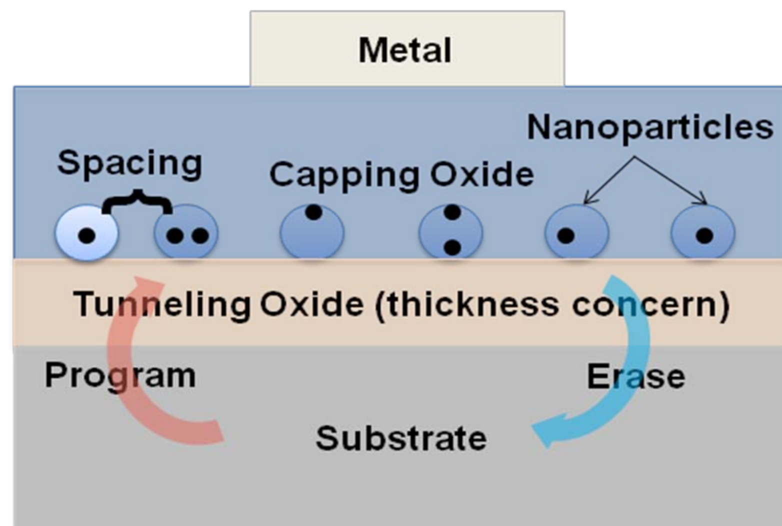


Figure 5.3: Schematic diagram of nanoparticle embedded non-volatile memory.

High frequency C-V measurements were performed at room temperature using a Keithley 4200-SCS equipped with the 4200-CVU integrated C-V option and pulse generator. Data was taken with a voltage step of 0.1 V and 30 mV AC signal at 1 MHz in a dark ambient. For the C-V sweep, no stress or presoak voltages were applied to measure memory window. The delay time was 0.5 s with long integration time. The device was swept from inversion to accumulation for electron injection and was followed by reverse swept voltages for hole injection without holding time. On the other hand, enough pre-stressing is required before starts C-V sweeping for dynamic characteristics such as endurance and retention. Figure 5.4 shows the example of measurement flow of dynamic characteristics. Note that all C-V profiles were corrected for the possible presence of series resistance [39].

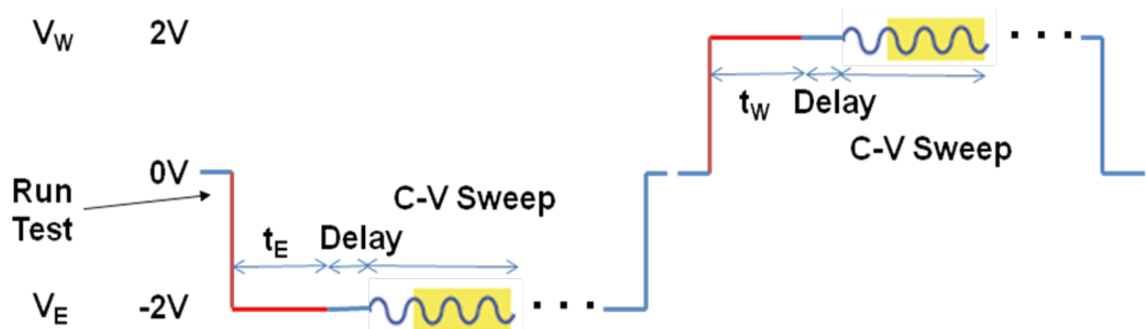


Figure 5.4: Example of measurement flow of dynamic characteristics. V_W and V_E denotes write and erase voltages, respectively. t_W and t_E denotes stressing duration time for write and erase voltages, respectively.

5.3. Discussion

Studies of Pt nanoparticles embedded in Al_2O_3 matrix have been conducted. The Pt nanoparticles range from 0.8 to 2.2 nm in diameter (Figure 5.5) with $> 5 \times 10^{12}$ cm^{-2} particle layer density. Although it is not shown here, the average diameter of particles is slightly smaller when deposited on Al_2O_3 as opposed to deposited directly on carbon support films. In this process, we believe that the point defects present in amorphous dielectric medium act as nucleation sites with high trapping energies for the formation of nanoparticles and hence make the composite thermally stable to 800 °C and higher [113].

In our Pt nanoparticles formation at room temperature using sputtering deposition system, we exploit the earliest stages of film growth where metal clusters arrive on the substrate surface and diffuse until encountering nucleation (trap) sites [116, 117]. Small clusters remain trapped at these sites and grow in size due to the continuous flux of atoms. The large surface energy difference between Al_2O_3 (40-50 mJ/m^2) and Pt (2190 mJ/m^2) dictates a Volmer-Weber type islanding growth mode with spherical particles. As atoms impinge the surface, they diffuse until they find high trap energy nucleation sites. A certain density of these traps is filled, which corresponds to the maximum particle density. As more material is deposited on the surface, the particles grow spherically and homogeneously until at a certain size they start to coalesce with neighboring particles. In our particle formation method, we are concerned with the region where the particles have not coalesced. Also, deposition temperatures higher than 300 °C cause a significant drop in particle density due to surface diffusion. Using deposition temperatures below this value yields virtually no difference in particle density. These particle density findings are consistent with scaling theories and experiments by J. A. Venebles *et al.* s' work [118].

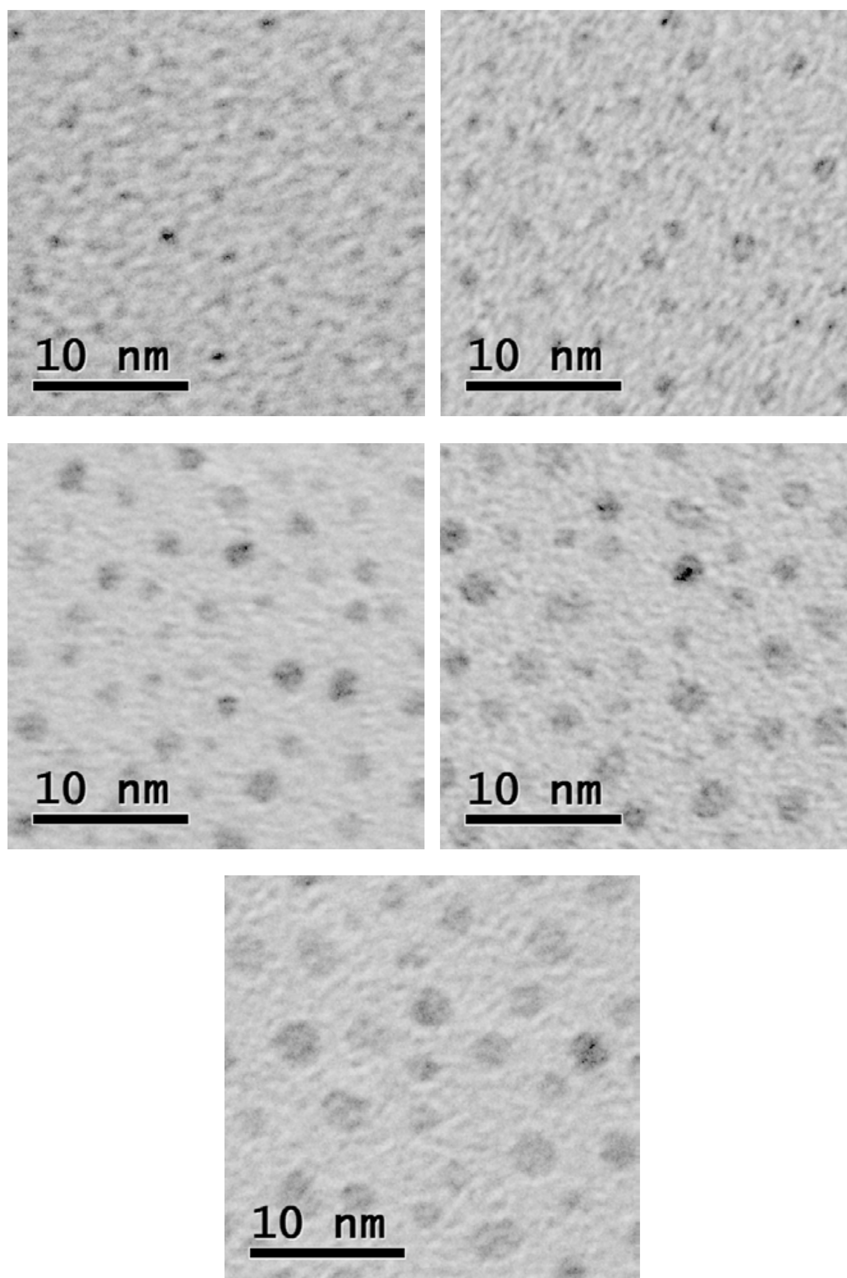
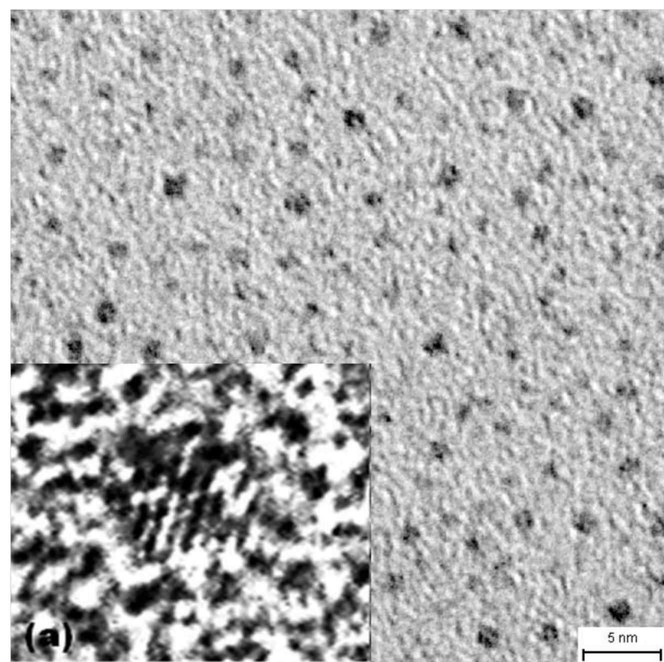


Figure 5.5: TEM images of Pt nanoparticles formation held for 10, 20, 30, 40, and 50 s (top to bottom, left to right). The mean diameter of the Pt nanoparticles is 0.8, 1.2, 1.5, 1.8, and 2.2 nm, respectively.

Figure 5.6 shows the plane view transmission electron microscopy (TEM) image (a) and size distribution analysis (b) of 20 s deposited Pt nanoparticles, whose average size and density are estimated as 1.14 nm and 4.87×10^{12} cm^{-2}, respectively. The high resolution TEM (HRTEM) image in inset of Figure 5.6 (a) shows the monocrystalline structure of the Pt nanoparticle. We have found particle size distribution of the sample over 3 images of 2 samples after statistical post-image analysis using The Scanning Probe Image Processor (SPIP™) 5.0 image software from Image Metrology A/S Company. Table 5.1 summarizes the nominal layer thickness, size, and density of Pt nanoparticles according to the different deposition time. The extreme error in the 5 s analysis is caused by the background noise which is a result of the lack of contrast between the nanoparticles and the amorphous substrate material. As the particle size increases, the contrast between the nanoparticles and background increases, which decreases the measurement error in the analysis.

We have provided an estimate of the nominal thickness at the Table 5.1 based on the mean particle diameter and density assuming that the particles are spherical. This is a reasonable assumption based on the large surface energy difference between alumina and Pt, which dictates that particle formation should be spherical. This assumption is also corroborated by the fact that the particle growth versus time fits the $t^{1/3}$ law [119]. The 1/3 exponent arises when growth is isotropically three dimensional. Deviations from this exponent indicate anisotropic or two-dimensional growth. Experimental evidence of three-dimensional growth of Au on SiO_2 performed with a similar sputtering method can be found in cross sectional images in S. H. Cho *et al.* [120].



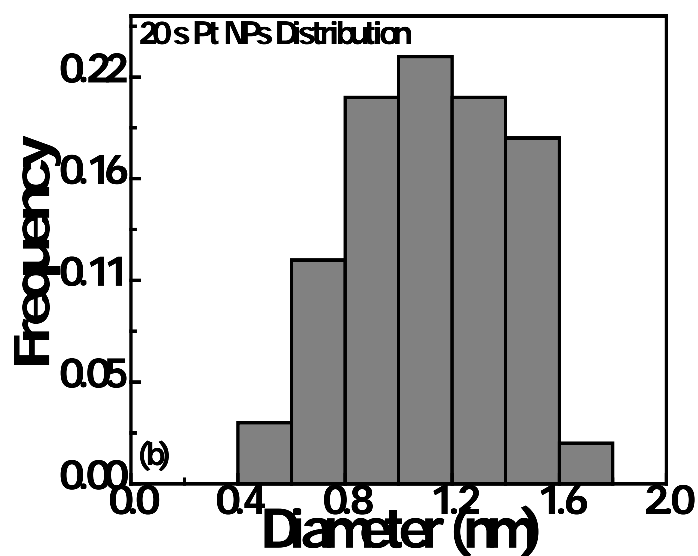


Figure 5.6: (a) Planar view TEM images of 20 s deposited Pt nanoparticles on a 4.3 nm Al_2O_3 layer on a carbon film grid. It has 1.14 nm average particle diameter with 4.87×10^{12} cm^{-2} particle density. The inset in (a) shows monocrystallinity of Pt nanoparticle identified by HRTEM and (b) Particle size distribution of 20 s deposited Pt nanoparticle samples over 3 images after statistical post-image analysis.

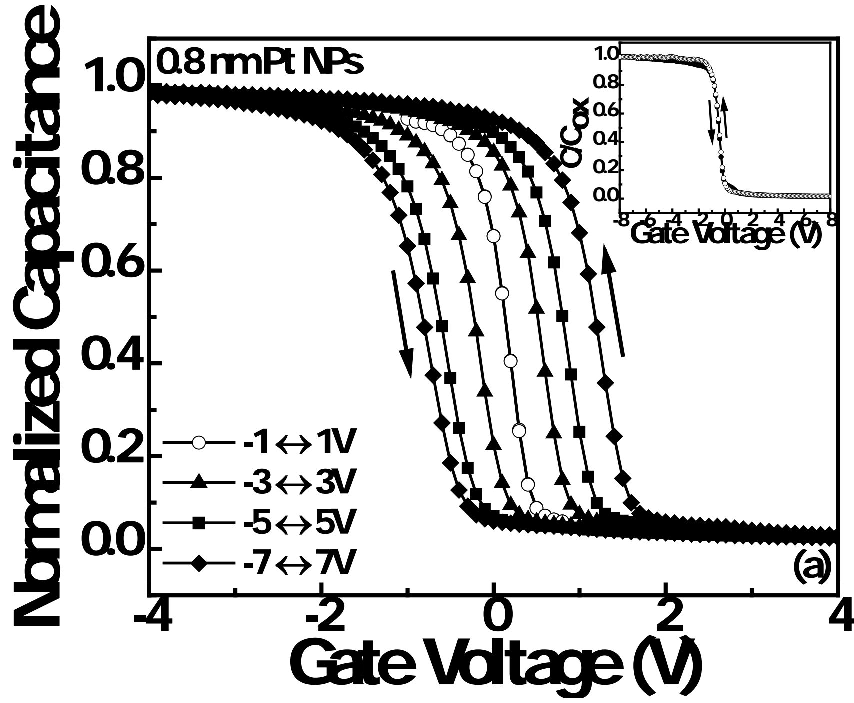
Deposition time (s)	5	10	20	30	45
Nominal thickness (nm)	~0.02	~0.11	~0.38	~0.94	~2.00
Average size (nm)	~0.5	~0.8±0.1	~1.14±0.07	~1.54±0.05	~1.98±0.02
Average particle density ($\times 10^{12}$ cm^{-2})	~1-3	~3.95±1.08	~4.87±0.63	~4.9±0.85	~4.85±0.2
Memory window (V)	0.92	2.03	4.26	3.78	1.63
Electron charge density ($\times 10^{12}$ cm^{-2})	1.1	2.3	4.7	4.3	1.9
Number of electrons per nanoparticle	0.36-1.1	0.58	0.97	0.77	0.39

Table 5.1: Summary of Pt nanoparticles as a function of deposition time.

Au and silica have a similarly large surface energy difference (Au: 1250 mJ/m^2 and SiO_2: 61 mJ/m^2) in our case.

Figure 5.7 (a) and (b) show the C-V curves of 0.8 and 1.14 nm Pt nanoparticles embedded memory device under different sweeping voltage operation. In the experiment, MOS devices were first scanned in a very narrow range between +1 and -1 V (±1 V sweep) to find the region where no hysteresis was found; indicating no charging of the Pt nanoparticles. The control and active devices have negligible hysteresis when uncharged, shown in the initial voltage sweep (open circles). The left three branches represent hole charging states while the right three branches represent electron charging states. Flatband voltage of this range is initial V_{FB} and used for V_{FB} shift calculation. Counterclockwise hysteresis loops are observed under all sweeping voltages, indicating electron injection from substrate to Pt nanoparticles under positive voltage for the program operation and hole injection (electron detrapping) under negative voltage for erase operation by F-N tunneling [121].

The inset of Figure 5.7 (a) shows that there is a negligible hysteresis in control sample under the same applied voltage. In addition, the leakage current density of Pt nanoparticles embedded sample at 4 MV/cm is 3×10^{-8} cm^{-2}, which is comparable to the control sample. Thus, the V_{FB} shift of the active device is attributed to electron charging in Pt nanoparticle or at the interface between nanoparticle and Al_2O_3, not from the defects in Al_2O_3 or the interface states between Al_2O_3 and Si [122]. Swept C-V curves, Figure 5.7, show symmetric V_{FB} shift in both positive and negative voltage region.



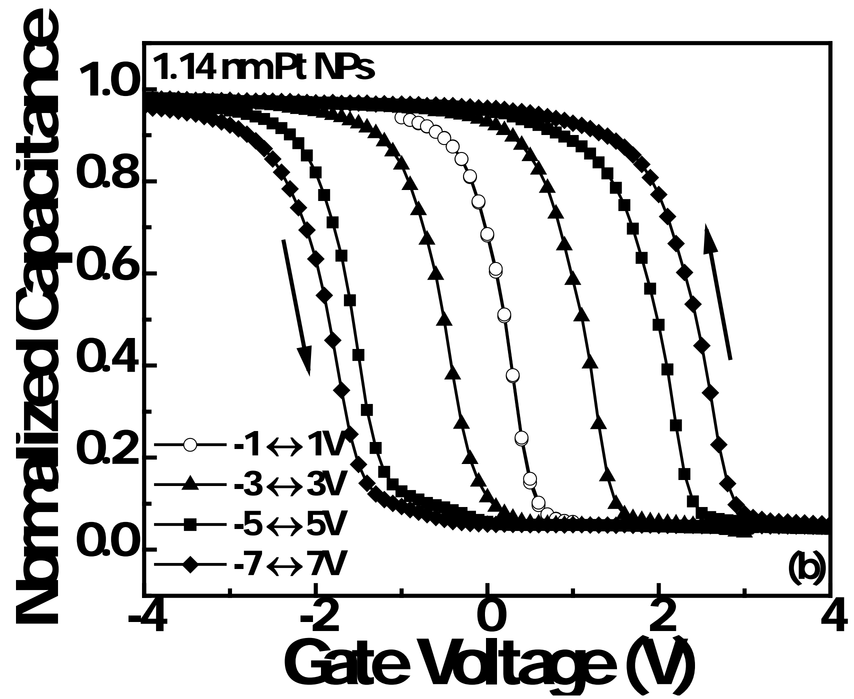


Figure 5.7: Typical high-frequency (1 MHz) bi-directional C-V curves of 0.8 nm (a) and 1.14 nm (b) Pt nanoparticles embedded memory device under different sweeping gate voltages.

Unlike pure hole charging of monodisperse 1 nm Si nanoparticle system [123], we obtained fairly symmetric electron and hole charging from different size of Pt nanoparticles embedded samples. In addition, although the use of Al_2O_3 for the tunneling layer substantially decreases the tunneling efficiency as the overall barrier profile is too high to induce a F-N tunneling at a moderate voltage [55], we successfully demonstrate gate voltage dependent memory window under ±7 V with the benefit of Coulomb blockade and quantum confinement effects in ~1 nm Pt nanoparticles. The size of nanoparticle plays a critical role in the memory performance. It was also shown that V_{FB} shift under different sweeping voltage gradually increased with a uniform increase of F-N injection and finally saturated or degraded over a certain value above the measurement range. The saturation of V_{FB} shift can be explained by both high tunneling probabilities after filling the effective potential well and the limited capacity of capturing electrons of ~1 nm nanoparticles. However, the saturation behavior of V_{FB} shift should be explained in terms of density of states of the nanoparticles and will be remained in the future work. Degradation is attributed to the applied voltage that is close to the breakdown field of dielectric or the coupling between control gate and nanoparticle [107].

The observed saturation is attributed to the Coulomb blockade effect taking place while Pt nanoparticles are charged. Note that we used medium sweeping rate with 0.5 s delay to avoid C-V stretch-out and small memory window. In addition, we annealed the sample with no contact under vacuum chamber or RTA at 450 °C to check if any plasma damage during Pt nanoparticles formation can induce the charge trapping process via nanoparticles. V_{FB} shift before and after annealing were no changes.

Interestingly, there is a remarkable difference of memory window between 0.8 and 1.14 nm Pt nanoparticles embedded sample. The V_{FB} shift as a function of P/E voltages according to the different size of Pt nanoparticles is plotted in Figure. 5.8. Note that there is slight charging state of 1.98 nm Pt nanoparticle sample at 1 V, and it cannot be further reduced by narrow biasing for the extraction of V_{FB}. Initially, there is no memory effect in the control sample, but the V_{FB} shift increases gradually with increased size and density of Pt nanoparticles. Among samples, a 1.14 nm Pt nanoparticle sample has maximum particle density and optimum interparticle distance in our deposition method and therefore shows maximum memory window [124]. However, as the particle size increases more over 1.14 nm, memory window decreases due to the following reasons: First, particle density slightly decreases and more greatly interparticle distance is narrowed by increasing particle size. We believe the possibility of charge hopping between neighboring particles increases after passing the necessary interparticle distance. Second, Coulomb charging force decreases as particle size increases and hence as the size of particle increases the capability of charging electrons of Pt nanoparticle decreases. We believe that charging behavior is the interplay of Coulomb force and particle size, density, and interparticle distance. Also, some of the individual particles were aggregated at longer deposition times above 40 s.

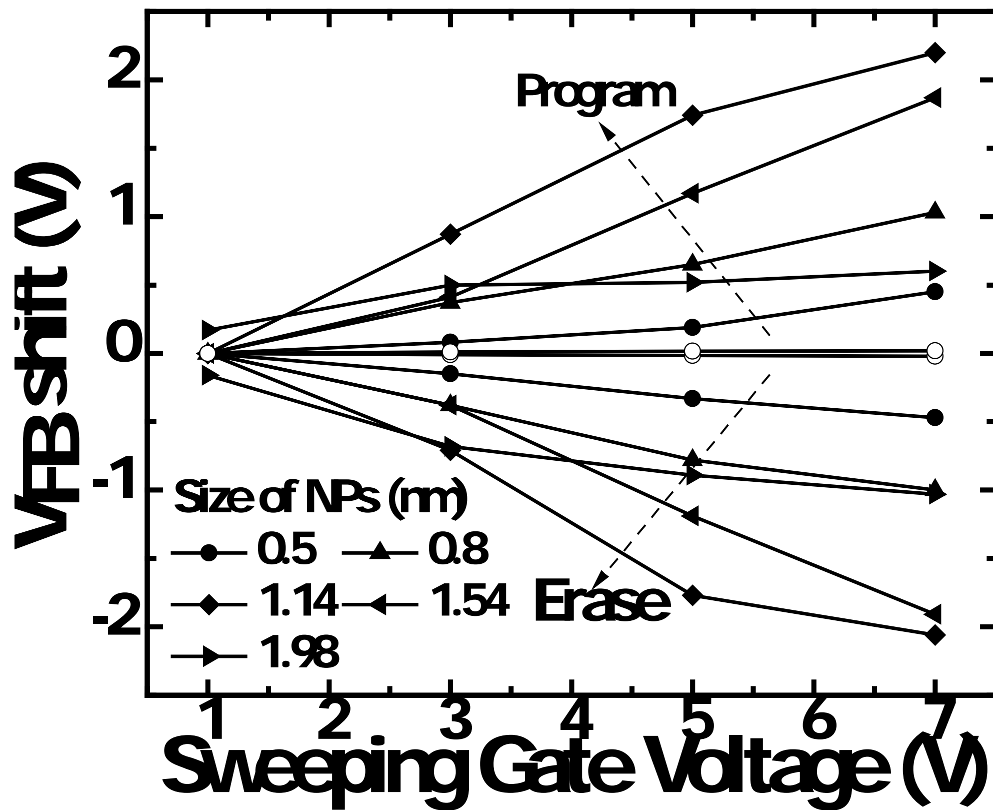


Figure 5.8: Flatband voltage shift as a function of program/erase voltages from C-V curves according to the different size of Pt nanoparticles. Negligible V_{FB} shift in the control samples is shown (light open, labeled).

However, the above explanation regarding the maximum memory window with 1.14 nm Pt nanoparticles is still unclear even though previous paragraph had explained the reason behind. When we carefully check the figures listed in the Table 5.1 in more detail, we can easily find the explanation seems not so persuasive in some range of Pt nanoparticle samples. First, for example, the average particle density for 1.14 and 1.98 nm nanoparticles are 4.87×10^{12} cm^{-2} and 4.85×10^{12} cm^{-2}, respectively. There is no big difference in these two particle densities, but the memory window drops more than 50% from 4.26 to 1.63V. Therefore, the slight decrease of Pt nanoparticle density after 20 s may not be a part of the reason for reduced memory window.

Second, ascribing shrinkage of memory window to the hopping of storage charge to the neighboring particle seems not reasonable. The hopping charge still remains in the cell. The charge centroid will not change after the charge tunnels from one particle to another particle. As a result, V_{FB} will not significantly change. Moreover, the empty particle after charge hopping is also able to capture another charge if the injection period is sufficiently long since the injection time is long enough by using C-V programming. Thus, the theory about charge hopping still needs to be checked by more comprehensive C-V programming with different injection times.

Finally, charging capability is closely related to the diameter of nanoparticle; particle of smaller size has larger electric field. This can be identified with comparison of different C-V sweeping speed result. In a very short period, it is very likely to see its impact on the programmed window. But, again, for long period memory window is determined by the number of storage charge sites rather than charging capability. We also believe that charging capability is closely related to the size of the nanoparticle, but it

needs to be verified through further experiments. Therefore, the exact nature of the decreasing memory window is still not clear and we are striving to find the reason using the transient P/E result of each different size of Pt nanoparticles embedded samples for clarifying this issue. Complete C-V and G-V measurements with different scan rates will be remained in the follow-up study.

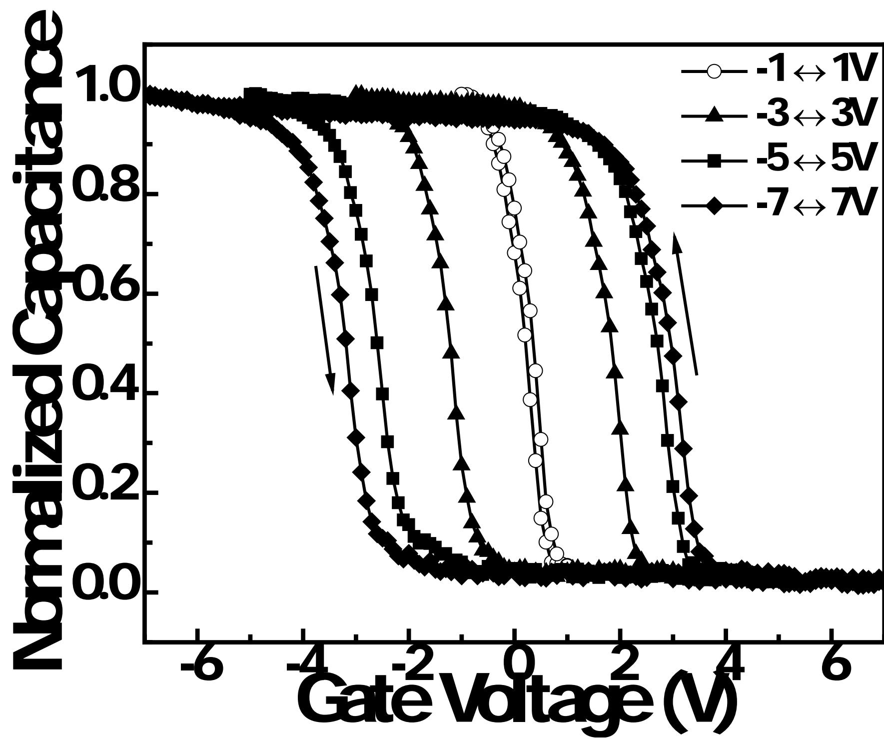
Since the C-V curve between ±1 V with no memory window is located approximately in the middle of the hysteresis loop for each device, the amount of electron storage in Figure 5.7 will be half of the area of the hysteresis loop. By using the relationship,

$$N_t = \frac{C_{OX}\Delta_{FB}}{q} \tag{5.1}$$

where N_t is the trapped charge and Δ_{FB} is the V_{FB} shift, we find that 1.14 nm Pt nanoparrticle with particle density (4.87×10^{12} cm^{-2}) and electron charge density (4.7×10^{12} cm^{-2}) after programming, each Pt nanoparticle serves one electron storage node due to the small ~1 nm size of nanoparticle, which is truly single electron memory device. We also checked the effect of high temperature annealing on the performance of the samples to determine the thermal stability of the nanoparticles when constrained in a dielectric matrix. TEM image and C-V curve reveals little to no change in the particle size, distribution, and density for annealing up to 950 °C [113]. This indicates the compatibility of our process to standard CMOS process necessary for complete implementation of MOSFET.

Owing to the easy process of our Pt nanoparticle formation at room temperature, we also successfully demonstrate double layer Pt nanoparticles embedded non-volatile

memory device where their C-V curves were shown in Figure 5.9. The memory window of 20 s (1.14 nm) and 30 s (1.54 nm) double layer devices is slightly lower than two fold increase memory window of their single layer devices probably due to the possible loss of charge injection into 2nd Pt nanoparticle layer, but this work denotes that with the use of multi-layer Pt nanoparticle layer there is a great potential to significantly enhance memory widow by stacking capability of nanoparticle. Several factors such as the thickness of interdielectric layer, charge injection and loss mechanism via 2nd nanoparticle layer needs to be investigated in order to make highly controllable multi-layered Pt nanoparticle embedded memory device. In addition, tunneling and capping oxide of HfO_2 or its combination with Al_2O_3 matrix is built to further engineered barrier height of nanoparticles on high-*k* dielectrics.



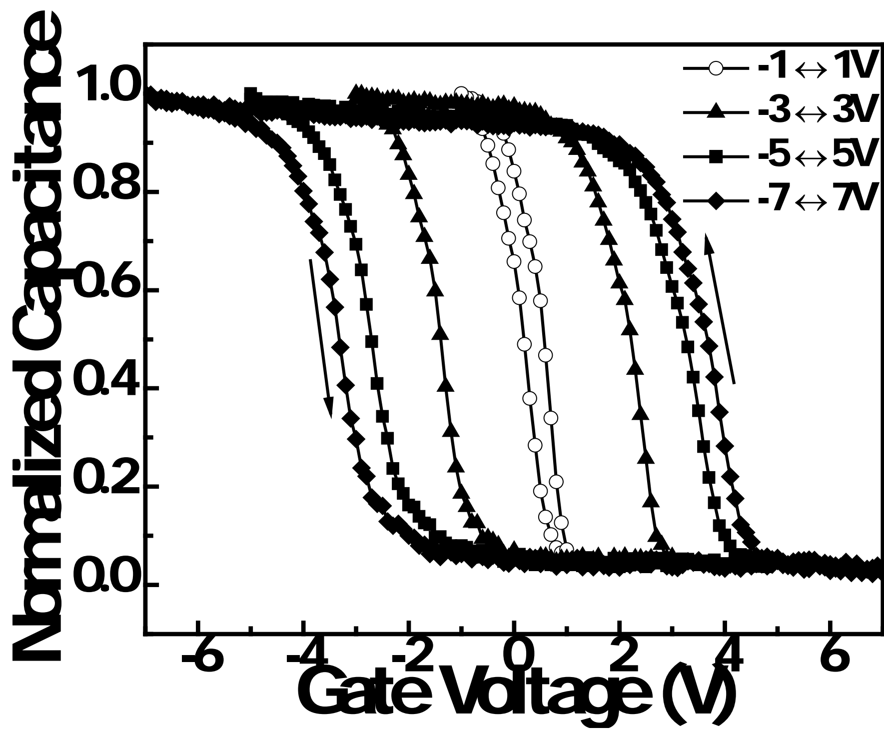


Figure 5.9: Typical high-frequency (1 MHz) bi-directional C-V curves of double layer 1.14 nm (a) and 1.54 nm (b) Pt nanoparticles embedded memory device.

Endurance testing stresses the DUT with a number of P/E waveform cycles, and then periodically measures both the V_{FB} in the programmed and erased states. The purpose of this test is to determine the lifetime of the DUT, based on the number of P/E cycles withstood by the device before a certain amount of shift, or degradation, in either the programmed or erased states. As shown in Figure 5.10 (a), endurance characteristics of the 1.14 nm Pt nanoparticle embedded memory devices were observed for up to 10^5 cycles with 100 ms stress pulses of ±6 V, demonstrating a stable memory window. The V_{FB} shift is defined as the difference of V_{FB} at the time of interest and at the beginning. No significant memory narrowing is observed up to 10^5 cycles.

The memory device also shows good retention characteristics when applying a 5 s stress pulse of 7 V program voltage and sweeping C-V periodically at room temperature, as shown in Figure 5.10 (b). The percentage of charge loss is calculated using the expression,

$$(1 - \frac{V_{FB}(t)}{V_{FB}(0)}) \times 100 \qquad (5.2)$$

where V_{FB} (0) is the V_{FB} after stressing and V_{FB} (t) is the V_{FB} at the time of interest. Initial capacitance abruptly drops by 10 % within a short time due to tunneling back of electrons and then maintains its V_{FB} up to 10^5 s because of buildup of a high opposing electric field in the tunnel oxide.

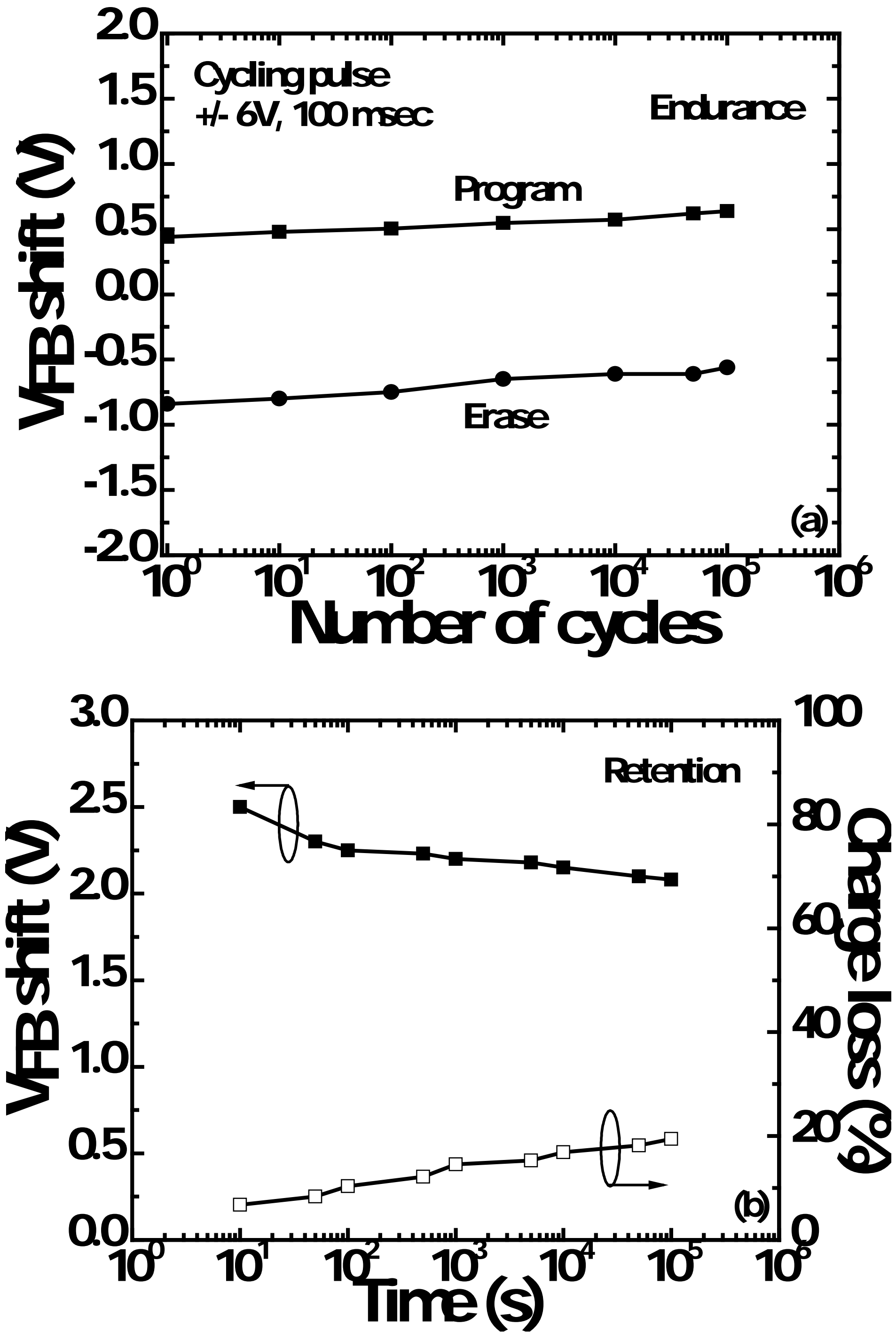


Figure 5.10: (a) Endurance characteristic of 1.14 nm Pt nanoparticles embedded memory device. Memory window remains unchanged even after 10^5 P/E cycles. (b) Retention properties of the memory device at programming and its charge loss percentage vs. time.

Chapter 6. Conclusion and Future Work

6.1. Conclusion

Hybrid metal-oxide-semiconductor structures with conjugated polymer, PF2/6 as the active polymer semiconductor layer, Al_2O_3 as the insulating oxide layer, and highly doped p-Si as the metal layer have been characterized by means of C-V and G-V methods. The negative shift of the flatband voltage with increasing frequency arises from positive interface charges in the (PF2/6)/Al_2O_3 layer. From C-V measurements the unintentional doping density is evaluated as ~5.7×10^{17} cm^{-3} at frequencies above 20 kHz. The interface trap density is estimated as ~7.7×10^{11} $eV^{-1}cm^{-2}$ at the flatband voltage. We also present detailed frequency dependent C-V and G-V characteristics of the semiconductor/dielectric interface.

It also has shown the influence of thermal cycling of PF2/6-based MOS structure on the interface properties using C-V and G-V measurements. PF2/6 undergoes a transition to an ordered crystalline phase upon thermal cycling from its nematic liquid crystalline phase, confirmed by our AFM images. Thermal cycling of PF2/6 films on Si substrates results in particles with an average footprint area of ~10^4 nm^2, as evident from the AFM images. This results in a reduction of the open charge centers and a decrease of charge migration into the polymer layer in MOS structures, thus reducing the magnitude of hysteresis in the C-V curves. In addition, thermal cycling of the PF2/6 films significantly improves the quality of the (PF2/6)/Al_2O_3 interface, which is identified as a reduced hysteresis in the C-V curve and a decreased interface state density from ~3.9 ×

10^{12} $eV^{-1}cm^{-2}$ to ~3.3×10^{11} $eV^{-1}cm^{-2}$ at the flatband voltage. Interface states give rise to energy levels that are confined to the semiconductor/dielectric interface. A conductance loss peak, observed due to the capture and emission of carriers by the interface states, fits very well with a single time constant model from which the D_{it} values are inferred. Annealing reduces the interface trap density at the (PF2/6)/Al_2O_3 interface and frequency dispersion in depletion region of the C-V curve. Further, enhanced charge carrier density in the annealed film is attributed to the morphological changes in the PF2/6 film as it goes through crystallization. The high quality interface of Al_2O_3/annealed (PF2/6) enables its application in high performance FETs and other organic devices.

Sub-2 nm size tunable Pt nanoparticles using room temperature sputter deposition with a simple variation of deposition time were embedded into Al_2O_3 double layers to develop non-volatile memory devices. The memory devices show different amounts of memory window from 1 to 4.5 V under low P/E voltages, good endurance, and long retention properties without narrowing. Our approach to develop metal nanoparticle embedded non-volatile memory device is very appealing in its performance characteristics and is compatible with current semiconductor processing. It can also be used to fabricate memory devices on flexible substrate using spincoated organic semiconductor due to the low temperature nanoparticles formation.

6.2. Future Work

Multi-layer Metal Nanoparticles Embedded Non-volatile Memory

In chapter 5 we had successfully fabricated Pt nanoparticle embedded non-volatile flash memory structure. Based on the finding, we will try to increase the nanoparticles density and the number of nanoparticle layers to improve memory properties and behavior. In terms of device structure, it has shown that double layers of nanoparticles have improved retention and charge density over single layers and can be programmed under similar voltage conditions as used for single layer nanoparticle. The leakage of stored charges in the upper layers to the channel can be suppressed due to the presence of the interdielectric oxide which also acts as second tunneling layer. This will be further extended to create multiple layers of nanoparticles embedded in the dielectric where each layer of nanoparticles can be composed of either the same metal or a different metal leading to varying P/E windows.

Integration with CMOS

Due to the formation of nanoparticles via CMOS compatible deposition system such as sputtering and e-beam, we can incorporate metal nanoparticles into a standard MOSFET structure to fabricate non-volatile flash memory devices. For this purpose, we will use 3-photomask level process as its key step shown in Figure 6.1. Starting with a cleaned p-Si wafer, then 4 nm Al_2O_3 tunneling oxide is grown by e-beam. Then the metal nanoparticle formation procedure is carried out, followed by Al_2O_3 capping oxide via e-beam. The control gate is formed on top of it by sputtering of W (Figure 6.1 (a)). The

gate is patterned with 1st photomask and etched by reactive ion etching. Then As^+ or P^+ (~10^{20} cm^{-3}) ion implantation followed by RTA at 800 °C is performed to form self-aligned source/drain (S/D) (Figure 6.1 (b)). Another 500 nm PECVD oxide layer is deposited to provide spacer isolation between gate and S/D. Then contact windows to both the gate and S/D are opened with 2nd photomask and etching (Figure 6.1 (c)). Finally W is sputtered (Figure 6.1 (d)) and patterned with 3rd photomask for the final metallization (Figure 6.1 (e)). A series of photomasks is designed with AutoCAD and converted into proper IC design software. Few key processes including fabrication of 3 photomasks and ion implantation must be worked with our collaborator, NCSU, due to the limitation of facilities in here.

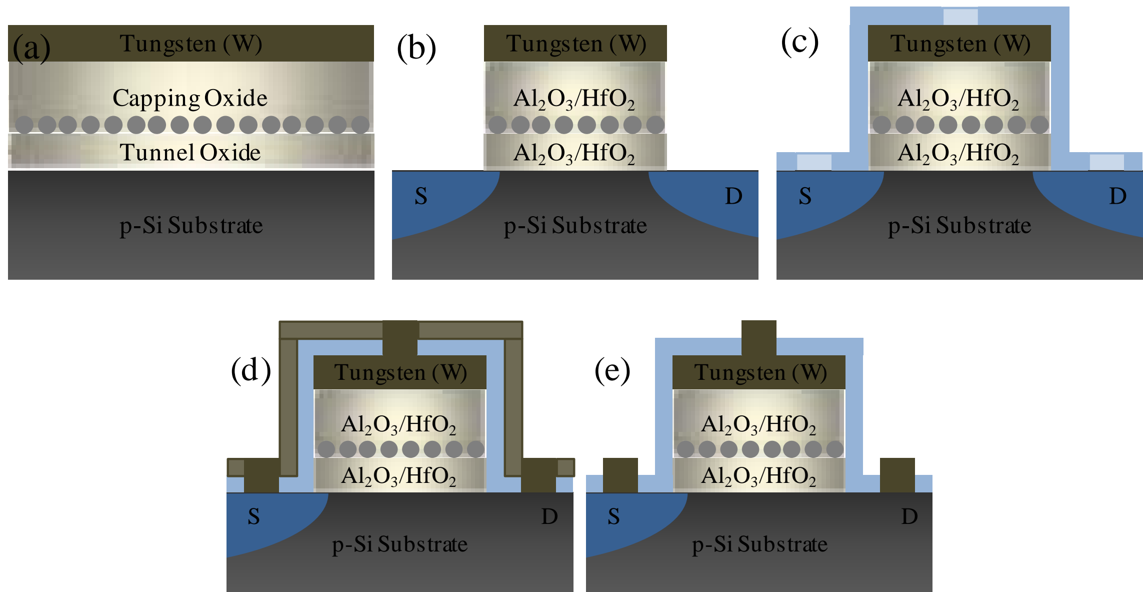


Figure 6.1: Process flow for the fabrication of Pt nanoparticle embedded n-channel Si-based non-volatile flash memory cell.

Metal Nanoparticle Embedded Flexible Polymer Based Non-volatile Memory

Due to the ability of our metal nanoparticle formation at room temperature, my major future work is to develop non-volatile memory device based on all organic semiconductor and dielectrics. Polymer based non-volatile memory devices have recently been considered for alternate cost-effective memory applications due to its simple structure, lower cost, and the stacking capability with high densities. Most polymer based non-volatile memories, however, were fabricated by mixing metal nanoparticles with polymer. This may not offer very high density and uniform distribution. Our approach can be utilized for fabricating nanoparticles embedded polymer based non-volatile memory devices at low temperature for flexible electronics application.

As for flexible devices, the usage of inorganic oxides as gate dielectrics could eventually lead to cracks and structural defects in the film under mechanical stress. It is possible to fabricate polymer non-volatile memory devices onto flexible substrates at temperatures below 200 °C. First of all, we will deposit metal nanoparticles through voids in polymer films or nanowires or nanoparticles and study the overall size, distribution, and thermal stability of metal nanoparticle/polymer composites. Voids between the polymer chains will determine the actual size of the metal nanoparticles. In addition, electronic charges present in conducting polymer will provide the electric shield of the metal nanoparticles and prevent the coagulation of each nanoparticle and hence improve the electrical properties of non-volatile memory. Next, as its device structure shown in Figure 6.2, we will build a conventional non-volatile memory device consisting of metal nanoparticles embedded semiconducting or insulating polymers with tunneling and capping polymer dielectrics and new types of non-volatile memories such as

nanoparticles embedded solid state ionic memory and polymer resistive memory. Thus, ultimately all organic memory devices onto flexible substrate are to be developed in near future.

Metal Nanoparticle Embedded Transparent Non-volatile Memory

Transparent electronics offer the opportunity to develop electronic and optoelectronic devices for see-through display and electronic circuit applications. ZnO-based TFTs attract much attention due to their advantages such as high mobility, electrical conductivity, and optical transparency. For the purpose of this, amorphous films (such as $InGaZnO_4$) are more suitable than microcrystalline type, because amorphous $InGaZnO_4$ films, with high mobility and no grain boundaries can be deposited at room temperature with better film smoothness and low compressive stress.

We are interested in the fabrication of fully transparent metal nanoparticles embedded non-volatile memory devices on flexible plastic substrates with the entire device structure processed at room temperature. A fully transparent memory device will be developed based on $InGaZnO_4$ semiconductor and metal nanoparticle embedded gate dielectric stack. We will start to optimize the $InGaZnO_4$ film growth condition to obtain high mobility and controllable conductivity onto both rigid (glass) and flexible substrate using RF magnetron sputtering. Our gate dielectric consists of metal nanoparticles embedded inorganic oxides such as Al_2O_3, HfO_2, and SiCON deposited at room temperature. We propose to utilize transparent and room temperature deposited dielectric films, transparent metal source and drain electrodes and active channel layer of amorphous $InGaZnO_4$ to build fully transparent non-volatile memory devices. Further,

our process exhibits tremendous potential for many different thin films processes where low temperature is extremely important as shown in Figure 6.3.

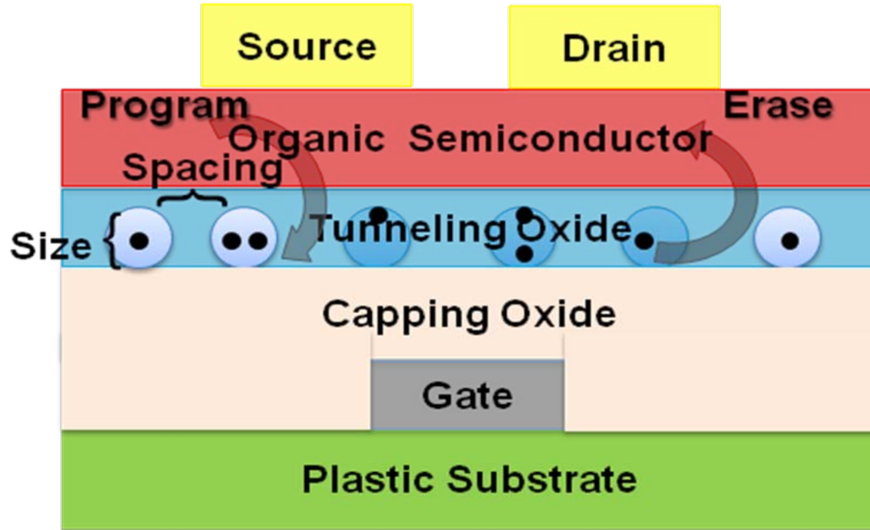


Figure 6.2: Schematic diagram of metal nanoparticle embedded organic semiconductor based non-volatile memory.

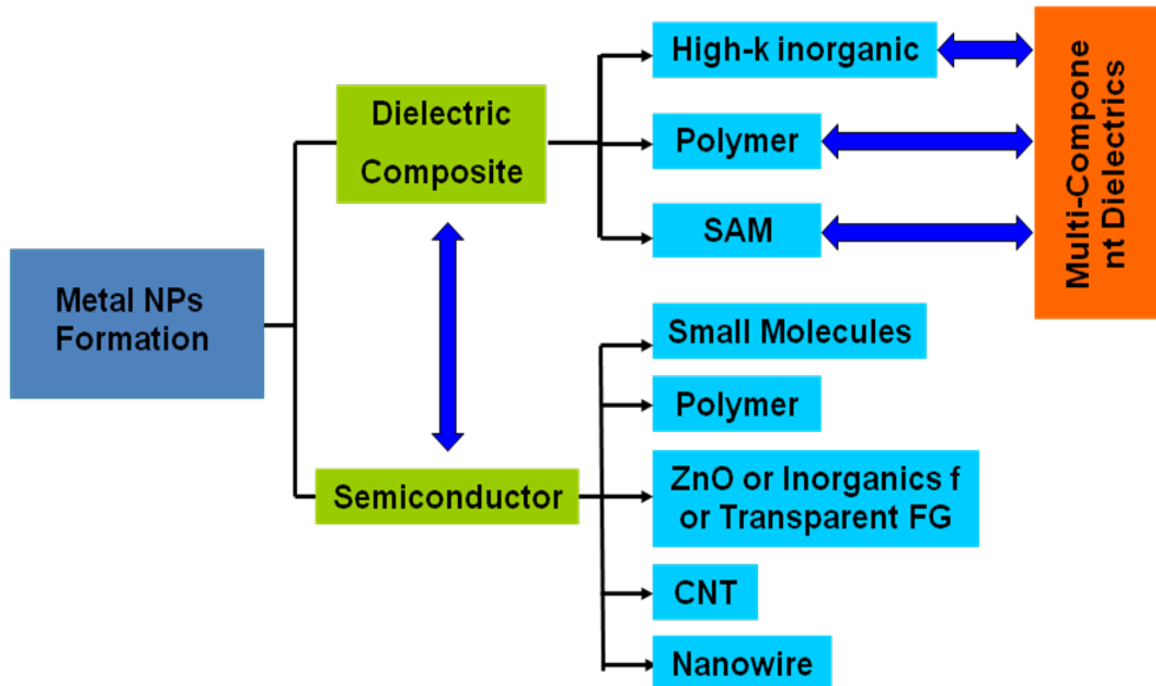


Figure 6.3: Schematic overview and classification of possible application using our room temperature formation metal nanoparticle.

Ch 7. References

[1] W. Brütting, *Physics of Organic Semiconductors*, 1st ed, Weinheim, Germany: WILEY-VCH, 2005.

[2] C. K. Chiang, C. R. Fincher, Y. W. Park, A. J. Heeger, H. Shirakawa, E. J. Louis, S. C. Gau, and A. G. MacDiarmid, "Electrical conductivity in doped polyacetylene," *Physical Review Letters*, vol. 39, no. 17, pp. 1098-1101, Oct. 1977.

[3] S. Forrest, P. Burrows, and M. Thompson, "The dawn of organic electronics," *IEEE Spectrum*, vol. 37, no. 8, pp. 29-34, Aug. 2000.

[4] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, no. 5499, pp. 2123-2126, Dec. 2000.

[5] W. Riess, H. Riel, T. Beierlein, W. Brütting, P. Müller, and P. F. Seidler, "Influence of trapped and interfacial charges in organic multilayer light-emitting devices," *IBM Journal of Research and Development*, vol. 45, no. 1, pp. 77-88, Jan. 2001.

[6] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Advanced Materials*, vol. 14, no. 2, pp. 99-117, Jan. 2002.

[7] O. D. Jurchescu, J. Baas, and T. T. M. Palstra, "Effect of impurities on the mobility of single crystal pentacene," *Applied Physics Letters*, vol. 84, no. 16, pp. 3061-3063, Apr. 2004.

[8] D. Fichou, "Structural order in conjugated oligothiophenes and its implications on opto-electronic devices," *Journal of Materials Chemistry*, vol. 10, no. 3, pp. 571-588, 2000.

[9] Z. Bao and J. Locklin, *Organic Field-Effect Transistors*, 1st ed, Boca Raton, FL: CRC Press, 2007.

[10] N. K. Patel, S. Cinà, and J. H. Burroughes, "High-efficiency organic light-emitting diodes," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 8, no. 2, pp. 346-346, Mar/Apr. 2002.

[11] H. Klauk, *Organic Electronics*, 1st ed, Weinheim, Germany: WILEY-VCH, 2006.

[12] Y. D. Park, J. A. Lim, H. S. Lee, and K. Cho, "Interface engineering in organic transistors," *Materials Today*, vol. 10, no. 3, pp. 46-54, Mar. 2007.

[13] M. E. Gershenson, V. Podzorov, and A. F. Morpurgo, "Colloquium: Electronic transport in single-crystal organic transistors," *Reviews of Modern Physics*, vol. 78, no. 3, pp. 973-989, Jul-Sep. 2006.

[14] R. A. Street and A. Salleo, "Contact effects in polymer transistors," *Applied Physics Letters*, vol. 81, no. 15, pp. 2887-2889, Oct. 2002.

[15] H. Sirringhaus, R. J. Wilson, R. H. Friend, M. Inbasekaran, W. Wu, E. P. Woo, M. Grell, and D. D. C. Bradley, "Mobility enhancement in conjugated polymer field-effect transistors through chain alignment in a liquid-crystalline phase," *Applied Physics Letters*, vol.77, no. 3, pp. 406-408, Jul. 2000.

[16] Z. Bao, A. Dodabalapur, and A. J. Lovinger, "Soluble and processable regioregular poly(3-hexylthiophene) for thin film field-effect transistor applications with high mobility," *Applied Physics Letters*, vol. 69, no. 26, pp. 4108-4110, Dec. 1996.

[17] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, and D. M. de Leeuw, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, vol. 401, no. 6754, pp. 685-688, Oct. 1999.

[18] H. Sirringhaus, N. Tessler, and R. H. Friend, “Integrated optoelectronic devices based on conjugated polymers,” *Science*, vol. 280, no. 5370, pp. 1741-1744, Jun. 1998.

[19] G. M. Wang, J. Swensen, D. Moses, and A. J. Heeger, “Increased mobility from regioregular poly(3-hexylthiophene) field-effect transistors,” *Journal of Applied Physics*, vol. 93, no. 10, pp. 6137-6141, May. 2003.

[20] J.-F. Chang, B. Sun, D. W. Breiby, M. M. Nielsen, T. I. Solling, M. Giles, I. McCulloch, and H. Sirringhaus, “Enhanced mobility of poly(3-hexylthiophene) transistors by spin-coating from high-boiling-point solvents,” *Chemistry of Materials*, vol. 16, no. 23, pp. 4772-4776, Jul. 2004.

[21] T. W. Kelley, D. V. Muyres, F. P. Baude, T. P. Smith, and T. D. Jones, "High performance organic thin film transistors," *Materials Research Society (MRS) Symposium Proceedings* (San Francisco, CA), vol. 771, pp. 169-179, 2003.

[22] W. A. Schoonveld, R. W. Stok, J. W. Weijtmans, J. Vrijmoeth, J. Wildeman, and T. M. Klapwijk, “Morphology of quaterthiophene thin films in organic field effect Transistors,” *Synthetic Metals*, vol. 84, no. 1-3, pp. 583-584, Jan. 1997.

[23] C. D. Dimitrakopoulos, A. R. Brown, and A. Pomp, “Molecular beam deposited thin films of pentacene for organic field effect transistor applications,” *Journal of Applied Physics*, vol. 80, no. 4, pp. 2501-2508, Aug. 1996.

[24] A. Facchetti, M.-H. Yoon, T. J. Marks, “Gate dielectrics for organic field-effect transistors: New opportunities for organic electronics,” *Advanced Materials*, vol. 17, no. 14, pp. 1705-1725, Jul. 2005.

[25] Y. Y. Lin, D. J. Gundlach, T. N. Jackson, and S. F. Nelson, “Pentacene-based organic thin-film transistors,” *IEEE Transactions on Electron Devices*, vol. 44, no. 8, pp. 1325-1331, Aug. 1997.

[26] S. Y. Yang, S. H. Kim, K. Shin, H. Jeon, and C. E. Park, “Low-voltage pentacene field-effect transistors with ultrathin polymer gate dielectrics,” *Applied Physics Letters*, vol. 88, no. 17, pp. 173507, Apr. 2006.

[27] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, and F. Stellacci, "Low-voltage organic transistors with an amorphous molecular gate dielectric," *Nature*, vol. 431, no. 7011, pp. 963-966, Oct. 2004.

[28] S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, and Y. Iwasa, "Fabrication and characterization of C_{60} thin-film transistors with high field-effect mobility," *Applied Physics Letters*, vol. 82, no. 25, pp. 4581-4583, Jun. 2003.

[29] A. Facchetti, M. Mushrush, H. E. Katz, and T. J. Marks, "N-type building blocks for organic electronics: a homologous family of fluorocarbon-substituted thiophene oligomers with high carrier mobility," *Advanced Materials*, vol. 15, no. 1, pp. 33-38, Jan. 2003.

[30] M. Ling, P. Erk, M. Gomez, M. Koenemann, and J. Locklin, "Air-stable *n*-channel organic semiconductors based on perylene diimide derivatives without strong electron withdrawing groups," *Advanced Materials*, vol. 19, no. 8, pp. 1123-1127, Apr. 2007.

[31] H Klauk, U. Zschieschang, J. Pflaum, and M. Halik "Ultralow-power organic complementary circuits," *Nature*, vol. 445, no. 7129, pp. 745-748, Feb. 2007.

[32] J. Zaumseil, R. H. Friend, and H. Sirringhaus, "Spatial control of the recombination zone in an ambipolar light-emitting organic transistor nature materials," *Nature Materials*, vol. 5, no. 1, pp. 69-74, Jan. 2006.

[33] R. G. Southwick and W. B. Knowlton, "Stacked dual-oxide MOS energy band diagram visual representation program," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 2, pp. 136-145, Jun. 2006.

[34] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 3rd ed, New York, NY: John Wiley & Sons, 2003.

[35] B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th ed, Upper Saddle River, NJ: Pearson Prentice Hall, 2006.

[36] Application Note 2896, *C-V Characterization of MOS Capacitors Using the Model 4200-SCS Semiconductor Characterization System*, Cleveland, OH: Keithley Instruments, Inc, 2007.

[37] B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, “Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing,” *Applied Physics Letters*, vol. 76, no. 14, pp. 1926-1928, Apr. 2000.

[38] R. F. Pierret, *Semiconductor Device Fundamentals*, 2nd ed, Addison-Wesley, 1996.

[39] S. M. Sze, *Physics of Semiconductor Devices,* 2nd ed, New York, NY: John Wiley & Sons, 1981.

[40] E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah, “Ion transport phenomena in insulating films,” *Journal of Applied Physics*, vol. 36, no. 5, pp. 1664-1673, May. 1965.

[41] B. E. Deal, “Standardized terminology for oxide charges associated with thermally oxidized silicon,” *Journal of Electrochemical Society*, vol. 127, no. 4, pp. 979-981, Apr. 1980.

[42] F. G. Allen and G. W. Gobeli, “Work function, photoelectric threshold, and surface states of atomically clean silicon,” *Physics Review*, vol. 127, no. 1, pp. 150-158, Jul. 1962.

[43] L. Terman, “An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes,” *Solid State Electronics*, vol. 5, no. 5, pp. 285-299, Sep-Oct. 1962.

[44] K. Lehovec, “Rapid evaluation of C-V plots for MOS structures,” *Solid State Electronics*, vol. 11, no. 1, pp. 135-137, Jan. 1968.

[45] K. Lehovec and A. Slobodoskoy, “Impedance of semiconductor-insulator-metal capacitors,” *Solid State Electronics*, vol. 7, no. 1, pp. 59-779, Jan. 1964.

[46] C. N. Berglund, “Surface states at steam-grown silicon-silicon dioxide interfaces,” *IEEE Transactions on Electron Devices*, vol. 13, no. 10, pp. 701-705, Oct. 1966.

[47] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed, Hoboken, NJ: John Wiley & Sons, 2006.

[48] E. H. Nicollian and A. Goetzberger, *Bell System Technology Journal*, vo. 46, pp. 1055, 1967.

[49] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Hoboken, NJ: John Wiley & Sons, 2003.

[50] N. Biswas, “Electrical properties of fluorinated amorphous carbon (a-C:F_x) and aluminum nitride (AlN) films,” Ph.D. Dissertation, Dept. Phys. & Eng. Phys., Stevens Institute of Technology, Hoboken, NJ, 2000.

[51] D. Kahng and S. M. Sze, “A floating gate and its application to memory devices,” *Bell System Technology Journal*, vol. 46, pp. 1283, 1967.

[52] R. H. Fowler and L. Nordheim, “Electron emission in intense electric fields,” *Proceedings of Royal Society A*, vol. 119, no. 781, pp. 173-181, Mar. 1928.

[53] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-*k* gate dielectrics: Current status and materials properties considerations,” *Journal of Applied Physics*, vol. 89, no. 10, pp. 5243-5275, May. 2001.

[54] B. Govoreanu, P. Blomme, M. Rosmeulen, J. V. Houdt, and K. D. Meyer, “VARIOT: a novel multilayer tunnel barrier concept for low-voltage nonvolatile memory devices,” *IEEE Electron Devices Letters*, vol. 24, no. 2, pp. 99-101, Feb. 2003.

[55] Y.-S. Lo, K.-C. Liu, J.-Y. Wu, C.-H. Hou, and T.-B. Wu, “Bandgap engineering of tunnel oxide with multistacked layers of Al_2O_3/HfO_2/SiO_2 for Au-nanocrystal memory application,” *Applied. Physics Letters*, vol. 93, no. 13, pp. 132907, Oct. 2008.

[56] Manual of WVASE 32®, Lincoln, NE: J. A. Woollam Co. Inc.

[57] A. W. Grice, D. D. C. Bradley, M. T. Bernius, M. Inbasekaran, W. W. Wu, and E. P. Woo, "High brightness and efficiency blue light-emitting polymer diodes," *Applied. Physics Letters*, vol. 73, no. 5, pp. 629-631, Aug. 1998.

[58] M. Ahles, A. Hepp, R. Schmechel, and H. V. Seggern, "Light emission from a polymer transistor," *Applied. Physics Letters*, vol. 84, no. 3, pp. 428-430, Jan. 2004.

[59] M. T. Bernius, M. Inbasekaran, J. O'Brien, and W. Wu, "Progress with light-emitting polymers," *Advanced Materials*, vol. 12, no. 23, pp. 1737-1750, Dec. 2000.

[60] B. Tanto, S. Guha, C. M. Martin, U. Scherf, and M. J. Winokur, "Structural and spectroscopic investigations of bulk poly[bis(2-ethyl)hexylfluorene]," *Macromolecules*, vol. 37, no. 25, pp. 9438-9448, Nov. 2004.

[61] M. Grell and D. D. C. Bradley, "Polarized luminescence from oriented molecular materials," *Advanced Materials*, vol. 11, no. 11, pp. 895-905, Aug. 1999.

[62] D. Neher, "Polufluorene homopolymers: Conjugated liquid-crystalline polymers for bright blue emission and polarized electroluminescence," *Macromolecular Rapid Communication*, vol. 22, no. 17, pp. 1366-1385, Dec. 2001.

[63] Y. Y. Deng and H. Sirringhaus, "Optical absorptions of polyfluorene transistors," *Physical Review B*, vol. 72, no. 4, pp. 045207, Jul. 2005.

[64] J. M. Shaw and P. F. Seidler, "Organic electronics: Introduction," *IBM Journal of Research and Development*, vol. 45, no. 1, pp. 3-9, 2001.

[65] J. Veres, S. Ogier, G. Lloyd, and D. D. Leeuw, "Gate insulators in organic field-effect transistors," *Chemistry of Materials*, vol. 16, no. 23, pp. 4543-4555, Sep. 2004.

[66] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, "General observation of n-type field-effect behavior in organic semiconductors," *Nature*, vol. 434, no. 10, pp. 194-199, Mar. 2005.

[67] D. Buchanan, "Scaling the gate dielectric: Materials, integration, and reliability," *IBM Journal of Research and Development*, vol. 43, no. 3, pp. 245-264, May. 1999.

[68] E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, "High-resolution depth profiling in ultrathin Al_2O_3 films on Si," *Applied Physics Letters*, vol. 76, no. 2, pp. 176-178, Jan. 2000.

[69] D.-G. Park, H.-J. Cho, K.-Y. Lim, C. Lim, I.-S. Yeo, J.-S. Roh, and J. W. Park, "Characteristics of n^+ polycrystalline-Si/Al_2O_3/Si metal-oxide-semiconductor structures prepared by atomic layer chemical vapor deposition using $Al(CH_3)_3$ and H_2O vapor," *Journal of Applied Physics*, vol. 89, no. 11, pp. 6275-6280, Jun. 2001.

[70] G. Wang, D. Moses, A. J. Heeger, H.-M. Zhang, M. Narasimhan, and R. E. Demaray, "Poly(3-hexylthiophene) field-effect transistors with high dielectric constant gate insulator," *Journal of Applied Physics*, vol. 95, no. 1, pp. 319-322, Jan. 2004.

[71] M. Raja, N. Sedghi, S. J. Higgins, and W. Eccleston, "The benefits of high-*k* dielectrics for polymer TFTs," *Materials Research Society (MRS) Symposium Proceedings*, vol. 734, pp. B9.1.1-B9.1.6, 2002.

[72] I. Torres and D. M. Taylor, "Interface states in polymer metal-insulator-semiconductor devices," *Journal of Applied Physics*, vol. 98, no. 7, pp. 073710, Oct. 2005.

[73] S. Grecu, M. Bronner, A. Optiz, and W. Brütting, "Characterization of polymeric metal-insulator-semiconductor diodes," *Synthetic Metals*, vol. 146, no. 3, pp. 359-363, Sep. 2004.

[74] N. Zhao, O. Marinov, G. A. Botton, M. J. Deen, B. S. Ong, Y. Wu, and P. Liu, "Characterization of MOS structures based on poly(3,3'''-dialky-quaterthiophene)," *IEEE Transaction on Electron Devices,* vol. 52, no. 10, pp. 2150-2156, Oct. 2005.

[75] K. Choi, H. Harris, S. Gangopadhyay, and H. Temkin, "Cleaning of Si and properties of the HfO_2-Si interface," *Journal of Vacuum Science Technology A*, vol. 21, no. 3, pp. 718-722, May. 2003.

[76] A. Ishizaka and Y. Shiraki, "Low temperature surface cleaning of silicon and its application to silicon MBE," *Journal of Electrochemical Society*, vol. 133, no. 4, pp. 666-671, Apr. 1986.

[77] J. P. Lehan, Y. Mao, B. G. Howard, and H. A. Macleod, "Optical and microstructural properties of hafnium dioxide thin films," *Thin Solid Films*, vol. 203, no. 2, pp. 227-250, Aug. 1991.

[78] M. Reed and J. Plummer, "Chemistry of Si-SiO_2 interface trap annealing," *Journal of Applied Physics*, vol. 63, no. 12, pp. 5776-5793, Jun. 1988.

[79] U. Scherf and E. J. W. List, "Semiconducting polyfluorene-towards reliable structure-property relationship," *Advanced Materials*, vol. 14, no. 7, pp. 477-487, Apr. 2002.

[80] M. A. Arif, "Raman scattering studies and charge transport in polyfluorenes," Ph.D. Dissertation, Dept. Phys. & Astron., University of Missouri, Columbia, MO, Aug. 2007.

[81] S. Scheinert, G. Paasch, S. Pohlmann, H.-H. Hörhold, and R. Stockmann, "Field effect in organic devices with solution-doped arylamino-poly-(phenylene-vinylene)," *Solid State Electronics*, vol. 44, no. 5, pp. 845-853, May. 2000.

[82] A. Cravino and N. S. Sariciftci, "Molecules as bipolar conductors," *Nature Materials*, vol. 2, no. 6, pp. 360-361, Jun. 2003.

[83] P. J. Brown, H. Sirringhaus, M. Harrison, M. Shkunov, and R. H. Friend, "Optical spectroscopy of field-induced charge in self-organized high mobility poly(3-hexyl thiophene)," *Physical Review B*, vol. 63, no. 12, pp. 125204, Mar. 2001.

[84] E. J. Meijer, A. V. G. Mangnus, C. M. Hart, D. M. D. Leeuw, and T. M. Klapwijk, "Frequency behavior and the Mott-Schottky analysis in poly(3-hexyl thiophene) metal-insulator-semiconductor diodes," *Applied Physics Letters*, vol. 78, no. 24, pp. 3902-3904, Jun. 2001.

[85] M. Arif, M. Yun, S. Gangopadhyay, K. Ghosh, L. Fadiga, F. Galbrecht, U. Scherf, and S. Guha, "Polyfluorene as a model system for space-charge-limited conduction," *Physics Review B*, vol. 75, no. 19, pp. 195202, May. 2007.

[86] M. Knaapila, K. Kisko, B. P. Lyons, R. Stepanyan, J. P. Foreman, O. H. Seeck, U. Vainio, L.-O. Pålsson, R. Serimaa, M. Torkkeli, and A. P. Monkman, "Influence of molecular weight on self-organization, uniaxial alignment, and surface morphology of hairy-rodlike polyfluorene in thin films," *Journal of Physical Chemistry B*, vol. 108, no. 30, pp. 10711-10720, Jul. 2004.

[87] S. Trogisch, M. J. Simpson, H. Taub, U. G. Volkmann, M. Pino, and F. Y. Hansen, "Atomic force microscopy measurements of topography and friction on doctriacontane films adsorbed on a SiO_2 surface," *Journal of Chemistry Physics*, vol. 123, no. 15, pp. 154703, Oct. 2005.

[88] T. Linder, G. Paasch, and S. Scheinert, "Hysteresis in orgnaic field-effect devices: Simulated effects due to trap recharging, " *Journal of Applied Physics*, vol. 98, no. 11, pp. 114505, Dec. 2005.

[89] L. Fumagalli, D. Natali, M. Sampietro, E. Peron, F. Perissinotti, G. Tallarida, and S. Ferrari, "Al_2O_3 as gate dielectric for organic transistors: Charge transport phenomena in poly-(3-hexylthiophene) based devices," *Organic Electronics*, vol. 9, no. 2, pp. 198-208, Apr. 2008.

[90] M. Yun, R. Ravindran, M. Hossain, S. Gangopadhyay, U. Scherf, T. Bünnagel, F. Galbrecht, M. Arif, and S. Guha, "Capacitance-voltage characterization of polyfluorene-based metal-insulator-semiconductor diodes," *Applied Physics Letters,* vol. 89, no. 1, pp. 013506, Jul. 2006.

[91] B. V. Zeghbroeck, *Principles of Semiconductor Devices*, 2007 [Online]. Available. http://ece-www.colorado.edu/~bart/book.

[92] S. Grecu, M. Roggenbuck, A. Opitz, and W. Brütting, "Differences of interface and bulk transport properties in polymer field-effect devices," *Organic Electronics*, vol. 7, no. 5, pp. 276-286, Oct. 2006.

[93] I. Torres, D. M. Taylor, and E. Itoh, "Interface states and depletion-induced threshold voltage instability in organic metal-insulator-semiconductor structures," *Applied Physics Letters*, vol. 85, no. 2, pp. 314-316. Jul. 2004.

[94] M. Kitamuraa and Y. Arakawa, "High-performance pentacene thin-film transistors with high dielectric constant gate insulators," *Applied Physics Letters*, vol. 89, no. 22, pp. 223525, Dec. 2006.

[95] A. Wang, I. Kymissis, V. Bulović, and A. I. Akinwande, "Tunable threshold voltage and flatband voltage in pentacene field effect transistors," *Applied Physics Letters*, vol. 89, no. 11, pp. 112109, Sep. 2006.

[96] X.-H. Zhang, S. P. Tiwari, and B. Kippelen, "Pentacene organic field-effect transistors with polymeric dielectric interfaces: Performance and stability," *Organic Electronics*, vol. 10, no. 6, pp. 1133-1140, Jun. 2009.

[97] K. Shin, S. Y. Yang, C. Yang, H. Jeon, and C. E. Park, "Effects of polar functional groups and roughness topography of polymer gate dielectric layers on pentacene field-effect transistors," *Organic Electronics*, vol. 8, no. 4, pp. 336-342, Aug. 2007.

[98] Y. Jang, D. H. Kim, Y. D. Park, J. H. Cho, M. Hwang, and K. Cho, "Low-voltage and high-field-effect mobility organic transistors with a polymer insulator," *Applied Physics Letters*, vol. 88, no. 7, pp. 072101, Feb. 2006.

[99] S. Y. Yang, K. Shin, and C. E. Park, "The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics" *Advanced Functional Materials*, vol. 15, no. 11, pp. 1806-1814, Nov. 2005.

[100] International Technology Roadmap for Semiconductors, 2007. [Online]. Available. http://public.itrs.net.

[101] H. I. Hanafi, S. Tiwari, and I. Khan, “Fast and long retention-time nano-crystal memory,” *IEEE Transaction on Electron Devices*, vol. 43, no. 9, pp. 15531558, Sep. 1996.

[102] J. D. Blauwe, “Nanocrystal nonvolatile memory devices,” *IEEE Transaction on Nanotechnology*, vol. 1, no. 1, pp. 72-77, Mar. 2002.

[103] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, “A silicon nanocrystals based memory,” *Applied Physics Letters*, vol. 68, no. 10, pp. 1377-1379, Mar. 1996.

[104] D. Zhao, Y. Zhu, R. Li, and J. Liu, “Simulation of a Ge-Si hetero-nanocrystal memory,” *IEEE Transaction on Nanotechnology*, vol. 5, no. 1, pp. 37-41, Jan. 2006.

[105] Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, “Metal nanocrystal memories-Part I: Device design and fabrication,” *IEEE Transaction on Electron Devices*, vol. 49, no. 9, pp. 1606-1613, Sep. 2002.

[106] S. Maikapa, P. J. Tzeng, H. Y. Lee, C. C. Wang, T. C. Tien, L. S. Lee, and M.-J. Tsai, “Physical and electrical characteristics of atomic layer deposited TiN nanocrystal memory capacitors,” *Applied Physics Letters*, vol. 91, no. 4, pp. 043114, Jul. 2007.

[107] J. J. Lee and D.-L. Kwong, “Metal nanocrystal memory with high-κ tunneling barrier for improved data retention,” *IEEE Transaction on Electron Devices*, vol. 52, no. 4, pp. 507-511, Apr. 2005.

[108] H. Tsuji, N. Arai, T. Matsumoto, K. Ueno, Y. Gotoh, K. Adachi, H Kotaki, and J. Ishikawa, “Silver nanoparticle formation in thin oxide layer on silicon by silver-negative-ion implantation for Coulomb blockade at room temperature,” *Applied Surface Science*, vol. 239, no. 1-4, pp. 132-137, Nov. 2004.

[109] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, “Room temperature operation of a quantum-dot flash memory,” *IEEE Electron Device Letters*, vol. 18, no. 6, pp. 278-280, Jun. 1997.

[110] J. Dufourcq, S. Bodnar, G. Gay, D. Lafond, P. Mur, G. Molas, J. P. Nieto, L. Vandroux, L. Jodin, F. Gustavo, and T. Baron, “High density platinum nanocrystals for non-volatile memory applications,” *Applied Physics Letters*, vol. 92, no. 7, pp. 073102, Feb. 2008.

[111] P. K. Singh, G. Bisht, R. Hofmann, K. Singh, N. Krishna, and S. Mahapatra, “Metal nanocrystal memory with Pt single- and dual-layer NC with low-leakage Al_2O_3 blocking dielectric,” *IEEE Electron Device Letters*, vol. 29, no. 12, pp. 1389-1391, Dec. 2008.

[112] C. Sargentis, K. Giannakopoulos, A. Travlos, N. Boukos, and D. Tsamakis, “Simple method for the fabrication of a high dielectric constant metal-oxide-semiconductor capacitor embedded with Pt nanoparticles,” *Applied Physics Letters*, vol. 88, no. 7, pp. 073106, Feb. 2006.

[113] D. W. Mueller, M. Yun, M. Hossain, V. Misra, and S. Gangopadhyay, “Sputter deposition and thermal stability of sub-2 nm size tunable Pt and Au nanoparticles,” submitted for publication.

[114] L. Perniola, B. D. Salvo, G. Ghibaudo, A. F. Para, G. Pananakakis, V. Vidal, T. Baron, and S. A. Lombardo, “Modeling of the programming window distribution in multinanocrystals memories,” *IEEE Transaction on Nanotechnology*, vol. 2, no. 4, pp. 277-284, Dec. 2003.

[115] C. Lee, J. Meteer, V. Narayanan, and E. C. Kan, “Self-assembly of metal nanocrystal on ultra-thin oxide for nonvolatile memory applications,” *Journal of Electronic Materials*, vol. 34, no. 1, pp. 1-11, Jan. 2005.

[116] J. Carrey, J.-L. Maurice, F. Petroff, and A. Vaurès, “Growth of Au clusters on amorphous Al_2O_3: Evidence of cluster mobility above a critical size,” *Physical Review Letters*, vol. 86, no. 20, pp. 4600-4603, May. 2001.

[117] M. Hirasawa, H. Shirakawa, H. Hamamura, Y. Egashira, and H. Komiyama, “Growth mechanism of nanoparticles prepared by radio frequency sputtering,” *Journal of Applied Physics*, vol. 82, no. 3, pp. 1404-1407, Aug. 1997.

[118] J. A. Venables, L. Giordano, and J. H. Harding, "Nucleation and growth on defect sites: Experiment-theory comparison for Pd/MgO(001)," *Journal of Physics: Condensed Matter,* vol. 18, no. 16, pp. S411-S427, Apr. 2006.

[119] D. Beysens, C. M. Knobler, and H. Schaffar., "Scaling in the growth of aggregates on a surface," *Physical Review B*, vol. 41, no. 14, pp. 9814-9818, May. 1990.

[120] S. H. Cho, S. Lee, D. Y. Ku, T. S. Lee, B. Cheong, W. M. Kim, and K. S. Lee, "Growth behavior and optical properties of metal nanoparticle dispersed dielectric thin films formed by alternating sputtering," *Thin Solid Films*, vol. 447-448, pp. 68-73, Jan. 2004.

[121] T. H. Ng, W. K. Chim, and W. K. Choi, "Conductance-voltage measurements on germanium nanocrystal memory structures and effect of gate electric field coupling," *Applied Physics Letters*, vol. 88, no. 11, pp. 113112, Mar. 2006.

[122] S. Huang, S. Banerjee, R. T. Tung, and S. Oda, "Electron trapping, storing, and emission in nanocrystalline Si dots by capacitance-voltage and conductance-voltage measurements," *Journal of Applied Physics*, vol. 93, no. 1, pp. 576-581, Jan. 2003.

[123] O. M. Nayfeha, D. A. Antoniadis, K. Mantey, and M. H. Nayfeh, "Memory effects in metal-oxide-semiconductor capacitors incorporating dispensed highly monodisperse 1 nm silicon nanoparticles," *Applied Physics Letters*, vol. 90, no. 15, pp. 153105, Apr. 2007.

[124] Minseong Yun, David W. Mueller, Maruf Hossain, Veena Misra, and Shubhra Gangopadhyay, "Sub-2 nm size tunable high density Pt nanoparticle embedded non-volatile memory", *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1362-1364, Dec. 2009.

LIST OF PUBLICATIONS

- **M. Yun** and S. Gangopadhyay, "Single electron tunneling and Coulomb blockade effect of 1 nm Pt nanoparticle embedded metal-oxide-semiconductor", in preparation, 2009.

- S. Hamm, M. Hossain, **M. Yun**, S. Gangopadhyay, J. Sulzen, K. Yoon, D. Krueger, A. Wolf, and A. Ladwig, "Nanocomposite thin film for use as high-voltage dielectric", in preparation, 2009.

- D. W. Mueller, **M. Yun**, S. R. Novak, M. Hossain, V. Misra, S. Gangopadhyay, "Sputter deposition and thermal stability of sub-2 nm size tunable Au and Pt nanoparticles," submitted to *IEEE Transaction on Nanotechnology*, 2009.

- **M. Yun**, D. W. Mueller, M. Hossain, V. Misra, and S. Gangopadhyay, "Sub-2 nm size tunable high density Pt nanoparticle embedded non-volatile memory", *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1362-1364, 2009.

- V. Korampally, S. Mukherjee, M. Hossain, R. Manor, **M. Yun**, K. Gangopadhyay, and S. Gangopadhyay, "Development of a miniaturized liquid core waveguide system with nanoporous dielectric cladding–a potential biosensing platform" *IEEE Sensors Journal*, vol. 9, no. 12, pp. 1711-1718, 2009.

- V. Korampally, **M. Yun,** R. Thiruvengadathan, P. K Dasgupta, K. Gangopadhyay, and S. Gangopadhyay, "Entropy driven spontaneous formation of highly porous films from polymer–nanoparticle composites", *Nanotechnology*, vol. 20, no. 42, pp. 425602, 2009.

- M. Hossain, **M. Yun**, V. Korampally, and Shubhra Gangopadhyay, "Low temperature crystallization of amorphous silicon carbide thin films for fabricating p-n junction devices", *Journal of Materials Science: Materials in Electronics*, vol. 19, no. 8-9, pp. 801-804, 2008.

- **M. Yun**, S. Gangopadhyay, M. Bai, H. Taub, M. Arif, and S. Guha, "Interface states in polyfluorene-based metal-insulator-semiconductor diodes", *Organic Electronics*, vol. 8, no. 5, pp. 591-600, 2007.

- M. Arif, **M. Yun,** S. Gangopadhyay, K. Ghosh, L. Fadiga, F. Galbrecht, U. Scherf, and S. Guha, "Polyfluorene as a model system for space-charge-limited conduction", *Physical Review B*, vol. 75, no. 19, pp. 195202, 2007.

- **M. Yun**, R. Ravindran, M. Hossain, S. Gangopadhyay, U. Scherf, T. Bünnagel, F. Galbrecht, M. Arif, and S. Guha, "Capacitance-voltage characterization of polyfluorene-based metal-insulator-semiconductor diodes", *Applied Physic Letters*, vol. 89, no. 1, pp. 013506, 2006.

- R. Ravindran, M. Othman, **M. Yun**, N. Biswas, N. Mehta, S. Guha, K. Gangopadhyays, and S. Gangopadhyay, "Enhanced dielectric constant of HfO_2 and Al_2O_3 thin-films with silver nanoparticles", *210th Electrochemical Society (ECS) Meeting* (Cancun, Mexico) vol. 3, no. 3, pp. 535-544, 2006.

- **M. Yun**, M. Arif, S. Gangopadhyay, and S. Guha, "Electrical characterization of polyfluorene-based metal-insulator-semiconductor diodes", *Materials Research Society (MRS) Symposium Proceedings* (San Francisco, CA) vol. 937E, M07-08, 2006.

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