A STUDY OF A PVT TOLERANT VOLTAGE-CONTROLLED OSCILLATOR FOR AUTOMOTIVE APPLICATIONS

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by

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The undersigned, appointed by the dean of the Graduate School, have examined the thesis entitled

A PVT TOLERANT VOLTAGE-CONTROLLED OSCILLATOR FOR AUTOMOTIVE APPLICATIONS

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ABSTRACT

This thesis focusses on the development of an integrated oscillator for automotive applications. The oscillator operates based on the Barkhausen criterion, which is a mathematical requirement used in electronics to predict whether a linear electronic circuit will oscillate. In this thesis, a voltage-controlled oscillator is designed for increased performance under various process, voltage and temperature (PVT) conditions. By applying a voltage reference block, the output frequency of 0.5MHz, 0.75MHz, 1MHz or 1.25MHz can be obtained. In order to compensate for the variations at PVT corners, the trimming technology is applied to increase the accuracy. The supply voltage is considered to be varying between 2.1V and 5.5V while the temperature range is $-40^{o}C$ $-125^{o}C$.

Chapter 1

INTRODUCTION

In this chapter, the background of the project is introduced in Section 1.1. Then the goal of this research is presented in Section 1.2. Section 1.3 describes an overview of the thesis.

1.1 Motivation

Automotive electronics represent electronic systems used in vehicles to improve safety and performance [3]. Common automotive electronic systems include engine management, in-car camera system, radar, and radio [4][5][6]. These systems use sensors and algorithms to process the data and make decisions. Automotive electronics are constantly evolving to keep up with the latest advances in technology. Modern electric vehicles rely on power electronics as their primary form of propulsion are becoming more and more popular these days. The electronic system components of the electric vehicles has grown in importance as it consititute a significant

percentage of the overall cost of the vehicle. Figure 1.1 illustrates a typical automotive electronics system in an electric vehicle.

Reliable timing solutions are becoming increasingly necessary as the automotive industry continues to incorporate electronic-based features and systems. Oscillator, for example, are currently widely used in automotive applications such as blocking systems, tire-pressure monitoring systems, and control systems. The stability of a frequency is quite important for the electronic components operating based on a clock

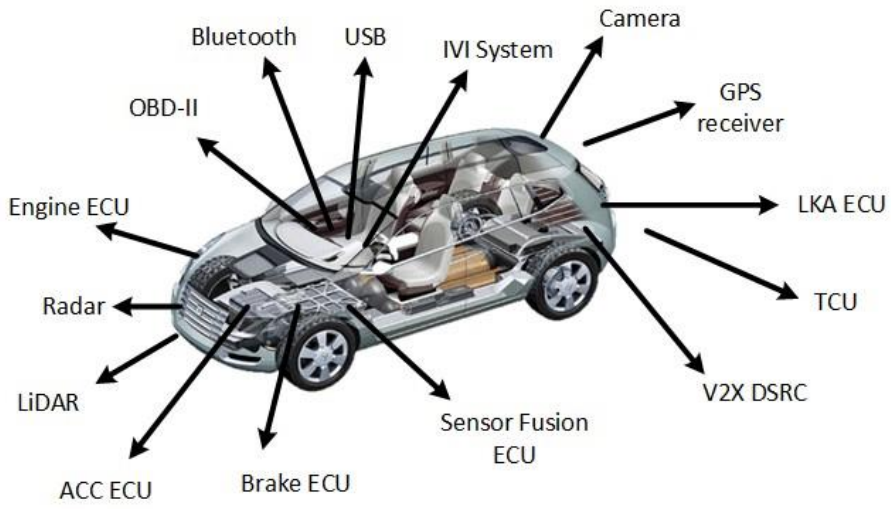

Figure 1.1: Schematic of an automotive showing various electronics blocks [1].

[7]. The environmental parameters that influence the stability of an oscillator include supply voltage, temperature, noise, process tolerances, etc. [8]. But the main factors which make a big difference in output frequency are the variations in process, voltage, and temperature (PVT). However, automotive electronic systems are required to be subjected to more extreme temperature ranges than traditional electronics [9]. This means that they must be designed to withstand extreme temperatures, both hot and

cold. In addition, they must be able to withstand vibration and shocks. To meet the expectations of the automobile industry, automotive electronics must be durable and dependable. Because different operating modes result in different supply voltages. The power supply must be capable of adjusting to the changing demand to maintain a stable voltage. The power supply must also be able to handle the different voltages required by the different components in the system.

Considering those challenges, design of a PVT tolerant integrated oscillator has been proposed in this thesis.

1.2 Research Goal

The purpose of this study is to develop a PVT tolerant and multi-frequency oscillator implemented for automotive applications. A general-purpose low-voltage low-power amplifier is implemented at first in a standard 180nm CMOS technology. The proposed oscillator is then designed with a temperature range of -40°C to 125°C and a supply voltage range of 2.1V to 5.5V, which demonstrates high stability as validated by the simulation results.

1.3 Overview of Thesis

The remaining sections of this thesis are arranged as follows: various oscillator typologies are reviewed in Chapter 2. Chapter 3 presents the design of the subthreshold opamp. Chapter 4 presents the system overview and discuss each part

of the oscillator design. Chapter 5 reports the simulation results of the opamp and the oscillator. Chapter 6 concludes with suggestions for possible future research.

Chapter 2

LITERATURE REVIEW

In this chapter, the Barkhausen criterion is introduced in detail as a fundamental principle to comprehend the working principle of the oscillators. In addition, different types of oscillator design and their working principles are introduced in this chapter.

2.1 Barkhausen Criterion for Oscillation

The Barkhausen stability criterion in electronics is a mathematical test for whether a linear electronic circuit may oscillate [10]. An amplifier with positive feedback should meet the Barkhausen requirements to guarantee sustained oscillations. A basic feedback oscillator is shown in Figure 2.1. The open-loop voltage gain of the amplifier is A and the feedback network is described by the transfer function β. The closed-loop voltage gain is given by the Equation 2.1. Thus, without an input, the output will continue to oscillate whose frequency depends upon the feedback network or the amplifier or both to maintain a voltage as shown below.

$$A_f = \frac{A}{1 - \beta A} \tag{2.1}$$

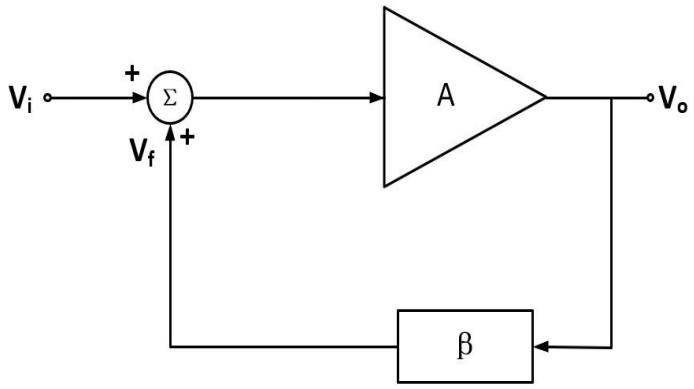

Figure 2.1: The basic structure of a sinusoidal oscillator.

According to the Barkhausen criterion, the loop gain must be unity in absolute magnitude, which is written as:

$$|\beta A| = 1 \tag{2.2}$$

In addition, the phase shift around the loop is zero or an integer multiplier of 2π, which is:

$$\angle \beta A = 2\pi n,\ n = 0,1,2... \tag{2.3}$$

Some circuits satisfy Barkhausen's criterion but do not oscillate, making it a required but not sufficient condition for oscillation [10]. Similarly, the Nyquist stability criteria flags instability but makes no mention of oscillation. A concise definition of an oscillation criterion that is both necessary and sufficient does not appear to exist.

2.2 Literature Review of Oscillators

2.2.1 RC Phase Shift Oscillator

An RC phase-shift oscillator is a type of electronic oscillator that provides the phase shift required by the feedback signal using a resistor capacitor (RC) network. Phase shift is an important factor in the oscillation of an electronic circuit, and the RC phase-shift oscillator is a popular choice for a wide range of applications. They can produce clean sine wave for a variety of loads and have good frequency stability, making them ideal for a variety of applications [7]. In particular, they are well-suited for use in renewable energy systems, where they can help to ensure a steady and reliable flow of power. Figure 2.2 shows an example of an RC phase-shift oscillator.

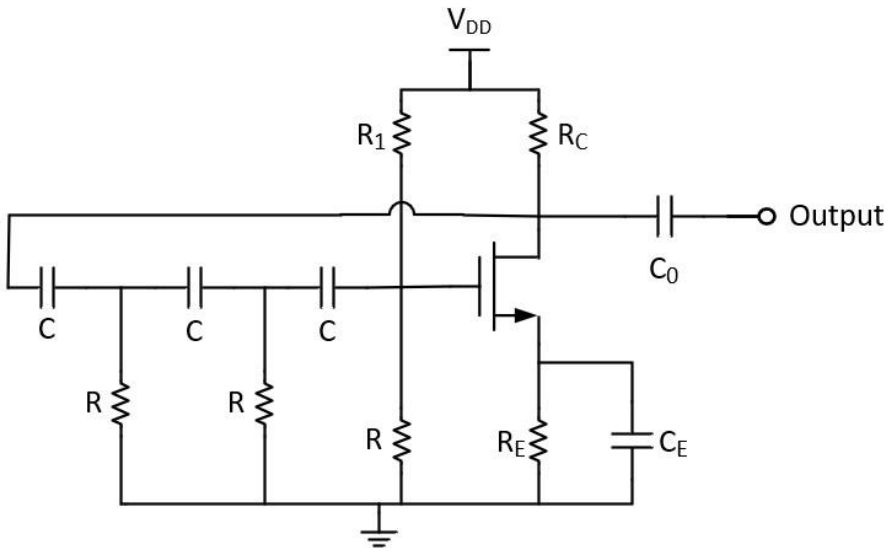

Figure 2.2: Circuit schematic of a RC phase-shift oscillator.

The frequency of oscillations generated by an RC phase-shift oscillator is expressed in general terms in Equation 2.1, where N is the sum of the RC stages created by the capacitors C and the resistors R.

$$f = \frac{1}{2\pi RC\sqrt{2N}} \tag{2.4}$$

Researchers have suggested using a single-tone pump with a frequency that is equal to the product of the frequencies of two acoustic modes within the same resonator to solve the issue of higher motional impedances and improve interface with electronic equipment. [11]. By using this strategy, it may be possible to decrease the size and weight of the entire system while increasing the efficiency of energy transfer. In [12], a fresh detection technique based on Fourier analysis of the phase shift noise of the SAW oscillator has been presented. This is a significant contribution to the field of AI, as it provides a more accurate way to detect and diagnose diseases. This new protocol is more sensitive than previous methods and can be used to detect a wide range of chemicals. This is a significant contribution to the field of chemical detection and has important implications for both industrial and environmental applications. In [13], a modified active RC differential circuit is employed for frequency selection. This circuit is capable of providing a broad spectrum of frequencies, making it ideal for applications that require a variety of frequencies. The circuit is also able to provide a high degree of accuracy and stability.

2.2.2 LC Oscillator

An electrical circuit known as an LC oscillator transforms a DC input (the supply voltage) into an AC output. The amount of inductance and the capacitance in the circuit determines the frequency of the output waveform. The shape and the frequency of the waveform can be controlled by changing the parameters of the system. This flexibility makes it possible to use the same system for a variety of different applications. In the case of LC oscillator, the oscillation frequency of output signal can be expressed as:

$$f = \frac{1}{2\pi RC} \tag{2.5}$$

The oscillators reported in [14] are designed to be highly stable, with a frequency drift of less than 1 ppm/°C. The oscillators are also designed to be low power, with less than 1 mW of power usage. The design replaces an equivalent crystal oscillator by producing an output of 16 MHz using a frequency divider. A varactor is used to adjust the capacitance of the circuit, which in turn compensates for the frequency drift. This ensures that the circuit operates at the correct frequency, regardless of the temperature changes. An open-loop LC oscillator serves as the foundation for the structure suggested in [15]. This design, which incorporates an on-chip temperature sensor, assures constant bias condition, temperature-insensitive operation, and digital control logics made up of an adaptive frequency calibration circuit and a non-volatile memory (NVM). This design is very adaptable and dependable since it allows for temperature compensation and frequency setup of the LC oscillator.

2.2.3 Relaxation Oscillators

The relaxation oscillator is so named because it employs a time constant, $\tau = RC$ which governs the rate of relaxation of charge in the RC network. The time constant determines the frequency of the oscillations generated by the relaxation oscillator. Because of the low power dissipation and CMOS compatibility, relaxation-oscillators are frequently employed in battery-powered applications such as wake-up timers or implanted biomedical systems [16] [17] [18]. However, this delay is subject to strong variations due to PVT. This error can be significant in applications where precise timing is required, such as in high-speed digital circuits. There are several ways to reduce this error, including using a more stable comparator delay. This approach is usually not possible because it cannot be reconciled with the requirement of a low-power oscillator. Another way to solve the problem is mentioned in [19]. The proposed oscillator based on a novel voltage averaging feedback has the advantage that oscillation depends only on the RC-product. That means its frequency is independent of the comparator delay. Therefore, it is possible for the proposed oscillator to meet the requirement of low power consumption.

2.2.4 Crystal Oscillator

Crystal oscillators are electronic devices that use piezoelectric effect to generate an alternating current. The capacity of certain materials to produce an electric field in response to an applied mechanical stress is known as the piezoelectric effect. The crystal vibrates at its natural frequency when an alternating voltage is placed across

its surfaces. This vibration is then used to generate an alternating current and eventually get converted into oscillations. Figure 2.3(a) depicts how a crystal is positioned between two metallic plates in a crystal oscillator, while Figure 2.3 depicts the electrical equivalent (b). In reality, the components of the crystal, a resistor (R_S) with a small value of resistance, a inductor (L_S) with large inductance, and a low-valued capacitor (C_S), which will be connected in parallel with the electrodes capacitance (C_p), behave like a series RLC circuit.

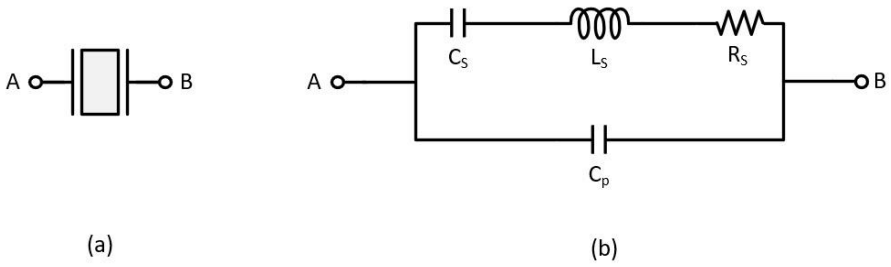

Figure 2.3: A quartz crystal and its equivalent circuit.

For Internet of Things (IoT) applications, [20] presents a temperature-compensated crystal oscillator (TCXO) of extremely low power with a pulsed-injection XO driver. By utilizing a delta-sigma modulator to switch the load capacitance between the two values, temperature compensation can be accomplished with an efficient use of space and power. The typical three-point Colpitts architecture-based crystal oscillator is presented to achieve lower power dissipation and greater frequency accuracy performance [21].

Chapter 3

SUBTHRESHOLD DESIGN

In this Chapter, Section 3.1 demonstrates the subthreshold design technique based on inversion coefficient. The proposed opamp design is presented in Section 3.2.

3.1 Subthreshold Technique

3.1.1 Operation Regions of a MOSFET

There are three operating ranges that a MOSFET can be operated: weak inversion, moderate inversion and strong inversion, which are defined by the gate-source voltage (V_{GS}) [22][23]. The relationship between the region and V_{GS} can be find in Figure 3.1. If V_{GS} - V_{TH} > 150mV, the MOSFET is biased in the strong inversion while MOSFET is operating in the weak inversion if V_{GS} - V_{TH} < -50mV. When the value of V_{GS} is around the value of V_{TH}, the MOSFET is considered to be operating in the moderate inversion.

For the strong and the weak inversions, the equations to calculate the drain current and the transconductance can be found in Table 3.1[22]. Traditionally no design equations are available for moderate inversion.

The level of channel inversion is numerically described by the inversion coefficient (IC), which normalized measures of MOSFET drain current [24].

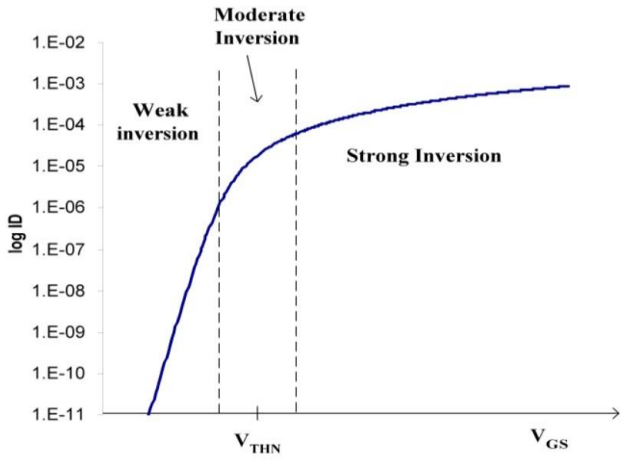

Figure 3.1: Operating regions of a MOSFET [2].

Table 3.1: Drain Current in Weak and Strong Inversion Regions

	I_D	g_m
Weak Inversion	$I_D = 2n\mu C_{ox}\frac{W}{L}U_T^2 exp(\frac{V_{GS}-V_{TO}}{nU_T})$	$g_m = \frac{I_D}{nU_T}$
Strong Inversion	$\mathrm{I}_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TO})^2$	$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$

Mathematically inversion coefficient is defined as:

$$IC = \frac{I_D}{I_0(\frac{W}{L})} = \frac{I_D}{2\mu C_{ox}(\frac{W}{L})U_T^2} \tag{3.1}$$

where I_0 is referred to the technology current. The inversion coefficient can be used to determine the operating region of the MOSFET. For IC < 0.1, the transistors are operating in the weak inversion; for 0.1 < IC < 10, the moderate inversion occurs; for IC > 10, the transistors are bias in the strong inversion. Figure 3.2 shows the relationship of inversion coefficient and transconductance efficiency.

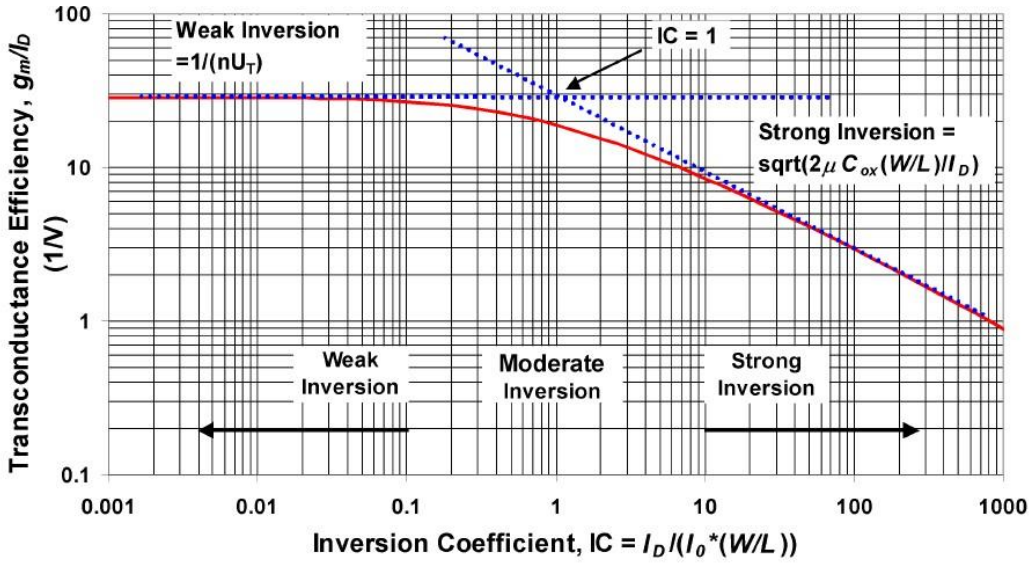

Figure 3.2: Transconductance efficiency in different regions of operation [2].

3.1.2 Subthreshold Technique

Subthreshold technique is one of the methods for low-power design to realize low power consumption. When transistors are biased in the weak inversion, a gate-source

voltage difference potential that is less than the threshold voltage is applied. Working in the weak inversion, the transistors will provide higher transconductance, low effective gate-source voltage and a larger gain, which only consumes a small amount of current.

3.2 Proposed Structure

The primary elements that must be considered when designing the amplifier are stability and low power dissipation. To realize high g_m/I_d efficiency and low power consumption, the input transistors are designed to be operated in the subthreshold region [25]. A folded-cascode amplifier is selected as the first step in the design of a low power opamp. which is shown in Figure 3.3. The input and the output currents through this structure are distinct from one another. By raising the transconductance of the input , the gain can be increased without impacting R_{out} and C_{out}. The gain can be calculated by:

$$A_v = g_m R_{out} = \frac{I_{D1}}{U_T} \frac{1}{\lambda I_{D6}} = \frac{1}{\lambda U_T} \frac{I_{D1}}{I_{D6}} \tag{3.2}$$

The proposed opamp is shown in Figure 3.4. It is made up with several parts: biasing circuit, first-stage amplifier, second-stage amplifier, Miller compensation circuitry and load.

A folded-cascode structure serves as the first-stage amplifier, which is composed of the transistors M_1 – M_8. M_1 and M_2 are combined to form a PMOS differential input pair while M_3 and M_4 make up a current-mirror structure. M_9 and M_{10} make up the

output stage amplifier circuit, where M_9 is the common source amplifier and M_{10} simultaneously supplies continuous bias current for it and the second stage output load. M_{11} and C_C make up the phase compensation while M_{11} is operating in the linear

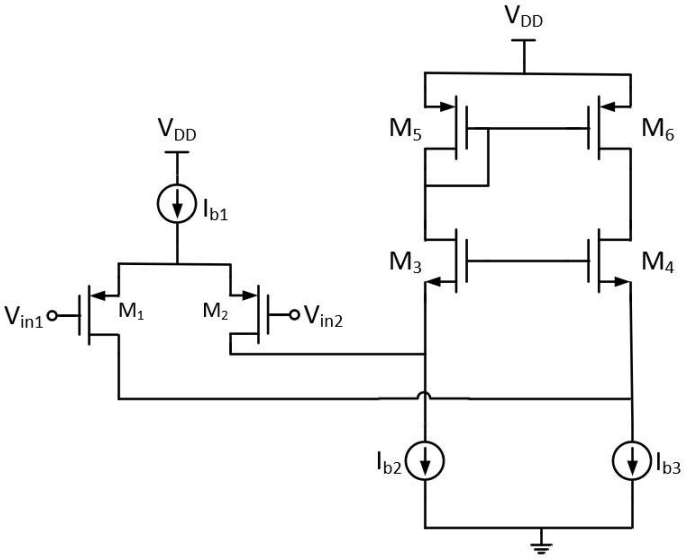

Figure 3.3: Circuit schematic of folded-cascode amplifier structure.

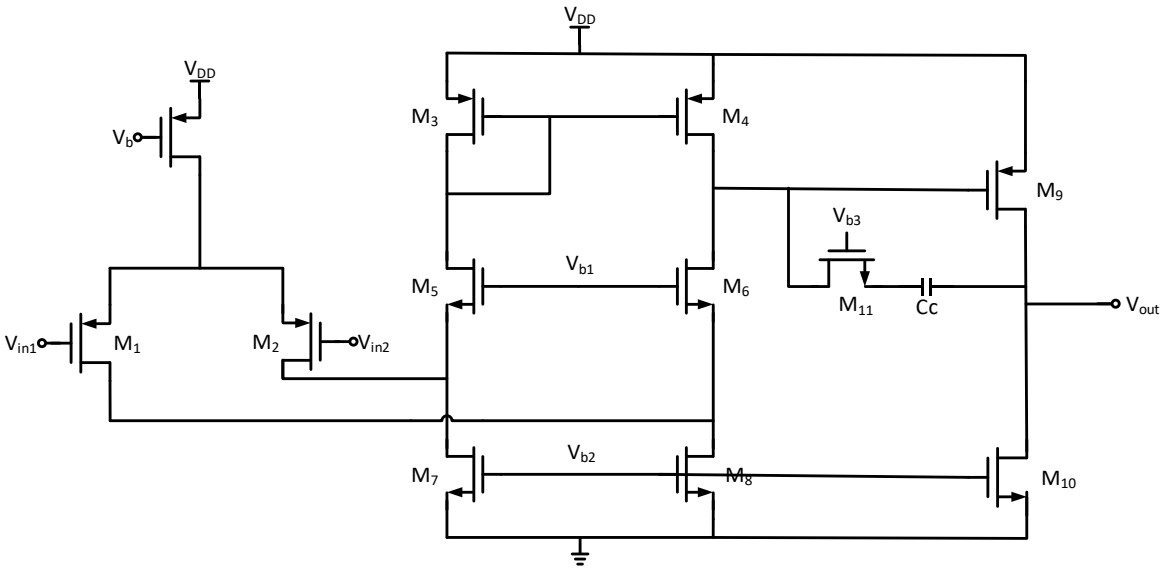

Figure 3.4: Circuit schematic of the proposed opamp.

region. The effect of M_{11} is a resistor, which is placed between the input of the second stage and the output together with the capacitor C_C to form RC Miller compensation network. The complete system operates with low power consumption due to the biasing of the transistors in the subthreshold region.

Chapter 4

OSCILLATOR DESIGN

In this chapter, the design of oscillator is introduced in detail. Section 4.1 includes the overview and the specifications of the design while the proposed circuit structure is introduced in Section 4.2. Each block is discussed and analyzed in Sections 4.3 -4.6.

4.1 Design Overview and Specifications

4.1.1 Overview

The aim of this project is to utilize the oscillator in a wide range of temperature with alternative supply voltage and minimize the power consumption. Figure 4.1 shows the block diagram of the system, which includes the biasing circuitry, the comparator block, the reference voltage generation block and the capacitance trimming block. These blocks are depicted in detail in the following sections 4-3 - 4-6.

4.1.2 Specifications

The supply voltage of the proposed design ranges from 2.1V to 5.5V while the temperature range is from -40^{o}C to 125^{o}C. Within this range, the oscillator can output four different frequencies: 0.5MHz, 0.75MHz, 1MHz and 1.25MHz.

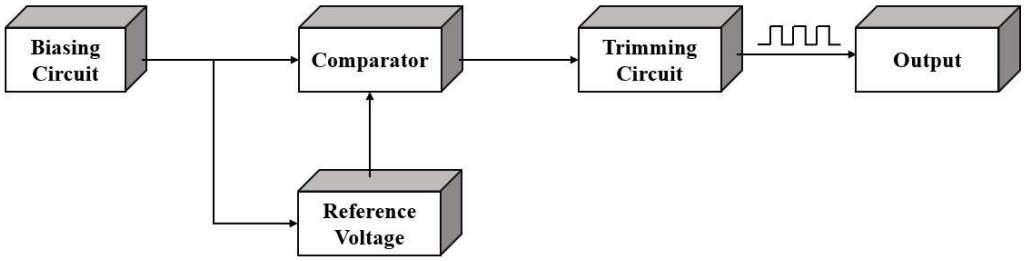

Figure 4.1: Overview of the proposed oscillator.

In addition, two digital bits are used to select frequency in need and 3 bits are used for the trimming purpose.

4.2 Proposed Structure of Oscillator

The proposed structure is shown in Figure 4.2. After the enable signal arrives, the switch SW_0 is closed, and the circuit begins its operation. The biasing circuit supply the biasing current for all the subsequent blocks so that each block functions correctly. There is a feedback loop between the charging circuitry and the comparator output.

The capacitance is switching between charging and discharging to generate a frequency. The current through the capacitor can be calculated by Equation 4.1. The voltage reference block generates two reference voltages, and the capacitor is charged and discharged back and forth from the two reference voltage values. ΔV represents the difference between the two reference voltages.

$$i = C\frac{\Delta V}{\Delta t} \tag{4.1}$$

The frequency of the oscillator can be calculated by

$$f_{osc} = \frac{i}{2C\Delta V} \tag{4.2}$$

According to the equation above, either one of the three variables can be changed to realize the function of multiple frequency. Combining the trimming method of the capacitance trimming, which is an easier way than trimming current, the capacitance trimming block is proposed to achieve the multiple frequency outputs.

4.3 Current Biasing Circuit

The biasing circuit is important because it is related to frequency stability according to the matching of currents flowing through the entire oscillator. A bad matching of the currents leads to alterations in frequency and duty-cycle since those parameters are directly related to the value of the current. In order to minimize the mismatch and

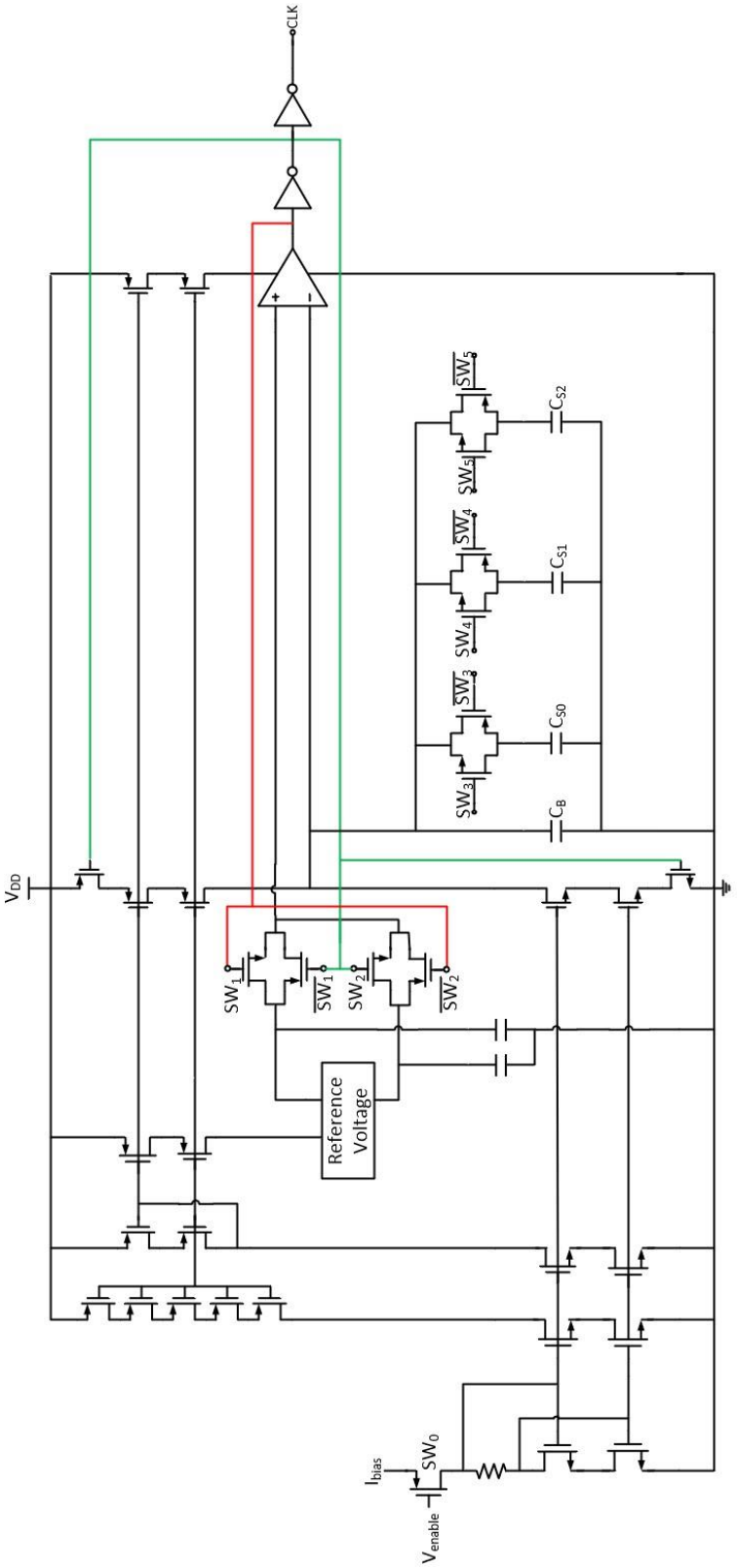

Figure 4.2: Circuit schematic of the proposed voltage-controller oscillator.

process variation, the transistors in use need to be carefully selected in terms of their types and sizes. The cascode current mirror structure is proposed in this design, which is shown in Figure 4.3.

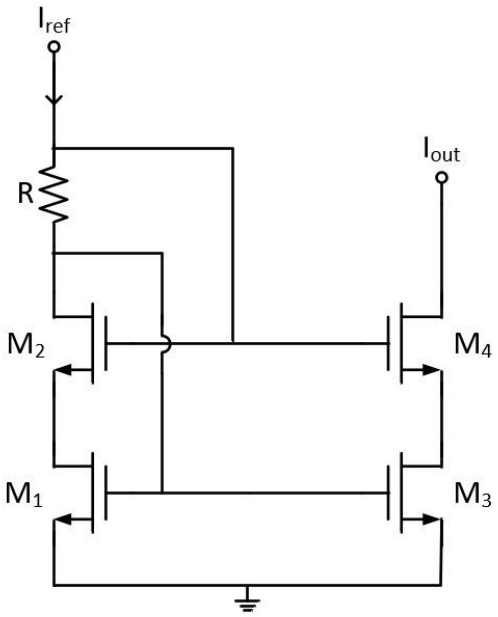

Figure 4.3: Circuit schematic of cascode current mirror.

This topology shows the advantage that by adjusting the value of the resistance, the transistor M1 can be ensured to be biased in saturation, which guarantees that the current mirror is operational and outputs a stable current. The relationship among the resistor and the transistors is obtained from the following equation:

$$V_R = V_{dsat,1} + V_{th,2} - V_{th,1} \tag{4.3}$$

where V_R is the difference voltage across the resistor R, $V_{dsat,1}$ is the offset voltage of the transistor M_1 which also can be expressed as V_{ov}, while $V_{th,1}$ and $V_{th,2}$ are the threshold voltages of the transistors M_1 and M_2 respectively.

In the proposed cascode current mirror structure, the transistor M_1 is the main component that alternates the matching situation. The accuracy of the transistors is determined by $g_m r_o$, where g_m is the transconductance of the transistor and r_o is the equivalent resistance of the transistor. The relationship between the offset voltage and the transconductance can be found in the Equation 4.4. If V_{ov} is too large, a smaller g_m should be applied to decrease the mismatch.

$$g_m = \frac{2I}{V_{ov}} \tag{4.4}$$

4.4 Comparator

A two-stage CMOS comparator is implemented to compare the voltage across the charging capacitance. Figure 4.4 shows the topology of the proposed comparator. The current biasing circuit produces the bias current. Since the comparator is required to be in saturation in any conditions, the bulk terminal of the input transistors are connected to the source to cancel the body effect and obtain a smaller threshold voltage V_{th} so that the gate-source voltage is sufficiently large.

Different from the normal case, the bulk terminals of M1 and M2 are connected to their source to reduce the transistors threshold voltage. In this way, the transistors can be guaranteed to operate in the saturation region.

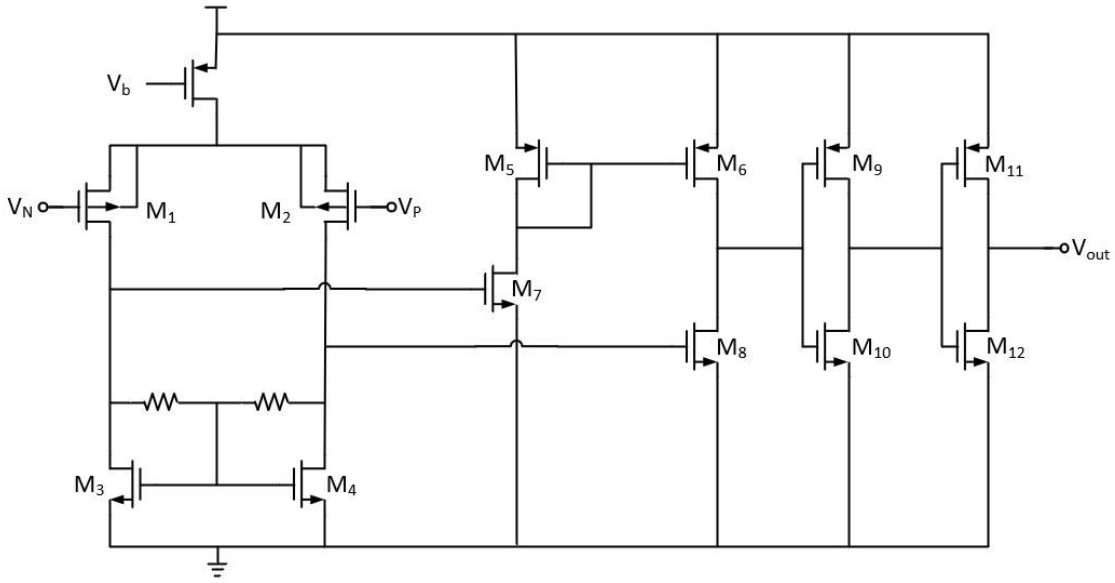

Figure 4.4: Circuit schematic of the proposed comparator.

4.5 Voltage Reference Circuit

The function of the voltage reference circuit is to produce the reference voltage for the input of the comparator. The proposed structure is designed based on a negative feedback amplifier. The simplified structure is shown in Figure 4.5. A fixed amount of voltage obtained from the band-gap circuit is applied to the positive pole of the amplifier, which is 0.4V in this circuit. The negative pole is connected to the secondary stage to form a feedback loop. Since the value of V_{FB} is the same as 0.4V according to the characteristics of the amplifier, the two reference voltages can be obtained by the resistive voltage divider structure. The reference voltages can be calculated by:

$$V_{ref,L} = V_{FB}\frac{R_3}{R_2 + R_3} \tag{4.5}$$

$$V_{ref,H} = V_{FB}\frac{R_1 + R_2 + R_3}{R_2 + R_3} \tag{4.6}$$

where $V_{ref,L}$ is the reference voltage with the smaller value while $V_{ref,H}$ is the reference voltage with larger value.

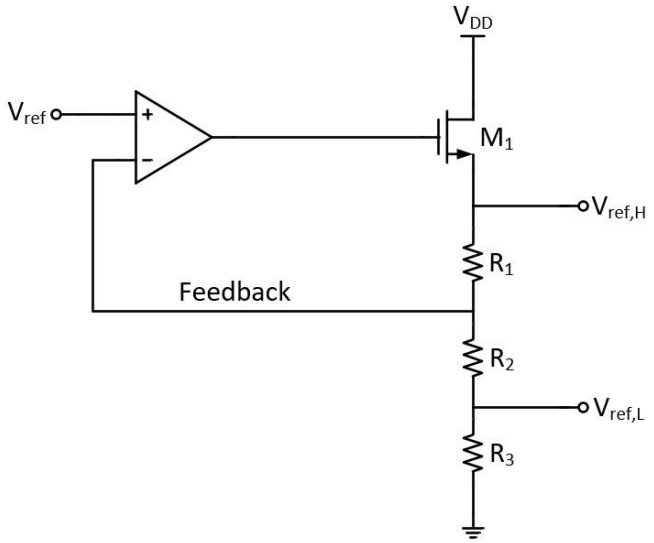

Figure 4.5: An overview schematic of the voltage reference circuit.

Figure 4.6 depicts the suggested voltage reference circuit architecture. In this design, the first stage is the structure of a folded-cascode amplifier while the second stage is a source follower with resistive voltage divider. The advantage of using this structure to obtain the reference voltage is that the mismatch of the resistance can be ignored. As calculated in Equations 4.5 and 4.6, the only parameters to determine the reference voltage are V_{FB} and the ratio of the resistance. In the same technology using the same type of the resistors, the mismatch is totally cancelled.

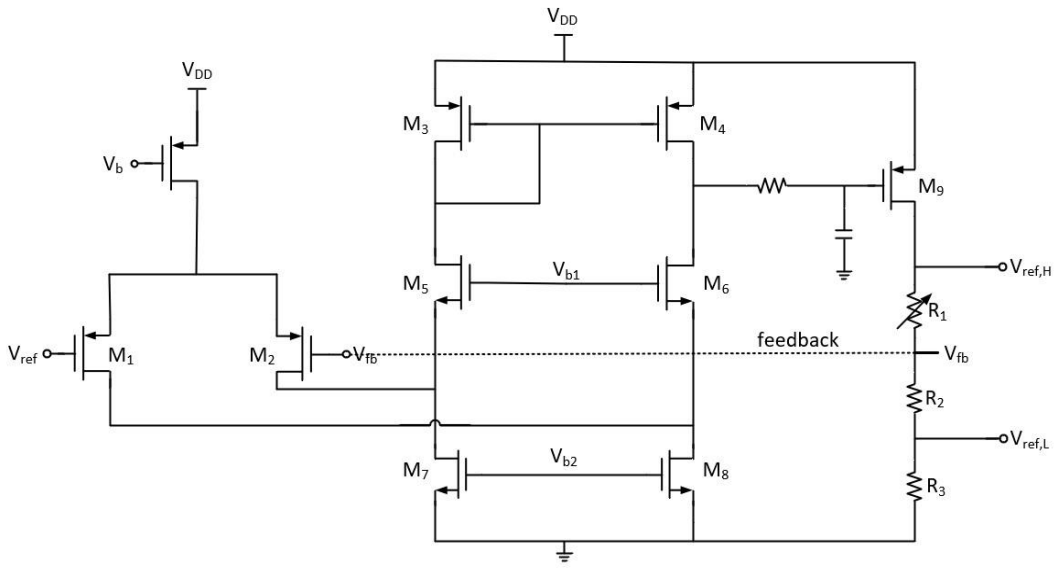

Figure 4.6: Circuit schematic of proposed voltage reference circuit.

To realize the function that the difference between the high reference voltage and low reference voltage is changeable, $V_{ref,L}$ is supposed to be a fixed value and $V_{ref,H}$ varies accordingly. The resistance of R1 is designed as a resistor block which requires a two-bit control while R2 and R3 keep unchanged.

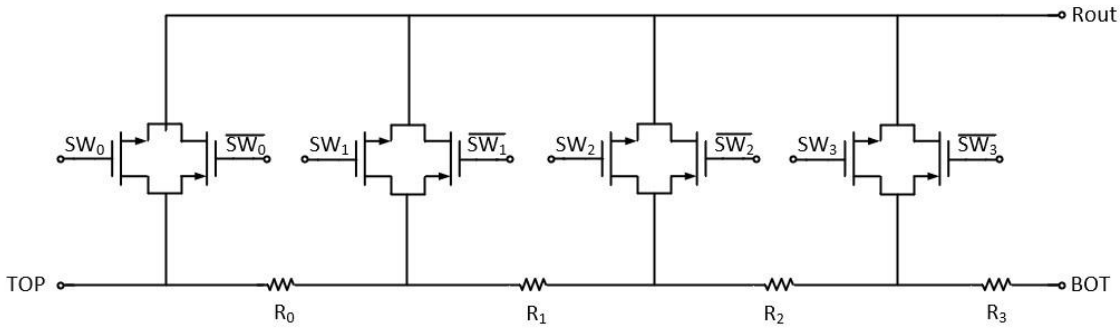

Figure 4.7: Circuit schematic of resistance block.

The resistor block is shown in Figure 4.7. By using the logic gate, four switches are controlled as the same time and output four different resistances. The transmission gate is used as a switch in this circuit to ensure that it will be turned on while the temperature and the supply voltage change. By using the logic gates, the realization of 2-bit control is summarized in Table 4.1.

Table 4.1: 2-bit Control of Output Resistance

2-Bit	SW_0	SW_1	SW_2	SW_3	R_{out}
00	1	0	0	0	$R_0 + R_1 + R_2 + R_3$
01	0	1	0	0	$R_1 + R_2 + R_3$
10	0	0	1	0	$R_2 + R_3$
11	0	0	0	1	R_3

4.6 Trimming Circuit

The performance of the system usually affected by three parameters in circuit design: process, voltage, and temperature, which is also known as 'PVT'. Trimming process is important to achieve a wide tolerant range of the PVT due to its ability to adjust the parameters by a small amount. Analog sensor and circuit variations brought on by manufacturing variations can be offset by trimming operations. Therefore, a

trimming circuit is combined in the voltage-controlled oscillator system to meet the requirement. In the proposed design, the charging capacitor C or the current through the capacitor, I can be possibly trimmed. However, not all of the possibilities are ideal for the system. To minimum the size of the circuit, the approach to trim the charging capacitor is adopted.

4.6.1 Calculation and Sizing

As shown in Figure 4.8, the proposed structure is a 3-bit trimming circuitry. Equations 4.5 and 4.6 can be used to calculate the value of each capacitance. C_B is the base capacitor while C_{S0}, C_{S1} and C_{S2} are the the trimming capacitance whose values are 4 times, 2 times and 1 time of the step size, respectively. C_{target} is the target value of the capacitance which is calculated by Equation 4.2.

$$C_B + C_{S0} = C_{target} \tag{4.7}$$

$$\frac{C_{S2}}{C_{target}} = step\ size \tag{4.8}$$

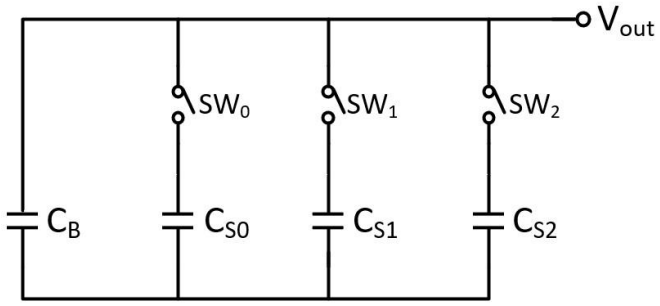

Figure 4.8: Circuit schematic of proposed trimming block.

4.6.2 Trim Range

The step size and the step range are decided by the Monte Carlo running results without trimming. To eliminate the error caused by the process variation and the mismatch of the transistors, the $\pm 4\sigma$ range of variation must be fully covered. According to the pre-trimmed simulation results, the step size is chosen to be 6%. This means that the maximum variation in the time period with respect to the target frequency is -18% to +24%.

Chapter 5

SIMULATION RESULTS

In this chapter, the simulation results for the proposed opamp and oscillator shown in Figures 3.4 and 4.2 are summarized.

5.1 Subthreshold Opamp

Table 5.1: Transistor Sizing and Bias Current for Folded-Cascode Opamp

	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}
$W(\mu m)$	4	4	2	2	6	6	8	8	30	8
$L(\mu m)$	2	2	1	1	1	1	1	1	1	1
$I_{bias}(nA)$	50	50	50	50	50	50	50	50	100	100

This section presents the suggested opamp simulation results using a 180nm CMOS process simulator. Table 5.1 provides a summary of the transistor size for this opamp. The supply Voltage is 0.7V.

5.1.1 Gain and Phase Margin

When designing a circuit, one of the most important things to keep in mind is that the circuit should be stable so that the system is always in the working mode and will not generate unexpected signal. The stability of an amplifier is usually measured by its gain and phase margins. However, the phase margin is reduced as a result of the increased open loop gain. While pursuing a higher gain, the phase margin at 0 dB should be ensured to be larger than 60^o so that the system is stable. As shown in the Figure 5.1, the open loop gain of the proposed opamp is 74 dB and the phase margin is 72^o.

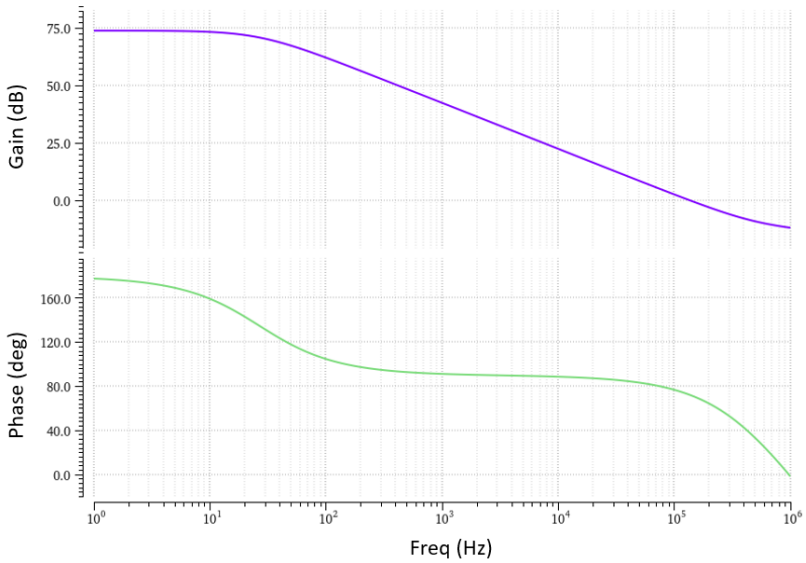

Figure 5.1: Bode plot of the proposed opamp.

5.1.2 Slew Rate (SR)

The maximum rate of change of the output voltage of an opamp is known as the slew rate. It is typically expressed in units of volts per microsecond. The opamp can react to changes in the input voltage more quickly for higher the slew rate. When selecting an opamp for a certain application, slew rate is a crucial consideration. Slew rate can be defined as:

$$SR = \frac{\Delta V}{\Delta t} \tag{5.1}$$

Since the operational amplifier controls the slew rate, the feedback used in the electronic circuit design has little bearing on how well the slew rate performs overall. In this design, the slew rate is 50.1V/ms.

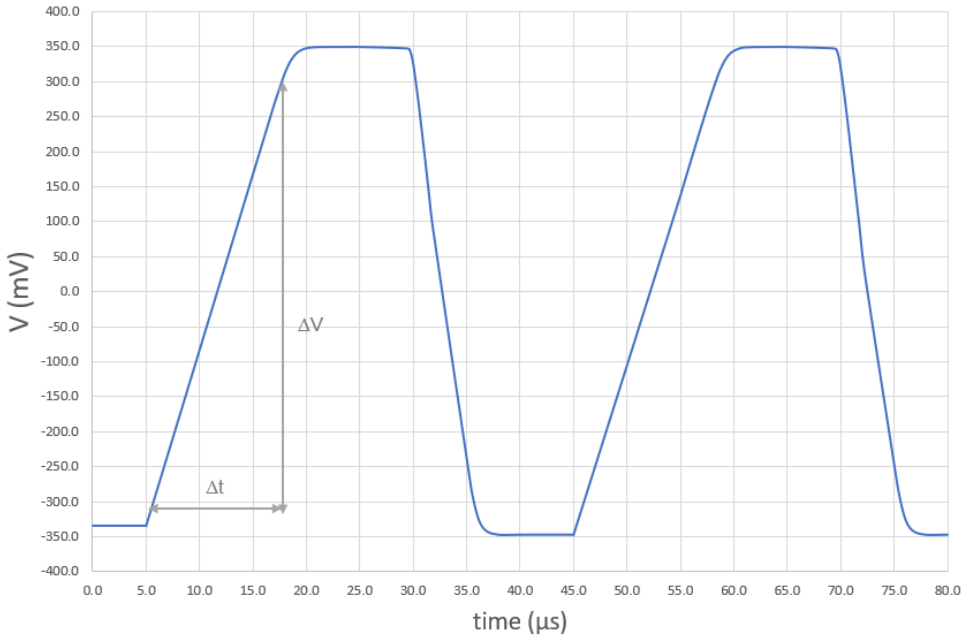

Figure 5.2: Output waveform of the proposed opamp.

5.1.3 Common Mode Rejection Ratio (CMRR)

CMRR is defined to be the differential-mode gain divided by the common-mode gain, which can be written as:

$$CMRR = |\frac{A_{dm}}{A_{cm}}| \tag{5.2}$$

The capacity of an amplifier to reject common-mode signals is measured by the common-mode rejection ratio (CMRR). In other words, it is a measure of how well the amplifier can amplify the difference between two signals while ignoring any common component between them. The higher the CMRR, the better the amplifier will be at rejecting common-mode signals. From Figure 5.3, the CMRR value for the proposed opamp is 90dB.

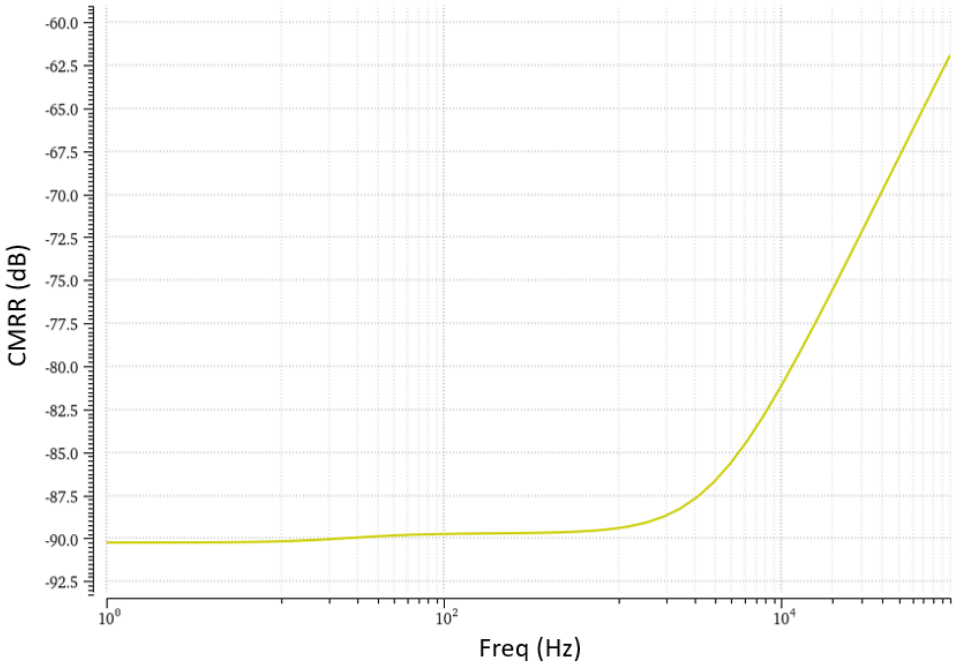

Figure 5.3: CMRR of the proposed opamp.

5.1.4 Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio (PSRR) is a widely used term to describe the ability of an electronic circuit to suppress any power supply variations to its output signal. The PSRR can be calculated as:

$$PSRR^{+} = \frac{A_{dm}}{A^{+}}, \quad PSRR^{-} = \frac{A_{dm}}{A^{-}} \tag{5.3}$$

The positive power supply rejection ratio $PSRR^{+}$ is the differential mode gain divided by the positive power supply gain, and the negative power supply rejection ratio $PSRR^{-}$ is the differential mode gain divided by the negative supply gain. The power supply rejection ratio should be as high as possible to minimize the influence of the power supply at the output. In practice, power supply rejection ratio decreases as the frequency increases.

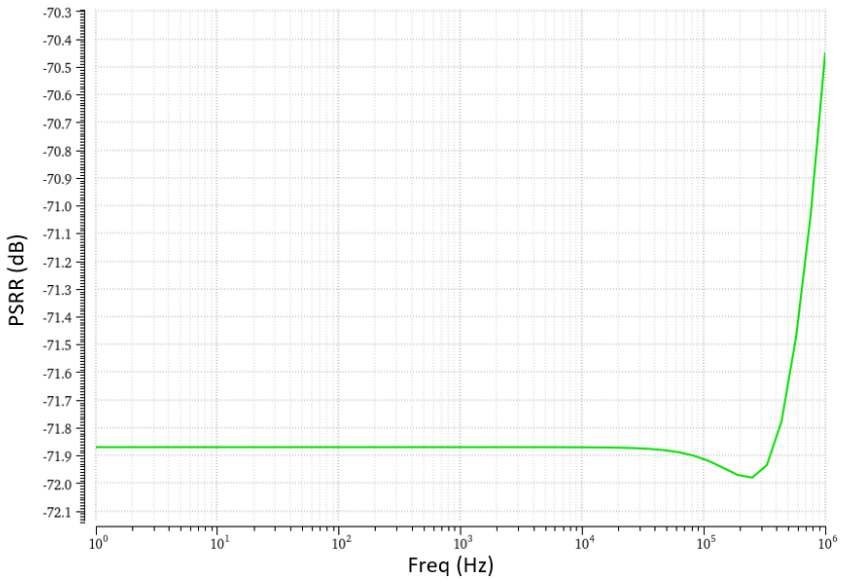

Figure 5.4: PSRR of the proposed opamp.

Figure 5.4 shows the PSRR simulation results for the proposed opamp, which is 71.87dB.

5.2 Proposed Oscillator

The simulation results of the proposed oscillator are presented in this section. Since the oscillator is sensitive to the PVT, the simulation running across different corners is necessary. The output frequency of the oscillator can be 0.5MHz, 0.75MHz, 1MHz and 1.25MHz. The result patterns are similar. Therefore, the results under 0.5MHz are shown in this section as a representative. The temperature range is -40^oC - 125^oC and the supply voltage range is 2.1V - 5.5V.

5.2.1 Transient Analysis

The transient simulation result is shown in Figure 4-4. The waveform in orange color represents a startup signal for the biasing circuit. The waveform in blue color represents a delayed signal, which is set to make sure the reference voltage is settled. The waveforms in yellow and green color are the output waveforms generated by the oscillator with the frequency of 0.5MHz and 1MHz, respectively.

The first cycle of the output should be discarded because at the start time the reference voltage is at 0V. But after the reference voltage is stable, which is switching between two voltage references whose lower bound is 200mV as the Figure 5.6 shows.

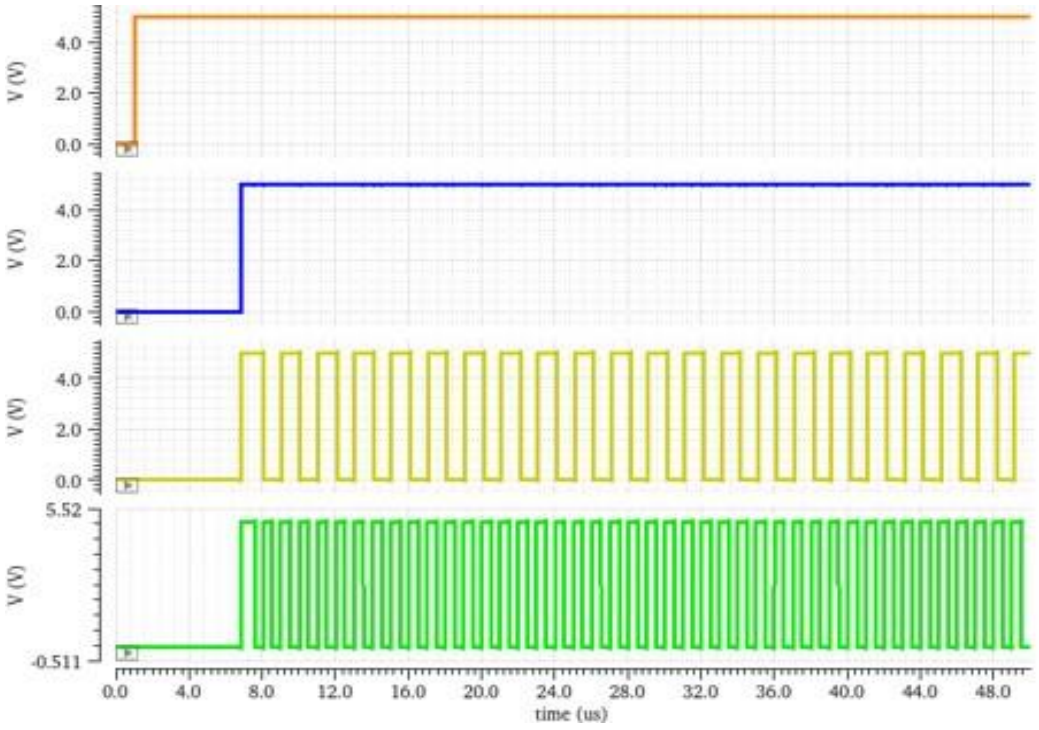

Figure 5.5: Transient analysis of the oscillator.

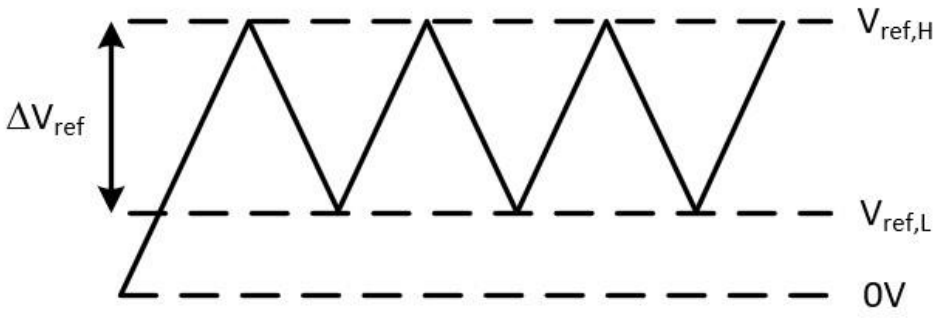

Figure 5.6: Window of reference voltage.

5.2.2 PVT Results Under Various Process Variation Corners

Process variation accounts for deviations in the semiconductor fabrication process. Variations in the process parameters can cause W/L variations in MOS transistors through impurity concentration densities, oxide thicknesses and diffusion depths. To test whether the proposed oscillator perform well, process variation corners are applied in the simulation process. The corners are: typical-typical (TT) corner, fast-fast (FF) corner, and slow-slow (SS) corner.

Figure 5.7 depicts the simulation results for the output frequency whose unit is kHz with PVT variations. The three temperatures are chosen for simulation: -40°C, -27°C (room temperature) and 125°C. The supply voltage has little impact on the output frequency while the process variation matters. The variation is 60kHz, which is 12% of the target. After trimming, the variation is decreased to 13kHz, which is 2.6% of the target, as illustrated in the Figure 5.8.

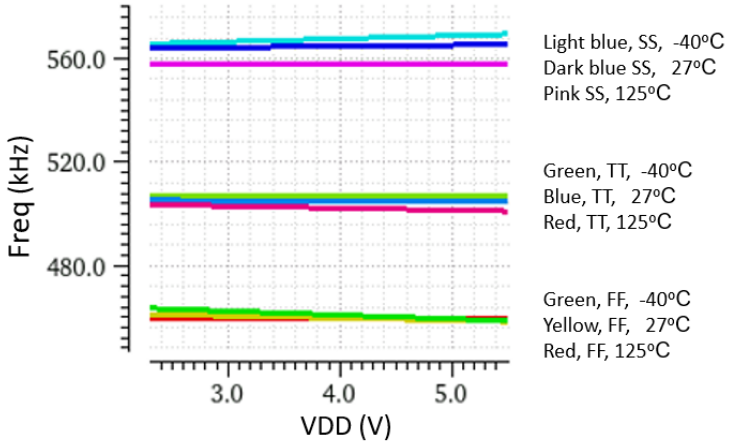

Figure 5.7: Frequency across different process corners.

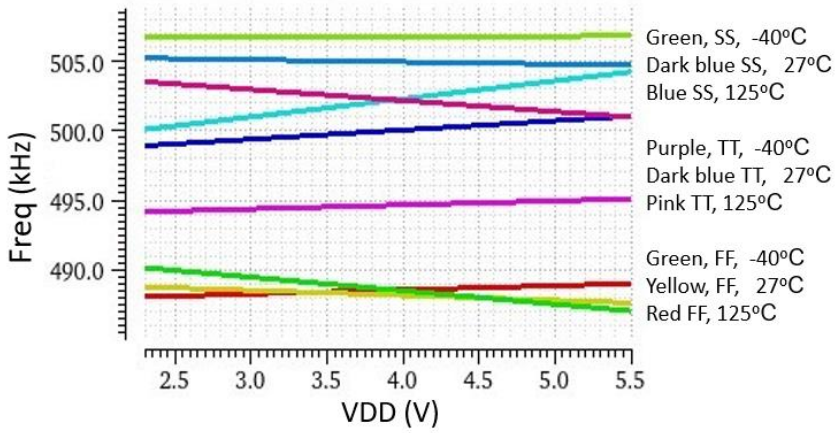

Figure 5.8: Frequency across different process corners with trimming.

5.2.3 Monte Carlo Simulation

The Monte Carlo simulation is applied to generate multiple simulated outcomes, and then uses the results to estimate the probability of each potential outcome. By generating multiple potential outcomes, the Monte Carlo simulation can help identify the most likely outcome, or the range of possible outcomes. The Monte Carlo simulation results are shown in Table 5.2.

Table 5.2: Monte Carlo Simulation Results

	$\mu - 4\sigma$	μ	$\mu + 4\sigma$
Frequency(kHz)	480	500	525

Chapter 6

CONCLUSION AND FUTURE WORK

In this chapter, a synopsis of this work is detailed in Section 6.1. Future direction of this work is pointed out in Section 6.2.

6.1 Conclusion

As the electronic systems are getting more widely used in automotive applications, the improvement of performance of the circuits is quite important.

In this thesis, a low power opamp is created and enhanced by altering the traditional design and incorporating the subthreshold approach. The proposed opamp is realized in 180nm standard CMOS process. According to simulation results, 420nW of powery is consumed in the propsed circuit. The open-loop gain is 74 dB while the phase margin is 72^{o}.

This work also presents a PVT tolerant oscillator is developed for automobile applications. The supply voltage range is 2.1V-5.5V and the temperature range is

-40^oC – 125^oC. According to the simulation results, the proposed design shows high performance which meets the specifications.

6.2 Future Work

The future work on this thesis can be aimed at improving the performance of the circuits. Future efforts can include the following considerations:

- Improve the opamp design for general applications
- Make modifications to the design to reduce the power dissipation of the oscillator.
- The accuracy of the proposed system can be increased by improving performance of the noise.
- Compare the simulation results with the test results obtained from future fabrication of the circuit is the 180nm CMOS process.

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