SILICON ON FERROELECTRIC INSULATOR FIELD EFFECT TRANSISTOR (SOFFET): A RADICAL ALTERNATIVE TO OVERCOME THE THERMIONIC LIMIT

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By

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ABSTRACT

The path of down-scaling traditional MOSFET is reaching its technological, economic and, most importantly, fundamental physical limits. Before the dead-end of the roadmap, it is imperative to conduct a broad research to find alternative materials and new architectures to the current technology for the MOSFET devices. Beyond silicon electronic materials like group III-V heterostructure, ferroelectric material, carbon nanotubes (CNTs), and other nanowire-based designs are in development to become the core technology for non-classical CMOS structures. Field effect transistors (FETs) in general have made unprecedented progress in the last few decades by down-scaling device dimensions and power supply level leading to extremely high numbers of devices in a single chip. High-density integrated circuits are now facing major challenges related to power management and heat dissipation due to excessive leakage, mainly due to subthreshold conduction. Over the years, planar MOSFET dimensional reduction was the only process followed by the semiconductor industry to improve device performance and to reduce the

power supply. Further scaling increases short-channel-effect (SCE), and off-state current makes it difficult for the industry to follow the well-known Moore's Law with bulk devices. Therefore, scaling planar MOSFET is no longer considered as a feasible solution to extend this law.

The down-scaling of metal-oxide-semiconductor field effect transistors (MOSFETs) leads to severe short-channel-effects and power leakage at large-scale integrated circuits (LSIs). The device, which is governed by the thermionic emission of the carriers injected from the source to the channel region, has set a limitation of the subthreshold swing (S) of $60\ mV/decade$ at room temperature. Devices with 'S' below this limit is highly desirable to reduce the power consumption and maintaining a high I_{on}/I_{off} current ratio. Therefore, the future of semiconductor industry hangs on new architectures, new materials or even new physics to govern the flow of carriers in new switches. As the subthreshold swing is increasing at every technology node, new structures using SOI, multi-gate, nanowire approach, and new channel materials such as III–V semiconductor have not satisfied the targeted values of subthreshold swing. Moreover, the ultra-low-power (ULP) design required a subthreshold slope lower than the thermionic-emission limit of $60\ mV/decade$. This value was unbreakable by the new structure (SOI-FinFET). On the other hand, most of the preview proposals show the ability to go beyond this limit. However, those pre-mentioned schemes have publicized very complicated physics, design difficulties, and process non-compatibility.

The objective of this research is to discuss various emerging nano-devices proposed for ***sub-60 mV/decade*** designs and their possibilities to replace the silicon devices as the core technology in the future integrated circuit. This dissertation also proposes a novel

design that exploits the concept of negative capacitance. The new field-effect-transistor (FET) based on ferroelectric insulator named ***Silicon-On-Ferroelectric Insulator Field-effect-transistor (SOFFET)***. This proposal is a promising methodology for future ultra-low-power applications because it demonstrates the ability to replace the silicon-bulk based MOSFET, and offers a subthreshold swing significantly lower than $60\ mV/decade$ and reduced threshold voltage to form a conducting channel. The proposed SOFFET design, which utilizes the negative capacitance of a ferroelectric insulator in the body-stack, is completely different from the FeFET and NCFET designs. In addition to having the NC effect, the proposed device will have all the advantages of an SOI device.

Body-stack that we are intending in this research has many advantages over the gate-stack. First, it is more compatible with the existing processes. Second, the gate and the working area of the proposed SOFFET is like the planar MOSFET. Third, the complexity and ferroelectric material interferences are shifted to the body of the device from the gate and the working area. The proposed structure offers better scalability and superior constructability because of the high-dielectric buried insulator. Here we are providing a very simplified model for the structure. Silicon-on-ferroelectric leads to several advantages including low off-state current and shift in the threshold voltage with the decrease of the ferroelectric material thickness. Moreover, having an insulator in the body of the device increases the controllability over the channel, which leads to the reduction in the short-channel-effect (SCE). The proposed SOFFET offers low value of subthreshold swing (S) leading to better performance in the on-state. The off-state current is directly related to S. So, the off-state current is also minimum in the proposed structure.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled "Silicon-on-Ferroelectric Insulator Field Effect Transistor (SOFFET): A Radical Alternative to Overcome the Thermionic Limit" presented by Azzedin Es-Sakhi, candidate for the Doctor of Philosophy degree, and hereby certify that in their opinion it is worthy of acceptance.

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LIST OF ACRONYMS

BOX	Buried Oxide (isolation layer of an SOI structure)
BTBT	Band-to-Band-Tunneling
CAD	Computer aided design
TCAD	Technology Computer Aided Design
CMOS	Complimentary metal-oxide-semiconductor
CNT	Carbon nanotube
DG	Double gate
DIBL	Drain-induced-barrier-lowering
FET	Field-Effect-Transistor
GAA	Gate All Around
GNR	Graphene nanoribbon
ITRS	International technology roadmap for semiconductors
MOSFET	Metal semiconductor field effect transistor
NW	Nanowire
SG	Single gate
SWNT	Single walled carbon nanotube
TFET	Tunnel field effect transistor
WKB	Wenzel-Kramer-Brillouin approximation

UTB	Ultra-Thin-Body
SCE	Short-channel-effect

LIST OF SYMBOLS

C	Capacitance
C_{dep}	Depletion capacitance
C_{ox}	Gate oxide capacitance
κ	Dielectric Constant
t_{ox}	Gate oxide thickness
t_{Si}	Strained silicon layer thickness
L	Gate length
h	Planck constant: $4.135 \cdot 10^{-15}\ eV/s$
K	Boltzmann constant: $8.617 \cdot 10^{5}\ eV/K$
m^*	Effective Mass
φ_m	Work function of control gate
ψ_s	Surface potential
N_{sub}	Substrate doping
V_{TH}	Threshold voltage
V_T	Thermal voltage
I_{sub}	Subthreshold Current
I_{off}	Off-state current
I_{on}	On-state current
S	Subthreshold swing

ε_0	Dielectric constant of the vacuum: $8.854 \cdot 10^{-12} As/(Vm)$
ε_r	Relative dielectric constant
q	Elementary charge: $1.6022 \cdot 10^{-19} C$
V_{DS}	Source to drain voltage
V_{GS}	Gate to source voltage
T_{WKB}	Tunneling Probability

DEDICATION

I would like to dedicate my dissertation to all my family especially my beloved grandmother

CHAPTER 1

INTRODUCTION

This dissertation discusses the emerging field of ultra-low-power devices, and investigation new approach and design of a *sub-60mV/decade* field effect transistor. It also discusses various materials and architecture to break the limit of $60mV/decade$. Toward the end of this research, a new concept of field-effect-transistor terminology based on negative capacitance phenomenon is introduced and the principle of operation is explained.

1.1. Organization

This dissertation consists of eleven chapters beginning with this chapter. Chapter 1 introduces the objectives and scope of the project, the background of emerging nanotechnology, as well as the layout of this dissertation. Chapter 2 describes in detail the subthreshold swing which is explained based on device dimension and materials with the most promising future in IC industry. Chapter 3 provides an overview of Multi-gate/FinFET devices, their design geometry, and a short discussion about the advantage and disadvantage, and the reason behind switching to multi-gate devices. Chapter 4 discusses the tunneling field-effect-transistor that involves various structures and different materials. Chapter 5 explains and summarizes the I-MOS and Nanowire schemes. Chapter 6 covers the application of ferroelectric material in Field effect transistor.

Chapter 7 presents an analytical model to approximate the subthreshold swing of SOI-FinFET. Chapter 8 proposes the model of Multi-CNT channel TFET. Chapter 9 and 10 address the body-stack proposals to lower subthreshold swing, and threshold voltage based on negative capacitance concept. Finally, chapter 11 lists the advantages of this approach, presents some manufacturing process, introduces future works and concludes this dissertation.

1.2. Thesis Objectives

The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the building block of all computing systems. MOSFETs handled an excessive material and structure development in the last decade. However, the advantage of this device starts vanishing in nanometer scale. Researchers are investigating numerous unconventional designs to solve the concern of density and power consumption (especially at standby or sleep mode) of the conventional MOSFET. Several nanotechnology methodologies to overcome the issues of downscaling and extend Moore's Law broadly stretched from materials substation point of view going through new architectures to new physics and/or operating principals.

This dissertation presents a study of the prospects of emerging FinFET and Carbon Nanotubes (CNTs) based FET device technologies for ultra-low-power subthreshold design, also investigate a new field-effect-transistor (FET) design based on ferroelectric material to utilize negative capacitance effect in subthreshold design. The nano-electronics

is an emerging field whose goal is not limited to surpass the existing technology but also to present a design with lower power consumption.

The main objectives of this dissertation are as follows:

- Understand the emerging technology devices characteristic, fundamental equation and mathematical analysis of the subthreshold design.
- Summary of the existing devices and proposals like FinFET and TFET and their application in ultra-low-power designs.
- An analytical model to approximate the subthreshold swing for SOI-FinFET
- Introducing a new field-effect-transistor design to lower subthreshold.
- Analysis and study of the proposed structures.

1.3. Nanotechnology Challenges

One of the challenges facing the conventional MOSFET is scaling the gate oxide to improve the transistor performance. Down-scaling the oxide thickness will increase the gate oxide capacitance and therefore, increase the drain current, lower the threshold voltage and improve the device speed. However, decreasing the gate oxide increases gate tunneling current, hence an increase of off-state current. Another challenge is the device channel down-scaling which causes the depletion areas of source and drain to be exceedingly close to each other and they can merge. This issue causes a high current leakage. This

phenomenon called Drain-induced-barrier-lowering (DIBL). Because of this short-channel-effect upsurge at every generation, planar devices are closer to their scaling limit.

The off-state current (I_{off}) has been exponentially increased by multiple times in every generation. To obtain a high performance MOSFET, high mobility is required. To achieve lower subthreshold slope and lower threshold voltage, high-κ materials are needed instead of SiO_2. This integration must consider mobility degradation or poor interference between the silicon substrate and any new material. Although supply voltage is decreased significantly, the number of transistor per chip is nearly doubled every 18 to 24 months (Moore's Law) causing the overall power consumption to increase dramatically. As we reach the end of MOSFET era, multiple proposals, approaches, and research are considered to keep Moore's law lively. For that reason, integrated circuit (IC) technologists are looking for a new material or a new technology with completely different concepts to start a new generation of transistors. FinFET and CNTFET are two promising substitutions to the conventional MOSFET.

1.4. Recent and Emerging Device Technologies

1.4.1. Emerging field of ultra-low-power devices

ICs power management has become a major concern in last decade due to the increase of number of transistor in single die Figure 1.1. Furthermore, down scaling gives privilege of faster devices under low supply. However, short-channel-effect increases

significantly to increase off-state current. Additionally, the supply voltage scaling increases delay and decrease noise margin therefore, the supply voltage scaling slowed down considerably in the last decade. Moore's Law is described in Figure 1.1 while Figure 1.2 shows the scaling trend at every technology node. An articulation of the projected chip sizes and the number of transistors per chip of the next technology generations is shown in Figure 1.3 [1, 2].

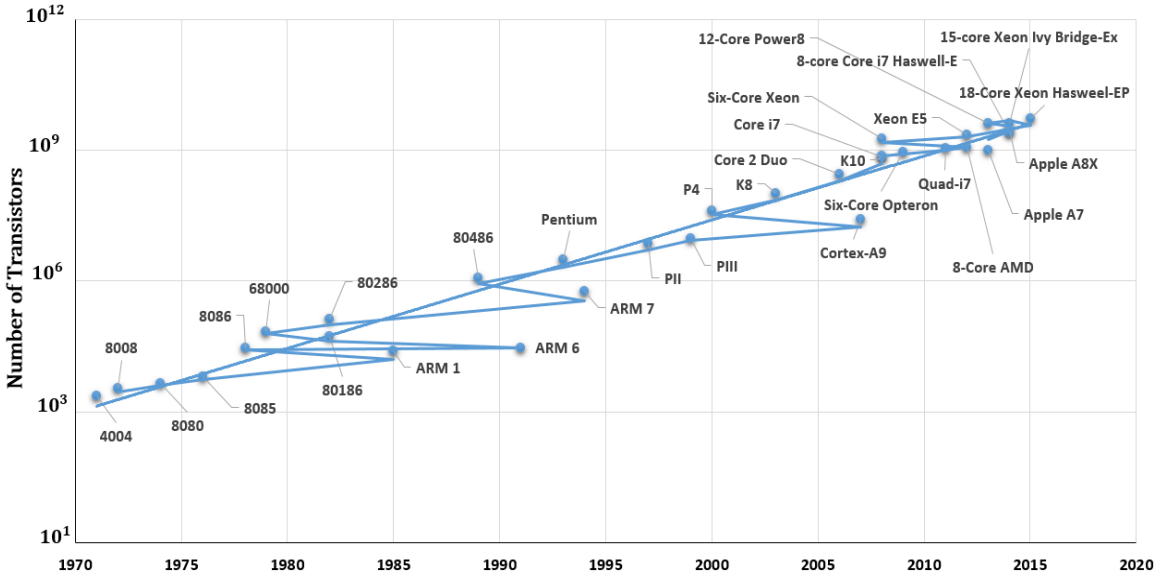


Figure 1.1: The progress of technology shows the increase of number of transistors at every process generation representing the projection of Moore.

Two figures of merit, on-state current (I_{on}) and off-state current (I_{off}), are strongly considered at the design level of every technology node. On-state current (I_{on}) and off-state current (I_{off}) both determine the power consumption and the performance of the

device. I_{on} is proportional to $(V_{GS} - V_T)^{\alpha}$ (α: alpha power law) and I_{off} is exponentially proportional to $q \times (V_{GS} - V_T)/nKT$. To turn on the device faster, low V_T is needed where for low $I_{off,}$ high V_T is needed. To keep standard functionality, the factor $(V_{GS} - V_T)$ has to be scaled by the same level. Therefore, high I_{on}/I_{off} ratio is required while lowering the supply voltage. Note that the there is a tradeoff between the power scaling and performance.

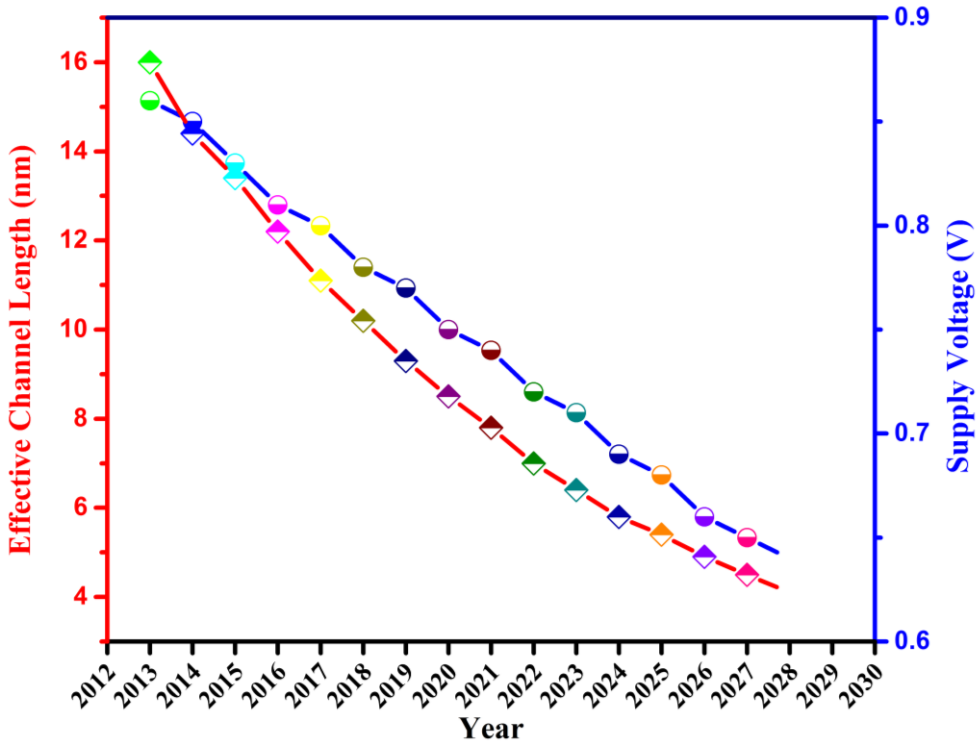


Figure 1.2: Supply voltage scaling trend at every technology node reported by ITRS 2012.

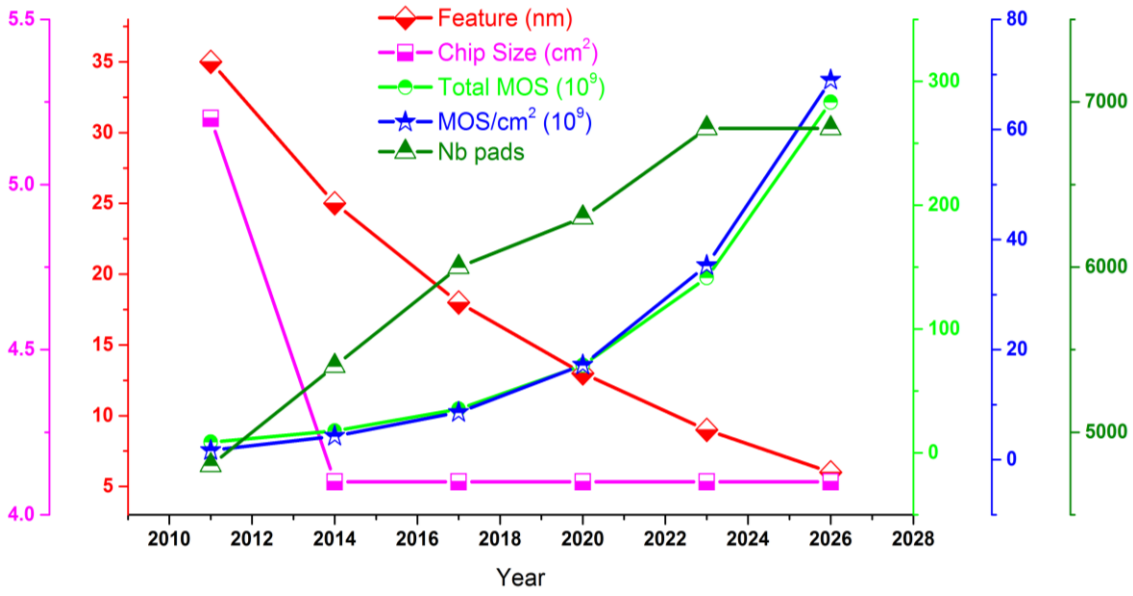


Figure 1.3: Number of MOS per chip and chip size projection of upcoming technology node [2].

Field effect transistors in general have made marvelous progress in the last few decades by down scaling device dimensions and power supply level, leading to extremely high numbers of devices in a single chip. High-density integrated circuits are now facing major challenges related to power management and heat dissipation due to excessive leakage, mainly due to subthreshold conduction. Subthreshold swing 'S' represents the behavior of the device at voltage lower than threshold voltage. It is a figure of merit for the ultra-low-power designs. Figure 1.4 illustrates the increase of the subthreshold swing as the scaling move toward sub nano-technology. S increases from 250nm to 130nm

technology nodes due to the aggressive scaling of oxide thickness. In contrast, excessive increase in gate leakage current slows down the gate oxide scaling, and S increases beyond 130nm which poorly affects the subthreshold operation by lowering I_{on}/I_{off} ratio.

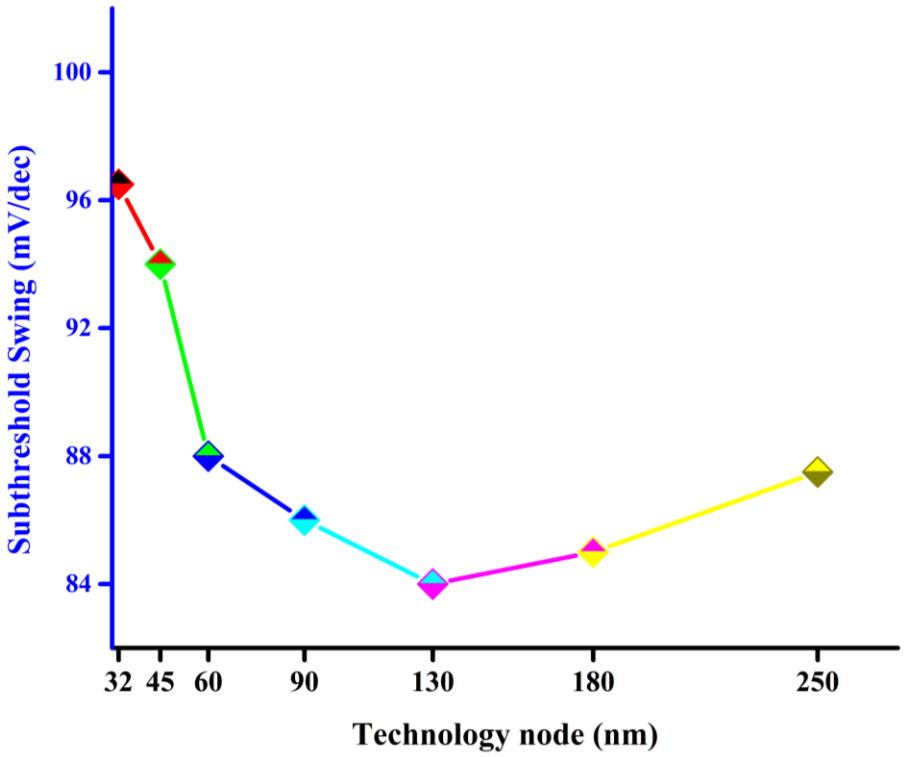


Figure 1.4: Subthreshold swing at different technology nodes [3].

Most academics believe that the fundamental thermodynamic limits on the minimum operational voltage and switching energy of conventional transistors are given by this limit of $S = 60\, mV/decade$, which is known as the '*Boltzmann tyranny*'. Even with the excellent electrostatic and enhanced transport properties in all the CMOS-based

transistors (bulk, FinFET, and fully depleted silicon-on-insulator: FDSOI), S will be over $60mV/decade$ at room temperature. Some novel transistor structures like nanowire FETs (NWFET), the carbon nanotube based tunnel FETs (T-CNFET), the impact ionization MOS-based transistors (I-MOS), and Tunnel-FET (TFET) have exhibited lower value of S. Figure 1.5 shows 'S' of various technology including the proposal of this research [4].

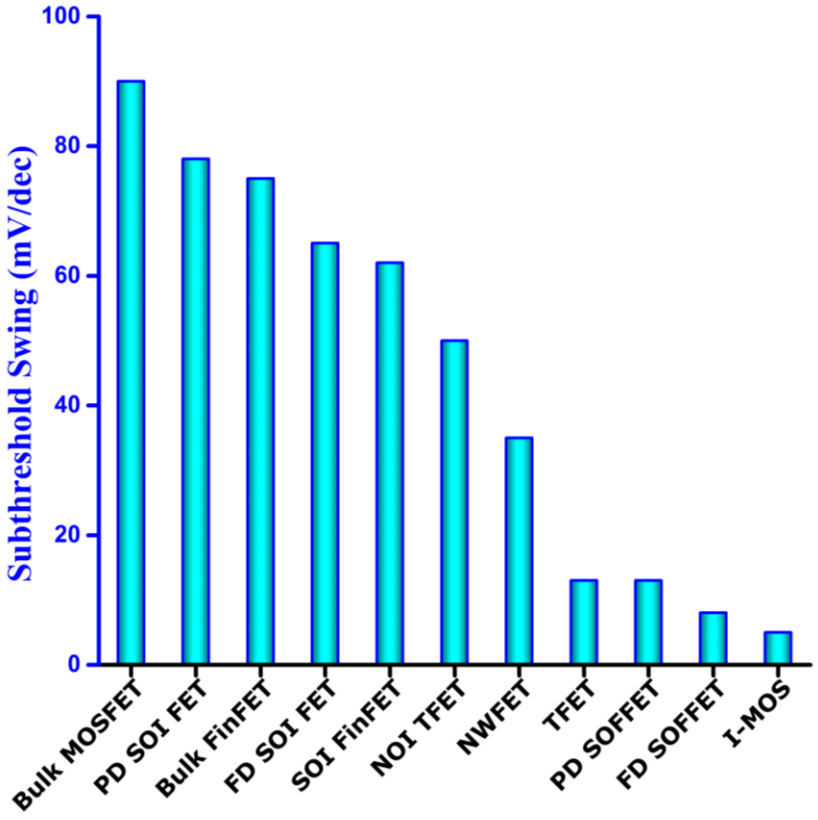


Figure 1.5 Subthreshold swings (S) reported for various CMOS and emerging Technologies [4].

Recently, DARPA initiated a program (STEEP: Steep-subthreshold-slope Transistors for Electronics with Extremely-low-power) with a target of $S \leq 20mV/decade$ (see Figure 1.6). Researchers are actively considering novel technologies based on tunneling mechanism of electrons. Carbon Nanotube Tunnel FET, Si/SiGe Vertical Tunnel FET, and Si Lateral Tunnel FET are leading to potential candidates to replace the conventional MOSFETs in the next generation ultra-low-power electronics that require very low value of S. Scientists and researchers are also considering new materials like ferromagnetic insulator.

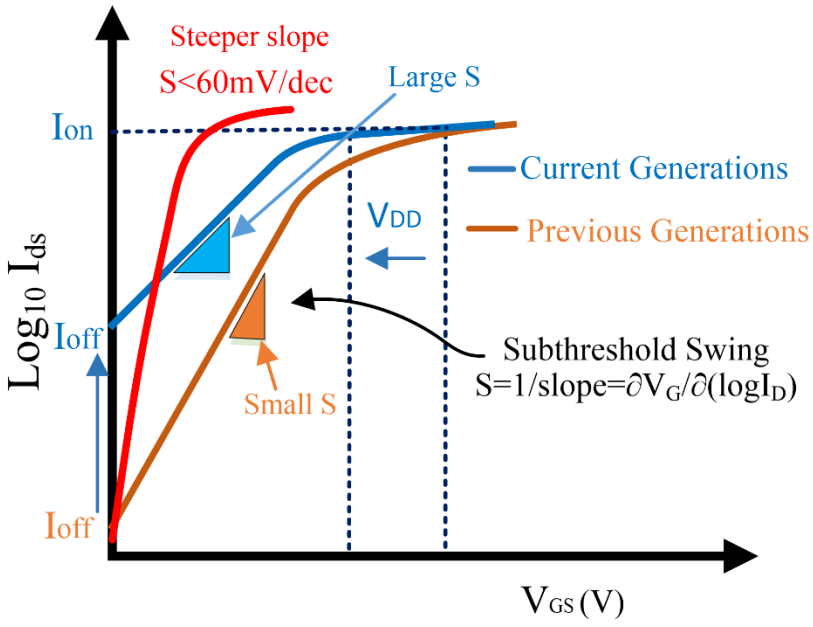


Figure 1.6: Subthreshold swing trend in conventional devices - past and current generations.

A brief discussion of the current researches and different schemes are presented in the next section and a detail discussion is presented in the upcoming chapters.

1.4.2. Silicon-On-Insulator (SOI) devices

The demand for a high-speed, high-performance, and low-power devices leads to devices and fabrication process to go beyond ultra-deep sub-micron (UDSM) technologies such 32nm and 22nm. However, these technology nodes and beyond cause severe short-channel-effects (SCEs). SCEs can be reduced by decreasing or eliminating source/drain to substrate junctions. This approach is set to separate or isolate the active region of the device from the underlying silicon substrate. SOI — silicon-on-insulator was introduced to limit the influence of the underlying silicon substrate leading to reduction in short-channel-effects. SOI refers to placing a thin layer of silicon on top of an insulator such as SiO_2. SOI devices reduce the capacitance at the source and drain junctions significantly by excluding the depletion regions extending into the substrate. SOI substrate leads to a dielectric isolation of the devices to lower the influence of the parasitic effects occurred in bulk devices. SOI has many promising features over the bulk technology [5, 6]. Merging this technology with scaling the gate length of MOSFETs has enhanced the speed of the device in addition to short-channel-effect reduction. Majumdar *et al*. show that a fully depleted SOI (FDSOI) transistors are expected to bring technology down under 22nm. They have also indicated that using back-gated and extremely thin silicon-on-insulator (ETSOI)

devices with thin buried oxide (BOX) will also lower the threshold voltage and allow lower voltage operation [7].

1.4.3. Carbon nanotube Field-effect-transistor (CNTFET)

The demand for fast computing devices, more applications, smaller dimensions and low-power consumption requires new architecture and/or material exploration to be the base of the future ICs. CNTs become known as the great solution to the power and scaling of future devices. Carbon nanotubes (CNTs) can be considered as single layer thick sheet of rolled graphite (SWNT). CNTs have taken much attention due to their abilities to carry high current. SWNTs are attractive material due to their unique electrical properties. SWNTs also drawn a significant attention to be integrated into future logic switches, and interconnects.

CNTFET is a three-terminal logic switch. The device consists of semiconducting nanotube (channel) sited between the source and the drain contacts, and the third terminal is the gate that controls the electrostatic of the device. An extensive research is recently conducted to understand the device physics, and properties. High carrier mobility, superconducting material, high stability, high scalability, ballistic or near-ballistic transport, the ability to be integrate with *high-κ* materials, low-power, low-leakage, and the electrical properties that can either be metallic or semiconducting is a list of the major properties that made the carbon nanotube based field-effect-transistor the future building

black of the upcoming nano-electronic circuits. All these decencies have made the CNTFET the first candidate to replace the conventional MOSFET for the future IC technology.

CNTFET using carbon nanotube as semiconducting channel and silicon substrate wafer was fabricated in 1998 [8]. This transistor had reported a poor performance. Since that time, the carbon nanotube based FET got extensive attention due to its outstanding properties. CNTFET shows an excellent compatibility with CMOS manufacturing process due to its similarities in structure and electrical operations. Another decency of the *n-type* and *p-type* of CNTFET is that they can be the same size, as opposed to CMOS technology where *p-type* has to be 2 to 3 times larger than *n-type*. Despite their functioning similarity, the CNTFET electrical switching principles and the physics dependence have not been fully explored. There are a set of mathematical models and numerical approximations as the base of the CNTFET operations. Those numerical models that depend on certain conditions and structures have not become an evaluation standard [9].

1.4.4. Multi-gate transistors

As desired to keep Silicon technology as the base technology while modernizing future devices; cost is an important factor, Tri-gate known as FinFET was introduced due to its similarities to conventional MOSFET. The fin shape introduces a gate that surrounds the channel from three sites. This structure presents a better control over short-channel-

effect. The new structure also shows a higher I_{on}/I_{off} ratio as compared to conventional MOSFET. FinFETs present a better performance, lower leakage current, and fabrication compatibility with CMOS process [10]. Down-scaling of the MOSFET was the only road to achieve high performance and low-power consumption. The gate length decreasing has been very aggressive. According to the International Technology Roadmap for Semiconductors (ITRS) projection of 2020-2025 the gate length of the MOSFET can be scaled down to 5-7 nm range. The planar MOSFET physics may not be able to maintain the basic principle of operation [11]. By that time, other technologies could be ready for a smooth transition away from the conventional MOSFET. New devices like tunnel transistors or the current 3D devices are very promising to take over. The FinFETs have substantial progress since it came out in 2012. FinFET third generation is already on the way.

1.4.5. Tunneling field-effect-transistors (TFETs)

The tunneling field-effect-transistor has been widely explored and multiple proposals are presented. The tunneling phenomenon was introduced to overcome the thermal voltage limitation of the conventional MOSFET. Multiple proposals based on Band-To-Band tunneling (BTBT) which includes several materials and structures were proposed. Band-To-Band tunneling devices, recommended by numerous researchers, shows that the subthreshold swing can be lower and $60mV/decade$ (at room temperature)

since it is independent of the thermal voltage (KT/q) [12]. There are many demonstrations showing a lower subthreshold swing using the BTBT. Zener or Esaki diode concept was utilized to build a T-FETs either based on silicon tunneling or CNTs tunneling. The tunneling robustness is depending on the width of the depletion region of the P-N junction, and thus the doping profile in both junctions and the channel. For high doping, the depletion width is small which allows a better tunneling.

Emerging SWCNTs and band-to-band tunneling (BTBT) have been a hot subject that encountered deep research in recent years. BTBT is the ability of electrons to tunnel from the valence band through the semiconductor band-gap to the conduction band or vice versa [4]. This phenomenon of BTBT will enable the subthreshold slope to go below the thermal voltage limitation. A widely-known arrangement of BTBT devices is based on *p-i-n* junction. This pattern introduced in [7] where carbon nanotube (CNT) is employed as the channel. CNT is placed between the *n-doped* drain and the *p-doped* source to give *p-i-n* junction. This geometry shows a subthreshold slope around $40mV/decade$. In [13], two geometries were compared; *p-i-n* and *n-i-n* CNT based. Both geometries have the advantage of driving a high current, functionality in high frequency, and low off-current. This research also indicates the possibility of subthreshold slope lower than the thermionic-emission limit of $60mV/decade$. In [14], a dual-gate nanowire field-effect-transistor

(NW-FET) built upon BTBT was proposed. This device principle of operation is based on gated Esaki diode. The device shows great operating characteristics.

The need of what is called in some literature "*Green*" devices, which are not governed $by \frac{kT}{q} \sim 60mV/decade$. These types of devices require the exploration of ground-breaking materials. Tunneling in state-of-the-art group III and V was proposed to overcome some of the concerns presented by the previews design. III-V staggered-hetrojunctions-based FET were considered due to their small bandgap and their compatibility with current CMOS process. These devices' design achieve a low subthreshold swing. However, III-V tunneling transistor physics are not fully explored and they demonstrate a low on-state current.

1.4.6. Negative capacitance gate-stack transistors

Ferroelectric materials are widely explored and considered to be groundbreaking emerging material. Previous research shows that replacing the ordinary gate insulator stack with a negative capacitance gate-stack will provide a power boosting to the device allowing it to operate under low voltage. The negative capacitance gate-stack is explained in [15] and the concept is proved in [16]. This proposal provides a steep subthreshold slope and the ability to operate at low voltage (reduced threshold voltage). More details on this subject are presented in chapter 6.

1.5. Contribution

In this study, a concept of a new field-effect-transistor (FET) based on ferroelectric insulator is introduced. The proposed design is named ***Silicon-on-Ferroelectric Insulator field-effect-transistor (SOFFET)***. The design combines the concept of negative capacitance in ferroelectric material and silicon-on-insulator (SOI) device. The design proposes that by burying a layer of ferroelectric insulator inside the bulk silicon substrate, an effective negative capacitance (NC) can be achieved. The NC effect can provide internal signal boosting that leads to lower subthreshold swing, which is the prime requirement for ultra-low-power circuit operation. In addition to introducing the concept of a new device SOFFET, this paper presents close form models to calculate the subthreshold swing and the threshold voltage of the proposed device. These models are used to analyze the dependence of subthreshold swing on the materials and geometric parameters of the device. Current-voltage (I-V) characteristics of the proposed device have also been derived. It is demonstrated that by carefully optimizing the thickness of the ferroelectric film, dielectric property of the insulator, and the doping profile of the device channel, the subthreshold swing and the threshold voltage can be reduced.

CHAPTER 2

SUBTHRESHOLD SWING

Subthreshold swing is an important figure of merit that describes how fast a device can turn ON and OFF. In the planar MOSFET, the subthreshold swing 'S' is limited by the thermal voltage $\left(\frac{KT}{q}\right)\ln 10\ (= 60\,mV/decade)$. This parameter represents the behavior of the device at subthreshold region.

2.1 Introduction

Off-state current (I_{off}) is considered as the main issue of down-scaling trend. I_{off} current is increasing at every generation of MOSFETs and no longer can be neglected. I_{off} determines the power consumption of chip in its idle (sleep) state. On another hand, the on-state current (I_{on}) determines the minimum voltage needed to turn ON the MOSFET. One factor that provides a clear understanding of the ratio I_{on}/I_{off} is called subthreshold swing. This factor provides design performance and ability of driving devices with minimum power consumption. As the number of transistors on a chip keeps increasing, the power consumption and leakage become the major concern in future ULSI design. Subthreshold circuit design is an ultimate solution to stay within the power budget. The design of ultra-low-power circuit in the subthreshold regime required a deep study of subthreshold swing and the parameters that fine-tune this factor. To evaluate the power

consumption, an extensive work has concentrated on threshold voltage V_{TH} where it's defined to be the amount of voltage required to turn on the MOSFET. The region where V_{TH} is less than V_{GS}, is called subthreshold region. One parameter that characterizes the MOSFET is the slope factor 'S'. S-factor is defined as the change in the gate voltage V_{GS} required to reduce subthreshold current I_{DS} by one decade.

2.2 Subthreshold Region

The basic study discusses the MOSFET behavior in linear region and saturation region. The subthreshold region refers to the region where V_{TH} less than V_{GS} This region reflects how the MOSFET can switch ON/OFF. Figure 2.1 shows the VTC of a MOSFET device in subthreshold region with the drain current in log scale ($log\ I_D$) and (V_{GS}) in linear scale. Since 'S' is defined as the inverse of the slope of this VTC, it indicates that the change in V_{GS} needed to adjust the current I_D by one decade. Normally, it is expressed in $mV/decade$ unit. In other word, S is the amount of change in V_{GS} requires to produce a *10× change* in I_D. Experimentally, I_{DS} has shown to be proportional to $\exp\frac{q(\psi_s)}{nkT}$, with $\psi_s$as the semiconductor surface potential, K as the Boltzmann constant, T as the absolute temperature, and q as the electron charge.

The Figure 2.1 presents the behavior of subthreshold swing as function of I_{off} and I_{on}. It also shows a figure of merit considered in ICs design which is the ratio I_{on}/I_{off}. I_{on} is a measure of the transistor drive current at fixed $V_{gs} = V_{ds} = V_{DD}$ where I_{off} is measured as device off-state current (not totally off due to leakage).

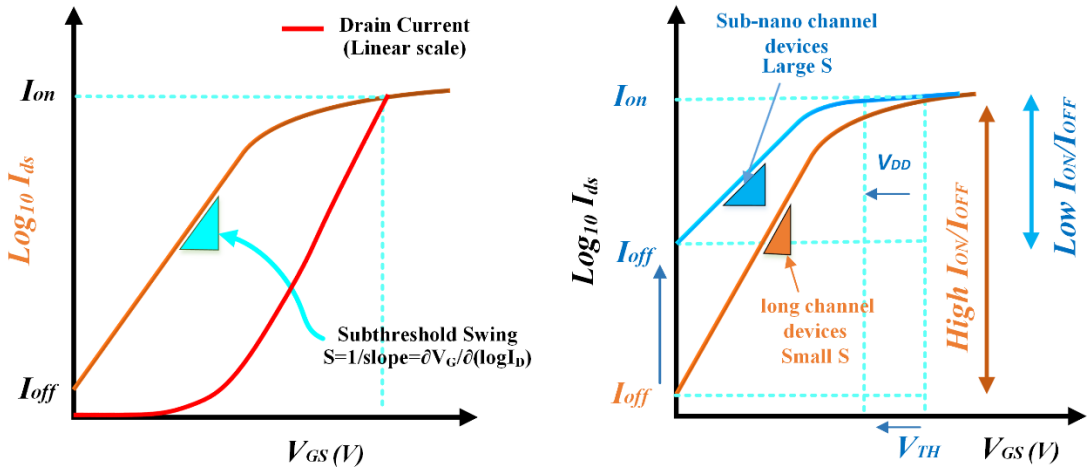


Figure 2.1: Device behavior at subthreshold region. a) Plot describes the exponential relationship between I_{DS} to V_{GS}, b) I_{on}/I_{off} ratio of the device in long-channel and short-channel devices.

Figure 2.1.a shows the behavior of the conventional MOSFET in subthreshold regime. Figure 2.1.b illustrates the subthreshold characteristics in long and short-channel devices and the necessity for high I_{on}/I_{off} ratio for better performance. A better performance for ultra-low-power designs are presented in steeper slope (small S) where I_{on} is measured high and I_{off} is measured low, hence, the reduced threshold voltage. The subthreshold slope is defined as:

$$S^{-1} = \frac{\partial \log I_D}{\partial V_G} = \frac{1}{2.3(k_B T/q)} \frac{\partial \psi_S}{\partial V_G} \tag{2.1}$$

And the subthreshold swing is defined as:

$$S = \frac{\partial V_G}{\partial (\log I_D)} = \frac{\partial V_G}{\partial \psi_s}\frac{\partial \psi_s}{\partial (\log I_D)} = \left(\frac{k_B T}{q}\right)\left(\frac{\partial V_G}{\partial \psi_s}\right) \times \ln(10) \qquad (2.2)$$

Where $\frac{\partial V_G}{\partial \psi_s}$ called the body factor and titled ɳ. V_G is related to ψ_S by a capacitive voltage divider show in Figure 2.2. S could be expressed as:

$$S = \ln(10)\frac{kT}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \qquad (2.3)$$

If there is a significant trap density (C_{it}: surface state capacitance):

$$S = 2.3\frac{kT}{q}\left(1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}}\right) \qquad (2.4)$$

$$S_{min} = 2.3(KT/q) = 60\, mV/dec \qquad (2.5)$$

Where C_{dep} is the depletion region capacitance, and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ is the gate oxide capacitance per unit area. S also characterizes the importance of the interface traps on device performance, and can be approximated as in (2.4) using the capacitive voltage divider of Figure 2.3 [17]. The depletion region capacitance C_{dep} is proportional to doping density N_A and $W_{dep}$is the maximum depletion width in strong inversion. We can write: $C_{dep} = \frac{\varepsilon_{si}}{W_{dep}} \propto \sqrt{\frac{1}{N_A}}$.

Smaller values of S give a better turn-on performance of the device, because the smaller value of S means that for a certain change in the current, we need lower voltage change or for a certain change in voltage, we can get higher current change, leading to

larger gain of the device. From equations (2.3) and (2.4), we can predict that if theoretically it is possible to make both C_{it} and C_{dep} zero in a conventional MOSFET device, then the

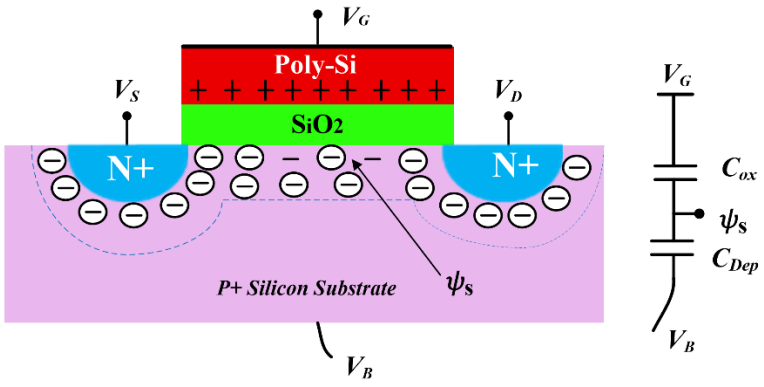


Figure 2.2: MOSFET and its equivalent capacitance coupling.

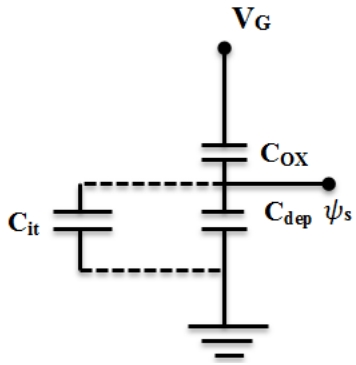


Figure 2.3: MOSFET equivalent capacitance coupling in case of significant trap density.

value of S at $T = 300°K$ temperature will be $60mV/decade$ as shown in (2.5), which is known as the theoretical minimum (S_{min}) subthreshold swing. This value is achievable only in the oxide thickness in silicon device approaches to zero. However, under any

practical scenario, this is not possible, and the factor η in (2.3) and (2.4) will be always larger than 1 (η ≥ 1). Therefore, S in silicon device is larger than $60mV/decade$ (typically, it is in the range of $80 - 120mV/decade$).

2.3 How to Achieve S Less Than 60mV/decade

The body factor is defined earlier as:

$$\eta = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_{dep}}{C_{ox}} \tag{2.6}$$

The equation (2.6) shows that η has multiple key dependencies that have significant impact on the value of S. Below is a list of those key parameters and how they relate to S.

- The gate oxide capacitance per unit area is defined as $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ where t_{ox} gate oxide thickness and ε_{ox} is the permittivity of the oxide. Decreasing t_{ox} will give a large C_{ox} accordingly, a lower η. Hence, a sharper subthreshold can be achieved ($t_{ox} \downarrow \rightarrow C_{ox} \uparrow \rightarrow \eta \downarrow$→Sharper subthreshold).
- Higher dielectric constant (*high-κ*) such as HfO_2 to replace SiO_2 has become necessary requirement for gate insulator. *High-κ* materials lead to high oxide capacitance which leads to high I_{on} and a decrease in gate tunneling by several orders hence low I_{off}.

- Substrate doping: The subthreshold voltage is controlled by doping of the channel. The thickness of the depletion layer depends on the doping level. Lower doping causes a thicker depletion layer, and therefore a higher depletion capacitance, and a softer subthreshold ($N_A \uparrow\rightarrow C_{dep} \uparrow\rightarrow \eta \uparrow\rightarrow$ Softer subthreshold).
- Substrate bias: When a substrate bias is applied the depletion thickness increases, and the subthreshold swing decreases. ($|V_{bs}| \uparrow\rightarrow C_{dep} \downarrow\rightarrow \eta \downarrow\rightarrow$ Sharper Subthreshold)
- Temperature: At room temperature ($300°K$), the ideal limit of S is $60mV\ /decade$. Normally, devices always work in higher temperature due to heat dissipation; S will be higher at greater temperature than room temperature. S can be also lowered at lower temperature. The equations (2.3) and (2.4) show that the subthreshold swing is proportional to the temperature T. Moreover, the subthreshold slope is proportional to 1/T ($T \uparrow\rightarrow$ Softer Subthreshold).

There is a trade-off between V_T and I_{on}/I_{off} ratio. Low V_T is required to have a high on-state current, where V_{TH} is needed for low off-state current. The equation (2.7) shows the saturation drain current dependencies of supply voltage/power and threshold voltage.

$$I_{DSAT} \propto (V_{DD} - V_T)^{\alpha} \qquad 1 < \alpha < 2 \qquad (2.7)$$

Leakage mostly happened when the circuit is inactive, this waste of power represents in I_{off}. To reduce the device leakage, long-channel and large threshold voltage are required. Conversely, performance and power budget are compromised.

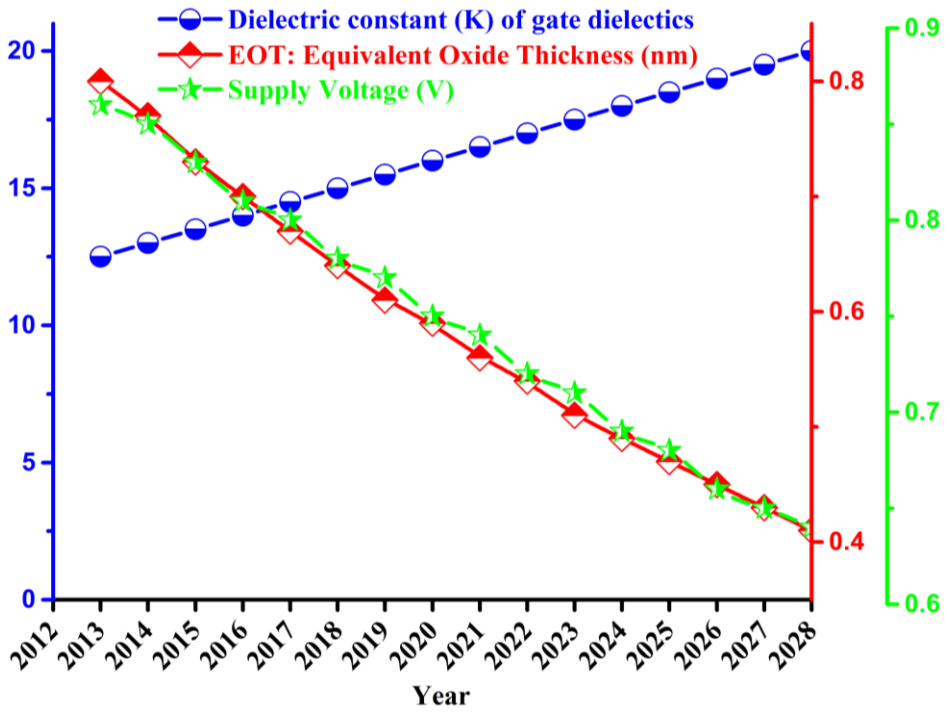


Figure 2.4: Dielectric constant of some *high-κ* materials suitable for oxide thickness below 1nm.

2.4 High-κ Gate Insulator

The electric field is the key to speed up the channel formation of the transistor, therefore a fast switching. Lowering the gate oxide thickness improved the electric field

applied by the gate at every technology node. Hence, increasing the gate capacitance and thereby drive current. At sub-nano scale, SiO_2 can no longer serve this purpose due to the physics limitation (as the thickness scales below 2nm), and leakage upsurge. Farther scaling would increase the electrons tunneling and therefore increase gate current leakage. To overcome this issue, new materials with high dielectric constant (*high-*κ) are used to serve as gate oxide. Some of these materials are presented in Figure 2.4. The new gate insulator materials that are investigated must fit certain fabrication process requirements. These requirements are discussed in [18, 19].

CHAPTER 3

MULTI-GATE DEVICES

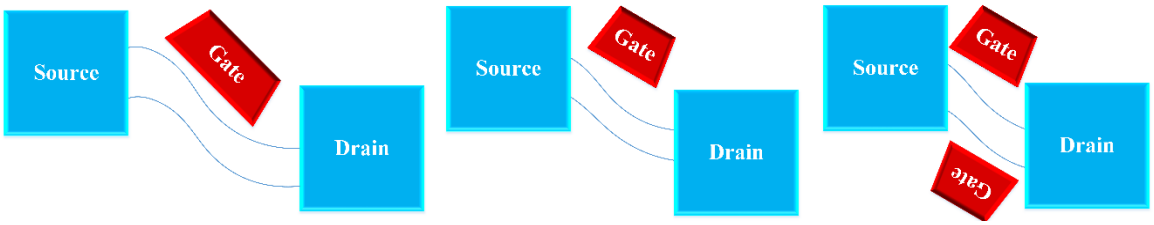
Researchers are currently investigating a variety of structures and materials to use for the future ICs designs. This chapter is a summary of Multi-gate structure and its advantages and applications.

3.1 SOI and Multi-Gate Devices

As the transistor shrinks, the device length also shortens. This pattern diminishes the gate capability of controlling the channel. This dimensional reduction causes a current flow even at off-state. As a result, the power consumption at idle state increases drastically. This leakage current is increased at every transistor generation. To lower this effect while maintaining a high performance, various proposals are introduced. Some of these proposals are promoted like SOI-FET and FinFET and others have not made it to the market. SOI and FinFETs have increased the manufacturing complexity by adding process steps and incorporating new materials.

One of the major issues of the short-channel is the drain-induced-barrier-lowering (DIBL). The barrier to carrier diffusion from the source into the channel is reduced. This uncontrollable concern at short-channel causes the drain current to increase with increasing the drain bias**.** DIBL is the source of decrease of the threshold voltage and the increase of

the subthreshold current (off-state current) of the transistor at higher drain voltages. Figure 3.1, demonstrates a short explanation of DIBL. For long-channel device (Figure 3.1.a), the drain has no effect on the electrons found in the source. In this case, only the gate controls the flow of the electrons. In the short-channel device (Figure 3.1.b), the source and the drain are placed near each other and therefore, the drain voltage contributes to the electrostatic of the device. In the short-channel device, not only the gate voltage that controls the electrons flow but also the drain voltage has a significant effect. The scientists noticed that a single gate will not be sufficient to eliminate the effect of DIBL. To improve the gate control, a supplementary gate is incorporated in several proposals. Figure 3.1.c demonstrates the concept of moving from a single gate to double gate in the short-channel device. The integration of this additional gate varied through the applications.



(a) (b) (c)

Figure 3.1: DIBL effect and the need of double gate devices, (a) long channel single gate device, (b) short-channel single gate device, (c) double gate device.

3.2 Silicon-On-Insulator Transistors (SOI)

SOI — silicon-on-insulator structure is an exciting technology primarily used to overcome SCEs. This technology has a similar geometry to the original MOSFET and

mostly has kept the silicon as the fundamental material. The idea behind SOI MOSFET is to separate or isolate the active region of the device from the underlying silicon substrate. SOI refers to placing a thin layer of silicon on top of an insulator such as SiO_2. The device is built on top of a thin layer of silicon. One of the major sources of parasitic capacitance is from the source and drain to substrate junctions. SOI reduces the capacitance at the source and the drain junctions significantly by excluding the depletion regions extending into the substrate. SOI substrate leads to a dielectric isolation of the devices to lower the influence of the parasitic effects experienced in bulk devices.

Merging SOI structure and device channel scaling of the MOSFETs has enhanced the speed of the device in addition to decreasing of I_{off}. Majumdar *et al*. show that a fully depleted SOI (FDSOI) transistors is the expected approach to bring down the technology under 22nm. They have also indicated that using back-gated, extremely thin silicon-on-insulator (ETSOI) device with thin buried oxide (BOX) will also lower the threshold voltage and allows for lower voltage operation [7].

3.3 The Road to Multi-gate Devices

Short-channel has reduced the time necessary for the electrons to cross from the source to drain and hence the faster device. The biasing of the substrate in the SOI devices creates a buried gate. The substrate acts as an additional gate and the device performs as a

vertical double gate transistor. The buried oxide prevents any leakage in the substrate leading to a better biasing. The device-to-device threshold variation in the conventional MOSFET can be limited by setting the operating area on insulator and lowering channel doping which is suitable for SOI technology.

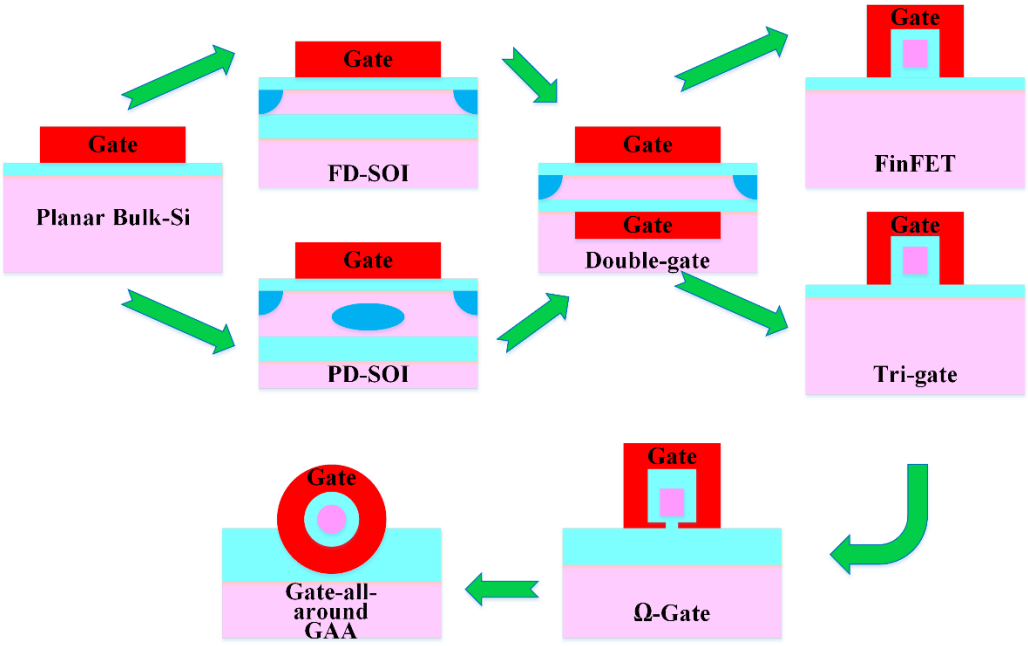


Figure 3.2: The road to the Multi-gate Transistors. Several approaches to improve gate control and device electrostatics.

A series of methods that reinforced better electrostatic or better gate control are demonstrated in Figure 3.2. In a planar device, the electrostatic is controlled by one gate. This single gate lost its potential at nano-scale channel length. SOI technique is a simple

way to overcome some of the SCE concerns. A thin oxide film is incorporated in the simplest way to improve the device electrostatically. The need for a second gate was proposed by implanting a bottom gate in the device for an easy biasing. However, the bottom gate added serious complications in the fabrication process. These complications are resolved by moving to 3D architecture (FinFET or/and Tri-gate). Moving through these proposals (Figure 3.2), various architectures to gain a better control over the channel are publicized where now a series of research is investigating the Gate-All-Around (GAA) or nanowire designs [7].

3.4 Introducing the FinFET

As the MOSFET channel length scaled down, the gate control over the channel decreases. One way to bring back a full gate control is to add another gate to help the existing gate and/or laying the device on an insulator where the body acts as a second gate. Both technologies have been confirmed to show a better performance in the extended down-scaling trend of the conventional MOSFET. However, there is still plenty of improvement required for better performance. The 3D devices are suggested to extend Moore's Law and to lower the power consumption. FinFET or Tri-gate emerge as the successors of SOI-MOSFET and the first replacement to conventional MOSFET for sub-22nm CMOS technology. The device shows the ability to support further scaling. Figure 3.2 shows the scaling history and the road to 3D devices [20].

Over the last 40 years, shorting the channel was the key to increase the performance and reduce the power consumption of the conventional MOSFET. Further scaling increases the short-channel-effect. This effect includes a significant increase of the off-state current and hence, the power consumption escalation. The FinFET comes into existence to solve the down-scaling related issues. FinFET was introduced due to its similarities to conventional MOSFET (silicon-based device). The fin shape introduces a gate voltage that surrounds the channel from three sites, and therefore, charges below the transistor are removed. This structure presents a better control over short-channel-effect. Thus, the effective switching capacitance is reduced, and the dynamic power dissipation is reduced [21]. The new structure shows a higher performance and low operating voltage. The device also shows a future scalability to continue Moore's Law. Furthermore, the device is compatible with silicon fabrication process.

FinFET has history back to 1990 when first introduced by Hisamoto *et al.* [1]. The FinFET was manufactured in 2012. Moreover, Intel's first 22nm bulk-FinFET based CMOS is currently available in the market [22]. This followed by 14nm and 10nm FinFET and currently, sub-7nm devices are in the development stage. The new structure comes in two modules SOI and bulk FinFET. The most common module is bulk-FinFET due to its manufacturing simplicity. Silicon-on-insulator (SOI) was introduced to extend the bulk-FinFET scaling for low-power applications. FinFET has merged with SOI to take

advantage of both emerging technologies. Most of the FinFET is fabricated on SOI substrate, Bulk-FinFET also was considered due its better heat dissipation and low wafer cost in addition to the simplicity of integration with today's planar CMOS design methodology and automation techniques. Meanwhile, the SOI-FinFETs have a high wafer cost and low heat dissipation.

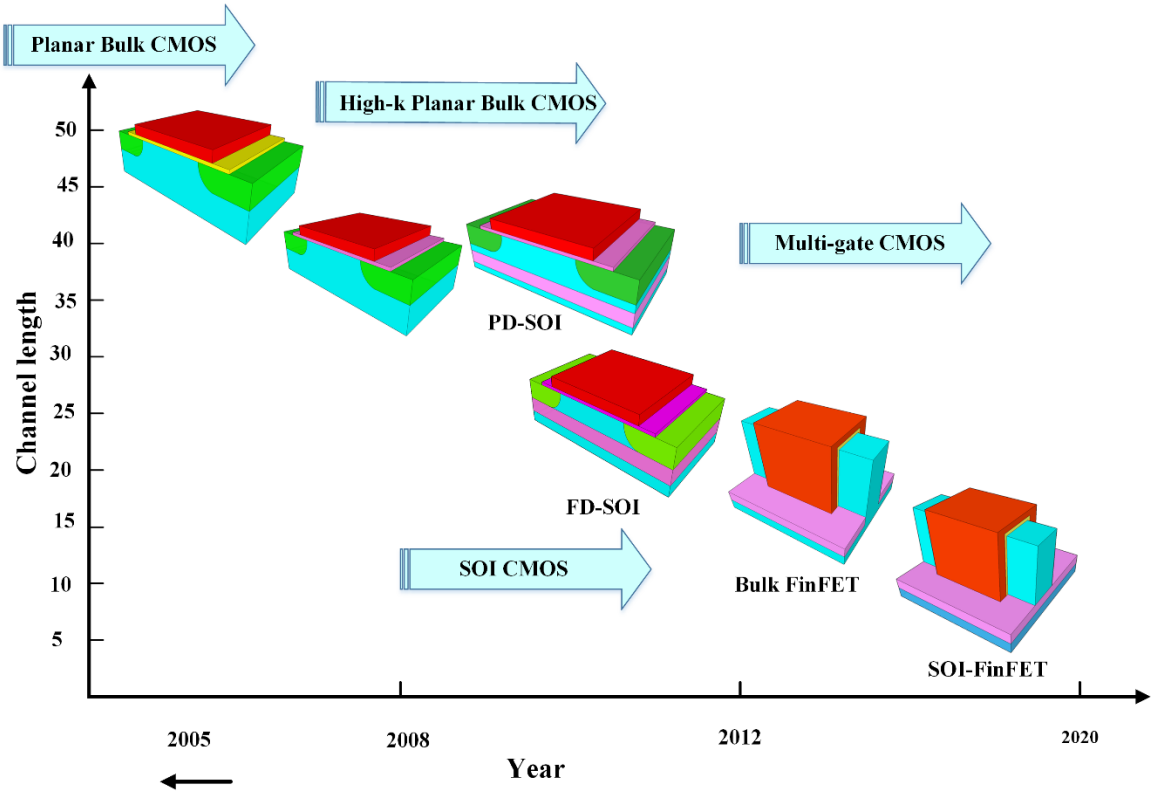


Figure 3.3: Background and motivation behind switching to 3D device.

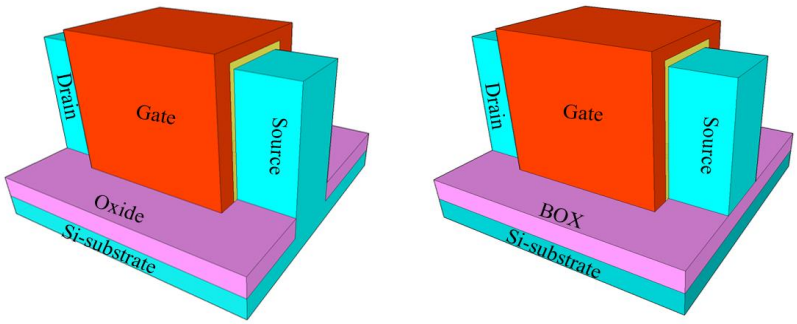
To maintain the benefits of technology scaling at the 22nm node and beyond, FinFET and (Ultra-Thin-Body) UTB-SOI show better performance. Both FinFET and UTB-SOI permit lower threshold voltage (V_{TH}), lower supply voltage (V_{DD}) and lower leakage and hence, the low-power consumption. To lower random dopant fluctuation and for better mobility, low doped or undoped body is used. Moreover, SOI-FinFET provides a speed improvement due to the elimination of the junction capacitance between the source/drain and substrate. Figure 3.3 displays the future scaling and the progress toward SOI-FinFET structures at nano-scale.

3.5 FinFET Structure Analysis

The FinFET operation is comparable to that of conventional MOSFET. The only exception here is that the on-state and off-state are controlled by the surrounding gate. The FinFET geometry has helped to increase the gate capacitance for the same oxide thickness compared to planar devices. The FinFET process is similar to that of MOSFET. The two structures of the FinFET (SOI and planar) are displayed in Figure 3.4. A cut-way view of the FinFET internal structure is shown in Figure 3.5.b and Figure 3.5.c. In this device, only the source and the drain are implanted, and then the gate is fabricated. The undoped channel eliminates Coulomb scattering due to impurities, resulting in higher mobility in FinFETs and removes excessive random dopant fluctuations RDF [23, 24]. Undoped channel FinFET is beneficial to control the issue of significant device-to-device threshold voltage

variations. In these devices, the channel is managed by the gate work function that requires a different material to serve as gate metal [20, 25, 26]. A higher I_{on} $/I_{off}$ can be achieved with a lightly doped channel as reported in [27].

Many ICs based on FinFETs technology have already been fabricated, ranging from digital logic, SRAM, DRAM to flash memory. FinFETs offer numerous advantages to be used in multiple ultra-large-scale integration (ULSI) circuits. This technology has reduced the SCEs, and leakage current, leading to a power consumption reduction. FinFET are mostly fabricated on silicon-on-insulator (SOI). SOI-FinFET works with lower supply voltage and threshold voltage less sensitive to gate length, and provides a high on-state current, lower off-state current comparable to the bulk counterpart, and lower subthreshold swing [28, 29].



(a) (b)

Figure 3.4: FinFET structures; (a) Bulk FinFET, (b) SOI FinFET.

The SOI-FinFET's ability to operate in lower supply voltage and low threshold voltage make it suitable for Low Standby Power (LSTP) Applications [30, 31]. The device also shows suppressed leakage current and superior short-channel-effects [32]. A closer view of the device is presented in Figure 3.5. The Fin width has a major impact on the performance of the device. A small W_{Si} is required for a better gate control over the channel. Hence, Small W_{Si} allows for a small subthreshold swing and less DIBL [33]. A various fin aspect ratio (AR = the fin height / the effective fin width) is studied in [34].

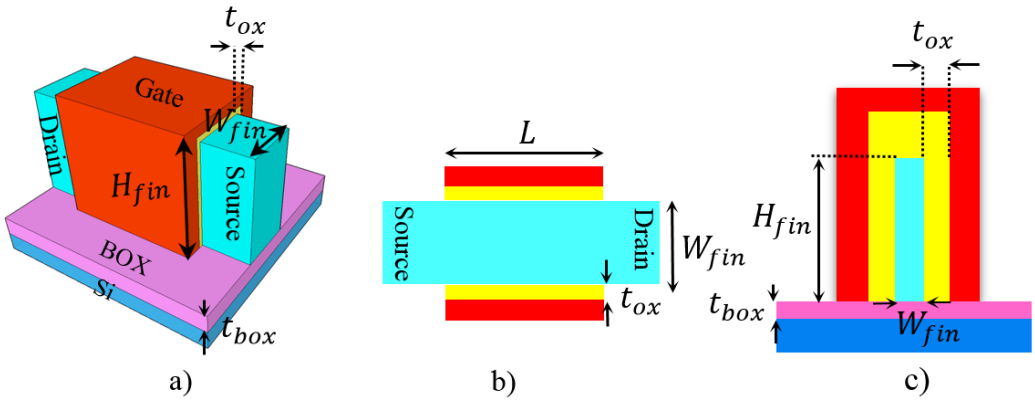


Figure 3.5: FinFET illustrations; (a) 3D schematic view of SOI FinFET, (b) Horizontal cross-section along transistor gate, (c) Vertical cross-section along transistor gate. H_{fin} and W_{fin} represent fin height and width, respectively, L is the gate length, t_{ox} is the gate oxide insulator.

SOI FinFET multi-gate structure provides a better controllability, higher SCE immunity, and substantial increase in current drive. However, this device has several

disadvantages that worth stating. Self-heating due to the SOI substrate [35, 36] and corner effect [37] due to the multi-gate configuration are two major issues of this SOI FinFET. The device performance depends on the geometrical parameters: fin width, and fin height. It is important to note that the fin aspect ratio (*AR = Fin-height/Fin-width*) is a very critical performance parameter. Therefore, neither the width nor the height should be changed independently. This geometric ratio has a significant effect on the controllability of the channel, short-channel-effects (SCE), on-current (I_{on}), buried-insulator-induced barrier lowering (BIIBL), drain-induced-barrier-lowering (DIBL) and other associated parameters.

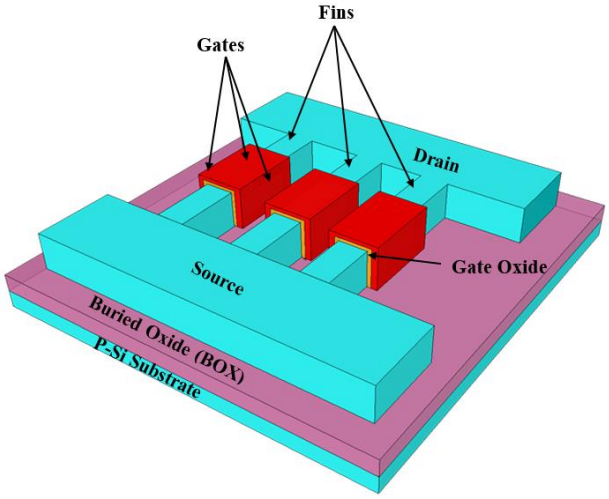


Figure 3.6: Structure SOI FinFET device with three fins

Where H_{fin} is the height of the fin and T_{fin} is the thickness of the silicon body. To obtain higher drive currents, additional fins must be applied in parallel. The total physical width of the transistor is [10]:

$$W_{total} = nW_{min} = n\times(2H_{fin} + T_{fin}) \tag{3.1}$$

This dimensional property known as width quantization allows for greater drive current realized by several discrete fins, with a single source, drain, and gate. Figure 3.6 shows the structure of the SOI FinFET device with three fins.

3.6 FinFET Advantages

To maintain the benefits of technology scaling at the 22nm node and beyond, FinFET and (Ultra-Thin-Body) UTB-SOI show better performance. Both FinFET and UTB-SOI allow for lower V_{TH} and V_{DD}. A list of some of the advantages of FinFET and UTB-SOI [38]:

- Better Swing
- S and V_{TH} less sensitive to gate length and V_{DD}
- No random dopant fluctuation
- No impurity scattering
- Less Surface scattering
- High on-current and lower leakage

- Much lower off-state current compared to the bulk counterpart.
- Lower V_{DD} and power consumption
- Further scaling and low cost

UTB is used to eliminate the leakage path. Since the silicon film is very thin, the gate can suppress the leakage efficiently. On the other side, SOI FinFET provides a speed improvement due to the elimination of the junction capacitance between the source/drain and body. FinFET also has a future in the analog circuit due to high-gain and excellent current saturation. A list of advantages and drawbacks of FinFET application in analog is presented below:

Advantages of FinFET for Analog:

- ✓ Improved frequency performance
- ✓ Reduced capacitance
- ✓ Higher drive current
- ✓ Reduction in interconnects length / reduced interconnect capacitance
- ✓ Noise and latchup are minimized through reduced substrate coupling
- ✓ Silicon resistors have improved linearity with respect to absolute voltage
- ✓ No reverse biased diodes to the substrate
- ✓ Inductor Q enhanced using very high resistivity substrates

Drawbacks of FinFET in analog applications:

- ☒ Poor thermal response due to buried oxide and trench isolation.
- ☒ Quantized widths

CHAPTER 4

TUNNELING FIELD EFFECT TRANSISTORS

The tunneling phenomenon was introduced to overcome the fundamental '*kT/q*' limitation on the subthreshold slope (S). Multiple proposals based on Band-To-Band tunneling (BTBT) which include several materials and/or structures were recommended. BTBT devices, endorsed by several scholars, are showing that the subthreshold swing can be lower than $60mV/decade$ since it is independent of the thermal voltage '*kT/q*'.

4.1 Introduction

Down-scaling of metal-oxide-semiconductor field effect transistors (MOSFETs) leads to severe short-channel-effects (SCEs) and an increase of power dissipation at large-scale integrated circuits (LSIs). The device, which is governed by the thermionic emission of carriers injected from the source to the channel region, have set a limitation of the subthreshold swing (S) of $60mV/decade$ at room temperature. Devices with S below this limit is highly desirable to reduce the power consumption and maintaining high I_{on}/I_{off} ratio. Therefore, the future of semiconductor industry relies on new architectures, new materials or even new physics to govern the flow of carriers in transistors. As the subthreshold swing is increasing at every technology node, new structures using SOI, multi-gate, nanowire approach, new channel materials such as III–V Semiconductors have

not satisfied the targeted values of this parameter. Tunneling field effect transistors (TFETs) are proposed for steeper subthreshold swing, aggressive device dimension scaling, and supply voltage reduction into *sub-0.5V*. This device approach has received much attention in research in the last decade.

4.2 Tunneling Phenomena- Esaki Tunnel Diode

Tunnel diode is a *p-n* junction where the charges can cross the barrier if the barrier is narrowed as opposed to the conventional transport where the carriers require higher energy than the barrier height. One way to lower the depletion region (thin region between *p* and *n*) is to use a highly doped *p-type* and *n-type* regions. This method increases the probability of electrons/ holes to tunnel from one region to the other. By Appling a forward bias voltage, the electrons in the conduction band of the *n-region* will tunnel to the empty states of the valence band in *p-region*. This phenomenon causes a current flow called forward bias tunnel current. A maximum current can be reached if the bias voltage increases and the electrons of the *n-region* are equal to that of the holes in the valence band of *p-region*. As the bias voltage keeps increasing, the number of electrons that able to tunnel decrease. Thus, the tunneling current decreases. The more forward voltage is applied, the lower the barrier potential becomes. In this phase, the tunneling current stops and the current flows due to the increase of electron-hole injection. In the case of reverse bias (small negative voltage), the electrons in the valence band of the *p-side* tunnel toward the empty states of the conduction band on the *n-side*. This phenomenon creates a large

tunneling current that increases significantly with slight increase of the reverse bias voltage [39].

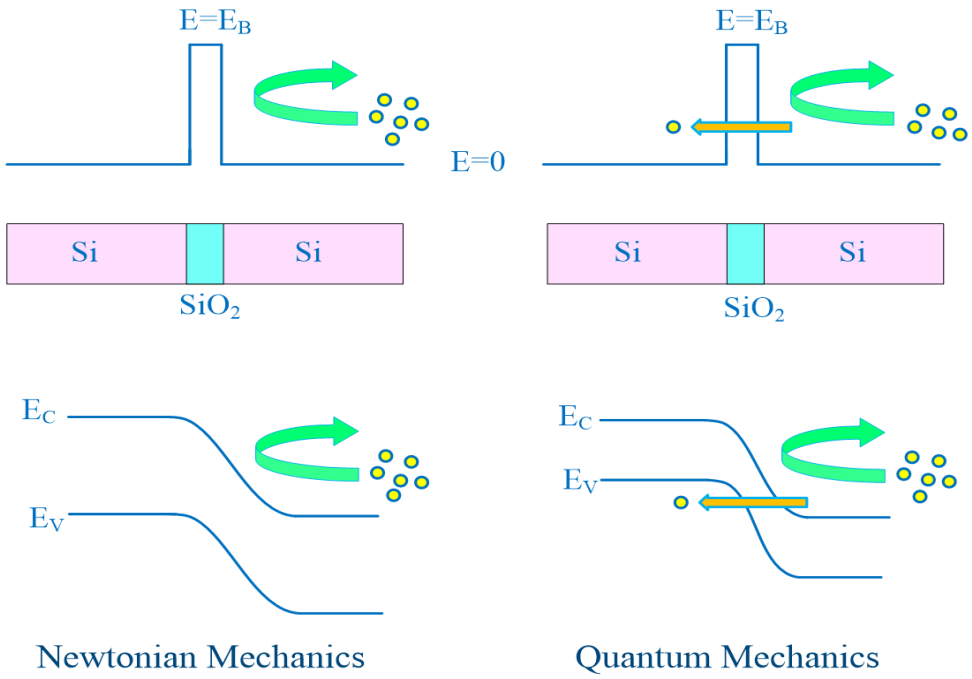


Figure 4.1: Electron Tunneling in *p-n junction* and the controversy of tunneling phenomenon in between Newtonian mechanics and quantum mechanical.

Newtonian mechanics deny the fact that particle can penetrate or "tunnel through potential well. Conversely, quantum mechanical phenomenon has acknowledged that particle can penetrate through a potential energy barrier that is higher in energy than the particle's kinetic energy. Figure 4.1 explains the phenomenon of tunneling where electrons with enough energy pass through an insulating layer [39].

4.3 Tunneling Field-effect-transistor (TFET)

Tunneling field-effect-transistor (TFET) has widely been explored in recent years as a new technological platform to go beyond the conventional MOSFET-based CMOS technologies. The tunneling phenomenon was introduced in semiconductor devices to overcome the thermal voltage limitation of conventional FETs.

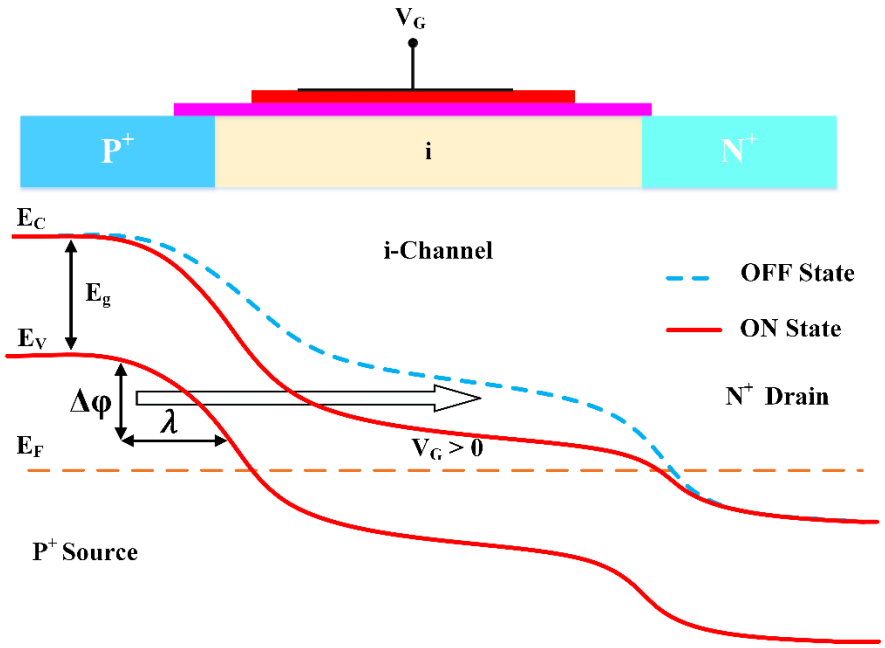


Figure 4.2: Band diagram of typical tunneling field-effect-transistor with a p^+-*doped* source side and n^+-*doped* drain side. The gate voltage controls the band bending of the *i-channel*.

The interest in having lower S is extended to several materials and structures tunnel FET. Tunnel FETs are gated diodes consisting of a p^+-*doped* source, n^+-*doped* drain, and intrinsic channel. The gate voltage controls the band bending of the channel. For a given gate voltage, if the conduction channel is above the valence band of the source the carriers cannot tunnel-cross, due to channel width that acts as a barrier. Conversely, by having the conduction channel below the valence band of the source the carrier can tunnel through generating a drain current for a given $V_{DS} > 0$ (Figure 4.2)

4.4 Various Tunneling Field Effect Transistors

Hitachi in 1988 proposed a new type of MOSFET. The device was based on Band-To-Band Tunneling (BTBT) and they called it B^2T-MOSFET. The device takes advantage of diffusion difference of $N^+ - doped$ source and $P^+ - doped$ drain, and the channel is $p - doped$ for $p - type$ devices and $n - doped$ for $n - type$ devices. This new proposal suffers from hole-trapping in $n - type$ FET. This issue causes hot-carrier-induced-degradation, where the threshold voltage decreases and the conductance increases [40]. An analytical inter-band SOI tunnel transistor shows a subthreshold below $60mV/decade$. The device geometry is shaped as a lateral p^+-n^+ tunnel junction formed in ultrathin semiconductor body. The junction is placed on top of a silicon insulator (SOI structure). The gate is placed over the *p-side* for superficial electrostatic control. The device 2-D simulation illustrate a subthreshold of about $7mV/decade$ occurs near $V_{GS} = 0.07V$. This

device also achieves an on-state current of $850\mu A/\mu m$ using a Ge channel, and low off-state current ($< 0.1\, nA/\mu m$).

To increase the on-current, Wang *et al*. proposed to use a Si_xGe_{1-x} (low bandgap material) as epitaxial tunnel layer (ETL) combining vertical tunneling orientated structure. This ETL band engineering have reduced the subthreshold swing from $47mV/decade$ to $29mV/decade$ and increases current ratio from 10^5 to 10^{10} [41]. Jeon *et al.* reported a subthreshold swing of $46mV/decade$ and a current ratio of $\sim 10^8$ in a *high-κ*/metal gate-stack and field-enhancing pocket structure TFET [42]. An experimental investigation of $70nm$ n-channel tunneling field-effect transistor (TFET) resulted in the *52.8 mV/decade* at room temperature but, the I_{on}/I_{off} ratio is significantly lower than that of the MOSFET. This research suggested to reduce the effective gate oxide thickness, increase source to channel doping peak profile, and the use of a lower bandgap channel material to improve on-state current [43].

To increase on-state current, Lee *et al.* experimentally show that strained Ge (110) *p-type* enhances BTBT current due to small band gap. Moreover, this experiment results in high I_{on}/I_{off} current ratio, and better control of leakage current without SOI substrate [44]. Another intention to increase the on-current is to use L-shaped tunnel FET (TFET). The device structure is built on BTBT perpendicular to the channel path. Post fabrication outcome indicates that for the same gate overdrive voltage, the on-current is *1000× higher*

than a conventional planar TFET owing to an improved subthreshold swing (S) and larger tunnel junction area [45]. An approach uses heterojunction-enhanced n-channel tunneling FET (HE-NTFET) achieves a steeper subthreshold swing and enhanced I_{on} [46]. Likewise, epitaxial grown Ge (epi-Ge)/Si TFET is another approach to improve I_{on} and DIBL [47]. Wang *et al.* demonstrated a superior device performance using epitaxial layer (ETL) SiGe/Si heteromaterial n-channel tunnel FET [48]. MOS gated-MIS tunnel transistor with $15.3mV/decade$ performance and on-current of $8.05 \times 10^{-3}\ \mu A/\mu m$ announced in [49]. Simulations of bilayer Tunnel FET (EHBTFET) proposed by Lattanzio *et al* [50] indicate an average subthreshold slope of $12mV/decade$ and current ratio of 10^8 at $V_D = V_G = 0.5V$.

4.4.1 Carbon nanotubes tunnel FET

A numerical simulation is presented based on gated *p-i-n* junction in [51]. The device uses carbon nanotube with a *p-doped* source side and *n-doped* drain side. The gate voltage controls the band bending of the channel. For a given gate voltage, if the conduction channel is above the valence band of the source, the carriers cannot tunnel cross due to channel width that act as barrier. Oppositely, by having the conduction channel below the valence band of the source, carrier can tunnel through generating the drain current for a given $V_{DS} > 0$. A sharp switching can be achieved which provides a subthreshold swing less than $60mV/decade$. (10, 0) CNTs that have a small band gap (1eV) provide a large

I_{on}/I_{off} ratio ($> 10^8$ at $V_{DD} = 0.4\,V$) and a subthreshold swing of $25mV/decade$. CNT-FET with $(Bi, Nd)_4Ti_3O_{12}$ (BNT) gate insulators structure was fabricated and the device properties are investigated. The device shows $62.5mV/decade$ subthreshold swing with threshold voltage of $0.45V$ and $I_{on}/I_{off} = 1.5\times10^7$ [52]. Partially Carbon Nanotube heterojunction TFET demonstrates superior subthreshold characteristics of subthreshold swing in rage of $22\sim 26mV/decade$ and I_{off} smaller than 10^4 [53]. A TFET based on *p-* and *n-doping* of the source and the drain respectively of SWNT FETs demonstrates decreased subthreshold swing down to $\sim25mV/decade$ for both *p-* and *n-channel* conduction (SWNT P-I-N FETs) [54].

Reducing the power consumption, while keeping the I_{on}/I_{off} ratio constant, is a major challenge of gate length scaling in modern technology. Logic switches with different operations were proposed to overcome the $60mV/decade$ limitations. In [55], a new concept of tunneling carbon nanotube FET was introduced. The device employed a dual-gate carbon nanotube that control the tunneling of carries between the both doped-extended drain and source. The device is based on Esaki diode with a negative gate voltage applied on the *p-portion* of the *p-n* junction. This device proposal offers the possibility of having a subthreshold slope that is far below $60mV/decade$. The BTBT probability T(E) between the source and the channel is approximated for a triangular potential using the WKB

approximation and its given as: $T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3|e|\hbar\xi}\right)$ where m^* is the effective carrier mass, E_g is the band gap, and $\xi = (E_g + \Delta\Phi)/\lambda$ is the electric field in the transition region. In $\xi = \frac{E_g+\Delta\Phi}{\lambda}$, $\lambda = \sqrt{\frac{\varepsilon_{nt}}{\varepsilon_{ox}} d_{ox} d_{nt}}$ is the screening Length, ε_{nt} and ε_{ox} are the dielectric constants of the gate oxide layer and CNT, respectively, d_{ox} is the thickness of the gate oxide and d_{nt} is the diameter of CNT. This device illustrates a subthreshold swing of $15mV/decade$.

A small effective mass, in addition to 1D electronic transportation, leads to high on-current and low subthreshold swing in CNT-based TFETs. A small band gap also increases the probability of tunneling, and on the other hand, increases the I_{off}. CNTs are suitable due to their 1D transport, small $m^*$and diameter d_{nt} and reasonable E_g. Furthermore, their integration ability with *high-κ* materials provides a small λ.

4.4.2 Graphene nanoribbon GRN

Graphene nanoribbon (GNR) is considered as a promising alternative to conventional semiconductor materials used in the IC industry because of its novel properties. Tunneling field effect transistors based on GNR have shown great rewards over other nanomaterials. Low bandgap (bandgap depending on their width), high mobility, and near- ballistic performance are some of the major advantages of the GNR. A structure of

p-channel GNR tunnel transistor is proposed by Zhang *et al.* [56]. In this structure, the source is heavily *n-doped* and the drain is heavily *p-doped*. The Zener tunneling probability is calculated by applying the WKB approximation to a triangular potential with a barrier height of E_g (bandgap) [56, 57]. The device illustrates an on-state current density of $800\mu A/\mu m$ and an off-state current of $26pA/\mu m$. The device also demonstrates an I_{on}/I_{off} ratio of more than seven orders of magnitude and a very low subthreshold swing.

4.4.3 Nanowires FET

Silicon Nanowires (SiNW) have gotten much attention as an emerging technology. Tri-gate SiGe NW TFETs was experimentally verified to show a minimum S of $30mV/decade$ in addition to providing a high on-current $I_D = 64\mu A/\mu m$ at $V_{DS} = V_{GS} - V_{off} = -1.0\,V$ [58]. In [59], a vertical gate-all-around GAA nanowire (NW) based tunneling field-effect transistor (TFET) is fabricated using a top-down compatible process technology. The TFET is operated as gated $p^+ - i - n^+$ in reverse bias mode. The device is designed such that no tunneling occurs in the off-state due to large barrier between the source and the drain. By pulling down the energy band of the channel region and reducing the width of the barrier, the carriers tunnel from the valence band to the conduction band. Henceforth, the on-state current is generated. This device delivers a high I_{on}/I_{off} ($\sim 10^5$) and subthreshold of $50mV/decade$ for about three decades of drain current and $30mV/decade$ for more than one decade of drain current.

4.4.4 Staggered heterojunctions

Gated *p-i-n* junction based on multiple geometries and materials are also considered in $sub - 60\ mV/decade$ devices. Wang *et al.* proposed a tunneling FET based on tunnel III-V staggered heterojunctions. The device used *high-κ* dielectric as gate oxide (AL_2O_3), $Al_{0.5}Ga_{0.5}\ As_{0.3}Sb_{0.7}$ as the source, $In_{0.8}Ga_{0.2}As$ as the channel, and $In_{0.8}Ga_{0.2}As$ as the drain. This device is operated at $0.3V$, provides an on-state current of $0.4mA/um$ and has an off-state current of $50nA/um$ [60].

Even though tunneling field effect transistors in many research show the possibility of having a subthreshold swing lower than $60mV/decade$ at room temperature, the devices suffer from low on-current (lower than MOSFETs). Dey *et al.* focused on the GaSb/InAs(Sb) hetero-structure that forms a broken type II band alignment. The device with *p+/n* doping profile hetero-structure was investigated and shows a maximum drive current of $310\mu A/\mu m$ at $V_{DS} = 0.5\ V$ [61].

Since silicon indicates a poor qualification in the revolutionary tunneling field effect transistors (large band gap is one of the disqualifications (1.1 eV)). New materials have been investigated and considered to bring a better outcome. Materials such as SiGe with lower band gap (~0.9 eV) show superior advantages over silicon on gated diode devices. In [62], TFET is proposed using Strained-Si/Strained-Ge lateral heterojunctions (HTFET). This combined structure has type-II band alignment and provides a small energy

barrier, allowing an enhanced tunneling at the heterointerface along with a large band gap past the interference region. The device operation is explained as follow: by applying a gate voltage the energy band overlap at the heterointerface, the electrons tunnel from the valence band of the strained Ge to the conduction band of the strained Si. The advantage of this proposal is the high tunneling rate established by short tunneling barrier at the injection region and large band gap away from that region.

CHAPTER 5

I-MOS & NW-FET TRANSISTORS

The fundamental *'kT/q'* limitation on the subthreshold slope (S) is one of the most significant challenges to the continual scaling of MOSFET devices. Impact-ionization metal-oxide-semiconductor (I-MOS) and NW-FET have recently attracted tremendous attention as a promising candidate in solid-state nanoelectronic devices.

5.1 Impact Ionization Transistors

Impact ionization is different carrier transport mechanism in transistors. High energetic charge carriers (electrons) strike a molecule causing a mobility of the electrons of that atom. The liberated electrons gain enough energy to move from valence band to the conducting band creating an electron-hole pair. The free electrons may move fast enough to knock other electrons, creating more free-electron-hole pairs generating more charge carriers. Based on this concept the ***impact-ionization metal-oxide*-semiconductor (*I-MOS*)** was designed.

I-MOS device first proposed in 2002 by *Gopalakrishnan et al.* [63]. The device attracts an extensive consideration, especially in ultra-low-power designs. The ability for this scheme to achieve a low subthreshold swing has drawn researcher's attention in the last decade. The I-MOS was design based on PiN structure and a gate partially covering the intrinsic area at the source side [64]. Figure 5.1 displays the most common structure

of this device. To reduce the influence of the drain bias on the breakdown voltage and to improve the short-channel-effect, the drain extension in this design is lightly doped. As pointed out in various section of this research, the thermal limitation *"KT/q"* or ($60mV/\,decade$ at room temperature) is the bottom limit of the subthreshold swing that can be achieved by the conventional MOSFET in the ideal conditions. I-MOS was proposed to solve some of the scaling concerns (mainly short-channel-effect). This device simulation also shows very high $I_{on}/I_{off,}$ low off-state leakage, and a subthreshold swing that is much lower than the previously publicized subthreshold swing [63, 64].

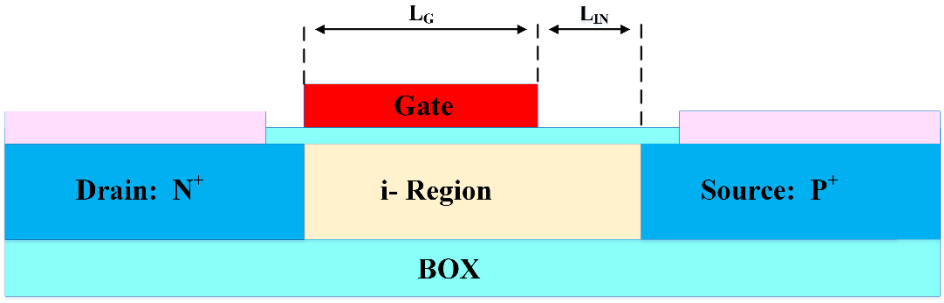


Figure 5.1: The basic structure of Lateral I-MOS.

A major drawback of the I-MOS is the requirement of a large source bias V_S. Few adjustments based on the same concept to overcome this issue are proposed in [65]. However, I-MOS suffers from reliability and threshold voltage stability in addition to integration difficulties to existing CMOS technology (fabrication process). To accomplish a subthreshold swing better than *"KT/q"* and maintain a lower supply voltage, different I-MOS structures are introduced. The L-shaped I-MOS (LI-MOS) is projected to overcome the previously discussed issues of the I-MOS [66]. This proposal achieves a subthreshold

swing below $5mV/decade$. Lateral I-MOS generally requires a high supply voltage for breakdown to occur, this result in hot carrier degradation effects, and damage of the gate oxide. This effect causes a short life of the I-MOS devices [67]. The Vertical I-MOS is attended to overcome the previous listed disadvantages of lateral I-MOS. Typical vertical I-MOS structure is shown in Figure 5.2. Vertical I-MOS is not based on the avalanche breakdown as the first proposed lateral I-MOS. As an alternative, holes are generated by impact ionization that charges the floating *p-type* body to result in lower threshold voltage. This causes a rapid increase of drain current in the subthreshold region [67, 68, 69].

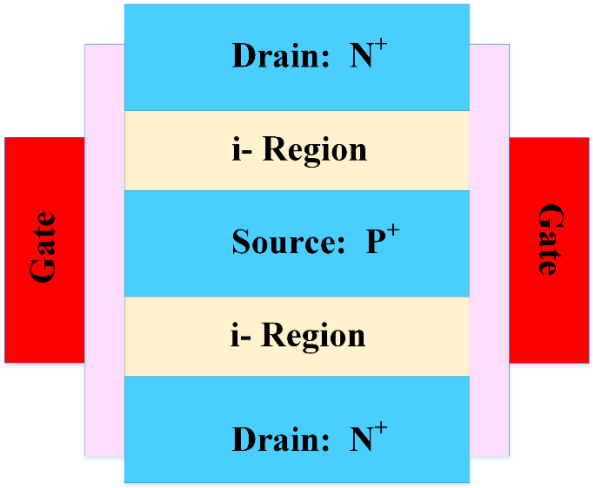


Figure 5.2: Vertical I-MOS structure

I-MOS devices, in general, have the potential to offer a steeper swing at room temperature since S is independent of the thermal voltage '*KT/q*' in such device [70]. The

Structure of L-shaped Impact-ionization MOS (LI-MOS) transistor proposed in [71] demonstrates a subthreshold swing of $4.5mV/decade$ at room temperature. Some novel transistor structures like enhanced electric-field impact-ionization MOS proposed in [72, 73] are publicized a $5mV/decade$ subthreshold swing. Recently, Kumar *et al.* [74] report Bipolar I-MOS exhibiting $6.25mV/decade$. Recent results have shown a sub-threshold slope that fell to $2mV/decade$ [75].

5.2 Nanowire Transistors

Maintain process simplicity and manufacturing cost to a minimum, another design approach that requires the use of different materials has recently drawn tremendous attention as a promising candidate in solid-state nanoelectronic devices. To lower leakage, while maintaining a high performance, various schemes were introduced. Nanowire (NW-FET) and Tri-gated field-effect-transistor are one of the existing proposals to overcome the issues of scalability (typical nanowire structure on SOI is shown in Figure 5.3). NW-FET architecture provides a better gate control over the channel.

A device that combines nanowire architecture and tunneling carrier transport is expected to break the thermal limits of the subthreshold swing. This methodology has some limitations of low on-state current, and the steepest switching slope is not sustained across the whole turn-on curve [66, 76]. This device report $13mV/decade$ and an on-state current $I_{on} = 4.5mA/um$ at $V_{DD} = 0.4V$. This scheme exploits InGaAs-InALAs pair placed in

between the source and the channel. The area between the source and the channel of NW-FET is divided by an interposing a superlattice (SL). A *p-channel* I-MOS transistor featuring Silicon Nano-Wire reports a $Sub - 5\ mV/decade$ Subthreshold Swing in [77].

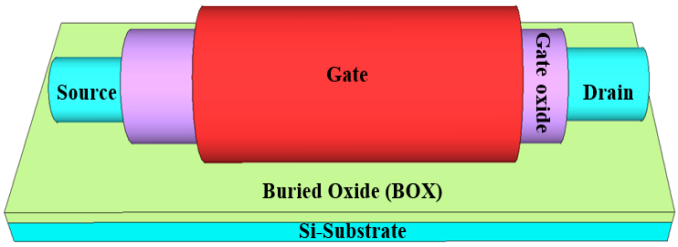


Figure 5.3: Typical nanowire MOSFET structure: the gate is surrounding the channel creating a better electrostatic control.

With the down-scaling issues of the MOSFET's devices, NWFET is of great interest in 10nm and beyond technology node [78]. These types of devices have shown tremendous electrical properties, energy efficiency, and improved performance. NWFET offers better electrostatic over the channel, thus a reduced short-channel-effect and lower subthreshold leakage current. Nanowire MOSFET, driven by Body-Bias Effect, reports a small subthreshold Effect. The device is fabricated on silicon-on-insulator (SOI) wafer with a nanowire channel and triple-gate structure. This structure allows high current controllability and large on/off current ratio. The device offers a subthreshold swing of $6.6mV/decade$ for *n-type* and $5.2mV/decade$ for *p-type* in the range of current of six

orders of magnitude. In [79], I-MOS transistor is designed using nanowire gate-all-around (GAA) architecture that gives a $sub - 5mV/decade$ at room temperature. The Vertical Si-Nanowire TFET proposed in [59] demonstrates a subthreshold swing of $30\,mV/decade$. Q. Li *et al.* report a Si-NWFET with subthreshold swing of $85mV/decade$ and a current ratio of 10^6 [80]. A technique of boosting the performance of NW-MOSFET impact-ionization-induced subthreshold kink is proposed by Chen *et al.* in [78]. Physical modeling and numerical simulation of this device demonstrate a steep switching. A comparison between standard impact ionization MG-MOS and a junctionless nanowire silicon transistor is presented in [81]. This research determines that junctionless MOSFET on germanium has the potential of steep subthreshold swing. Jeon *et al.* [82] present P^+-*i*-N^+ Si-nanowire with steep subthreshold swing characteristics. The device shows I_{on}/I_{off} current ratio of 10^6 and a $S \approx 18mV/decade$ in the *n-channel* device and a $10mV/decade$ in the *p-channel* device.

The topic of $sub - 60mV/decade$ or steep slope devices has been growing in the last decade. Several materials as well as different physics are proposed for this post-silicon integration. Nano-electronics based on nanowires and nanotubes is a promising alternative solution to break the scaling limit that silicon industry is facing. However, those architectures, and previously cited physics are still facing serious challenges in both IC integration and reliability. To maintain process simplicity and manufacturing cost to

minimum, other design approach that requires the use of different material have recently drawn tremendous attention as a promising candidate in solid-state nanoelectronic devices.

CHAPTER 6

FERROELECTRIC BASED FIELD EFFECT TRANSISTORS

Beyond Si electronic materials like ferroelectric material based FETs are in the developing stage to become the core technology for non-classical CMOS structures. This chapter presents a review of a new approach to $sub-60mV/decade$ design based on negative capacitance concept.

6.1 Introduction

To keep Silicon technology as the base technology while modernizing future devices where cost is an important factor, advance research has introduced multiple substitutions to the existing planar MOSFET. Scientists and engineers are investigating new physics, new materials as well as new device structures that can lead to steep subthreshold swings less than $60mV/decade$. The currently marketed FinFET has shown a better performance compared to the conventional MOSFET. This device has geometrical improvements that allow a better channel control. In previous chapters, we have introduced several motivations of research that proposes to use different materials. Materials like III-V staggered hetrojunctions, Carbon Nanotube, and Graphene shows superior performance. In chapter 4 and 6, alternative physics is explored. Band-To-Band tunneling has been introduced for high performance and low-power consumption. For the continuation of current technology and a smooth transition to new design platform, near-

future devices must be compatible with conventional MOSFET and CMOS manufacturing processes. It would be very useful if a lower value of S can be obtained in conventional FET or in a compatible device with some form of material and/or geometric modification of MOSFET until the complex fabrication processes involving emerging device technologies are well-understood and pioneered. Therefore, Si-FET based technology will remain as the foundation of micro-/nano-electronics for several more decades. This chapter presents new and different propositions to reduce subthreshold swing. These proposals require integrating ferroelectric materials to operate in negative region (negative capacitance) into the MOSFET basic structure.

6.2 Negative Capacitance Concept

Many contemporary scientists and engineers believe that negative capacitance is the answer to many problems in nanoelectronics [16, 83]. The NC effect, which implies that the voltage of the capacitor decreases as the charge is added, can be provided by the ferroelectric capacitor that arises from an internal positive feedback [15, 84].

For convenience, the definition for the subthreshold slope, which was previously presented, is repeated here:

$$S^{-1} = \frac{\partial \log I_D}{\partial V_G} = \frac{1}{2.3(k_B T/q)} \frac{\partial \psi_S}{\partial V_G} \tag{6.1}$$

And the subthreshold swing is defined as:

$$S = \frac{\partial V_G}{\partial (\log I_D)} = \frac{\partial V_G}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log I_D)} = \left(\frac{k_B T}{q}\right)\left(\frac{\partial V_G}{\partial \psi_s}\right) \times \ln(10) \tag{6.2}$$

Where $\frac{\partial V_G}{\partial \psi_s}$ called the body factor and titled η.

V_G is related to ψ_S by a capacitive voltage divider shown in Figure 6.1. 'S' could be expressed as:

$$S = \ln(10)\frac{kT}{q}\left(1 + \frac{C_S}{C_{INS}}\right) \tag{6.3}$$

Considering the coupling capacitance between the gate voltage and the bulk to evaluate S. Figure 6.1 illustrates the capacitance involved in the approximation. For a short-channel modeling, the analytical solution that uses voltage-doping transformation (VDT) is considered. This estimation also considered linearly varying potential LVP approximation to obtain the swing voltage [85, 86]. The body-factor of Si-bulk MOSFET can be approximated as in (6.4):

$$\eta = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{INS}} \tag{6.4}$$

ψ_s Semiconductor surface potential, η Body factor, C_s Semiconductor capacitance, and C_{INS} Gate insulator capacitance. If $0 < \eta < 1$ then $C_s/C_{INS} < 0$, therefor, $C_{INS} < 0$ a negative capacitance is needed to achieve a subthreshold swing lower than $S < 60mV/\,decade$. For device stability, the overall capacitance must remain positive as well as to keep similar transistor operation where the Negative capacitance acts as an amplifier stimulator.

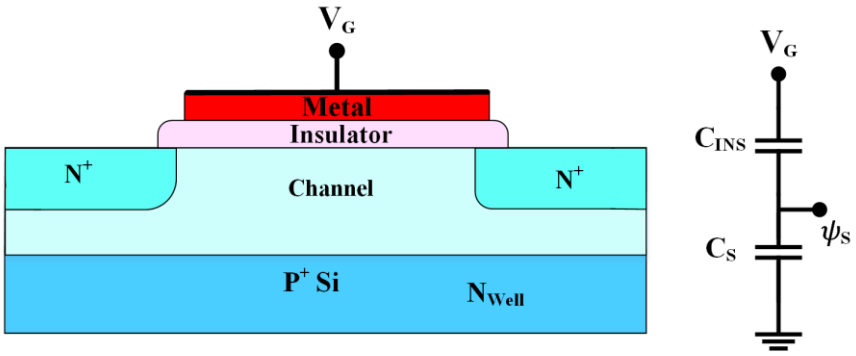


Figure 6.1: Si-Bulk MOSFET and its equivalent capacitance coupling

6.3 Ferroelectric Material Properties

Ferroelectric material proprieties have been deeply studied in the last 10 years. This interest has been driven by the exciting possibility of using ferroelectric thin film in a gate-stack MOSFET. The hysteresis proprieties made it possible for Ferroelectric Random Access Memory or Fe-RAM to be present in commercial products. Figure 6.2 explains the hysteresis proprieties and the charges loading of certain ferroelectric materials. Unlike linear and paraelectric capacitors, the charges on a ferroelectric capacitor does not go back to zero at $0V$. Some of the charges inside the capacitor will be tripped (cannot come out), and yet it still has zero volts on it. The reason is that the ferroelectric material between the plates of the capacitor has a naturally occurring built-in electric field. That electric field pulls in from the circuit just the right amount of excess charge of the opposite polarity to cancel itself on the surface of each plate [87].

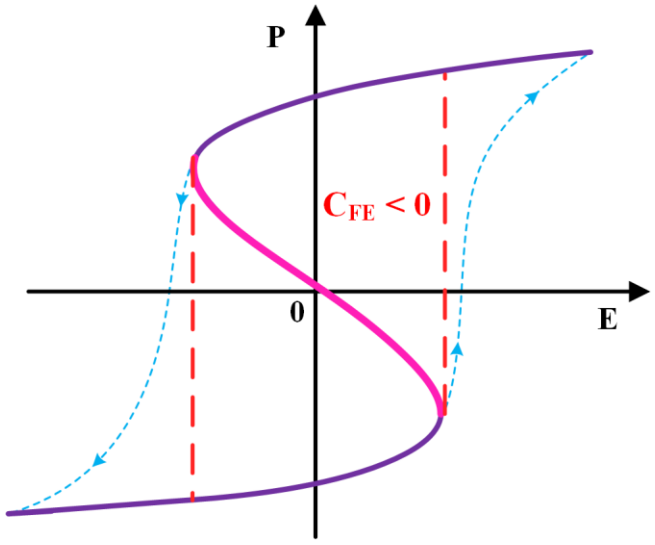


Figure 6.2: P-E curve (polarization versus electric field curve) showing negative slope which can lead to the negative capacitance (negative permittivity).

6.4 Negative Capacitance

Ferroelectric materials introduce a new hypothesis of negative capacitance. The concept was observed by Ershov in 1998 [88], reinstated by Salahuddin and Datta 10 years later. In 2011, I. Khan *et al.* have presented an evidence of ferroelectric negative capacitance in nanoscale heterostructures. Negative capacitance refers to the power boost provided by capacitor made with a ferroelectric material paired with a dielectric (electrical insulator) [16]. Integrating ferroelectric material into current MOSFET architecture will reserve the same field-effect-transistor operations, as well as the compatibility with CMOS existing fabrication technology.

Many experiments have been performed to explore the effects of negative capacitance. Gao *et al*. have demonstrated negative capacitance in a ferroelectric− dielectric superlattice heterostructure at room temperature [89]. Negative capacitance is exhibited in a thin single-crystalline ferroelectric film publicized by A. Khan *et al.* [90] and in organic/ferroelectric materials publicized by Jo *et al.* in [91]. The combination of the ferroelectric $BaTiO_3$ in series with the paraelectric $SrTiO_3$ at room temperature leads to negative capacitance in a device, which was experimentally demonstrated by Appleby *et al.* in [92].

6.5 Subthreshold Slope Lower than 60mV/decade

Nowadays, much research has been conducted to explore the ferroelectric material as a source of negative capacitance. This section offers a literature review of several devices using negative capacitance concept. The core idea is to integrate a ferroelectric layer into a MOSFET physical structure to lower its subthreshold slope. Salahuddin *et al*. showed that a ferroelectric insulator of correct thickness will amplify the gate voltage, leading to values of subthreshold lower than $60mV/decade$. This idea was based on integrating a negative capacitance provided by the ferroelectric material with no change in the basic transistor operation. Their objective is to reduce the body factor η ($\frac{\partial V_g}{\partial \psi_s} < 1$), which is different from other proposals that assumes that η cannot be changed, hence, intending an alter transistor operation principals. Furthermore, Khan *et al*. proposed a gate-stack of metal-ferroelectric that provides a new mechanism to set-up the semiconductor

surface potential ψ_s above the gate voltage. The capacitive voltage divider formed by C_{FE} will provide a new and stable operation region of the FET [83].

6.5.1 Non-hysteretic negative capacitance FET

Non-Hysteretic negative capacitance was proposed to decrease subthreshold swing. The proposed device in [85] shows that a $30mV/decade$ can be reached. The device structure is shown in Figure 6.3, the bottom layer (N_{well}) is heavily doped *p-type* to determinate the depletion region and to cutoff the subthreshold leakage path. The channel is a thin semiconductor on conductor (TSOC). A ferroelectric (FE) film is deposited over a metal/*high-κ* dielectric stack. Metal-Ferroelectric gate-stack FET (considered as voltage amplifier) is proposed in [16, 85]. The subthreshold swing is reduced by a factor β ($\beta = \Delta V_{MOS}/\Delta V_G$). β is derived from the capacitive voltage divider model shown in Figure 6.3.

$$\Delta V_{MOS} = \Delta V_G * C_{FE}/(C_{FE} + C_{MOS}) \tag{6.5}$$

Where: C_{MOS} is the series combination of C_{ox} and C_{DEP}.

$$\Delta V_{MOS} = \Delta V_G * |C_{FE}|/(|C_{FE}| - C_{MOS}) \tag{6.6}$$

To have a large β the denominator must be very small:

$$|C_{FE}| - C_{MOS} \approx 0 \ \rightarrow |C_{FE}| \approx C_{MOS} \tag{6.7}$$

Conversely, C_{MOS} is not constant through the variation of V_G causing unstable device, and $|C_{FE}|$ required to be larger than C_{MOS}. To achieve that condition, a thin semiconductor on conductor (TSOC) of thickness T_{TSOC} was incorporated to make C_{DEP} larger and insensitive to gate bias. Consequently, a smaller subthreshold swing can be succeeded [85].

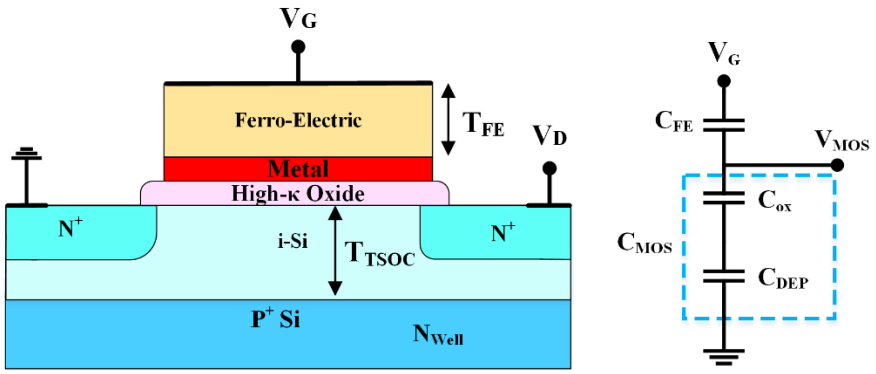


Figure 6.3: Cross section and the capacitance representation of NCFET [85].

6.5.2 Fe-FET with P(VDF-TrFE)/SiO_2 gate-stack

Salvatore *et al.* research demonstrates experimentally that a $13mV/decade$ in Fe-FETs with 40nm P(VDF-TrFE)/SiO_2 could be achieved at room temperature by incorporating a thin ferroelectric layer (negative capacitance) into a gate stack. The negative ferroelectric capacitance is integrated to lower the η-factor by providing voltage amplification. The added layer introduces a positive feedback that increases the polarization. A positive oxide capacitance is also included in series with the negative

capacitance to resolve the stability concerns [86]. The device was designed to place a 40nm P(VDF-TrFE) on top of 10nm SiO_2 gate stack. The charges obtained by the positive feedback can be described as:

$$Q = C_{gate}(V_G + \alpha_F Q) \tag{6.8}$$

The η -factor becomes:

$$\eta(V_G) = 1 - \frac{C_S}{C_{ins-eq}(V_G)}\left(\alpha_F C_{ins-eq}(V_G) - 1\right) \tag{6.9}$$

Where: $1/C_{ins-eq} = 1/C_{ox} + 1/C_{ins-eq}(V_G)$, For $\alpha_F C_{ins} > 1$ the η-factor is smaller than 1.

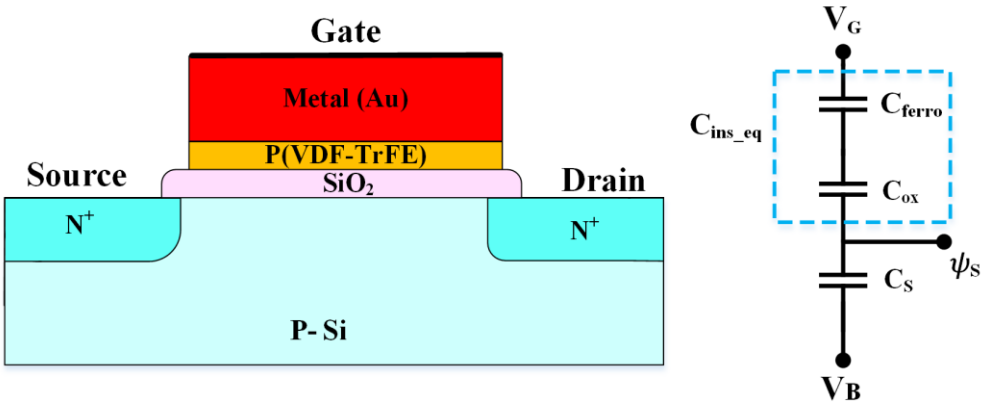


Figure 6.4: Fe-FET and equivalent capacitive divider [86].

Different approaches and studies publicize that the ferroelectric negative capacitance is merged into the MOSFET existing design. One of these designs is the double-gated ferroelectric MOSFET shown in Figure 6.5 [93]. This idea is similar to the

one discussed above except that a double-gate device leads to a better channel control, and hence, improved performance. In [94], a different gate stack is introduced to break the $60\ mV/decade$ limitation. This structure has a *Metal-Ferroelectric-Metal-Oxide-Semiconducto*r gate stack. This gate arrangement as mentioned earlier has a subthreshold swing of $46mV/\ decade$.

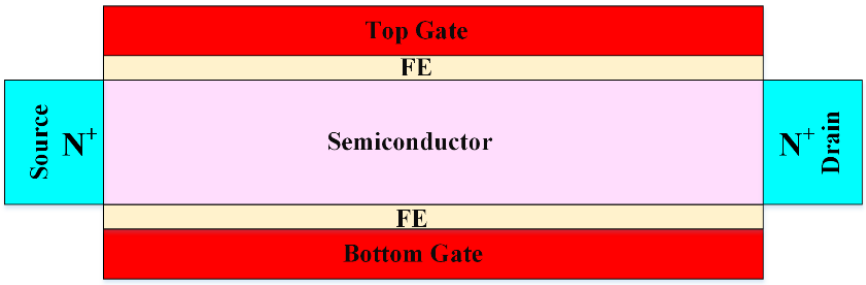


Figure 6.5: A Cross-sectional view of a double-gate negative capacitance FET [93].

Many contemporary researchers believe that negative capacitance will be the answer to many of the problems in nanoelectronics [15, 95]. DasGupta *et al* has demonstrated experimentally that a subthreshold swing of $13mV/decade$ at room temperature can be achieved in a MOSFET with $PbZr_{0.52}Ti_{0.48}O_3$ gate insulator and HfO_2 as a buffer interlayer [96]. The approach of attaining $sub-60mV/decade$ subthreshold swing by introducing a negative capacitance in the gate-stack, which keeps the same carrier as the conventional MOSFET, is extended beyond hysteresis in ferroelectric materials to

antiferroelectric and nonhysteretic materials. These materials have shown to extract a negative capacitance in the MOSFET gate stack structure [83]. Other non-silicon based devices are still at the theoretical level and far away from realization [4]. However, it is important to note that the abrupt move to a new technology platform (away from MOSFET) is not feasible for the industry in near future.

CHAPTER 7

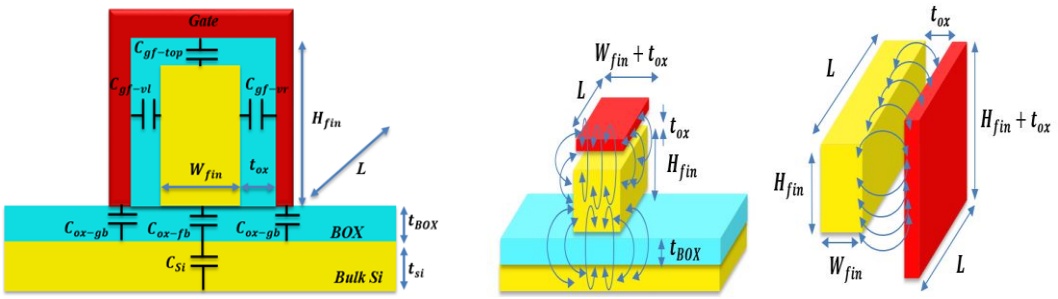
AN ANALYTICAL MODEL TO APPROXIMATE THE SUBTHRESHOLD SWING FOR SOI-FINFET

CMOS tradition of scaling, which includes reducing devices' dimension and power consumption, is sustained by introducing new geometries and new materials. This sequence of further shrinking has moved the technology from planar to 3D structure. Several device geometries are proposed to reduce the off-state leakage and extend Moore's Law. FinFETs have been proposed due to their process similarities with existing technology and their immunity to short-channel-effect (SCE). The 3D or Tri-gate shows a promising future for further scaling. This chapter presents a closed form model of the SOI Tri-gate device internal capacitance and an optimization method to reduce the subthreshold swing and drain-induced barrier lowering (DIBL).

7.1 Introduction

Because cost is an important factor, it is important to keep Silicon technology as the base technology while modernizing future devices. To achieve this, Tri-gate, known as FinFET, was introduced due to its similarities to conventional MOSFET. The fin shape introduces a gate voltage that surrounds the channel from three sites presenting a better control over the short channel. The new structure also shows a higher I_{on}/I_{off} ratio as compared to the conventional MOSFET. FinFETs present a better performance, lower

leakage current, and fabrication compatibility with CMOS process [97]. Various device characteristics like the drive current (I_{on}), the subthreshold swing (S), and the buried-insulator-induced barrier lowering (BIIBL) depend on the *high-aspect-ration* of the "fin" structure. This parameter presents a significant challenge for process control and design flexibility [98, 99]. The gate geometry plays a decisive key that controls the performance of the FinFETs. Fin-width is an important design parameter, which requires being around half the channel length. Simulations by Konishi and Omura show that DIBL and subthreshold swing escalate when the fin aspect ratio (*AR = fin-height / fin-width*) goes below 1.5. They also show that this ratio controls the on-current of the device along with the SCEs [99]. The vertical architectures of the device make it very compact compared to conventional MOSFET. FinFET design parameters are shown in Figure 7.1.



(a) (b)

Figure 7.1: a) SOI-FinFET cross section and intrinsic capacitances. H_{fin} is the fin height, W_{fin} is the channel width, t_{BOX} is the buried oxide thickness, L is the channel length, and t_{ox} is the gate channel insulator thickness, b) Formation of the components of the total capacitance of the fin (channel) of *SOI-FinFET*. Here $C_{gf-vl} = C_{gf-vr}$.

This chapter presents a theoretical analysis to approximate the subthreshold swing of SOI-FinFET. This approximation is based on coupling capacitance of the device; it doesn't count for the doping attenuation of the channel, which is undoped or slightly doped. As we deal with different structure, multiple coupling capacitances will be considered. The fin shape introduces a gate voltage that surrounds the channel from three sites. The gate will form a coupling capacitance not just through the fin formed channel, but through the silicon dioxide on both sides of the fin (Figure 7.1).

7.2 SOI FinFET Subthreshold Swing

7.2.1 Model approach

Studying subthreshold swing is an important aspect of controlling on-state current and off-state current. The subthreshold swing (S) has increased by down-scaling trend at every technology node. There are multiple ways to lower S, for example, engineering the design parameters like substrate thickness, buried oxide film thickness, fin height, and the fin width. Figure 7.1 illustrates various capacitances that are created between different materials. Capacitance is formed every time two conductors/semiconductors are placed closely separated by an insulating material or a depleted layer. The next section, presents an approximated calculation of these capacitances.

7.2.2 SOI FinFET capacitance calculations

Capacitance is present whenever two conductors are placed closely separated by an insulating material. Using Yang formula, an approximation of the capacitance of two square plates shown in Figure 7.2 is intended. The total capacitance per unit length that includes fringing can be written as [100, 101]:

$$C = \varepsilon \frac{w}{h}\left[1 + \frac{2h}{\pi w}\ln\left(\frac{\pi w}{h}\right) + \frac{2h}{\pi w}\ln\left(1 + \frac{2t}{h} + 2\sqrt{\frac{t}{h} + \frac{t^2}{h^2}}\right)\right] \quad (7.1)$$

Where: $2h$ is the distance between the two plates, W and t are the length and the width of the top plate respectively.

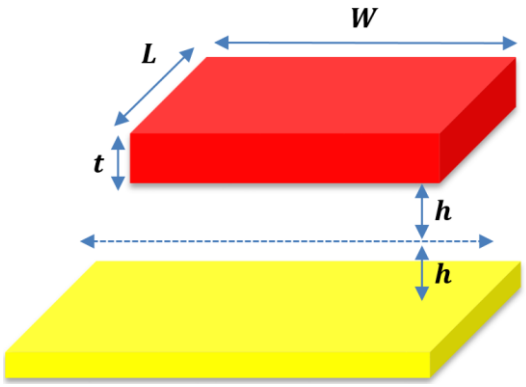


Figure 7.2: A capacitor is formed from two conducting plates separated by a thin insulating layer.

From Figure 7.1, the total gate-channel capacitance can be written as:

$$C_{gf} = C_{gf-top} + C_{gf-vl} + C_{gf-vr} \quad (7.2)$$

Where: C_{gf-top} C_{gf-vl}, and C_{gf-vr} represent the capacitances of the top plate (capacitance created between the top gate and the channel), vertical left, and vertical right capacitance created between the vertical gates and channel respectively. For uniform dispersed gate-shape, both capacitance C_{gf-vl} and C_{gf-vr} are assumed to be equal. Using Yang formula, an approximation of the capacitance formed by the bridge-shape gate and the channel can be obtainable [100, 101].

$$C_{gf-vl} = \varepsilon_{ox}\frac{2H_{fin}}{t_{ox}}L\left[1 + \frac{t_{ox}}{\pi H_{fin}}\ln\left(\frac{2\pi H_{fin}}{t_{ox}}\right) + \frac{t_{ox}}{\pi H_{fin}}\ln\left(1 + \frac{2W_{fin}}{t_{ox}} + 2\sqrt{\frac{2W_{fin}}{t_{ox}} + \frac{4W_{fin}{}^2}{t_{ox}{}^2}}\right)\right] \quad (7.3)$$

Similarly:

C_{ox-top} and C_{ox-fb} are the front and back oxide capacitances and can be written as;

$$C_{gf-top} = \varepsilon_{ox}\frac{2W_{fin}}{t_{ox}}L\left[1 + \frac{t_{ox}}{\pi W_{fin}}\ln\left(\frac{2\pi W_{fin}}{t_{ox}}\right) + \frac{t_{ox}}{\pi W_{fin}}\ln\left(1 + \frac{4(H_{fin} - t_{ox})}{t_{ox}} + 2\sqrt{\frac{2H_{fin}}{t_{ox}} + \frac{4H_{fin}{}^2}{t_{ox}{}^2}}\right)\right] \quad (7.4)$$

$$C_{ox-fb} = \varepsilon_{ox}\frac{2W_{fin}}{t_{BOX}}L\left[1 + \frac{t_{BOX}}{\pi W_{Si}}ln\left(\frac{2\pi W_{fin}}{t_{BOX}}\right) + \frac{t_{BOX}}{\pi W_{fin}}ln\left(1 + \frac{4\left(H_{fin} - t_{ox}\right)}{t_{BOX}} + 2\sqrt{\frac{2H_{fin}}{t_{BOX}} + \frac{4{H_{fin}}^2}{{t_{BOX}}^2}}\right)\right] \quad (7.5)$$

$$\mathrm{C_{gf}} = \mathrm{C_{gf-top}} + \mathrm{C_{gf-vl}} + \mathrm{C_{gf-vr}} \quad (7.6)$$

$$\mathrm{C_{ox}} = 2\mathrm{C_{ox-gb}} + \mathrm{C_{ox-fb}} \quad (7.7)$$

7.2.3 SOI FinFET Established Capacitive Network and Subthreshold Swing Calculation.

To estimate the subthreshold swing, we have considered the coupling capacitance between the gate voltage and the bulk Figure 7.1 shows the capacitance involved in this approximation. For short-channel modeling, we have intended an analytical solution that uses voltage-doping transformation **(**VDT**)** [102]. In this study, we have also considered a linearly varying potential (LVP) approximation to obtain the swing voltage [103, 104].

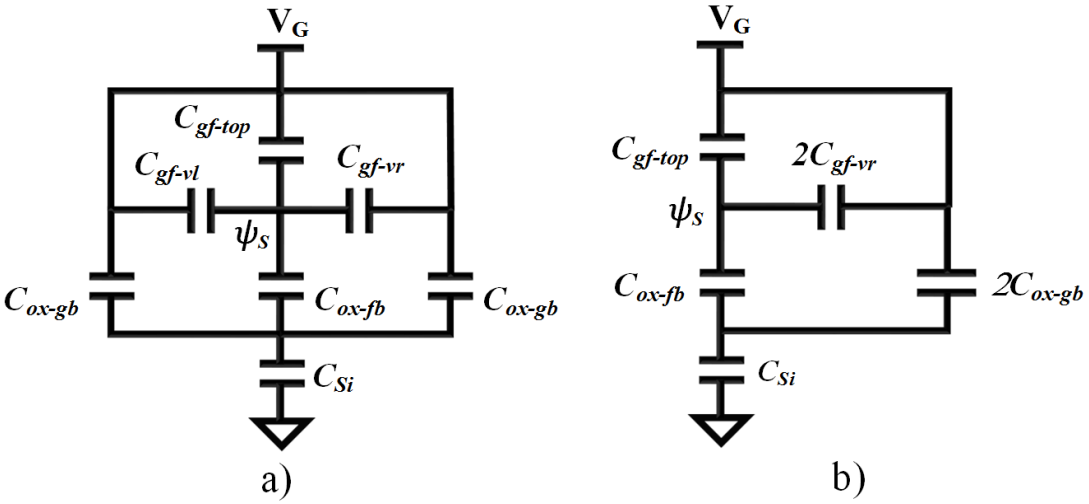


Figure 7.3: SOI FinFET's approached intrinsic capacitive network a) Equivalent capacitive model of SOI FinFET b) Simplification of an equivalent capacitive model of SOI FinFET.

Figure 7.3.a illustrates the approached capacitive network of SOI-FinFET, where the Figure 7.3.b shows a capacitive simplification of the capacitive network. The body-factor η (see Appendix A for detail calculations) can be evaluated as:

$$\eta = 1 + \frac{C_{ox-fb} \times C_{Si}}{\left(C_{gf-top} + 2 \times C_{gf-vr}\right) \times \left(C_{ox-fb} + C_{Si} + 2C_{ox-gb}\right) + 2 \times C_{ox-fb} \times C_{ox-gb}} \tag{7.8}$$

$$\eta = 1 + \frac{C_{ox-fb} \times C_{Si}}{C_{gf} \times (C_{ox} + C_{Si}) + C_{ox-fb}(C_{ox} - C_{ox-fb})} \tag{7.9}$$

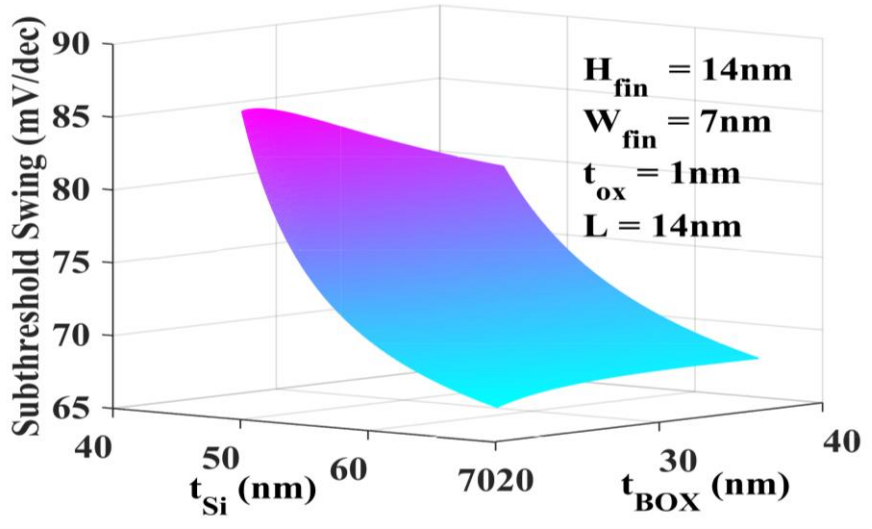
Where C_{gf} is the total gate-channel capacitance, C_{ox-fb} is the capacitance formed between the conducting channel and the silicon substrate, C_{ox} represents the total capacitance

created between the working area of the device and the silicon substrate, C_{Si} is the silicon film capacitance ($= \frac{\varepsilon_{Si}}{t_{Si}}$, ε_{Si} being the silicon permittivity and t_{Si} is silicon film thickness), and C_{BOX} is the oxide film capacitance ($= \frac{\varepsilon_{ox}}{t_{BOX}}$, ε_{ox} being the oxide permittivity and t_{BOX} the oxide film thickness). The resulting model for the body-factor (η) of the SOI-FinFET is given in (7.9). For brevity, the derivation is omitted. The detailed steps of deriving the model for the body factor are shown in Appendix A. The model presented in (7.8) can be simplified as in (7.9) by the replacements using (7.6) and (7.7). Therefore, the body factor (η) of the SOI-FinFET can be estimated by either (7.8) or (7.9). Using the derived η (expression (7.8) or (7.9)), the subthreshold swing of SOI-FinFET can be calculated. Due to the unique arrangement and the relative dimensions of the intrinsic components of SOI-FinFET, the device offers near-ideal coupling that ensures a value of η close to unity. However, subthreshold swing depends on several parameters, such as buried oxide thickness (t_{BOX}), channel dimensions (fin-height, fin-width and channel-length), gate oxide thickness (t_{ox}), and the silicon bulk thickness (t_{si}).

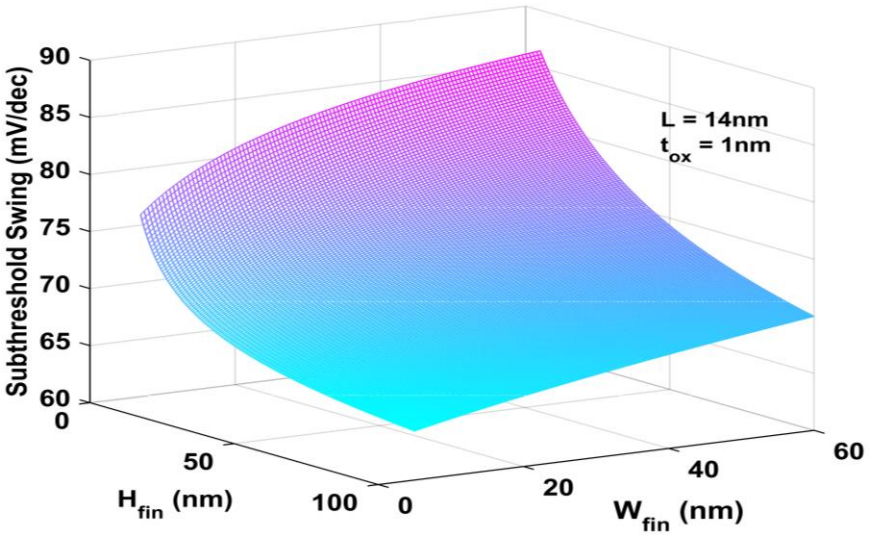
7.3 Simulation, Discussion, and Considerations

Figure 7.4.a shows the dependence of the subthreshold swing (S) on the thickness of the substrate (t_{si}) and the buried oxide film (t_{BOX}). It illustrates how a desired value of S can be achieved by selecting suitable values of t_{si}, t_{BOX} and/or the ratio t_{si}/t_{BOX}. It is

observed that when this ratio is much larger than 1, S is reduced. Therefore, SOI-FinFET on a thin BOX and thicker substrate gives a better subthreshold swing. Figure 7.4.b shows the dependency of the subthreshold swing on the fin geometrical parameters: fin-width, and fin-height. It is observed that smaller width and larger height of the fin give a smaller value of subthreshold swing leading to better performance in the subthreshold region. It is important to note that the fin aspect ratio (*AR = Fin-height/Fin-width*) is a very critical performance parameter. Therefore, neither the width nor the height should be changed independently. This geometric ratio has a significant effect on the controllability of the channel, short-channel-effects (SCEs), on-current (I_{on}), buried-insulator-induced barrier lowering (BIIBL), drain-induced-barrier-lowering (DIBL) and other related parameters. Therefore, it would be more relevant to observe the behavior of the SOI-FinFET for different fin aspect ratios. It is clear that the aspect ratio H_{fin}/W_{fin} must be much larger to reduce the subthreshold swing. However, technology scaling and fabrication process may restrict the use of such large ratio.



(a)



(b)

Figure 7.4: a) Variation of subthreshold swing with the thicknesses of the substrate (t_{si}) and buried oxide film (t_{BOX}). $H_{fin} = 14nm$, $W_{fin} = 7nm$, $t_{ox} = 1nm$, $L = 14nm$. b) Subthreshold swing for various values of fin height and fin width.

7.4 I_D vs. V_{GS} Characteristic

SOI-FinFET design requires a dimension analysis to limit short-channel-effect by controlling the subthreshold slope and the drain-induced-barrier-lowering (DIBL). This can be achieved by selecting a proper range of the aspect ratio H_{fin}/W_{fin}. In this section, we have investigated the (*I-V*) characteristics and the DIBL of the SOI-FinFET in the subthreshold region. The drain current of the SOI-FinFET at subthreshold region is dominated by diffusion current. This region illustrates how fast the device switches *ON* and *OFF*. For low-power applications leakage has to be well managed. The drain current for fully depleted SOI-FinFET at subthreshold region is given by (7.10) [105, 106]. Where $V_T = kT/q$, μ_n is electronic mobility, n_i is the intrinsic carrier concentration, V_{ds} is the drain-to-source applied voltage, and $V_{gs}^r = V_{gs}^l = V_{gs}$ is the gate voltage (same voltage applied to both left and right gates). $V_{fb}^r = V_{fb}^l = V_{fb} = \frac{\emptyset_m - (\chi + \frac{E_g}{2} + \emptyset_b)}{q} - \frac{K_B T}{2q} \ln\left(\frac{N_C}{N_V}\right)$ is the flat-band voltage (both left and right are equal due to the symmetrical structure of the device). χ is the electron affinity. Here $\emptyset_m$ is the potential difference between the Fermi level of the intrinsic silicon and the *p-type* silicon and is given by $\emptyset_m = V_T \ln(N_A/n_i)$. E_g is the silicon band-gap at room temperature (*300°K*), and q is the elementary charge.

Figure 7.5 presents the (*I-V*) characteristic of the SOI-FinFET for several aspect ratios ($AR = H_{fin}/W_{fin}$). It is shown that the leakage current decrease as *AR* increases.

This provides a way to select a reasonable *AR* to obtain the lower value of *S* and low leakage.

$$I_{ds} = \frac{W_{Fin}H_{Fin}\mu_n}{L_{gate}V_T} qn_i \exp\big((V_{gs} - V_{fb})/nV_T\big)[1 - \exp(-V_{ds}/V_T)\,] \quad (7.10)$$

$$DIBL = \frac{V_{th}(V_{DS} = 0.5) - V_{th}(V_{DS} = 25mV)}{V_{DS}(= 0.5V) - V_{DS}(= 25mV)} \quad (7.11)$$

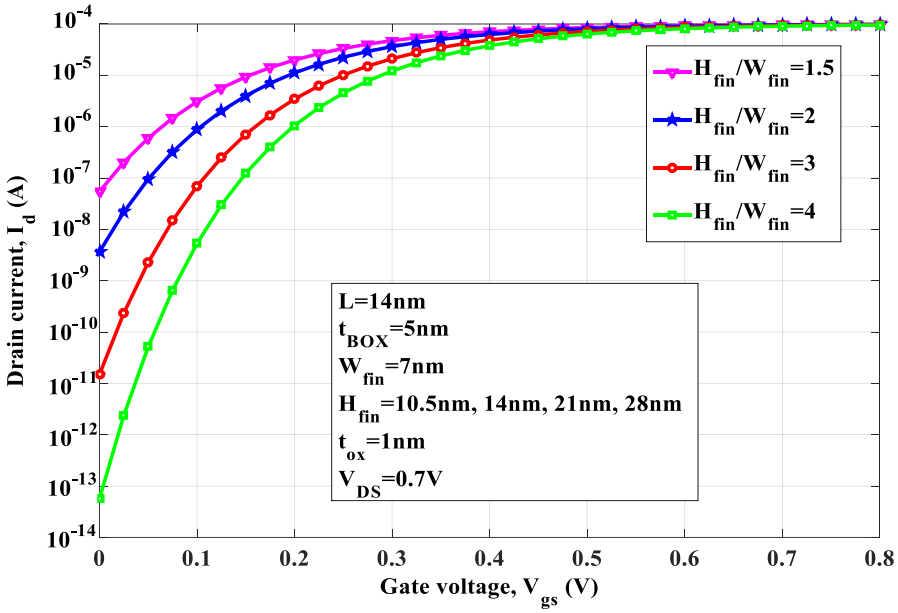
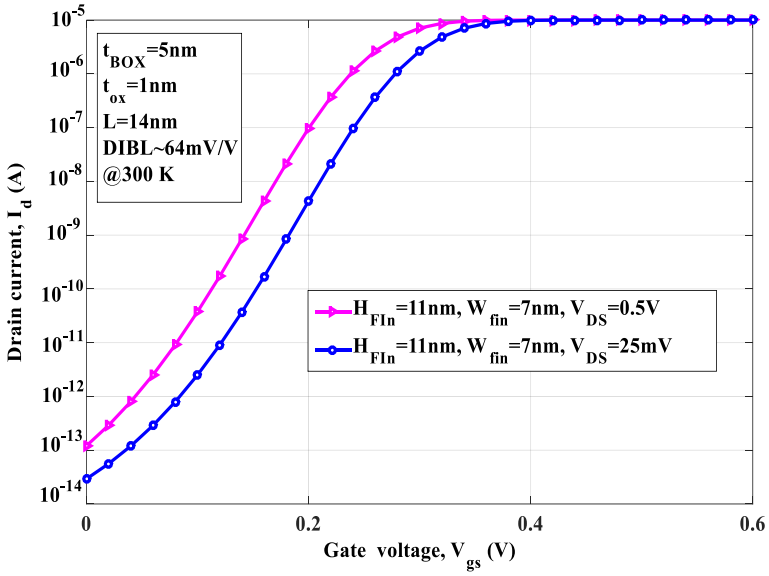


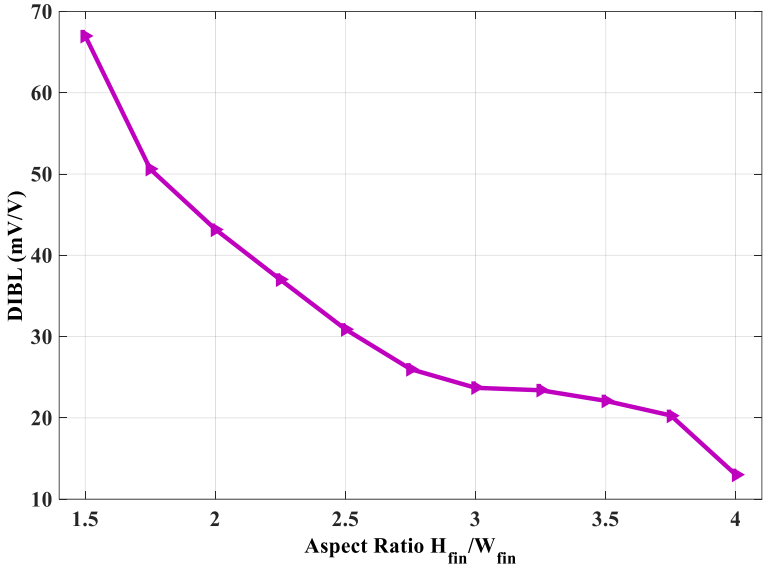
Figure 7.5: $I_d - V_{gs}$ characteristic of SOI-FinFET device, $L = 14nm$, $W_{fin} = 7nm$ and $H_{fin} = 10.5nm - 28nm$ at $V_{ds} = 0.7V$.

We have also studied the impacts of the SOI-FinFET aspect ratio (H_{fin}/W_{fin}) on the Drain-induced-barrier-lowering (*DIBL*). The *DIBL* is defined as the difference in the

threshold voltage extracted at $V_{DS} = 25mV$ and $V_{DS} = 0.5V$ and normalized by this difference of drain voltage. *DIBL* is calculated using (7.11), where V_{th} is the threshold voltage for each geometric aspect ratio. Figure 7.6.a shows *DIBL of* $\sim 64\, mV/V$ at $AR \sim 1.5$. This value can be reduced by increasing the aspect ratio (*AR*). From Figure 7.6.b, it is observed that by lowering *AR*, *DIBL* effect can be reduced.



(a)



(b)

Figure 7.6: a) I-V characteristics of SOI-FinFET showing the effect of the drain-source voltage V_{DS}, b) DIBL dependency on the aspect ratio H_{fin}/W_{fin}

Engineering the structure of the SOI-FinFET by optimizing the fin height, fin-thickness, oxide thickness, and the channel length is a key factor to increase the on-current and to reduce the leakage current. This can be achieved by having a superior electrostatic and excellent control over the channel. Our results indicate that the aspect ratio H_{fin}/W_{fin} can be modified for high–performance and ultra-low-power subthreshold applications. For an aspect ratio greater than 2 ($AR > 2$), the transistor effective area increases, therefore, the driving capability enhanced due to superior electrostatic integrity and large vertical channel. This capacitance and geometrical analysis, show that increasing

the aspect ratio H_{fin}/W_{fin} from 2 to 3 can improve device conductivity levels and lower *DIBL* giving an excellent subthreshold performance. This corresponds to a wide channel closer to the vertical gates improving the electrostatic of the device. Therefore, a high aspect ratio will give a lower DIBL and lower subthreshold swing. Hence, device with FinFET structure (*AR > 2*) exhibit better characteristics owing to more uniform potential distribution inside the channel. The concept of tall and narrow fins has been proven in several publications [34, 107]. These conclusions also agree with A. Kranti *et al*. in [31] and J.-P. Colinge in [5] that tall fins reduce short-channel-effect and lead to better performance. B. Yu *et al*. conclude that FinFET electrostatics could be further enhanced by reducing the fin width [108]. M. Rodwell and D. Elias in [109], reported that tall and narrow fins exhibit excellent subthreshold performance with nearly ideal subthreshold slope and DIBL. In [107], high aspect ratio of tri-gate FinFETs fabricated with fin widths down to 5nm and a record aspect ratio of 13. The device demonstrates excellent performance, manifest in reduced off-state leakage due to the improved electrostatic control of the gate over the channel.

The aspect ratio tuning and tradeoffs can be summarized in the area or layout efficiency, manufacturing complexity (fins with uniform and narrow width), design efficiency (short-channel-effect). FinFETs with high aspect ratio are superior layout efficiency and less area penalty [110]. This result is established by Anil *et al*. [111] which

conclude that higher fin aspect ratio is required for FinFET to have layout efficiency comparable to that of planar MOSFET. Narrow width and a large aspect ratio provide better channel control, hence lower leakage (W_{fin} is scaled to prevent short-channel-effects). However, wider transistors (large W_{fin}) provide more current per Fin. W_{fin} must be smaller to effectively suppress off-state leakage current. FinFET efficiency can be increased by integrating various effective channels in multi-parallel fins fusion (Figure 3.6), in addition to increasing the fin height for larger current per layout area.

7.5 Conclusion

In this chapter, we have studied the subthreshold swing of the SOI FinFET device. We proposed an analytical model to approximate the subthreshold swing based on the capacitive coupling model in subthreshold regime. We have also demonstrated the impact of the substrate thickness, the buried oxide film thickness (BOX), the fin width, fin height and the gate oxide thickness (TOX) on the subthreshold swing. This approximation shows that the *aspect ratio* H_{fin}/W_{fin} has a significant effect on the subthreshold swing and DIBL of the device.

CHAPTER 8

MULTICHANNEL TUNNELING CARBON NANOTUBE FET

TFETs, in general, suffer from low on-state current (I_{on}). In this chapter, we propose a new TFET structure to increase the drain to source current of the tunneling devices. This design is based on single-walled carbon nanotubes (SWCNTs). The idea is to provide multiple SWCNTs as tunneling path. We demonstrated the concept with three SWCNTs. By having three tunneling paths in a single device, higher on-current can be achieved. In this study, the diameter of the tubes and the gate oxide thickness are adjusted to obtain a high I_{on}.

8.1 Introduction

Ultra-low-power (ULP) designs using conventional FETs face fundamental roadblocks due to the thermionic emission limit of $60mV/decade$ (KT/q). This barrier is unbreakable even in the very new emerging device structure SOI-FinFET. ULP design requires a subthreshold swing much lower than $60mV/decade$ - a limit imposed by the factor *KT/q*, which is known as "*Boltzmann tyranny*". The tunnel field-effect transistor (TFET) is a revolutionary technology that has a very strong potential to break the thermodynamic barrier of conventional FETs and provide a very steep subthreshold slope. TFET technology is not impacted by *KT/q* factor, and would also allow further

reduction of channel length to extend Moore's law. However, TFETs, in general, suffer from low on-state current (I_{on}).

We propose a new TFET structure to increase the drain-to-source current of the tunneling device. The design is based on single-walled carbon nanotubes (SWCNTs). The idea is to provide multiple SWCNTs as tunneling paths. We have demonstrated the concept with three SWCNTs. By having three tunneling paths in a single device higher on-current can be achieved while keeping subthreshold swing lower than $60mV/decade$. In this study, the diameter of the tubes and the gate oxide thickness are adjusted to obtain a high I_{on} and steep subthreshold slope.

8.2 The Proposed Multichannel Carbon Nanotube Tunnel-FET (MT-CNTFET)

To improve the device characteristics, the industry as a whole is moving towards multi-gate technologies. Recent FinFET is a successful implementation of tri-gate MOSFET structure. In the introduction chapters, we have already elaborated that Carbon nanotube is considered as a promising alternative to conventional semiconductor materials used in the IC industry because of its novel properties. Tunneling field effect transistors based on CNT have shown great rewards over other nanomaterials. Low bandgap (bandgap inversely proportional to diameter of the tubes) [112], high mobility, and near- ballistic performance [113, 114], high stability, high scalability, the ability to be integrate with *high-*κ materials [115], low power, low leakage [116] are some of the major advantages of the CNT. Our proposed TFET encompasses these two emerging trends in material and device structure in a new logic device. The concept is illustrated in Figure 8.1. Here, three

SWCNTs are carefully placed in between the source and the drain to form the multichannel tunneling path (channel), while the gate surrounds the SWCNTs on three sides as shown in Figure 8.1. The entire active region (source-channel-drain) of the device is separated from the body by a buried layer of SiO_2. This structure maintains the tri-gate shape where the source is highly *n-doped* (n^+), the drain is highly *p-doped* (p^+), and the channel that consists of three SWCNTs provides an easy tunneling path. We called this structure ***Multichannel Tunneling Carbon Nanotube Field-effect-transistor (MT-CNTFET)***. The proposed structure combines the advantages of CNTs and already commercialized SOI-FinFET technology.

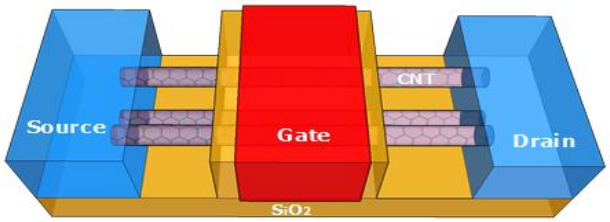


Figure 8.1: The proposed structure of Multichannel Tunneling Carbon Nanotube Field-effect-transistor (MT-CNTFET). The MT-CNTFET is a three-terminal device with the channel that consists of three carbon nanotubes (undoped or slightly doped), and highly doped p^+ and n^+ source and the drain, respectively.

BTBT phenomenon is widely perceived as a way to achieve lower subthreshold swing. The tunneling robustness depends on the barrier width of the *p-n* junction, and thus

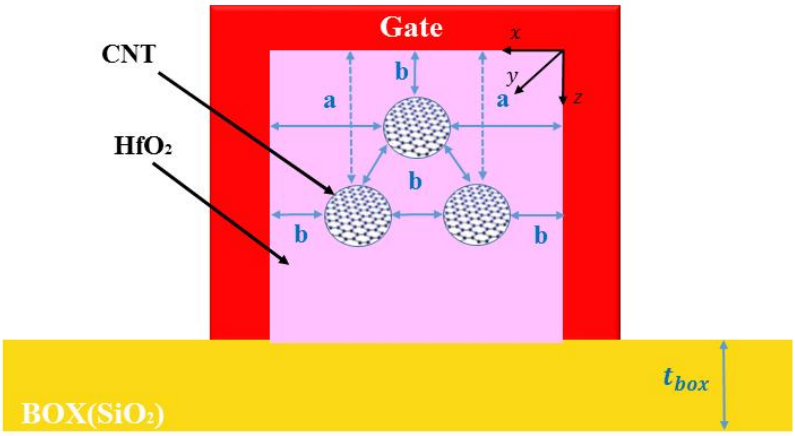


Figure 8.2: MT-CNTFET vertical cross section: *b* is the distance of the CNT from its nearest gate and *a* is the distance of a CNT from other two gates. We assumed that the three CNTs are at a distance *b* from each other. This internal structure is selected to maintain the exact same electric field in every tube. In this design structure, we have taken $a = \frac{3b+d_{ct}}{2}$.

the doping profile in both the junction and the channel. With high doping, the depletion width is small, which allows for better tunneling. In this design, the CNTs were placed so that the electric field applied on the CNTs is parallel. By having a similar electrostatic potential over all the CNTs, the same amount of carriers can tunnel through every channel. Consequently, each channel can deliver the same current density, leading to a large total on-state current. Conversely, having different electrostatic fields applied over all CNTs

lead to a complex analysis and difficult gate control as well as increasing off-state current. Figure 8.2 shows a vertical cross section along the transistor gate of the proposed arrangement of CNTs. Figure 8.2 also displays the structural design and how the CNTs are placed to ensure the same electrostatic potential on each CNT. The arrangement will provide three identical parallel current paths that would increase the overall tunneling current density.

The electrical behavior of the proposed device depends on the surface potential. For all the analysis and modeling of the device properties and operation, a comprehensive investigation of the surface potential is required. That's why we first present the analysis and modeling of surface potential of the proposed device. The electrostatic potential $\psi(x, y, z)$ in the CNTs of *MT-CNTFET* device obeys the Poisson equation (8.1).

$$\Delta^2\psi(x, y, z) = \frac{qN_A(x, y)}{\varepsilon_{si}} = \frac{q}{\varepsilon_{si}} n_i e^{q\psi/KT} \tag{8.1}$$

Where $\psi(x, y, z)$ is the potential at a particular point (x, y, z) in the CNTs channel, n_i is the intrinsic carrier concentration, ε_{ct} is the CNT permittivity. The boundary conditions required to solve the 3D Poisson's equation are given as:

$$\psi(a, y, z) - \frac{b}{\varepsilon_{ox}}\left[\varepsilon_{ct} \left.\frac{\partial\psi(x, y, z)}{\partial x}\right|_{x=a}\right] = V_g^l - V_{fb}^l \tag{8.2}$$

$$\psi(a, y, z) - \frac{b}{\varepsilon_{ox}}\left[\varepsilon_{ct} \left.\frac{\partial\psi(x, y, z)}{\partial x}\right|_{x=-a}\right] = V_g^r - V_{fb}^r \tag{8.3}$$

$$\psi(x,0,z) = V_{bi} \tag{8.4}$$

$$\psi(x,L_{ch},z) = V_{bi} + V_{ds} \tag{8.5}$$

$$\psi(x,y,a) - \frac{b}{\varepsilon_{ox}}\left[\varepsilon_{ct}\left.\frac{\partial\psi(x,y,z)}{\partial z}\right|_{z=a}\right] = V_g^{top} - V_{fb}^{top} \tag{8.6}$$

$$\psi(x,y,-a) + \frac{b}{\varepsilon_{ox}}\left[\varepsilon_{ct}\left.\frac{\partial\psi(x,y,z)}{\partial z}\right|_{z=-a}\right] = 0 \tag{8.7}$$

Where: V_{bi} is the built-in potential at n^+-p junctions, V_{ds} is the drain-to-source applied voltage, $V_g^l = V_g^r = V_g^{top} = V_{gs}$ is the gate voltage (same voltage applied on three sides of the gate), $V_{fb}^r = V_{fb}^l = V_{fb}^{top} = \varphi_m - \Phi_{ct}$ is the flat-band voltage (due to symmetrical device). χ_{ct} is the electron affinity and φ_m is the work function of the metal. Where Φ_{ct} is the CNTs work function, which is given by $\Phi_{ct} = \chi_{ct} + \frac{E_g}{2q} - \Phi_B$, E_g is the CNT's band-gap at room temperature $300°K$, χ_{ct} is the electron affinity of CNTs, $\Phi_B = V_T \times \ln\left(\frac{N_d}{n_i}\right)$ is the Fermi potential, V_T is the thermal voltage, n_i is the intrinsic carrier concentration, and q refers to elementary charges.

To solve equation(8.1) we separate it into 1D, 2D, and 3D Poisson equation as shown in (8.8)-(8.11) using the boundary condition(8.2) – (8.7).

$$\psi(x,y,z) = \psi_{1D}(x) + \psi_{2D}(x,y) + \psi_{3D}(x,y,z) \tag{8.8}$$

$$\frac{\partial^2 \psi_{1D}(x)}{\partial^2 x} = \frac{q}{\varepsilon_{ct}} n_i e^{q\psi_1/KT} \tag{8.9}$$

$$\frac{\partial^2 \psi_{2D}(x,y)}{\partial^2 x} + \frac{\partial^2 \psi_{2D}(x,y)}{\partial^2 y} = 0 \tag{8.10}$$

$$\frac{\partial^2 \psi_{3D}(x,y,z)}{\partial^2 x} + \frac{\partial^2 \psi_{3D}(x,y,z)}{\partial^2 y} + \frac{\partial^2 \psi_{3D}(x,y,z)}{\partial^2 z} = 0 \tag{8.11}$$

Detailed solutions for the Poisson/Laplace equations (8.9) – (8.11) are provided in APPENDIX B. Surface potential at each CNT can be calculated as:

$$\begin{aligned} \psi(x,y,z) = {} & \sqrt{\lambda}\left(Ae^{\sqrt{\lambda}y} - Be^{-\sqrt{\lambda}y}\right)\left(\frac{\varepsilon_{ox}}{\varepsilon_{ct}\, b} + 1\right) \\ & + \sqrt{\frac{2k_B T n_i}{\varepsilon_{ct}}} \tan\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{ct} k_B T}}\, e^{\frac{q\psi_0}{2K_B T}} x\right) \\ & + \eta\, k_2 \sin(k_1 x)\, \cos(k_2 z)\, \cosh(k_3 y) \end{aligned} \tag{8.12}$$

8.3 Analysis and Modeling of Electric Field, Drain Current, and Subthreshold Swing

The electric-field distribution along the *x-axis* can be obtained by differentiating the surface potential $\psi(x)$ with respect to x. The lateral electric field can be written as:

$$E(x) = \frac{d\psi(x)}{dx} = \sqrt{\frac{2qn_i}{\varepsilon_{ct} V_t}} \tan\left(\zeta e^{\frac{\psi_0}{2V_t}} x\right) \tag{8.13}$$

The electric-field distribution along the *y-axis* can be obtained by differentiating the surface potential $\psi(x, y)$ with respect to y as in (8.14). Similarly, the electric-field distribution along the *z-axis* can be obtained by differentiating the surface potential $\psi(x, y, z)$ with respect to *z* as in (8.15).

$$E(y) = \sqrt{\lambda}\left(Ae^{\sqrt{\lambda}y} - Be^{-\sqrt{\lambda}y}\right)\left[\left(x - \frac{x^2}{a + \frac{d_{ct}}{2}}\right)\frac{\varepsilon_{ox}}{\varepsilon_{ct\,b}} + 1\right] \tag{8.14}$$

$$E(z) = \frac{d\psi(x, y, z)}{dz} = \eta\, k_2 \sin(k_1 x)\ \cos(k_2 z)\ \cosh(k_3 y) \tag{8.15}$$

The drain current I_{ds} in the Multi-gate TFET is based on the tunneling of electrons from the valence band of the source to the conduction band of the CNT tubes. The tunneling generation rate (G) can be calculated using Kane's model. The total drain current is computed by integrating the band-to-band generation rate over the volume of the device [117]. Therefore, the drain current of the device can be expressed as in (8.16).

$$I_{ds} = q \iiint G(E)dxdydz \tag{8.16}$$

Where $G(E) = C\frac{|E|^2}{\sqrt{E_g}}e^{\left(-\frac{E_g^{\frac{3}{2}}}{|E|}\right)}$, and $|E|$ is the magnitude of the electric field defined as $|E| = \left(E_x^2 + E_y^2 + E_z^2\right)^{\frac{1}{2}}$.

First few terms of the Taylor series expansion are used to approximate the drain-source current:

$$
\begin{aligned}
I_{ds} = {} & 4CaL_{ch}\tan\left(a\zeta e^{\frac{\psi_0}{2V_t}}\right) \\
& + 4a^2\lambda\left(\frac{\varepsilon_{ox}}{\varepsilon_{ct\,b}}+1\right)^2\left\{\frac{A^2}{2\sqrt{\lambda}}\left(e^{2\sqrt{\lambda}L_{ch}}-1\right)\right. \\
& \left.-\frac{B^2}{2\sqrt{\lambda}}\left(e^{-2\sqrt{\lambda}L_{ch}}-1\right)2ABL_{ch}\right\} \\
& + \eta^2k_2^2\left(a+\frac{\sin(ak_2)}{ak_2}\right)\left(\frac{2k_3L_{ch}+\sinh(2k_3L_{ch})}{4k_3}\right)\left(a-\frac{\sin(2ak_1)}{2k_1}\right)
\end{aligned}
\tag{8.17}
$$

The subthreshold swing of the device is defined as in (8.18) from (8.17). Utilizing mathematical expansion subthreshold swing (S) can be written as in (8.20):

$$S = \left(\frac{d\log(I)}{dV_{gs}}\right)^{-1} \tag{8.18}$$

$$S = \ln 10\left[\frac{d}{dV_{gs}}\ln\left\{4CaL_{ch}\tan\left(a\zeta e^{\frac{\psi_0}{2V_t}}\right)\right\}\right]^{-1} \tag{8.19}$$

$$S = \ln 10\times\left[\frac{\psi_0}{2V_t}\ln\left\{4\mathrm{CaL_{ch}}\tan\left(a\zeta e^{\frac{\psi_0}{2V_t}}\right)\right\}\frac{d\psi_0}{dV_{gs}}\right]^{-1} \tag{8.20}$$

Where $\frac{d\psi_0}{dV_{gs}} \approx 1 - \frac{V_t(V_{gs}-\varphi_{ms})}{\left(\frac{qn_i}{C_{ox}\varepsilon_{ct}}\right)^2+(V_t[V_{gs}-\varphi_{ms}])^2}$ and $C_{ox} = \frac{\varepsilon_{ct}}{b}$

8.4 Analysis of the On-state Current (I_{on}) of the Proposed MT-CNTFET

The tunneling current depends on the transmission probability, $T(E)$ of the inter-band tunneling barrier. The BTBT probability *T(E)* between the source and the channel is approximated for a triangular potential using the Wentzel-Kramers-Brillouin (WKB) approximation and it is given by (8.21) [51, 117, 118], where m^* is the effective carrier

mass, E_g is the band gap, and $\xi = (E_g + \Delta\Phi)/\lambda_{Tri-gate}$ is the electric field in the transition region ($\Delta\Phi$ denoted the energy overlap between the conduction band edge and the valence band edge at the source/channel tunneling junction). The screening length ($\lambda_{Tri-gate}$) is given by (8.22), where ε_{ct} and ε_{ox} are the dielectric constants of the CNTs and the gate oxide layer, respectively. *b* is the thickness of the gate oxide at a distance from the tubes, and d_{ct} is the diameter of CNTs [118, 119, 120]

$$T(E) = \exp\left(\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3q\hbar\xi}\right) \tag{8.21}$$

$$\lambda_{Tri-gate} = \sqrt{\frac{2\varepsilon_{ct}d_{ct}^2 \ln\left(1+\frac{2b}{d_{ct}}\right) + \varepsilon_{ox}b^2}{16\varepsilon_{ox}}} \tag{8.22}$$

For simplicity, we have associated each tube with the neighboring gate in the screening length formula (8.22). The screening length ($\lambda_{Tri-gate}$) refers to the spatial extent of the electric field, which depends on the device geometry (number of gates), the dielectric constants, the thickness of the gate dielectric, and type of semiconductor used in the device. Increasing the number of gates will reduce the screening length. In the proposed device, $\lambda_{Tri-gate}$ also depends on the screening by neighboring tubes, which is not covered by this approximation [121]. The tunneling arises through the screening length. As the channel length is scaled down, the depletion zones of the source and the drain side cross. Also as

the channel length is scaled down, the barrier is reduced and the source-drain potential contributes to band bending over a significant portion of the device and the rest of charge controlled by the gate. A small screening length will reduce the drain contact on the channel and suppresses short-channel-effect (SCE). $\lambda_{Tri-gate}$ depends on device geometry, doping profiles, and gate capacitance. Screening length should be minimized for high barrier transparency [119, 122].

The dielectric constant of CNT is dependent on its symmetry and the tube diameter d_{ct}. $\varepsilon_{ct} = 1 + \frac{2\alpha_0}{R^2}$, where for $\alpha_0 = \frac{Cd_{ct}^2}{4}$ semiconducting CNT, $C = 2.15$. Since we are using undoped low-dimensional semiconductor CNTs, the dielectric constant is $\varepsilon_{ct} = 1$ [123]. The semiconducting bandgap of CNTs can be expressed in (8.23) [124], where v_F is the Fermi velocity (8.1×10^5m/s), $\mathrm{d_{ct}}(11,3) = \frac{\alpha\sqrt{3}}{\pi}\sqrt{(m^2+n^2+nm)} \approx 1\ nm$, n(11) and m(3) are chirality of CNT, and $\alpha_0 = 0.142nm$ is the inter-atomic distance between each carbon atom and its neighbor [125, 126]. With the above-mentioned parameters, the bandgap is $E_{gap} = 0.71\ eV$. The electron affinity of the carbon nanotube is taken to be 4.18 eV based on the work of [127, 128].

$$E_{gap} = \frac{4\hbar v_F}{3d_{ct}} \tag{8.23}$$

$$I = \frac{4q}{h}\int T(E)[f_S(E) - f_D(E)]dE \tag{8.24}$$

The tunneling current density is given by (8.24) [129], where *T(E)* is the transmission probability across the junction, $f_S(E)$and $f_D(E)$ are the Fermi function in the source and the drain respectively, q is the electron charge, and h is the Planck's constant. Based on Kane's model, the tunneling current density can be derived as in [122]. Here (8.25) is modified to include multichannel tunneling design.

$$J = \frac{\sqrt{2m^* q^3}\xi V}{4\pi^2 \hbar^2 \sqrt{E_g}} \exp\left(\frac{-4\sqrt{2m^* E_g^3}}{3q\hbar\xi}\right) \tag{8.25}$$

This design retains the same concept of tunneling and is expected to break the $60mV/decade$ due to its carrier transport property which is independent of "*KT/q*". In addition, the I_{on} would be expected to increase by a factor of three compared to single-channel TFET.

8.5 Result and Discussion

In our analysis, it is observed that by carefully tuning the gate oxide thickness and using a small tube diameter, a high I_{on} can be realized. CNTs also boost the tunneling current because of their small effective mass. Figure 8.3 shows the probability of tunneling current as a function of the CNT's diameter (d_{ct}) and the oxide thickness (b). Smaller d_{ct} and b leads to higher energy window ($\Delta\Phi$) and lower screening length ($\lambda_{Tri-gate}$). In addition, smaller b provides better control of the gates over the CNTs. Consequently, the

probability of tunneling current increases with the decrease of d_{ct} and b as shown in Figure 8.3. With higher probability of tunneling $T(E)$, a large current density can be achieved at lower gate voltage.

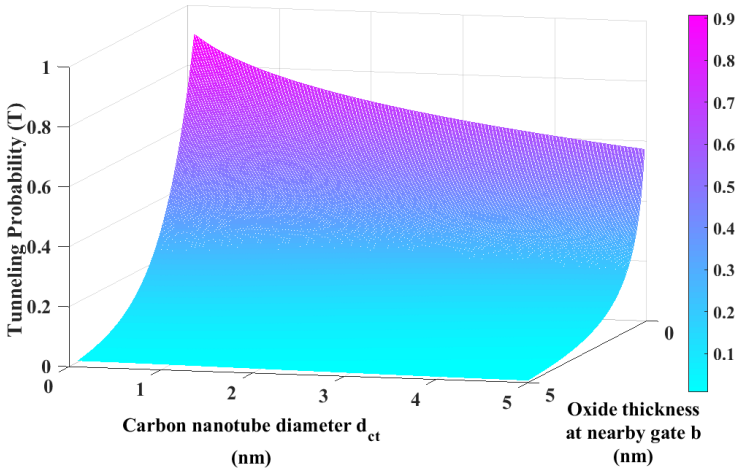


Figure 8.3: Probability of tunneling in MT-CNTFET as a function of CNT diameter (d_{ct}) and oxide thickness (b) between a CNT and nearest gate.

Figure 8.4 illustrates the dependence of the current density on b and V_{gs}. A higher current density can be achieved with smaller b and higher V_{gs}. Figure 8.5 shows the dependency of the current density on CNT's diameter (d_{ct}) and V_{gs}. It is observed that smaller diameter leads to a higher current density for a particular V_{gs}. For a constant d_{ct}, current density increases with the increase of V_{gs}. A smaller CNT diameter increases the tunneling probability because the energy bandgap of CNT is inversely proportional to its diameter. Therefore, higher I_{on} can be obtained from CNTs with smaller diameter.

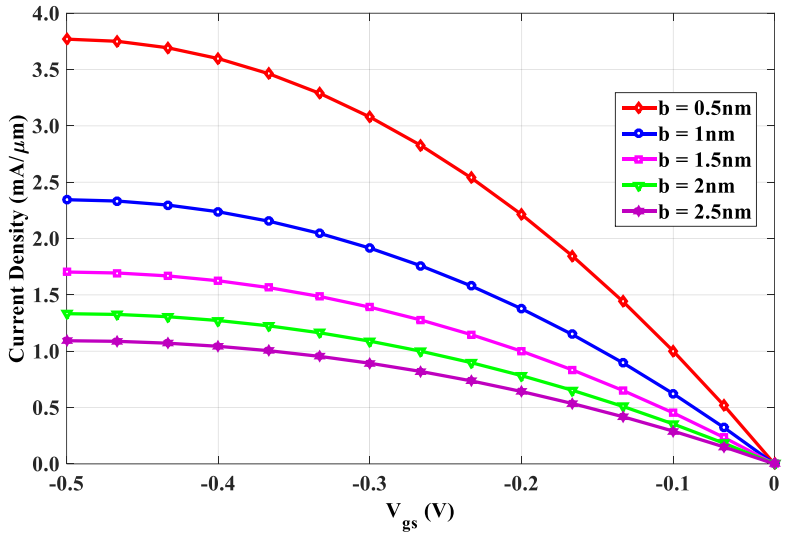


Figure 8.4: Tunneling current density of the p-type MT-CNTFET as a function of gate voltage (V_{gs}) and oxide thickness (b).

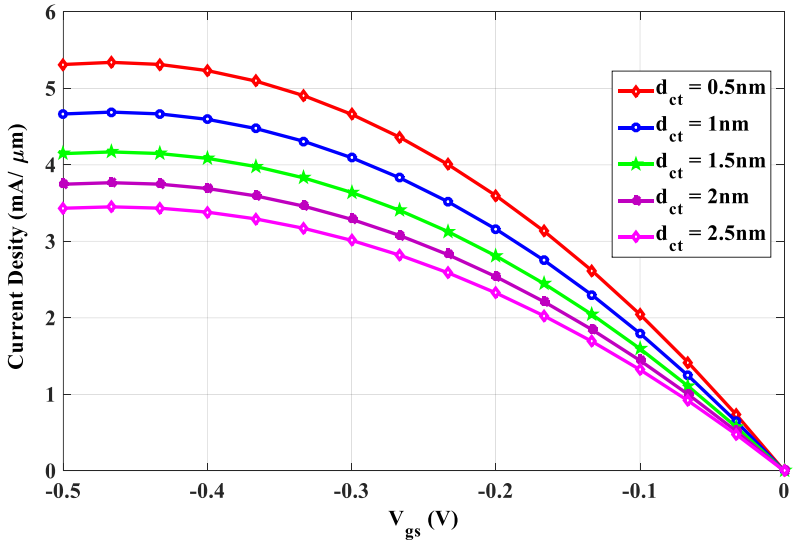


Figure 8.5: Tunneling current density of the p-type MT-CNTFET as a function of carbon nanotube diameter d_{ct}.

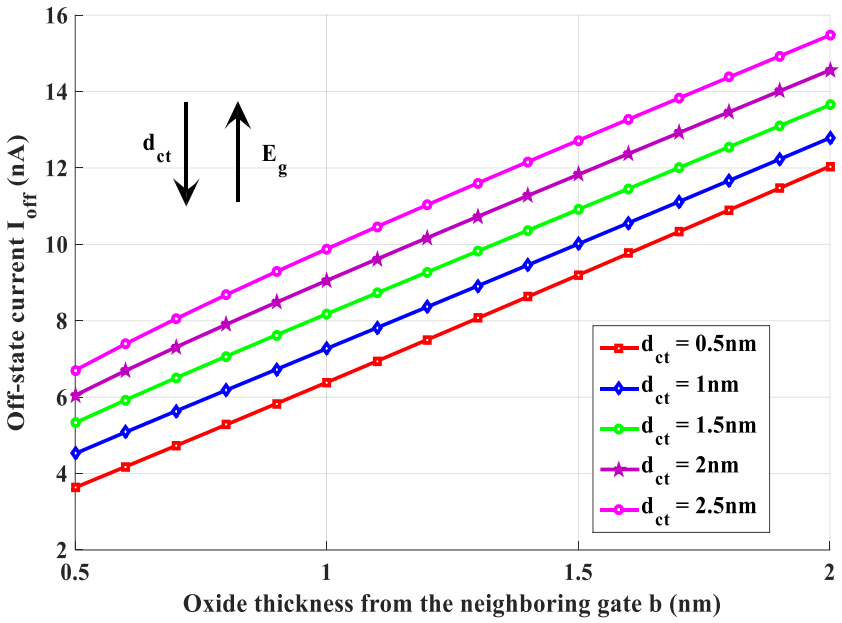


Figure 8.6: Off-state current I_{off} as function of the of oxide thickness from the neighboring gate b at different nanotube diameter. Channel length of $10nm$.

Larger CNT diameter leads to higher leakage where off-state current (I_{off}) increase as the bandgap decreases. A motivation to keep the CNT's diameter smaller in MT-CNTFET to increase I_{on} and decrease I_{off}. It is also important to note that the lower oxide thickness (b) provides better gate control over CNTs, which leads to lower leakage. Figure 8.6 shows the variation of I_{off} as a function of b and d_{ct}. It is also important to notice that the ratio a/b will also have an impact on the subthreshold swing. From Figure

8.7, it can be observed that having a value close to 1 for the ratio *a/b* leads to a smaller value of *S* (steeper slope).

Since the bandgap is inversely proportional to the CNT's diameters, the subthreshold swing increases at a large diameter. We also notice that a small ratio gives a better subthreshold swing due to the better electrostatic field at a lower oxide thickness. Figure 8.8 shows small CNT's length and a small diameter required for a steeper slope (small *S*). It is also seen that small CNT's length and a small diameter is required for a steeper slope (small *S*).

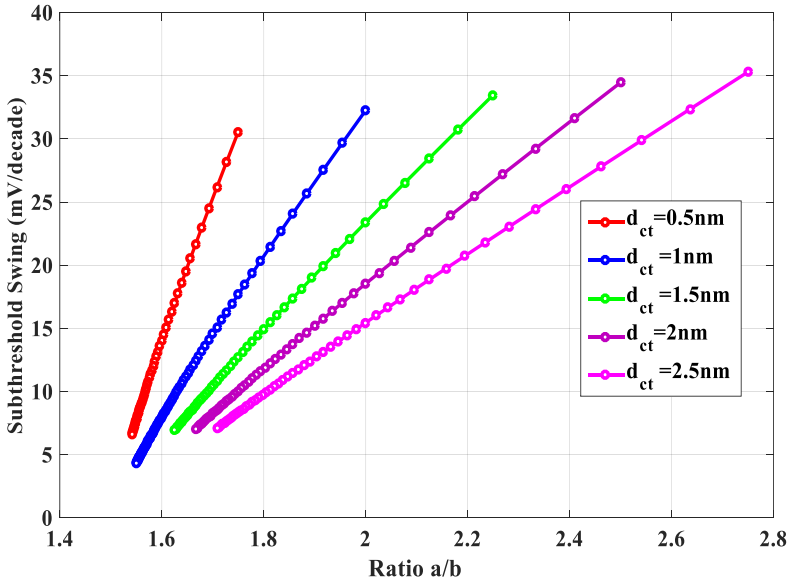


Figure 8.7: Subthreshold swing as a function of *a/b* ratio for different CNT's diameter.

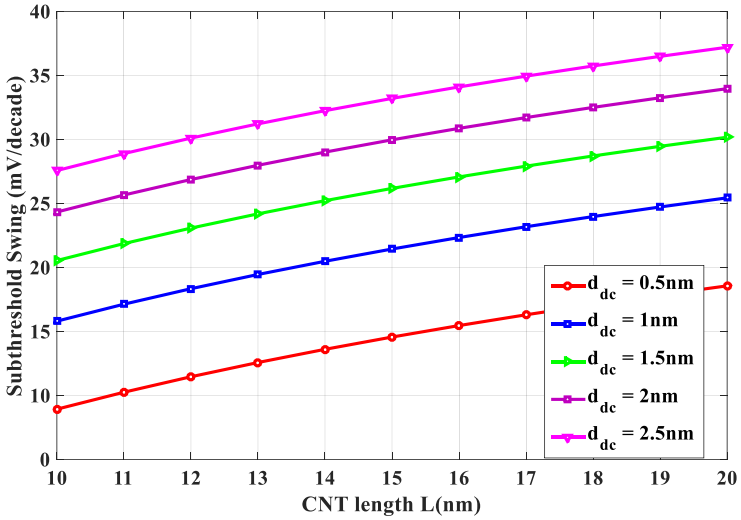


Figure 8.8: The dependence of the subthreshold swing on the CNT's length.

Since nanotubes typically exhibit very small diameters, they allow excellent gate control without suffering from mobility degradation. With a small diameter (d_{ct}~$0.5nm$) of a CNT, the gate can strongly impact the bands inside the tube channel, resulting in a high tunneling probability for electrons and holes. A large diameter decreases the gate controllability and the oxide capacitance in the channel, leading to poor control of the gate on the conductivity of the channel. Therefore, a smaller subthreshold swing can be obtained when a smaller CNT diameter is used. In previous CNT based TFET proposals, it has always been a trade-off between low I_{off} and higher I_{on}/I_{off} ratio. In this proposed MT-CNTFET, smaller-diameter CNTs ensure lower I_{off} and multiple parallel tunneling paths ensure higher I_{on}, leading to larger I_{on}/I_{off} ratio. Therefore, the thickness of the gate

insulator and the diameter of the tubes can be scaled aggressively to obtain better electrostatic control, lower subthreshold swing, higher on-current and lower off-current in the proposed MT-CNTFET. At this point, it is important to elaborate on a critical observation about the dependence of the performance of the MT-CNTFET on CNT diameter. For a conventional conductor, a larger cross-section (larger diameter) means higher electrical conductivity. Therefore, it is natural to assume that smaller CNT diameter would lead to higher resistance in the channel, source and drain areas. However, CNTs exhibit some unique electrical and physical properties, which sometimes defy conventional conductor characteristics. In [130], it is demonstrated that the off-current in a CNT with a narrower diameter is much lower than that for wider diameters. The high off-current level in the wider diameter CNTs can be attributed to the leakage of current due to the increase in the thermally excited carriers in larger CNTs. In smaller diameter CNTs, the tunneling current probability increases (as depicted in Figure 8.5) due to reduced leakage. Due to this inverse dependence characteristic, the I_{ds} conductivity increases as the d_{ct} decreases. Also, the valence band edge of the CNT-channel is closer to the conduction band edge of the source at the same gate field for smaller diameter CNTs. Furthermore, smaller d_{ct} and a/b lead to higher energy window ($\Delta\Phi$) and lower screening length ($\lambda_{Tri-gate}$). *0.5* to *1nm* diameter enhances the gate's ability to control the potential of the channel, particularly

when the gate is configured to lay at the same distance from the CNTs. However, there are other factors that need to be taken into consideration.

8.6 Conclusion

In this chapter, we have proposed a new multichannel TFET based on single-walled CNT. The concept is validated through modeling and simulation of the physical and electrical characteristics of the proposed MT-CNTFET. It has been demonstrated that by optimizing the physical dimensions (ratio of the gate oxide thickness, CNT length, and CNT diameter) and careful placement of the CNTs, the proposed MT-CNTFET can achieve a much higher on-current and lower off-current compared to the conventional silicon MOSFET. Additionally, the proposed TFET has the potential to break the thermionic limit of the subthreshold swing of the conventional and emerging FETs. It is observed that for a certain set of geometric and electrical parameters the proposed MT-CNTFET provides very high I_{on}/I_{off} ratio and subthreshold swing far below $60mV/decade$. It is concluded that careful placement of the tubes between the highly-doped drain and source will increase the probability of tunneling current leading to higher I_{on}. The device geometry and the control voltage can be optimized to improve the performance. However, this analysis is not comprehensive. There are many other factors that need to be analyzed, such as the feasibility and manufacturing techniques of the device. We consider that CNTs are suitable for this type of design due to their 1D transport and smaller effective

carrier mass m^*. CNTs allow electrical transport with small diameter, and reasonable energy bandgap (E_g). The potential of integrating CNTs with *high-*κ materials ensures smaller screening length λ.

CHAPTER 9

PARTIALLY DEPLETED SILICON-ON-FERROELECTRIC INSULATOR FET

This chapter presents the concept of a new field-effect transistor based on ferroelectric insulator. The proposed design is named ***Silicon-on-Ferroelectric Insulator field-effect-transistor (SOFFET).*** The design combines the concept of negative capacitance in ferroelectric material and silicon-on-insulator (SOI) device. The design proposes that by burying a layer of ferroelectric insulator inside the bulk silicon substrate, an effective negative capacitance (NC) can be achieved.

9.1 Introduction

The fundamental thermodynamic limits on the minimum operating voltage and switching energy of conventional field effect transistors (FETs) is given by the limit of $S = 60mV/decade$, which is known as the '*Boltzmann tyranny*'. Even with the excellent electrostatic and enhanced transport properties in all the CMOS-based transistors (bulk, FinFET, and fully depleted silicon-on-insulator: FDSOI), the subthreshold swing 'S' will be larger than $60mV/decade$ at room temperature. For continuation of current technology and a smooth transition to a new design platform, near future devices must be compatible with conventional MOSFET and CMOS manufacturing processes. It would be very useful

if a lower value of S could be obtained in conventional FET or in a compatible device with some form of material and/or geometric modification until the complex fabrication processes involving emerging device technologies are well understood and pioneered. Therefore, FET based technology will remain as the foundation of micro-/nano-electronics for several more decades. Many contemporary researchers believe that negative capacitance will be the answer to many of the problems in nanoelectronics [15, 95]. Therefore, our intent is to develop a new device design for ultra-low-power applications employing silicon-on-insulator (SOI) FET structure and the concept of negative capacitance. Several novel device structures have been proposed to utilize negative capacitance of ferroelectric materials [15, 16]. Yet, all of these recent studies have suggested replacing the standard gate insulator (SiO_2) with a ferroelectric insulator to achieve a negative capacitance across the gate-stack leading to subthreshold swing below the Boltzmann limit. The negative capacitance based on ferroelectricity provides internal voltage amplification and lowers subthreshold swing.

9.2 Negative Capacitance Devices

Khan *et al.* [16] and Rusu *et al*. [94] suggested that by replacing the standard insulator (SiO_2) of MOSFET with a ferroelectric insulator of the right thickness, a negative capacitance can be reached that arises from the hysteresis of internal positive feedback from a ferroelectric capacitor. Ershov *et al.* [88] provided a proof of the hypothesis of negative capacitance effect in a nanoscale ferroelectric-dielectric heterostructure. Negative

capacitance refers to the power boost provided by the capacitor made of ferroelectric material paired with a dielectric (electrical insulator) [16]. Integration of ferroelectric materials into current MOSFET designs will preserve the same field-effect transistor operation, as well as compatibility with existing CMOS technology. In the design proposed in [15], the standard gate insulator (SiO_2) is replaced by a ferroelectric insulator. This design gives an amplification of the gate voltage, which leads to a subthreshold swing below the thermal voltage limit of $60mV/decade$. Salvatore *et al.* [86] claim that $S \approx 13mV/decade$ is achievable in a gate-stack of *Metal-Ferroelectric-Insulator*. However, recent studies predicted severe stability and reliability issues with a ferroelectric insulator at the gate. In addition to these issues, the gate-stack negative capacitance design would face front-end process difficulties and problems regarding high offset workfunction due to the stacking of multiple materials in the gate area. Since the gate is the control terminal of device, any unpredictable variation and reliability concern will greatly affect the operation of any circuits and systems based on gate-stack negative capacitance devices. In the current proposed gate-stack designs, the electric field due to the gate voltage can penetrate deep into the body and affect the behavior of the device. However, if the body contains a buried insulator layer, the electric field will die at the insulator layer.

In this research, we adopted a different approach. We propose a new device using SOI structure, where the buried SiO_2 insulator layer of SOI device would be replaced by a

ferroelectric insulator, while the gate insulator is the standard gate oxide dielectric. The goal is to increase the efficiency of subthreshold operation by lowering subthreshold swing (S) without changing the device structure and conventional fabrication process while taking advantage of the negative capacitance effect. The body-stack that we are proposing in this research has many advantages over the negative capacitance gate-stack. First, it is more compatible with the existing processes. Second, the gate and the working area of the device is similar to the planar MOSFET. Third, the complexity and material interferences are shifted to the body of the device rather than the gate and the working area. The function of the body region is to set the device characteristics so that the active terminals (source, drain and gate) can function properly. Therefore, the stability and reliability concerns will be significantly less prominent in our proposed negative capacitance body-stack device. Moreover, the proposed structure has a better scalability and superior constructability because of the high-dielectric buried insulator.

9.3 The Concept of Negative Capacitance based SOFFET

In the conventional MOSFET, the limit of $S = 60\, mV/decade$ is due to non-scaling of the thermal voltage "KT/q". To achieve a lower value of S, the ratio of the depletion capacitance and the oxide capacitance (C_{dep}/C_{ox}) of the device has to be restructured to develop a negative capacitance (NC) effect in the device structure.

Considering the coupling capacitance between the gate voltage and the bulk of a planar MOSFET, the body factor can be defined as (9.1):

$$\eta = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{\sum C_{channel-ground}}{C_{channel-gate}} \tag{9.1}$$

Here ψ_s is the surface potential, $\sum C_{channel-ground}$ is the semiconductor capacitance, and $C_{channel-gate}$ is the gate insulator capacitance. For S value below $60mV/decade$, the value of the body factor must be less than 1. For $0 < \eta < 1$, we must have $\sum C_{channel-ground}/C_{channel-gate} < 0$ or $\sum C_{channel-ground} < 0$, which means a negative capacitance is needed to achieve a subthreshold swing lower than $60mV/decade$.

We proposed to exploit negative capacitance (NC) phenomenon of the ferroelectric materials in the SOI device structure to reduce the subthreshold swing (S) below $60mV/decade$. We recommended to resolve the previously stated ferroelectric integration issues by having a buried layer of ferroelectric insulator inside the device structure (Figure 9.1). Our proposed design is the first effort to utilize the NC effect of ferroelectric insulators inside the SOI device body. The NC effect will boost the internal electric field and lower the subthreshold swing. This approach can have two structures – fully depleted and partially depleted SOFFET. Figure 9.1 presents the concept and the physical structure of PD-SOFFET and the fully depleted device is explored in chapter 10.

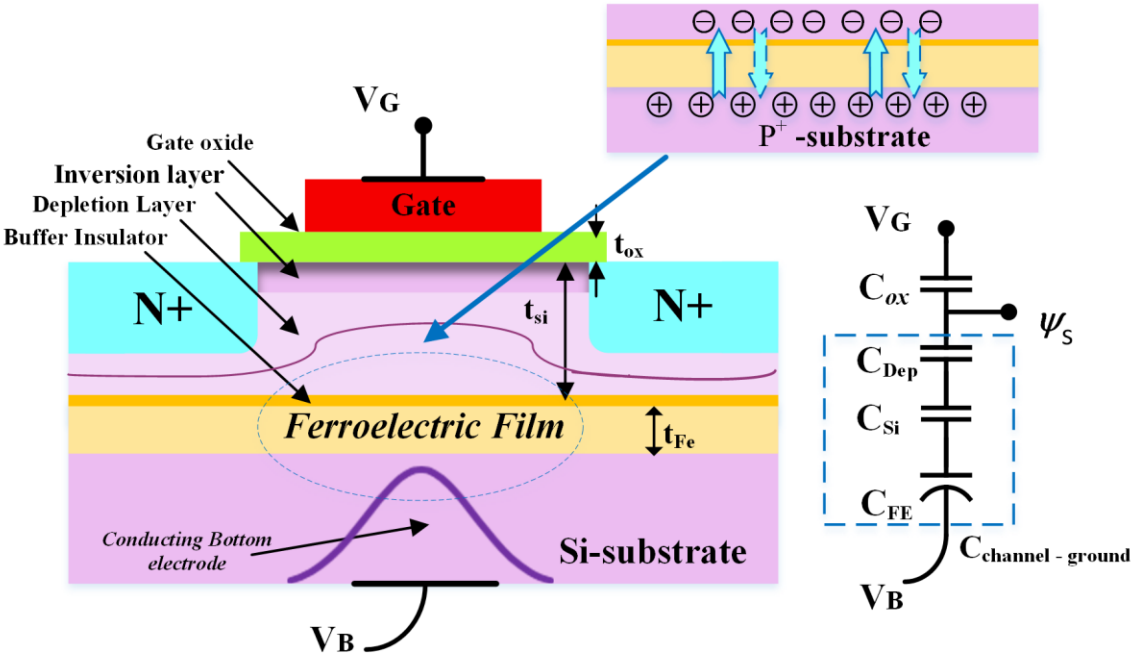


Figure 9.1: The proposed *PD-SOFFET* and its equivalent capacitive divider. In this design C_{Fe} is the ferroelectric capacitance, which acts as a back gate, and C_{Si} is the capacitance of the thin silicon film. The substrate is heavily doped *p-type* silicon to implement a bottom electrode.

9.4 The proposed PD-SOFFET

In this research, we adopted a different approach. We propose a new device using the SOI device structure, where a ferroelectric insulator replaces the buried SiO_2 insulator layer while the gate insulator would be the standard SiO_2 (or any other *high-κ* materials). Figure 9.1 illustrates the new device structure, which is very similar to the partially

depleted SOI device. The goal is to increase the efficiency of subthreshold operation by lowering the subthreshold swing (S) without changing the device structure and conventional fabrication process while taking advantage of the negative capacitance effect.

Inserting a buffer insulator layer can minimize the effect of charge accumulation between the silicon and the ferroelectric film. This insulating material is required to hold a high dielectric constant, high thermal stability, low leakage current, and good interface property with the silicon substrates. Materials like silicon oxynitride (SiON) and titanium dioxide (TiO_2) are considered as the diffusion barrier between silicon and ferroelectric film [131, 132].

The proposed device offers better switching performance due to inherent low short-channel-effects. Moreover, the SOFFET structure keeps the operating area of the device similar to the conventional MOSFET. Furthermore, the electric field (gate voltage) applied to construct the channel will not be deviated by the integration of additional processing materials in the gate stack. Thus, this structure provides a stable gate voltage compared to the gate-stack structure demonstrated in recent research.

9.5 Subthreshold Behavior of the Proposed PD-SOFFET

9.5.1 Subthreshold swing of PD-SOFFET

From the structure of Figure 9.1, we can calculate the body factor of the PD-SOFFET as shown in (1), where Δ represent the ratio $\sum C_{channel-ground}/C_{ox}$ as shown in (9.2) and (9.3), $\sum C_{channel-ground}$ represents the series association of C_{Dep}, C_{Si} and C_{Fe}. C_{Fe} represents the negative capacitance extracted by integrating a thin ferroelectric layer.

$$\eta = 1 + \Delta \tag{9.2}$$

$$\Delta = \sum C_{channel-ground}/C_{channel-gate} \tag{9.3}$$

$$\Delta = \frac{-C_{Si}C_{Dep}|C_{Fe}|}{C_{ox}\left(C_{Dep}C_{Si} - |C_{Fe}|C_{Dep} - |C_{Fe}|C_{Si}\right)} \tag{9.4}$$

To have a body factor less than one ($\eta < 1$), Δ must be a negative quantity, and for stability reasons, Δ must satisfy the condition in (9.5):

$$-1 < \frac{-C_{Si}C_{Dep}|C_{Fe}|}{C_{ox}\left(C_{Dep}C_{Si} - |C_{Fe}|C_{Dep} - |C_{Fe}|C_{Si}\right)} < 0 \tag{9.5}$$

For $C_{Fe} < 0$ and $C_{Si}C_{dep} > |C_{FE}|(C_{Dep} + C_{Si})$ the portion $0 < \frac{C_{Si}C_{Dep}|C_{Fe}|}{C_{ox}(C_{Dep}C_{Si} - |C_{Fe}|C_{Dep} - |C_{Fe}|C_{Si})} < 1$ is attenuated to be less than zero, leading to a body-factor (η) ranged between 0 and 1. A second stability condition can also be derived from (9.5) shown in (9.6) where we have:

$$|C_{Fe}| < \sum\{C_{Si}, C_{Dep}, C_{ox}\} \tag{9.6}$$

This condition of $0 < \eta < 1$ yields to a sharper subthreshold slope. *S* can be written as:

$$S = 2.3\frac{kT}{q}\left(1 + \frac{\sum C_{channel-ground}}{C_{ox}}\right) \tag{9.7}$$

$$S = 2.3\frac{kT}{q}\left(1 - \frac{C_{Si}C_{Dep}|C_{Fe}|}{C_{ox}\left(C_{Dep}C_{Si} - |C_{Fe}|C_{Dep} - |C_{Fe}|C_{Si}\right)}\right) \tag{9.8}$$

The proposed body stack requires careful adjustments of the thickness to keep the body factor in between 0 and 1 ($0 < \eta < 1$). This can be accomplished by satisfying the stability condition derived earlier. The subthreshold swing and the threshold voltage depend on gate dielectric material (gate oxide), doping profile that determines the depletion width, and dielectric permittivity of the ferroelectric and buffer materials. In this research, the derived models are simplified by ignoring the effect of the buffer layer on the device operation. We considered it as an extension to the ferroelectric layer. Therefore, the buffer layer must be charge-neutral and chemically inactive towards silicon and ferroelectric material.

A small gate-to-source voltage creates a voltage V_{FE} in between C_{Si} and C_{Fe}, where $C_{Fe} = \varepsilon_{Fe}/t_{Fe}$ is the ferroelectric material capacitance per unit area, t_{Fe} is the thickness of the ferroelectric film, and ε_{Fe} is the permittivity of ferroelectric material. The subthreshold swing of the proposed PD-SOFFET depends on several parameters. The most

significant parameters are the thicknesses of the ferroelectric film, the depleted silicon film, and the gate oxide. The developed model in (9.8) is based on the approximation that the impact of the unipolar junctions between the top plate of the negative capacitance and the diffusion areas (drain and source) can be ignored due to their minor effect on overall device operation.

9.5.2 Threshold voltage of the proposed PD-SOFFET

The capacitances of Figure 9.1 can be used to derive a model for the threshold voltage of the proposed PD-SOFFET. First order approximation of V_{TH} is illustrated in (9.9) – (9.12). From the derived model (9.12), it is observed that the threshold voltage of the proposed PD-SOFFET depends also on the thickness of the ferroelectric material.

$$\psi_S = \frac{C_{ox}}{C_{ox} + \sum C_{channel-ground}} (V_G - V_{FB}) \tag{9.9}$$

$$V_G = \psi_S \left(1 + \frac{\sum C_{channel-ground}}{C_{ox}}\right) + V_{FB} \tag{9.10}$$

$$V_{TH} = V_G|_{\psi_S = 2\psi_b} \tag{9.11}$$

$$V_{TH} = 2\frac{KT}{q} ln(N_A/n_i) \left(1 + \frac{\sum C_{channel-ground}}{C_{ox}}\right) + V_{FB} \tag{9.12}$$

Here $\psi_b = \frac{KT}{q} ln(N_A/n_i)$ is the difference between Fermi and intrinsic levels. When $V_{GS} > V_{TH}$ (n-type FET), the semiconductor/oxide interface is inverted (inversion layer is formed). Here, $V_{FB} = \psi_{MS} - Q_{ss}/C_{ox}$ is the flat band voltage, Q_{ss} is the surface

state charge of the channel, $\psi_{MS} = \psi_{Si} - \psi_F = \frac{-E_g}{2} - \psi_F$ is the work function difference between the gate and the channel, $\psi_F = \frac{kT}{q} ln(N_A/n_i)$ is the Fermi potential, and E_g is the silicon energy band gap.

9.6 SOFFET Design Parameters and I-V Characteristic

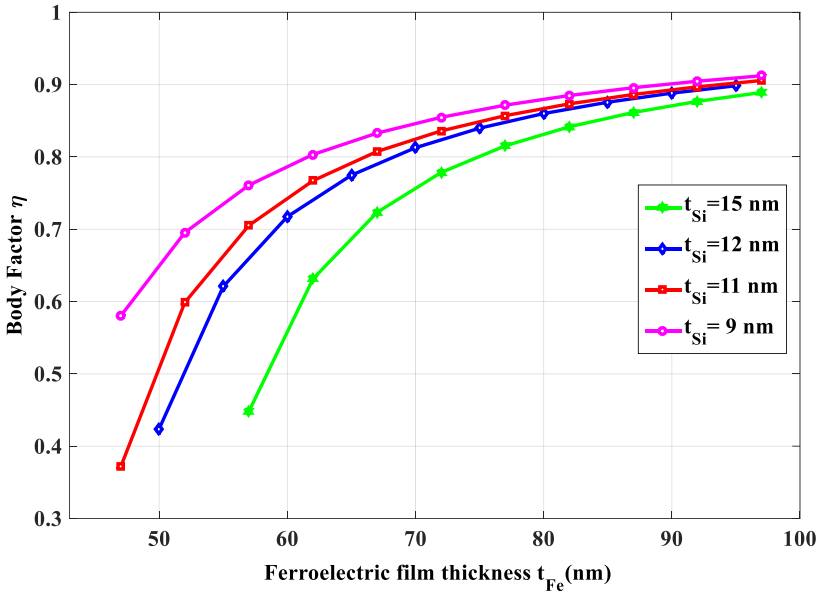
9.6.1 Different design parameters

The goal is to achieve lower threshold voltage (V_{TH}) and subthreshold swing (S) in the proposed PD-SOFET of Figure 9.1. From the derived models of (9.8) and (9.12), it can be observed that there are several elements that can be adjusted for this purpose. The key factors are the thickness of the ferroelectric film (t_{Fe}), the thickness of the depleted thin silicon film (t_{Si}) above the ferroelectric insulator, the thickness of the gate oxide (t_{ox}), and the doping profile (N_A). To break the thermodynamic limit of $S = 60mV/decade$, the body-factor must be less than 1 ($0 < \eta < 1$). By selecting these parameters carefully, the value of the body-factor can be decreased.

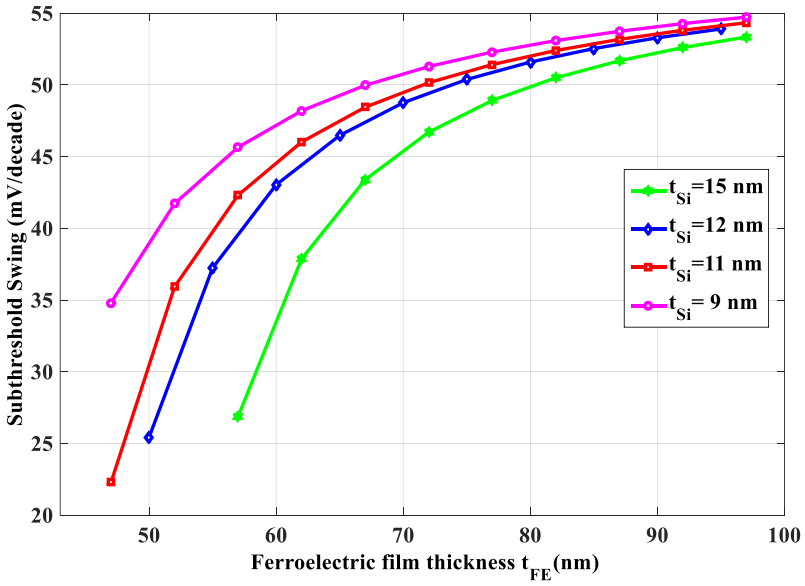
Equation (9.8) indicates that decreasing the depleted silicon capacitance and increasing the oxide capacitance are two possibilities. However, the thickness of the ferroelectric material must be selected carefully to maintain a stable device. The depleted thin silicon film (t_{Si}) and the ferroelectric film thickness (t_{Fe}) are two parameters that can be tuned to manage the device stability. From Figure 9.2, it is observed that the structure

requires a thicker silicon and thinner ferroelectric material to achieve a lower body-factor, leading to lower values of S and V_{TH}.

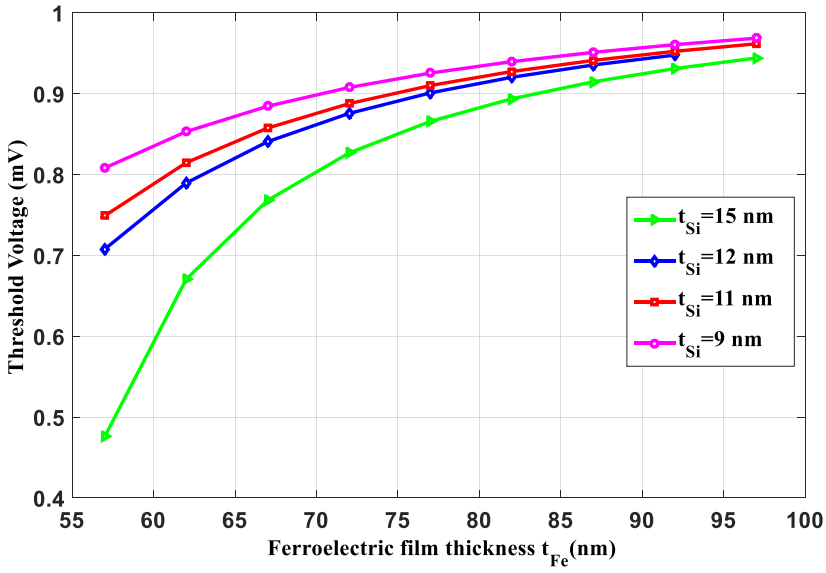
The subthreshold behavior of the proposed device also depends on the depletion layer width W_D, which depends on the channel doping N_A. A numerical simulation of uniform channel doping N_A versus subthreshold swing is shown in Figure 9.3.a. It is observed that lower values of S can be achieved at lower channel doping in the proposed device. This is beneficial in lowering short-channel-effect (SCE). The ability to maintain a lower doping profile in the proposed device will limit the effect of non-uniform lateral doping of short-channel devices, thereby decreasing the off-state current. Low doping also removes excessive random dopant fluctuations (RDF) and eliminates the issue of significant device-to-device threshold voltage variations. Figure 9.3.b demonstrates that at $t_{Fe} = 65nm$, large gate oxide thickness t_{ox} reduces S. However, small t_{ox} is required to have better electrostatic and control over the channel. For $t_{ox} = 2nm,\ S < 20mV/decade$ can be obtained.


Body Factor η
Ferroelectric film thickness t_Fe (nm)
t_Si=15 nm
t_Si=12 nm
t_Si=11 nm
t_Si= 9 nm

(a)

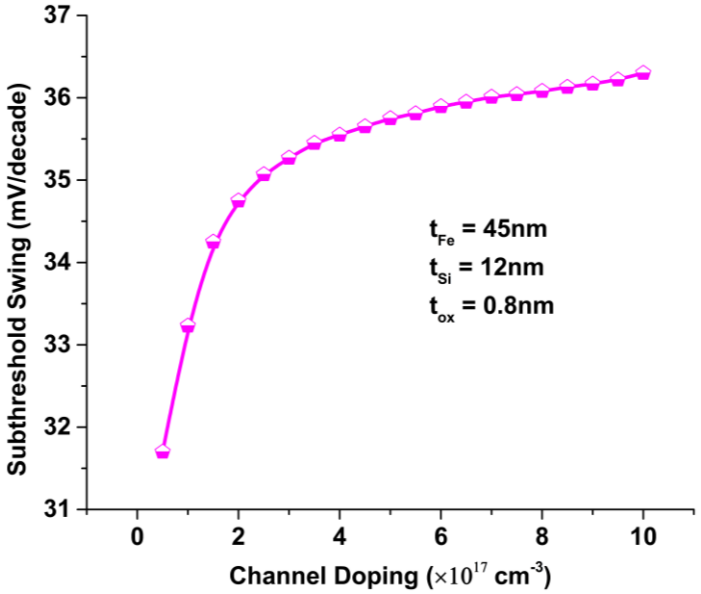

Subthreshold Swing (mV/decade)
Ferroelectric film thickness t_FE (nm)
t_Si=15 nm
t_Si=12 nm
t_Si=11 nm
t_Si= 9 nm

(b)

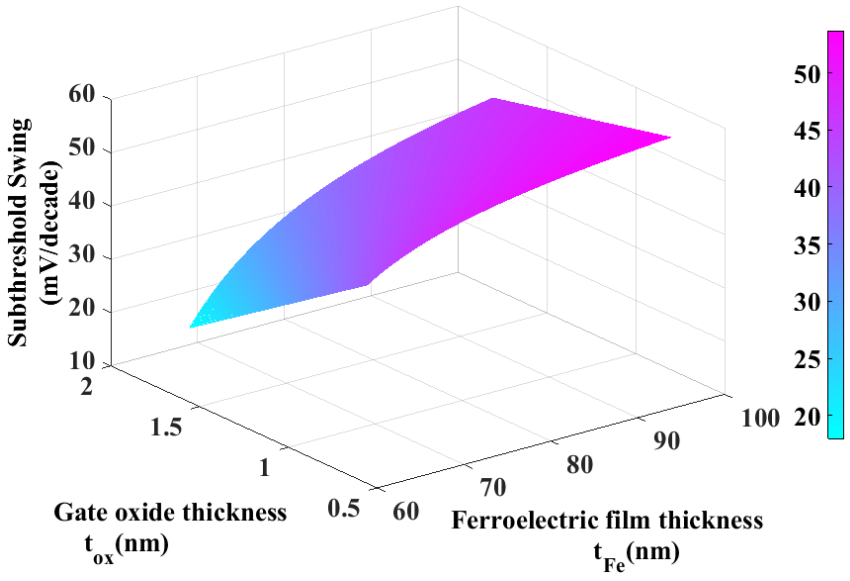


(c)

Figure 9.2: Plot of the a) Body factor, b) Subthreshold swing, and c) Threshold voltage for a t_{Fe} vary from $55nm$ to $100nm$.



(a)



(b)

Figure 9.3: Plot of S: (a) at various channel doping; (b) at various t_{ox}/t_{FE} ratios and using SiO_2, $L = 22nm$, $N_A = 1\times10^{17}$, and $t_{ox} = 1nm$.

The impacts of gate insulator properties on the behavior of the proposed PD-SOFFET have also been investigated. Many promising *high-k* dielectric materials and various ferroelectric materials have been investigated recently for application in DRAM. Several parameters of these dielectric materials are presented in [131, 133]. Using *high-κ* gate oxide requires a thinner ferroelectric film to keep the body-factor in a practical range. However, SiO_2 can also be employed. Furthermore, technology scaling, fabrication process and variation of ferroelectric materials may restrict the use of certain gate oxide materials.

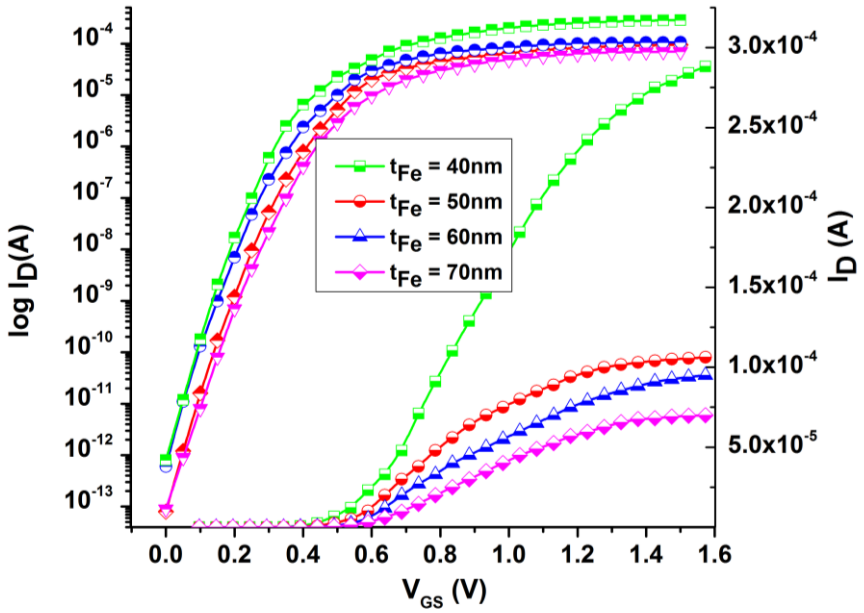


Figure 9.4: The transfer characteristic of the PD-SOFFET for $V_{GS} < V_{th}$, $V_{DS} = 0.05V, L = 22nm, W = 60nm, t_{ox} = 1nm, t_{Si} = 20nm, \varepsilon_{Fe} = 100$, and $N_A = 1\times10^{17}cm^{-3}$.

9.6.2 I_D vs. V_{GS} characteristic of PD-SOFFET

To understand the behavior and performance of the proposed PD-SOFFET, we have investigated the (I-V) characteristics of the device both in the subthreshold and in the saturation regions. For this, we have utilized the model used for SOI device, but the parameters are derived from the proposed device structure. An accurate model for the subthreshold operation of SOI-MOSFET is given in [134, 135]. The current is defined as in (9.13).

$$I_{Sub} = 2\mu C_{ox}\frac{W}{L}\left(\frac{KT}{q}\right)^2 |\eta - 1| \times exp\left(\frac{V_{GS} - V_{TH}}{\eta KT/q}\right)\left[1 - exp\left(-\frac{V_{DS}}{KT/q}\right)\right] \qquad (9.13)$$

Where *W* and *L* are the dimensions of the device, V_{TH} is the threshold voltage, and η is the body factor. Correspondingly, the body-factor calculated to be $\eta = 0.33$ and the subthreshold swing is $S = 19.9mV/decade$ *(for* $l = 22nm, W = 60nm, t_{ox} = 1nm, t_{si} = 20nm,\ t_{Fe} = 65nm,$ and $\varepsilon_{Fe} = 100$). Equations (9.4) – (9.8) are used to calculate η and S. The subthreshold region (I-V) characteristic ($I_{DS} - V_{GS}$) of the PD-SOFFET device is shown in Figure 9.4. For a threshold voltage of $0.2V$ and body-factor $\eta = 0.33$, off-current ($V_{GS} = 0V$) is about $1\mu A/\mu m$ (note that the leakage current depends on how fast the ferroelectric capacitor can help evacuate the carriers of the channel). This simulation also shows that the device derives a current of $1.6\mu A/\mu m$ at the threshold voltage ($V_{th} = V_{GS}$).

9.7 Curie Temperature of the Body Stack

Ferroelectric materials switch to paraelectric when the temperature is higher than the Curie temperature T_C, above this temperature no ferroelectricity is observable. The main goal here is to keep this insulator operating under Curie temperature, where we can have the hysteresis phase transitions. A composite of ferroelectric material and a buffer layer with high dielectric constant stabilize the dielectric constant. Semiconductor devices used in ultra-low-power designs are operating in temperatures up to 85℃ (for industrial

applications and lower than that for commercial applications). This margin allows for a wide range of ferroelectric materials to be integrated into the nanotechnology. Several materials have a Curie temperature around $650°K$ ($\sim 376℃$). Under this temperature, these materials operated in ferroelectric phase. To explain the phase transitions in the ferroelectric material, Landau model (non-linear) is employed. The Landau model (non-linear) is also proposed to describe the phase transitions temperature dependency, and a qualitative change of the capacitive regime. The influence of the temperature on the ferroelectric material is précised in Landau theory. Because the negative capacitance required for this design may not be stable due to the electric field applied and the temperature, a stability model has to be considered. Landau's theory provides a general framework for the study of phase transitions [84]. The behavior of the ferroelectric material is pronounced in the thermodynamic theory that applies Taylor series expansion of the free energy F which can be developed into series of powers of polarization P. F can be read as follows (only the first two terms are considered here).

$$F = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 \tag{9.14}$$

Where α, and β are coefficient depend on the temperature. The coefficient α is inversely proportional to the permittivity ε_{Fe}

$$\varepsilon_{Fe} \propto \frac{C_{CW}}{T - T_C} \tag{9.15}$$

Where C_{CW} is the Curie-Weiss constant, T is the temperature and T_C is Curie temperature. A model for the dielectric permittivity, as derived in [84], is presented in (9.16)

$$\varepsilon_{Fe} = \frac{1}{\varepsilon_0 \alpha} = \lambda \frac{C_{CW}}{T - T_C} \quad with \begin{cases} \lambda = -\frac{1}{2} & T < T_C \\ \lambda = 1 & T > T_C \end{cases} \tag{9.16}$$

Where ε_0 is the vacuum dielectric permittivity, and C_{CW} is the Curie-Weiss constant. Depending on the phase paraelectric or ferroelectric, the sign of α could be positive or negative. A model was developed by Salvatore based on Landau's theory. This model demonstrates that the subthreshold and the inversion regions have their maximum and minimum respectively, of its trans-conductance and subthreshold swing at the Curie temperature T_C due to the divergence of the ferroelectric permittivity at T_C [136]. To find the Curie temperature, the application of conventional methods of thermodynamics theory allows the determination of the changes in permittivity and spontaneous polarization as a function of temperature. Due to the continuity of the depletion layer, which caused by the partially depleted arrangement, both C_{Fe} and C_{Si} potentials are roughly stood in series (if we neglected the effect of the buffer layer). The charge per unite area Q_{Fe} caused by ferroelectric polarization P is written as $Q_{Fe} = C_{Fe}V_{Fe}$, using capacitive divider to determine V_{Fe} (Figure 9.1):

$$Q_{Fe} = C_{Fe}V_{Fe} = \frac{|C_{FE}|^2 C_{Si} C_{Dep}}{C_{Fe}C_{Si} + C_{Fe}C_{Dep} + C_{Si}C_{Dep}} \psi_S \tag{9.17}$$

$$Q_{Fe} = C_{Fe} \sum C_{channel-ground}\, \psi_S$$

$$Q_{Fe} = -\frac{C_{ox}^2 |C_{FE}| C_{Si}}{C_{ox}^2 (C_{Si} - |C_{Fe}|) - C_{Si}|C_{Fe}|} V_G \qquad (9.18)$$

Since with positive gate voltage, the ferroelectric capacitance charges decreases (ferroelectric proprieties), we can decide a third stability condition: $|C_{FE}| < \sum\{C_{Si}, C_{Dep}, C_{ox}\}$.

Here, an indication that the stability condition '1' is related to Curie-Weiss temperature can be seen by:

$$\sum\{C_{Si}, C_{Dep}, C_{ox}\} > |C_{FE}| = \frac{\varepsilon_{Fe}}{t_{Fe}} = \lambda \frac{C_{CW}}{t_{Fe}(T - T_C)} \qquad (9.19)$$

CHAPTER 10

FULLY DEPLETED SILICON-ON-FERROELECTRIC INSULATOR FET

The proposed structure of SOFFET can have two variants – fully depleted and partially depleted SOFFET. In this chapter, we considered the fully depleted approach where in chapter 9 we have studied partially depleted device. We explored the possibility of having a $sub - 60mV/decade$ device by positioning a ferroelectric layer on top of the silicon substrate in fully depleted configuration.

10.1 Introduction

In the previous chapter, we proposed a new $Sub - 60mV/decade$ device named PD-SOFFET. The structure of the device is very similar to PD-SOI MOSFET. The differences are in terms of the properties and the roles of the buried layer inside the silicon body of the transistor. In the proposed PD-SOFFET, a layer of ferroelectric material and a buffer material have replaced the buried silicon dioxide (SiO_2) of the SOI device. The ferroelectric material acts as an insulator, similar to the traditional SOI device, and provides an internal signal boosting through negative capacitance to make the subthreshold slope of the device steeper. The theoretical model shows that the device can operate at lower threshold voltage and a subthreshold swing below $60mV/decade$. This analysis shows

that the device V_{TH} and S depend on several factors, such as the thicknesses of the gate oxide, ferroelectric film and the depleted silicon, and the doping profile.

In this chapter, we extended the idea of extracting negative capacitance from partially depleted (PD) to fully depleted (FD). FD offers solutions to several issues facing the PD-SOI FET, like floating body and short-channel-effect. FD-SOI FET has better performance due to low doping that reduces random fluctuations, elimination of kink effect, and a higher on-current. Because of this, we considered investigating the device performance after we substituted the buried oxide with a ferroelectric insulator.

10.2 Fully Depleted Silicon-on-Ferroelectric Insulator Field Effect Transistor

This chapter presents a concept of a new transistor design using a ferroelectric insulator embedded in a silicon substrate. The construction of this new device is similar to a silicon-on-insulator (SOI) device. We propose to replace the buried silicon dioxide (SiO_2) insulator layer in an SOI device with a layer of ferroelectric insulator and a layer of thin film buffer insulator. The proposed device is named ***Fully Depleted Silicon on Ferroelectric Insulator Field-effect-transistor (FD-SOFFET)***. Figure 10.1 presents the concept and the physical construction of the proposed fully depleted SOFFET.

The primary idea of this design is to use ferroelectric decencies as a pre-existing boost for the device. The surface-trapped charges in the ferroelectric film can be collected to assist in channel formation by applying small gate voltage. Hence, a conducting channel can be formed by low gate voltage. To attain this concept, a thin layer of ferroelectric

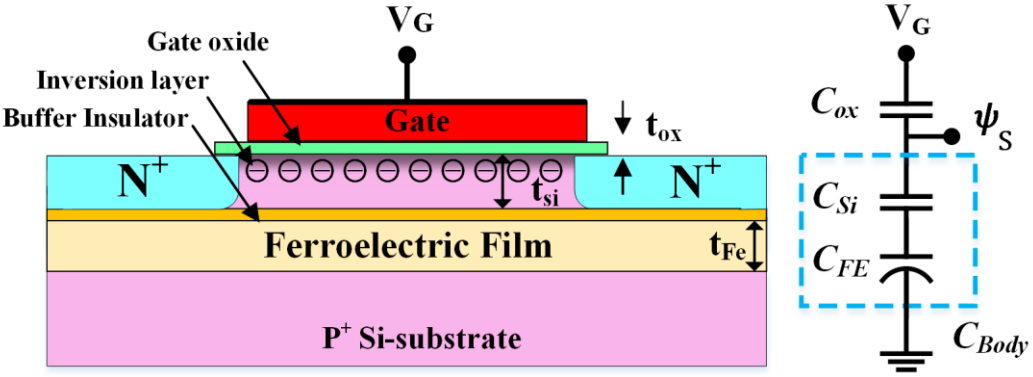


Figure 10.1: The Proposed SOFFET and its equivalent capacitive divider.

material is placed on top of the silicon substrate. This proposed design takes advantage of the extracted ferroelectric negative capacitance and SOI technology. The NC phenomenon has been displayed by a variety of electronic devices, both heterostructures and homostructures, made of crystalline and amorphous semiconductors. A ferroelectric insulator like $BaTiO_3$ exhibits hysteresis in *P-E* curve (polarization versus electric field curve, which is a scaled version of *Q-V* plot). The current studies focus on the dielectric permittivity enhancement of ferroelectric or near-ferroelectric composites like *lithium tantalite* ($LiTaO_3$), *barium titanate* ($BaTiO3$), and *lead magnesium niobate* ($Pb(Mg_{0.33}Nb_{0.77})O_3$). These types of materials can exhibit dielectric constants of a few hundred to a few thousand, enabling them to convey hysteresis needed for negative capacitance application [16, 137, 138]. The ferroelectric property of these materials is dependent on the operating temperature. The previous works on negative capacitance based

FET did not elaborate on this concern. It should be noted that, in this structure, we desired the same gate capacitance so that the same current drive can be achieved for the same capacitance. Furthermore, ferroelectric negative capacitance can only be stabilized in a certain range of temperatures. Electromechanical fatigue, coercive electric field, and Curie temperature transition behavior are still major research concerns in the field of ferroelectric materials processing and integration for nanoelectronic applications. In this structure, we proposed to use ferroelectric materials like $Bi_4Ti_3O_{12}$, which has many desirable properties such as fatigue-free, low processing temperature, low switching fields and low leakage current [139]. At room temperature, it has a dielectric constant of ~ 100 and the Curie temperature is reported to be 650°C [140, 141].

10.3 SOFFET Device Physics and Mode of Operation

The mode of operation of the SOFFET is illustrated in Figure 10.2. By applying a positive gate voltage less than threshold voltage, the electrons start their attraction toward the gate insulator. Correspondingly, the ferroelectric film helps to develop the channel at low voltage. The polarity of the upper plate of the negative capacitance repulses the electron toward constructing the channel. The electrons need less energy to move from the valence band to the conduction band. Reasonably, using a bottom gate requires a voltage to be connected to it. Nevertheless, using a ferroelectric layer ensures the same concept of double gate devices. The ferroelectric film provides a bias supply to the device that could

be considered a bottom gate. Figure 10.2 displays the concept of switching. Similarly, switching OFF requires terminating the gate voltage, causing the surface potential (channel voltage) to converge to zero. Therefore, the negative capacitance will be disconnected and the device completely OFF.

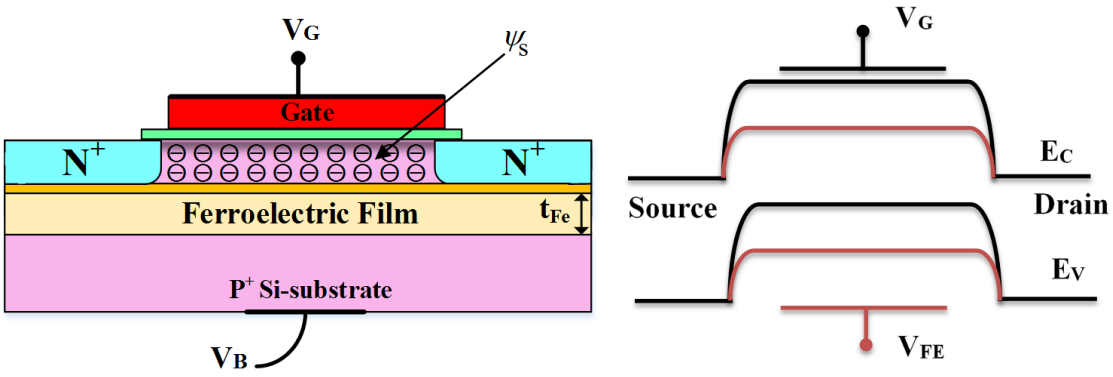


Figure 10.2: SOFFET band diagram for $0 < V_G < V_{TH}$ and $V_{FE} > 0$. Gate voltage attracts electrons and pushes holes away. Similarly, the ferroelectric film repulses electrons to the top of the silicon. Hence, n-type channel is formed promptly and SOFFET transistor begins to conduct.

10.4 Subthreshold Behavior of Proposed SOF-FET

Subthreshold Swing 'S' is defined as the amount of gate voltage required for one-decade change of the drain current. A Smaller value of S gives a better turn-on performance of a device because the smaller value of S means for a certain change in current we will need lower gate voltage change, or for a certain change in voltage we can get higher current

change, leading to larger gain of the device. The lower value of S is achievable only if the oxide thickness in the silicon device approaches to zero. However, under any practical scenario, this is not possible, and the value of S is dependent on the body factor (η), which is always larger than 1 ($\eta > 1$). If, under an ideal scenario, we can set $\eta = 1$, the theoretical minimum value of S for the silicon devices, including the conventional and emerging MOSFET is $S_{min} = 60mV/decade$ due to non-scaling of the thermal voltage "kT/q". Typically, the value is larger than $60mV/decade$ (in the range of $80 - 120mV/decade$). But for ultra-low-power operation, obtaining a lower value of S is the prime requirement that needs a new design and material alternatives to the traditional bulk silicon devices.

10.4.1 Subthreshold swing of SOF-FET

From the equivalent capacitance of Figure 10.1, we can calculate the body factor of the SOFFET as shown in (10.1). Where $\varkappa$ expressed in (10.2), represents the ratio of C_{Body}/C_{ox}, C_{Body} represents the series association of C_{si} and C_{Fe}, and C_{Fe} represents the negative capacitance extracted by integrating a thin ferroelectric layer.

$$\eta = 1 + \varkappa \tag{10.1}$$

$$\varkappa = \frac{C_{Body}}{C_{ox}} = \frac{C_{Si}C_{Fe}}{C_{ox}(C_{Si} + C_{Fe})} = -\frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si} - |C_{Fe}|)} \tag{10.2}$$

To obtain body factor less than one ($\eta < 1$) $\varkappa$ must be negative quantity, and for stability reasons, $\varkappa$ must satisfy the condition in (10.3):

$$-1 < -\frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si} - |C_{Fe}|)} < 0 \tag{10.3}$$

For $C_{Fe} < 0$ and $C_{Si} > |C_{Fe}|$, the portion $0 < \frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si}-|C_{Fe}|)} < 1$ attenuate to be less than zero, leading to a body factor (η) ranged between 0 and 1. The second stability condition can also be derived from (10.3) and this is shown in (10.4):

$$\frac{C_{Si}}{C_{ox}} < \frac{C_{Si} - |C_{Fe}|}{|C_{Fe}|} = \frac{C_{Si}}{|C_{Fe}|} - 1 \rightarrow 0 < \frac{C_{Si}}{C_{ox}} < \frac{C_{Si}}{|C_{Fe}|} - 1 \tag{10.4}$$

This condition of $0 < \eta < 1$ yields to a sharper subthreshold slope. Since the device operation is similar to that of the MOSFET, this approach will lead to a subthreshold swing (S) much lower than $60mV/decade$. S can be written as:

$$\mathrm{S} = 2.3\frac{\mathrm{kT}}{\mathrm{q}}\left(1 + \frac{C_{Body}}{C_{ox}}\right) = 2.3\frac{\mathrm{kT}}{\mathrm{q}}\left(1 - \frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si} - |C_{Fe}|)}\right) \tag{10.5}$$

This design requires careful planning, where the thickness and the placement of the ferroelectric layer will control the subthreshold swing. By applying voltage to the gate of the device, a voltage V_{FE} in between C_{Si} and C_{Fe} formed, controlling the charges of C_{Fe}. The gate oxide capacitance is given by: $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ (here ε_{ox} is the permittivity of the oxide), and $C_{Fe} = \varepsilon_{Fe}/t_{FE}$ is the ferroelectric material capacitance per unit area (t_{FE} is the

thickness of the ferroelectric film, ε_{Fe} is the permittivity of ferroelectric material). The subthreshold swing of the proposed SOFFET depends on several parameters; the most significant is the thickness of the ferroelectric film, the depleted silicon, and the gate oxide. The developed model in (10.5) is based on the approximation that the impact of the unipolar junctions between the top plate of the negative capacitance and the diffusion areas (drain and source) can be ignored due to their minor effect on overall device operation.

10.4.2 Threshold voltage of SOF-FET

The equivalent capacitances of Figure 10.1 can be used to derive a model for the threshold voltage of the proposed SOFFET. A first order approximation of V_{TH} is illustrated in (10.6) – (10.9). From (10.9), it is observed that the threshold voltage of the proposed SOFFET depends on the thickness of the ferroelectric material.

$$\psi_S = \frac{C_{ox}}{C_{ox} + C_{Body}} (V_G - V_{FB}) \tag{10.6}$$

$$V_G = \psi_S \left(1 + \frac{C_{Body}}{C_{ox}}\right) + V_{FB} \tag{10.7}$$

$$V_{TH} = V_G|_{\psi_S = 2\psi_b} \tag{10.8}$$

$$V_{TH} = 2\frac{KT}{q} \ln(N_A/n_i) \left(1 + \frac{C_{Body}}{C_{ox}}\right) + V_{FB} \tag{10.9}$$

Here $\psi_b = \frac{KT}{q} ln(N_{Si}/n_i)$ is the difference between Fermi and intrinsic levels. When $V_{GS} > V_{TH}$ (*n-type* FET), the semiconductor/oxide interface is inverted (inversion layer is formed), and E_g is the silicon energy band gap. V_{FB} is the flat-band voltage. A model

proposed by C. Ravariu *et al* [142, 143] was adopted: $V_{FB} = -\frac{Q_{FE}}{2C_{FE}}t_{FE} - \frac{Q_{FE}^2}{2q\varepsilon_{Si}N_{SUB}} + \frac{KT}{q}\ln\frac{N_{SUB}N_{Si}}{n_i^2} + \Phi_{MS}$, where N_{Si} is the doping concentration in the silicon film, N_{SUB} is the doping concentration in *p-type* silicon substrate, Φ_{MS} is the metal-semiconductor work-function ($\Phi_{MS} = 4.35\ eV$), and $C_{FE} = \varepsilon_{FE}/t_{FE}$ is the extracted negative capacitance.

10.4.3 Impacts of ferroelectric film thickness

From the derived models (10.5) and (10.9), it can be observed that there are several factors that can be adjusted to lower the threshold voltage and the subthreshold swing. Equation (10.5) indicates that depressing the depleted silicon and increasing the oxide capacitance are two possibilities. However, the thickness of the ferroelectric material has to be selected carefully to maintain a stable device. The depleted thin silicon film (t_{Si}) and the ferroelectric film thickness (t_{FE}) are two parameters that can be adjusted to manage the device stability. Figure 10.3 presents the dependency of the body-factor, subthreshold, and threshold voltage.

Normally, the applied gate voltage inverts the doping of silicon directly under the gate to form a channel between the source and drain. The trapped charges in the ferroelectric material will help form the channel at a lower voltage. Smaller thickness of the ferroelectric film gives higher negative capacitance ($\mathrm{C_{FE}} = \varepsilon_{\mathrm{FE}}/\mathrm{t_{FE}}$), leading to higher trapped charge in the film. This helps the creation of the channel at a lower V_{TH}. With

thicker ferroelectric film, the device will behave like a regular SOI device, where the ferroelectric material and buffer insulator will serve as a low conducting material. This will increase both V_{TH} and S. When the device is turning OFF, the ferroelectric capacitance starts collecting charge from the channel. This quick evacuation improves the device's turn OFF speed. These trapped charges in the ferroelectric capacitance will again support the channel establishment when the device switches back to on-state.

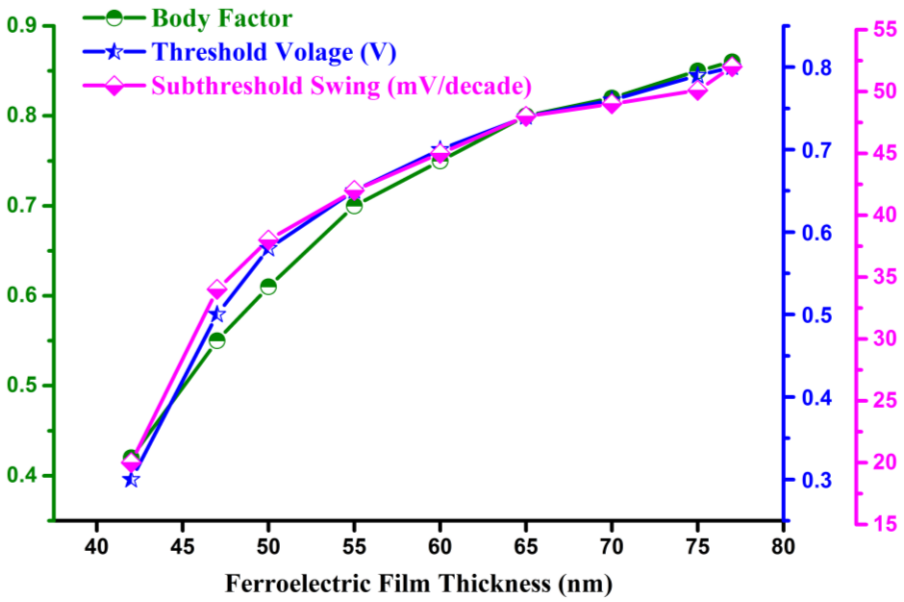


Figure 10.3: The Plot of the Body factor, Subthreshold swing, and Threshold voltage for a t_{FE} vary from $40nm$ to $75nm$, channel length $L = 22nm$, channel width $W = 60nm$, gate oxide thickness $t_{ox} = 1nm$, channel doping $N_{Si} = 1\times10^{17}cm^{-3}$, substrate doping $N_{Sub} = 1\times10^{17}cm^{-3}$, and ferroelectric dielectric constant of $\varepsilon_{Fe} \approx 100$ (at room temperature).

10.4.4 Impacts of channel doping.

From (10.5) and (10.9), it can be deduced that the subthreshold swing and the subthreshold voltage of the proposed device are dependent on the doping profile of the channel. The thickness of the depletion layer also depends on the doping level. A lower doping will cause a thicker depletion layer, and produce in a higher depletion capacitance $\left(W_{dep} \propto \sqrt{\frac{1}{N_A}}\ \&\left(C_{dep} \propto \sqrt{N_A}\right)\right)$. Hence, the magnitude of the body factor will decrease, resulting in an increase of subthreshold swing, because in the proposed device we have to make sure that the body-factor remains between 0 and 1 by ensuring the following conditions: $-1 < \varkappa = -\frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si}-|C_{Fe}|)} < 0$. A numerical simulation of the various doping profile is presented in Figure 10.4 to observe its effect on the value of S. It can be seen that the device will have a better operation with low doping profile. This is a significant advantage compared to the conventional and other FETs. Ability to maintain a lower doping profile in the proposed device will limit the effect of non-uniform lateral doping of short-channel devices, thereby decreasing the off-state current. Low doping also removes excessive random dopant fluctuations (RDF) and eliminates the issue of significant device-to-device threshold voltage variations.

10.4.5 Impacts of various design elements

From (10.5) and (10.9), it can be deduced that the subthreshold swing and the subthreshold voltage of the proposed device are dependent on the gate oxide thickness, the ferroelectric film thickness, and the depleted thin silicon film. These elements are engineered to prompt the channel formation, therefore the sharpness of the subthreshold slope. If the thicknesses of the elements mentioned before are selected cautiously, the magnitude of the body-factor will decrease. A numerical simulation of these elements and their impact on the subthreshold swing is presented in Figure 10.5.

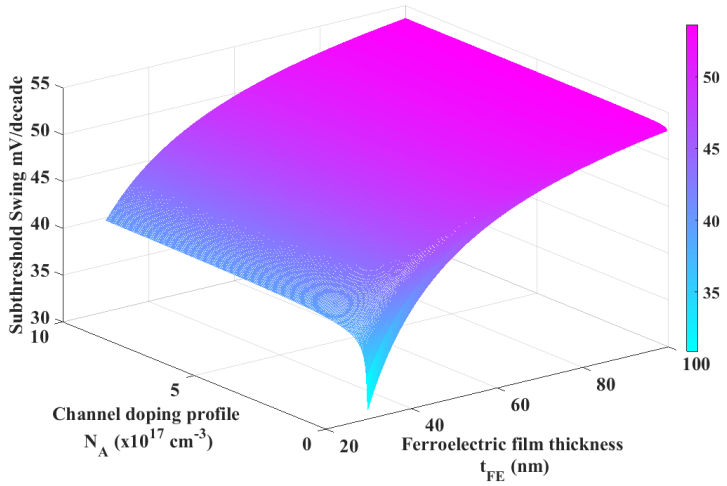
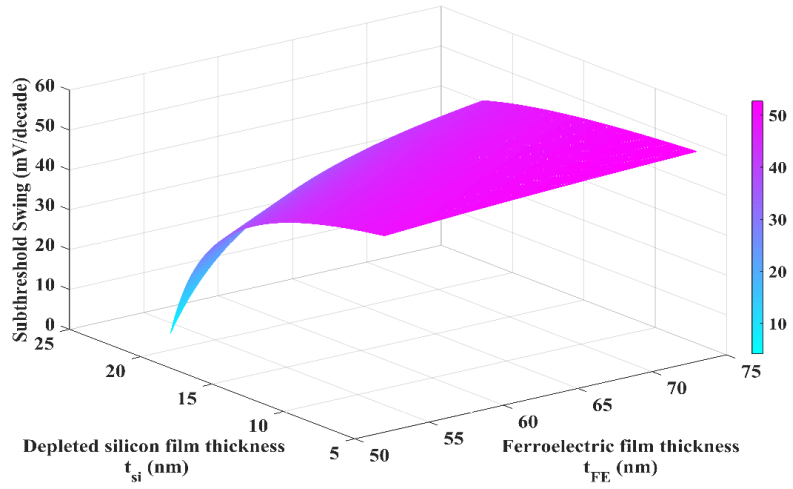
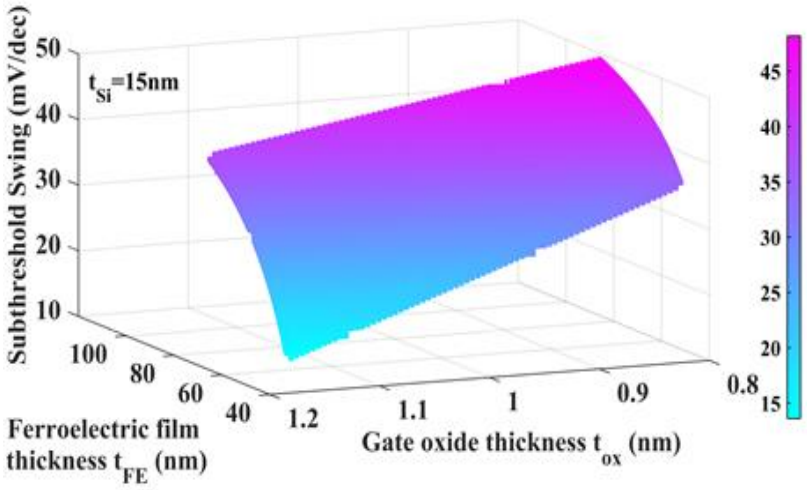


Figure 10.4: Numerical simulation of the subthreshold swing and its dependencies on the channel doping N_A and ferroelectric film thickness t_{FE}.



(a)



(b)

Figure 10.5: Plot of S a) At various t_{Si}/t_{FE} ratios and b) At various t_{ox}/t_{FE} ratios, using SiO_2, for channel length $L = 22nm$, channel width $W = 60nm$, substrate doping $N_{Sub} = 1{\times}10^{17}cm^{-3}$, and ferroelectric dielectric constant of $\varepsilon_{Fe} \approx 100$ (at room temperature).

Figure 10.5.a demonstrates that a large thickness of the depleted silicon film improves S. This enhancement is limited by the first stability condition presented in (9.4). It can be seen from Figure 10.5.b that the t_{Si}/t_{FE} ratio must be greater than 2 for a lower S. In this case, a subthreshold swing less than $5\ mV/decade$ can be obtained. This is a significant advantage compared to conventional and other emerging technologies.

10.4.6 Impact of gate insulator on the device operation

The impacts of the gate insulator property on the behavior of the proposed SOFFET have been investigated. Figure 10.5.c shows how the ferroelectric capacitance ($C_{Fe} = \varepsilon_{FE}/t_{FE}$) and the gate oxide capacitance (ε_{ox}/t_{ox}) were adjusted to realize a practical body-factor for a stable device. Many promising *high-k* dielectric materials and various ferroelectric materials have been investigated recently for application in DRAM. Using *high-k* gate oxide requires a thinner ferroelectric film to keep the body-factor in a realistic range. However, SiO_2 can also be employed. The simulation for SiO_2 is shown in Figure 10.5.c. In this case, a thicker ferroelectric film is needed to accomplish a practical body-factor, hence a low subthreshold swing. Furthermore, technology scaling, fabrication process and variation of ferroelectric materials may restrict the use of certain gate oxide materials.

10.4.7 Current-voltage (I-V) characteristics of SOFFET

To understand the behavior and performance of the proposed SOFFET, we investigated the (I-V) characteristics of the device in both subthreshold regime and saturation regime. For this, we have utilized the model used for SOI devices, but the parameters are derived from a SOFFET structure. An accurate model for the subthreshold operation of SOI-MOSFET is presented in [134, 135]. The current at that region is defined in (10.10).

$$\mathrm{I_{Sub}} = 2\mu \mathrm{C_{ox}} \frac{\mathrm{W}}{\mathrm{L}} \left(\frac{\mathrm{KT}}{\mathrm{q}}\right)^2 |\eta - 1| \exp\left(\frac{\mathrm{V_{GS}} - \mathrm{V_{TH}}}{\eta \mathrm{KT/q}}\right) \left[1 - \exp\left(-\frac{\mathrm{V_{DS}}}{\mathrm{KT/q}}\right)\right] \qquad (10.10)$$

Where W and L are the dimensions of the device, V_{TH} is the threshold voltage and η is the body factor. The body-factor that determines the slope of the characteristic of the device in the subthreshold region is calculated to be $\eta = 0.3$ for $t_{FE} = 45nm$ and the subthreshold swing is found to be $S = 23mV/decade$. The subthreshold region characteristic of the SOFFET device is shown in Figure 10.6. The off-state current ($V_{GS} = 0V$) is ~0.1 $pA/\mu m$ (note that the leakage current depends on how fast the ferroelectric capacitor can promote carriers' subtraction in the channel).

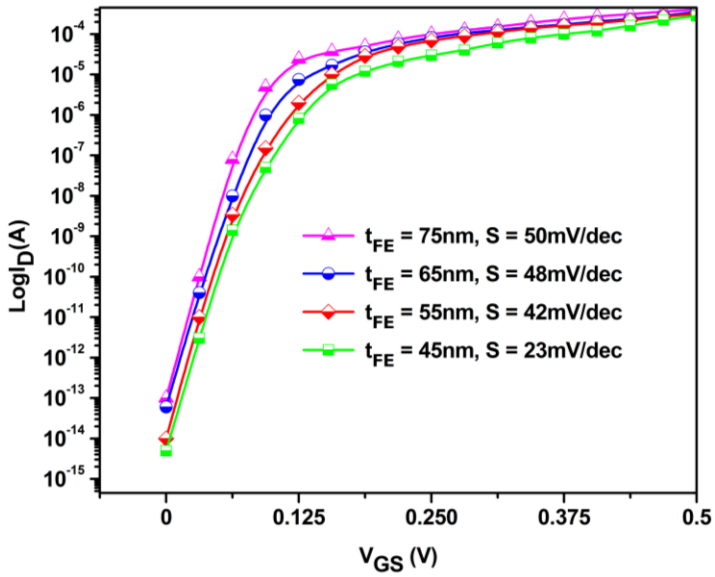


Figure 10.6: The transfer characteristic of the SOFFET for $V_{GS} < V_{th}$, $V_{DS} = 0.05V, L = 22nm, W = 60nm,$ $t_{ox} = 1nm, t_{Si} = 20nm$ and $\varepsilon_{Fe} = 100$, $N_{Si} = 1\times10^{17}cm^{-3}$, and $N_{Sub} = 1\times10^{17}cm^{-3}$.

10.4.8 Linear and saturation region

A model of saturation drain current of FD-SOI MOSFET is proposed by (10.11) [120]:

$$\mathrm{I_{Dsat}} = \frac{1}{2\eta}\mu\mathrm{C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}(\mathrm{V_{GS}} - \mathrm{V_{TH}})^2(1 + \lambda(\mathrm{V_{DS}} - \mathrm{V_{Dsat}})) \qquad (10.11)$$

Where θ is the mobility reduction factor.

The (I-V) characteristic of the proposed device is presented in Figure 10.7 for different body factor values. The simulation shows the dependency of the drain current on the body-

factor. Note that as η increases, the drain current decreases significantly. It is observed that like conventional FET, the current initially increases linearly after the threshold voltage, and then the device becomes saturated. The figure also demonstrates that the device provides a large on-state current for small body-factor. The saturation current of this device is of $\sim 200\mu A/\mu m$ for $t_{Fe} = 45nm$. Notice also that different body factors give various threshold voltages and on-state current. Another observation is the ability of the device to saturate early.

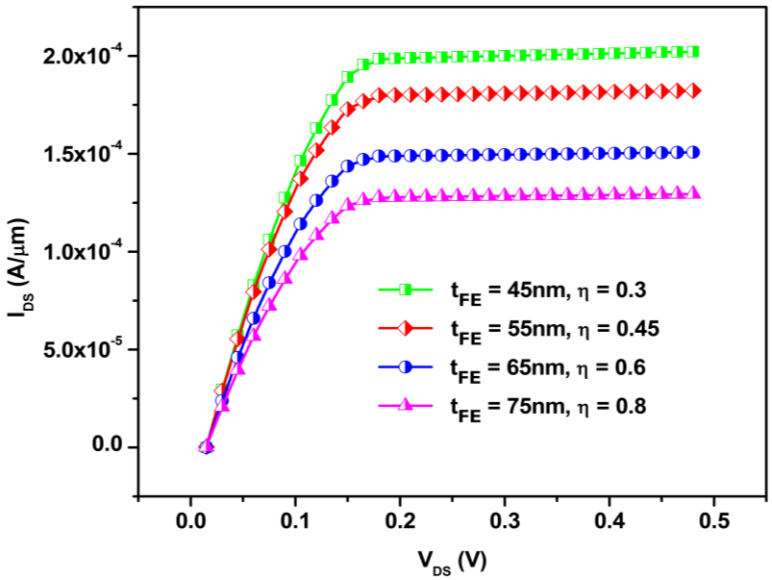


Figure 10.7: (I-V) characteristic and the impact of the body-factor on drain current, $L = 22nm, W = 60nm, \quad t_{si} = 20mn, t_{ox} = 1nm, \quad V_{th} = 0.2V,$ $\varepsilon_{Fe} = 100, \varepsilon_{ox} = 3.9, \theta = 10^{-2}V^{-1}, N_{Sub} = 1\times10^{17}cm^{-3} \quad , \quad N_{Si} = 1\times 10^{17}cm^{-3}$, and $\frac{kT}{q} \approx 60mV\ @RT$.

10.5 Discussion and conclusion

In this chapter, we have presented a new approach to integrating the ferroelectric material into field effect transistors to achieve a negative capacitance. As opposed to the previously proposed gate-stack negative capacitance device, we have introduced a new concept of SOI device with a body-stack ferroelectric negative capacitance. All the Ferroelectric Field Effect Transistors (FeFETs) and negative capacitance FETs (NCFETs) that are currently under investigation are based on the concept of replacing the gate insulator (SiO_2) in the conventional MOSFET with a ferroelectric insulator. However, many recent works have pointed out some serious challenges and reliability issues in these FeFET and NCFET structures. The problems with these device structures are that the ferroelectric materials are very unstable and temperature sensitive. Therefore, using it directly as the gate insulator would make the device very unreliable. Besides, in these devices, the problems of short-channel-effects, substrate noise, device scaling and density would remain as severe as in the conventional bulk silicon MOSFET. Another severe issue is the fact that ferroelectric materials form a silicate layer due to the chemical interaction between the silicon and the ferroelectric materials, which would seriously affect device properties if a ferroelectric insulator is placed at the gate. Therefore, the device geometry proposed in earlier FeFET and NCFET related research would not be feasible from both physical and electrical stability points of view. We concluded that utilizing the negative

capacitance in an SOI device structure is the best possible alternative to avoid the above-mentioned issues with the ferroelectric materials at the gate stack. The proposed SOFFET design, which utilizes the negative capacitance of a ferroelectric insulator in the body-stack, is completely different from the FeFET and NCFET designs. In addition to the NC effect, the proposed device will have all the advantages of an SOI device.

The body-stack that we are proposing in this work has many advantages over the gate-stack. First, it is more compatible with existing processes. Second, the gate and the working area of the proposed SOFFET is similar to the planar MOSFET. Third, the complexity and ferroelectric material interferences are shifted to the body of the device from the gate and the working area. The proposed structure offers better scalability and superior constructability because of the high-dielectric buried insulator. Here, we are providing a very simplified model for the structure. Silicon-on-ferroelectric leads to several advantages, including low off-current and shift in the threshold voltage with the decrease of the ferroelectric material thickness. Moreover, having an insulator in the body of the device increases the controllability over the channel, which leads to a reduction in the short-channel-effects (SCEs). The proposed SOFFET offers a low value of subthreshold swing (S), leading to better performance in the on-state. The off-state current is directly related to S, so the off-state current is also minimum in the proposed structure.

During the first 3 or 4 decades of the FET technology, the industry was solely focused on bulk MOSFET. When SOI technology was introduced in the 1990s by a simple modification of the device structure (burying a layer of insulator inside the body), a new generation of device technology was born and many issues of bulk MOSFET technology were solved. Similarly, when researchers started to introduce a new series of device technologies based on the negative capacitance of ferroelectric materials, the very first proposal was to put the ferroelectric material in the gate stack. However, gate-stack negative capacitance designs are facing some serious issues, as mentioned above. As all the contemporary researchers agree that negative capacitance is the answer to many of the issues of nanoelectronics, we need a better device design to utilize the negative capacitance. We anticipate that, if successful, the proposed SOFFET will bring transformative change in the way negative capacitance can be utilized in nanoelectronic devices. Therefore, our alternative to the previously proposed gate stack negative capacitance FET design may seem like a simple modification, but the proposed design has enormous potential. In this research, our attempt is to introduce this new concept and highlight its potential. There are many design and fabrication issues that need to be resolved.

CHAPTER 11

ADVANTAGES, MANUFACTURING PROCESS, AND FUTURE WORK OF THE PROPOSED DEVICES

11.1 Introduction

Since the middle of the last decade, the topic of $sub - KT/q$ or steep slope devices has emerged. Several materials as well as different physics are proposed for this post-silicon integration. Nano-electronics based on tunneling, I-MOS, and ferroelectric are considered to be promising alternative solutions to break the scaling limit of silicon industry that the industry may soon have to face. Leakage current and power supply is going to be a limiting factor for successive down-scaling of transistors. Due to smaller feature sizes, short-channel-effect also increases the leakage current of the transistor. To be able to continue power scaling both new materials and new device architectures become a necessity. Therefore, new architectures and/or materials were proposed and integrated in both channel and gate oxide.

Field-effect-transistor based on ferroelectric is a promising alternative solution to extend Moore's Law and continue the down-scaling path while avoiding the energy crisis. Recently, ferroelectric was proposed as an important candidate to merge in gate-stack of field-effect-transistors. Ferroelectric materials' high-dielectric and remnant polarization allow for a negative-region extraction known as negative capacitance (NC).

Extracting this NC gate of the device will boost the device switching speed and lower its power consumption.

Significant progress has been made in the investigation of emerging ferroelectric in nano-fabrication in recent years. Most of the gate structures use Metal Ferroelectric Insulator Semiconductor (MFIS) or metal–ferroelectric–metal–insulator–silicon (MFMIS) due to simplicity. However, ferroelectric-gate devices suffer from short-channel-effect, reduced gate voltage controllability, and increase the leakage current. Either MFIS or MFMIS has limited advantage like low subthreshold swing, but the main disadvantages are high off-state current and limited channel scaling. Poor device performance, due to inefficient gate control, was approached by numerous proposals. Several methods to improve these promising emerging nanomaterial integrations and take full advantage of its electrical properties to improve the electrostatic and to increase the I_{on}/I_{off} ratio while keeping I_{off} low. The Silicon-on-Ferroelectric field effect transistors exhibited significantly reduced subthreshold swing. Thus, integrating ferroelectric body insulators into the device structure is expected to enhance the device performance.

11.2 Advantages of the SOF-FET

Theoretically, we demonstrate that extracting a negative capacitance from ferroelectric materials inside the device body could boost the device subthreshold operations. This approach keeps the device operation similar to the SOI-technology and opens a new way of the realization of transistors with steeper slope ($S < 60mV/decade$). This proposal

conserves the same carrier transport mechanism. Thus, a high on-state current can be derived at low threshold voltage. This proposal has superior advantages that make it preferred over other ultra-low-power design especially ferroelectric-based designs. The fabrication process is similar to currently used SOI CMOS technology. Since high doping increases threshold voltage and random fluctuations, this proposition perceptibly can be designed with a low channel doping. In addition, having a ferroelectric film that acts as supplement gate reduces short-channel-effects (SCEs), which gives the possibility of further device scaling. Furthermore, this design structure keeps the operating area of the device similar to the conventional MOSFET. Moreover, the electric field (gate voltage) applied to construct the channel will not be deviated by integration an additional material or two on the gate stack. Thus, this structure provides a stable gate voltage compared to gate-stack structure discussed previously. The approach used to model and analyze the device provided new set of parameters to improve the subthreshold performance of the proposed device. These analyze also predict several advantages as listed below:

- ✓ Speed: Due to low doping and better channel control, the device switching speed is improved.
- ✓ Power: Operate at low threshold voltage and supply voltage.
- ✓ Fabrication process: Integration capability in current CMOS technology.

- ✓ Low leakage: Low off-state current inherited from better mobility and lower short-channel-effect.
- ✓ Low leakage: Negative capacitance removes all the injected carries when the device switching from on to off state.
- ✓ High on-state current.
- ✓ All the advantage of SOI technology.

Over the last decade, broad research concentrated on investigating and understanding in detail the concept of negative capacitance extracted from ferroelectric materials and studying the ferroelectric-based field-effect transistor. Ferroelectric materials integration into logical switch requires a deep investigation to determine its performance and stability in the IC working atmosphere. Moreover, polarization fatigue and an increase of stress that is associated with switching cycles, temperature variation, and the applied electric field are the major challenges of this integration. Identification of the appropriate material with minimal or stress-free as well as good interfacing ferroelectric material with silicon that provides the best subthreshold swing and low leakage.

The integration of any new material into IC requires temperature investigation. With this means, the integration of the ferroelectric film in this design restricted by temperature limitation and hysteresis properties that result in intrinsically unstable negative capacitance [144]. These restraints capitalized in temperature dependency of the

ferroelectricity behavior of the material. Langenberg *et al.* reports a dielectric deviation of the ferroelectric material to temperature variation [145]. This nonconformity obliges a thoughtful design to distinguish an accurate polarization under external electric field.

11.3 Potential Manufacturing Process

The existing processing and fabrication technologies for Silicon-On-Insulator technology (SOI) and Silicon-On-Sapphire (SOS) can be adopted for the proposed SOFFET. Instead of a single layer of the insulator as in SOI and SOS devices, there will be a thin layer of ferroelectric material and another thin layer of buffer insulator placed over a silicon wafer. Several deposition methods of ferroelectric materials were explored by several research groups to be used in semiconductor devices.

The deposition of the ferroelectric materials on a silicon wafer is a hot research topic nowadays due to potential advantages that could be gained from this preparation. The successful growth of ferroelectric materials on silicon will open the door for further progress in IC design. The interest of integrating ferroelectric materials with silicon has grown recently, especially in the nonvolatile ferroelectric memories. An approach of depositing $La_xSr_{1-x}TiO_3$ $(LSTO)$ and $SrTiO_3$ (STO) onto silicon wafers are reported by [146, 147]. Spin-coating and thermal annealing process used to deposit thin film of Ferroelectric *lead calcium titanate* $[(Pb_{0.76}Ca_{0.24})TiO_3]$ on platinum-coated silicon substrates was described in [148]. Ferroelectric nature of the material was preserved after

the deposition. Molecular beam epitaxy (MBE) was also used to deposit epitaxial $SrTiO_3$ films on (001) Si-substrates via a kinetically controlled growth process [149, 150]. Physical and chemical deposition techniques have proved successful deposition of PZT films [151, 152]. $Pb(Zr_xT_{i-x})O_3(PZL)$ and $\left(Pb_{1-2/3y}, La_y\right)(Zr_{1-x}, Ti_x)O_3$ (PLZT) have shown numerous advantages, therefore, well-thought-out for the ferroelectric random access memories (Fe-RAM) designs. PZT were prepared by several methods. However, pulsed laser deposition is a suitable method for preparation of highly oriented multicomponent thin films [153].

Ferroelectric material sensitivity to temperature causes the formation of intermediate layer (structural changes in lettuce structure) on the silicon. To solve this issue, an insulator layer placed in between the active device and the ferroelectric material. A group of materials to serve this purpose are studied in [131, 132]. This layer role is to manage the stability between the silicon and the ferroelectric materials. The buffer insulator layer must hold a high dielectric constant, and high thermal stability.

11.4 Discussion and Conclusion

During the first 3 or 4 decades of the FET technology, the industry was solely focused on bulk MOSFET. When SOI technology was introduced in the 1990s by a simple modification (burying a layer of insulator inside the body) of the device structure, a new generation of device technology was born and many issues of bulk MOSFET technology

were solved. Similarly, when researchers started to introduce a new series of device technologies based on the negative capacitance of ferroelectric materials, the very first proposal was to put the ferroelectric material in the gate-stack. However, gate-stack negative capacitance designs are facing some serious issues as mentioned above. As all the contemporary researchers agree that negative capacitance is the answer to many of the issues of nanoelectronics, we need a better device design to utilize the negative capacitance. We anticipate that, if successful, the proposed SOFFET will bring transformative change in the way negative capacitance can be utilized in nanoelectronic devices. Therefore, our alternative to the previously proposed gate-stack negative capacitance FET design may seem like a simple modification, but the proposed design has enormous potential. In this early research, our attempt is to introduce this new concept and highlight its potential. There are many designs and fabrication issues that need to be resolved.

APPENDIX A

ESTIMATION OF THE BODY FACTOR (η) OF SOI FinFET

For convenience, the equivalent circuit (Figure 7.3) of the internal device capacitances of SOI-FinFET has copied here again in Figure A. 1.

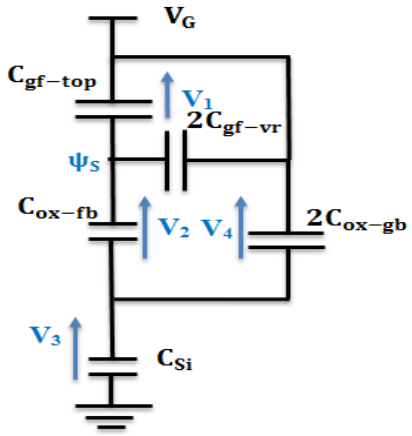


Figure A. 1: An equivalent circuit model of SOI-FinFET capacitances.

For the ease of calculation and handling let us use the following notation for the capacitances.

$$C_1 = C_{gf-top} + 2C_{gf-vr} \tag{0.1}$$

$$C_2 = C_{ox-fb} \tag{0.2}$$

$$C_3 = C_{Si} \tag{0.3}$$

$$C_4 = 2C_{ox-gb} \tag{0.4}$$

Here C_1 and C_2 are in series and their equivalent capacitance can be given by (A5). And the equivalent capacitance C_{eq} can be given by (A6).

$$C_o = C_1C_2/(C_1 + C_2) \tag{0.5}$$

$$C_{eq} = (C_o + C_4)C_3/(C_o + C_3 + C_4) \tag{0.6}$$

The total charges distributed in the capacitive network can be written as: $q = V_G C_{eq}$. V_G is the total voltage applied on the network (gate voltage).

Since C_1 and C_2 are in series, thus, share the same charge. Similarly, C_1, C_2, C_4 shared the same charges with C_3. By considering the same ideologies of a current flow past a given point (if V_i is the voltage across the capacitor C_i, the charges is defined by the relation $Q_i=C_iV_i$). The total charges can be expressed as shown in the equations below:

$$q = C_1V_1 + C_4V_4 \quad (0.7)$$

$$q = C_2V_2 + C_4V_4 \quad (0.8)$$

$$q = C_3V_3 \quad (0.9)$$

$$q = C_{eq}V_G \quad (0.10)$$

Furthermore, since C_1 and C_2 share the same charges and V_1 and V_2 are the voltages across each of them, we have: $C_1V_1 = C_2V_2$ hence $V_1 = C_2V_2/C_1$

From Kirchhoff's Loop Rule: $V_1 + V_2 = V_4$ (Figure A.1 shows the loop). Substitute for V_1 its equivalent expression to get:

$$V_4 = V_2(C_1 + C_2)/C_1 \quad (0.11)$$

By equating (A9) and (A10) we get the expression (A12).

$$V_3 = C_{eq}V_G/C_3 \quad (0.12)$$

Substituting (A11) into (A8) to get:

$$q = \left[C_2 + (C_2 + C_1)\frac{C_4}{C_1}\right]V_2 \tag{0.13}$$

Equating the equations (A10) and (A13) and solve for V_2 to get:

$$V_2 = \frac{C_{eq}V_G}{C_2 + (C_2 + C_1)\frac{C_4}{C_1}} \tag{0.14}$$

We have:

$$\psi_S = V_2 + V_3 \tag{0.15}$$

Replacing (A12) and (A14) into (A15) to get:

$$\psi_S = C_{eq}V_G\left[\frac{C_1C_2 + C_1C_3 + (C_2 + C_1)C_4}{\{C_1C_2 + (C_1 + C_2)C_4\}C_3}\right] \tag{0.16}$$

Solving for V_G to get:

$$V_G = \frac{1}{C_{eq}}\frac{\{C_1C_2 + (C_1 + C_2)C_4\}C_3}{C_1C_2 + C_2C_3 + (C_2 + C_1)C_4}\,\psi_S \tag{0.17}$$

The body factor η can evaluated as:

$$\eta = \frac{1}{C_{eq}}\frac{\{C_1C_2 + (C_1 + C_2)C_4\}C_3}{C_1C_2 + C_2C_3 + (C_2 + C_1)C_4} \tag{0.18}$$

The equation (A18) simplified to:

$$\eta = 1 + \frac{C_2C_3}{C_1(C_2 + C_3 + C_4)C_2C_4} \tag{0.19}$$

Replacing C_{eq}, C_1, C_2, C_3, and C_4 with their values (A1, A2, A3, and A4) to get:

$$\eta = 1 + \frac{C_{ox-fb} \times C_{Si}}{\left(C_{gf-top} + 2 \times C_{gf-vr}\right) \times \left(C_{ox-fb} + C_{Si} + 2C_{ox-gb}\right) + 2 \times C_{ox-fb} \times C_{ox-gb}} \quad (0.20)$$

APPENDIX B

SOLUTION FOR THE POISSON EQUATION of MT-CNTFET

To solve equation (0.1) we separate it into 1D, 2D, 3D Poisson/Laplace equations as shown below:

$$\psi(x,y,z) = \psi_{1D}(x) + \psi_{2D}(x,y) + \psi_{3D}(x,y,z) \tag{0.1}$$

$$\frac{\partial^2 \psi_{1D}(x)}{\partial^2 x} = \frac{q}{\varepsilon_{ct}} n_i e^{q\psi_1/KT} \tag{0.2}$$

$$\frac{\partial^2 \psi_{2D}(x,y)}{\partial^2 x} + \frac{\partial^2 \psi_{2D}(x,y)}{\partial^2 y} = 0 \tag{0.3}$$

$$\frac{\partial^2 \psi_{3D}(x,y,z)}{\partial^2 x} + \frac{\partial^2 \psi_{3D}(x,y,z)}{\partial^2 y} + \frac{\partial^2 \psi_{3D}(x,y,z)}{\partial^2 z} = 0 \tag{0.4}$$

Where q is the electric charges, ε_{ct} is the permittivity of CNT, n_i is the intrinsic carrier density, ψ is the electric potential of the silicon surface, K_B is Boltzmann's constant, T is the temperature in °K. Here we consider triple-channel Multi-gate with $q\psi/K_BT >> 1$ so that the hole density is negligible [154].

A) Solution to 1D Poisson equation (0.2)

The boundary conditions are presented in (0.5) and (0.6). Integrating (0.2) for, $0 \leq x \leq a$ to get (0.7).

$$\varepsilon_{si} \left.\frac{\partial \psi_{1D}(x)}{\partial x}\right|_{x=a} = C_{ox}\left(V_{gs} - \varphi_{ms} - \psi_{1D}(a)\right) \tag{0.5}$$

$$\left.\frac{\partial \psi_{1D}(x)}{\partial x}\right|_{x=0} = 0 \tag{0.6}$$

$$\psi_{1D}(x) = \psi_0 - 2V_t \ln\left[\cos\left(\zeta e^{\frac{\psi_0}{2V_t}x}\right)\right] \tag{0.7}$$

$$\psi_s = \psi_0 - \frac{2k_BT}{q}\ln\left[\cos\left(\zeta a e^{\frac{\psi_0}{2V_t}}\right)\right] \; at \; \psi_{1D}|_{x=a} = \psi_s \tag{0.8}$$

Where $\zeta = \sqrt{\frac{qn_i}{2\varepsilon_{ct}V_t}}$, $V_t = \frac{k_BT}{q}$ and $\psi_0 \approx \frac{V_{gs}-\varphi_{ms}}{\frac{qn_i}{C_{ox}\varepsilon_{ct}}-(V_t[V_{gs}-\varphi_{ms}]-1)}$

B) Solution to 2D Laplace equation (0.3)

$\psi_{2D}(x,y)$ is the solution for 2D Laplace equation (0.3) for the following boundary conditions:

$$\psi_{2D}(x,0) = V_{bi} \tag{0.9}$$

$$\psi_{2D}(x,L_{ch}) = V_{bi} + V_{ds} \tag{0.10}$$

$$\psi_{2D}(0,y) - \frac{t_{ox_l}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left.\frac{\partial\psi_{2D}(x,y)}{\partial x}\right|_{x=0}\right] = 0 \tag{0.11}$$

$$\psi_{2D}(W_{fin},y) - \frac{t_{ox_r}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left.\frac{\partial\psi_{2D}(x,y)}{\partial x}\right|_{x=W_{fin}}\right] = 0 \tag{0.12}$$

The potential profile in the *(x, y)* plane $\psi_{2D}(x,y)$ is the solution to (0.3) and can written as $\psi_{2D}(x,y)$ using the method proposed by [5, 155], 2D Poisson's equation solution is:

$$\psi_{2D}(x,y) = C_0(y) + C_1(y)x + C_2(y)x^2 \tag{0.13}$$

Where $C_0(y), C_1(y),$ and $C_2(y)$are arbitrary functions of y and determined by sing the boundary conditions given above.

$$\psi_{2D}(0,y) = \psi_{2D}\left(a + \frac{d_{ct}}{2}, y\right) = \psi_f(y) = C_0(y) \tag{0.14}$$

Where $\psi_f(y)$ is the left/right surface potential:

$$\left.\frac{\partial \psi_{2D}(x,y)}{\partial x}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{ct}} \frac{\psi_f(y) - \psi_{gs}}{b} = C_1(y) \tag{0.15}$$

$$\begin{aligned} \left.\frac{\partial \psi_{2D}(x,y)}{\partial x}\right|_{x=W_{fin}} &= \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_f(y) - \psi_{gs}}{b} \quad = C_1(y) + 2\left(a + \frac{d_{ct}}{2}\right) C_2(y) \\ &= -C_1(y) \end{aligned} \tag{0.16}$$

Where: $\psi_{gs} = V_{gs} - V_{fb}$

Thus $C_2(y) = -\frac{C_1(y)}{a + \frac{d_{ct}}{2}}$

$$\psi_{2D}(x,y) = \psi_f(y) + \frac{\varepsilon_{ox}}{\varepsilon_{ct}} \frac{\psi_f(y) - \psi_{gs}}{b} \left(x - \frac{x^2}{a + \frac{d_{ct}}{2}} \right) \tag{0.17}$$

Replace this equation into 2D to determine $\psi_f(y)$

$$\psi_f(y) = Ae^{\sqrt{\lambda}y} + Be^{-\sqrt{\lambda}y} - \psi_{gs} \tag{0.18}$$

y is the electron affinity (denoted by χ_{ct}) and λ is the characteristics length where:

$\lambda_{Tri-gate} = \sqrt{\frac{2\varepsilon_{ct} d_{ct}^2 \ln\left(1 + \frac{2b}{d_{ct}}\right) + \varepsilon_{ox} b^2}{16\varepsilon_{ox}}}$ Using the boundary condition (0.9) and (0.10) we can calculate A and B:

$$A = V_{bi}\left(1 - \frac{e^{\frac{\sqrt{\lambda}L_{ch}}{2}}\sinh\left(\frac{\sqrt{\lambda}L_{ch}}{2}\right)}{\sinh\left(\sqrt{\lambda}L_{ch}\right)}\right)$$

$$B = \frac{V_{bi}\, e^{\frac{\sqrt{\lambda}L_{ch}}{2}}\sinh\left(\frac{\sqrt{\lambda}L_{ch}}{2}\right)}{\sinh\left(\sqrt{\lambda}L_{ch}\right)} \tag{0.19}$$

C) Solution to 3D Laplace equation (B4)

Apply separation of variables to (0.4):

Let $\psi_{3D}(x,y,z) = F(x)G(y)H(z)$ and substituting in (0.4) and dividing by $\psi_{3D}(x,y,z)$

We can derive the equations (0.20) to (0.22). Where $k_1^2 + k_2^2 = k_3^2$

$$\frac{\mathrm{F"(x)}}{\mathrm{F(x)}} = -\frac{G"(y)}{G(y)} - \frac{H"(z)}{H(z)} = k_1^2 \tag{0.20}$$

$$\frac{G"(y)}{G(y)} = -\frac{\mathrm{F"(x)}}{\mathrm{F(x)}} - \frac{H"(z)}{H(z)} = k_3^2 \tag{0.21}$$

$$\frac{H"(z)}{H(z)} = -\frac{\mathrm{F"(x)}}{\mathrm{F(x)}} - \frac{G"(y)}{G(y)} = k_2^2 \tag{0.22}$$

Applying the boundary condition F(0) = 0 so that $C_{10} = 0$ and H(0)=0 so that $C_{20}=0$. For simplicity and clarity $C_{30} = C_{31}$ assumed which gives:

$$\psi_{3D}(x,y,z) = \eta \sin(k_1 x)\ \sin(k_2 z)\ \cosh(k_3 y) \tag{0.23}$$

To calculate $\eta, k_1, k_2,$ and k_3 we apply the boundary condition (0.9) and (0.10)

$$\eta = \frac{\varepsilon_{ox}}{\varepsilon_{ct}} \frac{\sqrt{2}}{bk_3} \tan\left(\frac{ak_3}{\sqrt{2}}\right),\ k_1 = k_2 = \frac{1}{a} \tan^{-1}\left(\frac{\varepsilon_{ct}}{\varepsilon_{ox}} \frac{k_3}{\sqrt{2}} b\eta\right),$$

$$k_3 \approx \frac{\ln\left(1 + \frac{V_{ds}}{V_{bi}} + \sqrt{\frac{2V_{ds}}{V_{bi}}}\right)}{L_{ch}} \tag{0.24}$$

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