ADDRESSING ON-CHIP POWER CONVERSTION AND DISSIPATION ISSUES IN MANY-CORE SYSTEM-ON-A-CHIP BASED ON CONVENTIONAL SILICON AND EMERGING NANOTECHNOLOGIES

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By

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ABSTRACT

Integrated circuits (ICs) are moving towards system-on-a-chip (SOC) designs. SOC allows various small and large electronic systems to be implemented in a single chip. This approach enables the miniaturization of design blocks that leads to high density transistor integration, faster response time, and lower fabrication costs. To reap the benefits of SOC and uphold the miniaturization of transistors, innovative power delivery and power dissipation management schemes are paramount. This dissertation focuses on on-chip integration of power delivery systems and managing power dissipation to increase the lifetime of energy storage elements. We explore this problem from two different angels: On-chip voltage regulators and power gating techniques. On-chip voltage regulators reduce parasitic effects, and allow faster and efficient power delivery for microprocessors. Power gating techniques, on the other hand, reduce the power loss incurred by circuit blocks during standby mode.

Power dissipation ($P_{total} = P_{static}$ *and* $P_{dynamic}$) in a complementary metal-oxide semiconductor (CMOS) circuit comes from two sources: static and dynamic. A quadratic dependency on the dynamic switching power and a more than linear dependency on static power as a form of gate leakage (subthreshold current) exist. To reduce dynamic power

loss, the supply power should be reduced. A significant reduction in power dissipation occurs when portions of a microprocessor operate at a lower voltage level. This reduction in supply voltage is achieved via voltage regulators or converters. Voltage regulators are used to provide a stable power supply to the microprocessor. The conventional off-chip switching voltage regulator contains a passive floating inductor, which is difficult to be implemented inside the chip due to excessive power dissipation and parasitic effects. Additionally, the inductor takes a very large chip area while hampering the scaling process. These limitations make passive inductor based on-chip regulator design very unattractive for SOC integration and multi-/many-core environments. To circumvent the challenges, three alternative techniques based on active circuit elements to replace the passive LC filter of the buck convertor are developed. The first inductorless on-chip switching voltage regulator architecture is based on a cascaded 2^{nd} order multiple feedback (MFB) low-pass filter (LPF). This design has the ability to modulate to multiple voltage settings via pulse-with modulation (PWM). The second approach is a supplementary design utilizing a hybrid low drop-out scheme to lower the output ripple of the switching regulator over a wider frequency range. The third design approach allows the integration of an entire power management system within a single chipset by combining a highly efficient switching regulator with an intermittently efficient linear regulator (area efficient), for robust and highly efficient on-chip regulation.

The static power (P_{static}) or subthreshold leakage power (P_{leak}) increases with technology scaling. To mitigate static power dissipation, power gating techniques are implemented. Power gating is one of the popular methods to manage leakage power during standby periods in low-power high-speed IC design. It works by using transistor based

switches to shut down part of the circuit block and put them in the idle mode. The efficiency of a power gating scheme involves minimum I_{off} and high I_{on} for the sleep transistor. A conventional sleep transistor circuit design requires an additional header, footer, or both switches to turn off the logic block. This additional transistor causes signal delay and increases the chip area. We propose two innovative designs for next generation sleep transistor designs. For an above threshold operation, we present a sleep transistor design based on fully depleted silicon-on-insulator (FDSOI) device. For a subthreshold circuit operation, we implement a sleep transistor utilizing the newly developed silicon-on-ferroelectric-insulator field effect transistor (SOFFET). In both of the designs, the ability to control the threshold voltage via bias voltage at the back gate makes both devices more flexible for sleep transistors design than a bulk MOSFET. The proposed approaches simplify the design complexity, reduce the chip area, eliminate the voltage drop by sleep transistor, and improve power dissipation. In addition, the design provides a dynamically controlled V_t for times when the circuit needs to be in a sleep or switching mode.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled "Addressing On-Chip Power Conversion and Dissipation Issues in Many-Core System-on-a-Chip based on Conventional Silicon and Emerging Nanotechnologies," presented by Emeshaw Ashenafi, candidate for the Doctor of Philosophy degree, and hereby certify that in their opinion it is worthy of acceptance.

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CONTENTS

LIST OF ILLUSTRATIONS

Figure Page

LIST OF TABLES

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Emeshaw Ashenafi
Friday, June 30’ 2017, Kansas City, MO

DEDICATION

I would like to dedicate this work to all my family especially my beloved mother, Elsabet T. Abebe. Her audacity and conviction gave me all the strength that propelled me throughout the years, and helped me overcome all the challenges and difficult times along the way to achieve my academic and now professional goals.

CHAPTER 1

INTRODUCTION

As process technologies pursuing Moore's law [1] down to nanometer dimensions, many IC based applications are moving to system-on-a-chip (SOC) designs [2], which will adopt a multi-/many-core platform instead of a single-core implementation [3]. Scaling down of CMOS technology is happening at a stupendous rate. As a result of miniaturization and enormous transistor density, power delivery and power dissipation are becoming grand challenges and vital parameters to be addressed. As shown by Figure 1.1 (a), the supply voltage and threshold voltages are reduced with technology node scaling. This allows a greater number of transistors to be fabricated on a single die and operate at a very high speed. According to [4], a chip fabricated in 2003 with 45 nm technology had 153 million transistors switching near 3 GHz will be fabricated with 7 nm technology containing 4,908 million transistors operating at 53 GHz frequency in 2018. Even though the reduction of transistor size and the drop in the operating voltage should lower dynamic power loss, due to the surge in the operating frequency, the dynamic power dissipation increases. As depicted by Figure 1.1 (b), the static power dissipation is becoming prominent and contributes more to the total power dissipation with the miniaturization of the transistor. As integrated circuits are moving towards SOC designs, integration of entire power management systems within a single chipset require new approaches. Therefore, alongside the SOC systems, an on-chip power delivery and advance architectures intended to lower power dissipation are paramount and should be investigated. Both of the above interlocked

issues are identified and explored in this document and the proposed designs are presented in detail over the next chapters.

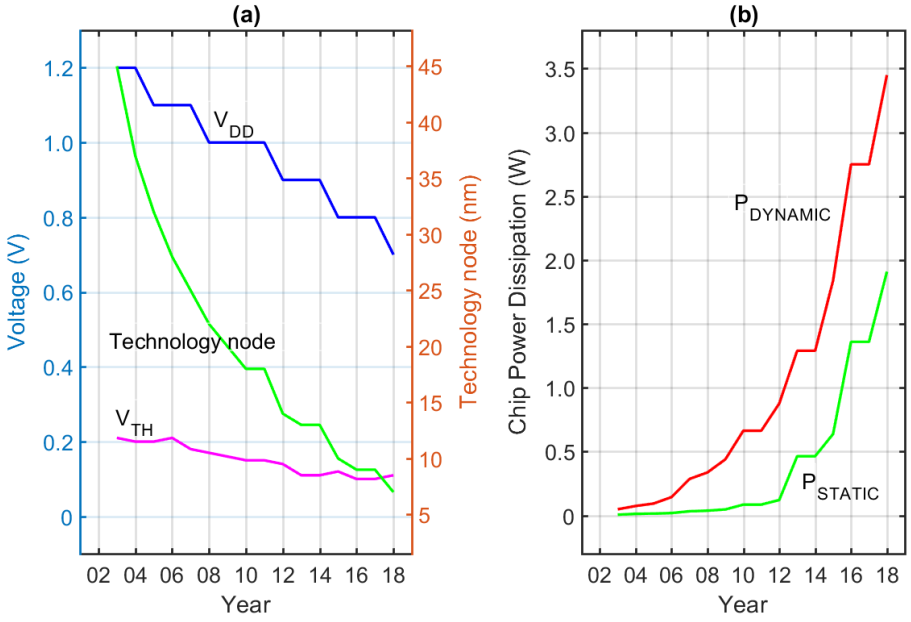

Figure 1.1: Technology scaling with dynamic and static power dissipation [4] [5]

1.1 Organization

This dissertation consists of seven chapters beginning with this chapter. Chapter 1: gives the general overview and objective of the projects, the contribution of the work, as well as the layout of the dissertation. Chapter 2: presents the background of the various projects. This chapter includes short introductions for the five main chapters that focus on the following: an on-chip switching regulator, hybrid low dropout regulator, fully on-chip power management system, above threshold sleep transistor design, and subthreshold sleep transistor design. Chapter 3: is an introduction to switching regulators, in particular, on-chip voltage regulators. This chapter presents the proposed design and implementation. It also discusses the advantage and disadvantages of on-chip switching voltage regulators.

Chapter 4: provides a hybrid low dropout scheme to improve the output voltage ripple of the switching voltage regulator. This architecture is designed to work in synergy with the switching regulator implemented in Chapter 3. Chapter 5: integrates the entire power management system within a single chipset by combining an on-chip switching regulator with a linear regulator. Chapter 6: presents a sleep transistor design for an above threshold operation depicting an innovative approach to existing sleep transistor design. Chapter 7: provides a subthreshold sleep transistor design. This chapter considers an ultra-low voltage design environment and presents a newer approach to manage power dissipation by utilizing sleep transistors.

1.2 Dissertation Objectives

Many researchers have proposed numerous designs to solve power management problems. The aim of this research is to enhance existing capabilities and address lingering power management issues from both the delivery and utilization ends. The challenges are identified and tackled by providing advance and novel solutions. As mentioned above, IC designs are moving to SOC integration when possible. SOC provides the flexibility of implementing different electronic systems into a single chip. This method enables the function blocks to shrink allowing greater transistor integration. In addition, it provides a faster response time and reduction in fabrication costs. In order to take advantage of the benefits of SOC and miniaturization of transistors, innovative power delivery and power dissipation management systems are vital. The core objectives of this dissertation are the integration of on-chip power delivery systems and managing power dissipation to increase the lifetime of energy storage elements. We explore this problem from two different angels:

on-chip voltage regulators and power gating techniques. On-chip voltage regulators reduce parasitic effects and allow faster and efficient power delivery for specified loads or microprocessors. Power gating techniques, on the other hand, reduce the power loss incurred by circuit blocks during standby mode.

The main objectives of this dissertation are summarized as follows:

- To show existing on-chip switching voltage regulators and present the new on-chip architecture and to compare the advantages and disadvantages of the design.
- To illustrate how a low dropout voltage regulator is implemented and explain how the new hybrid design is used as a standalone voltage regulator or in synergy with the switching regulator.
- To implement a complete on-chip power management system and display the performance of the design.
- To present the sleep transistor design for a conventional (above threshold) operation and compare it with the existing designs.
- To introduce the new sleep transistor design for a subthreshold region operation and to show the advantages of the design over conventional design approaches.

1.3 Summary of Contributions

Voltage regulators are used to provide a stable power supply to microprocessors. The conventional off-chip switching voltage regulator contains a passive floating inductor that is difficult to be implemented inside the chip due to excessive power dissipation and parasitic effects. Additionally, the inductor takes a very large chip area, and thereby hampers the scaling process. These limitations make passive inductor based on-chip

regulators very unattractive for SOC design and multi-/many-core environments. To circumvent these challenges, three alternative techniques for voltage regulators that are based on active circuit elements are presented. On-chip voltage regulators provide power deliver at a very high speed, utilize smaller filter elements, reduce parasitic effects, and have faster transient response to load change. One of the few drawbacks of an on-chip voltage regulator is the amount of instantaneous charges available to the load due to the smaller filter capacitors. The first design utilizes active filters and adjust the output voltage ranges between 0.5 V to 1.5 V with 100 µA to a 150 mA output current depending on the load requirement. This regulator has an output ripple of +/- 8 mV and operates at a 5 MHz frequency. The second design is a hybrid scheme that combines a linear regulator and a switching voltage regulator. This regulator can suppress an output voltage ripple further up to 10 MHz and can provide a stable output voltage from 0.5 V to 1.2 V with a maximum 120 mA output current. The third design, which is a complete on-chip power management system, has three unique design options. It can generate the adjustable switching output voltage between 0.5 V to 1.5 V/1.6 V and 100 µA to a 150 mA output current, or/and an adjustable linear output voltage between 0.5 V to 1.2 V and 100 µA to a 120 mA output current at the second stage.

To address static power dissipation, Power Gating techniques are utilized to manage power consumption and thermal stress in microprocessors and other high-performance integrated circuits. Most of the power gating techniques utilize sleep transistors in different configurations to reduce the subthreshold leakage current, which is the primary source of the standby power. These sleep transistors, which are added between

the supply lines and the logic circuits as header and footer switches, impose additional area, delay, power, and other overheads and design complexities. The proposed design concept combines the functionality of the sleep transistors with the logic devices. For an above threshold operation, the architecture is implemented using a fully depleted silicon-on-insulator (FDSOI) device. For a subthreshold circuit operation, the newly developed Silicon on Ferroelectric-Insulator FET (SOFFET) is utilized for sleep transistor design. Both approaches eliminate the requirement of employing a separate set of sleep transistors to place the circuit in the sleep or idle mode during the standby period. This technique reduces the overall complexity and overhead of integrated circuits and simplifies the power gating techniques. In addition, the designs improve the overall power efficiency and lower thermal effects.

The five main contributions of this work are delineated as follows:

- The first design is a fully integrated on-chip switching voltage regulator. This regulator utilizes cascaded MFB loop filters with an error correction amplifier. The voltage regulator is controlled by specifying the reference voltage and by varying the pulse width via the PWM signal. The output voltage can be adjusted dynamically and the output current can be changed based on the requirement load.
- The second design is a hybrid low dropout (LDO) voltage regulator. This regulator has multiple feedback loops for error correction. This regulator can be controlled via a reference voltage. The regulator can also be used as a standalone design to supply different output voltages and currents as required by reference voltage and

the load. In addition, the regulator can be integrated to work in synergy with the proposed on-chip voltage regulator to suppress and lower the output voltage ripple.

- The third design is a fully on-chip power management system. This design provides three different unique architectures depending on the specified application. Since the internal post regulating stage minimizes the output ripple, it can be used as a standalone regulator to drive a load with a low noise requirement.
- The fourth design is an above threshold sleep transistor design. This design is implemented using FDSOI. The FDSOI provides a double gate structure that allows the modulation of the threshold voltage via the back gate. The back bias is used to change the threshold setting between *low-Vt* and *high-Vt*. This enables the design of the sleep transistor to be incorporated as part of the logic block.
- The fifth design is a subthreshold sleep transistor design. The presented architecture utilizes SOFFET devices. SOFET provides both a steep subthreshold swing and high *Ion*/*Ioff* ratio. Conventional sleep transistor architectures have to be restructured for subthreshold region designs. The proposed solution obviates the standalone sleep transistor switch, which reduces area, improves speed, avoids voltage drop by the sleep transistor and simplifies the design complexity.

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

In this chapter, we discuss the background of on-chip voltage regulators and sleep transistor designs. Specifically, we look at existing designs pertaining to on-chip voltage regulators and sleep transistor designs, and present the findings. A compilation of previous works and literature reviews are also organized and presented in this chapter. The approaches taken and specific design parameters of the proposed designs are covered in later chapters.

2.1 Introduction

Conventional DC-DC converters can be grouped into three main categories: switching, switched capacitor, and linear DC-DC converters [6], [7], and [8]. Buck converters are considered step down switching regulators. A buck converter can generate a regulated lower output voltage from a higher dc input voltage with high efficiency. The major drawback of using buck converters is the bulky inductor in the LC filter. The most commonly used linear regulator is a low-dropout (LDO) regulator. LDO regulators are more area efficient as compared to buck converters and generally can be implemented on the chip [6], [7]. These regulators, however, require a large output capacitance to maintain stability. This output capacitor is generally implemented off-chip [7]. Switched capacitor DC-DC converters (or charge pumps) utilize non-overlapping switches to charge the capacitor to transfer the charge from input to output [6], [7]. It is capable of generating a higher or lower output voltage source using capacitors. However, these voltage converters dissipate a significant amount of power through the resistive switches [6], [7].

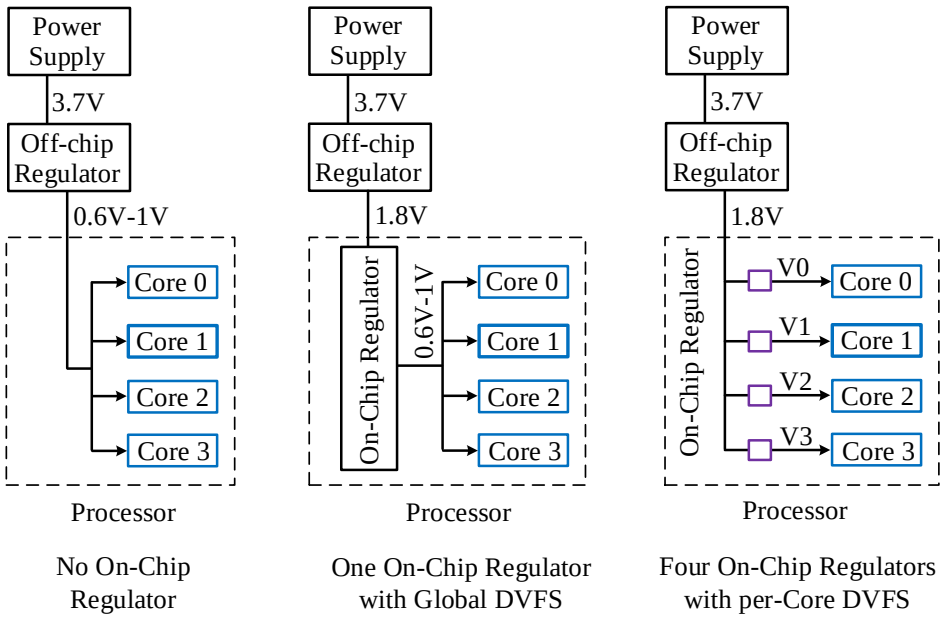

Figure 2.1: Power-supply configurations for a 4-core [9]

Figure 2.1 illustrates the three types of power-supply configurations for a processor with a 4-core [9]. The first configuration (left) represents a conventional design scenario that only uses an off-chip voltage regulator. This off-chip voltage regulator down covert the voltage provided by the battery to the proper values required by each core. The second configuration (middle) implements a two-step voltage conversion scenario [9]. In this approach, the off-chip regulator steps down the voltage and supply to the global voltage regulator placed inside the chip. The voltage needs to be farther reduced by the global on-chip regulator. This approach improves efficiency but lucks the flexibility of powering each core with different voltage settings. The third configuration (right) expands on the second configuration by providing four separate on-chip power domains via individual on-chip voltage regulators [9]. The third approach exhibits the highest flexibility for per-core voltage regulation. All three of the voltage regulator designs presented in this dissertation are designed in mind to work for both configurations, two and three.

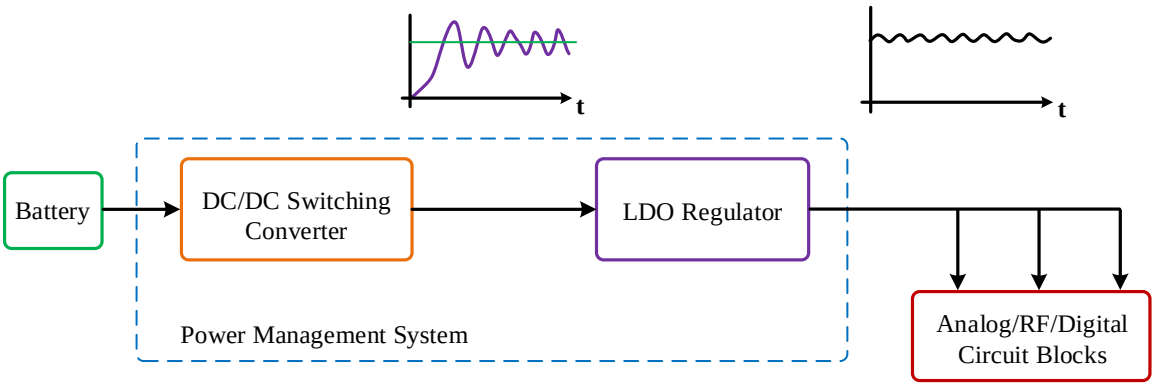

Figure 2.2: Block diagram of typical power management system [10]

Switching regulator or Buck converter is highly efficient and provides power to the microprocessors or loads. An off-chip switching regulator is an integral part of almost every electronic application. Currently, there is a great push for on-chip integration of voltage regulators for better management of power, temperature, and load or activity migration among the functional blocks or cores. An on-chip regulator is critically important for SOC and multi-/many-core ICs, because based on activity levels of different blocks or cores in high-density and high-performance ICs, the supply voltage has to be adjusted in nano or pico second time. To reap the given benefits, the goal of the voltage regulator architectures presented in this dissertation is to have them integrated on-chip. To that end, all the regulators, the on-chip switching regulator, the hybrid on-chip LDO regulator designs and the fully on-chip power management system were designed to work independently. Switching regulators are highly efficient convertors but generate unwanted voltage ripple at the output. As shown by [10], it is customary to use LDO regulators cascaded with switching regulators for post ripple rejection. The designs in this dissertation are implemented with this specification to work in synergy as shown by Figure 2.2. The details of the designs and simulation results are presented in the later chapters.

Leakage power consumption has become a major bottleneck for the continuous scaling of CMOS technologies. It has been reported that leakage power accounts for as much as 42% of the total power in a high-end microprocessor in 65 nm technology [11], [12]. Power gating is one of the popular methods to manage leakage power during the standby mode in low-power and high- speed ICs. It works by using transistor based switches (sleep transistors) to shut down part of the circuit block and put them in an idle mode. Sleep transistors help ICs manage power and thermal effects efficiently. The total power consumption of the ICs is comprised of static, dynamic and short circuit effects. The dynamic behavior has an exponential effect on the power dissipation, and as a result, it leads to a higher temperature injection in the circuit node. In the static mode, temperature has an exponential effect on the leakage current. This inter-dependence of power and thermal impacts makes efficient power gating circuit a very critical requirement for integrated circuits and systems.

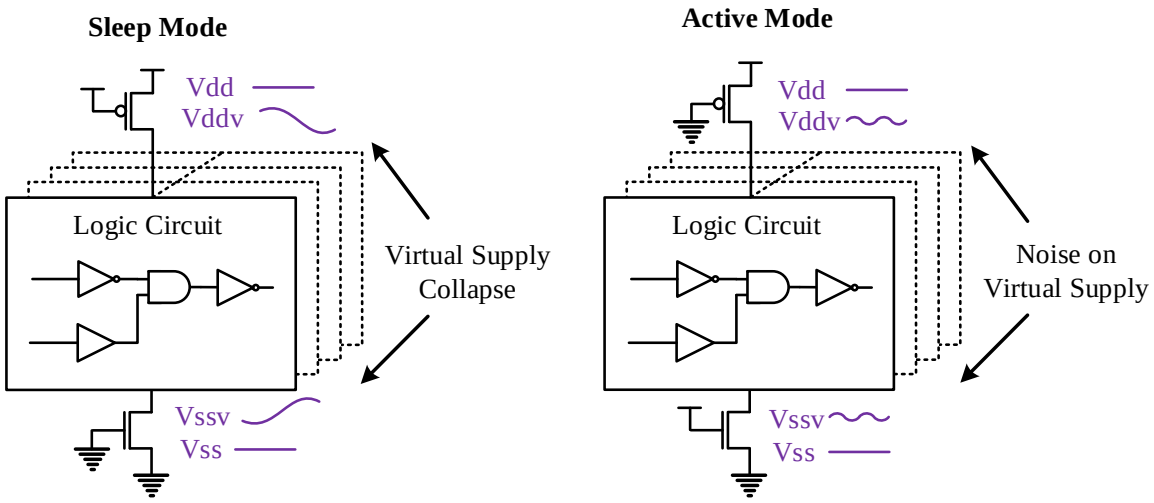

Figure 2.3: General sleep transistor architecture

There is a growing need for energy efficient, portable, and handheld electronic devices. These devices demand better power management schemes to mitigate leakage power in the idle or sleep mode. For the next generation IC designs, the reduction of the supply voltage (V_{DD}) is vital to reduce the dynamic power and avoid reliability problems in deep submicron (DSM) and nanometer regimes [13]. However, a unilateral approach of reducing the supply voltage will result in performance degradation. In addition, with the scaling down of V_{DD} and transistor sizes, the threshold voltage is inherently lowered. This threshold voltage reduction increases the off-state current. Therefore, the power during off-state accordingly increases and becomes a dominant concern in low power designs. A comprehensive approach to reduce the total power while maintaining performance is to scale down V_{DD} with the option of a variable threshold voltage. Consequently, a power gating technique using multi-threshold FETs has become a very effective and popular method to manage leakage power during standby periods in low-power high-speed IC design. As shown by Figure 2.3, the technique is implemented by using a high threshold voltage (V_T) sleep transistor with low threshold voltage logic gates. It works by using transistor based switches to shut down or move part of the circuit block to the idle mode. In this dissertation, two sleep transistor designs are presented. Both designs are implemented with dynamically controlled threshold voltage. The first design addresses the issues for conventional operations. On the other hand, the second design focus on subthreshold region design. Both architectures are presented in detail in later chapters.

2.2 Switching Voltage Regulator Review

Switching voltage regulators are highly efficient voltage converts. The work presented in [14] shows the design of an inductor based on-chip CMOS linear-assisted DC-DC regulator. In the presented technique, an auxiliary linear regulator is used to cancel the output voltage ripple and provides fast responses for load and line variations. The presented structure has good features for on-chip power supply systems and on-chip power management systems with low-to-medium current consumption. The voltage regulator generates 1.1 V and around 15 mA output current from 1.6 V to 1.8 V input.

Switching voltage regulator is popular due to the high efficiency and good output voltage regulation characteristics [15]. The conventional on-chip switching voltage regulator usually utilizes an L-C passive low pass filter in the output terminal [16]. The proposed design in [16] utilizes a diode and a second-order passive L-C low pass filter. In the simulation, a 10 µF capacitor is used in the filter design, which is very large for fully on-chip integration. The system runs at 500 kHz and generates 1.8 V, 2.5 V, and 3.3 V output voltage from 5 V input [16].

In [6], [7], and [8] a hybrid architecture is presented by combining a switching voltage regulator and a linear voltage regulator. For all the designs in [6], [7], and [8], a third order low pass unity-gain Sallen-Key filter topology is used instead of the conventional LC filter. In [8], the design is fabricated with a commercial 110 nm CMOS technology. The area of the voltage regulator is 0.015 mm^2 and delivers up to 80 mA of output current. The transient response with no output capacitor ranges from 72 ns to 192 ns. The hybrid voltage regulator dissipates 0.38 mA quiescent current and delivers up to

80 mA current while generating 0.9 volts from a 1.8 volt input voltage. The voltage regulator in [6] can supply over 100 mA current while generating 0.9 volts from a 1.2 input voltage. The regulator dissipates 0.25 mA quiescent current and can deliver over 220 mA current to the load circuitry while generating 0.8 volts [6]. The proposed circuit in [7] can supply over 100 mA current while generating 0.9 volts from a 1.2 input voltage. The total on-chip area is approximately 0.026 mm^2 [7]. The regulator dissipates 0.38 mA quiescent current and can deliver over 140 mA current to the load circuitry.

The analysis considered in [17] utilizes an on chip inductor proposed by [54]. This inductor is fabricated with amorphous CoZrTa film and can work in GHz frequency. It also has low series resistance that can make it better than the conventional integrated spiral inductor. The design in [17] requires a large capacitor and inductor area [17]. An efficiency of 88.4% is shown for a voltage conversion from 1.2 to 0.9 V while supplying 9.5 A maximum current at a switching frequency of 477 MHz. The area of the buck converter at the target design point is 12.6 mm^2, which is primarily occupied by a 100 nF filter capacitor [17].

Dynamic voltage and frequency scaling (DVFS) is a well-known technique to reduce energy in portable systems, but DVFS effectiveness suffers from the fact that voltage transitions occur on the order of tens of microseconds. Voltage regulators that are integrated on the same chip as the microprocessor core provide the benefit of both nanosecond-scale voltage switching and improved power delivery [55]. In [55], a multi-phase buck converter is modeled in Simulink using parasitic resistances and capacitances extracted from HSPICE. Multi-phase designs are also suitable for on-chip power

regulators, because they allow for small output capacitance and achieve fast transient response [55]. In the proposed model, a 1.9 V to 1.1 V step-down converter to deliver power to a 4-core embedded processor implemented in a 130 nm CMOS process, where each core is similar to an Intel Xscale processor [55], [20]. Each core operates at a maximum frequency of 1.1 GHz with a 1.1 V regulated voltage, while consuming 400 mA per core. By making the required filter inductor sufficiently small for the on-chip design, air-core surface mount inductors are assumed, based on products from Datatronic [55]. A total on-chip capacitance of 16 nF is assumed, and the on-chip regulator uses this capacitance as its output filter capacitor [55].

2.3 LDO Voltage Regulator Review

Low dropout voltage regulators (LDO) are widely used in portable products such as cellular phones, cameras, and laptops [21]. In [21], a wide range load (100mA) LDO designed with 0.25 µm CMOS process is presented. By using a fast transient loop, a high performance in transient response and output stability is shown. Due to the improved transient response, the value of the output capacitor can be decreased. This allows the integration of the capacitor within the LDO chip [21]. The proposed design is composed of a two-stage error amplifier, band-gap voltage reference and power transistor. The fast transient loop is added to improve the circuit stability and response [21]. The LDO requires a 300pf load capacitor and an input voltage from 2.3 V to 5 V. The output voltage is observed within 2±0.01 V. The chip area is 135 µm X 125 µm, which includes the on-chip load capacitor [21].

Generally, the output voltage ripple of switched mode power supplies can be further reduced by means of an additional LDO, which is used as post-regulator/filter for the output voltage [22]. In [22], a Current Mode LDO in combination with a load current dependent dropout tracking circuit, where the output current information comes from a replica of the pass transistor in the LDO is used. The dropout tracking circuit compares the voltages on the LDO terminals and sends a load current dependent control signal to the DC/DC converter [22]. The goal of this configuration is to obtain a high power supply rejection ratio to lower the output voltage ripple at optimized efficiency [22]. The power management system in [22] requires an input voltage range from 2.5 V to 5 V. The proposed LDO can generate a load current up to 20 mA and has 0.22 µF load capacitor and an output voltage ripple of about 7 mV [22].

The work in [23] proposes a solution to the present bulky external capacitor of LDO voltage regulators with an external capacitorless LDO architecture. The 2.8 V capacitorless LDO voltage regulator with a power supply of 3 V was fabricated in a commercial 0.35 µm CMOS technology, consuming only 65 µA of quiescent current with a dropout voltage of 200 mV [23]. The conventional LDO voltage regulator, for stability requirements, requires a relatively large output capacitor in the single microfarad range. Large microfarad capacitors take large chip areas, thus each LDO regulator needs an external pin for a board mounted output capacitor [23]. The absence of a large external output capacitor presents several design challenges both for ac stability and a load transient response [23]. Thus, a capacitorless LDO requires an internal fast transient path to compensate for the absence of

the large external capacitor. An on-chip 100 pF load capacitor was included and the chip area is 0.29 mm^2 [23].

The work in [24] presents a capacitor-less LDO regulator with a slew rate enhancement circuit. The proposed slew-rate enhancement circuit senses the transient voltage at the output of the LDO to increase the bias current of the error amplifier for a short duration. Hence, the transient response of the regulator significantly improves due to the enhancement of the slew-rate at the gate of the pass transistor [24]. The design and simulation is done in 0.18 μm standard CMOS process. The LDO regulator consumes a quiescent current of 40 μA. It regulates the output voltage at 1.2 V from a 1.4 V to 1.8 V supply, with a minimum drop-out voltage of 200 mV at the maximum output current of 100 mA [24]. The width of the pass transistor is 10.8 mm to maintain saturation at a low dropout condition. The on-chip parasitic capacitance (C_o) of load is estimated as 100 pF [24]. The layout of the final chip excluding pads occupies an area of 260 μm × 169 μm [24].

An on-chip, LDO voltage regulator with improved power-supply rejection (PSR) that is able to drive large capacitive loads is presented in [25]. The LDO compensation is achieved via a custom, wide bandwidth capacitance multiplier (c-multiplier) that emulates a nanofarad-range capacitance at the LDO output node [25]. The proposed LDO achieves a PSR of 39 dB up to 20 MHz at 1.2 V output voltage, while maintaining a 97.4% current efficiency. The design was fabricated in a 0.18 μm technology for a 1.2 V output voltage with 10 mA maximum output current [25]. To verify the performance of the LDO, the prototype includes an on-chip 600 pF capacitor to mimic the supply-line capacitance of the

load circuit. The design takes 1.50 mm x 1.50 mm chip area and requires a quiescent current of 265 μA [25].

In [10], an LDO regulator with a feed-forward ripple cancellation (FFRC) technique is proposed. The LDO is implemented in 0.13 m CMOS technology and achieves a PSR better than 56 dB up to 10 MHz for load currents up to 25 mA [10]. A load regulation of 1.2 mV for a 25 mA step is measured, and the LDO consumes a quiescent current of 50 μA with a bandgap reference circuit included [10]. The main advantage of this FFRC approach is achieving a high PSR for a wide frequency range, without the need to increase the loop bandwidth and hence, the quiescent power consumption [10]. The LDO achieves the worst PSR of 56 dB at 10 MHz for a load current of 25 mA. The pass transistor is implemented using a pMOS device with a minimum channel length and 2.4 mm width [10]. The total on-chip capacitance, which is used to compensate the amplifiers, is less than 5 pF. Two off-chip capacitors, each 2 μF, are used as the capacitive load of the LDO. The total active area of LDO is 0.1 mm including the bandgap circuitry [10].

The output of LDO is often used as the power supply of cellular phones, MP3 players, personal digital assistances (PDAs), numeral cameras, and so on. In these systems, a large load current is required. A high PSR LDO with a maximum output current of 300 mA is proposed in [26]. The LDO was designed with a standard TSMC 0.18 μm CMOS process. The input voltage range is 2 V to 3.5 V with a minimum dropout voltage of 200 mV [26]. The output voltage of the LDO is 1.8 V. The LDO has a maximum load current as large as 300 mA. The design requires a quiescent current of 153 μA. The LDO achieves the worst PSR of 59 dB at 1 KHz for a load current of 300 mA [26].

Off-chip LDOs or on-chip LDOs with off-chip decoupling capacitors are commonly used for rejecting supply noise. However, an off-chip capacitor cannot effectively reduce the supply noise at the point-of-load, due to the bond-wire effect [27]. A fully-integrated LDO with a fast transient response and full spectrum PSR is proposed in [27]. Tri-loop architecture that is based on the flipped voltage follower and buffer impedance attenuation techniques is presented in the design and verified in a 65 nm CMOS process [27]. The LDO requires 50 μA of total quiescent current. For a 1.2 V input voltage and 1 V output voltage, the measured undershoot and overshoot is only 43 mV and 82 mV, respectively, for a load transient of 0 to 10 mA [27]. The LDO achieves a PSR of 15.5 dB at 1 GHz and 12 dB at 5 MHz. The chip has an area of 260 x 90 μm^2, including 140 pF of stacked on-chip capacitors [27].

LDO regulators can be used to act as a postregulating stage to reject the ripple noise generated by the buck converter [28], [29]. An LDO for on-chip application with a PSR boosting filter circuit for enhancing supply noise rejection at a middle-to-high frequency over a wide loading range is presented in [28]. In order to extend the PSR bandwidth, an extra filter is added. The added filter will have an input proportional to the supply voltage. It will drive the gate of a power transistor together with the normal error amplifier [28]. For the PSR filter design, the total on-chip capacitance is 20 pF [28]. The LDO is experimentally verified with a standard 0.13 μm CMOS process and achieves a PSR of 40 dB at 1 MHz [28]. The regulator can operate with a supply voltage of 1.2 V with a nominal dropout voltage of 0.2 V at a maximum load current of 50 mA and quiescent current of 37.32 μA. Output load transient variation between 50 μA to 50 mA can be recovered within

400 ns with small overshoots/undershoots. The proposed LDO requires a chip area of 0.018 mm^2.

2.4 Sleep Transistor Review

Sleep transistors are effective to reduce leakage power during standby modes [30]. In [30], a distributed sleep transistor network (DSTN) is proposed. The DSTN is better than the cluster-based design in terms of the sleep transistor area and circuit performance. According to [31], the centralized sleep transistor design in [32], [33] suffers from large interconnect resistances between distant blocks. Such resistance has to be compensated by an extra-large sleep transistor area [30]. In contrast, such overhead can be avoided by having a local sleep transistor per cluster, as in a cluster-based sleep transistor design (CBSD), and a sleep transistor area can be further reduced by clustering the gates that do not switch simultaneously together to minimize the Maximum simultaneous switching current (MSSC) in the cluster [30]. The work presented in [30] purports that the DSTN approach assumes that conservative virtual-ground wires achieve (on average) a 49.8% sleep transistor area reduction and leads to a smaller performance loss [30].

Multithreshold CMOS (MTCMOS) has emerged as an effective technique for reducing subthreshold currents in standby mode while maintaining circuit performance. MTCMOS technology essentially places a sleep transistor on gates and puts them in sleep mode when the circuit is nonoperational [34]. The work in [34] presented a fine-grained approach where each gate in the circuit is provided with an independent sleep transistor. Since the fine-grained scheme has the potential for a very high area penalty, a standard cell-placement-driven sizing methodology is presented [34]. To this end, an optimal

polynomial-time fine-grained sleep transistor sizing algorithm is utilized. According to [34], on average, the sleep transistor placement and optimal sizing algorithms gave 50.9% and 46.5% savings in leakage power as compared with the conventional fixed-delay penalty algorithms for 5%and 7% circuit slowdown, respectively [34].

Power Gating is effective for reducing leakage power. Previously, a DSTN was proposed to reduce the sleep transistor area by connecting all the virtual ground lines together to minimize the Maximum Instantaneous Current (MIC) through sleep transistors [35]. In [35], methodologies for determining the size of sleep transistors of the DSTN structure considering a charge-balancing effect is proposed [35]. The worst-case IR drop across a sleep transistor takes place when the corresponding MIC flows through it. The minimum size of a sleep transistor can be calculated based on both the MIC and the IR-drop constraint [35]. According to [35], in the DSTN scenario, the charge balancing effect greatly complicates the sleep transistor-sizing problem. However, since the DSTN relies on tying all virtual ground lines together, the traditional ways of relating the independent clusters MIC cannot assure the quality of the final sizing [35]. The main idea of [35] is to consider the charge balancing effect and introduce the fine-grained *MIC*(*Ci*) within a clock period from a temporal perspective [35]. Each cluster *Ci* is connected to the corresponding sleep transistor *STi* and to other sleep transistors by virtual ground. The *MIC*(*Ci*) is defined as the MIC of cluster *Ci* and *MIC*(*STi*) as the MIC flowing through sleep transistor *STi* [35]. As stated in [35], on average, the sizing algorithm presented in [35] can achieve a 37.5% size reduction than that in [30].

The conventional sleep transistor sizing schemes do not consider the resonant supply noise that represents the worst-case supply disturbance [36]. The work presented in [36] investigates the impact of sleep transistor sizing on different on-chip noise components and shows that, contrary to conventional wisdom, a larger sleep transistor is not always favored in term of performance when the resonant supply noise is taken into account [36]. To achieve a smaller supply droop, a larger sleep transistor is conventionally preferred to introduce less resistance on the supply path. However, the leakage saving with a larger sleep transistor is smaller due to the weaker collapse of the virtual supply during idle periods in the circuit [36]. In order to deal with the sporadic nature of the resonant, [36] proposed an adaptive sleep transistor circuit that adjusts the size of the sleep transistor on the fly to remove the DC noise penalty of the fixed sizing scheme. Simulation results on 32 nm CMOS technology are used to demonstrate the functionality and effectiveness of the proposed adaptive sizing circuits [36]. Simulation results show that the proposed sizing scheme reduces the worst-case noise by 17% compared with the conventional sizing techniques. Smaller sleep transistors used in the scheme also lead to around 60% leakage and area savings [36].

Power supply noise has become a major design concern in recent years. Excessive power supply noise causes timing violations, reliability issues, and self-heating problems [37]. The work in [37] describes an optimal sleep transistor sizing method considering the dominant resonant supply noise. In addition, [37] proposed an adaptive sleep transistor technique where the effective sleep transistor width is varied on the-fly to damp the resonance noise only when it is detected. By doing so, the IR-drop penalty of the sleep

transistor can be eliminated when the resonance noise is not excited [37]. The objective of this approach is to increase the damping only when resonance is detected and maintains a small IR-drop at times when there is no resonant noise [37]. Simulation results on 32 nm CMOS show that the proposed technique achieves a 32% reduction of resonant noise and 17% reduction of total supply noise without having to trade off the IR-drop [37].

The work in [38] introduced the concept of reconfigurable sleep transistors, in which two different topologies are used in active versus sleep mode. In active mode, transistors are stacked as in traditional power gating schemes. In sleep mode, sleep transistors are reconfigured to reduce gate-induced drain leakage (GIDL) current, in addition to subthreshold leakage [38]. Conventional techniques are not effective in suppressing other leakage contributions such as GIDL of sleep transistors, which dominates at battery voltages (V_{DD}) of 3 V or higher [38]. In sleep mode, the sleep transistor conducts a leakage current that is dominated by either GIDL or subthreshold leakage, depending on the value of V_{DD} [38]. Measurements on a 180 nm CMOS test chip shows a 12.6× standby leakage reduction when the supply voltage is 4.0 V at 25°C temperature [38].

Power switches, also referred to as sleep transistors (STs) are implemented either as header or footer switches [39]. ST aging, due to Negative Bias Temperature Instability (NBTI) can considerably benefit leakage power saving. As a result, the effectiveness of power gating in terms of leakage reduction increases with ST aging [39]. In [39], an NBTI and leakage aware ST design method for reliable and energy efficient power gating is proposed. According to [39], as STs age, their leakage power drastically decreases, making

power gating techniques more effective over time. Therefore, the work in [39] advocates to renounce part of this leakage power over-reduction in order to counteract the detrimental effect of ST aging on IR drop and propagation delay, thus improving circuit lifetime and long-term reliability [39]. Through SPICE simulations, [39] shows a lifetime extension up to 19.9x and an average leakage power reduction up to 14.4% compared to standard STs design approach without additional area overhead [39].

CHAPTER 3

FULLY INTEGRATED ON-CHIP SWITCHING VOLTAGE REGULATOR

Voltage regulators are used to provide a stable power supply to the microprocessor. The conventional off-chip switching voltage regulator contains a passive floating inductor, which is difficult to be implemented inside the chip. In addition, the inductor takes up a very large chip area that hampers the scaling process and exhibits parasitic effects. These limitations make a passive inductor based on-chip regulator very unattractive for a system-on-a-chip (SOC) design and multi-/many-core environments. To circumvent the challenges, this chapter presents an alternative technique for an on-chip voltage regulator based on active circuit elements by replacing the passive LC filter in a buck converter. In the circuit layout, the proposed hybrid scheme utilizes a cascaded second order multiple feedback low pass filter (MFB LPF) along with buffers, driver switches, feedback error amplifier, and comparator circuitry. The presented fully on-chip voltage regulator combines a linear and a switching voltage regulator and employs two separate drivers for current and voltage sourcing. The amalgamation of the two regulators obviate the need to use a physical inductor and achieves high power efficiency near 78 %. Design and layout of the circuit is demonstrated on Cadence Virtuoso tools.

3.1 Introduction

Miniaturization and proliferation of portable electronic gadgets along with robust energy storage systems elevate the need for better power management techniques. Due to the quadratic dependence of the dynamic switching power and the more than linear dependence of the subthreshold and gate leakage power on the supply voltage, power

dissipation is significantly reduced when portions of a microprocessor operate at a lower voltage level. A linear relationship exists between the current demand and power consumption [17]. A fast switching, well-regulated, and highly efficient voltage regulator is needed to provide stable supply voltage. However, the supply voltage of an IC is dictated by the system supply that is not scaled fast enough to keep up with advances in the IC technologies. Therefore, a regulator that can bridge the supply gap between the system and internal circuitry needs to be integrated on the IC [40]. However, integration of the regulator onto the chip presents many challenges. Reducing on-chip filter capacitor limits the total amount of instantaneous charge available to the load, which then introduces a higher susceptibility of a large dI/dt event that can cause large voltage fluctuations [19]. Additionally, on-chip inductor sizes must be drastically reduced, resulting in a higher switching frequency but lower conversion efficiencies with low inductance, which limits the amount of power it can deliver. Typically, they are fabricated as part of the package or placed in the PCB board outside the chip. In some regulator designs, on-chip spiral inductors can be employed. However, spiral inductors take up a very large chip area that hampers the scaling process and exhibits parasitic effects.

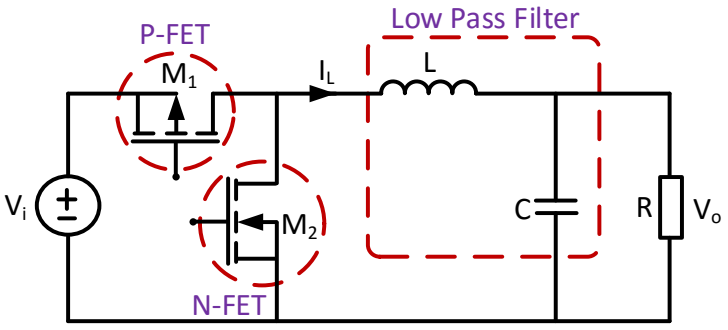

Figure 3.1: General implementation of buck converter circuit

Power management integrated circuits (PMIC) are the SOC power portion of the design. It encompasses, switching regulators, voltage reference circuits, LDOs (low dropout regulators), battery charging circuits, and others. Switching voltage regulators are found in nearly all electronic systems. They are essential for delivering power from an energy source to discrete circuit blocks or integrated circuits at their respective and desired voltage levels. Conventional switching regulators (see Figure 3.1) are typically off-chip devices made of large power transistors and passive filter elements. As the demand for smaller portable devices increases with more SOC integration, miniaturization of ICs (including voltage regulators) are expected to trail a similar trend. Currently, there is a great push for on-chip integration of voltage regulators for better management of power, temperature, and load or activity migration among circuit blocks or cores. An on-chip regulator is critically important for SOC and multi-/many-core ICs, because based on activity levels of different blocks or cores in high-density and high-performance ICs, it can enable the voltage to be adjusted in nano or pico second time. As a potential solution, three approaches are mostly used in designing switching voltage regulators. The first one is to utilize the packages of the host ICs to integrate filter elements [41], [42]. The second approach is to employ air-core surface mount inductors on top of the chip [43], [44], and the last method is to incorporate more complex PMICs for stand-alone applications by integrating the entire regulator within the chipset. Current and future ICs with multi-voltage SOCs demand for a robust design that can be scalable, on-demand adjustable and on-chip voltage regulators. Many works by various research groups are presented seeking better on-chip switching regulators [7], [8], [16], and [45]. As a potential solution, this chapter

focuses on inductorless, fully integrated on-chip voltage regulator design and implementation.

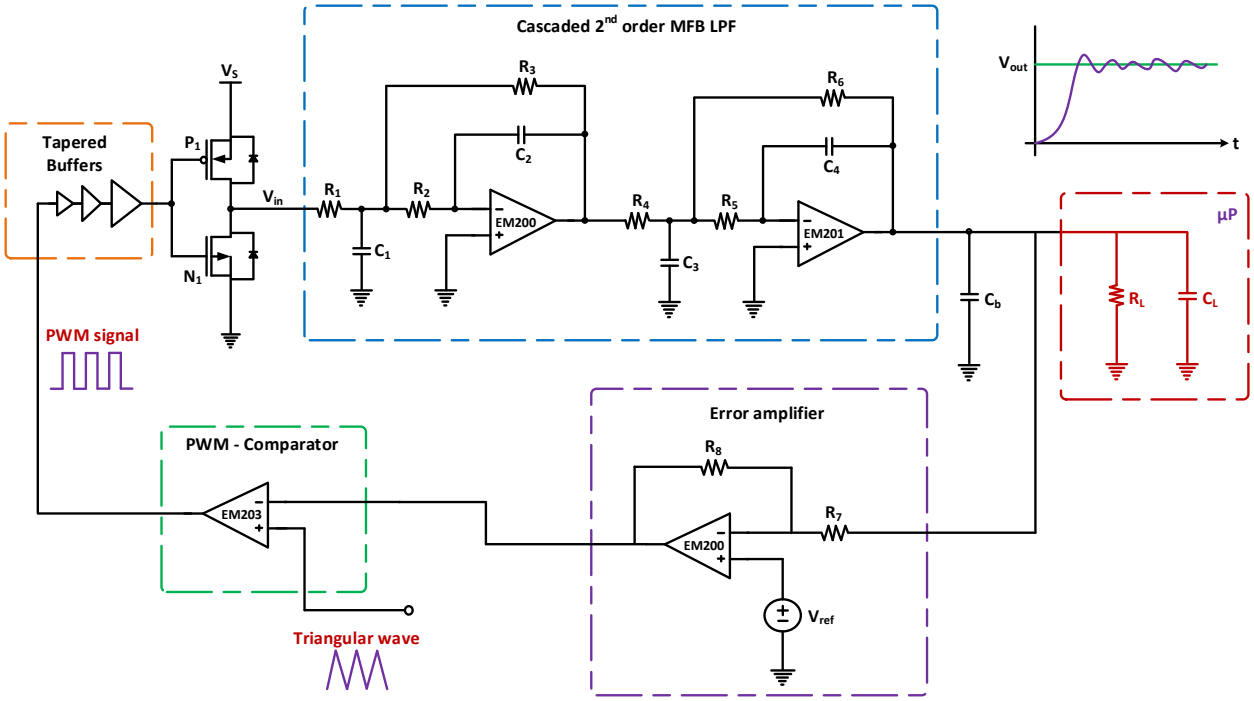

Figure 3.2: Proposed hybrid on-chip switching voltage regulator (SVR) circuit implementation

3.2 Hybrid On-chip Switching Voltage Regulator Design

The approach used for an on-chip regulator design in this chapter is to replace the passive low pass filter (see Figure 3.1) with an active device. The method combines switching and linear regulators and utilizes two separate drivers for current and voltage sourcing. As shown by Figure 3.2, the proposed design is composed of tapered gate drivers, driver switches, a cascaded 2nd order multiple feedback loop low pass filter (MFB LPF), error amplifier, and comparator. The proposed design can generate adjustable output voltage between 0.5 V to 1.5 V and 100 µA to 150 mA output current from 2.5 V input voltage. In addition, the architecture is inductorless and fully integrated on-chip design. It

takes a 0.5 mm X 0.5 mm area, has a settling time of 2.5 µs, 78 % efficiency, an output voltage ripple ±8 mV, and operating frequency of 5 MHz. The design requires a reference voltage input, a triangular signal, and a DC voltage source. Depending on the reference voltage setting, the driver switches open and close to generate a noisy voltage. The voltage is then filtered through the MFB LPF and a smoother output voltage signal is generated at the output. The second stage of MFB LPF is also the current generation node. Depending on the load variation and output voltage ripple, the error amplifier amplifies the signal to be corrected. The comparator then takes the signal and moves it up and down to adjust the duty cycle. This last stage is where the pulse-with modulation signal (PWM) is generated and adjusted. The tapered gate drivers then respond to the PWM signal to switch the driver switches accordingly.

The buck regulator shown in Figure 3.1 operates by opening and closing the alternative switches. When the top switch is closed (on), the bottom switch is reverse biased by the voltage source and no current can flow through it. When the top switch is open (off), the input voltage applied to the circuit is removed and the bottom switch is forward biased. These power switches of the LC switching voltage regulator are controlled by a PWM signal. PWM is a technique that generates control signals to manage pulse width. The output voltage of the regulator is controlled by the duty cycle, and the duty cycle (D) is defined by the switch on time (ton) divided by the total period (Ts). The PMW signal allows the regulator to switch on/off, which enables the LC buck regulators to achieve high efficiency. The drawback of the simultaneous switching is the introduction of unwanted voltage ripple. In an LC based buck regulator, an alternating switches are used as driver

transistors. The same design approach is mimicked here in the active on-chip hybrid implementation using large NMOS and PMOS transistors. Similar to a conventional buck converter, the output voltage of the proposed regulator can be described mathematically as in (3.1) [16].

$$V_o = \frac{1}{T_s}\int_0^{T_s} V_o(t)dt = \frac{t_{on}}{T_s}.V_{in} = D.V_{in} \tag{3.1}$$

3.3 Active Filter Design

Active filters require one or more operational amplifiers, but passive filters do not. In addition to being SOC friendly, one of the main advantages of having active filters is to boost the signal via gain. An active filter based on-chip voltage regulators can deliver power at a very high frequency. On-chip filters also require smaller filter elements and provide a faster response to changes to the load. One of the few disadvantages of having on-chip regulation is the total amount of instantaneous charge availability due to the smaller filter capacitors. Many of the low cost PMICs are integrated into the IC's package and are considered as SOC. For higher end stand-alone designs, a more complex and fully integrated on-chip PMIC requires the need to incorporate the regulators as part of the chipset.

The PMIC design in this work utilize MFB based active filters. As shown by Figure 3.3, in the filter arrangement, the first stage filter is a MFB LPF with a square pulse input. The non-inverting input of the op amp is grounded, which is great for reducing noise. The in-band signal gain is set by – (R_3/R_1). Additionally, R1 also sets the Q of the filter while having no influence over ω_o. Embedded within the filter is an Integrator comprised of R_2

and C_2, along with the Voltage FeedBack (VFB) op amp. This design normally needs to be implemented using a unity-gain stable VFB op amp, because the core gain element needs to be configured as an Integrator [46]. The embedded integrator enables the proposed PMIC design to go from switching input to stable linear output.

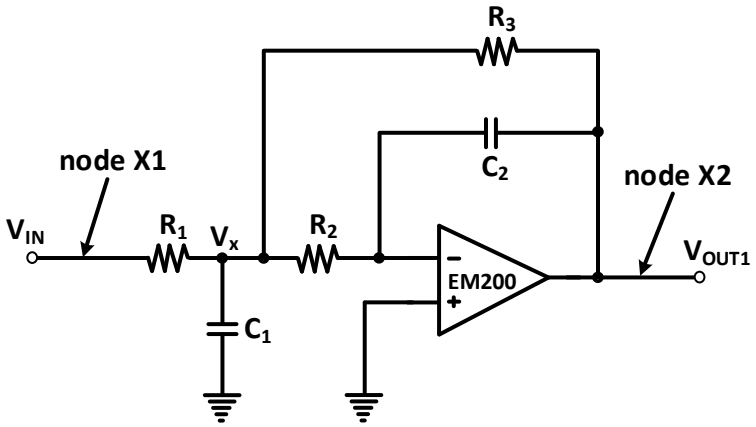

Figure 3.3: Second order MFB filter topology

Integrating circuits perform the mathematical operation of integrations with respect to time on a given input signal. It then generates an output voltage that is proportional to the applied input voltage integrated over time. During the first stage of MFB, as the input pulsates at a specific duty cycle, the continuous time square wave charges and discharges the feedback capacitor. This result in an integrated output by the MFB with a triangular wave output. During the first half cycle of the square shaped input when the signal is going from low to high, the current flows from the driver PMOS transistor through the input resistor. The same current flows through the feedback capacitor until the capacitor is charged. During the second half cycle when the signal is going from high to low, the direction of the current changes. The feedback capacitor now discharges generating a triangular wave. In the second MFB, the process is repeated to further integrate the

triangular wave, which is another triangular signal but with smaller amplitude. This stage also inverts the signal back.

As compared to the sallen-key, the MFB second order filter requires one more passive component. In sallen-key architecture, at low frequency the filter acts like a buffer. In the case of MFB, as shown by Figure 3.3, it acts like an inverting amplifier. The MFB is little more noisy as compared to the sallen-key filter, but the MFB has a direct DC path from the input to the output, which is critical factor when using it as part of the voltage regulator. Also, the MFB architecture inverts the signal, whereas in sallen-key, this is not an issue. In MFB architecture, without the feedback resistor, the system can be viewed to have an infinite DC gain. The feedback resistor, in parallel with the feedback capacitor, provides the filter to have finite DC gain. Since the gain is set by the ratio of the feedback resistor to the input resistor and the system no longer has infinite DC gain, it fixes the output offset to a constant value.

A second order Butterworth optimization is chosen for the on-chip voltage regulator design since precise regulation is required across the passband. Butterworth architecture provides maximum passband flatness. The filter also has an intermediate roll off factor in the time domain and less ringing in the frequency domain as compared with other filter structures. From Figure 3.3, by performing KCL at V_x and V_-, the MFB filter topology transfer function can be derived as a second order filter with two poles. The quality factor, corner frequency, and DC gain can be obtained from the transfer function as given below. Since the voltage regulator is operating at a higher frequency, the Q factor is low as expected.

$$A(s) = \frac{V_o}{V_i} = -\frac{1}{As^2 + Bs + C} = \frac{K\omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2} \tag{3.2}$$

$$A(s) = -\frac{\frac{R_3}{R_1}}{1 + \left(R_2 + R_3 + \frac{R_2R_3}{R_1}\right)Sc_2 + R_2R_3C_1C_2S^2} \tag{3.3}$$

$$K = -\frac{R_3}{R_1} \tag{3.4}$$

$$A = R_2R_3C_1C_2 \tag{3.5}$$

$$B = \left(R_2 + R_3 + \frac{R_2R_3}{R_1}\right)C_2 \tag{3.6}$$

$$C = \frac{R_1}{R_3} \tag{3.7}$$

$$Q = \frac{\sqrt{R_2R_3C_1C_2}}{\left(R_2 + R_3 + \frac{R_2R_3}{R_1}\right)c_2} \tag{3.8}$$

$$\omega_c = 2\pi f_c = \sqrt{\frac{1}{R_2R_3C_1C_2}} \tag{3.9}$$

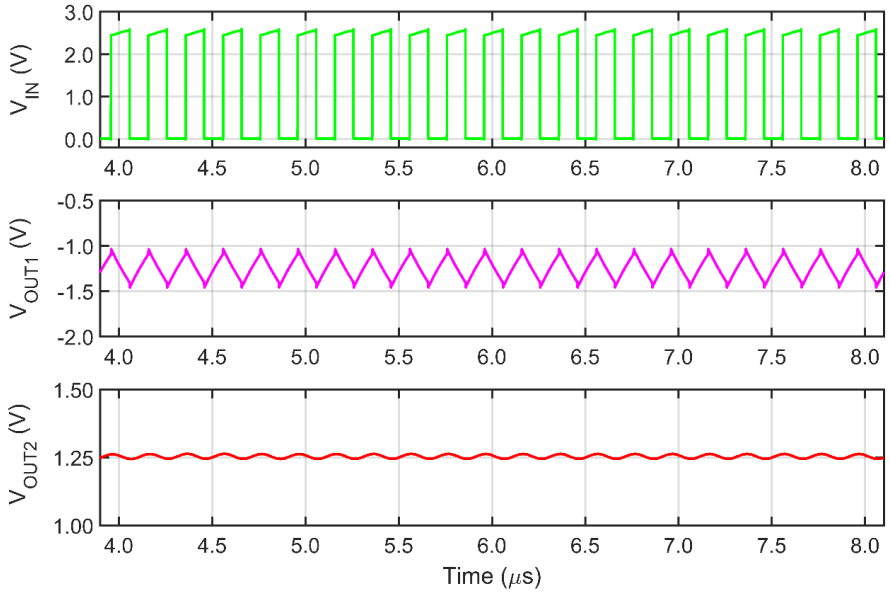

Figure 3.4: Integration stages of SVR at 50 % duty cycle

As shown by Figure 3.4, which is based on Figure 3.2, the input voltage at node X1 (V_{IN}) is switching at 50 % duty cycle from a 2.5 V source. At the next node X2 (V_{OUT1}), the output of the first stage filter integrates the square input to a triangular output while inverting the signal. At the output node (V_{OUT2}), the signal is integrated once more and inverted to generate a 1.25 V at the output. The low pass filter operating in the time domain integrates the square pulse into a triangular wave by charging and discharging the capacitors at a given frequency. Depending on the duty cycle, the output voltage can go up or down. The MFB filters integrate a switching input signal at a given frequency and converts it to a DC output voltage.

3.4 Output Stage Circuit Analysis

The first stage of the MFB filter is designed with a 70 dB gain and an 86^{o} phase margin two stage operational amplifier. Depicted by Figure 3.5, the second stage of the

MFB has a 73 dB gain and a 68^{o} phase margin. The op-amp at the last stage of the MFB filter is also the source of the output current. To generate the required output current, an operational transconductance amplifier (OTA) is used with a buffer output stage. OTA at a specified input behaves as a voltage controlled current source (VCCS). An OTA without a buffer can only drive capacitive loads. A resistive load (unless the resistor is very large) will kill the gain of the OTA [47]. In the output buffer stage, the PMOS transistor M10 is the source of the regulator current, so it is made very large to supply the necessary output current. In addition, the NMOS transistor M11 is also sized-up to be able to sink current.

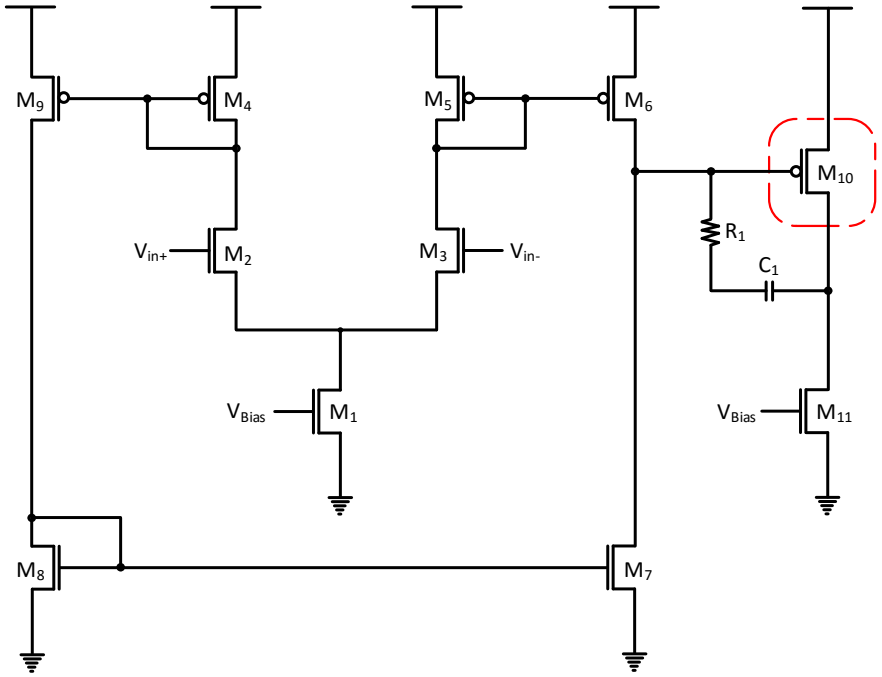

Figure 3.5: Operational transconductance amplifier with a buffer stage

The compensation capacitor C_C is used to stabilize the regulator at a higher load. If the voltage regulator drops suddenly, the decrease in voltage is fed back directly to the gate of M10 through C_C. This turns on M10 quickly and allows it to pull the voltage regulator back up bypassing the slower feedback system [47]. To maintain the stability and rapid

response to the load change, an on-chip bypass C_B is implemented. This capacitor is used to supply charges to a sudden current transient demand before the OTA responds to the load change.

M10 is sized based on the voltage drop value from a 2.5 V supply and expected maximum output current. For the bottom limit, a maximum 2.0 V voltage drop for a minimum V_{OUT} (0.5 V) voltage at a maximum output current of $I_{o(max)}$ = 300 mA is used to size the current source. In addition, for the upper limit, a 1.0 V voltage drop is considered for a maximum V_{OUT} (1.5 V) voltage with a maximum output current $I_{o(max)}$ = 150 mA is also considered. However, the actual output current depends on the load requirement that the SVR can supply as $I_{o\,(max)} = Ip_{10(source)} - In_{11(sink)}$. The M10 transistor is 2.5 times the NMOS current sink M11 transistor. Depending on the output load requirement, the output current source is adjusted via V_{sg} change at M10. The width and length of the current source is designed based on equations (3.10) and (3.11).

$$V_{DO} \leq R_{DS(\max)} I_{O(\max)} \approx \frac{I_{O(\max)}}{K_p \left(\frac{W}{L}\right)(V_{SD} - |V_{TP}|)} \leq 200\ mV \tag{3.10}$$

$$\frac{W}{L} \geq \frac{I_{O(\max)}}{K_p V_{DO} \left(\frac{W}{L}\right)(V_{SD} - |V_{TP}|)} \tag{3.11}$$

3.5 Drivers and Buffers

The transistors MP_1 and MN_1 are the driver switches of the voltage regulator. The output of this stage generates a square pulse (V_{in}) depending on the duty cycle as shown

by Figure 3.6. The regulator is designed for a minimum of 20 % and a maximum of 60 % duty cycle. At the maximum duty cycle, an output current I = Vin/R1 is supplied. Even though the driver switches are used to set the input voltage by periodically turning on and off, the proper size is required to lower the power dissipation, hence, efficacy is increased. Both driver switches W/L ratios are sized up to lower the R_{ds} of both transistors. During the charging cycle, the MP_1 driver is on making a series path with the filter resistor. If the transistor resistors are not lowered, it reduces the supply current. This affects the output regulated voltage by shifting it higher and manifesting a voltage variation at the output. It is pertinent to have the PMOS R_{ds} lower than 10 Ω to have innocuous voltage perturbation. The MN_1 transistor is also sized up to have a lower impedance path during the discharging cycle. The MP_1 driver switch is designed two times the MN_1.

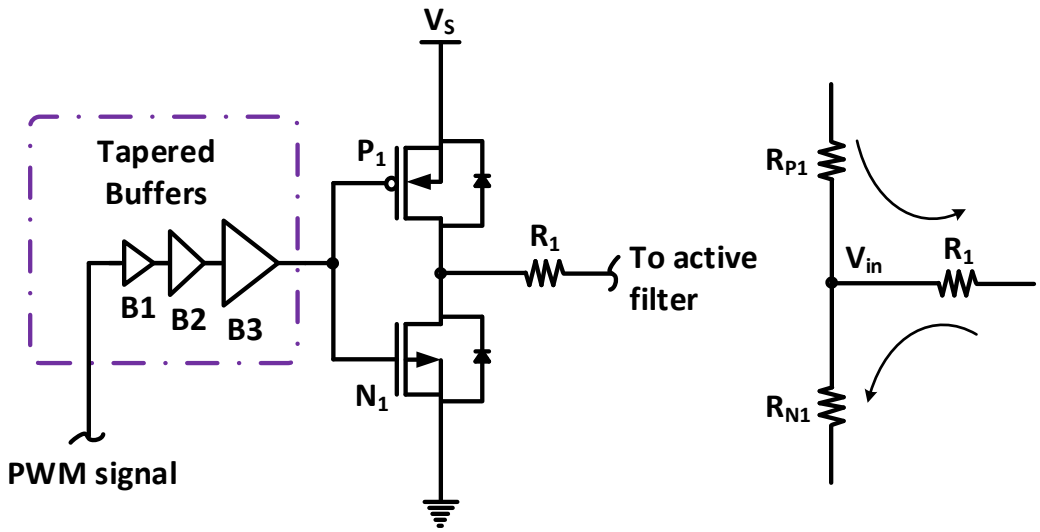

Figure 3.6: Tapered buffers and driver switches

The diodes are used in parallel with the driver switches to provide a momentary conduction path. This makes the current flow through the diode before the low-side driver

switch is turned on allowing the current to conduct during dead time. This technique increases efficiency by reducing the losses of the body drain diode in the driver switch. The buffer cells are designed using fan-in and fan-out techniques and making sure the high slew rate is achieved at each stage. The input resistance of each stage are kept as large as possible to reduce the input current. The resistance at the output of each stage is also lowered to increase the output current of each stage. The driving strength of buffer cell B2 is 4 times that of buffer cell B1, and buffer cell B3 is 8 times that of buffer cell B2. The fan-in and fan-out ratio of 1-4-8 is used to enhance the dynamic performance of the buffers.

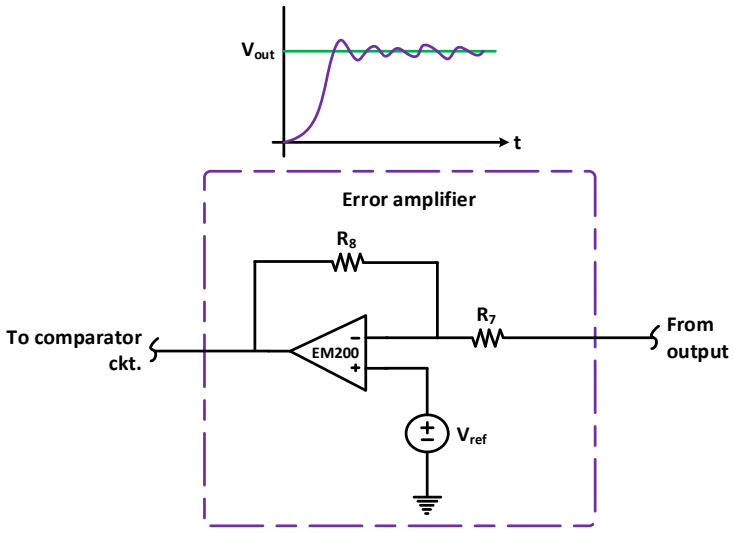

Figure 3.7: Error amplifier circuit of the proposed SVR

3.6 Error Amplifier Circuit

Depicted by Figure 3.7, the error amplifier is a two stage op-amp with a gain of 70 dB and an 86^o phase margin. It has two inputs, the reference voltage and the output voltage of the regulator. The inverting end of the amplifier is connected to the output of the voltage regulator with a gain factor of -R8/R7. The error amplifier stage is used for output voltage

ripple suppression and correction. As the voltage at the output node fluctuates up and down, the error amplifier compares the difference between the reference and the regulated output voltage and amplifies the error. This stage generates a V_{err} (ERROR) voltage that is used to adjust the voltage level by going up and down to correct for any oscillation at the output or sudden change in the load demand. The mathematical representation of the error amplifier stage is shown by equation (3.12). In addition, the reference voltage is used as a prelude to initiate the voltage regulation process at the error amplifier stage, which is dictated by the reference voltage and sets the desired regulated output voltage.

$$V_{err} = V_{ref}(R_7 + R_8) - V_{out}\left(\frac{R_8}{R_7}\right) \tag{3.12}$$

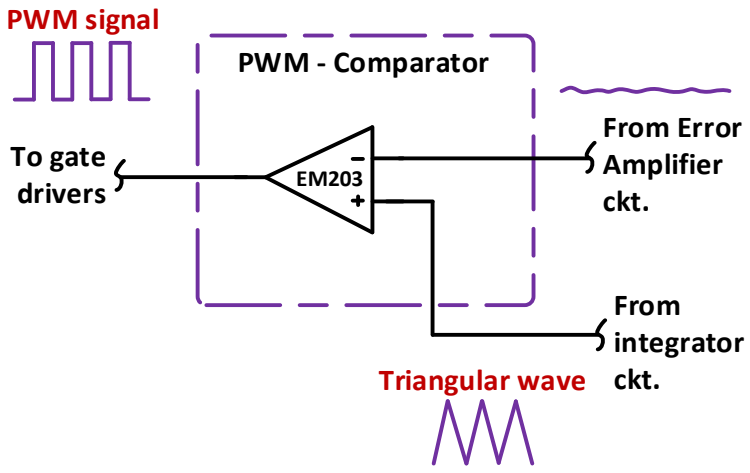

Figure 3.8: Comparator circuit of the proposed SVR

3.7 Comparator Circuit

The comparator circuit takes two types of input, one from the output of the error amplifier and the other from the triangular wave input signal generator. The basic op-amps can be used as a voltage comparator, in some less demanding low-frequency or speed

applications. For high frequency operations, a practical comparator with a push-pull architecture is used where propagation delay and sensitivity are important [47]. The comparator architecture has a 185 uA bias current (I_B), a 76 dB gain and is sensitive to discern a change in mV level signals. A block diagram of a high-performance comparator is shown in Figure 3.8. The comparator consists of three stages: the input preamplifier, a positive feedback or decision stage, and an output buffer [47]. The comparator decides between the error amplifier signal and triangular signal and generates a PWM signal. The on/off ration is dictated by the level of the error amplifier output signal. As this voltage level goes up and down, the width of the output pulse is adjusted. The duty cycle is set by vertically moving the error signal. The output of the comparator is directly connected to the first stage buffer.

3.8 Regulator Performance

Testing the stability of voltage regulation at low I_o, a maximum R_L with minimum C_L is considered. This allows the regulator to always supply a minimum output current of V_{OUT}/R_{Lmax}. At the lowest voltage setting, a 0.5 V output voltage is regulated with a 150 mA output current. At 5 KΩ the voltage regulator supplies a minimum current of 100 μA and maintains stability. The output stage OTA is designed for a large resistive load in mind to make sure the gain of the amplifier is not significantly lowered and also, most importantly, remains stable. For maximum C_L and minimum R_L, the highest amount of I_o is generated. Loads with higher C_L, beyond the specified value, will cause the phase margin of the OTA to deteriorate and move closer to an unstable state.

Efficiency is one of the most important parameters in power conversion. The application note provided by [48] and [49] explains how to perform an efficiency calculation for linear regulators and a conventional buck converter. In the design proposed here, a physical inductor is eliminated and the current and voltages are set separately by different driver switches. This means the given equation in [49] has to be slightly modified to account for the changes. As shown by equation (3.15), efficiency is a function of input voltage, quiescent current, output voltage, and output current. By minimizing the quiescent current and by lowering the input to the output range, a higher efficiency can be obtained. At full load, the efficiency is higher when compared with a light load. In addition, the efficiency of the proposed hybrid on-chip switching regular is lower than conventional buck converter but better than linear regulators.

$$P_{FET} = \left[\frac{V_o}{V_i} x\ (R_{DSON1} - R_{DSON2}) + R_{DSON2}\right] \tag{3.13}$$

$$P_D = P_{FET} + P_{IQ} \tag{3.14}$$

$$\eta = 0.5\ x \left[\frac{V_o\ x\ I_o}{I_o\ x\ V_o + P_D} + \frac{V_o\ x\ I_o}{(I_o + I_q)V_i}\right] x\ 100 \tag{3.15}$$

As depicted by equation (3.15), the efficiency of the proposed voltage regulator is the amalgamation of both switching and linear regulations. For the switching part, the switching loss of the drivers, as well as the quiescent current, are considered. For the linear regulator part, the quiescent current is added as part of the loss. The efficiency is the

average of both regulators. The power loss of the driver transistors can be obtained using the on resistance and output current. R_{DSON1} is the on-time drain-to-source resistance of the high-side MOSFET and R_{DSON2} is the on-time drain-to-source resistance of the low-side MOSFET [49]. In Figure 3.9, the efficiency of the switching part is shown in green, the linear is depicted in red, and the combined efficiency is shown in magenta. The switching loss caused by the driver switches at the switching input is minimized since a different current driver transistor performs the current sourcing linearly. The proposed voltage regulator has 79 % and 58 % efficiency at the output voltages of 1.5 V and 0.5 V (dotted magenta). At full load, the efficiency is higher when compared with a light load. As shown, the efficiency of the proposed hybrid on-chip switching regular is lower when compared to a conventional buck converter, but higher when compared to linear regulators.

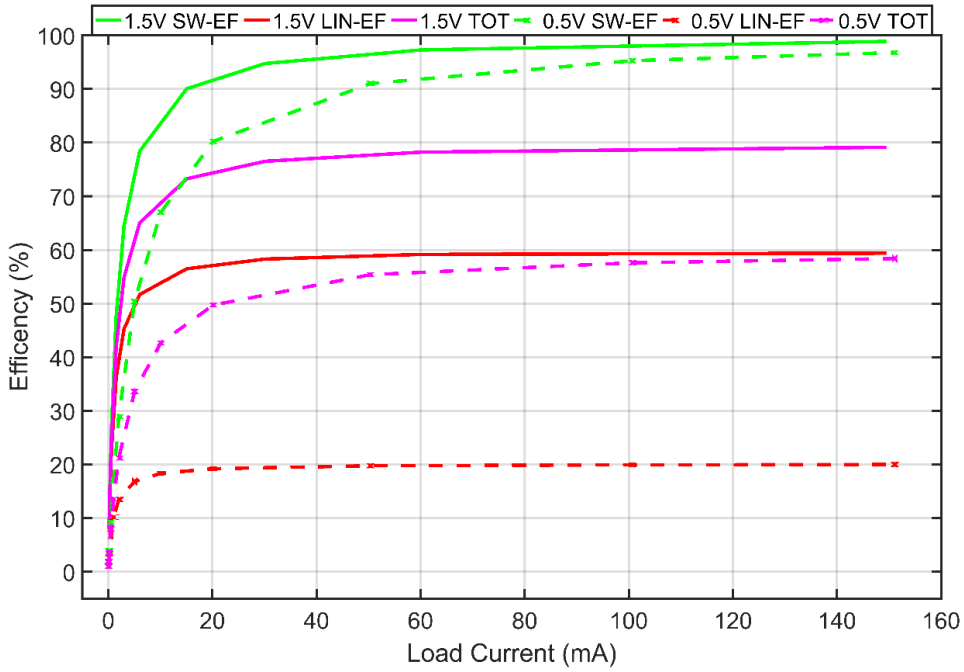

Figure 3.9: Proposed SVR efficiency for 1.5 V and 0.5 V voltages and load currents

Figure 3.10 shows the AC analysis for various voltage levels. The power supply rejection ratio (PSRR) is a key parameter for voltage regulators to determine the amount of input ripple generated by the energy source is mitigated at the output of the regulator. The operating frequency of the proposed voltage regulator is 5 MHz. At this frequency, the PSRR is especially important to decide if the output ripple is small enough to have a direct connection to the load or a linear regulator is needed for farther ripple suppression. In the proposed design, nearly a 145 dB PSRR is achieved in the frequency band until 1 MHz. Also, up until a 35 MHz frequency range, the voltage regulator can obtain above a 110 dB PSRR. Since the proposed regulator is going to be used in both standalone and in conjunction with a linear voltage regulator, higher ripple suppression is desired especially at the operating frequency.

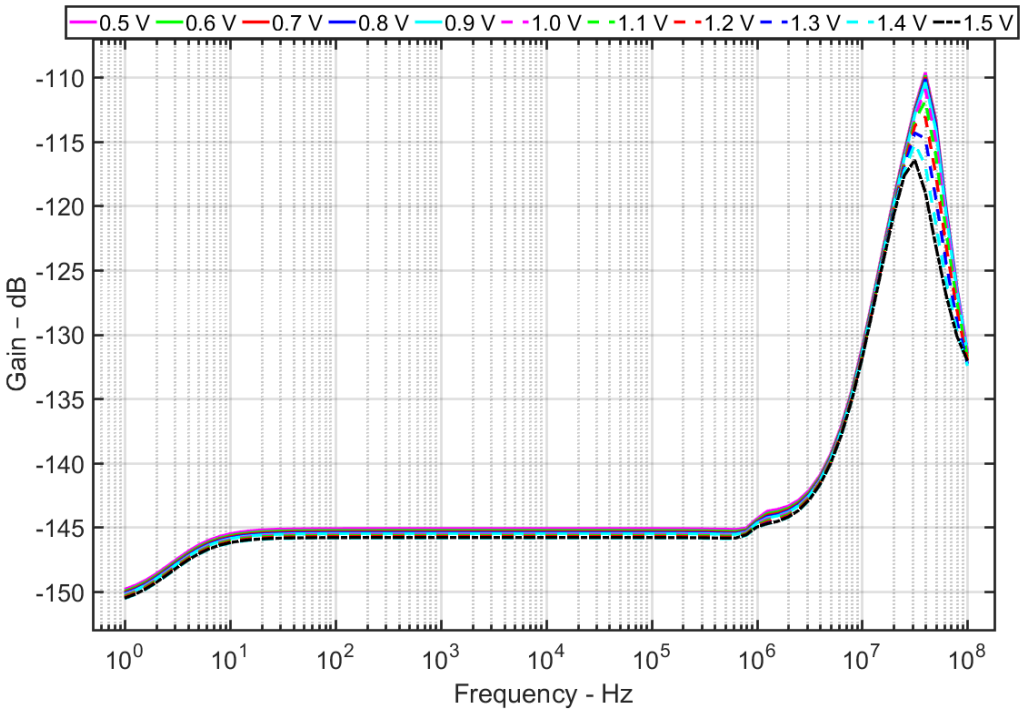

Figure 3.10: Proposed SVR AC analysis at various voltage levels

An important parameter, which is critical for stability of the voltage regulator, is the line regulation. Line regulation is a measure of the circuit's ability to maintain the specific output voltage with varying input voltage [48]. The line regulation is expressed via the percent change in the output voltage with respect to the change in the input voltage. Equation (3.16) shows the mathematical representation of the line regulation. In the proposed design, the voltage regulator can be varied between a maximum output voltage of 1.5 V and a minimum output voltage of 0.5 V. At near 500 mV voltage difference between the input and output, and for the line regulation of 1.5 V output, the input voltage is varied between 2.0 to 2.5 V. Also, for the line regulation of 0.5 V output, the input is varied between 1.0 to 2.5 V. At heavy load, the line regulations are 5.6 % and 2.0 % for 1.5 V and 0.5 V output voltages. In both cases, the feedback system of the SVR along with the reference voltage try to manage the changes in the input by adjusting accordingly. For a line transient response, the SVR is tested via a voltage step input with 10 ns rise and fall time. Figure 3.11 shows the input and output voltage transient response of the SVR for 1.0 V regulated output voltage at heavy (V_{OUTH}) and light (V_{OUTL}) load currents. In both heavy and light loads, the output voltage variation for step input between 1.5 V and 2.5 V is less than 32 mV. The line regulation for the light load is 2.82 % and 3.14 % for the heavy load as shown by Figure 3.11. Also, an overshoot and undershoot around ±18 mV is shown on the figure during the step input voltage transition.

$$Line\ regulation = \frac{\Delta V_o}{\Delta V_i} \tag{3.16}$$

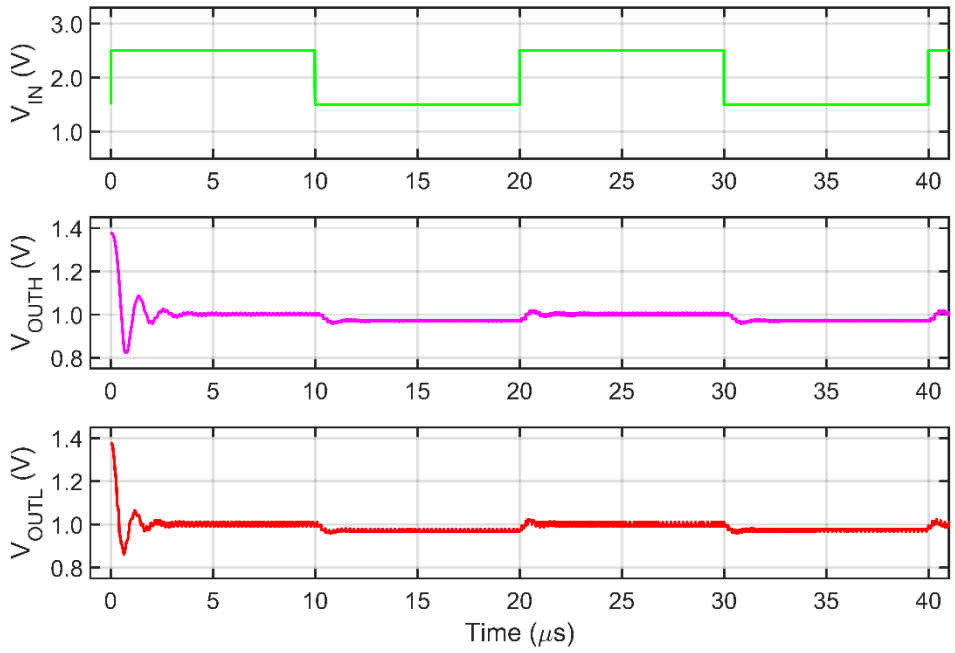

Figure 3.11: SVR line transient response for I_{out} = 100 mA and I_{out} = 200 µA

Another critical parameter for stability of the voltage regulator is the load regulation. Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions [48]. The load regulation is expressed in the percent change in the output voltage with respect to the change in the output current. Equation (3.17) shows the mathematical representation of the load regulation. The worst case of the output voltage variations occurs as the load current transitions from zero to its maximum rated value or vice versa [48]. At a 1.5 V output voltage with a maximum load variation, the output voltage varied by 8.7 mV. Also, at 0.5 V output, a 1.15 mV variation is witnessed as the load transitions from minimum to maximum. The load regulations are 5.8 % and 2.3 % for 1.5 V and 0.5 V output voltages. For the load transient response, the SVR is tested via a current step input with 10 ns rise and fall time. Figure 3.12 shows the

step input and output voltage transient response of the SVR for 1.0 V regulated output voltage. The output voltage variation for step current input between 0 and 100 mA is less than 3.8 mV. Also, an overshoot and undershoot around ±0.34 V is shown on the figure during the step current transition. The SVR takes a few cycles to stabilize after each current transition states.

$$Load\ regulation = \frac{\Delta V_o}{\Delta I_o} \tag{3.17}$$

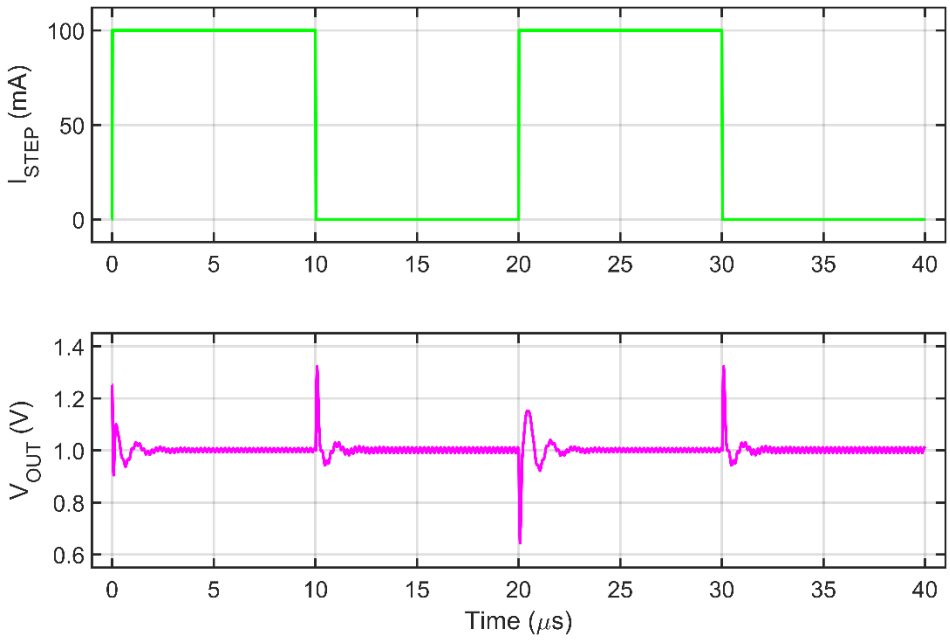

Figure 3.12: Load transient response of the proposed SVR

3.9 Simulation Results and Discussions

The second-order low pass MFB frequency response of the circuit is presented in Figure 3.13. In the design, Butterworth optimization is chosen since precise regulation is

required across the passband. As depicted by the Figure, Butterworth architecture provides maximum passband flatness. The frequency response at the end of the first filter is depicted in green (V_{OUT1}), the second filter is in blue (V_{OUT2}) and the combined filter response is shown in red (V_{TOT}). The simulation result is performed at full load. The general curve structure of the circuit frequency response follows closely with the ideal curve (magenta). The deviation from the actual curve resulted from the parasitic issues of the filter. The parasitic capacitors, filter resistors, and output stage filter OTA performance degradation at full load adds up at the output node causing a skew in the plot. In terms of the dynamic response of the system, the simulation result shows that the low frequency part of the input signal passed to the output and frequencies higher than the cutoff frequency (fc) attenuated.

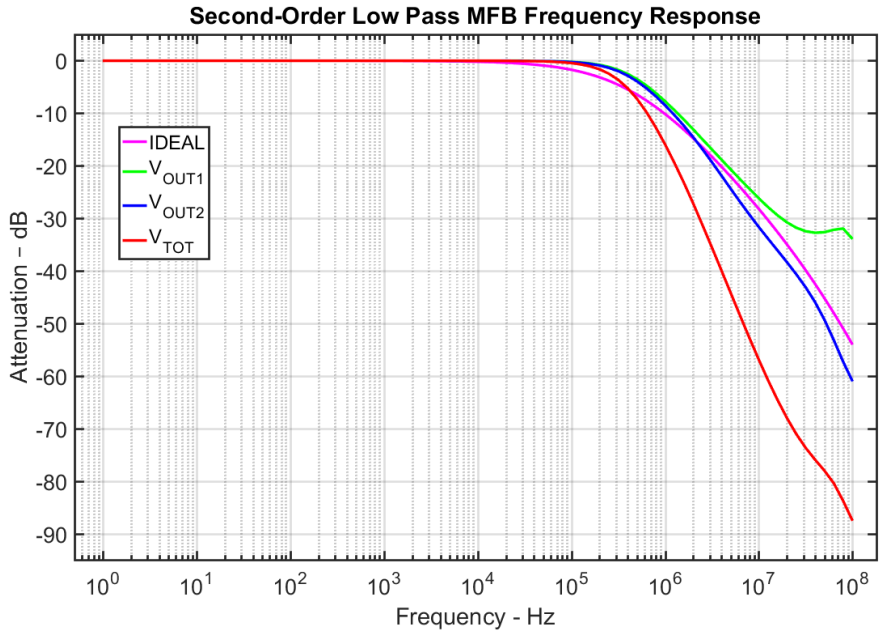

Figure 3.13: Second-order low pass MFB frequency response

Figure 3.14 shows the combined system performance of the voltage regulator at 0.5 V output voltage. In cyan (DRIVER), the output of the buffers that is the input of the driver

switches is shown. Represented by the magenta (V_{IN}) is the switching input to the regulator at 20 % duty cycle. The voltage is then integrated and shown in red (V_{OUT1}), which is also integrated again to become the output as depicted in blue (V_{OUT2}). The error amplifier then compares the output voltage with the reference value and sends the signal in green (ERROR) to the comparator. The comparator takes the signal and compares it with the triangular input signal shown in black (COMP). After this, the comparator generates the PWM signal and the process repeats to make any adjustments. As shown by the figure, the regulator takes a few cycles to adjust before settling to the prescribed voltage settings. In the simulation result, due to the input switches, a small oscillation in the output caused by the drivers is visible. The active filter is able to minimize the unwanted switching noise but not fully capable to completely eradicate it. The voltage ripple is well within a tolerable margin.

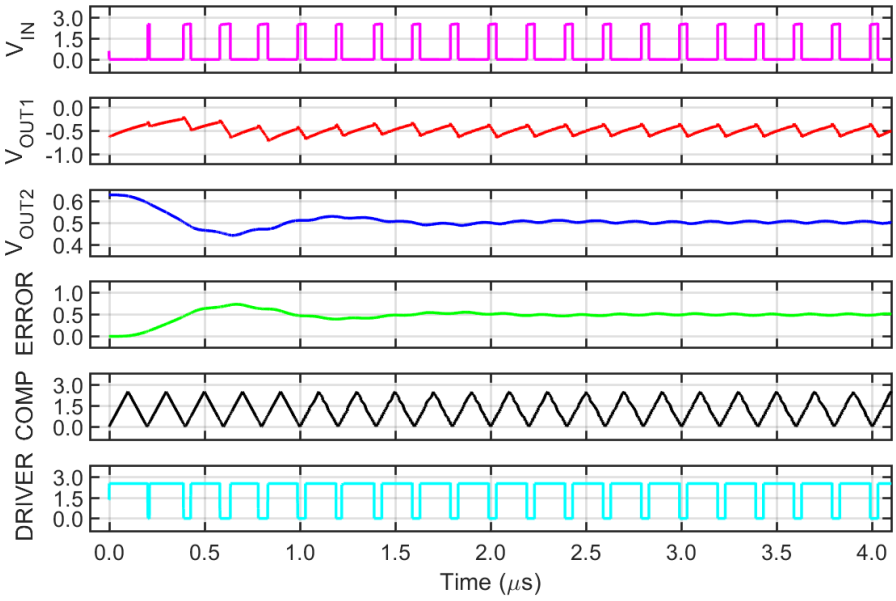

Figure 3.14: SVR system performance simulation for 0.5 V

The voltage regulator output current and voltage are presented in Figure 3.15. Output voltage ripple ±8 mV is witnessed at the end of the second filter. The voltage regulator is shown to be fully settled at around 2.5 µs. The proposed circuit is tested for various loads and the transient response of the output voltage and current corresponding to the input are obtained. When the system tested for loads from low to high at 60 % duty cycle, a worst-case output voltage fluctuation of 12 mV occurred from 1.5 V. A slight over-or-under shoot and almost no ringing are visible in the output of the transient voltage and current analysis. The regulator is notably vigilant to the abrupt changes in the load and responds swiftly to the demand. A switching frequency in both kHz and MHz range was used in the simulation with almost no change in the result. The switching signal can be increased with relatively lower power efficiency degradation. To maintain stability and rapid response to the load change, an on-chip bypass C_B is implemented. This capacitor is used to supply charges to a sudden current transient demand before the OTA responds to the load change.

A performance comparison table presented in [8] is slightly modified and shown in Table 3.1 and compares the proposed design with other existing converters. The proposed active hybrid on-chip regulator utilizes 0.5 mm X 0.5 mm on-chip area. The driver's large transistors take up a considerable portion of the chip area. The size of the driver transistors in the output stages can be adjusted according to the design requirements depending on the current demand, which will increase or decrease the chip size. The regulator is capable of supplying adjustable output voltage between 0.5 V to 1.5 V and 100 µA to 150 mA output current from 2.5 V input voltage. Depending on the required load, the output voltage can

be controlled via duty cycle. Since the regulator comprises both switching and linear regulators, the linear side causes the main power dissipation. The switching loss by the drivers is minimized since a different current driver transistor performs the current sourcing linearly. The proposed voltage regulator has 79 % and 58 % efficiency at the output voltages of 1.5 V and 0.5 V. The efficiency of the proposed hybrid on-chip switching regular is lower when compared to a conventional buck converter, but higher when compared to linear regulators. The voltage regulator can supply 225 mW of maximum power at a relatively high efficiency.

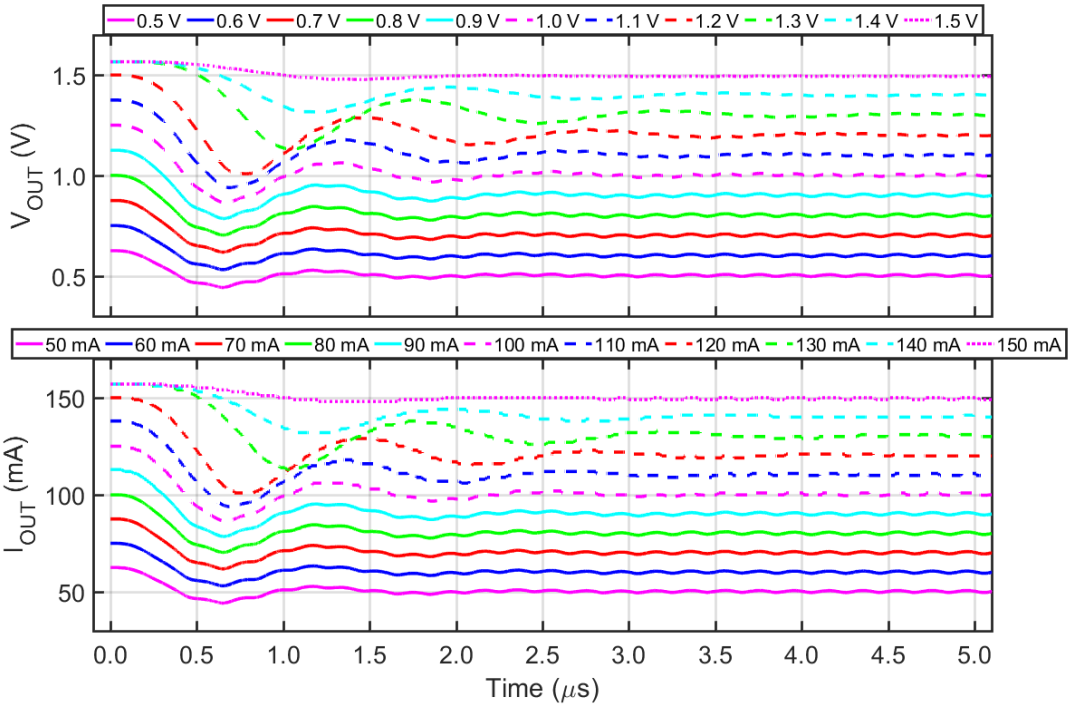

Figure 3.15: SVR transient response showing output voltage and output current

Table 3.1: Performance comparison among various designs

	[17]	[16]	[50]	[8]	**This work**
Type	Buck	Active filter	SC	Hybrid	**MFB SVR**
Technology [nm]	80	N/A	45	110	**500**
Response time [ns]	87	N/A	120 - 1200	72 - 192	**80 - 198**
On-chip area [mm^2]	12.6	N/A	0.16	0.015	**0.25**
V_{in} (V)	1.2	5	N/A	1.2	**1.0 - 2.5**
V_{out} (V)	0.9	1.8 – 3.3	0.8 – 1.0	0.9	**0.5 - 1.5**
I_Q (mA)	N/A	N/A	N/A	0.38	**0.53**
I_{max} (mA)	9500	N/A	8	80	**150**
Current efficiency (%)	N/A	N/A	N/A	99.5	**98.8**
Δ Output voltage [mV]	100	N/A	N/A	44	**±8**

3.10 Summary

In this chapter, we have introduced a hybrid active on-chip voltage regulator architecture for on-chip integration. The presented circuit offers an alternative topology and proposes a design approach with high power efficiency around 78 %. The proposed hybrid architecture utilizes cascaded second order multiple feedback low pass filter (MFB LPF) along with buffers, driver switches, feedback error amplifiers and comparator circuitry. This approach allows the highly efficient switching regulator to be combined with a linear regulator for a robust and highly efficient on-chip regulation. Extensive post fabrication analysis and experimental measurements have been performed to validate the

presented hybrid voltage regulator. The proposed design can generate adjustable output voltage between 0.5 V to 1.5 V and 100 µA to 150 mA output current to the load from a 2.5 V voltage source. Moreover, the architecture is inductorless and fully integrated on-chip design. It takes 0.5 mm X 0.5 mm area, has a settling time of 2.5 µs, 78 % efficiency, an output voltage ripple ±8 mV, and an operating frequency of 5 MHz. The innovative design closely matches the performance of a buck converter while obviating the physical inductor that is an integral part of the conventional buck converter. In addition, it offers an effective technique for SOC integration of a voltage regulator.

CHAPTER 4

HYBRID LDO VOLTAGE REGULATOR BASED ON CASCADED SECOND ORDER MULTIPLE FEEDBACK LOOP

As current and future ICs are moving towards system-on-a-chip (SOC) designs, integration of entire power management systems within a single chipset require new approaches. For ripple control, switching regulators are typically implemented along with low drop-out (LDO) regulators. The operating frequency of switching regulators is growing with a faster response time to meet the requirement of new generation multi-voltage high speed ICs. Accordingly, the design of LDOs needs to suppress the high-speed ripples by suppling a higher power supply rejection (PSR) over a wider frequency range. In order to realize the high PSR, this chapter presents a fully on-chip approach with a modified dual feedback loop LDO and active filter design. In the circuit layout, the proposed architecture utilizes a cascaded second order multiple feedback low pass filter (MFB LPF), inner and outer error correction loops, and driver switches. The presented fully on-chip hybrid LDO employs two separate drivers for current and voltage sourcing. The hybrid LDO achieves a PSR of -86 dB at 100 kHz and maintains above -62 dB until 10 MHz for load currents all the way up to 120 mA. Design and layout of the circuit is demonstrated on Cadence Virtuoso tools. Post fabrication experimental measurements and results are presented in the later sections.

4.1 Introduction

The demand for smaller portable electronic gadgets along with robust energy storage systems elevates the need for better power management techniques. Power delivery

for cellular phones, MP3 players, personal digital assistances (PDAs), cameras, and so on requires a stable and noiseless multi-voltage supply and a large load current [26]. These devices are typically powered with buck or switching voltage regulators along with LDOs. Switching regulators are very efficient in delivering power but introduce unwanted high frequency ripple voltage. LDOs are especially used to power oscillators, data converters, RF circuitry as well as other noise sensitive circuitry in wireless communication since these voltages have to be ripple free. In addition, LDO regulators are utilized to act as a post-regulating stage to reject the ripple noise generated by the buck converter [22], [28]. LDOs with large decoupling capacitors in a microfarad range are commonly used for rejecting switching noise [23], [27]. Large capacitors take an enormous area, but by suppressing the output ripple voltage, the overall power-supply rejection of the power delivery system improves.

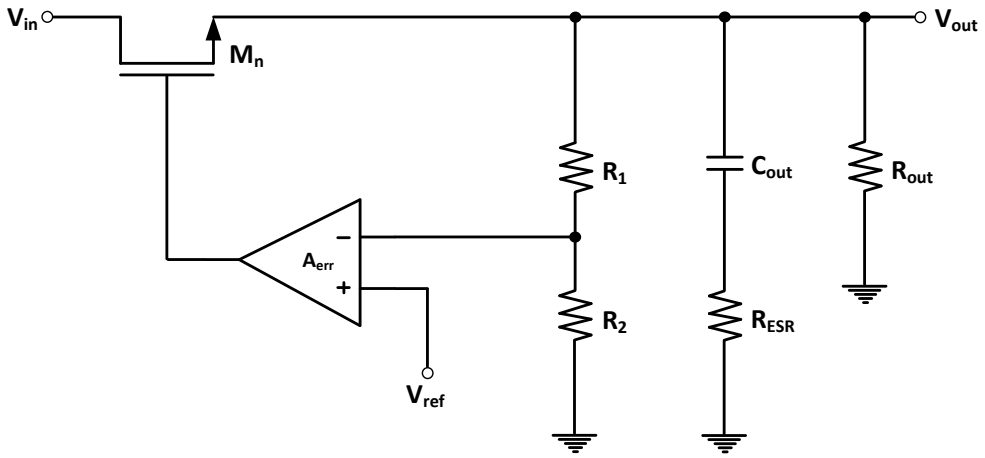

Figure 4.1: General Schematic of low dropout regulator (LDO)

Power management integrated circuits (PMIC) are the SOC power portion of the design. It encompasses, switching regulators, voltage reference circuits, LDOs, battery

charging circuits, and others. LDOs are found in nearly all electronic systems both as a stand-alone regulator or in synergy with a switching regulator. They are essential for delivering power from an energy source to discrete circuit blocks or integrated circuits at their respective and desired voltage levels. Conventional LDOs (see Figure 4.1) typically require a large output capacitor placed on the PCB or host IC's package for stability and have poor PSR at high frequencies (above 300 kHz) [10]. The bulky off-chip or on package capacitor takes a valuable area. Many capacitorless [23] [24] LDOs were proposed in the past including those with a capacitance multiplier [25] to mitigate the use of large capacitors. In addition, capacitorless designs or small on-chip capacitor based LDOs provide a better slew rate and enable greater power system integration in SOC. Also, as the demand for more SOC integration increases with a higher operating frequency above 1 MHz of switching regulator, the PSR of LDOs are expected to go up accordingly.

In the past few years, several LDO voltage regulator designs have been proposed to improve the PSR over wider frequency range. According to [10], potential PSR enhancement techniques can be generally classified in three main groups. The first method utilizes a simple RC or LC filtering at the input of the LDO [51]. The second approach is realized by cascading two LDO regulators [51]. The last approach employs various architectures; naming a few include the following: the feed-forward ripple cancellation (FFRC) approach [10], utilizing capacitance multiplier (c-multiplier) to emulate nanofarad-range capacitance [25], cascading filter along with the LDO [28], cascading pass transistor along with drain-extended FET devices [52], and tri-loop architecture based on a flipped voltage follower and buffer impedance attenuation techniques [27]. Each of the designs

have advantages and disadvantages based on their respective applications. Current and future ICs with multi-voltage SOCs demand for a robust design that can be scalable, have on-demand adjustability, and fully on-chip LDO voltage regulators. As a potential solution, this chapter presents a fully on-chip approach with a modified LDO with a dual feedback path and active filter design.

4.2 Hybrid On-chip Low Dropout Regulator Design

To improve the power supply rejection ratio (PSRR), the proposed design provides isolation between the input and the output voltage by inserting an active filter in between. The active filter acts as a stabilizer instead of large output capacitor. The design also employees two separate drivers for current and voltage sourcing. In addition, inner and outer feedback loops are implemented to monitor and correct the first stage and the output voltage for any changes. As depicted by Figure 4.2, the proposed design is composed of a pass transistor, two error amplifiers, and a cascaded second order multiple feedback loop low pass filter (MFB LPF). The proposed design takes an input voltage range between 1.4 V to 2.5 V. It can generate an adjustable output voltage between 0.5 V to 1.2 V and a 100 µA to 120 mA output current. In addition, the architecture is a fully integrated on-chip design and does not need an external capacitor for stability. It takes a 0.45 mm X 0.5 mm area, has a PSRR of -86 dB at 100 kHz and -62 dB at 10 MHz, has an output voltage ripple less than ±1 mV, and a 200 mV dropout voltage. The design requires a reference voltage input and a DC voltage source. Depending on the reference voltage setting, the input is adjusted by the first error amplifier and pass transistor to generate an input to MFB LPF. The voltage is then filtered through the MFB LPF and a smoother output voltage signal is

generated at the output. The second stage of the MFB LPF is also the current generation node. Depending on the load variation and output voltage ripple, the second error amplifier adjusts the input to the pass transistor. In correlation with the first error amplifier, the feedback system enables the pass transistor to make the necessary changes. The input to the MFP LPF and the output node are both monitored by the feedback system to match any changes between the two nodes.

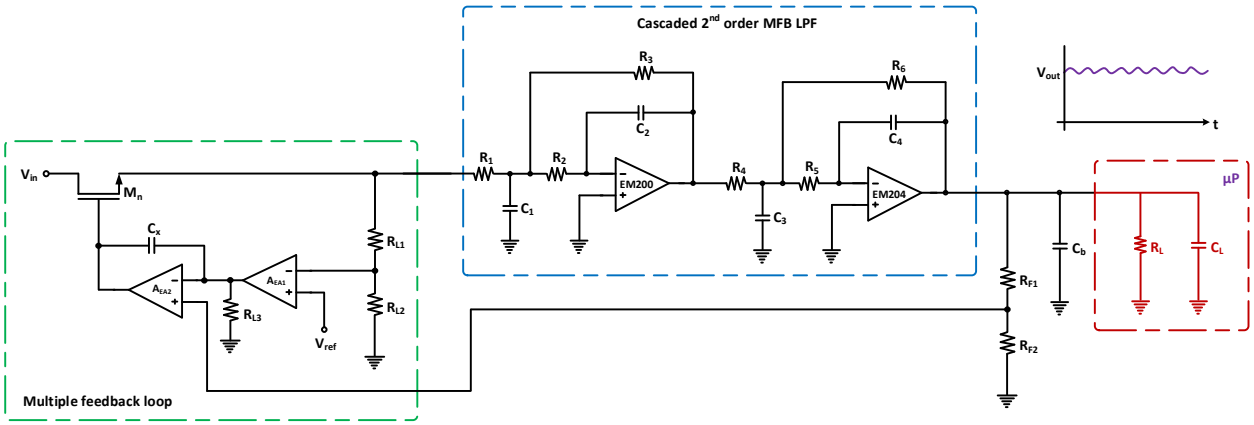

Figure 4.2: Proposed on-chip hybrid low dropout regulator (HLDR) circuit implementation

4.3 Active Filter Design

Active filters require one or more operational amplifiers, but passive filters do not. In addition to being SOC friendly, one of the main advantages of having active filters is to boost the signal via gain. An active filter based on-chip voltage regulators can deliver power at a very high frequency. On-chip filters also require smaller filter elements and provide a faster response to changes to the load. One of the few disadvantages of having on-chip regulation is the total amount of instantaneous charge availability due to the smaller filter capacitors. Embedded within the filter is an Integrator comprised of R_x and

C_x, along with the Voltage FeedBack (VFB) op amp. This design normally needs to be implemented using a unity-gain stable VFB op amp, because the core gain element needs to be configured as an Integrator [46]. The embedded integrator enables the proposed PMIC design to go from switching input to stable linear output. A more detailed analysis on MFB filter design and implementation is presented in chapter 3.

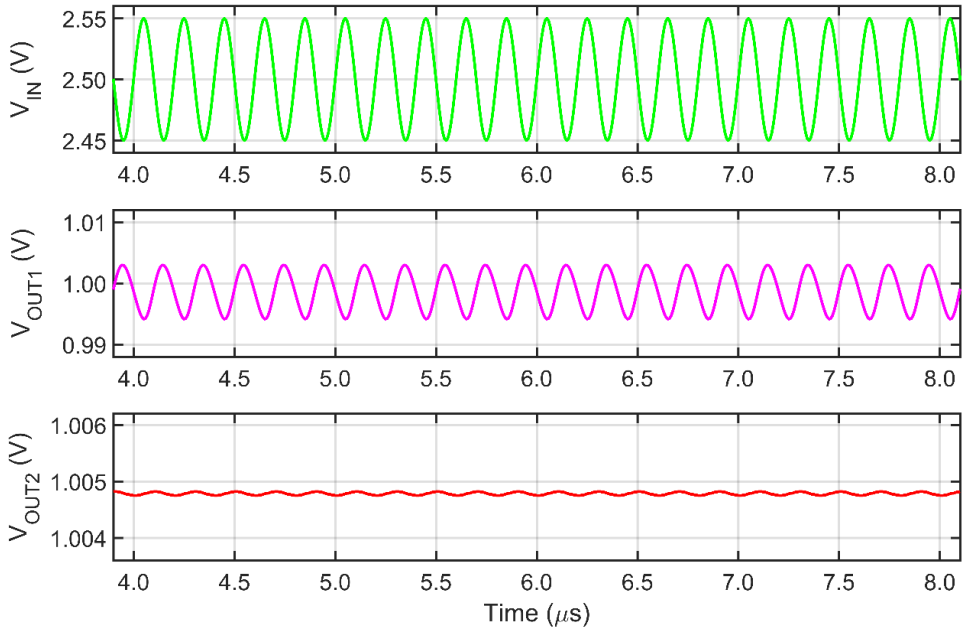

Figure 4.3: Integration stages of HLDR at 1.0 V output voltage

As shown by the Figure 4.3, which is based on Figure 4.2, the input voltage (V_{IN}) from external energy storage is shown in green with 2.5 V dc source and 100 mV noise oscillation. The hybrid LDO regulator reduces the oscillation depicted in magenta (V_{OUT1}) and passes the signal to the filter. Then, the MFB first stage filter integrates the output signal while inverting the signal. At the last MFB stage (V_{OUT2}), the signal is integrated once more and inverted to generate a stable DC 1.0 V at the output. The low pass filter operating in a time domain integrates a noisy oscillating dc signal by charging and

discharging the capacitors at a given frequency. Depending on the reference voltage, the output voltage can go up or down.

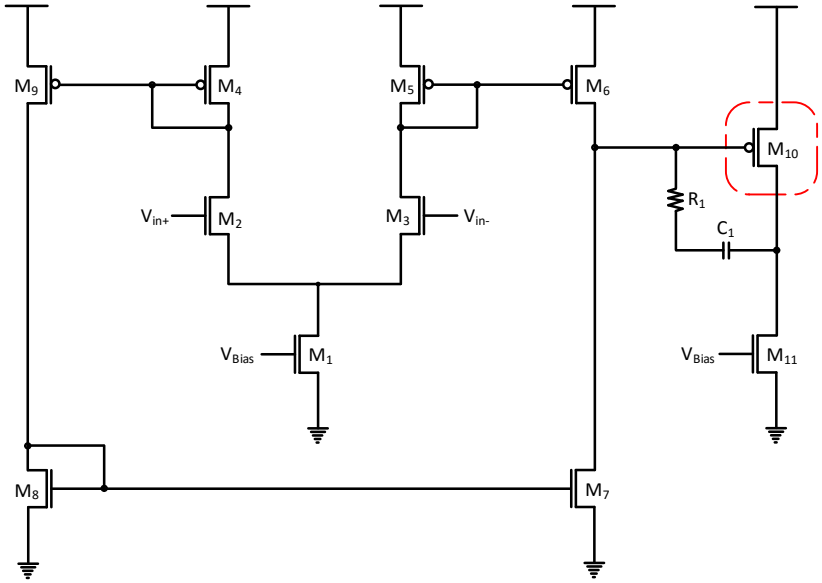

Figure 4.4: Operational transconductance amplifier with a buffer stage

4.4 Output Stage Circuit Analysis

The first stage of the MFB filter is designed with a 65 dB gain and a 65^{o} phase margin two stage operational amplifier. Depicted by Figure 4.4, the second stage of the MFB has a 70 dB and a 65^{o} phase margin. The op-amp at the last stage of the MFB filter is also the source of the output current. To generate the required output current, an operational transconductance amplifier (OTA) is used with a buffer output stage. OTA at a specified input behaves as a voltage controlled current source (VCCS). An OTA without a buffer can only drive capacitive loads. A resistive load (unless the resistor is very large) will kill the gain of the OTA [47]. In the output buffer stage, the PMOS transistor M10 is the source of the regulator current, so it is made very large to supply the necessary output current. In addition, the NMOS transistor M11 is also sized-up to be able to sink current.

The compensation capacitor C_C is used to stabilize the regulator at a higher load. If the voltage regulator drops suddenly, the decrease in voltage is fed back directly to the gate of M10 through C_C. This turns on M10 quickly and allows it to pull the voltage regulator back up bypassing the slower feedback system [47]. To maintain the stability and rapid response to the load change, an on-chip bypass C_B is implemented. This capacitor is used to supply charges to a sudden current transient demand before the OTA responds to the load change.

M10 is sized based on the voltage drop value from a 2.5 V supply and expected maximum output current. For the bottom limit, a maximum 2.0 V voltage drop for a minimum V_{OUT} (0.5 V) voltage at a maximum output current of $I_{o(max)}$ = 300 mA is used to size the current source. In addition, for the upper limit, a 1.3 V voltage drop is considered for a maximum V_{OUT} (1.2 V) voltage with a maximum output current $I_{o(max)}$ = 195 mA is also considered. However, the actual output current depends on the load requirement that the HLDR can supply as $I_{o\,(max)} = Ip_{10(source)} - In_{11(sink)}$. The M10 transistor is 2.5 times the NMOS current sink M11 transistor. Depending on the output load requirement, the output current source is adjusted via V_{sg} change at M10. The width and length of the current source is designed based on equations (3.10) and (3.11) (Chapter 3). Also, at the minimum voltage supply of 1.4 V for a maximum output current and output voltage at the specified W/L result in a minimum voltage drop near 200 mV.

The dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage [48]. The dropout voltage is expressed in terms

of its on-resistance and output current as stated by equation (3.10). Figure 4.5 shows the HLDR dropout regions. The dropout region for both first LDO stage (V_{OUT1}) and entire HLDR (V_{OUT2}) is depicted in the figure. It is difficult to tell from the simulation plot but within 180 mV dropout region, the voltages start to level out and settle to a stable output at 200 mV. Below this prescribed dropout region, the HLDR does not operate properly. Low dropout voltage is necessary to maximize the regulator efficiency [48]. A slight DC shift is shown between the first LDO stage and HLDR output but for the most part, they are overlapping each other especially at higher output voltages. The figure also displays the dropout regions and the regulation regions for various output voltages.

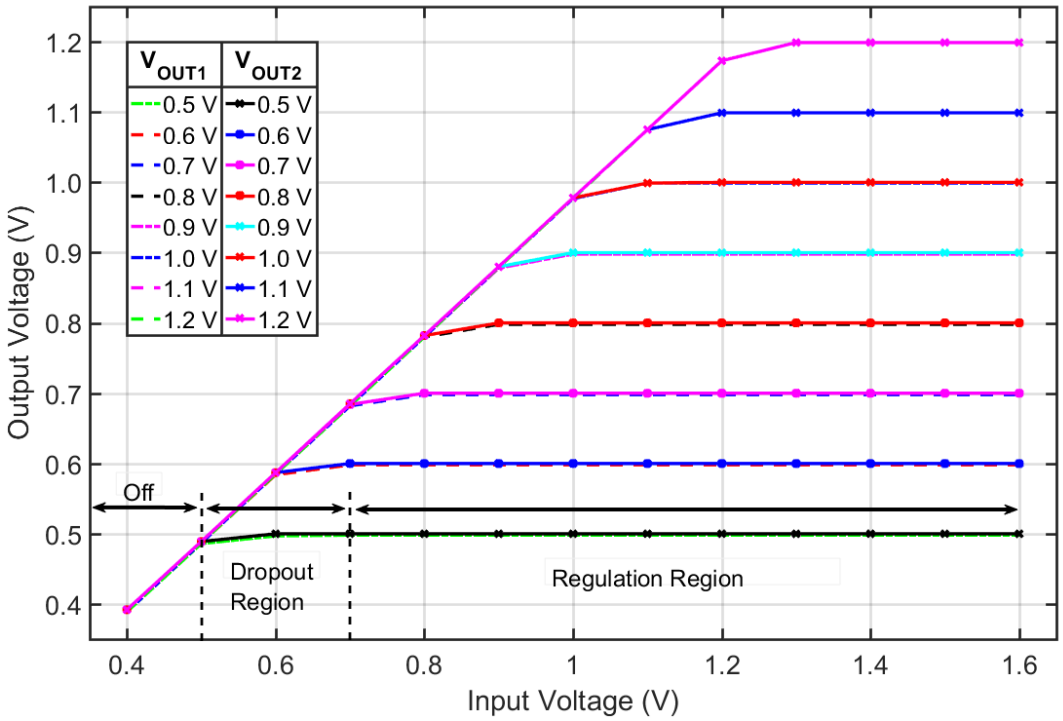

Figure 4.5: HLDR dropout region analysis

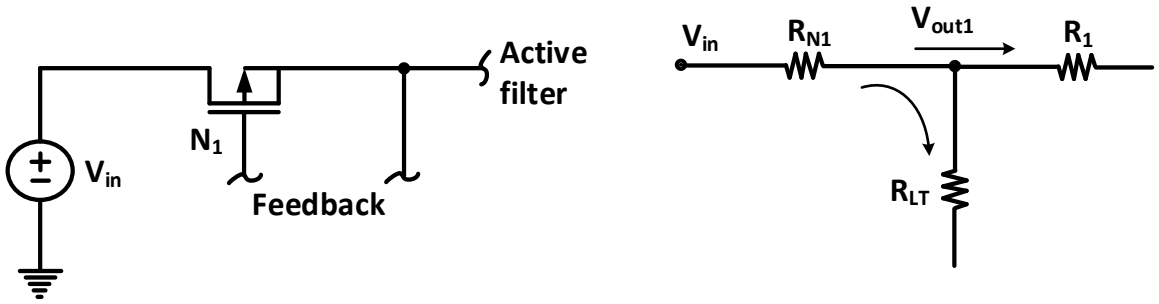

Figure 4.6: Driver switch of the HLDR

4.5 Driver Switch Design

The transistor M_n is the driver switch of the voltage regulator. The output of this stage generates a noisy oscillating voltage depending on the reference value as shown by Figure 4.6. The regulator is designed for a minimum of 200 mV and a maximum of 2 V dropout voltage. At the maximum output voltage, an output current I_{o1} = Vout1/ (R1 // R_{LT}) is supplied to the inner node. The driver switch W/L ratio is sized up to lower the R_{ds} of the transistor and supply I_{o1}. If the transistor resistors are not lowered, it reduces the supply current. This affects the output regulated voltage by shifting it higher, manifesting a voltage variation at the output. It is pertinent to have the R_{ds} lower than 10 Ω to have innocuous voltage perturbation. In addition, the feedback resistors as well as filter resistors are high to lower the amount of supplied current I_{o1} to the inner node. This is important since a different driver in the OTA performs the current sourcing. The main purpose of the driver M_n is to set the voltage part of the regulation.

4.6 Error Amplifier Circuit

Depicted by Figure 4.7, the error correction is performed by two different error amplifiers, A_{EA1} and A_{EA2}. The first error amplifier A_{EA1} is a two stage op-amp with a gain

of 65 dB and a 65^{o} phase margin. It has two inputs, the reference voltage and the output voltage of the inner stage. The second error amplifier A_{EA2} is a single stage op-amp with a gain of 38 dB. It has two inputs, the output of the first stage error amplifier and the output voltage of the regulator. The error amplifier stages are used for voltage ripple suppression and correction. As the voltage at the inner node fluctuates up and down, the A_{EA1} error amplifier compares the difference between the reference and the first stage HLDR and amplifies the error. The output resistor R_{L3} is utilized to lower the gain and improve the bandwidth of the first stage of the amplifier. This allows the regulator to maintain the PSRR for a wider frequency range. The output is then fed to the second error amplifier. The A_{EA2} compares the value with the output of the regulated voltage and generates an output signal that is used to adjust the gate voltage of the driver switch by going up and down to correct for any oscillation at the output or sudden change in the load demand. The A_{EA2} along with capacitor C_x forms an integrator/low pass filter to lower the oscillation at the gate of the pass transistor. The reference voltage sets the operation point of the voltage regulator.

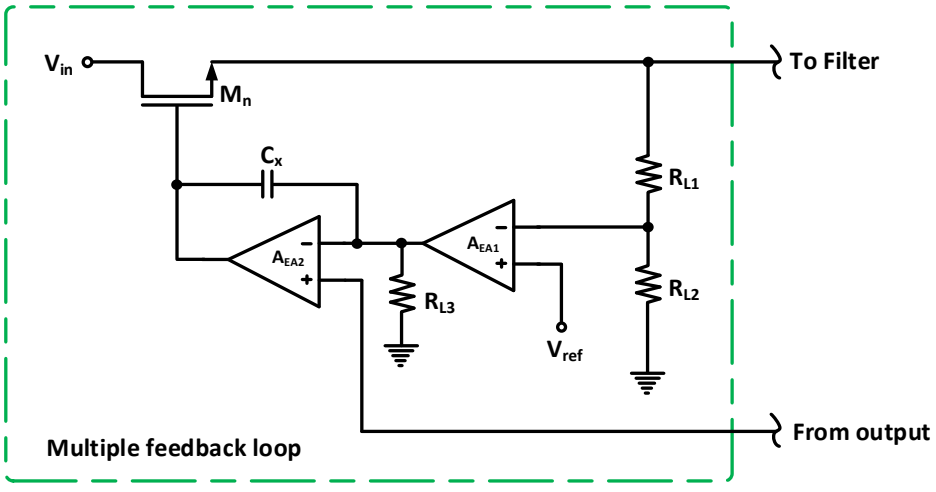

Figure 4.7: Error amplifiers of the proposed HLDR

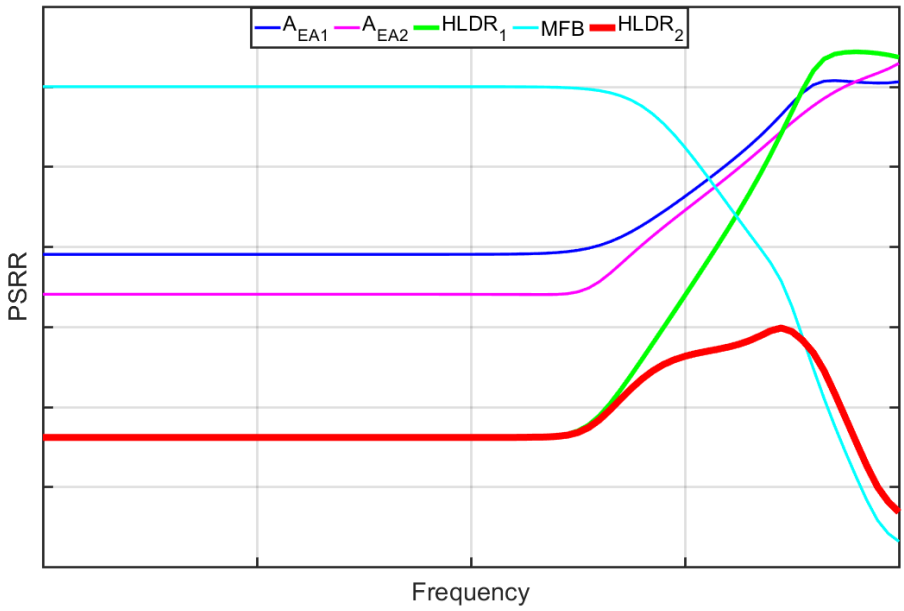

Figure 4.8: PSRR of HLDR for each path and the total combined PSRR of the regulator

4.7 PSRR Analysis of HLDR

The finite PSR of the conventional LDO is due to several paths between the input and output of the LDO [10]. Figure 4.8 shows the PSRR plot of each path of the proposed HLDR. The plot in blue corresponds to the PSRR of the first stage error amplifier (A_{EA1}). The second error amplifier (A_{EA2}) PSRR is represented in magenta. Combined, the two error amplifiers generate the PSRR in green at the first $HLDR_1$ output stage. The total PSRR at the second stage ($HLDR_2$) is shown in red. The second stage of HLDR combines the PSRR of the MFB filter in cyan with the first output stage (green). The transfer function due to multiple path loop gains are presented below. By breaking the first feedback loop and looking through the first stage of the HLDR, we can deduce the transfer functions of each path. In equation (4.9), the loop gain due to A_{EA1} amplifier is given. Equation (4.13) shows the transfer function with respect to the second A_{EA2} amplifier. The HLDR first stage

total loop gain ($HLDR_1$) is given by equation (4.14). The transfer equation for the MFB filter is given in equation (3.3) (Chapter 3) and together with the HLDR first stage loop gain, the total hybrid regulator transfer function can be formed. As shown by the equations (4.14), the PSR of the first HLDR output stage depends on the feedback gain of the first and second feedback loops (see green on Figure 4.8). The PSRR of the entire HLDR ($HLDR_2$) can be improved in conjunction with the MFB filter as depicted in red by Figure 4.8.

$$v_{fb1} = \frac{R_{L2}}{R_{L1} + R_{L2}} V_{out1} \tag{4.1}$$

$$v_{fb2} = \left(\frac{R_{F2}}{R_{F1} + R_{F2}} || \frac{1}{sC_b}\right) V_{out2} \tag{4.2}$$

$$v_{fb2} = \left(\frac{1}{\frac{R_{F2} sC_b}{R_{F1} + R_{F2}} + 1}\right) V_{out2} \tag{4.3}$$

$$R_{oHLDR1} = r_{ds-Pass} || R_{L1} + R_{L2} || R_{o1} \tag{4.4}$$

$$R_{oHLDR2} = r_{oMFB} || R_{F1} + R_{F2} || R_{o2} \tag{4.5}$$

$$Z_{cHLDR2} = \frac{1 + sC_o R_{ESR}}{sC_o} \tag{4.6}$$

$$Z_{oHLDR2} = R_{oHLDR2} || Z_{cHLDR2} \tag{4.7}$$

$$A_{v_{EA1}} = \frac{v_{fb1}}{V^-} = (0 - v_{fb1}) g_{EA1} (r_{oEA1} // R_{L3}) \tag{4.8}$$

$$A_{v_{EA1}} = g_{EA1} \left(\frac{r_{oEA1} R_{L3}}{r_{oEA1} + R_{L3}} \right) \frac{R_{L2}}{R_{L1} + R_{L2}} V_{out1} \tag{4.9}$$

$$A_{v_{EA2}} = (v_{fb2} - v_{EA1}) g_{EA2} \left(r_{oEA2} || \frac{1}{sC_x} \right) \tag{4.10}$$

$$A_{v_{EA2}} = (v_{fb2} - v_{EA1}) g_{EA2} \left(\frac{1}{1 + sC_x r_{oEA2}} \right) \tag{4.11}$$

$$A_{v_{EA2}} = (v_{fb2} - g_{EA1} \left(\frac{r_{oEA1} R_{L3}}{r_{oEA1} + R_{L3}} \right) \frac{R_{L2}}{R_{L1} + R_{L2}} V_{out1}) g_{EA2} \left(\frac{1}{1 + sC_x r_{oEA2}} \right) \tag{4.12}$$

$$A_{v_{EA2}} = \left(\left(\frac{1}{\frac{R_{F2} sC_b}{R_{F1} + R_{F2}} + 1} \right) g_{MFB} Z_{oHLDR2} - g_{EA1} \left(\frac{r_{oEA1} R_{L3}}{r_{oEA1} + R_{L3}} \right) \frac{R_{L2}}{R_{L1} + R_{L2}} V_{out1} \right) g_{EA2} \left(\frac{1}{1 + sC_x r_{oEA2}} \right) \tag{4.13}$$

$$A_{v_{HLDR1}} = \left(\left(\frac{1}{\frac{R_{F2} s C_b}{R_{F1} + R_{F2}} + 1} \right) g_{MFB} Z_{oHLDR2} - g_{EA1} \left(\frac{r_{roEA1} R_{L3}}{r_{oEA1} + R_{L3}} \right) \frac{R_{L2}}{R_{L1} + R_{L2}} g_{M-pass} R_{oHLDR1} \right) g_{EA2} \left(\frac{1}{1 + s C_x r_{oEA2}} \right) \tag{4.14}$$

4.8 Regulator Performance

Testing the stability of voltage regulation at low I_o, a maximum R_L with minimum C_L is considered. This allows the regulator to always supply a minimum output current of V_{OUT}/R_{Lmax}. At the lowest voltage setting, a 0.5 V output voltage is regulated with a 120 mA output current. At 5 KΩ the voltage regulator supplies a minimum current of 100 µA and maintains stability. The output stage OTA is designed for a large resistive load in mind to make sure the gain of the amplifier is not significantly lowered and also, most importantly, remains stable. For maximum C_L and minimum R_L, the highest amount of I_o is generated. Loads with a higher C_L beyond the specified value will cause the phase margin of the OTA to deteriorate and move closer to an unstable state.

Efficiency is one of the most important parameters in power conversion. The application note provided by [48] explains how to perform efficiency calculations for linear regulators. The efficiency equation given in [48] is slightly modified to account for the second driver. As shown by the equation (4.15), efficiency is a function of input voltage,

quiescent current, output voltage and output current. By minimizing the quiescent current and by lowering the input to output range, a higher efficiency can be obtained. Since different drivers perform the voltage and current sourcing, the current supplied by the voltage driver M_n, which is limited by V_{OUT1}/R_1, is added to the efficiency calculation. In addition, as the efficiency of the linear regulator is limited by V_{OUT}/V_{IN}, the proposed HLDR is also governed by the same parameter. The feedback resistors R_{L1} and R_{L2} are sized up to allow most of the current to flow through the MFB filter. At full load, the efficiency is lower when compared with a light load.

$$\eta = \frac{V_o\, x(\, I_{o1} + \, I_o)}{(\, I_{o1} + \, I_o + I_q)V_i} x\ 100 \tag{4.15}$$

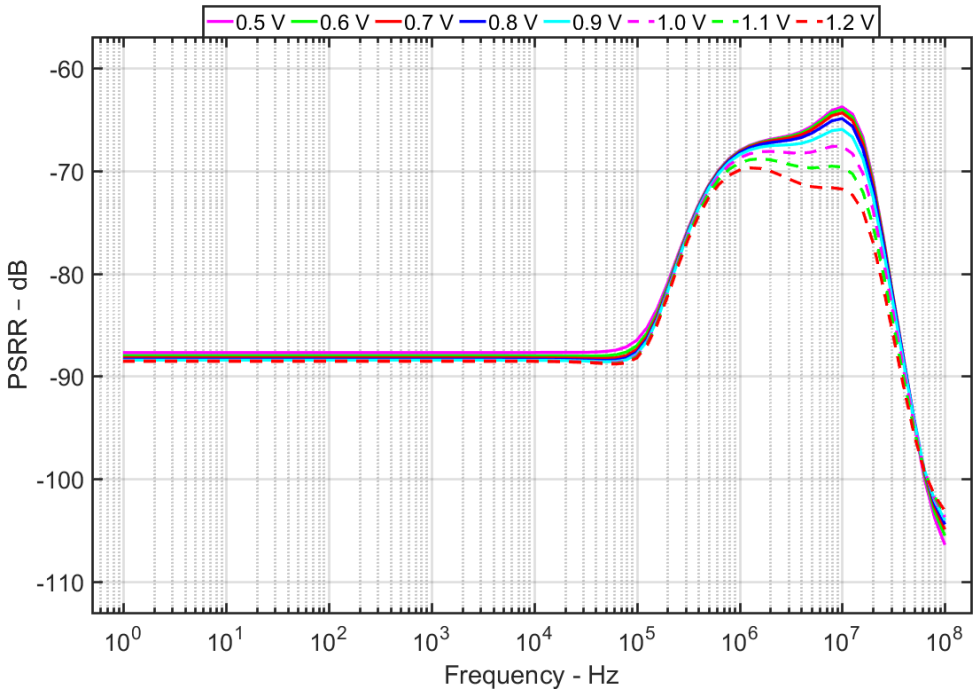

Figure 4.9: Proposed HLDR AC analysis at various voltage levels

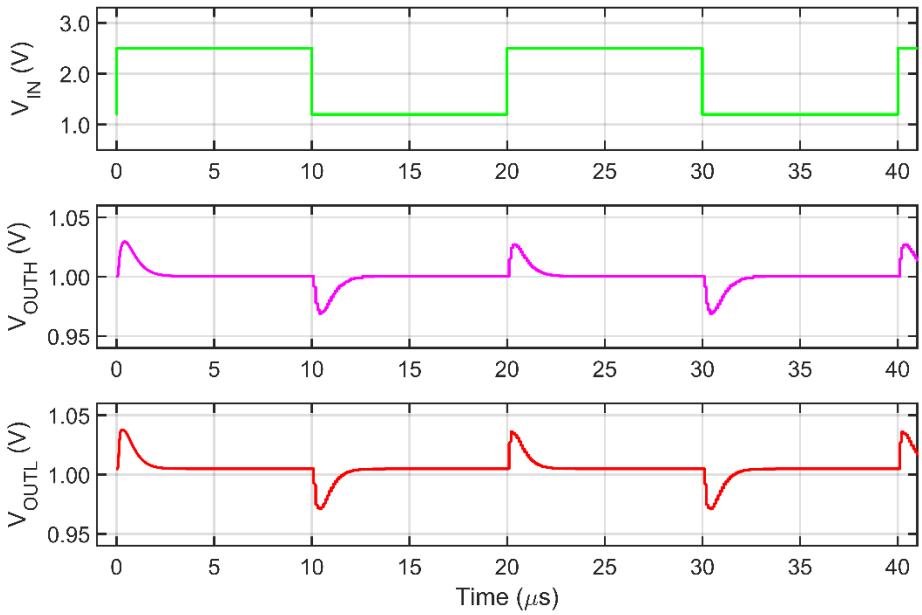

Figure 4.10: HLDR line transient response for I_{out} = 100 mA and I_{out} = 200 µA

Figure 4.9 shows the AC analysis for various voltage levels. The PSRR is a key parameter for voltage regulators to determine the amount of input ripple generated by the energy source that is mitigated at the output of the regulator. The HLDR is tested for a noisy oscillating DC voltage source with 5 MHz frequency to simulate for switching regulator or power supply with 5 MHz ripple noise. At this frequency, PSRR is especially important to decide if the output ripple is small enough to have a direct connection to the load or if an additional linear regulator is needed for farther ripple suppression. In the proposed design, near -88 dB PSRR is achieved in the frequency band until 100 kHz. Also, up until a 10 MHz frequency range, the voltage regulator can obtain above -62 dB PSRR. The error amplifiers set the PSRR up to near 1 MHz then the MFB takes over and extends the PSRR past 10 MHz. Since the proposed regulator is going to be used in both standalone and in conjunction with a linear voltage regulator, higher ripple suppression is desired,

especially at the operating frequency. Along with the dual feedback loops and the active MFB filters, conventional LDO can be implemented to achieve a higher PSRR.

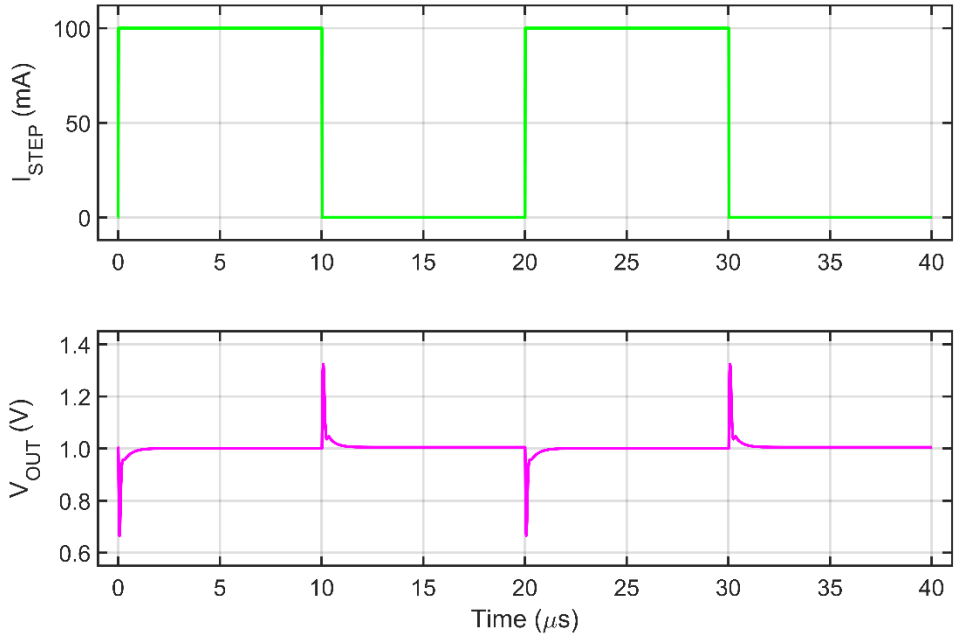

Figure 4.11: Load transient response of the proposed HLDR

An important parameter that is critical for stability of the voltage regulator is the line regulation. Line regulation is a measure of the circuit's ability to maintain the specific output voltage with varying input voltage [48]. The line regulation is expressed in percent change in the output voltage with respect to the change in the input voltage. Equation (3.16) shows the mathematical representation of the line regulation. In the proposed design, the voltage regulator can be varied between a maximum output voltage of 1.2 V and a minimum output voltage of 0.5 V. At a minimum voltage drop of a near 200 mV, and for the line regulation of 1.2 V output, the input voltage is varied between 1.4 to 2.5 V. Also, for the line regulation of 0.5 V output, the input is varied between 0.7 to 2.5 V. At heavy load, the line regulations is <1 % for both 1.2 V and 0.5 V output voltages. For the line

transient response, the HLDR is tested via a voltage step input with 10 ns rise and fall time. Figure 4.10 shows the input and output voltage transient response of the HLDR for 1.0 V regulated output voltage at a heavy (V_{OUTH}) and light (V_{OUTL}) load current. In both heavy and light loads, the output voltage variation for step input between 1.2 V and 2.5 V is near 50 µV, which is well within the PSRR of -88 dB. Also, an overshoot and undershoot around ±29 mV is shown on the figure during the step input voltage transition.

Another critical parameter for stability of the voltage regulator is the load regulation. Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions [48]. The load regulation is expressed in the percent change in the output voltage with respect to the change in the output current. Equation (3.17) shows the mathematical representation of the load regulation. The worst case of the output voltage variations occurs as the load current transitions from zero to its maximum rated value or vice versa [48]. At a 1.2 V output voltage with a maximum load variation, the output voltage varied by 6.8 mV. Also, at 0.5 V output, a 2 mV variation is witnessed as the load transitions from minimum to maximum. The load regulations are 5.7 % and 4 % for 1.2 V and 0.5 V output voltages. For the load transient response, the HLDR is tested via a current step input with 10 ns rise and fall time. Figure 4.11 shows the step input and output voltage transient response of the HLDR for 1.0 V regulated output voltage. The output voltage variation for a step current input between 0 and 100 mA is less than 4.5 mV. Also, an overshoot and undershoot around ±0.33 V is shown on the figure during the step current transition. Figure 4.12 shows the HLDR circuit performance with respect to the change in the output load. Performance degradation is shown at a high output load

current for each corresponding output voltage. The boundary line divides the performance of the HLDR between the areas of stable operation with low DC shift and better PSRR against higher DC shift with poor PSRR. To obtain higher efficiency and lower DC shift as well as a better PSRR, the HLDR should be operated within the prescribed boundaries.

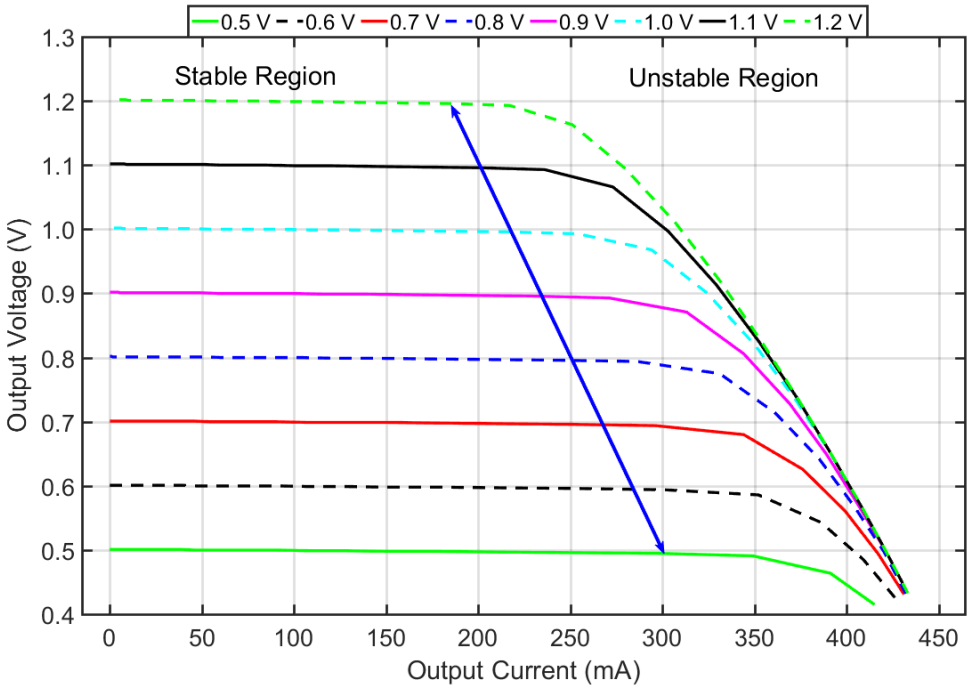

Figure 4.12: HLDR output voltage with respect to output current

4.9 Simulation Results and Discussions

The second-order low pass MFB frequency response of the circuit is presented in Figure 4.13. In the design, Butterworth optimization is chosen since precise regulation is required across the passband. As depicted by the Figure, Butterworth architecture provides maximum passband flatness. The frequency response at the end of the first filter is depicted in green (V_{OUT1}), the second filter is in blue (V_{OUT2}) and the combined filter response is shown in red (V_{TOT}). The simulation result is performed at full load. The general curve

structure of the circuit frequency response follows closely with the ideal curve (magenta). The deviation from the actual curve resulted from the parasitic issues of the filter. The parasitic capacitors, filter resistors, and output stage filter OTA performance degradation at full load adds up at the output node causing a skew in the plot. In terms of the dynamic response of the system, the simulation result shows that the low frequency part of the input signal passed to the output and frequencies higher than the cutoff frequency (fc) attenuated.

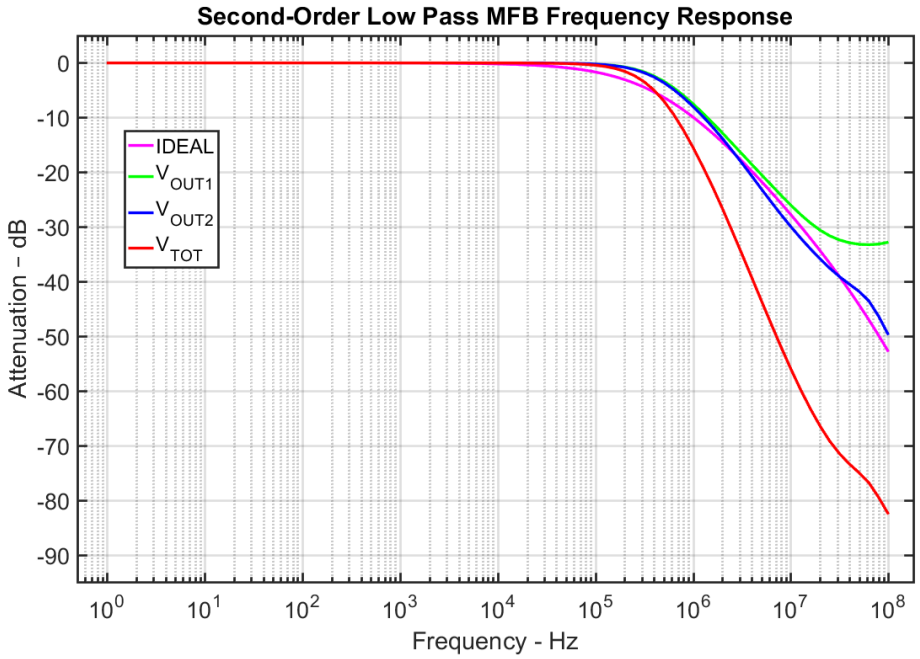

Figure 4.13: Second-order low pass MFB frequency response

Figure 4.14 shows the combined transient system performance of the voltage regulator for 0.5 V output voltage at full load with 100 mV added oscillating noise to the DC source. In magenta, the output of the HLDR first stage output (V_{OUT1}) is shown. Represented in black (V_{FB1}) is the input to the first error amplifier (A_{EA1}) set by the feedback resistors. The A_{EA1} then compares the voltage with the reference value and sends the signal in red (A_{EA1}) to the second error amplifier (A_{EA2}). The V_{OUT1} is filtered and

integrated twice by the MFB and becomes the V_{OUT2} as depicted in cyan. The outer loop feedback sets the second voltage (green) via the feedback resistors (V_{FB2}) and the value is compared with the output of the A_{EA1} by the second error amplifier (A_{EA2}). The output of the A_{EA2} then drives the pass transistor (blue) and the process repeats to make any adjustments. The inner and outer feedback loops try to match V_{OUT1} and V_{OUT2} and make corrections for any sudden load changes. As shown by the figure, the regulator takes a few cycles to adjust before settling at the prescribed voltage settings. The active filter is able to minimize the unwanted ripple voltage well within a tolerable margin less than 0.1 mV with a DC shift less than 3 mV.

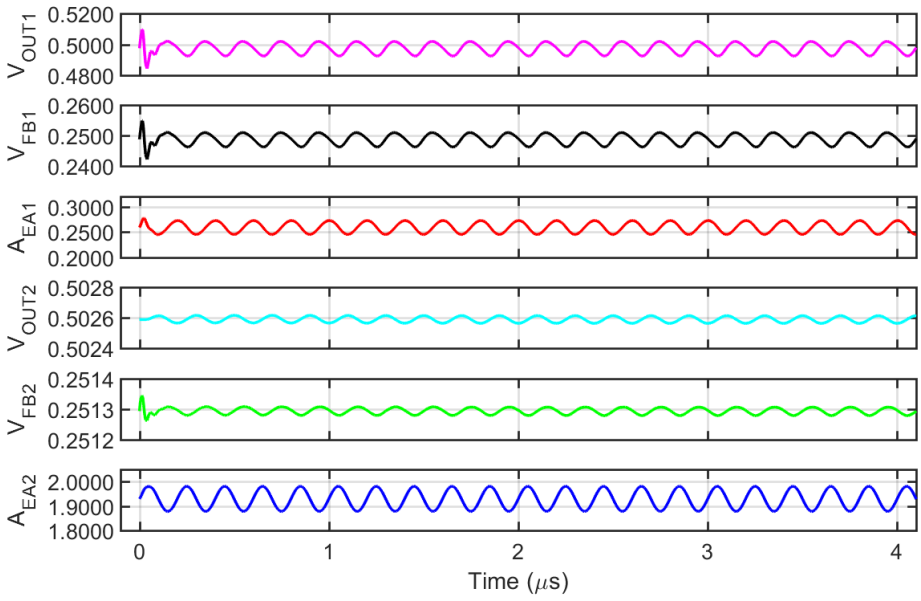

Figure 4.14: HLDR transient system performance simulation for 0.5 V

The voltage regulator output current and voltage are presented in Figure 4.15 and Figure 4.16. The simulation is performed at a full load with a noisy oscillating DC input and the figure (see Figure 4.16) is zoomed in to show the small output ripples. Output

voltage ripple less than 1 mV is seen at the end of the second filter. The voltage regulator is shown to be fully settled at around 400 ns. The proposed circuit is tested for various loads and the transient response of the output voltage and current corresponding to the input is obtained. When the system tested for loads from low to high at 1.3 V voltage drop, the worst-case output voltage DC shift of 4 mV and less than 1 mV voltage fluctuation occurred from 1.2 V. A slight over-or-under shoot and almost no ringing are visible in the output of the transient voltage and current analysis. The regulator is notably vigilant to the abrupt changes in the load and responds swiftly to the demand. A noisy oscillating signal was added to the DC voltage source, and both kHz and MHz range ripples were used in the simulation with almost no change in the result. The ripple signal frequency can be increased up until 10 MHz with relatively low performance or efficiency degradation.

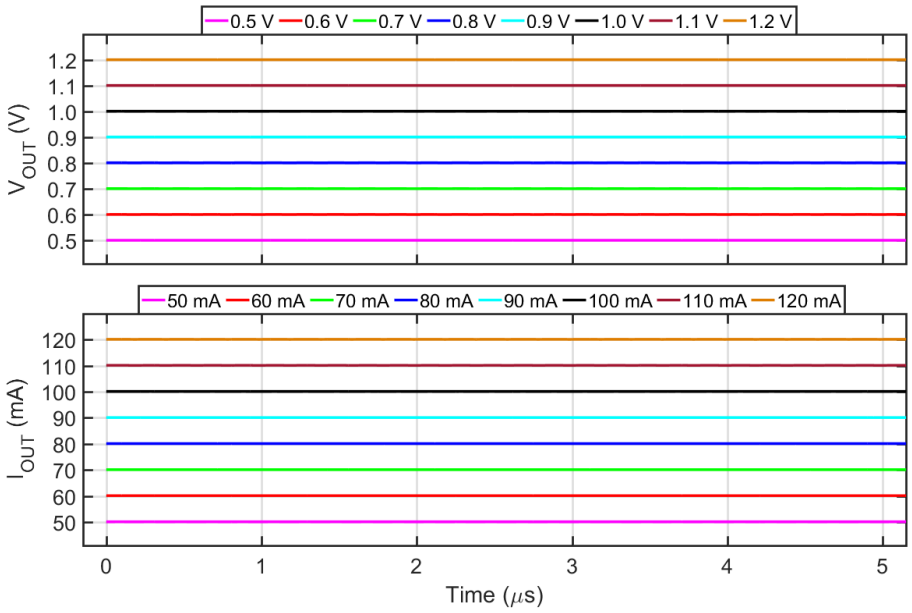

Figure 4.15: HLDR transient response showing output voltage and output current. From bottom up, each color-coded lines show the output voltages and currents from 0.5 V to 1.2 V and from 50 mA to 120 mA

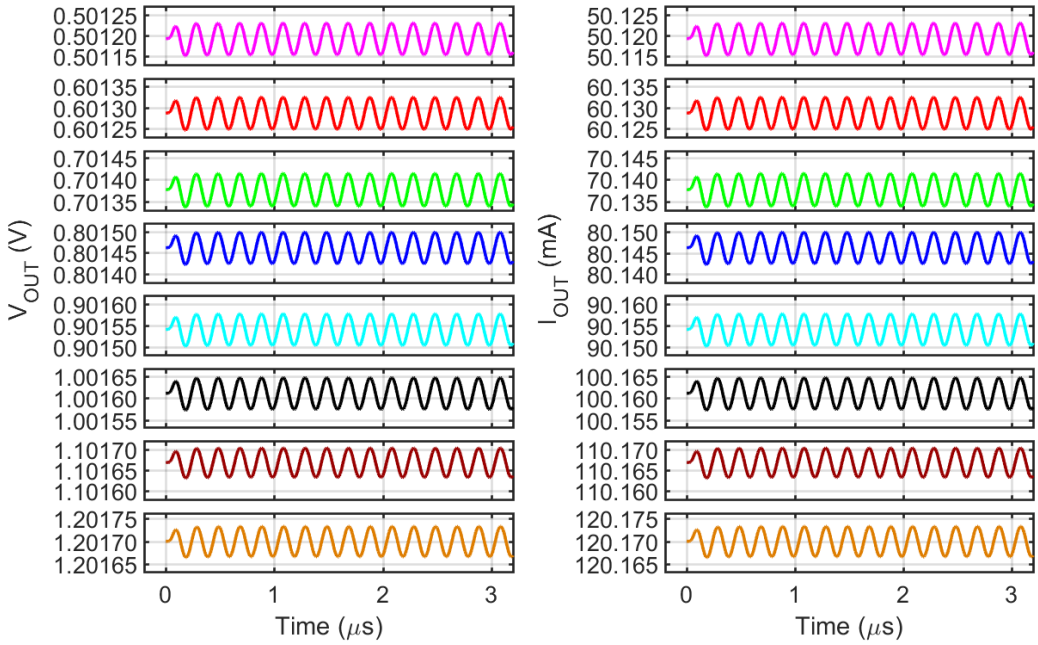

Figure 4.16: Close-up HLDR transient response showing output voltage and output current. From top down, each color-coded lines show the output voltages and currents from 0.5 V to 1.2 V and from 50 mA to 120 mA

A performance comparison table presented in [10] is slightly modified and shown in Table 4.1: LDO performance comparison among various designs comparing the proposed design with other existing converters. The proposed on-chip hybrid low dropout regulator utilizes a 0.45 mm X 0.5 mm on-chip area. The driver large transistors take a considerable portion of the chip area. The size of the driver transistors in the output stages can be adjusted according to the design requirements depending on the current demand, which will increase or decrease the chip size. The regulator is capable of supplying adjustable output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current from 2.5 V input voltage. Depending on the required operating voltage, the output voltage can be adjusted via reference voltage. The HLDR employs two separate drivers for current and voltage sourcing along with MFB filter for ripple suppression and stability. The HLDR

regulator can achieve 98 % current efficiency. The HLDR also has a 200 mV voltage drop with a 4 mV full load worst DC shift. The voltage regulator can supply 144 mW of maximum power at comparably the same efficiency with conventional LDOs.

4.10 Summary

In this chapter, we have introduced a fully on-chip hybrid LDO voltage regulator with a dual feedback path and active filter to achieve a high PSR over a wider frequency range. The proposed hybrid architecture utilizes a cascaded second order multiple feedback low pass filter (MFB LPF), inner and outer error correction loops, and driver switches. This approach allows the hybrid LDO to employ two separate drivers for current and voltage sourcing. Extensive post fabrication analysis and experimental measurements were performed to validate the presented hybrid voltage regulator. The proposed design takes the input voltage range between 1.4 V to 2.5 V. It can generate an adjustable output voltage between 0.5 V to 1.2 V and a 100 µA to 120 mA output current. In addition, the architecture is a fully integrated on-chip design and does not need an external capacitor placed on the PCB or host IC's package for stability. The design takes a 0.45 mm X 0.5 mm area, has a PSRR of -86 dB at 100 kHz and -62 dB at 10 MHz, has an output voltage ripple less than 1 mV, and 200 mV dropout voltage. The innovative hybrid LDO design can deliver power both as a stand-alone regulator or in synergy with a switching regulator. In addition, it offers an effective technique for SOC integration of a voltage regulator.

Table 4.1: LDO performance comparison among various designs

	[52]	[53]	[54]	[10]	**This work**
Approach	Two pass transistor	Two pass transistor	Extended loop bandwidth	Feed-Forward Ripple Cancellation	**Two pass transistor with MFB**
Technology [µm]	0.13	0.6	0.35	0.13	**0.6**
Drop-out Voltage (V)	0.2	0.6	0.15	0.15	**0.2**
On-chip area [mm^2]	0.166	N/A	0.053	0.049	**0.225**
V_{in} (V)	3	>1.8	>1.05	>1.15	**0.7 – 2.5**
V_{out} (V)	2.8	1.2	0.9	1.0	**0.5 - 1.2**
I_Q (µA)	100	70	160	50	**320**
I_{max} (mA)	150	5	50	25	**300/195**
PSRR (dB)	-57 @ 100 kHz -40 @ 1 MHz	-70 @ 100 kHz -40 @ 1 MHz	-50 @ 100 kHz -50 @ 1 MHz	-60 @ 100 kHz -67 @ 1 MHz -56 @ 10 MHz	**-86 @ 100 kHz -70 @ 1 MHz -62 @ 10 MHz**

CHAPTER 5

SINGLE AND DUAL OUTPUT TWO-STAGE ON-CHIP POWER MANAGEMENT SYSTEM

An efficient power management system (PMS) in high-density integrated circuits requires full on-chip integration of a voltage regulator. As integrated circuits (ICs) are moving towards system-on-a-chip (SOC) designs, integration of an entire power management system within a single chipset requires new approaches. For ripple control, switching regulators are typically implemented along with linear regulators. The conventional off-chip switching voltage regulator contains a passive floating inductor, which is difficult to be implemented inside the chip. The proposed fully on-chip architecture in this paper, incorporates both an inductorless switching regulator and a linear regulator in a single design to achieve better ripple suppression. The operating frequency of switching regulators are growing with faster response times to meet the requirement of new generation multi-voltage high speed ICs. However, linear regulators are not meeting the demand to mitigate the high-speed power supply ripples. In this chapter, multiple on-chip hybrid switching regulators, along with hybrid linear regulators with a higher power supply rejection (PSR) over a wider frequency range are proposed. Both switching and linear regulator designs are implemented with cascaded second order multiple feedback low pass filters (MFB LPF). The PMS scheme has three different combinations: a switching stage with a single switching and a single linear output stage (0.48 mm^2), a switching stage with a single linear output stage (0.44 mm^2), and a switching stage with a dual linear stage (0.70 mm^2). The design and layout of the circuits are demonstrated on

Cadence Virtuoso tools. Post fabrication experimental measurements and the results are presented in later sections.

5.1 Introduction

Placement of entire power management systems (PMS) within a single chipset requires changes in current design methods. Power delivery for cellular phones, MP3 players, personal digital assistances (PDA), cameras, and so on require stable and noiseless multi-voltage supply and large load current [26]. These devices are typically powered with buck or switching voltage regulators along with LDOs for generating multiple supply voltages and ripple rejection [55]. A conventional buck regulator requires an inductor, which takes a very large chip area and exhibits parasitic effects. In addition, the buck converter needs a large output capacitor. However, integration of the buck regulator onto the chip presents many challenges. Reducing the on-chip filter capacitor limits the total amount of instantaneous charge available to the load, which then introduces a higher susceptibility of a large dI/dt event that can cause large voltage fluctuations [19]. Additionally, on-chip inductor sizes must be drastically reduced, resulting in higher switching frequency but lower conversion efficiencies with low inductance, which limits the amount of power it can deliver. Typically, both the inductor as well as capacitor of buck converters are fabricated as part of the package or they are placed in the PCB board outside the chip. Conventional LDOs typically require a large output capacitor placed on the PCB or host IC's package for stability and have a poor PSR at high frequencies (above 300 kHz) [10]. The bulky off-chip or on package capacitor takes up a valuable area. Many capacitorless [23] [24] LDOs were proposed in the past including those with a capacitance

multiplier [25] to mitigate the use of large capacitors. In addition, capacitorless designs or small on-chip capacitor based LDOs provide a better slew rate and enable greater power system integration in SOC.

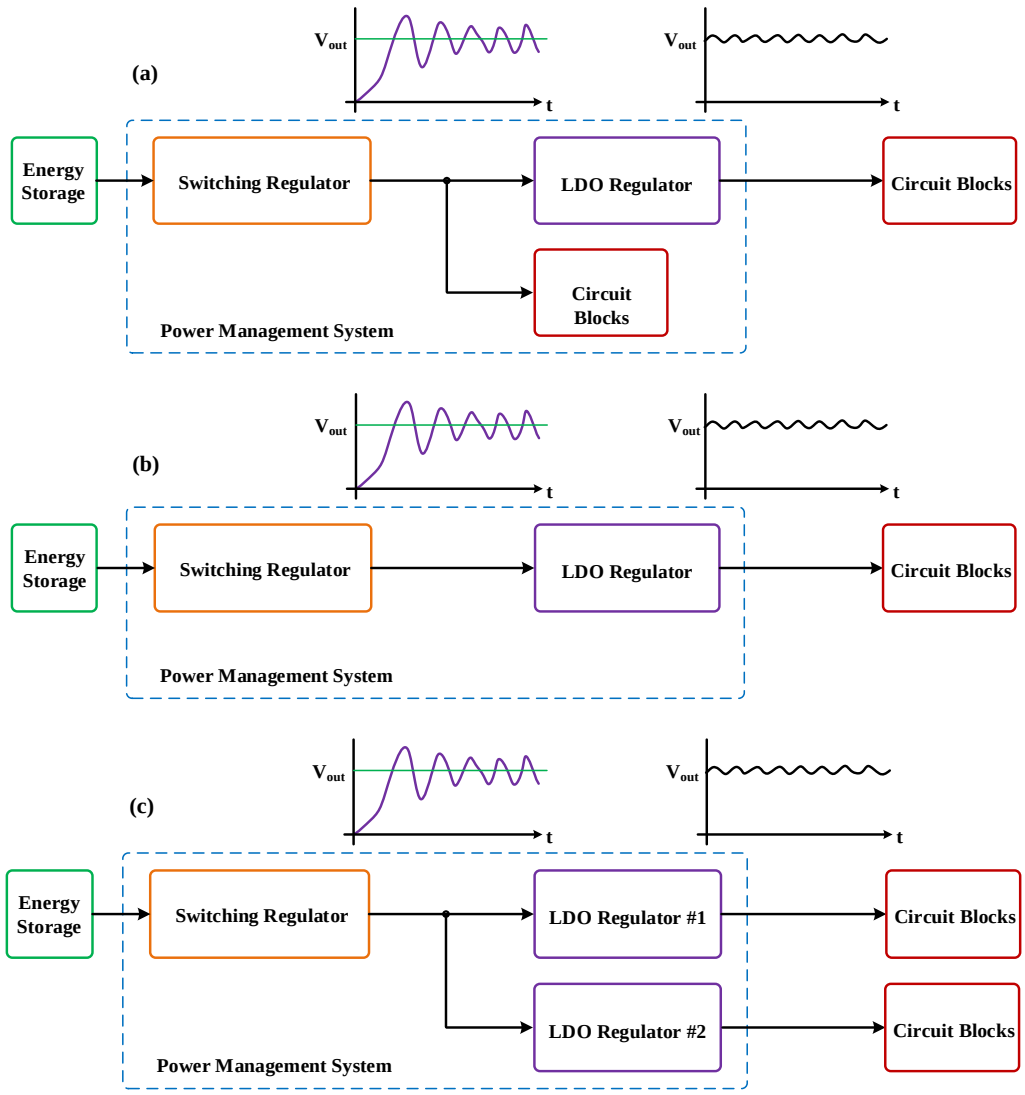

Figure 5.1: (a) Block diagram of switching input stage with single switching and single linear output stage, (b) Block diagram of switching input stage with single linear output stage, (c) Block diagram of switching input stage with dual linear output stage

Power management integrated circuits (PMIC) are the SOC power portion of the design. They encompass, switching regulators, voltage reference circuits, LDOs (low dropout regulators), battery charging circuits, etc. Switching regulators and LDOs are found in nearly all electronic systems, both as a stand-alone regulator or cascaded with each other. They are essential for delivering power from an energy source to discrete circuit blocks or integrated circuits at their respective and desired voltage levels. Currently, there is a great push to incorporate the entire power management system on a single chip. On-chip regulators are critically important for SOC and multi-/many-core ICs, because based on activity levels of different blocks or cores in high-density and high-performance ICs, they can enable the voltage to be adjusted in nano or pico second time. Switching regulators with LC filters are very efficient in delivering power but introduce unwanted high frequency ripple voltage and are off-chip due to the filter elements. We introduce a new fully on-chip and inductorless switching regulator design in Chapter 3. LDO regulators are utilized to act as a post-regulating stage to reject the ripple noise generated by the buck converter [22], [28]. LDOs with large decoupling capacitors in a microfarad range are commonly used for rejecting switching noise [23], [27]. Large capacitors take up a large area, but by suppressing the output ripple voltage, the overall power-supply rejection of the power delivery system is improved. As the demand for more SOC integration increases with higher operating frequency above 1 MHz of switching regulator, the PSR of the LDOs is expected to go up accordingly. However, conventional regulators have poor PSR at high frequencies. In Chapter 4, we introduce a hybrid LDO design to improve the PSR over a wider frequency range.

Current and future ICs with multi-voltage SOCs demand a robust design with minimum ripple noise that can be scalable, on-demand adjustable and fully on-chip regulators. As a potential solution, this chapter presents a fully on-chip PMS scheme with three different combinations: a switching stage with a single switching and single linear output stage (see Figure 5.1 (a)), a switching stage with a single linear output stage (see Figure 5.1 (b)), and a switching stage with a dual linear stage (see Figure 5.1 (c)). Both switching and linear regulator designs are implemented with a cascaded second order multiple feedback low pass filter (MFB LPF). Active filters require one or more operational amplifiers, but passive filters do not. In addition to being SOC friendly, one of the main advantages of having active filters is to boost the signal via gain. Active filter based on-chip voltage regulators can deliver power at a very high frequency. On-chip filters also require smaller filter elements and provide a faster response to changes to the load. One of the few disadvantages of having on-chip regulation is the total amount of instantaneous charge availability due to the smaller filter capacitors. Embedded within the filter is an Integrator comprised of R_x and C_x, along with the Voltage FeedBack (VFB) op amp. This design normally needs to be implemented using a unity-gain stable VFB op amp, because the core gain element needs to be configured as an Integrator [46]. The embedded integrator enables the proposed PMS design to go from a noisy oscillating input to stable linear output. A more detailed analysis on MFB filter design and implementation is presented in Chapter 3.

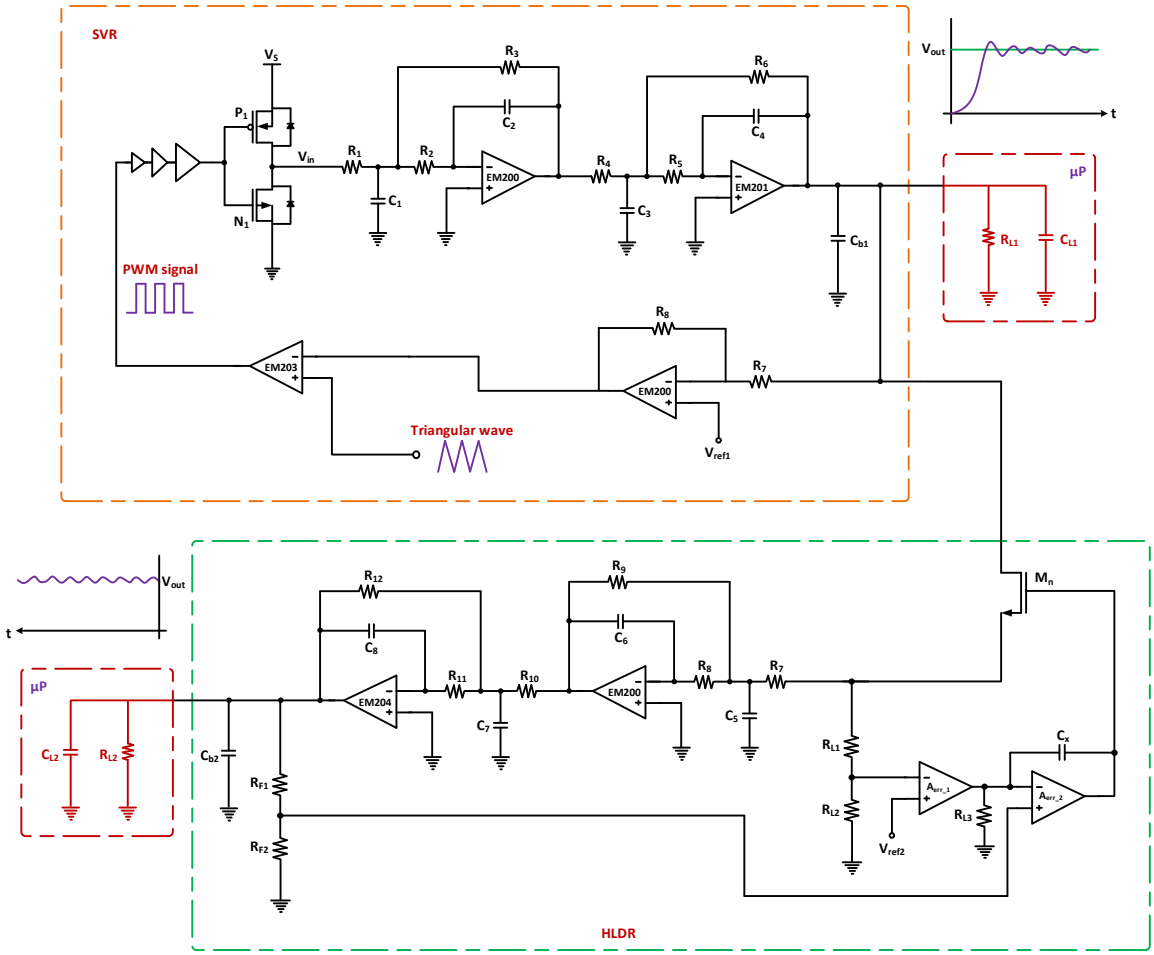

Figure 5.2: Proposed on-chip SIS-SOS-SLOS PMS deign

5.2 Switching Input Stage with Single Switching and Single Linear Output Stage

The first PMS design (see Figure 5.2) incorporates a switching input stage with a switching output stage and a single linear output stage (SIS-SOS-SLOS). The total PMS area is 0.5 mm X 0.5 mm. The switching voltage regulator (SVR) input stage utilizes two separate drivers for current and voltage sourcing. As shown in Figure 5.2, the SVR is comprised of tapered gate drivers, driver switches, cascaded 2nd order MFB LPF, an error amplifier and a comparator. The SVR part of the design can generate adjustable output

voltage between 0.5 V to 1.5 V and 100 µA to 150 mA output current from 1.0 V to 2.5 V input voltage. In addition, the architecture is inductorless and fully integrated on-chip design. It also has a settling time of 2.5 µs and an operating frequency of 5 MHz. Depending on the reference voltage setting, the driver switches open and close to generate a noisy voltage. The second stage of MFB LPF is also the current generation node. Depending on the load variation and output voltage ripple, the error amplifier amplifies the signal to be corrected. The comparator then takes the signal and moves it up and down to adjust the duty cycle. This last stage is where the pulse-with modulation signal (PWM) is generated and adjusted. The tapered gate drivers then respond to the PWM signal to switch the driver switches accordingly. Similar to a conventional buck converter, the output voltage of the proposed switching regulator input stage can be described mathematically as in (3.1) [16]. Duty cycle (D) is defined by the switch on time (t_{on}) divided by the total period (T_s).

To suppress the noise generated by the SVR and improve the PSSR of the system, the proposed PMS employs an on-chip hybrid low dropout regulator (HLDR) as the second stage. The proposed linear regulator design employs two separate drivers for current and voltage sourcing. In addition, inner and outer feedback loops are implemented to monitor and correct the first stage and the output voltage for any changes. As depicted by Figure 5.2, the proposed design is comprised of a pass transistor, two error amplifiers, and a cascaded 2^{nd} order MFB LPF. The proposed design takes an input voltage range between 0.7 V to 2.5 V. It can generate an adjustable output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current. Also, the architecture is fully integrated on-chip design and

does not need an external capacitor for stability. In addition, it has a power-supply rejection ratio (PSRR) of -86 dB at 100 kHz and -62 dB at 10 MHz, has an output voltage ripple less than ±1 mV, and 200 mV dropout voltage. Depending on the reference voltage setting, the input is adjusted by the first error amplifier and pass transistor to generate the input to MFB LPF. The voltage is then filtered through the MFB LPF and a smoother output voltage signal is generated at the output. The second stage of MFB LPF is also the current generation node. Depending on the load variation and output voltage ripple, the second error amplifier adjusts the input to the pass transistor. The input to the MFP LPF and the output node are both monitored by the feedback system to match any changes between the two nodes.

5.2.1 Output Stage Circuit Analysis

For both SVR and HLDR designs, the op-amp at the last stage of the MFB filter is also the source of the output current. To generate the required output current, an operational transconductance amplifier (OTA) is used with a buffer output stage. OTA at a specified input behaves as a voltage controlled current source (VCCS). An OTA without a buffer can only drive capacitive loads. A resistive load (unless the resistor is very large) will kill the gain of the OTA [47]. In the output buffer stage, the PMOS transistor is the source of the regulator current, so it is made very large to supply the necessary output current. In addition, the NMOS transistor is also sized-up to be able to sink current. For the SVR, the PMOS is sized based on the voltage drop value from a 2.5 V supply and expected maximum output current. For the bottom limit, a maximum 2.0 V voltage drop for a minimum V_{OUT} (0.5 V) voltage at a maximum output current of $I_{o(max)}$ = 300 mA is used to size the current

source. In addition, for the upper limit, a 1.0 V voltage drop is considered for a maximum V_{OUT} (1.5 V) voltage with a maximum output current $I_{o(max)}$ = 150 mA is also considered. For the HLDR, the PMOS is sized based on the voltage drop value from a 2.5 V supply and expected maximum output current. For the bottom limit, a maximum 2.0 V voltage drop for a minimum V_{OUT} (0.5 V) voltage at a maximum output current of $I_{o(max)}$ = 300 mA is used to size the current source. In addition, for the upper limit, a 1.3 V voltage drop is considered for a maximum V_{OUT} (1.2 V) voltage with a maximum output current $I_{o(max)}$ = 195 mA is also considered. In both SVR and HLDR, depending on the output load requirement, the output current source is adjusted via V_{sg} change at the PMOS. The width and length of the current source is designed based on equations (3.10) and (3.11).

5.2.2 Pass Transistor Analysis

The HLDR utilizes two error amplifier stages for voltage ripple suppression and correction along with a cascaded MFB filter, and a driver switch for voltage level control. The pass transistor of HLDR generates a noisy oscillating voltage depending on the reference value at the end of its first stage output. The regulator is designed for a minimum of 200 mV and a maximum of 2 V dropout voltage. At the maximum output voltage, an output current $I_{o1} = V_{OUT1}/ (R1 // R_{LT})$ is supplied to the inner node. The driver switch W/L ratio is sized up to lower the R_{ds} of the transistor and supply I_{o1}. If the transistor resistors are not lowered, it reduces the supply current. This affects the output regulated voltage by shifting it higher, manifesting a voltage variation at the output. It is pertinent to have the R_{ds} lower than 10 Ω to have innocuous voltage perturbation. In addition, the feedback resistors, as well as filter resistors, are high to lower the amount of supplied current I_{o1} to

the inner node. This is important since a different driver in the OTA performs the current sourcing. The main purpose of the pass transistor is to set the voltage part of the regulation. The width and length of the pass device is also designed based on equations (3.10) and (3.11).

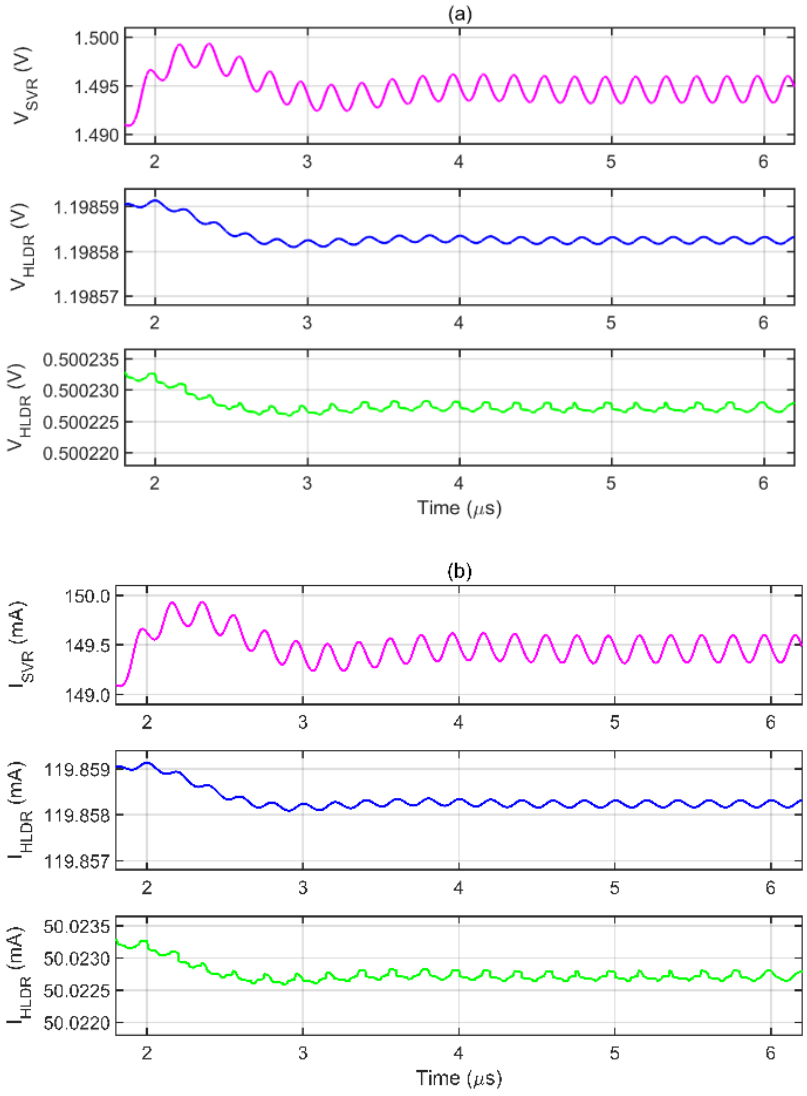

Figure 5.3: Transient response of SIS-SOS-SLOS: (a) output voltage, (b) output current

5.2.3 Simulation Results

The output current and voltage of the PMS with a SIS-SOS-SLOS is presented in Figure 5.3 (a) and Figure 5.3 (b). The simulation is performed with a noisy oscillating DC input. The output voltage ripple for the SVR is less than ±7 mV and for the HLDR is less than 1 mV. The PMS is shown to be fully settled at around 2.5 µs, which is primarily due to the SVR. The HLDR can achieve stability within 400 ns by itself. The proposed PMS is tested for various loads and the transient response of the output voltage and current corresponding to the input is obtained. For a heavy load, when the SVR is tested at 60 % duty cycle, the worst-case output voltage fluctuation of 8.7 mV with a 5.2 mV DC shift occurred from 1.5 V (magenta). However, the HLDR at heavy load shows a 1.5 mV DC shift from 1.2 V (blue) output voltage and less than a 1 mV DC shift from 0.5 V (green) output voltage while maintaining less than a 1 mV worst-case voltage fluctuation.

Figure 5.4 shows the AC analysis for various voltage levels of the first PMS design. The SIS-SOS-SLOS PMS is tested for a noisy oscillating DC voltage source with 5 MHz frequency to simulate a switching regulator or power supply with 5 MHz ripple noise. In the proposed PMS design, a -151 dB of PSRR at 5 MHz is obtained for the SVR and a -88 dB PSRR is achieved in the frequency band until 100 kHz by the HLDR. Also, up until a 10 MHz frequency range, the HLDR can obtain above -62 dB PSRR for both 1.2 V (magenta) and 0.5 V (green) output voltages. In the HLDR architecture, the first stage via error amplifiers sets the PSRR up to near 1 MHz then the MFB takes over and extends the PSRR passed 10 MHz. Since the proposed PMS is implemented as a standalone solution

by combining both the SVR and HLDR, higher ripple suppression is achieved even at high frequencies.

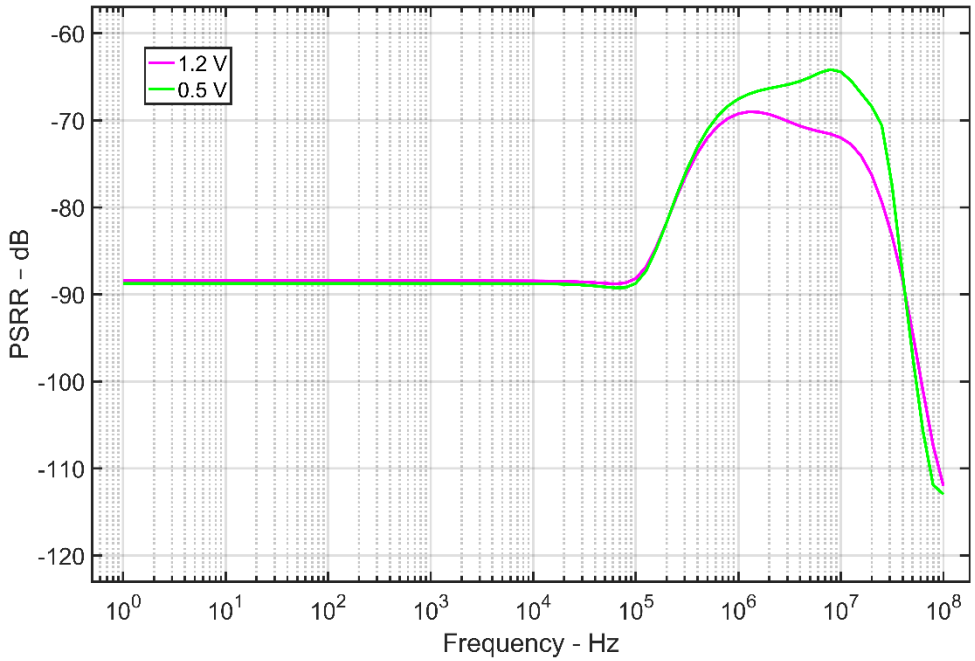

Figure 5.4: Proposed SIS-SOS-SLOS AC analysis at various voltage levels

Line regulation is a measure of the circuit's ability to maintain the specific output voltage with varying input voltage [48]. The line regulation is expressed in percent change in the output voltage with respect to the change in the input voltage. In the proposed SIS-SOS-SLOS PMS design, the SVR is varied between a maximum output voltage of 1.5 V and a minimum output voltage of 0.5 V. At a near 500 mV voltage difference between the input and output (see Figure 5.5), for the line regulation for 1.5 V (magenta) output, the input voltage is varied between 2.0 to 2.5 V via a voltage step input with a 10 ns rise and fall time (green). At heavy load, the line regulation for 1.5 V output voltage is 3.1 %. The feedback system of the SVR along with the reference voltage try to manage the changes in

the input by adjusting accordingly. The output of the SVR is fed to the HLDR to generate output voltage between 0.5 V to 1.2 V depending on the reference voltage. As shown by Figure 5.5, the HLDR at heavy load shows a 1.5 mV DC shift from 1.2 V (red) output voltage and a less than 1 mV DC shift from 0.5 V (blue). At heavy load, the line regulations are <1 % for both 1.2 V and 0.5 V output voltages. For the SIS-SOS-SLOS PMS, an overshoot and undershoot less than ±2 mV is shown in Figure 5.5 during the step input voltage transition.

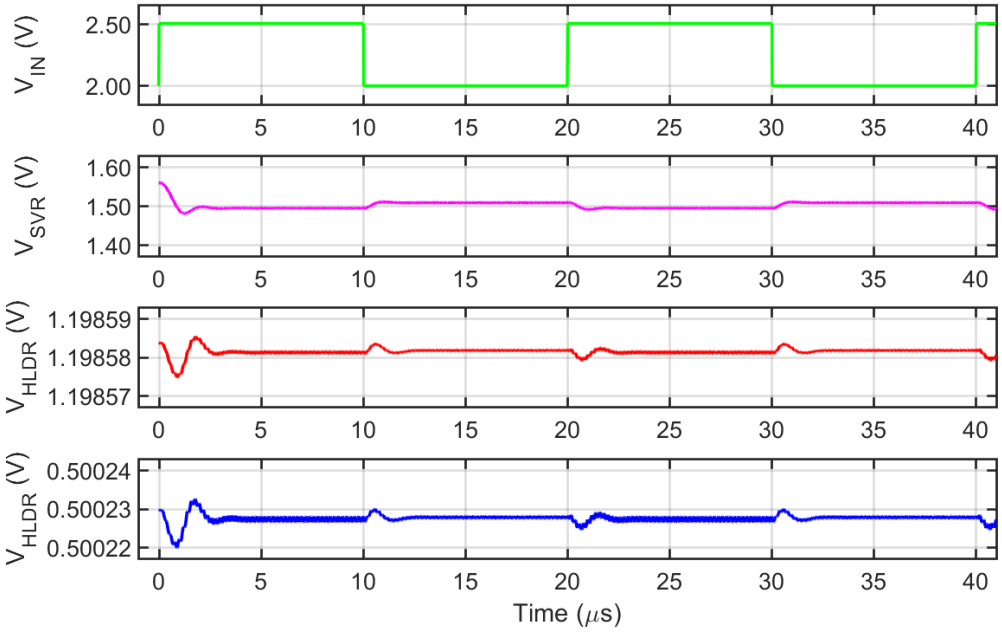

Figure 5.5: SIS-SOS-SLOS line transient response for I_{out} = 150 mA and I_{out} = 50 mA

Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions [48]. The load regulation is expressed in percent change in the output voltage with respect to the change in the output current. The worst case of the output voltage variations occurs as the load current transitions from zero to its

maximum rated value or vice versa [48]. In the proposed SIS-SOS-SLOS PMS design, the SVR at a 1.5 V (magenta) output voltage with a maximum load variation, the output voltage varied by 10.4 mV (see Figure 5.6). The SVR is tested via a current step input 150 mA with a 10 ns rise and fall time (green). The load regulation is 6.9 % for 1.5 V output voltage. For the HLDR, at 1.2 V (blue) output voltage with a maximum load variation, the output voltage varied by 3.2 mV. The HLDR is tested via a current step input 120 mA with a 10 ns rise and fall time (red). The load regulation is 2.7 % for 1.2 V output voltage. For the SIS-SOS-SLOS PMS, an overshoot and undershoot voltage around ±0.50 V is shown in Figure 5.6 during the step current transition.

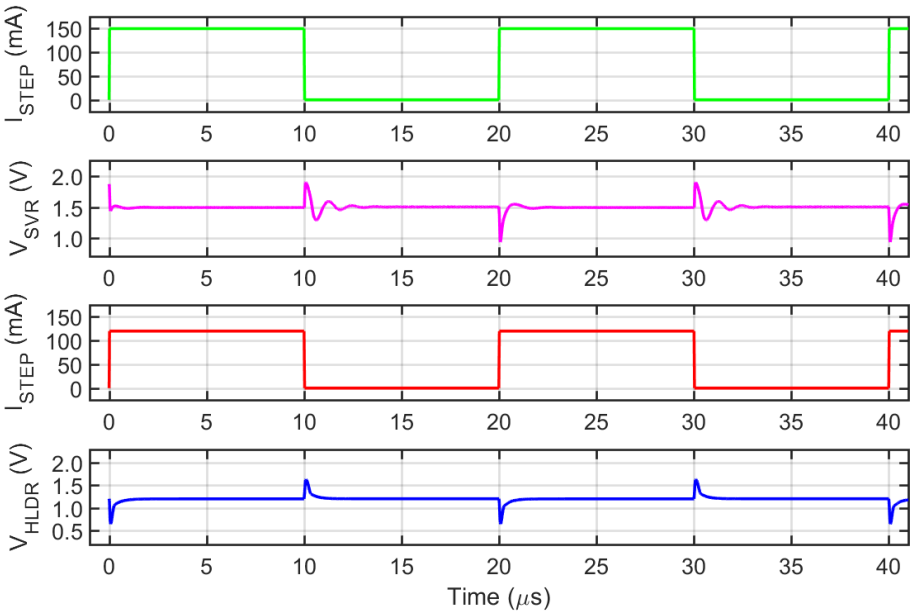

Figure 5.6: Load transient response of the proposed SIS-SOS-SLOS

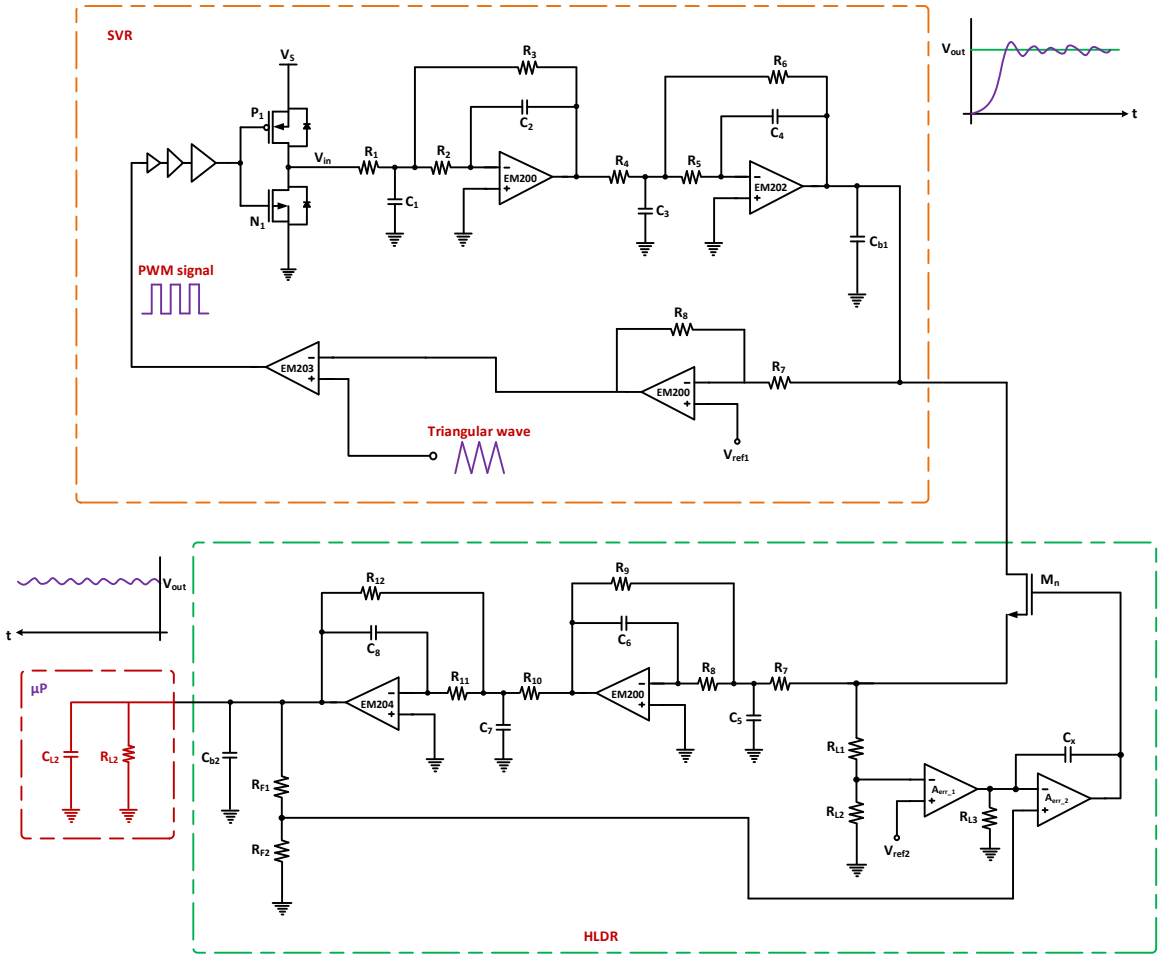

Figure 5.7: Proposed on-chip SIS-SLOS PMS deign

5.3 Switching Input Stage with Single Linear Output Stage

The second PMS design (see Figure 5.7) incorporates a switching input stage with a single linear output stage (SIS-SLOS). The total PMS area is 0.5 mm X 0.5 mm. The SVR part of the design can generate adjustable output voltage between 0.5 V to 1.6 V and 175 µA to 20 mA output current from 1.0 V to 2.5 V input voltage. In addition, the architecture is inductorless and fully integrated on-chip design. It also has a settling time of 1.5 µs and an operating frequency of 5 MHz. The PWM signal controls the operation of

the switching input part via equation (3.1). Depending on the reference voltage setting, the driver switches open and close to generate a noisy voltage. To suppress the noise generated by SVR and improve the PSSR of the system, the proposed PMS employs an on-chip HLDR as the second stage. The proposed HLDR takes an input voltage range between 0.7 V to 1.5 V. It can generate an adjustable output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current. Also, the architecture is fully integrated on-chip design and does not need an external capacitor for stability. In addition, it has a PSRR of -86 dB at 100 kHz and -62 dB at 10 MHz, has an output voltage ripple less than ±1 mV, and 200 mV dropout voltage.

5.3.1 Output Stage Circuit and Pass Transistor Analysis

For the second PMS design (SIS-SLOS), the op-amp at the last stage of the MFB filter is also the source of the output current. In this PMS architecture, the current source by the SVR is only used to drive the pass transistor of the HLDR. Beside the HLDR, no other output loads are fed by the SVR. The PMOS sizing for the SVR is based on the voltage drop value from a 2.5 V supply and expected maximum output current. The supply current is dictated by the load requirement in the pass transistor of the HLDR. A minimum 0.9 V voltage drop for a maximum V_{OUT} (1.6 V) voltage at a maximum output current of $I_{o(max)}$ = 20 mA is used to size the current source. Since the HLDR is driving the output load, the PMOS sizing is based on the voltage drop value from a 2.5 V supply and expected maximum output current. For the bottom limit, a maximum 2.0 V voltage drop for a minimum V_{OUT} (0.5 V) voltage at a maximum output current of $I_{o(max)}$ = 300 mA is used to size the current source. In addition, for the upper limit, a 1.3 V voltage drop is considered

for a maximum V_{OUT} (1.2 V) voltage with a maximum output current $I_{o(max)}$ = 195 mA is also considered. For both SVR and HLDR, using the specs provided above, the width and length of the current source is designed based on equations (3.10) and (3.11). The HLDR utilizes two error amplifier stages for voltage ripple suppression and correction along with a cascaded MFB filter, and a pass transistor switch for voltage level control. For the design of a pass transistor in HLDR, the same spec is used as in section 5.2.1 and 5.2.2, and the width and length of the pass device is also designed based on equations (3.10) and (3.11).

5.3.2 Simulation Results

The output current and voltage of the PMS with SIS-SLOS is presented in Figure 5.8 (a) and Figure 5.8 (b). The simulation is performed with a noisy oscillating DC input. The output voltage ripple for the SVR is less than ±12.5 mV and for the HLDR, it is less than 1 mV. The SVR operating at 5 MHz is shown to be fully settled at around 1.5 µs and 400 ns for the HLDR. The proposed PMS is tested for various loads and the transient response of the output voltage and current corresponding to the input is obtained. For a heavy load, when the SVR is tested at a 60 % duty cycle, the worst-case output voltage fluctuation of 12 mV with a 5 mV DC shift occurred from 1.5 V (magenta). However, the HLDR at heavy load shows a 1.5 mV DC shift from 1.2 V (blue) output voltage and less than a 1 mV DC shift from 0.5 V (green) output voltage while maintaining less than a 1 mV worst-case voltage fluctuation. In the SIS-SLOS PMS design, the SVR can supply up to 1.6 V and remain stable, since the load requirement is only coming from the pass transistor of the HLDR and it is well within the upper current limit of the design. The top

of Figure 5.8 (b) depicts the output current of the SVR, which is the input of the pass transistor of the HLDR (magenta).

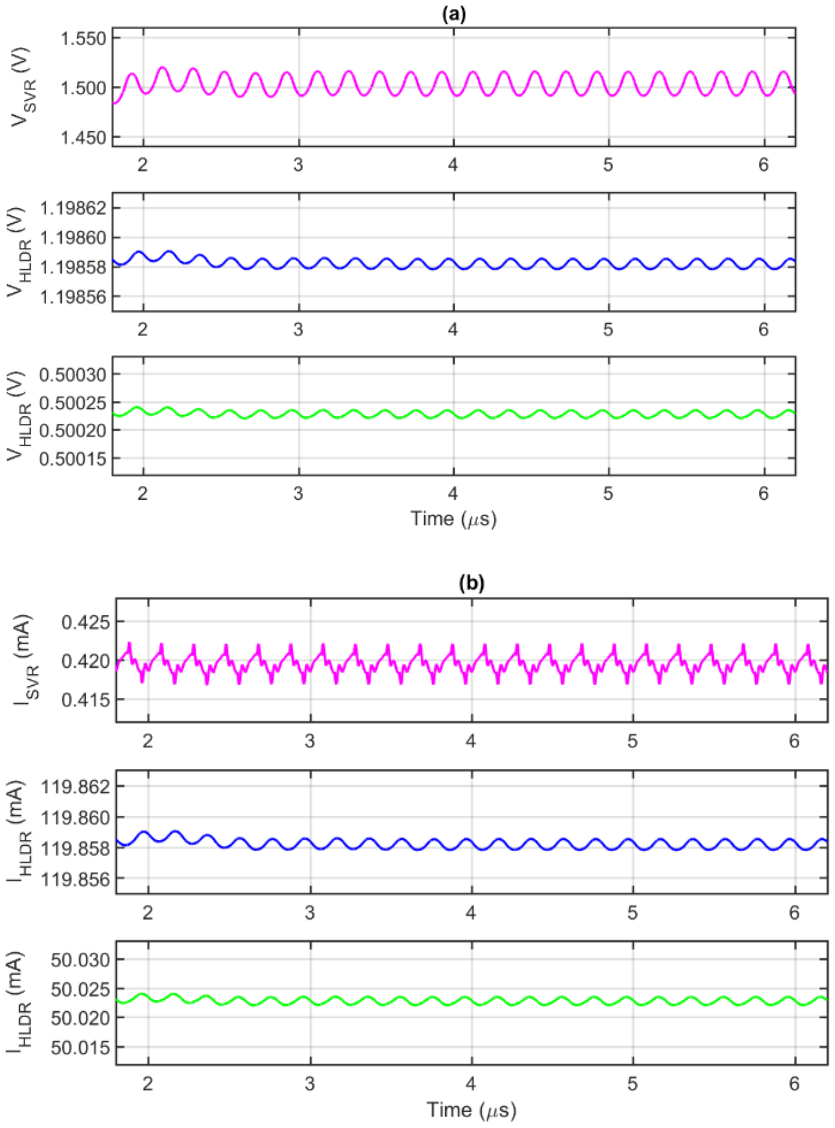

Figure 5.8: Transient response of SIS-SLOS: (a) output voltage, (b) output current

Figure 5.9 shows the AC analysis for various voltage levels of the second PMS design. The SIS-SLOS PMS is tested for a noisy oscillating DC voltage source with 5 MHz frequency to simulate a switching regulator or power supply with 5 MHz ripple noise. In

the proposed PMS design, a -132 dB of PSRR at 5 MHz is obtained for the SVR and a -88 dB PSRR is achieved in the frequency band until 100 kHz by the HLDR. Also, up until a 10 MHz frequency range, the HLDR can obtain above -62 dB PSRR. For the HLDR, the error amplifiers sets the PSRR up to near 1 MHz then the MFB takes over and extends the PSRR passed 10 MHz. Since the proposed PMS is implemented as a standalone solution by combining both the SVR and HLDR, higher ripple suppression is achieved even at high frequencies.

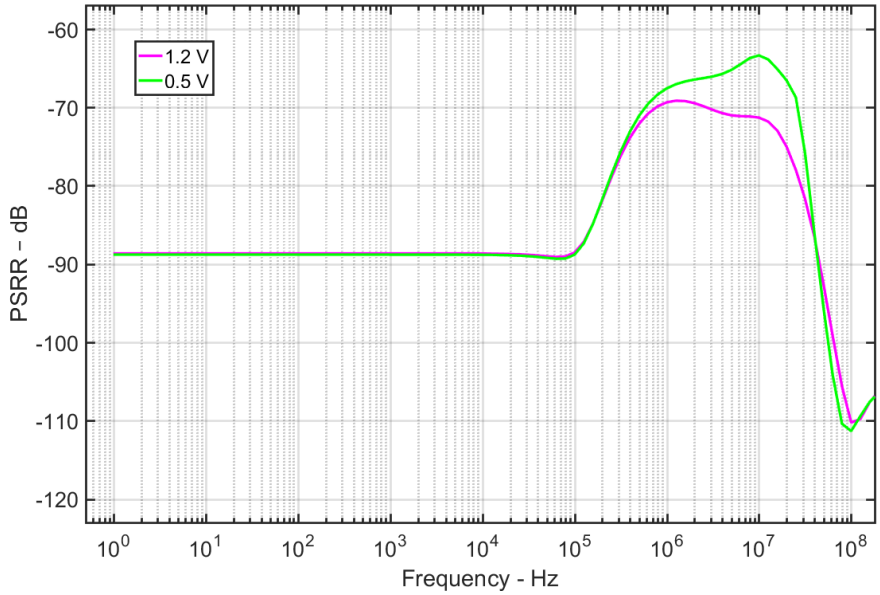

Figure 5.9: Proposed SIS-SLOS AC analysis at various voltage levels

In the proposed SIS-SLOS PMS design, the SVR is varied between a maximum output voltage of 1.5 V and a minimum output voltage of 0.5 V. At nearly a 500 mV voltage difference between the input and output (see Figure 5.10), for the line regulation of 1.5 V (magenta) output, the input voltage is varied between 2.0 to 2.5 V via a voltage step input with a 10 ns rise and fall time (green). At heavy load, the line regulation for 1.5 V output

voltage is 4.8 %. The feedback system of the SVR, along with the reference voltage, try to manage the changes in the input by adjusting accordingly. The output of the SVR is fed to the HLDR to generate an output voltage between 0.5 V to 1.2 V depending on the reference voltage. As shown in Figure 5.10, the HLDR at heavy load shows a 1.5 mV DC shift from 1.2 V (red) output voltage and a less than 1 mV DC shift from 0.5 V (blue). At heavy load, the line regulations is <1 % for both 1.2 V and 0.5 V output voltages. For the SIS-SLOS PMS, an overshoot and undershoot less than ±2 mV is shown in Figure 5.10 during the step input voltage transition.

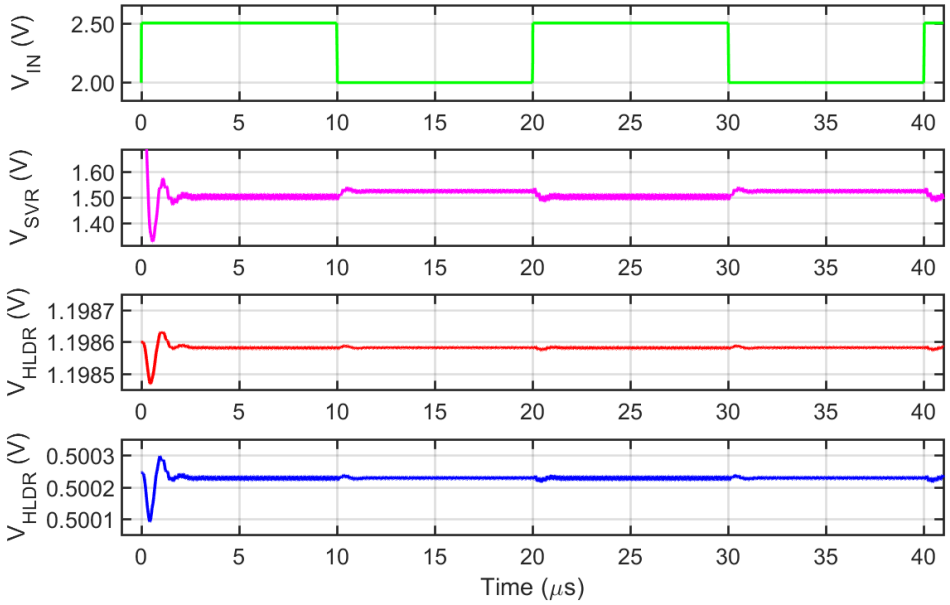

Figure 5.10: SIS-SLOS line transient response for I_{out} = 150 mA and I_{out} = 50 mA

To test for the load regulation of the SIS-SLOS PMS design, the worst-case output voltage variation is considered by changing the load current from low to high. For the SVR of SIS-SLOS, since it is not directly connected to the output load, at the 1.5 V and 0.5 V output voltages with a maximum load variation, the output voltage varied by less than 2.5

mV. For HLDR, at a 1.2 V output voltage with a maximum load variation, the output voltage varied by 3.2 mV. Also, at 0.5 V output, a 1 mV variation is witnessed as the load transitions from minimum to maximum. The load regulations are 2.7 % and 2 % for 1.2 V and 0.5 V output voltages. Figure 5.11 shows the step input and output voltage transient response of the PMS for 1.2 V and 0.5 V regulated output voltage. An overshoot and undershoot voltage around ±0.40 V is shown in the figure during the step current transition.

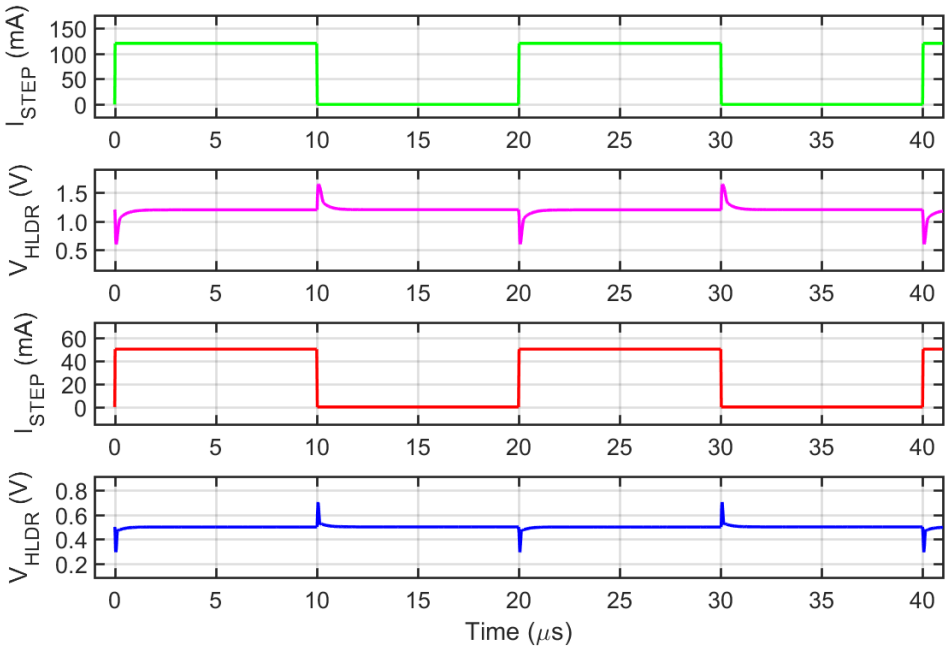

Figure 5.11: Load transient response of the proposed SIS-SLOS

5.4 Switching Input Stage with Dual Linear Output Stage

The Third PMS design (see Figure 5.12) incorporates a switching input stage with a dual linear output stage (SIS-DLOS). The total PMS area is 0.5 mm X 0.5 mm. The SVR part of the design can generate adjustable output voltage between 0.5 V to 1.6 V and 350 µA to 20 mA output current from 1.0 V to 2.5 V input voltage. In addition, the architecture

is inductorless and fully integrated on-chip design. It also has a settling time of 1.5 µs and operating frequency of 5 MHz. The PWM signal controls the operation of the switching input part via equation (3.1). Depending on the reference voltage setting, the driver switches open and close to generate a noisy voltage. To suppress the noise generated by SVR and improve the PSSR of the system, the proposed PMS employs two on-chip HLDRs as the second stage. Both of the proposed HLDRs take an input voltage range between 0.7 V to 1.5 V and can generate an adjustable output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current. Also, the architecture is fully integrated on-chip design and does not need an external capacitor for stability. In addition, it has a PSRR of -86 dB at 100 kHz and -62 dB at 10 MHz, has an output voltage ripple less than ±1 mV, and 200 mV dropout voltage.

5.4.1 Output Stage Circuit and Pass Transistor Analysis

For the third PMS design (SIS-DLOS), the op-amp at the last stage of the MFB filter is also the source of the output current. In this PMS architecture, the current source by the SVR is only used to drive the two pass transistor of the HLDRs. Beside the two HLDRs, no other output loads are fed by the SVR. The PMOS sizing for the SVR is based on the voltage drop value from a 2.5 V supply and expected maximum output current. The supply current is dictated by the load requirement in the pass transistor of the HLDR. A minimum 0.9 V voltage drop for a maximum V_{OUT} (1.6 V) voltage at a maximum output current of $I_{o(max)}$ = 20 mA is used to size the current source. Since the HLDRs are driving the output load, the PMOS sizing is based on the voltage drop value from a 2.5 V supply and expected maximum output current. For the bottom limit, a maximum 2.0 V voltage

drop for a minimum V_{OUT} (0.5 V) voltage at a maximum output current of $I_{o(max)}$ = 300 mA is used to size the current source. In addition, for the upper limit, a 1.3 V voltage drop is considered for a maximum V_{OUT} (1.2 V) voltage with a maximum output current $I_{o(max)}$ = 195 mA is also considered. For both SVR and HLDRs, using the specs provided above, the width and length of the current source is designed based on equations (3.10) and (3.11). Each of the HLDRs utilize two error amplifier stages for voltage ripple suppression and correction along with a cascaded MFB filter, and a pass transistor switch for voltage level control. For the design of a pass transistor in the HLDRs, the same spec is used as in section 5.2.1 and 5.2.2, and the width and length of the pass device is also designed based on equations (3.10) and (3.11).

5.4.2 Simulation Results

The output current and voltage of the PMS with SIS-DLOS is presented in Figure 5.13 (a) and Figure 5.13 (b). The simulation is performed with a noisy oscillating DC input. The output voltage ripple for the SVR is less than ±13.0 mV and for the HLDR, it is less than 1 mV. The SVR operating at 5 MHz is shown to be fully settled at around 1.5 µs and 400 ns for the HLDR. The proposed PMS is tested for various loads and the transient response of the output voltage and current corresponding to the input is obtained. For a heavy load, when the SVR is tested at a 60 % duty cycle, the worst-case output voltage fluctuation of 13 mV with a 3 mV DC shift occurred from 1.5 V (magenta). However, the HLDR at heavy load shows a 2.3 mV DC shift from 1.2 V (blue) output voltage and a less than 1 mV DC shift from 0.5 V (green) output voltage while maintaining less than a 1 mV worst-case voltage fluctuation. In the SIS-DLOS PMS design, the SVR can supply up to

1.6 V and remain stable, since the load requirement is only coming from the pass transistors of the two HLDRs and it is well within the upper current limit of the design. The top of Figure 5.13 (b) depicts the output current of the SVR, which is the input sum of the two pass transistors of the HLDRs (magenta).

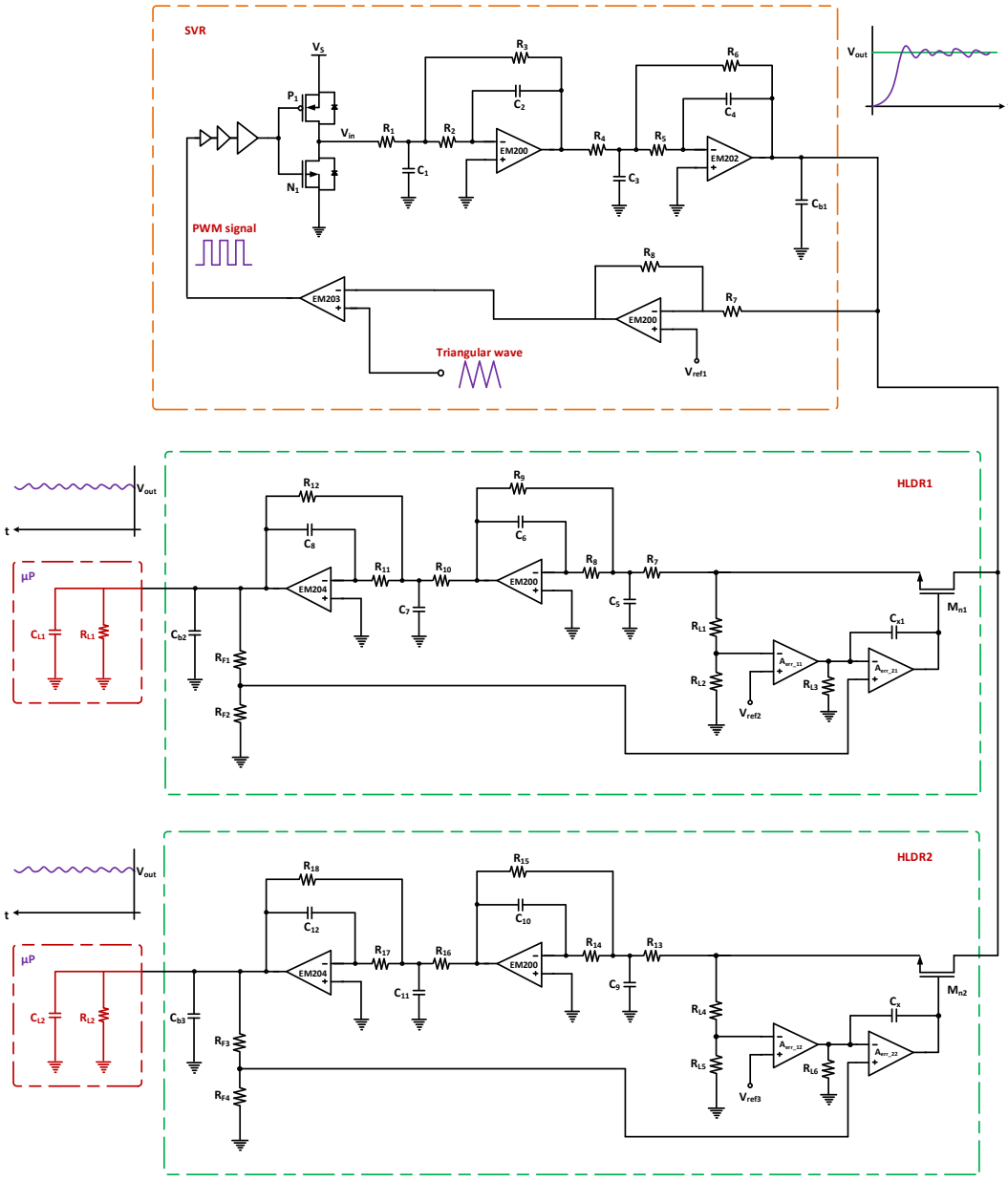

Figure 5.12: Proposed on-chip SIS-DLOS PMS deign

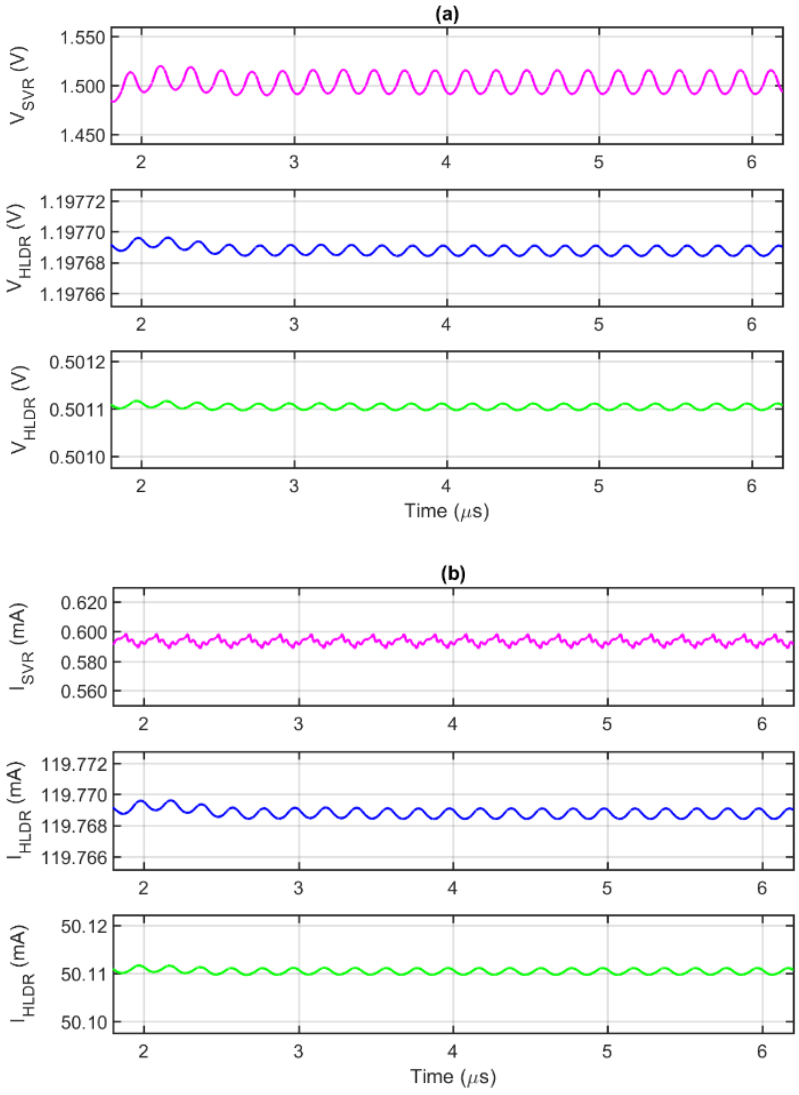

Figure 5.13: Transient response of SIS-DLOS: (a) output voltage, (b) output current

Figure 5.14 shows the AC analysis for various voltage levels of the third PMS design. The SIS-DLOS PMS is tested for a noisy oscillating DC voltage source with 5 MHz frequency to simulate a switching regulator or power supply with 5 MHz ripple noise. In the proposed PMS design, a -132 dB of PSRR at 5 MHz is obtained for the SVR and a -88 dB PSRR is achieved in the frequency band until 100 kHz by the HLDR. Also, up until a

10 MHz frequency range, the HLDR can obtain above -62 dB PSRR. For the HLDR, the error amplifiers sets the PSRR up to near 1 MHz then the MFB takes over and extends the PSRR passed 10 MHz. Since the proposed PMS is implemented as a standalone solution by combining both the SVR and HLDR, higher ripple suppression is achieved even at high frequencies.

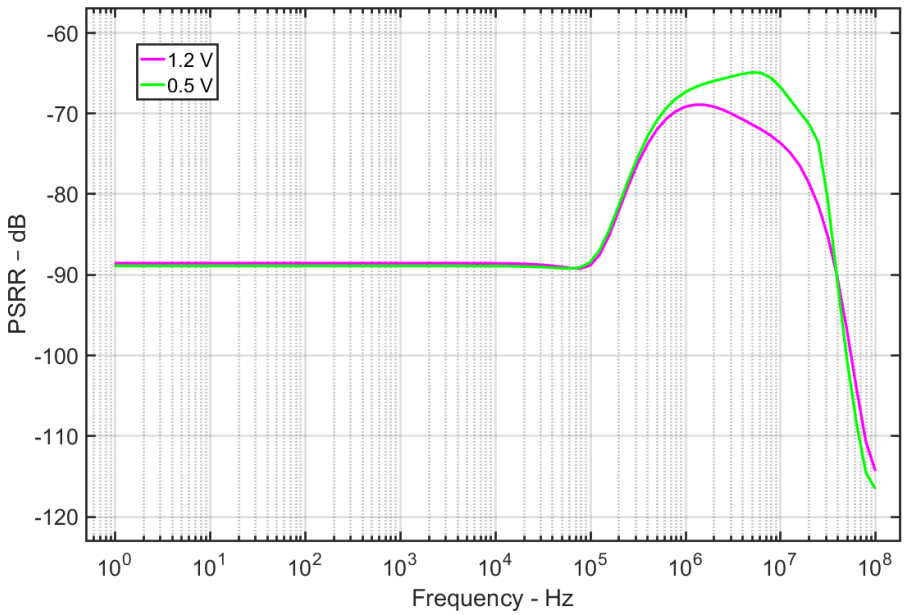

Figure 5.14: Proposed SIS-DLOS AC analysis at various voltage levels

In the proposed SIS-DLOS PMS design, the SVR is varied between a maximum output voltage of 1.5 V and a minimum output voltage of 0.5 V. At nearly a 500 mV voltage difference between the input and output (see Figure 5.15), for the line regulation of 1.5 V (magenta) output, the input voltage is varied between 2.0 to 2.5 V via a voltage step input with a 10 ns rise and fall time (green). At heavy load, the line regulation for 1.5 V output voltage is 2.8 %. The feedback system of the SVR, along with the reference voltage, try to manage the changes in the input by adjusting accordingly. The output of the SVR is fed to

two HLDRs to generate an output voltage between 0.5 V to 1.2 V depending on the reference voltage. As shown in Figure 5.15, the HLDRs at heavy load show a 2.3 mV DC shift from 1.2 V (red) output voltage and a less than 1 mV DC shift from 0.5 V (blue). At heavy load, the line regulations is <1 % for both 1.2 V and 0.5 V output voltages. For the SIS-DLOS PMS, an overshoot and undershoot less than ±2 mV is shown in Figure 5.15 during the step input voltage transition.

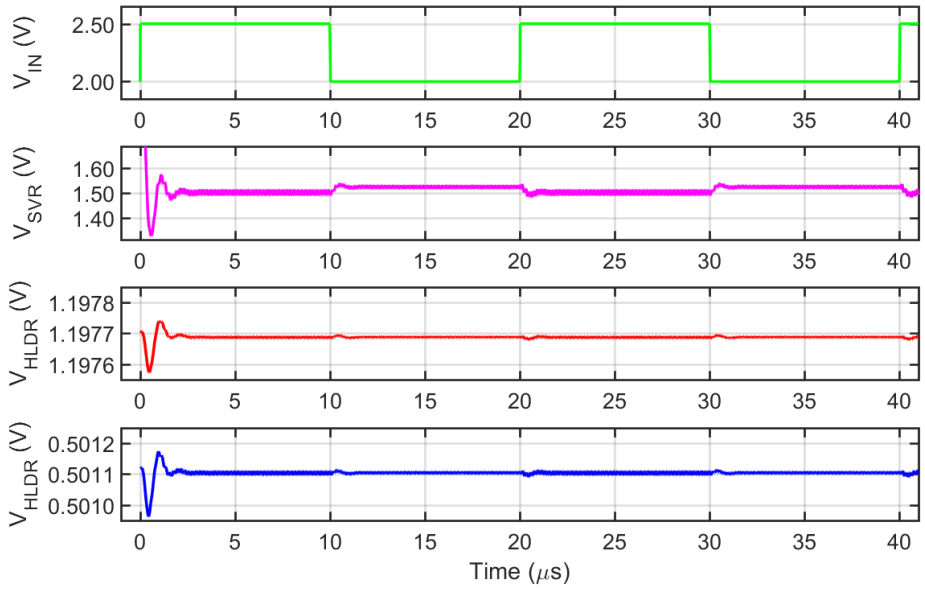

Figure 5.15: SIS-DLOS line transient response for I_{out} = 150 mA and I_{out} = 50 mA

To test for the load regulation of the SIS-DLOS PMS design, the worst-case output voltage variation is considered by changing the load current from low to high. For the SVR of SIS-DLOS, since it is not directly connected to the output load, at the 1.5 V and 0.5 V output voltages with a maximum load variation, the output voltage varied by less than 2.5 mV. For both HLDRs, at a 1.2 V output voltage with a maximum load variation, the output voltage varied by 3.2 mV. Also, at 0.5 V output, a 1 mV variation is witnessed as the load

transitions from minimum to maximum. The load regulations are 2.7 % and 2 % for 1.2 V and 0.5 V output voltages. Figure 5.16 shows the step input and output voltage transient response of the PMS for 1.2 V and 0.5 V regulated output voltage. An overshoot and undershoot voltage less than ±0.45 V is shown in the figure during the step current transition.

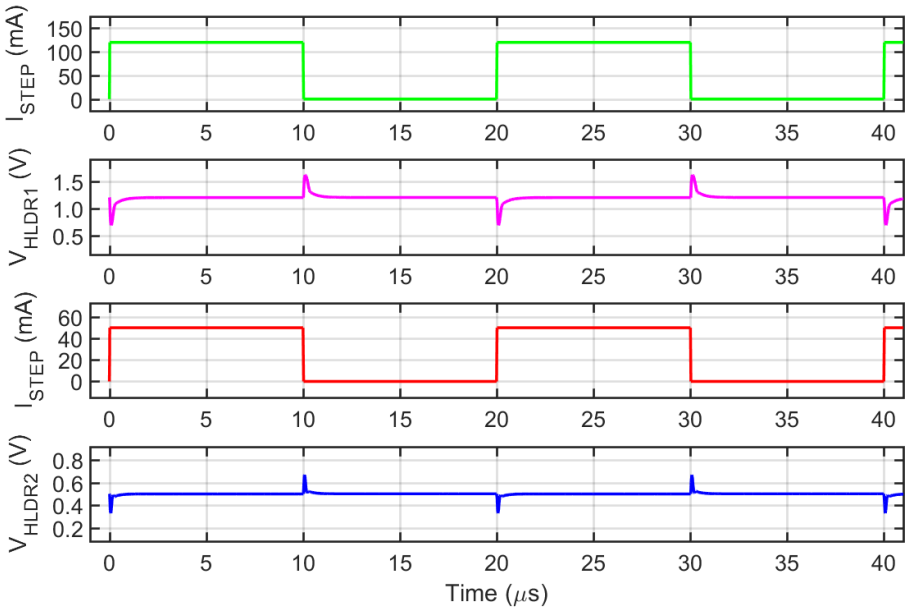

Figure 5.16: Load transient response of the proposed SIS-DLOS

5.5 Regulator Performance

A photograph of the IC chip containing all three PMS designs is shown in Figure 5.17. The chip is fabricated using a C5 CMOS process through a Multi-Project Wafer (MPW) run provided by MOSIS. The first design (SIS-SOS-SLOS) at the upper left side is the switching stage with single switching and a single linear output stage. In the first PMS, the SVR is to the right, the HLDR is to the left, and the entire PMS takes up an area of 0.48 mm^2. The second design (SIS-SLOS), at the middle left side, is the switching stage

with a single linear output stage. The SVR does not have large power transistors since the output is only coming out of the HLDR. Because of that, the second PMS area, which is 0.44 mm^2, is slightly less than that of the first PMS. The third design (SIS-DLOS), at the bottom left side, is the switching stage with a dual linear stage. In this PMS design, the SVR is feeding two HLDRs. For that reason, this PMS utilizes a greater area than both the first and second designs and also requires more input/output pins. The third design has a total area of 0.70 mm^2.

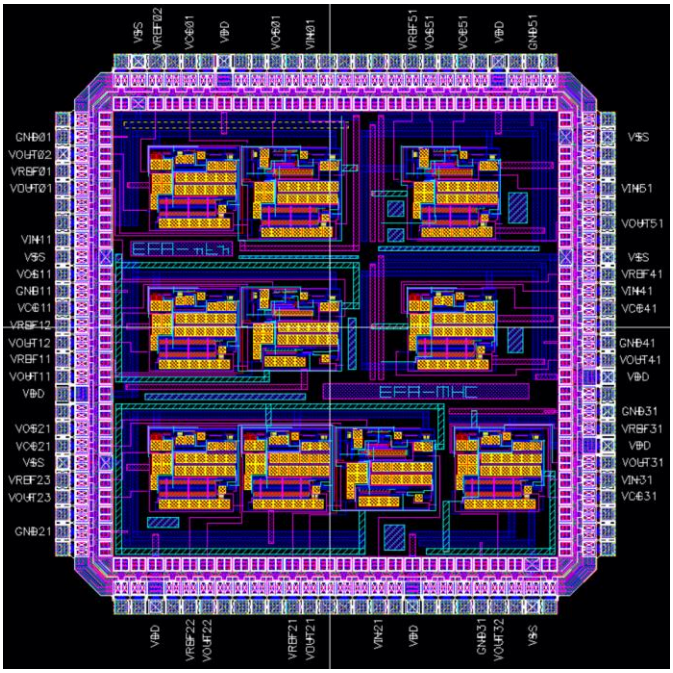

Figure 5.17: Layout of the fabricated CMOS IC containing all three PMS designs

Testing the stability of the PMS designs at low I_o, a maximum R_L with minimum C_L is considered. This allows the regulator to always supply a minimum output current of V_{OUT}/R_{Lmax}. For the HLDO and SVR, at the lowest voltage setting, a 0.5 V output voltage is regulated with the lowest output current. At 5 KΩ, both SVR and HLDR can supply a

minimum current of 100 µA and maintain stability. The output stage OTA is designed for a large resistive load in mind to make sure the gain of the amplifier is not significantly lowered and most importantly that it remains stable. The switching loss of SVR by the drivers is minimized since a different current driver transistor performs the current sourcing linearly. The SVR design can achieve efficiency as high as 78 %. The efficiency of the SVR is lower than a conventional buck converter, but it is better than linear regulators while being inductorless and fully on-chip. The efficiency of the linear regulator is limited by V_{OUT}/V_{IN}, and the proposed HLDR is also governed by the same parameter. At full load, the efficiency of HLDR is lower when compared with light load. However, for the SVR, at full load, the efficiency is higher when compared with light load.

Table 5.1 presents a comprehensive performance analysis between each design. Three on-chip PMS architectures are presented. Each one of the designs are pertinent for different applications. The regulators are capable of supplying adjustable output voltages as specified by the table. In the PMS designs, the driver large transistors take up a considerable portion of the chip area. The size of the driver transistors in the output stages can be adjusted according to the design requirements depending on the current demand, which will increase or decrease the chip size. In addition, the architecture choice can also dictate the area of the design. As depicted by the table, SIS-SOS-SLOS provides both SVR and HLDR output at the output stage. This can drive two different loads, one that can tolerate noise and another sensitive to noise. The main objective of the PMS designs is to provide a complete fully on-chip PMS design that can incorporate both switching and linear

regular that can suppress output voltage ripple. All the PMS designs generate less than 1 mV output ripple noise with less than 4 mV full load worst DC shift.

Table 5.1: Performance comparison among proposed designs

		Tech. [µm]	I_Q [mA]	On-chip area [mm^2]	V_{in} [V]	V_{out} [V]	Max. Load [mA]	PSRR
1st Stage SVR	SIS-SOS-SLOS	0.6	0.85	0.48	1.0 – 2.5	0.5 – 1.5	150	-151 @ 5 MHz
1st Stage SVR					1.2 – 2.5	0.7 – 1.5	150	-100 @ 10 MHz
2nd Stage HLDR					0.7 – 1.5	0.5 – 1.2	120	-88 @ 100 kHz -68 @ 1 MHz -63 @ 10 MHz
1st Stage SVR	SIS-SLOS	0.6	0.83	0.44	1.2 – 2.5	0.7 – 1.6	20	-132 @ 5 MHz
2nd Stage HLDR					0.7 – 1.5	0.5 – 1.2	120	-88 @ 100 kHz -68 @ 1 MHz -63 @ 10 MHz
1st Stage SVR	SIS-DLOS	0.6	1.15	0.70	1.2 – 2.5	0.7 – 1.6	20	-132 @ 5 MHz
2nd Stage HLDR					0.7 – 1.5	0.5 – 1.2	120	-88 @ 100 kHz -68 @ 1 MHz -63 @ 10 MHz
2nd Stage HLDR					0.7 – 1.5	0.5 – 1.2	120	-88 @ 100 kHz -68 @ 1 MHz -63 @ 10 MHz

5.6 Summary

In this chapter, we have introduced a fully on-chip power management system that incorporates a switching regulator along with a linear regulator in a single design to achieve better ripple suppression. The proposed PMS architecture utilizes a cascaded second order multiple feedback low pass filter (MFB LPF). The presented switching regulator architecture is a fully on-chip inductorless design. The linear regulator is implemented for the post-regulating stage to suppress ripple noise generated by the switching regulator. The PMS scheme has three different combinations: the switching stage with a single switching and a single linear output stage (0.48 mm^2), a switching stage with a single linear output stage (0.44 mm^2), and a switching stage with a dual linear stage (0.70 mm^2). The proposed design takes input voltage range between 1.0 V to 2.5 V at the first switching stage. It can then generate adjustable switching output voltage between 0.5 V to 1.5 V/1.6 V and 100 µA to 150 mA output current, and/or adjustable linear output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current at the second stage. Extensive post fabrication analysis and experimental measurements have been performed to validate the presented hybrid voltage regulator. In addition, the architecture is fully integrated on-chip design and does not need an external inductor or capacitor placed on the PCB or host IC's package. The switching regulator has an operating frequency of 5 MHz and the linear regulator has a PSRR of -86 dB at 100 kHz and -62 dB at 10 MHz. The innovative PMS design can deliver power both as a stand-alone regulator or in synergy with a switching regulator. In addition, it offers an effective technique for SOC integration of the voltage regulator.

CHAPTER 6

SLEEP TRANSISTOR DESIGN USING DOUBLE-GATE FDSOI

Power gating circuits are utilized to manage power consumption and thermal stress in microprocessors and other high-performance integrated circuits. Most of the power gating techniques utilize sleep transistors in different configurations to reduce the subthreshold leakage current, which is the primary source of the standby power. These sleep transistors, which are added between the supply lines and the circuits as header and footer switches, impose additional area, delay, power and other overheads and complexities. This work introduces the concept of combining the functionality of the sleep transistors with the logic devices by utilizing fully depleted silicon-on-insulator (FDSOI) device. This FDSOI transistor based power gating circuit design approach will eliminate the requirement of employing a separate set of sleep transistors to place the circuit in the sleep or idle mode. This will reduce the overall complexity and overheads of integrated circuits and simplify power gating techniques. In the proposed circuit design approach, the flexibility to control the threshold voltage of a double-gate FDSOI device via back gate has been exploited to eliminate the need for using a separate set of sleep transistors. The presented sleep transistor design is verified via Hspice simulation using Leti-UTSOI model from *CEA-Leti*.

6.1 Introduction

Power gating is one of the popular methods to manage leakage power during the standby mode in low-power and high- speed ICs. It works by using transistor based switches (sleep transistors) to shut down part of the circuit block and put them in idle mode.

Sleep transistors help ICs manage power and thermal effects efficiently. The total power consumption of the ICs is comprised of static, dynamic and short circuit effects. The dynamic behavior has an exponential effect on the power dissipation, and as a result, it leads to a higher temperature injection in the circuit node. In the static mode, temperature has an exponential effect on the leakage current. This inter-dependence of power and thermal impacts makes efficient power gating circuit a very critical requirement for integrated circuits and systems.

Traditional sleep transistor based power gating techniques utilize one of the three approaches as shown in Figure 6.1. The first one employs *high-Vt* transistors between the supply lines and the circuit to create virtual *Vdd* and *Vss* nodes at every cell that needs to be shut down or placed in sleep mode. The *high-Vt* sleep transistors are implemented in the form of a "header switch" and a "footer switch" to isolate the virtual supply nodes from the actual supply lines (see Figure 6.1 (a) and [34]). The second approach utilizes only a "header switch" by connecting a *high-Vt* transistor between the actual power rail and the virtual *Vdd* node (see Figure 6.1 (b) and [32]). And the third approach utilizes only a "footer" switch (see Figure 6.1 (c) and [30]). All of the above approaches are used to lower subthreshold leakage. Recent advance techniques such as reconfigurable sleep transistor technique [38] and negative bias temperature instability (NBTI) aware sleep transistor [39] designs are proposed as potential solutions. In [56], sleep transistor is inserted as part of 3T DRAM cell to reduce leakage power. In all of these approaches, *low-Vt* transistors are used inside the logic circuits to ensure higher performance during the active mode of the circuit. *High-Vt* sleep transistors are placed between the logic circuits and the supplies to

reduce leakage power during the standby period. These sleep transistors used as “header” and/or “footer” switches impose extra area, delay and power overheads. Additionally, the design complexity involved with the implementation of transistors with different threshold voltages in the same circuit makes these design techniques less appealing. Moreover, the additional wiring required for the virtual nodes will introduce unwanted RLC issues and IR-drops causing voltage variations.

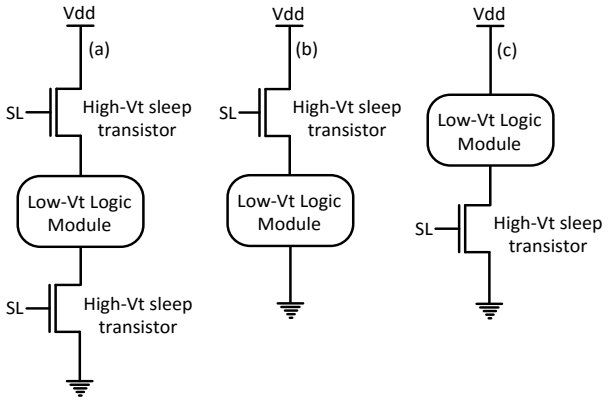

Figure 6.1: Conventional sleep transistor designs. (a) Showing a header switch and a footer switch. (b) Showing a header switch. (c) Showing a footer switch

The efficiency of a power-gating scheme involves minimum off-current (I_{off}) and low on-resistance (R_{on}) (i.e., high I_{on}) for the sleep transistors while keeping the wake-up time below 100ns [57]. In line with this specification, a potential newer solution is presented in this work. The new power gating approach will not require a separate set of sleep transistors (header and footer switches). The proposed technique utilizes double-gate fully depleted SOI (FDSOI) MOSFET (see Figure 6.2) that will perform both the functions of the sleep transistors and the logic devices. This will help overcome the limitations of the existing sleep transistor designs. Under this approach, we will not need a separate set of sleep transistors and can avoid all the overheads and complexities of implementing two

sets of transistors in the same circuit with two different threshold voltages. In the proposed technique, we will achieve high and low threshold voltages dynamically by utilizing double-gate FDSOI device. Here, the idea is to exploit the back-gate bias in a double-gate FDSOI to achieve the required high and low threshold voltage values dynamically without employing header and/or footer transistor.

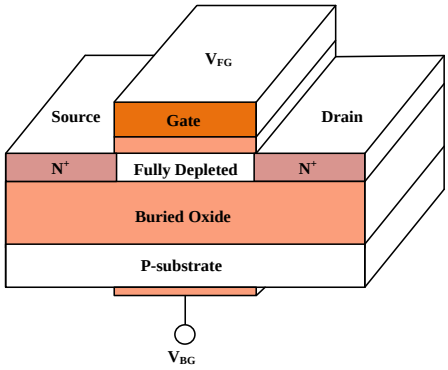

Figure 6.2: Illustration of Double Gate SOI MOSFET

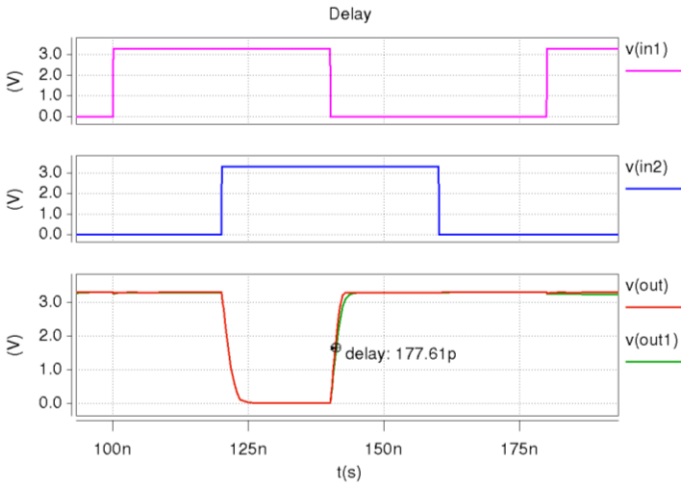

Figure 6.3: Propagation delay incurred by header switch (transistor) in 2-input NAND gate SOI FET design at *high-Vt*

6.2 FDSOI Based Power Gating Technique

In conventional CMOS sleep transistor design, logic gates or blocks are connected to the power supplies through sleep transistors [30]. These sleep transistors are controlled

by signals generated by a central gate controller or distributed control logics. As stated in [30], centralized sleep transistor designs suffer from large interconnect resistances between distant blocks. Such resistance has to be compensated by an extra-large sleep transistor area. In the distributed and cluster-based designs of sleep transistors (as opposed to the centralized control approach), additional wiring is required. In the proposed FDSOI design the additional sleep transistors are completely eliminate, which provides 100% savings of the area overheads of the sleep transistors. However, the wiring overheads remain the same.

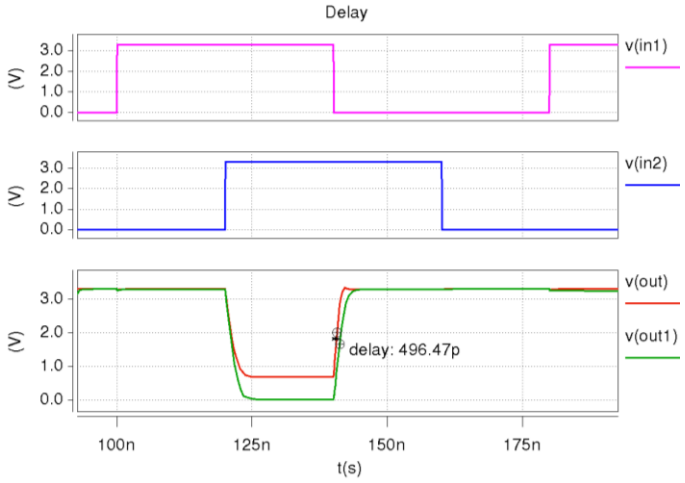

Figure 6.4: Propagation delay incurred by header switch (transistor) in 2-input NAND gate SOI FET design at *low-Vt*

$$T_{pd} = \frac{C_L V_{dd}}{(V_{dd} - V_{tL})^{\alpha}} \tag{6.1}$$

$$T_{pd-MT} = \frac{C_L V_{dd}}{(V_{dd} - V_{sd} - V_{tL})^{\alpha}} \tag{6.2}$$

$$PL = 1 - \frac{T_{pd}}{T_{pd-MT}} \tag{6.3}$$

The additional wiring and the placement of additional sleep transistors (as in Figure 6.1) between the functional blocks and the power supplies result in a delay penalty in the conventional designs. In the absence of a sleep transistor, the propagation delay τ_{pd} of a logic gate depends on the supply and threshold voltages. This dependency can be expressed by the Alpha Power law model as depicted in (6.1) [58], [59], where C_L is the load capacitance, α is the velocity saturation index, which is process specific. For simplicity, α is usually assumed to be 1 in short-channel device. When a sleep transistor is present, a source drain voltage (V_{sd}) drop occurs causing the propagation delay to increase as shown in (6.2) [30]. The performance loss (PL) due to the increase in propagation delay related to the sleep transistors is defined in [31] and depicted by (6.3). Since the proposed design eliminates the additional sleep transistors, this delay overheads depicted by (6.3) is absent in the proposed design. On Figure 6.3, two input NAND gate with header switch (green) and without header switch or back gate controlled design (red) is depicted. At a high threshold voltage setting, the proposed approach shows 177.6ps propagation delay improvement. Figure 6.4 shows how the new method (red) can farther push the threshold voltage to low setting and allow it to turn on quicker than the one with header switch (green). A whopping near 500ps improvement is exhibited via dynamic threshold control. Additionally, the slope of the new circuit is much steeper, this is especially important for the transient response of the circuit in active mode. The work will discuss and show in depth how the threshold voltage is dynamically controlled via back gate in latter sections.

Now the question is how to combine the functionality of the sleep transistors with that of the logic transistors. To answer this question, we have to identify the design and

functional objectives of the sleep and logic transistors. For faster operation in the active mode we would like to have lower threshold voltage (for higher gate drive) for the logic transistors. For power savings in the standby mode, we would like to have higher threshold voltage in the sleep transistors, because higher threshold voltage leads to exponential decrease of the subthreshold current, which is the primary source of standby power. Since the same set of transistors will be performing both the functions (of logic and sleep transistors) in the proposed design, we need to be able to dynamically set lower and higher values of threshold voltage in same transistors. This can be done in a double-gate SOI device. The flexibility of the double-gate SOI devices provides the option to dynamically set the threshold voltage to appropriate level for active and standby modes. Moreover, SOI technology is in general attractive in terms of performance (high speed, low power consumption, radiation-hardness, etc.), higher scalability, improved noise immunity, lower parasitic capacitances, and higher yield [60], [61].

6.3 Double-Gate FDSOI

Figure 6.2 shows the basic device model of the double-gate fully depleted SOI MOSFET, where an additional gate contact (back gate) is provided under the substrate. As the name designation indicates, it consists of two gates that control the charges in the silicon channels. The fundamental idea behind the double-gate FDSOI technology is to add additional conductive under layer beneath the SOI device [62]. As depicted in the Figure 6.2, the body region of this SOI MOSFETs is floating as opposed to the bulk MOSFET device, where the body is inherently connected to the substrate. From functional point of view, the double-gate device can be viewed as two MOSFETs (front and back MOSFETs)

that share same body, drain, and source regions [63]. There are two structures of widely used SOI MOSFETs: (i) fully depleted (FD) and (ii) partially depleted (PD) channel region (body) [62]. This work focuses on FDSOI devices for the proposed sleep transistor design. The FDSOI provides much better control of the back-gate on the channel. In the PDSOI, the back gate or the substrate has very minor influence on the front surface and channel potential. In FDSOI device, the silicon film thickness is usually less than or equal to half of the depletion width of the bulk device [62]. Electrical parameters, including threshold voltage and drain current of the SOI devices, are influenced by the film thickness. Since fully depleted SOI MOSFET threshold voltages are sensitive to the variations in SOI silicon film thickness, T_{si} [64], thin films are required in order to have great control over the performance of a device. In addition, thinner SOI film thickness is required for the minimization of short-channel effects and elimination of the current kinks in the SOI MOSFETs [65]. The surface potentials of FDSOI at the front and back interfaces are strongly coupled to each other and capacitively coupled to the front-gate and the substrate through the front-gate oxide and buried oxide, respectively [62].

The threshold voltage of a double-gate FDSOI can be modeled as in (6.4) and (6.5), where V_t^f and V_{BG} are the front threshold and back gate voltages, V_{FB}^f and V_{FB}^b are the front gate and back gate flatband voltages, C_{ox}, C_{BOX}, and C_{si} are front and back gate oxide, and the buried oxide capacitance and depleted silicon film capacitances. Q_b is the area charge density in the depleted silicon film [65]. Figure 6.5 shows the dependence of the threshold voltage on the back gate of the device for both NSOI and PSOI. Another option to control subthreshold leakage is to lower the subthreshold swing (S) of the transistor. The FDSOI

provides a lower value of *S* (between 65-80 mV/dec) and it can even be further improved by reducing η (DIBL or drain induced barrier) using the thin film (T_{si}) design. The achievable values of *S* in the conventional bulk MOSFET are between 90-120 mV/dec. The subthreshold swing *S* of FDSOI device is given by (6.6) [66], where $C_{it1,2}$ is interface-trap capacitance in the wafer process, which can dynamically be charged or discharged. In this device, the threshold voltage values can be controlled by applying a bias voltage at the back gate.

$$V_t^f = V_{FB}^f + 2\Phi_B - \frac{Q_b}{2C_{Ox}} - \left(V_{BG} - V_{FB}^b - 2\Phi_B + \frac{Q_b}{2C_{BOX}}\right) \cdot \frac{C_{si}C_{BOX}}{C_{ox}\,(C_{si} + C_{BOX})} \tag{6.4}$$

$$Q_b = -qN_AT_{si}\ or + qN_DT_{si} \tag{6.5}$$

$$S_1^{dep} = 2.3\frac{KT}{q}\left(1 + \frac{C_{it_1}}{C_{Ox1}} + \frac{C_{Ox2} + C_{it_2}}{C_{si} + C_{Ox2} + C_{it_2}} + \frac{C_{si}}{C_{Ox1}}\right) \tag{6.6}$$

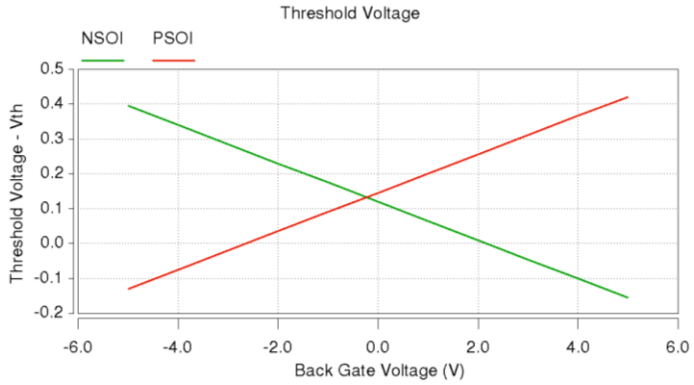

Figure 6.5: Variation of threshold voltage with back gate bias

6.4 2-input NAND Gate based on FDSOI

Figure 6.6 shows a 2-input NAND gate, where the conventional bulk MOSFET transistors are replaced by double-gate FDSOI transistors. In the proposed design, the front

gates of all of the transistors of Figure 6.6 are connected to appropriate supplies, while the back gates are connected to a centralized back gate controller (BCR). It can also be managed by distributed control logic in the same manner conventional sleep transistors are connected and controlled. Therefore, the wiring and controlling complexity and overheads of the back-gate connections needed for the FDSOI transistors are not different from those of the conventional sleep transistors. The advantage of this circuit is that it does not need the additional sleep transistor, because the back-gate MOSFET within the double-gate FDSOI device structure will perform this function. Different levels of I_{on} current can be specified based on the effective bias at the back gates of the transistors. In the active mode, higher I_{on} current can be set for faster operation. In the standby mode the transistors can be set to low-current and low-power mode dynamically. Additional analysis are presented in the last section.

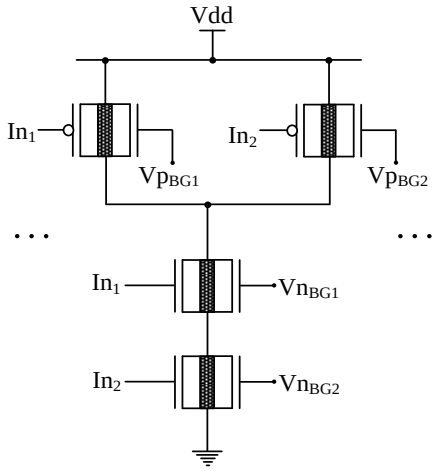

Figure 6.6: A 2-input NAND gate based on the proposed design concept, where the same set of transistors will be used as the sleep and logic transistors

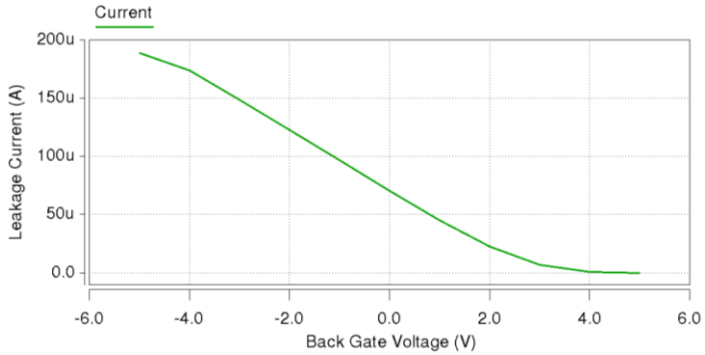

Figure 6.7: Variation of leakage current with the back gate voltage.

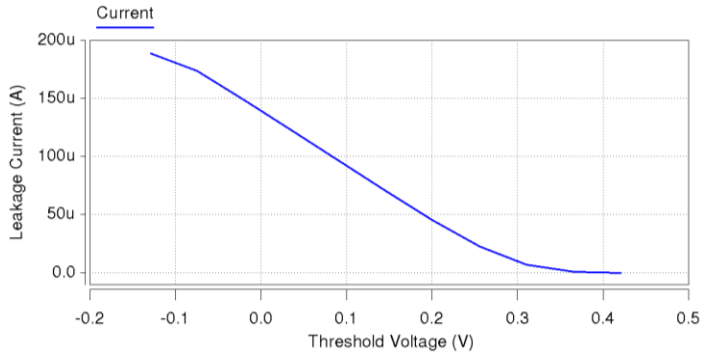

Figure 6.8: Relation between leakage current and threshold voltage

6.5 Reduction of Leakage Current and Power Dissipation

The subthreshold leakage current in a MOSFET device can be modeled as in (6.7) - (6.9) [59], [67], and [68]. These equations are slightly modified to represent the back gate bias voltage.

$$I_{leakage} = I_0 e^{\frac{V_{GS}-V_{THf}-\eta V_{DS}+\gamma V_{BS}}{nV_T}}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{6.7}$$

$$I_{leakage} = I_0 e^{\frac{V_{GS}-V_{THf}-\eta V_{DS}+\gamma V_{BS}}{S}}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{6.8}$$

$$I_0 = \mu C_{ox}\frac{W}{L}V_T^2 e^{1.8} \; and \; V_T = \frac{KT}{q} \tag{6.9}$$

Here V_{GS}, $V_{DS,}$ and V_{BS} are the gate to source, drain to source, and bulk to source voltages, respectively, and μ denotes the carrier mobility. C_{ox} is the gate oxide capacitance, W and L denote the channel width and length of the SOI MOSFET, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, V_T is the thermal voltage, V_{THf} is the threshold voltage at the front gate (as a function of the bias voltage), γ is the body effect coefficient, η denotes the drain induced barrier lowering coefficient, n is the subthreshold swing coefficient, and S is the subthreshold swing (as in equation 6).

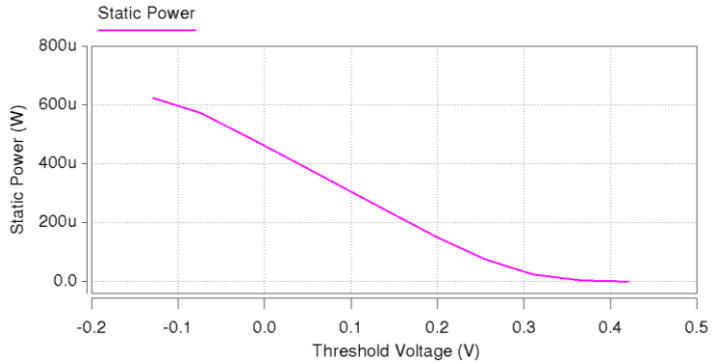

Figure 6.9: Relation between threshold voltage and standby power

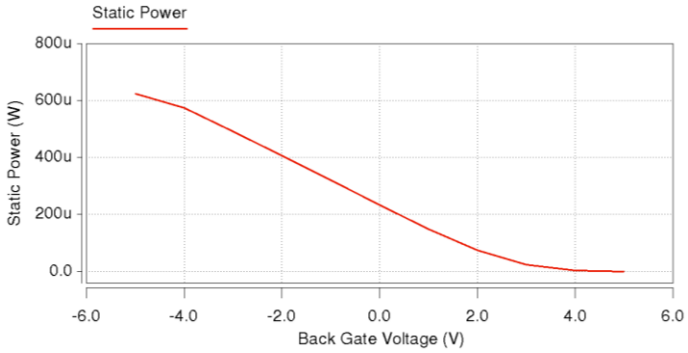

Figure 6.10: Relation between back gate voltage and standby power

For the proposed 2-input NAND sleep transistor circuit, various Hspice simulations were performed and the results are presented in Figure 6.7 to Figure 6.10. Figure 6.7 shows the variation of the leakage current with the back gate voltage. The correlation between the

threshold voltage and leakage current is shown in Figure 6.8. As depicted by Figure 6.7 and Figure 6.8, by setting proper value of the threshold voltage through back-gate, an acceptable level of leakage current can be set for the standby mode. The subthreshold leakage current is the dominant source of static or standby power dissipation. Figure 6.9 and Figure 6.10 shows the change in standby power with the change of the threshold voltage and back gate bias. Therefore, by properly adjusting the back gate bias it is possible to control the standby power dissipation in the circuit designed following approach depicted in Figure 6.6 for a two input NAND gate.

6.6 Preliminary analysis and simulation results

Before implementing the design on Hspice, the sleep transistor design was first simulated and verified on MATLAB. The equations provided above from (6.4) to (6.9) are used to base the foundation for the design approach. The simulation results for the preliminary analysis are presented below. The input voltages as well as some of the device parameters are not the same with the Hspice design. Also, some of the equations were simplified to facilitate the coding. Figure 6.11 (a), shows threshold dependency of NSOI by varying the back gate voltage. FDSOI can be viewed and modeled as two FETs with two gates that control the charges in the silicon channels (see Figure 6.11 (b)). This allows the designer to accurately modulate the I_{on} current to increase and I_{off} current to decrease dynamically. Figure 6.11 (c) and Figure 6.11 (d), are very critical especially to sleep transistor design. The Figures show the flexibility of FDSOI to the back bias voltage in determining the leakage current. Farther expanding on the analysis, Figure 6.11 (e) and Figure 6.11 (f) explain the correlation between high and low threshold voltage and their

role when it comes to static power dissipation.

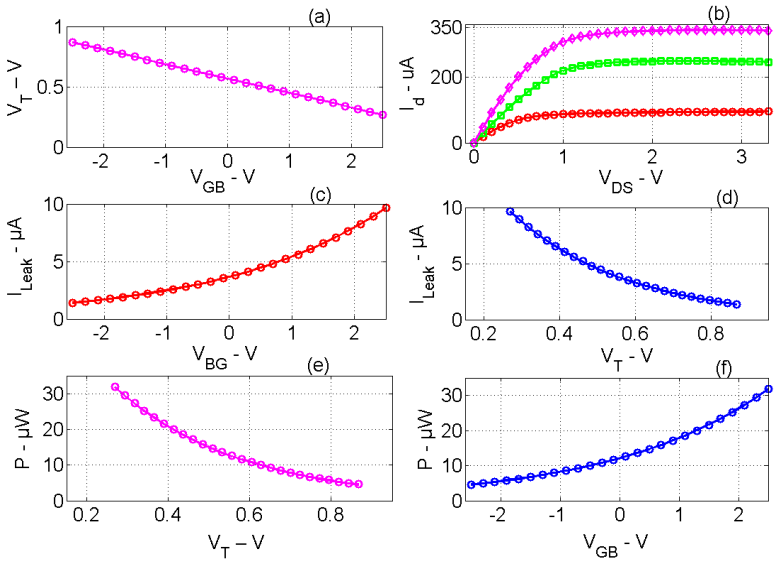

Figure 6.11: (a) Threshold voltage vs back gate bias. (b) Drain current for bottom gate (red), top gate (green), and top and bottom gate (magenta) with respect to drain voltage and back gate bias. (c) Leakage current vs back gate voltage. (d) Leakage current vs threshold voltage. (e) Threshold voltage vs static power. (f) Back gate voltage vs static power

6.7 Summary

In this work, we presented a new design approach to mitigate static power consumption using double gate FDSOI transistors. As the power gating techniques based on sleep transistors are an essential part of IC design, new methods need to be explored for robust and efficient design. We proposed an alternative approach to design sleep transistors and control their characteristics via back gate bias. This approach simplifies design complexity, reduces chip area, improves power dissipation, and lowers thermal effects in the circuit. Our proposed design prevents performance loss due to propagation delay caused by additional transistors between the *low-Vt* logic blocks and supply line. The key of this approach is the fact that it incorporates the sleep transistor design as part of the circuit design and avoids the standalone complex design technique. It provides a dynamically

controlled *Vt* for the circuits that need to be switched between sleep and active modes. There are many design and implementation issues that are still being investigated. In this work, we just presented the new concept of combining the functionalities sleep and logic transistors by utilizing double-gate FDSOIC device in integrated circuits.

CHAPTER 7

SUBTHRESHOLD REGION SLEEP TRANSISTOR DESIGN

Sleep transistors are essential parts of the power gating techniques used in IC design to reduce/manage subthreshold leakage current. Most of the microprocessors and high-density ICs employ many sleep transistors. In this work, we present a sleep transistor design based on our proposed ferroelectric insulator based device, Silicon on Ferroelectric-Insulator FET (SOFFET). This device has shown tremendous potential for various Ultra-low-power (ULP) applications. SOFFET has the potential to provide high performance $multi - V_T$ design, strong threshold voltage control, low voltage operation, *below 60mV/decade* subthreshold swing, higher current drive, and better short-channel characteristics. These advantages of SOFFET makes it very attractive for the sleep transistors design and many other integrated circuit applications. The flexibility to control the threshold voltage via back gate offers a tremendous opportunity for double-gated SOFFET to introduce a new generation of power gating and leakage control techniques by combining the operation of the sleep transistors and the logic devices. The proposed approach simplifies the design complexity, reduces chip area, eliminates voltage drop and extra power dissipation in the conventional sleep transistors, and improves overall speed and energy efficiency of the system.

7.1 Introduction

Sleep transistors are used to manage leakage power in the standby modes. Conventional sleep transistor architectures are presented in Chapter 6 (see Figure 6.1). The existing sleep transistor design utilizes a high-Vt header/footer switch and a low-Vt

transistors for logic gates. In ULP application, this design approach is hindered by the headroom. In subthreshold design, the addition of sleep transistors between the supply and logic gates creates voltage drop farther lowering the supply voltage. This can seriously impede the logic gates by preventing the pull up network not to swing all the way up to the rail. Also, additional signal delay is incurred due to the sleep transistor. Moreover, the additional wiring in the virtual nodes cause unwanted RLC issues, switching noise and results in IR-drops leading to voltage variations.

The power dissipation during the inactive (standby) mode can be significantly reduced compared to traditional power gating methods by utilizing new circuit techniques and emerging *sub-60mV/decade* devices. Our group recently proposed a new ultra-low-power device named Silicon on Ferroelectric-Insulator FET (SOFFET) [69], [70], which is capable of providing a subthreshold swing below the fundamental thermodynamic limits (*60mV/decade*) of the conventional MOSFET. In the proposed device, the substrate biasing can suppress standby leakage at sleep mode. Typically, the threshold voltage reduction increases the off-state current. Therefore, the power at off-state increases and become a dominant issue in low power designs. SOFFET can achieve a high-speed operation with low power requirements. The design is applicable for both critical and non-critical circuitry to reduce the power. The SOFFET structure offers better switching performance due to the inherent reduced short channel effect and low subthreshold swing. SOFFET operates with lower supply voltage and its threshold voltage is less sensitive to gate length that makes it suitable for low standby power (*LSTP*) applications. SOFFET also provides higher I_{on} and

lower I_{off}. Its subthreshold swing is below *60mV/decade,* and its short-channel-effects (SCEs) and leakage levels are significantly lower than those of the conventional MOSFET.

In recent years, multi-threshold CMOS (MTCMOS) has emerged as an effective technique for reducing subthreshold current in standby mode while maintaining circuit performance. MTCMOS technology essentially places a sleep transistor on gates and puts them in sleep mode when the circuit is non-operational [71]. As an alternative design approach for the subthreshold region, this work presents a power gating technique using sleep transistor design based on the newly introduced SOFFET. This device is a form of silicon on insulator (SOI) with the buried oxide (BOX) replaced by a ferroelectric insulator and a layer of thin film buffer insulator. The ferroelectric layer allows a negative capacitance (NC) to form. The NC effect provides an internal signal boost and lowers subthreshold swing [69]. For various high density integrated circuit designs, SOFFET is showing an alternative choice to bulk silicon technology due to its performance and many other advantages including yield and power consumption. The ability to control the threshold voltage (see Figure 7.4 and equation (7.1)) via bias voltage at the back gate makes SOFFET devices more flexible for sleep transistor design than bulk MOSFET. This option of SOFFET to provide $multi - V_T$ operation through back gate control would be a very effective way to manage power dissipation.

7.2 CMOS Sleep Transistor Techniques and Limitations

In the recent year, there has been a surge of interest to design circuits to be operated in the subthreshold region of the conventional MOSFET to secure ultra-low-power operation. Subthreshold circuits sleep transistor designs based on the conventional

approaches and MOSFETs will not be appropriate, since the headroom of subthreshold operation is limited to few mV. The sleep transistors with *high-V_t* causes a voltage drop (see Figure 7.1) that can make the virtual V_{dd} not be sufficient enough to keep the *low-V_t* logic gates in on-state/saturate in the subthreshold circuits. The designs in [71] and [72] are suitable for circuits that operate above the threshold region. The proposed SOFFET based sleep transistor design would provide a significant reduction of the subthreshold leakage in all types of circuits including ULP circuits that utilize subthreshold logic. The proposed design would also reduce the number of transistors (which reduces the area) to be used in the power gating technique and address the voltage drop issue. This is achieved by incorporating the options of *low-V_t* and *high-V_t* within a SOFFET by controlling it via the back gate.

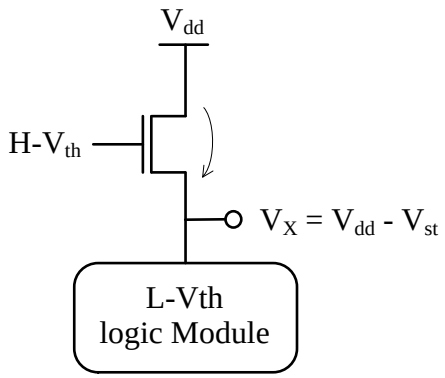

Figure 7.1: Sleep transistor showing voltage drop across high V_t

A chip is composed of blocks, such as ALU, control units, and other functional units. In conventional CMOS sleep transistor design, sleep transistors are placed between the supplies and the circuit blocks to provide an option to cut off the circuit blocks from the supply if needed [73]. These sleep transistors are controlled by a signal generated by a back gate controller (BCR) or distributed control logics. As stated by [73], centralized sleep

transistor design suffers from large interconnect resistances between distant blocks. Such resistance has to be compensated by extra-large sleep transistor that consumes huge area. In terms of the number of transistors, SOFFET based sleep transistor design completely eliminates the standalone sleep transistors by 100% with sleep transistor area reduction compared to the cell-based, distributed, or cluster-based designs. Both distributed and cluster-based designs require wiring to the controller as it is the case for the SOFFET based sleep transistor. The wire routing remains the same.

In conventional CMOS sleep transistor design as shown in Chapter 6, Figure 6.1, the placement of additional transistors between the functional block and the power supply results in a delay penalty. In the absence of a sleep transistor, the propagation delay τ_{pd} is related to the supply voltage and the threshold voltage by the Alpha Power law as depicted in Chapter 6 by (6.1) [74], [75]. When the sleep transistor is present a source-drain voltage (V_{sd}) drop occurs causing the propagation delay to increase as shown by equation (6.2) in Chapter 6 [73]. The performance loss (PL) via propagation delay is defined by [76] and depicted by equation (6.3) in Chapter 6. Since the proposed SOFFET based sleep transistor design is embedded with the logic functions, the propagation loss, as well as the area penalty imposed by the CMOS sleep transistors is eliminated.

7.3 SOFFET Based Sleep Transistor Design

The structure of the new device is similar to silicon-on-insulator (SOI) device. It was proposed to replace the buried silicon dioxide (SiO_2) insulator layer in an SOI device with a layer of ferroelectric insulator and a layer of thin film buffer insulator. The device formally named *Silicon-on-Ferroelectric Insulator (SOF)* FET. The proposed SOFFET can

have two variants – fully depleted and partially depleted SOF. Figure 7.2 presents the concept and the physical structure of proposed fully depleted double-gate SOFFET. The device is used to increase the efficiency of subthreshold operation by lowering the subthreshold swing (*S*) without changing the device structure and conventional fabrication process while taking the advantage of the negative capacitance effect.

Ferroelectric materials display hysteresis behavior, which can be utilized to generate a negative capacitance (NC) effect inside a transistor. This NC effect can be exploited to overcome some fundamental technological limitations encountered by the existing and emerging device technologies [77], [78], and [79]. In this structure, we are taking advantage of ferroelectricity decencies as a pre-existing boost for the device. The trapped charges in a ferroelectric film can be collected after the application of a smaller gate voltage, the channel in between the drain and the source can be developed at lower gate voltage and substrate biasing. Placing a thin ferroelectric film layer on top of silicon substrate will develop a negative capacitance inside the body of the device. This scheme shows a promising and extremely attractive characteristics. The highly-doped Si-substrate acts as a back gate. The ferro-material is the body insulator that the device is built on rather than buried-oxide in traditional SOI devices.

To avoid interfacial reaction between silicon (active area of the device) and the ferroelectric film, an additional layer has to be inserted. This layer improves the electrical operation of the device by eliminating the structural changes at the silicon-ferroelectric interface. The effect of charge between silicon and ferroelectric film can be minimized by inserting a buffer insulator layer. This insulating material is required to hold a high

dielectric constant, high thermal stability, low leakage current, and good interface property with silicon substrates [69], [80]. Integration of a ferroelectric negative capacitance in Si-bulk shrinks the depletion layer. In addition, the thinner ferroelectric film gives higher negative capacitance, leading to higher trapped charges in the film. This helps the creation of the channel at a lower V_T. Moreover, the negative capacitance effect provides internal signal boost and lower subthreshold swing [70].

The operation mode of the proposed structure is similar the traditional MOSFET with a significant enhancement in channel conduction. A gate voltage V_{gs} (n-type for $V_{gs} < V_{th}$) start attracting charges under the oxide layer where the ferro-capacitance impulse the charges upward to accelerate the channel conduction. Since the voltage developed at the ferroelectric capacitance provides a boost during the channel formation, the device behaves as a double-gated structure. Similarly, as the gate voltage decreases, the surface potential at the channel declines freeing charges to the ferro-capacitance. Additional, analysis regarding SOFFET is given by [69] and [81].

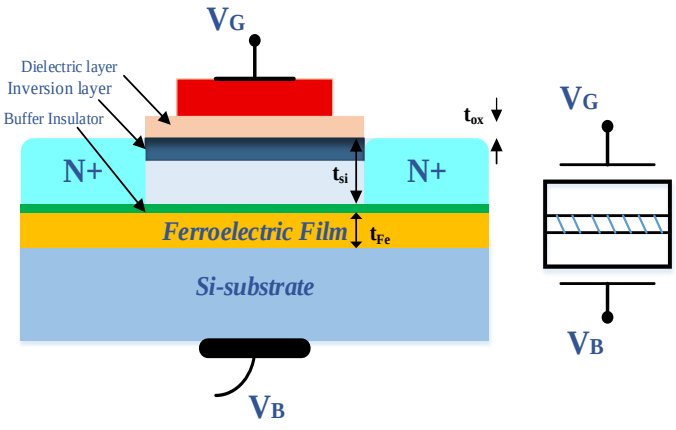

Figure 7.2: 2D structure model of Double Gate SOFFET

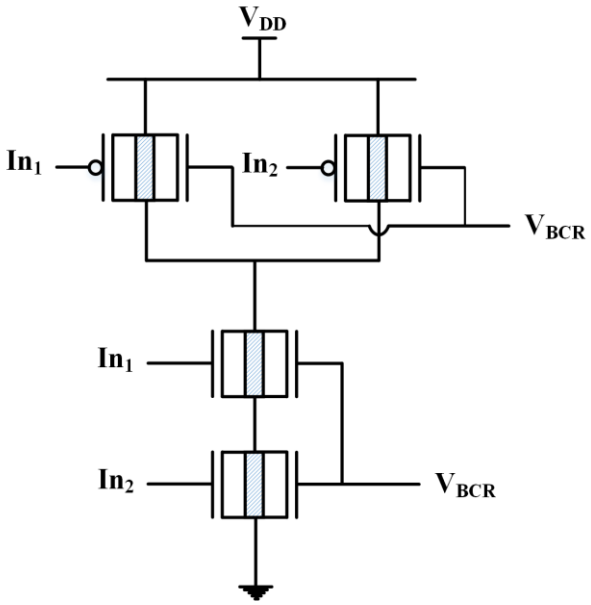

Figure 7.3: Proposed sleep transistor schematic

We have developed single and multi-gate devices based on fully depleted FD-SOFFET for new IC designs. Figure 7.2 depicts the basic device model of a *double-gate* SOFFET. As the name indicates, it consists of two gates that control charges in the channel of the device (thin silicon layer on top of the ferroelectric layer), the top poly-silicon is the traditional gate, with the substrate biasing, it operates as the bottom plate of ferro-capacitance integrated into the device. The fundamental idea here is to add a ferroelectric layer beneath the thin film insulator. Additionally, by replacing the substrate with a back-gate, the device becomes a dual-gated device. As depicted in Figure 7.2, the body region of the SOFFET is floating as opposed to bulk MOSFET, which has the body inherently connected to the substrate. The double gate SOFFET device is a four terminal device defined by the front gate, drain, source, and back-gate. A two input NAND gate schematic is given by Figure 7.3 depicting the proposed dynamic threshold control. The V_t and the

performance of the circuit can be controlled via the back gate. The back gate is routed to BCR to control the behavior of the circuit.

Fully depleted (FD) and partially depleted (PD) SOFFET have been developed in [69], [81]. This work will only focus on the use of FD-SOFFET device for sleep transistor design. The FD design is unique because both of the front-gate and back-gate have control of the charges in the silicon film. In the strongly PD device, the back-gate or substrate has no influence on the front surface potential. For strongly FD device, the silicon film thickness is usually less than or equal to half of the depletion width of the bulk device [82]. Electrical parameters including the threshold voltage and the drain current of the device are influenced by the film thickness. Since the fully depleted SOFFET is like a regular FDSOI device, the threshold voltage is sensitive to the variations in silicon film thickness (T_{si}) [83]. Therefore, thin films are required to ensure a better control over the performance of the device. In addition, the thinner film thickness is required for the minimization of short channel effects and elimination of the current kinks [84]. The surface potentials at the front and back interfaces are strongly coupled to each other and capacitively coupled to the front gate and the substrate through the front gate oxide [82] and buried ferroelectric insulator, respectively. The threshold voltage showing the properties given above is expressed by equation (7.1) and (7.2).

$$V_t^f = V_{FB}^f + 2\Phi_B - \frac{Q_b}{2C_{Ox}} - \left(V_{BG} - V_{FB}^b - 2\Phi_B + \frac{Q_b}{2C_{Fe}}\right) \cdot \eta \tag{7.1}$$

$$Q_b = -qN_A T_{si}\ or + qN_D T_{si} \tag{7.2}$$

where V_t^f and V_{BG} are the front threshold and back-gate voltages, V_{FB}^f and V_{FB}^b are the front gate and back gate flat-band voltages, C_{ox} and C_{Fe}, are front and back-gate oxide and ferroelectric capacitances. Q_b is the area charge density in the depleted silicon film [84], η the body factor of the SOFFET, $\psi_b = \frac{KT}{q} ln(N_{Si}/n_i)$ is the difference between Fermi and intrinsic levels. The subthreshold swing *S* is given by equation (7.3), where C_{Si} is depleted silicon-film capacitance and C_{Body} is the body capacitance. To understand the behavior and performance of the proposed SOFFET, the (*I-V*) characteristics of the device in the subthreshold regime was investigated [69], [81]. The current is defined by equation (7.4).

$$S = 2.3\frac{\mathrm{kT}}{\mathrm{q}}\left(1 + \frac{C_{Body}}{C_{ox}}\right) = 2.3\frac{\mathrm{kT}}{\mathrm{q}}\left(1 - \frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si} - |C_{Fe}|)}\right) \tag{7.3}$$

$$I_{Sub} = 2\mu\mathrm{C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}\left(\frac{\mathrm{KT}}{\mathrm{q}}\right)^2 |\eta - 1|\exp\left(\frac{\mathrm{V_{GS}} - \mathrm{V_{Tf}}}{\eta\mathrm{KT/q}}\right)\left[1 - \exp\left(-\frac{\mathrm{V_{DS}}}{\mathrm{KT/q}}\right)\right] \tag{7.4}$$

Variable-threshold-voltage (VTV) is an effective technique to reduce the leakage current in the standby mode. In the conventional sleep transistor techniques, *low-V_T* logic devices are used in the active mode and *high-V_T* sleep transistors are used in the standby mode. In our proposed design we are utilizing the same SOFFET transistor for both purposes. The logic devices operate at low voltage (due to a low V_{DD}) and at high switching speed (due to a *low-V_T*). The substrate bias control circuit generates a low substrate voltage in the standby mode to increase the threshold voltage. In active mode, the substrate bias control circuit generates a high back-gate voltage, which allows the SOFFET to decrease its threshold voltage. Figure 7.4 shows the threshold response as a result of back gate

voltage variation. The back gate voltage varies between 0 to 0.5 V. As the back potential increased, the threshold of the device is reduced. At high substrate biasing, the logic blocks will be able to turn on faster. At lower biasing voltage, the device will have a high threshold voltage and function as a sleep transistor.

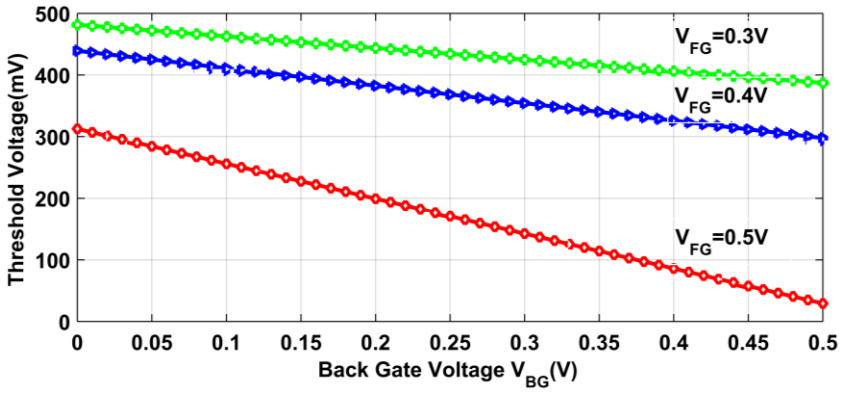

Figure 7.4: Simulation result showing the back gate controlling threshold voltage. $L = 22nm, W = 60nm, t_{si} = 20nm, t_{ox} = 1nm, \varepsilon_{Fe} = 100,\ N_{sub} = 1 \times 10^{17} cm^{-3}$, and $N_{Si} = 1 \times 10^{17} cm^{-3}$

If the gate voltage is below the threshold voltage (Figure 7.5), the transistor is turned off and ideally there is no current from the drain to the source of the transistor. However, there is a current even for gate biases below the threshold, which is known as the subthreshold leakage current. This current is small and varies exponentially with the gate and substrate bias voltages. As depicted in Figure 7.2, the device can be viewed as two MOSFETs (front and back MOSFETs) that shares the same body, drain, and source regions [85]. As shown by Figure 7.5, each MOSFET is controlled by its own gate (V_{DS} varied from 0.2 to 0.5 V). The Figure also shows that the substrate biasing controls the on-state current (I_{on}). In addition, the drain current curves (I_D) are shown for a 30-nm ferroelectric film thick SOFFET. Therefore, the SOFFET is expected to derive a high on-current at higher biasing substrate.

7.4 Leakage Current and Power Dissipation

For high yield transistor on a single chip, the size of the devices has been scaled down. The supply voltage was also reduced to subthreshold operation region to meet with the scaling of the transistor. To maintain the driving strength of the transistors, the threshold voltage was also decreased accordingly. As the supply voltage reduces, the leakage current become more prominent, especially in the subthreshold region. The subthreshold drain current or subthreshold leakage is the current between the source and drain of a MOSFET when the transistor is in subthreshold region (or at$V_{gs} < V_t$). The transistor is confined at this region when the voltage at the gate-to-source node is below the threshold voltage. Reducing the V_t increases the subthreshold leakage current (exponentially). In addition, reducing V_t decreases gate delay (lower propagation delay) which increases performance. The use of high V_t on the other hand will help control leakage but reduces the I_{on} current and increase the gate delay. In a given design, there are two ways to minimize I_{off}. The first option is to select a transistor with large *Vt* and the other option is to choose a transistor with lower the subthreshold swing (*S*). SOFFET provides lower subthreshold swing (*sub-60mV/decade*) [70] and it can even be further improved by reducing η (good for drain induced barrier lowering, DIBL, reduction) via thin films (T_{si}) design. Also, *low-Vt* and *high-Vt* can be achieved by changing the bias voltage at the back gate. That means SOFFET provide much better design flexibility and performance superiority when compared to bulk CMOS based sleep transistor techniques.

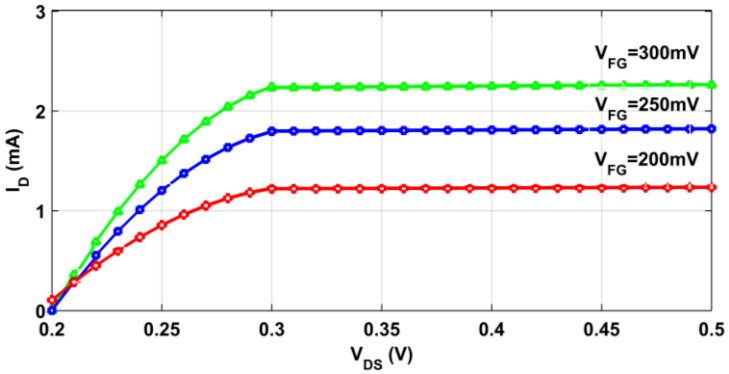

Figure 7.5: Simulation result depicting the drain current of both back and front gates with respect to the drain voltage. $L = 22nm, W = 60nm, t_{si} = 20nm, t_{ox} = 1nm,\ \varepsilon_{Fe} = 100, \theta = 10^{-2}V^{-1}, N_{sub} = 1 \times 10^{17}cm^{-3}$, and $N_{Si} = 1 \times 10^{17}cm^{-3}$

$$P = C_L V_{DD}^2 f + I_{leak} V_{DD} \tag{7.5}$$

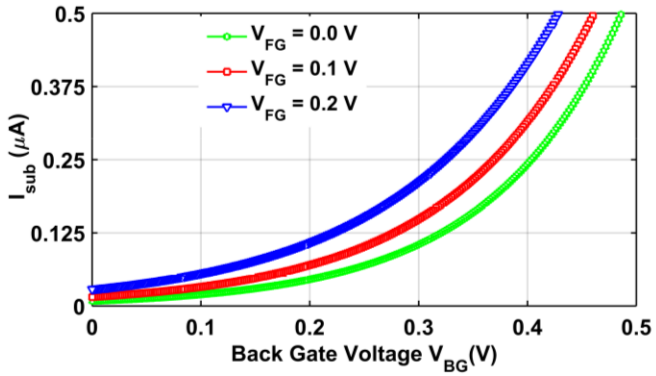

Figure 7.6: Leakage current of the SOFFET versus substrate biasing at different threshold voltage. $L = 22nm, W = 60nm, t_{si} = 20nm, t_{ox} = 1nm, \varepsilon_{Fe} = 100,\ N_{sub} = 1 \times 10^{17}cm^{-3}$, and $N_{Si} = 1 \times 10^{17}cm^{-3}$

The SOFFET subthreshold leakage current when $V_{gs} < V_t$ with the back gate bias voltage is given by equation (6.7) – (6.9) in Chapter 6. The overall power consumption can be expressed using equation (7.5) (not including short circuit power). The first term (dynamic power) is determined by the load capacitance (C_L), the operating frequency, and the supply voltage. Since it is quadratically dependent on the operating voltage, reducing this value will enormously lower the power consumption. The subthreshold voltage supply

is limited to few mV. Even though the capacitance effect becomes prominent with the scaling of the transistors, the dynamic power consumption is much lower in this region. Reducing the threshold voltage will increase subthreshold leakage current. The second term (static power) represents the power consumption resulted from leakage current I_{leak}. This leakage current is relatively high in the idle mode. The leakage is more prominent, especially in the subthreshold region ICs. To mitigate this problem, our approach utilizes a dynamically controlled *multi-*V_t SOFFET to increase the V_t value during the standby or sleep mode. Since SOFFET provide minimum I_{off} and high I_{on} current, it inherently provides lower leakage current in the idle mode. In addition, the V_t is set to a higher value to reduce the leakage even farther. Therefore, the overall power consumption is reduced. In the active operating state (on state) of the transistor the same leakage current also exists. However, this standby component is only a few percent of the dynamic component representing the power consumed for continuous signal processing, it is negligible in the active state [72].

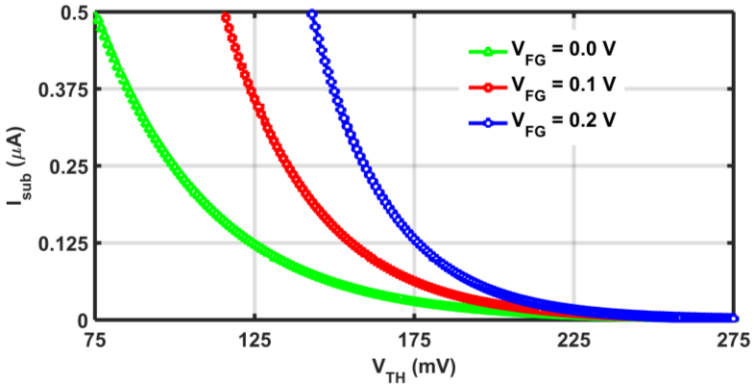

Figure 7.7: Leakage current of the SOFFET for deferent threshold design at various substrate biasing. $L = 22nm, W = 60nm, t_{si} = 20nm, t_{ox} = 1nm,\ \varepsilon_{Fe} = 100,\ N_{sub} = 1 \times 10^{17} cm^{-3}$, and $N_{Si} = 1 \times 10^{17} cm^{-3}$

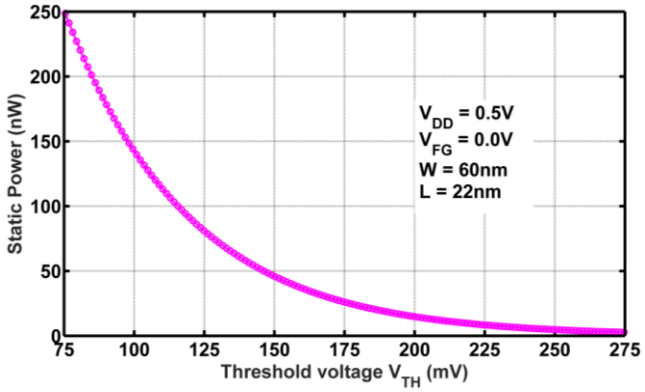

Figure 7.8: Simulation result showing threshold voltage vs static power for a single SOFFET

Figure 7.6 shows the I_{leak} characteristic of the $22nm$ SOFFET device with different offset substrate biasing voltage. As shown in Figure 7.6, the back gate voltage is varied from 0.15 to 0.5 V. With the increase of the back-gate voltage, the threshold voltage decreases (see Figure 7.4) leading to increased leakage current. The maximum leakage current is observed to be around $0.5\ \mu A$. Figure 7.6 also indicates that the back-gate potential enhanced surface potential of the channel region, hence, the conduction speed that results in a threshold voltage shift. At a lower substrate-biasing, the device functions as planar MOSFET with an extended threshold. As the back-gate biasing increases, the surface potential of the channel also increases, leading to higher speed and device conductivity that improve the on-state driving current I_{on}. Consequently, resulting in a significant reduction of power consumption in both standby and active modes. Also, the correlation between the threshold voltage and leakage current is shown in Figure 7.7. As the threshold voltage is raised the leakage current is reduced. These results demonstrate the controllability is enhanced due to the assistance of the back-gate biasing. As a result, a lower leakage current in the OFF state and higher driving current in the ON state can be

provided by the SOFFET devices by using different biasing, thereby effectively reducing the power dissipation and increasing the performance of the circuit.

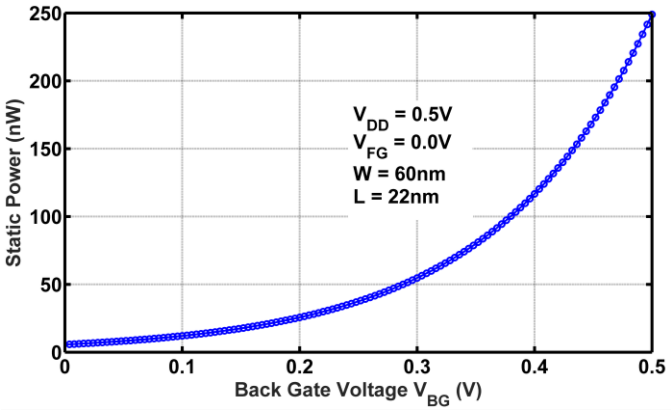

Figure 7.9: Simulation result showing back gate voltage vs static power for a single SOFFET

Figure 7.8 and Figure 7.9 illustrates the change in the static power as a result of the leakage current generated by varying the threshold voltage via the back-gate. Both simulations are performed for a single SOFFET with $W = 60nm$ and $L = 22nm$. Expanding on the back-gate biasing technique for a single transistor, a circuit block with 200K SOFFETs is considered at the macro scale. A simulation environment with the equivalent capacitance model for the circuit block is formed to simulate the benefits of back-gate biasing with respect to power consumption. The back-gate biasing allows the dynamic settings of the threshold voltage based on specific circuit block activity. This attribute enables the circuit block to regulate power consumption locally. In Figure 7.10, a circuit block with 200K SOFFETs is considered and the simulation is performed with the BCR setting the threshold voltage to low-V_T (red), intermediate-V_T (blue), and high-V_T (green). The contribution of both dynamic and static power consumption is depicted in the Figure. In this simulation, the f is varied between 100 MHz to 10 GHz. The leakage

contribution of the devices at various V_T is performed and as shown the higher power consumption is presented at low-V_T transistors.

The BCR is forced to turn off (setting part of the circuit to high-Vt) part of the circuit block to remain under 40 mW power envelop. The Figure 7.11 shows how the contribution of static power affects the overall power consumption. As depicted by Figure 7.11, the static power increased as part of the circuit changes to idle mode. The static power increased as the circuit block experience an increase in leakage current by 10 and 18 percent. Which means, the static power increased from 15 (red), to 25 (blue) and 33 percent (green). For most ICs, static power accounts for about 15% of the total power. Leakage power consumption has become a major bottleneck for the continuous scaling of CMOS technologies. It has been reported that the leakage power accounts for as much as 42% of the total power in a high-end microprocessor in 65 nm technology [11], [12]. In Figure 7.11, both contributions from active and passive power is depicted. It shows that the active power reduced by 25 and 50 percent as static power takes over and contribute to the power consumption. As shown, the circuit block consumes less power at 100 MHz than when it operates at 10 GHz. In addition, higher switching frequency will directly increase the temperature of the circuit block, causing thermal spike which in turns exponentially affect the static contribution to become even higher. In both Figure 7.10 and Figure 7.11, total power consumption is reduced by sleep mode operation via BCR settings to high-V_T transistors.

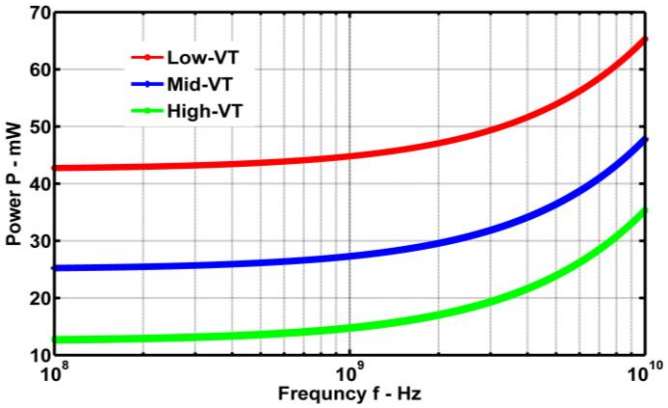

Figure 7.10: Change in power consumption of a circuit block with 200K SOFFETs in GHz switching frequency via Low-V_T, Mid-V_T, and High-V_T

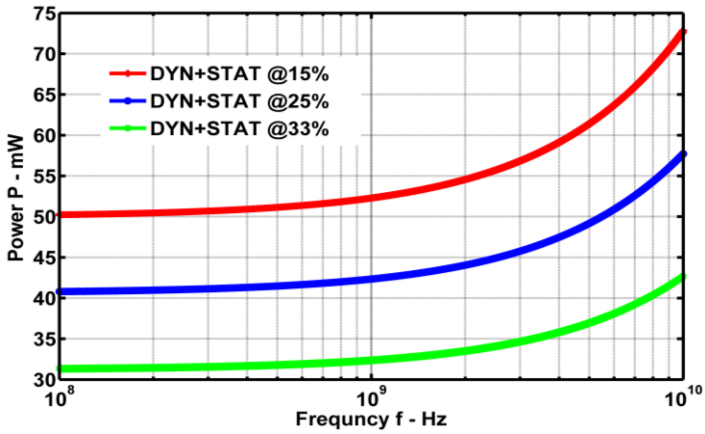

Figure 7.11: Change in both dynamic and static power consumption with sleep mode transistor contributing to static power loss

7.5 Summary

SOFFET devices have shown tremendous design flexibility for next-generation subthreshold IC designs. In this work, we have presented a design approach to mitigate power loss using double gate SOFFET transistors. The approach used here implements a sleep transistor design and control the characteristics via the back gate. This method simplifies the design complexity, reduces the chip area, and improve power dissipation. SOFFET provides a strong threshold voltage control, lower supply voltage, sub-*60mV/decade* operation, higher current drive, and better short-channel characteristics.

These are the main advantages of using SOFFET for sleep transistors and other high speed IC applications. Especially in the subthreshold region, where headroom is limited to few mV, the presented technique with SOFFET addresses the voltage drop problem of current designs. The key to this approach is the fact that it incorporates the sleep transistor design as part of the circuit design by avoiding the standalone complex design technique. At the same time, it provides a dynamically controlled V_t for times the circuit needs to be in sleep or switching mode, which makes it far better for subthreshold region design. The approach provided in this work try to address the overall power consumption while reducing the static contribution without additional area penalty.

CHAPTER 8

CONCLUSION

To conclude the dissertation and summarize the contributions of the work:

Three on-chip voltage regulator designs:

- The first design is a fully integrated on-chip switching voltage regulator. This regulator is indutorless design and utilizes a cascaded MFB loop filters with an error correction amplifier. The voltage regulator is controlled by specifying the reference voltage and by varying the pulse width via PWM signal. The regulator can generate an adjustable output voltage between 0.5 V to 1.5 V and 100 µA to 150 mA output current. The output voltage can be adjusted dynamically and the output current can be changed based on the load requirement.
- The second design is a hybrid LDO voltage regulator. This regulator has multiple feedback loops for error correction and can achieve a PSR of -62 dB until 10 MHz. The regulator can generate an adjustable output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current. Also, the regulator can be used as standalone design to supply different output voltages or in synergy with a switching regulator to suppress and lower the output voltage ripple.
- The third design is a fully on-chip power management system. This design provide three different unique architectures depending on the specified application. The PMS can generate adjustable switching output voltage between 0.5 V to 1.5 V/1.6 V and 100 µA to 150 mA output current, or/and adjustable linear output voltage between 0.5 V to 1.2 V and 100 µA to 120 mA output current at the second stage.

Due to the low output ripple, the design can be used as standalone regulator to drive a load with low noise requirement.

Two sleep transistor designs:

- The first sleep transistor design is based on conventional above threshold transistor design. This design is implemented using FDSOI. The FDSOI provides a double gate structure, which allows the modulation of the threshold voltage via the back gate. The back bias is used to change the threshold setting between *low-Vt* and *high-Vt*. This enables the design of sleep transistor to be incorporated as part of the logic block.
- The second sleep transistor design is a subthreshold sleep transistor design. The presented architecture utilizes SOFFET device. SOFET provides steep subthreshold swing and high *Ion*/*Ioff* ratio. The design solution obviates the standalone sleep transistor switch, which reduces area, improves speed, avoid voltage drop by the sleep transistor and simplifies the design complexity.

APPENDIX I

The appendix section contains detail layout and pin arrangement of the fabricated chip

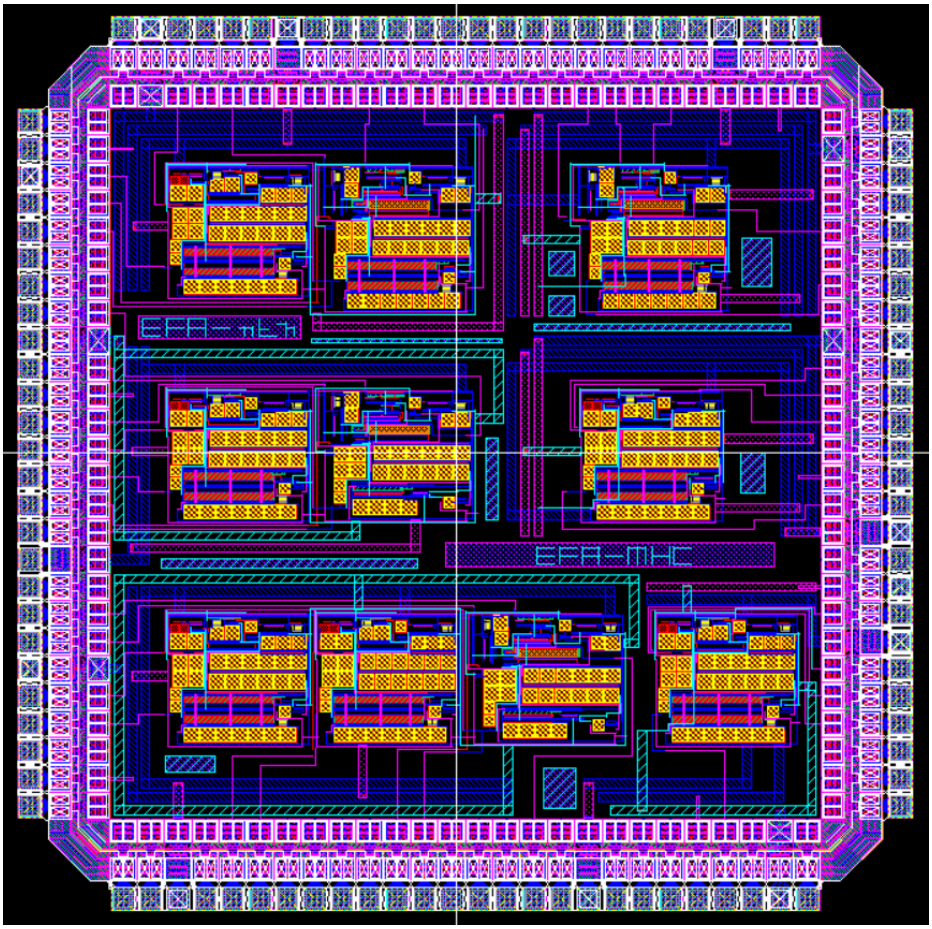

Figure 8.1: Layout of the fabricated chip containing HLDR, SVR, and all three PMS designs

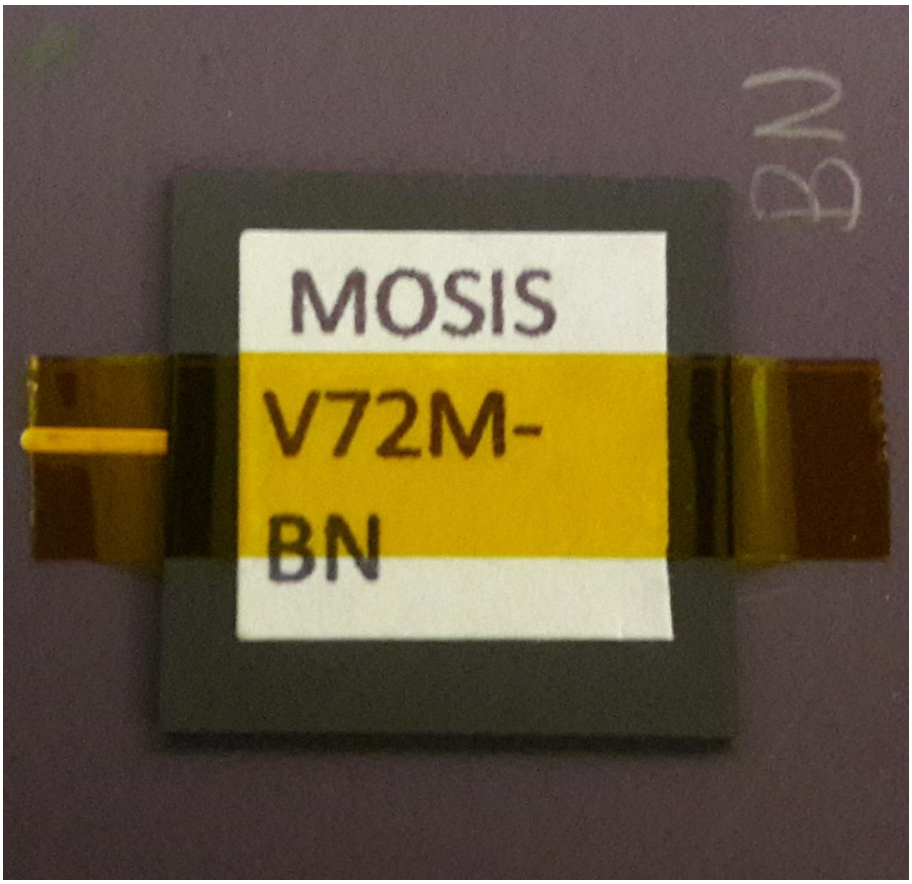

Figure 8.2: Picture of the fabricated chip containing HLDR, SVR, and all three PMS designs

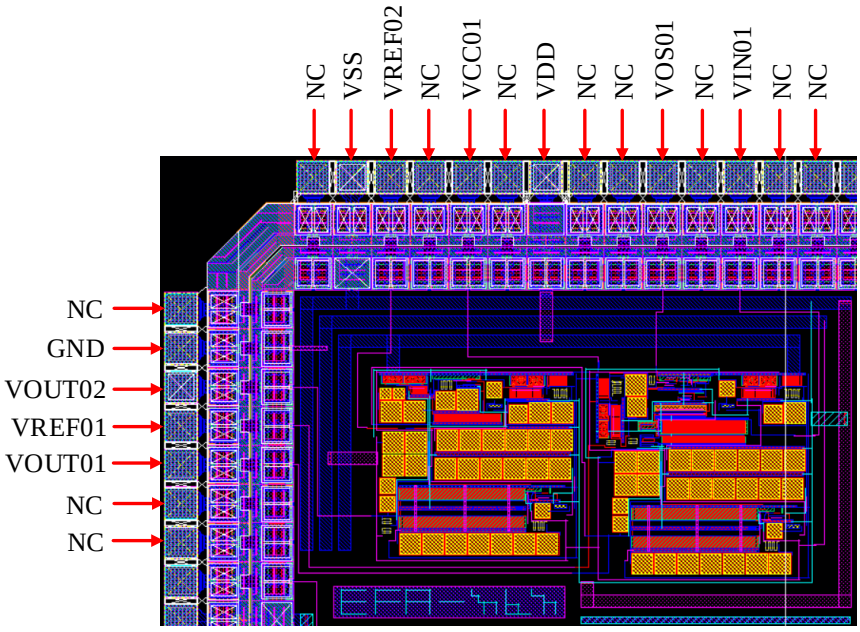

Figure 8.3: On-Chip SIS-SOS-SLOS chip layout

Table 8.1: Pin arrangement for on-chip SIS-SOS-SLOS depicted on Figure 8.3

Pin #	Package Pin #	Pin Name	Note
1	M12	Not connected	Not connected
2	L11	GND	GND
3	L12	VOUT02	HLDR output stage
4	K11	VREF01	Reference voltage for SVR
5	K12	VOUT01	SVR output stage
6	J10	Not connected	Not connected
7	J11	Not connected	Not connected
94	L6	Not connected	Not connected
95	M6	Not connected	Not connected

Table 8.1: Pin arrangement for on-chip SIS-SOS-SLOS depicted on Figure 8.3 (cont…)

Pin #	Package Pin #	Pin Name	Note
96	K7	VIN01	Input dc voltage
97	L7	Not connected	Not connected
98	M7	VOS01	Triangular signal input
99	K8	Not connected	Not connected
100	L8	Not connected	Not connected
101	M8	VDD	VDD
102	K9	Not connected	Not connected
103	L9	VCC	VCC
104	M9	Not connected	Not connected
105	K10	VREF02	Reference voltage for HLDR
106	L10	VSS	VSS
107	M10	Not connected	Not connected
108	M11	No pin	Not part of the pin layout

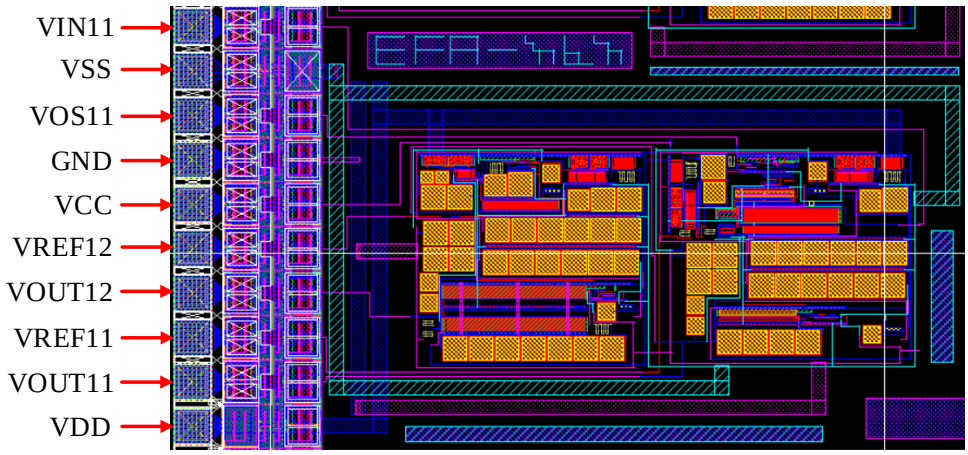

Figure 8.4: On-Chip SIS-SLOS chip layout

Table 8.2: Pin arrangement for on-chip SIS-SLOS depicted on Figure 8.4

Pin #	**Package Pin #**	**Pin Name**	**Note**
8	J12	VIN11	Input dc voltage
9	H10	VSS	VSS
10	H11	VOS11	Triangular signal input
11	H12	GND	GND
12	G10	VCC	VCC
1	G11	VREF12	Reference voltage for SVR
14	G12	VOUT12	SVR output stage
15	F10	VREF11	Reference voltage for HLDR
16	F11	VOUT11	HLDR output stage
17	F12	VDD	VDD

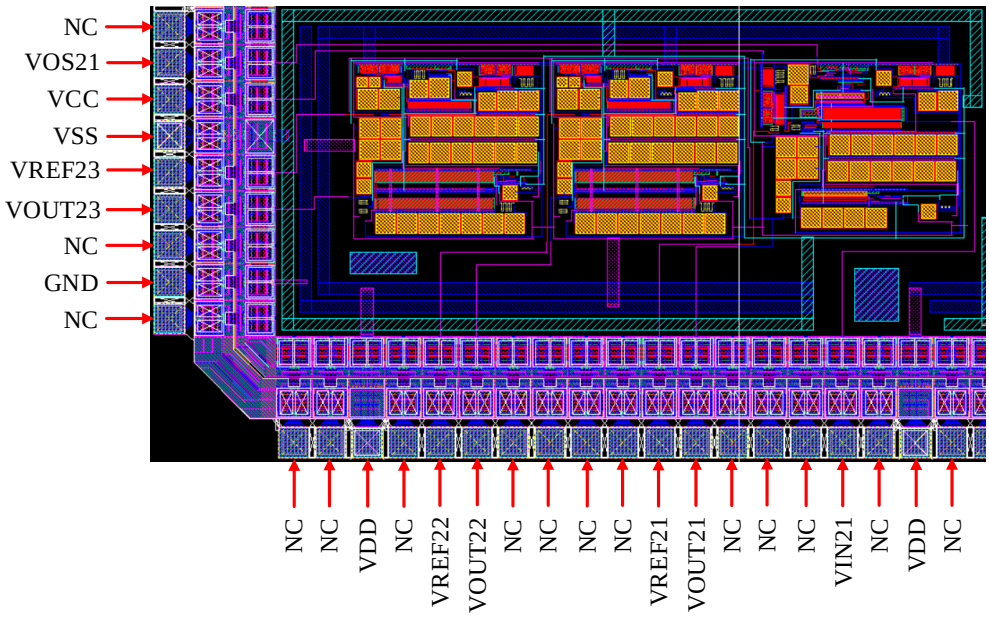

Figure 8.5: On-Chip SIS-DLOS chip layout

Table 8.3: Pin arrangement for on-chip SIS-DLOS depicted on Figure 8.5

Pin #	Package Pin #	Pin Name	Note
18	E10	Not connected	Not connected
19	E11	VOS21	Triangular signal input
20	E12	VCC	VCC
21	D10	VSS	VSS
22	D11	VREF23	Reference voltage for HLDR2
23	D12	VOUT23	HLDR2 output stage
24	C10	Not connected	Not connected
25	C11	GND	GND
26	C12	Not connected	Not connected
27	B12	No pin	Not part of the pin layout

Table 8.3: Pin arrangement for on-chip SIS-DLOS depicted on Figure 8.5 (cont…)

Pin #	Package Pin #	Pin Name	Note
28	A12	Not connected	Not connected
29	B11	Not connected	Not connected
30	A11	VDD	VDD
31	B10	Not connected	Not connected
32	A10	VREF22	Reference voltage for HLDR1
33	C9	VOUT22	HLDR1 output stage
34	B9	Not connected	Not connected
35	A9	Not connected	Not connected
36	C8	Not connected	Not connected
37	B8	Not connected	Not connected
38	A8	VREF21	Reference voltage for SVR
39	C7	VOUT21	SVR output stage
40	B7	Not connected	Not connected
41	A7	Not connected	Not connected
42	C6	Not connected	Not connected
43	B6	VIN21	Input dc voltage
44	A6	Not connected	Not connected

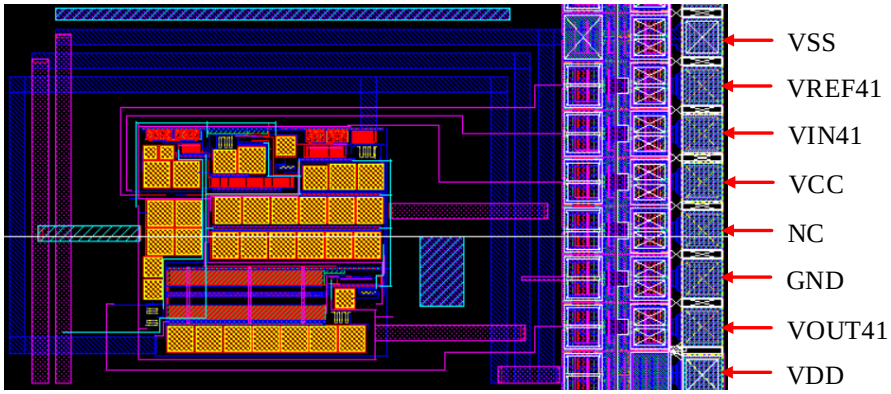

Figure 8.6: On-Chip HLDR chip layout

Table 8.4: Pin arrangement for on-chip HLDR depicted on Figure 8.6

Pin #	Package Pin #	Pin Name	Note
65	E1	VDD	VDD
66	F3	VOUT41	HLDR output stage
67	F2	GND	GND
68	F1	Not connected	Not connected
69	G3	VCC	VCC
70	G2	VIN41	Input dc voltage
71	G1	VREF41	Reference voltage for HLDR
72	H3	VSS	VSS

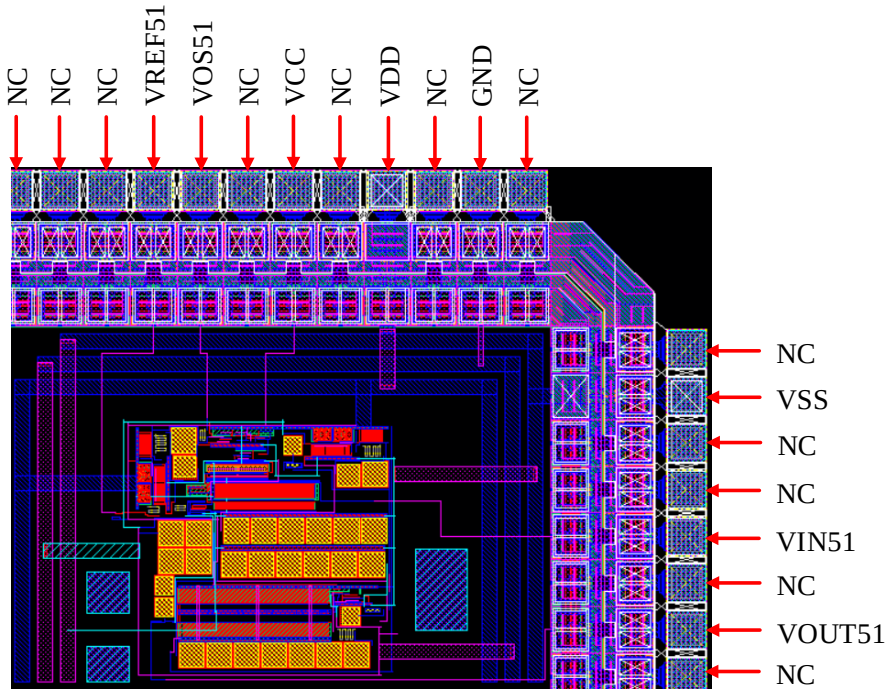

Figure 8.7: On-Chip SVR chip layout

Table 8.5: Pin arrangement for on-chip SVR depicted on Figure 8.7

Pin #	Package Pin #	Pin Name	Note
73	H2	Not connected	Not connected
74	H1	VOUT51	SVR output stage
75	J3	Not connected	Not connected
76	J2	VIN51	Input dc voltage
77	J1	Not connected	Not connected
78	K3	Not connected	Not connected
79	K2	VSS	VSS
80	K1	Not connected	Not connected

Table 8.5: Pin arrangement for on-chip SVR depicted on Figure 8.7 (cont…)

Pin #	Package Pin #	Pin Name	Note
81	L1	No pin	Not part of the pin layout
82	M1	Not connected	Not connected
83	L2	GND	GND
84	M2	Not connected	Not connected
85	L3	VDD	VDD
86	M3	Not connected	Not connected
87	K4	VCC	VCC
88	L4	Not connected	Not connected
89	M4	VOS51	Triangular signal input
90	K5	VREF51	Reference voltage for SVR
91	L5	Not connected	Not connected
92	M5	Not connected	Not connected
93	K6	Not connected	Not connected

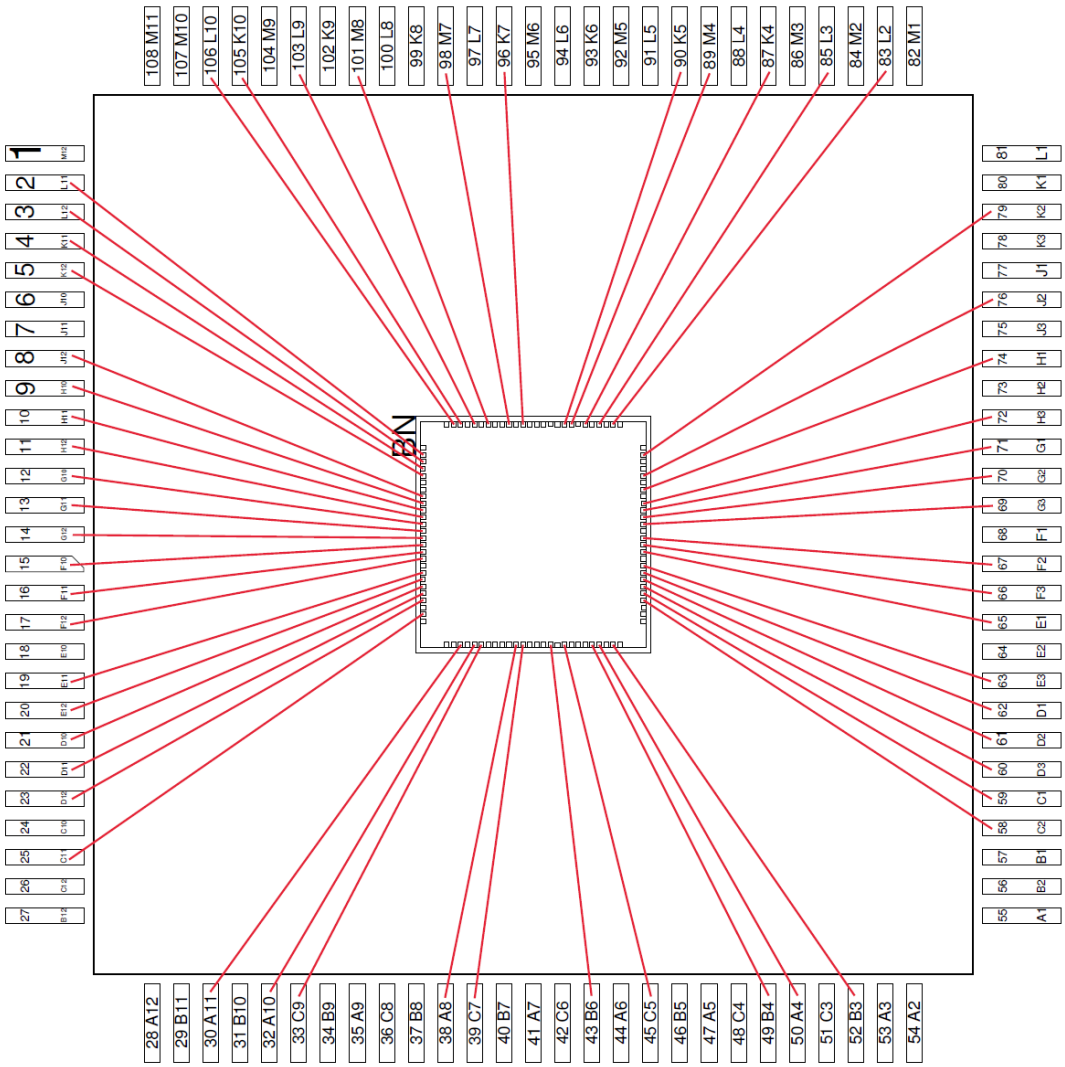

Figure 8.8: Bonding diagram of the complete chip

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