STATIC RANDOM-ACCESS MEMORY DESIGNS BASED ON DIFFERENT FINFETS AT LOWER TECHNOLOGY NODE (7NM)

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By

Athiya Nizam

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Osmania University

Kansas City, Missouri

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Athiya Nizam, Candidate for the Master of Science Degree

University of Missouri - Kansas City, 2019

ABSTRACT

The Static Random-Access Memory (SRAM) has a significant performance impact on current nanoelectronics systems. To improve SRAM efficiency, it is important to utilize emerging technologies to overcome short-channel effects (SCE) of conventional CMOS. FinFET devices are promising emerging devices that can be utilized to improve the performance of SRAM designs at lower technology nodes. In this thesis, I present detail analysis of SRAM cells using different types of FinFET devices at 7nm technology. From the analysis, it can be concluded that the performance of both 6T and 8T SRAM designs are improved. 6T SRAM achieves a 44.97% improvement in the read energy compared to 8T SRAM. However, 6T SRAM write energy degraded by 3.16% compared to 8T SRAM. Read stability and write ability of SRAM cells are determined using Static Noise Margin and N-curve methods. Moreover, Monte Carlo simulations are performed on the SRAM cells to evaluate process variations. Simulations were done in HSPICE using 7nm Asymmetrical Underlap FinFET technology.

The quasiplanar FinFET structure gained considerable attention because of the ease of the fabrication process [1] – [4]. Scaling of technology have degraded the performance of CMOS designs because of the short channel effects (SCEs) [5], [6]. Therefore, there has been upsurge in demand for FinFET devices for emerging market segments including artificial intelligence and cloud computing (AI) [8], [9], Internet of Things (IoT) [10] – [13] and biomedical [17] –

[18] which have their own exclusive style of design. In recent years, many Underlapped FinFET devices were proposed to have better control of the SCEs in the sub-nanometer technologies [3], [4], [19] – [33]. Underlap on either side of the gate increases effective channel length as seen by the charge carriers. Consequently, the source-to-drain tunneling probability is improved. Moreover, edge direct tunneling leakage components can be reduced by controlling the electric field at the gate-drain junction . There is a limitation on the extent of underlap on drain or source sides because the ION is lower for larger underlap. Additionally, FinFET based designs have major width quantization issue. The width of a FinFET device increases only in quanta of silicon fin height (HFIN) [4]. The width quantization issue becomes critical for ratioed designs like SRAMs, where proper sizing of the transistors is essential for fault-free operation. FinFETs based on Design/Technology Co-Optimization (DTCO_F) approach can overcome these issues [38]. DTCO_F follows special design rules, which provides the specifications for the standard SRAM cells with special spacing rules and low leakages. The performances of 6T SRAM designs implemented by different FinFET devices are compared for different pull-up, pull down and pass gate transistor (PU: PD:PG) ratios to identify the best FinFET device for high speed and low power SRAM applications. Underlapped FinFETs (UF) and Design/Technology Co-Optimized FinFETs (DTCO_F) are used for the design and analysis. It is observed that with the PU: PD:PG ratios of 1:1:1 and 1:5:2 for the UF-SRAMs the read energy has degraded by 3.31% and 48.72% compared to the DTCO_F-SRAMs, respectively. However, the read energy with 2:5:2 ratio has improved by 32.71% in the UF-SRAM compared to the DTCO_F-SRAMs. The write energy with 1:1:1 configuration has improved by 642.27% in the UF-SRAM compared to the DTCO_F-SRAM. On the other hand, the write energy with 1:5:2 and 2:5:2 configurations have degraded by

86.26% and 96% in the UF-SRAMs compared to the DTCO_F-SRAMs. The stability and reliability of different SRAMs are also evaluated for 500mV supply. From the analysis, it can be concluded that Asymmetrical Underlapped FinFET is better for high-speed applications and DTCO FinFET for low power applications.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Computing and Engineering have examined a thesis titled "Static Random-Access Memory Designs based on Different FinFETs at Lower Technology node (7nm)" presented by Athiya Nizam, candidate for the Master of Science degree, and certify that in their opinion it is worthy of acceptance.

Supervisory Committee

Masud H Chowdhury Ph.D., Committee Chair

Department of Computer Science Electrical Engineering

Ghulam Chaudhry, Ph.D., Committee member

Department of Computer Science Electrical Engineering

Mahbube Khoda Siddiki, Ph.D., Committee member

Department of Computer Science Electrical Engineering

Ahmed Hassan, Ph.D., Committee member

Department of Computer Science Electrical Engineering

CONTENTS

ABSTRACT……………………………………………………………………………...iii

LIST OF ILLUSTRATIONS viii

LIST OF TABLES x

ACKNOWLEDGEMENTS xi

1 INTRODUCTION 1

1.1 Problem Statement 2

1.2 Goals and Organization of the Thesis 3

2 NEXT GENERATION HIGH PERFORMANCE DEVICE: FINFET 4

2.1 Introduction 4

2.2 FinFET Device 5

2.3 Characteristics of FinFET Devices..6

2.4 Conclusion...9

3 FINFET BASED SRAM BITCELL DESIGNS 10

3.1 Introduction 10

3.2 6T AUF SRAM 11

3.3 8T AUF SRAM 13

3.4 Hspice Simulation of 6T and 8T SRAMs ……………………………………..14

3.5 Performance and Reliability of 6T and 8T AUF SRAM………………………17

3.6 Conclusion 21

4 BENCHMARKING OF UF-SRAMS AND DTCO-F-SRAMS 22

4.1 Introduction 22

4.2 UF and DTCO_F Devices 23

4.3 UF-SRAMs and DTCO_F SRAMs 26

4.4 Conclusion 31

5 COLLABORATIVE PROJECT 32

5.1 Introduction 32

5.2 Double Gate FDSOI Device 34

5.3 FDSOI based 6T SRAM Bitcell Design 35

5.4 Benchmarking of FDSOI based SRAM Cells 40

5.5 Conclusion....................43

6. INTERNSHIP EXPERIENCE AT INTEL AND MARVELL SEMICONDUCTOR 44

7. CONCLUSION AND FUTURE WORK 47

7.1 Summary of Research Work 47

7.2 Direction of Future Work 49

BIBLIOGRAPHY 50

VITA....................58

LIST OF ILLUSTRATIONS

Figure Page

1. A double gate FinFET Device 6

2. ION of n-type AUF devices with varying DU and SU [46] 8

3. IOFF of n-type AUF devices with varying DU and SU [46]....8

4. AUF device structure having DU=1.635 nm and SU=1.09 nm [8] 8

5. Schematic of 6T AUF SRAM cell [7], [8]....12

6. Schematic of 8T AUF SRAM cell [9], [10], [12] 14

7. Read Characteristics of 6T Asymmetrical Drain underlapped FinFET....14

8. Read Characteristics of 8T Asymmetrical Drain underlapped FinFET....15

9. Write operation of 6T Asymmetrical Drain underlapped FinFET (Q=1, QB=0)....16

10. Write operation of 8T Asymmetrical Drain underlapped FinFET (Q=1, QB=0)....16

11. N-curve analysis of 6T and 8T AUF SRAM cell 17

12. Read energy of 6T and 8T AUF SRAM cell 19

13. Write energy of 6T and 8T AUF SRAM cell 20

14. N-curve analysis of 6T AUF SRAM cell under process variation 20

15. N-curve analysis of 8T AUF SRAM cell under process variation 20

16. (a) I_{ON}; (b I_{OFF}; (c) SS (d) DIBL; (e) I_{ON}-I_{OFF} ratio of different existing n-type FinFET 25

17. RSNM of different configuration UF-SRAMs 27

18. N-curve analysis of different configuration UF-SRAMs....27

19. N-curve analysis of 1:1:1 UF SRAM under process variation....28

20. Read energy of different configurations 6T SRAM bitcell....29

21. Write energy of different configurations 6T SRAM bitcell....29

22. Conventional power gating configuration of SRAM....33

23. FDSOI MOSFET device....35

24. Dependence of threshold voltage upon back gate bias....36

25. Different configuration of double gate FDSOI based SRAM bitcell....37

26. N curve analysis of CI configuration SRAM cell....40

27. Intel Solid State Drive....45

28. Thunder X2 Server Processor....46

LIST OF TABLES

Figure Page

1. Existing P-Type FinFETs Device Characteristics 7

2. Benchmarking of AUF SRAM Designs 18

3. Existing DTCO FinFETs Device Charactersitics…………………………………………...24

4. Benchmarking of 6T UF-SRAM and 6T DTCO_F-SRAM Designs.................................30

5. Performance summary of different FDSOI based SRAM bitcell configuration................37

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CHAPTER 1
INTRODUCTION

In today's world Data center plays a huge role. The security and welfare of people are passed on these data centers which control and store data and information. Day by day, technologies are getting advanced and people are depending more on Data centers as they offer the greater levels of security, flexibility and accessibility to data and information around the world.

A Data center is made up of numerous data servers. A Server processor (CPU) is one of the main components of a Server where all the computations required to complete various tasks assigned to them are performed. Multicore CPUs with dozens of cores is the heart of a server delivering powerful performance and high-speed computation.

In the early days of computing, performance of a CPU was slow as it depends heavily on limited memory. Hence, Cache memory was introduced. The development of caches is one of the most significant events in the history of computing. An SRAM (Static Random-Access Memory) is used to serve as cache memory and applications to provide low power and high speed. It provides a direct interface with the CPU at speeds not attainable by DRAMs. The Static Random-Access Memory (SRAM) has a significant performance impact on current server systems Hence, using high speed and low power cache memory i.e. SRAM (Static Random-Access Memory) inside a CPU provides better performance.

1.1 Problem Statement

Scaling of technology has increased serious challenges like the short channel effects (SCEs) in the bulk CMOS devices. To overcome these issues, FinFET devices are introduced. FinFET offers better gate control, higher ION, better scalability and therefore, improved performance and reliability compared to the conventional CMOS designs. Among the double gate devices, the quasiplanar FinFET structure gained considerable attention because of the ease of the fabrication process [1] – [4].

Nanotechnology is leading world towards many new applications in various fields of computing, medical, defense and energy. Modern world technologies and Data centers CPU heavily rely on memories. Data centers are powered by virtualization technologies that allow multiple resources being shared among a large number of users with diverse time-varying access patterns [7] - [9]. Also, SRAM has a vital role in the modern deep learning applications, which require intensive memory access. To satisfy these requirements, emerging devices are utilized to design memories for better performance and speed. Static Random Access Memory (SRAM) occupies more than 50% of the total die area and imposes the majority of the power consumption [5]-[6]. Therefore, it is necessary to design a power, energy efficient and high speed SRAM cell to improve performance of the system.

In recent years, many Underlapped FinFET devices were proposed to have better control of the SCEs in the sub-nanometer technologies [3], [4], [19] – [33]. Underlap on either side of the gate increases effective channel length as seen by the charge carriers. Consequently, source-to-drain tunneling probability is improved. This overall increases the performance of the device. Hence, Underlapped FinFET based SRAMs have become a capable solution to a

more robust and energy efficient SRAM cell design. Also, Design co-optimized FinFETs are designed to provide low power SRAM cell design. DTCO_F provides a higher ION-IOFF ratio compared to the UF Device.

1.2 Goals and Organization of the Thesis

Taking Underlapped and Design co-optimized FinFET advantages into consideration, I aim to design a Static Random-Access Memory (SRAM) based on these FinFET devices. The proposed memory will satisfy the low power and high efficiency requirement. The rest of the book is arranged as follows. Chapter 2 describes Next Generation High Performance Device - Fin Field Effect Transistor (FinFET). In Chapter 3, Asymmetrical Underlapped FinFET SRAM design is discussed. Chapter 4 talks about the benchmarking of underlapped FinFET (UF) and Design/Technology Co-optimize FinFET (DTCO) based SRAMs. Chapter 5 provides a collaborative project work. Chapter 6 talks about my internship experience at Intel Corporation and Marvell Semiconductor Inc. Finally, Chapter 7 provides a conclusion of this thesis.

CHAPTER 2

NEXT GENERATION HIGH PERFORMANCE DEVICE: FINFET

Scaling down of technology has degraded the performance of CMOS designs because of short channel effects (SCE), DIBL and various other new challenges associated. As we look forward to 7 nm technology and beyond, we must address the challenges associated with scaling down.

FinFET has emerged as a promising device to replace Bulk CMOS due to reduced Short Channel Effects, high ON current, low leakage current and better performance. However, with scaling advantages of FinFETs, there are some challenges like width quantization that needs to be overcome. Hence, Asymmetrical underlapped FinFET is used to overcome such challenges and provide much better performance.

2.1 Introduction

Exponential increase in number of transistors, have increased the density and the total power consumption of the system. Moreover, the scaling of technology has degraded the performance of CMOS designs because of the short channel effects (SCEs). In sub nanometer technologies, FinFET devices have better gate control and therefore, achieves better performance than CMOS designs. In addition to this, FinFET devices possess high ION and better scalability in contrast to bulk CMOS [1] - [3]. The fundamental thermionic limit of 60 mV/decade for the subthreshold swing of the MOSFET devices restricts the supply voltage scaling and achievable ION/IOFF ratio [5]. Among various double gate devices, the

quasiplanar FinFET structure gained huge attention because of the ease in fabrication process [4]. However, FinFET based designs have major width quantization issue. The width of FinFET device increases only in quanta of silicon fin height (HFIN) [4]. Width quantization issue becomes more critical for ratioed designs like SRAMs, where proper sizing of transistors is essential for correct functionality. With process variations this problem is further worse and affect the reliability of SRAM cell.

Hence, FinFET helps to achieve high speed and low power SRAM (Static Random-Access Memory) inside a CPU which provides better performance.

In this Chapter, Section 2.2 talks about FinFET Devices, Section 2.3 provides details about Characteristics of FinFET Devices and Section 2.4 provides conclusion.

2.2 FinFET Device

FinFETs (refer Figure 1) have emerged as the most promising alternatives to MOSFETs. FinFETs have attracted increasing attention over the past decade because of the degrading short-channel effects of MOSFETs [14] - [16]. Two or three gates wrapped around a vertical channel enables easy alignment of gates and compatibility with the standard CMOS fabrication process.

While the planar MOSFET channel is horizontal, the FinFET channel (also known as the fin) is vertical. Hence, the height of the channel (HFIN) determines the width (W) of the FinFET. This leads to a special property of FinFETs known as width quantization. According to this property, FinFET width must be a multiple of HFIN, that is, widths can be increased by using multiple fins. Thus, arbitrary FinFET widths are not possible. Although smaller fin heights offer more flexibility, they lead to multiple fins, which in turn leads to more silicon

area. On the other hand, taller fins lead to less silicon footprint, but may also result in structural instability. Typically, the fin height is determined by the process engineers and is kept below four times the fin thickness [16].

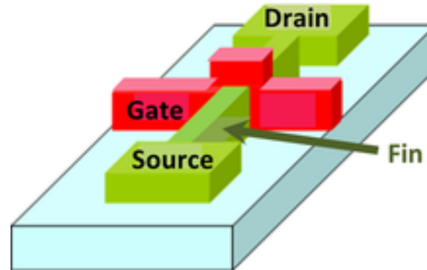

Figure 1: A double gate FinFET device [16]

2.3 Characteristics of FinFET Devices

There are two types of Underlapped FinFET (UF) devices available in the literature - the equal or symmetric underlapped FinFETs (SUF) and the unequal or asymmetric underlapped FinFETs (ASUF), where the unequal underlap on either side of the gate in FinFETs leads to different values of ION based on which ends of the device act as the source and drain terminals. The ASUFs offer better performance compared to the SUFs [20]. Moreover, the ASUFs with long drain side underlapped (DU) achieves improved Drain Induced Barrier Lowering (DIBL) due to the better shielding of the channel potential barrier from the drain field lines by superseding drain underlap [20]. However, characteristics of the ASUFs with SU are worse because of the existence of the edge direct tunneling (EDT) [20]. The n-type ASUF device with SU=1.09 nm and DU= 1.635 nm achieve the maximum I_{ON}-I_{OFF} ratio among the available n-type ASUFs. Table 1 shows the device characteristics of the p-type FinFET devices. For our

analysis, we have selected an n-type ASUF device with DU=1.635 nm and SU=1.09 nm, and a p-type SUF device illustrated in [4] and [20] to implement the design of the UF 6T SRAM.

Underlap on either side of gate increases effective channel length as seen by the charge carriers. Hence, source-to-drain tunneling probability is improved. Moreover, edge direct tunneling leakage components can be reduce by controlling electric field at the gate-drain junction [20]. There is limitation on the extent of underlap on drain or source sides, as ION decreases corresponding to the large underlap [4], [20]. Figure 2 and Figure 3 show ION and IOFF of AUF for different drain underlapped (DU) and source underlapped (SU) devices. AUF device with DU=1.635 nm and SU=1.09 nm (black color) achieves maximum ION/IOFF ratio among different AUF devices (refer Figure 4). Based on high ION/IOFF ratio criteria, we designed optimized SRAM designs using AUF device with DU=1.635 nm and SU=1.09 nm. On DTCO FinFET process, SRAM is designed using three primary configurations. 1:1:1, 2:5:2 and 1:5:2. The impact of Results is also discussed. It is observed that the n-type DTCO_F has lower ION compared to the n-type UF. However, the DTCO_F offers higher ION-IOFF ratio compared to the UF.

Table 1: Existing P-Type FinFETs Device Charactersitics

p-FinFET	I_{ON}	I_{OFF} (nA/µm)	SS (mV/dec)	DIBL (mV/V)	I_{ON}/I_{OFF}
SUF	1.99 mA/µm	100.44	78.4	74.9	$1.98\text{x}10^4$
DTCO_F	26.90 µA/µm	0.004	64.34	24.1	$6.72\text{x}10^6$

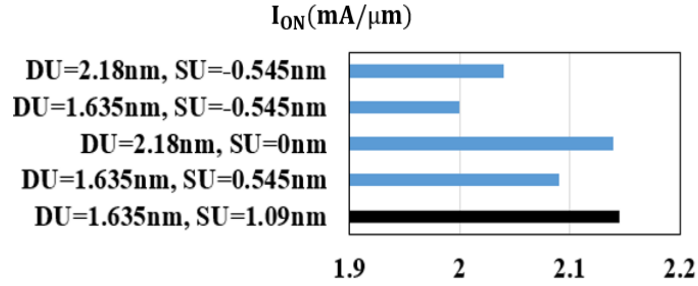

Figure 2: ION of n-type AUF devices with varying DU and SU [45].

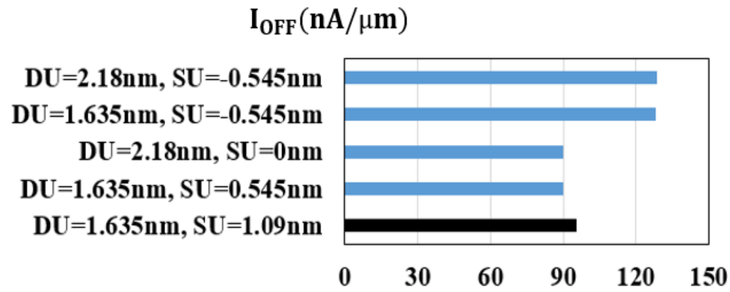

Figure 3: IOFF of n-type AUF devices with varying DU and SU [45].

Based on high ION/IOFF ratio criteria, we designed optimized SRAM designs using AUF device with DU=1.635 nm and SU=1.09 nm.

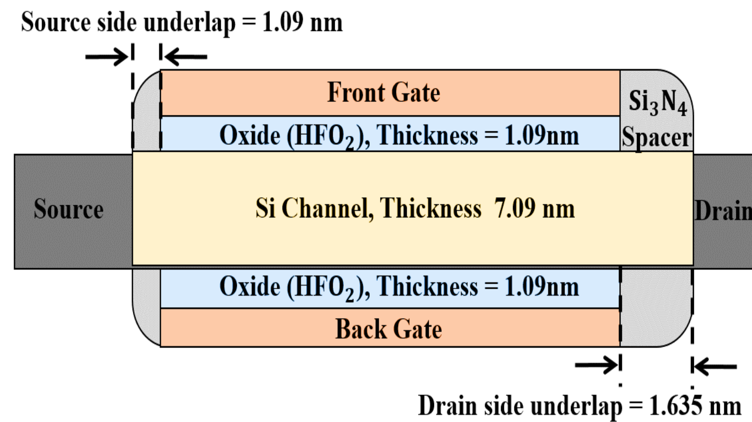

Figure 4: AUF device structure having DU=1.635 nm and SU=1.09 nm [45].

2.4 Conclusion

Hence, it can be concluded that, with exponential increase in number of transistors and scaling down of technology, FinFET and Asyymetrical Underlapped FinFETs has emerged as a promising device to provide better performance than CMOS design. FinFETs overcome the limit of scaling issue and fundamentally have good suppression of short-channel effects (SCEs), sub-threshold swing (SS), low leakage current, and better performance. However, with FinFET having width quantization issue, Asymmetrical underlapped FinFET design overcomes this limitation by providing an underlap on either side of the gate. Asymmetrical Underlapped FinFET (AUF) devices have better control on SCEs in sub nanometer technologies Thus, for High speed and low power applications, Asymmetrical Underlapped FinFET offers a promising direction in VLSI.

CHAPTER 3

FINFET BASED SRAM BITCELL DESIGN

The degraded read and write stability of SRAM cells have become primary design concerns wirh scaling down of CMOS in sub 10 nm rechnology. In this Chapter, Asymmetrical Underlapped FinFET based 6T and 8T SRAM cells is designed at a reduced supply voltage of 500mV. Performance and reliability of both SRAM designs is evaluated and benchmarked. Read and Write stability of SRAM cells are determined using Static Noise Margin and N-curve methods. In addition to this, Monte carlo simulations are also performed on SRAM cells to evaluate process variations. Simulations are done using HSPICE using 7nm Asymmetrical Underlap FinFET technology.

3.1 Introduction

Exponential increase in number of transistors, have increased the density and the total power consumption of the system. Moreover, the scaling of technology has degraded the performance of CMOS designs because of the short channel effects (SCEs) [35]. In sub nanometer technologies, FinFET devices have better gate control and therefore, achieves better performance than CMOS designs. In addition to this, FinFET devices possess high ION and better scalability in contrast to bulk CMOS. Among various double gate devices, the quasiplanar FinFET structure gained huge attention because of the ease in fabrication process. However, FinFET based designs have major width quantization issue. The width of FinFET device increases only in quanta of silicon fin height (H_{FIN}). Width quantization issue becomes

more critical for ratioed designs like SRAMs, where proper sizing of transistors is essential for correct functionality. With process variations this problem is further worse and affect the reliability of SRAM cell. Therefore, it is necessary to optimize the SRAM bitcell for better performance, read stability and write ability [40], [41].

Besides, additional improvements in overall power consumption of system can be achieved with proper optimization of SRAM bitcell circuit. SRAM occupies nearly 70% of the total die area and provides circuit level optimization platform [41]. In this chapter, we designed optimized 6T and 8T SRAM bitcell circuits for intermediate application (trade-off between high density, high performance). The pull-up (PU), pull-down (PD) and pass gate (PG) ratio of both SRAM designs are 1:5:2. This chapter address the read stability and write ability of both 6T and 8T FinFET based SRAM designs in sub 10nm domain. In addition to this, the chapter present performance summary of optimized SRAM designs.

The rest of chapter is organized as follows. Section 3.2 and 3.3 provides a brief overview of the 6T AUF SRAM and 8T AUF SRAM designs. Section 3.4 presents the Hspice simulation of 6T and 8T AUF SRAM. Section 3.5 evaluates performance and reliability of 6T and 8T AUF SRAM. Finally, Section 3.6 concludes the chapter.

3.2 6T AUF SRAM

Reliable read and write operations are the key consideration in SRAM design. Due to the simplicity and symmetry of the 6T SRAM cell circuit it is very area efficient. However, special attention should be given for properly sizing the transistors to avoid read and write upsets, because the design is based on strict sizing ratios among the six transistors to ensure stable read and write operation. In the 6T SRAM, two-bit lines are used to store and read the data as shown

in Figure 5. In this two bit-line architecture of 6T cell the bit lines are not electrically separated from the storage nodes during the read and write operations. This leads to inadvertent toggling of data stored in the cross-coupled inverter during the read operation. Moreover, the cell is highly vulnerable to noise during the read operation. This increase the chances of error known as read upset. Apart from this, during read operation the voltage of storage node with logic "0", increases to a certain value based on the voltage division between access and pull-down transistors. Increase in the voltage at storage node with logic "0", leads to decrease in the voltage of storage node with logic "1" because of the positive feedback characteristic. Yet, this enhancement in the voltage cannot flip the data of cell. Therefore, read operation is done successfully. However, write operation require strong access transistor to write data. Write ability of the cell reduces if minimum size access transistors are used. This challenge is referred as read and write access transistor sizing conflict [41].

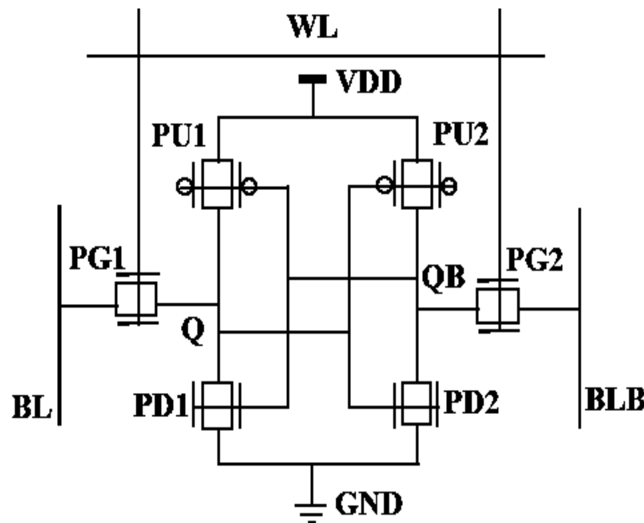

Figure 5: Schematic of 6T AUF SRAM cell [42], [45]

Besides, 6T SRAM cell fails to operate in low-power and ultra-low-power (subthreshold) regions. 8T SRAM cell overcome the limitation of the 6T SRAM using different techniques to improve the functionality and stability of SRAM cell. Some of these techniques are (i) using separate read mechanism, (ii) asymmetric design, and (iii) one-sided access [42].

3.3 8T AUF SRAM

In 8T SRAM as shown in Figure 6, there are two additional stack transistors that provide the access to the cell through the additional read bit-line (RBL). It has two dedicated word-lines (WWL and RWL). Everything else is similar to the standard 6T SRAM. The reading operation of this 8T SRAM is separated from the rest of the cell, which increases the read static noise margin (RSNM). Higher noise margin ensures better read stability and robustness. The read operation of 8T SRAM does not disturb the storage data of cell. However, 6T SRAM is vulnerable to read upset, because in 6T the access transistor pulls the "0" storage node above the ground, which degrades the SNM.

The performance of 8T SRAM during the read operation is determined by the strength of the read stack transistors. To improve the read stability of 6T SRAM cell both halves of the cells should be enlarged. But in 8T SRAM, the read stability can be improved by increasing the size of the stack transistors only [34], [40].

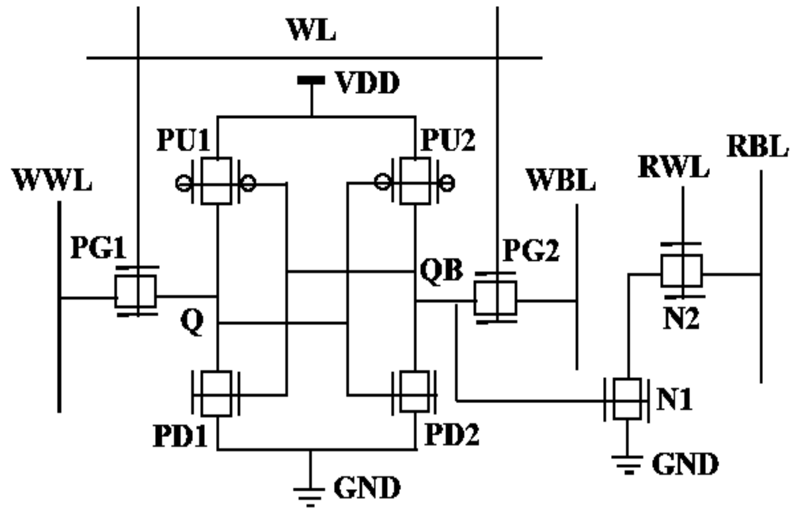

Figure 6: Schematic of 8T AUF SRAM cell [45].

3.4 HSPICE simulation of 6T and 8T AUF SRAMs

Considering LSU=1.09 nm and LDU=1.635 nm and using HSPICE, Assymetric Drain underlapped FinFET based 6T and 8T SRAM simulation is done in 7nm technology.

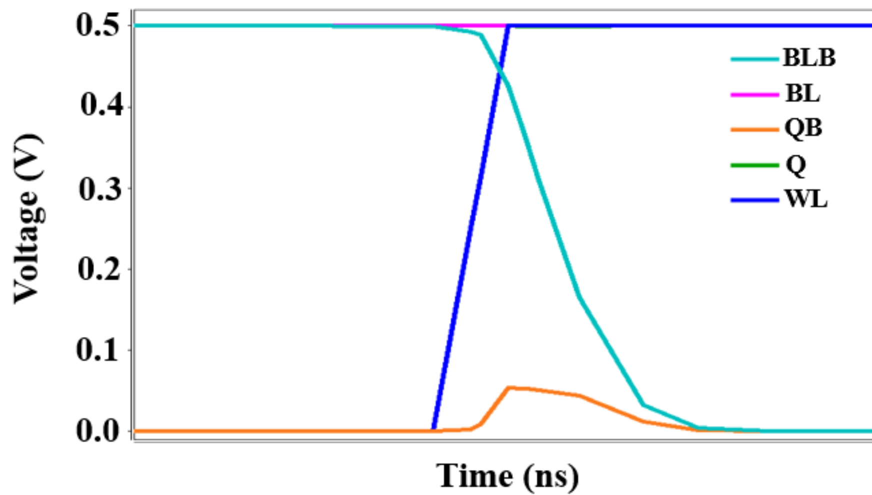

Figure 7: Read Characteristics of 6T Asymmetrical Drain underlapped FinFET.

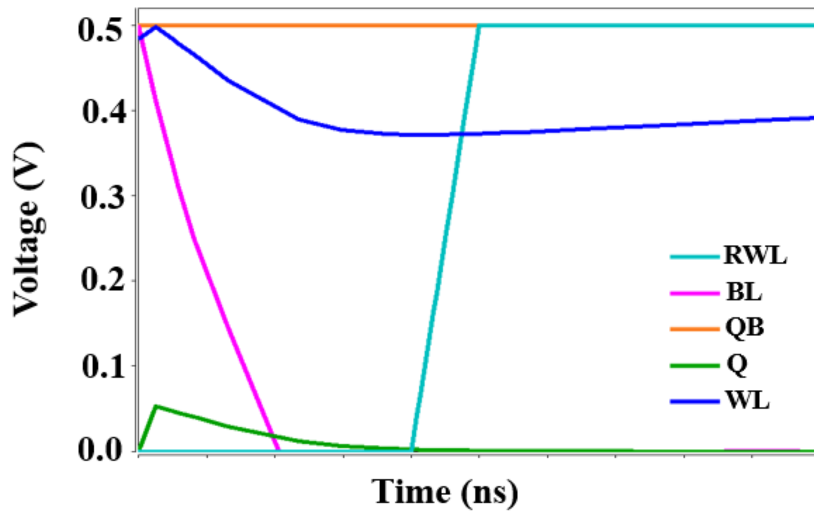

Figure 8: Read Characteristics of 8T Asymmetrical Drain underlapped FinFET

Figure 7 shows the read characteristics of 6T SRAM cell using Asymmetrical Drain underlapped FinFET. When WL (navy blue line) is asserted and QB=0 and Q=1 is given, it can be seen the BLB (blue line) discharges to GND. Hence QB=0 is read. (orange line)

Figure 8 shows read characteristics of 8T SRAM cell using Asymmetrical Drain underlapped FinFET. When WL (green line) is asserted and QB=1 and Q=0 is given, it can be seen the RBL (violet line) discharges to GND. Hence Q=0 is read. (green line)

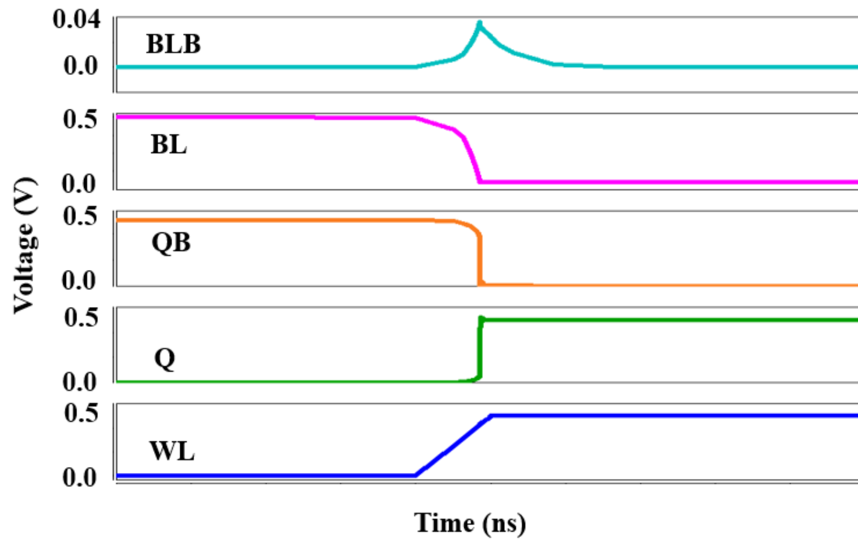

Figure 9: Write operation of 6T Asymmetrical Drain underlapped FinFET (Q=1, QB=0).

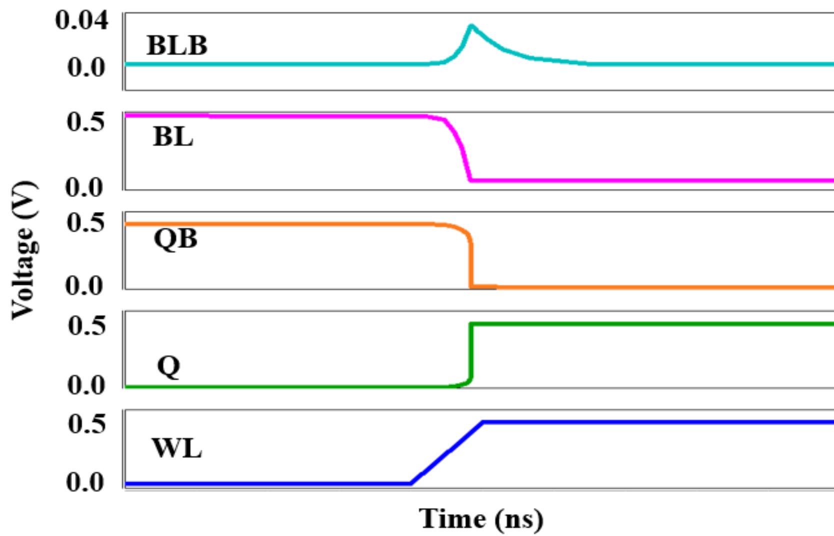

Figure 10: Write operation of 8T Asymmetrical Drain underlapped FinFET (Q=1, QB=0).

Figure 9 shows the write operation of 6T SRAM cell using Asymmetrical Drain underlapped FinFET. During the write operation, WL (navy blue line) is asserted, QB=1 and Q=0 is given initially. From the Figure 4 Q=1 is written (green line) and (b) QB=0 is written (orange line)

Figure 10 shows the write operation of 8T SRAM cell using Asymmetrical Drain

underlapped FinFET. During the write operation, WL (navy blue line) is asserted, QB=1 and Q=0 is given initially. From the Figure 5 QB=0 is written (orange line) and Q=1 is written (green line).

3.5 Performance and reliability of 6T and 8T AUF SRAMs

Two of the most critical metrics in terms of the reliability and the robustness of the SRAMs are the read stability and the write ability. The reliability and the robustness of the SRAM cell are investigated using greatly accepted N-curve method [43] - [45]. This approach is used to determine the read stability as well as to measure the write ability. The N-curve illustrates the stability of the SRAM cell in terms of current. The proposed design is initially set to hold the "0". DC noise source (IIN) is connected to QB of the SRAM cell. Bit-lines are clamped to VDD. Then a DC sweep is performed on QB to get current waveform through IIN. This current curve crosses zero at A, B and C as shown in Figure 11.

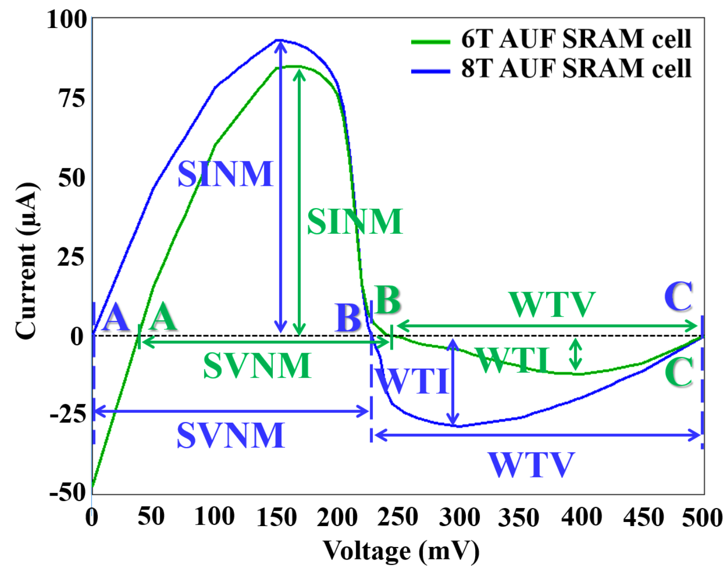

Figure 11: N-curve analysis of 6T and 8T AUF SRAM cell.

The part between C and B represents write ability. The voltage difference between C and B is defined as write trip voltage (WTV). It is the voltage required to change the data of cell. The negative peak current between C and B is the write trip current (WTI). It is the current margin of the cell which changes the data stored at the storage node. Similarly, the part between A and B represents read stability. Static voltage noise margin (SVNM) is the voltage difference between A and B. It is the maximum tolerable DC noise voltage before flipping the content of the cell. The current peak between A and B is the Static current noise margin (SINM). It is the maximum current which can be injected in SRAM cell without flipping the data of cell. Table 1 shows the performance and reliability summary of 6T and 8T AUF SRAM designs.

Table 2: Benchmarking of AUF SRAM designs [45].

AUF SRAM Designs		6T SRAM	8T SRAM
Supply Voltage		500 mV	
Standby Leakage Power (nW)		2.71	2.98
Read	Delay (ns)	2.25	2.85
	Power (nW)	2.415	2.764
Write	Delay (ns)	0.65	0.75
	Power (nW)	2.512	2.109
Static Noise Margins	HSNM (mV)	181.3	185.8
	RSNM (mV)	135.6	180.2
	WSNM (mV)	420.4	436.2
N-curve	SVNM (mV)	206.79	228.06

SINM (μA)	84.74	93.02
WTV (mV)	255.29	271.94
WTI (μA)	-11.98	-28.49

From the analysis, it is observed that 6T AUF SRAM cell achieves 44.97% improvement in the read energy compared to 8T AUF SRAM cell. However, 6T SRAM cell write energy degraded by 3.16% compared to 8T SRAM cell, as shown in Figure 12 and Figure 13. Monte Carlo simulations were performed on 6T and 8T AUF SRAMs to evaluate process variations. For simulation, V_{TH} was modeled as a ±10% Gaussian distribution with variation at the ±3σ level. Figure 16 and Figure 17 show Monte Carlo simulations [46] – [49] of 6T and 8T AUF SRAMs with 2000 samples at 500mV supply voltage. The simulation results show that with process variation, the worst SVNM, worst SINM, worst WTV and worst WTI of 6T AUF SRAM are 40.54mV, 4.06μA, 101.33mV and 326.43nA. Similarly, worst SVNM, worst SINM, worst WTV and worst WTI of 8T AUF SRAM are 151.92mV, 29.86μA, 194.73mV and 9.921μA.

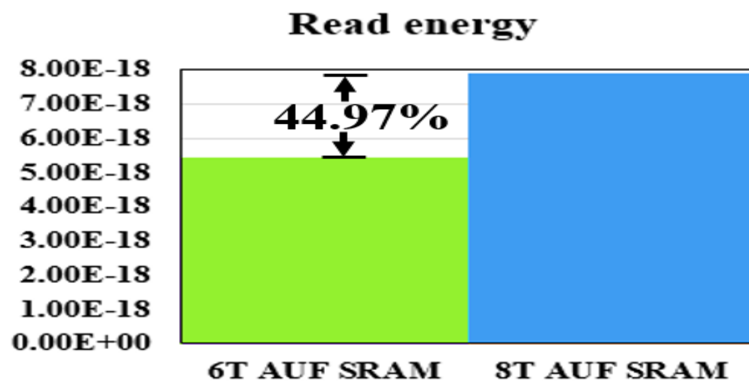

Figure 12: Read energy of 6T and 8T AUF SRAM cell.

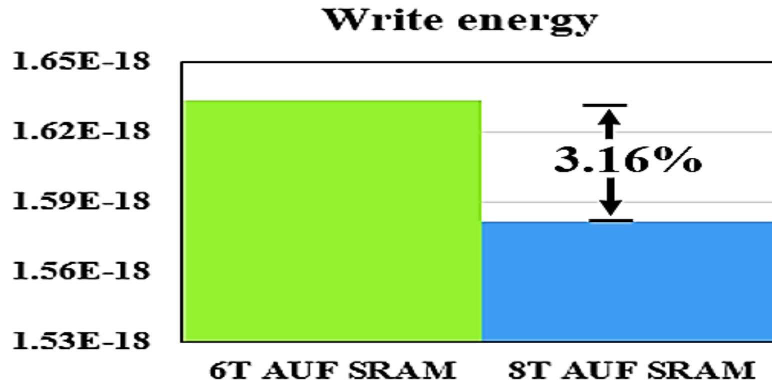

Figure 13: Write energy of 6T and 8T AUF SRAM cell.

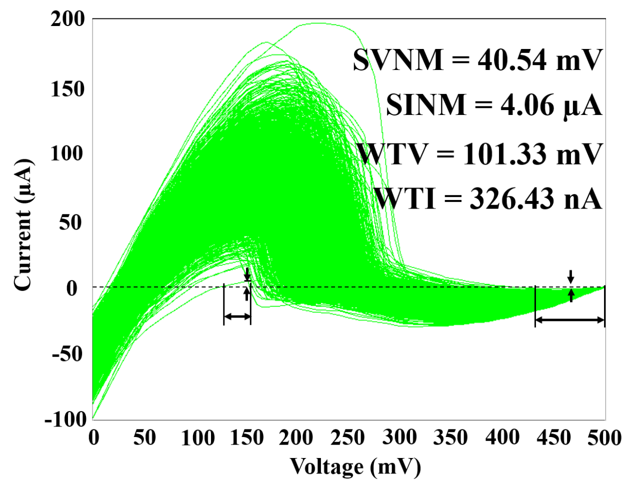

Figure 14: N-curve analysis of 6T AUF SRAM cell under process variation.

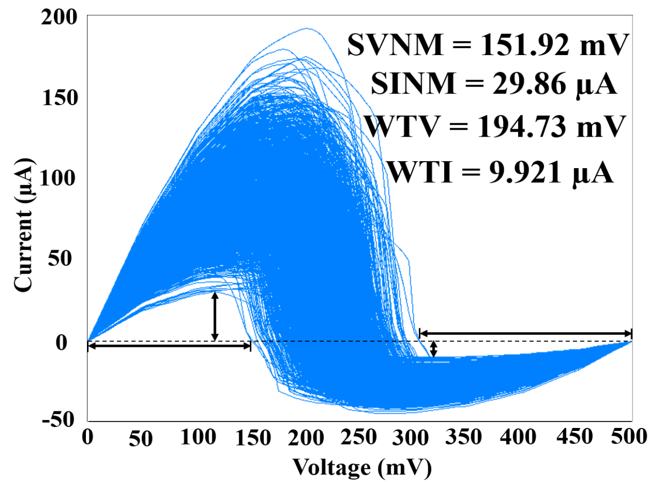

Figure 15: N-curve analysis of 8T AUF SRAM cell under process variation.

Important aspects of the benchmarking are discussed as follow.

- 6T AUF SRAM have low read stability compared to 8T AUF SRAM, which further degrade due to process variations. Worst SVNM and worst SINM of 6T AUF SRAM are 3.74 and 7.35 times less than 8T AUF SRAM.

- Worst WTV of 6T AUF SRAM is 1.92 time less than worst WTV of 8T AUF SRAM. However, worst WTI of 6T AUF SRAM improved by 30.39 times compared to 8T AUF SRAM.

3.6 Conclusion

Among different existing AUF devices, underlap FinFET device with DU=1.635 nm and SU=1.09 nm achieve maximum ION/IOFF ratio. With the selected AUF device, comparisons were done with optimized 1:5:2configuration6T and 8T SRAM designs in terms of performance, read stability and write ability. It is observed that 6T attains 44.97% improvement in the read energy compared to 8T AUF SRAM. However, write energy of 6T AUF SRAM worsen by 3.16% compared to 8T AUF SRAM. From the analysis, the optimized 8T AUF SRAM design possess high stability in ideal case and under process variation compared to the optimized 6T AUF SRAM design.

CHAPTER 4

BENCHMARKING OF UF-SRAMS AND DTCO-F-SRAMS

This chapter determines the robustness of 6T SRAM designs for different pull up, pull down and pass gate transistor ratio (PU: PD:PG) configuration using underlapped FinFETs (UF) and design/technology co-optimized FinFETs (DTCO_F). It is observed that UF-SRAMs read static noise margin worsen by 83.353%, 28.61% and 28.45% for 1:1:1, 1:5:2 and 2:5:2 configurations compared to DTCO_F-SRAMs. However, write static noise margin of UF-SRAMs improved by 52.7%, 54.86% and 53.71% for 1:1:1, 1:5:2 and 2:5:2 configurations compared to DTCO_F-SRAMs. In addition to this, the paper presents Monte Carlo simulations of SRAM designs, which determine the robustness of SRAM cell under process variations. Simulations were done in HSPICE.

4.1 Introduction

Performance of CMOS designs degrade at lower technology node because of short channel effects (SCEs). However, FinFET designs achieve better performance because of the better ability to control gate. FinFET devices provide high ION and better scalability compared to bulk CMOS. Quasiplanar FinFET structure gained huge attention among different available double gate devices because of the ease in fabrication process. Underlap on source and drain sides increases the effective channel length seen by the charge carriers. Therefore, source-to-drain tunneling probability is improved. Moreover, edge direct tunneling leakage components can be reduce by controlling electric field at the gate-drain junction. There is limitation on the extent of underlap on drain or source sides, as ION decreases corresponding to the large

underlap. However, FinFET based designs have major width quantization issue. The width of FinFET device increases only in quanta of silicon fin height (HFIN. Width quantization issue becomes more critical for ratioed designs like SRAMs, where proper sizing of transistor is essential for correct functionality. With process variations, this problem further degrades and affect the reliability of SRAM cell. FinFET devices developed using design/technology co-optimization (DTCO_F) overcome these issues. DTCO_F follow the design rules released in the kit. The PDK provides standard SRAM cell with special spacing rules and low leakages [20].

Read stability and write-ability are the important aspects of the SRAM cells in sub-nanometer technologies, because of the increase in die variability [19]. In this paper, we address the stability and reliability of SRAMs based on underlapped FinFETs (UF) and DTCO_F for high density, high performance and intermediate (trade-off between density and performance) applications. Robustness of 1:1:1, 1:5:2 and 2:5:2 (PU: PD:PG) configurations SRAM designs are evaluated at 500mV supply voltage. In this chapter, Section 4.2 presents about presents UF and DTCO_F devices. Section 4.3 talks about UF and DTCO_F based SRAMS. Section 4.4 concludes the chapter.

4.2 UF and DTCO_F Devices

There are two types of UF devices available in the literature - the equal or symmetric underlapped FinFETs (SUF) and the unequal or asymmetric underlapped FinFETs (ASUF), where the unequal underlap on either side of the gate in FinFETs leads to different values of ION based on which ends of the device act as the source and drain terminals. The ASUFs offer

better performance compared to the SUFs. Moreover, the ASUFs with source side underlapped (SU) having long drain side underlapped (DU) achieves improved Drain Induced Barrier Lowering (DIBL) due to the better shielding of the channel potential barrier from the drain field lines by superseding drain underlap [20]. However, characteristics of the ASUFs with SU are worse because of the existence of the edge direct tunneling (EDT). Figure 16 shows the Ion, Ioff, DIBL and Ion-Ioff ratio of different existing n-type FinFET devices. The n-type ASUF device with SU=1.09 nm and DU= 1.635 nm achieves the maximum ION-IOFF ratio among the available n-type ASUFs. A Predictive process design kit (PDK) is developed by Arizona State University. This FinFET device is developed using design/technology co-optimization (DTCO_F) and overcomes FinFET's width quantization issues.

DTCO_F follow the design rules released in kit.. The PDK provides standard SRAM cell with special spacing rules and low leakages. PDK fins are 32nm in height, 6.5nm thick and 7nm in width.[38]. On DTCO FinFET process, SRAM is designed using three primary configurations. 1:1:1, 2:5:2 and 1:5:2. The impact of Results is also discussed. It is observed that the n-type DTCO_F has lower ION compared to the n-type UF. However, the DTCO_F offers higher ION-IOFF ratio compared to the UF. For our analysis, we have selected an n-type ASUF device with DU=1.635 nm and SU=1.09 nm, and a p-type SUF device illustrated in [4] and [19] to implement the design of the UF 6T SRAM. The following chapter explores different metrics of the UF and DTCO_F based SRAMs for different pull-up, pull-down and pass-gate configurations.

Table 3: Existing DTCO FinFETs Device Charactersitics

DTCO FinFET	I_{ON} uA	I_{OFF} nA	SS (mV/dec)	DIBL (mV/V)
p-FinFET	26.90	0.004	64.34	24.10
n-FinFET	28.57	0.001	62.44	19.23

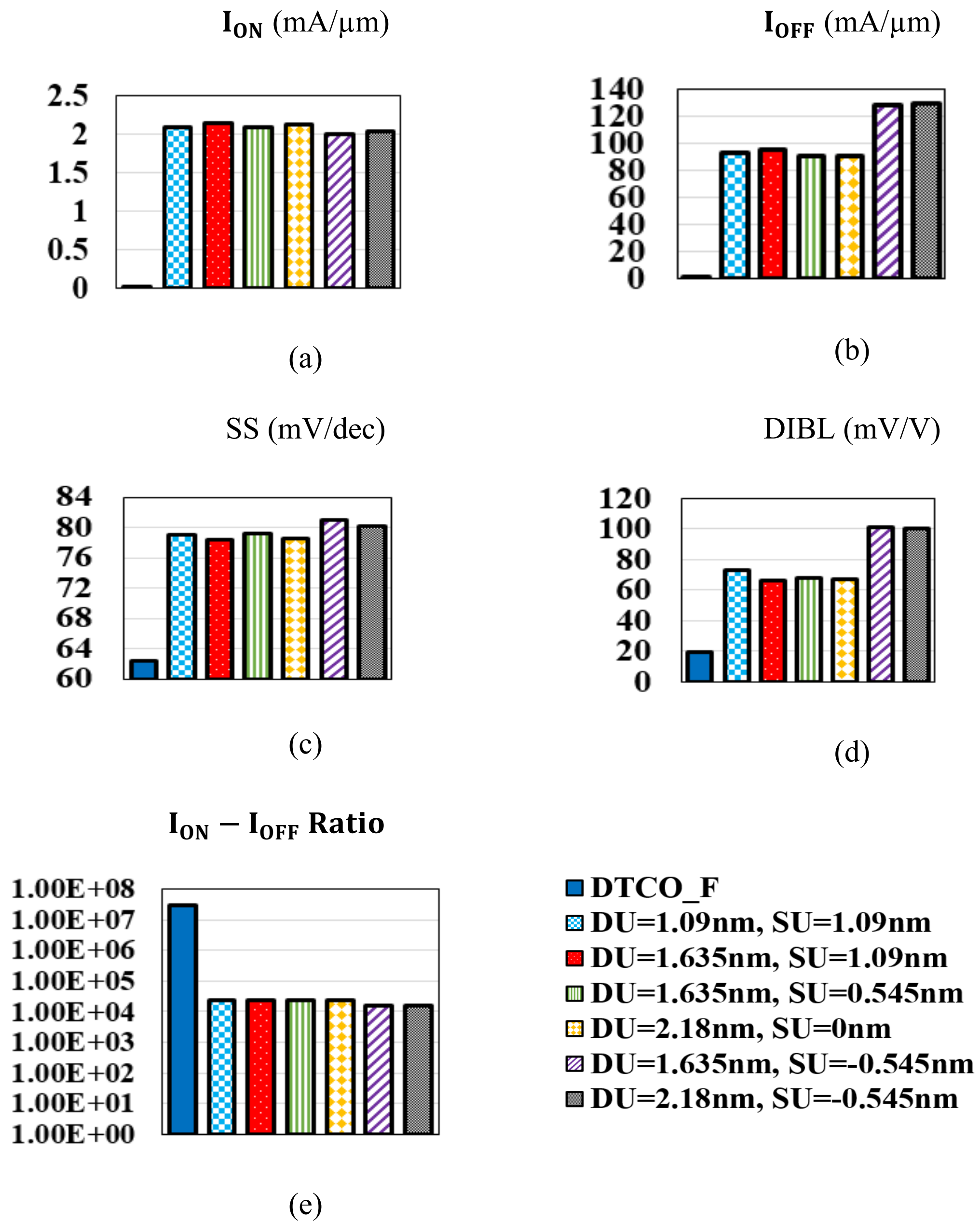

Figure 16: (a) I_{ON}; (b I_{OFF}; (c) SS (d) DIBL; (e) I_{ON}-I_{OFF} ratio of different existing n-type FinFET devices [39].

4.3 UF-SRAMS and DTCO_F SRAMS

In this section the performance of 6T SRAM designs are compared for different pull up, pull down and pass gate transistor ratio configurations (PU:PD:PG) using underlapped FinFETs (UF) and design/technology co-optimized FinFETs (DTCO_F). The objective is to identify the best FinFET device for designing SRAM for high speed and low power applications. Moreover, this section present reliability and stability analysis of UF-SRAMs and DTCO_F-SRAMs for different pull up, pull down and pass gate transistor ratio configurations.

Three different static noise margin (SNM) Figures are essential to evaluate the robustness of the SRAM bit cell. These are the Hold Static Noise Margin (HSNM), the Write Static Noise Margin (WSNM) and the Read Static Noise Margin (RSNM). Figure 17 and 18 show the RSNM and the N-curve analysis of the UF-SRAM with a 500mV supply. It is observed that for the 1:1:1configurationthe UF-SRAM have the lowest robustness compare to the designs with other ratios. Monte Carlo simulation is also performed for the UF-SRAM with 1:1:1 ratio to evaluate the impact of the process variations. The threshold voltage (VTH) is modeled as a ±10% Gaussian distribution with a variation of the ±3σ level. 21 shows the Monte Carlo analysis of the UF-SRAM bit cell for 1:1:1configurationwith 3000 samples at the 500mV supply voltage. Table 4 provides the summary of the performance and stability of the UF and DTCO_F based SRAMs for different PU: PD:PG configurations.

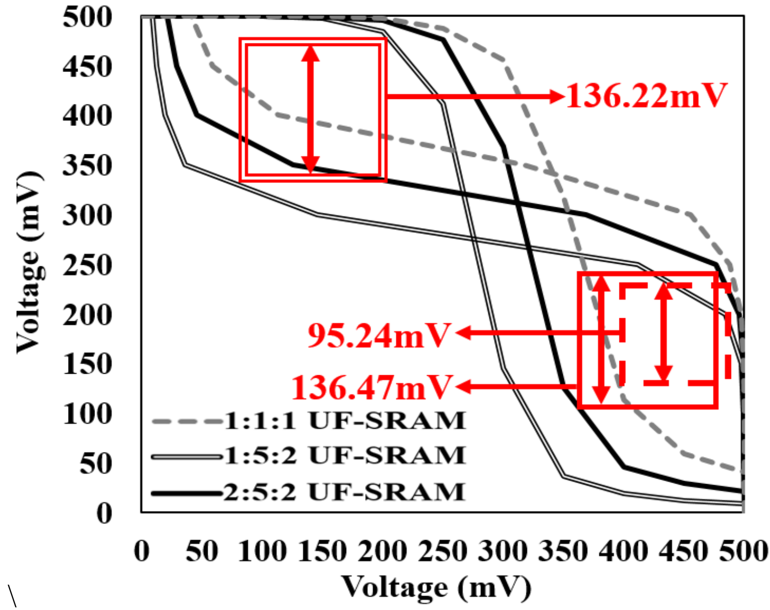

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Figure 17: RSNM of different configuration UF-SRAMs.

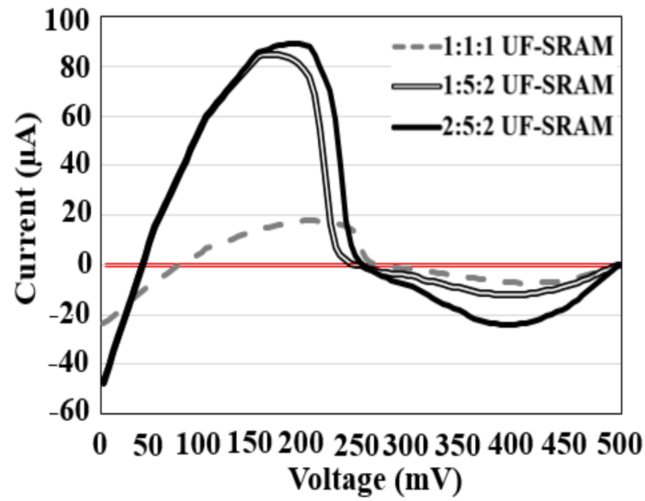


Figure 18: N-curve analysis of differentconfigurationUF-SRAMs.

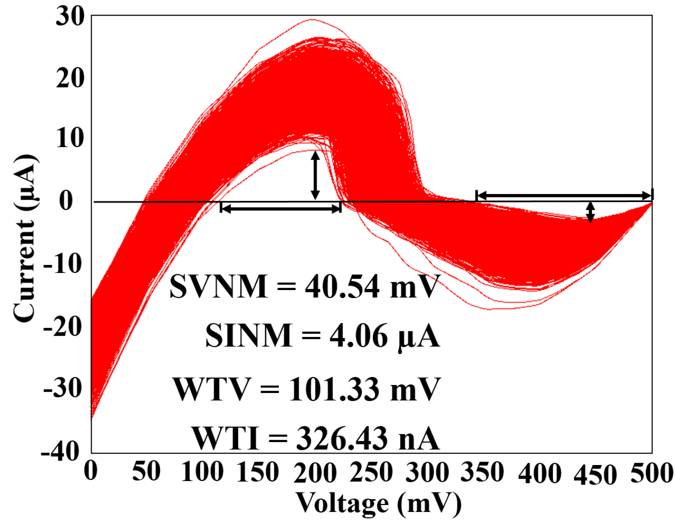


Figure 19: N-curve analysis of 1:1:1 UF SRAM under process variation.

Read energy of 1:1:1 and 1:5:2 UF-SRAMs degraded by 3.31% and 48.72% compared to DTCO_F-SRAMs. However, read energy of 2:5:2 UF-SRAM improved by 32.71% compared to DTCO_F-SRAMs. Similarly, write energy of 1:1:1 UF-SRAM improved by 642.27% compared to DTCO_F-SRAM. Conversely, write energy of 1:5:2 and 2:5:2 UF-SRAMs worsen by 86.26% and 96%. Figure 20 and Figure 21 show the read and write energy comparison of UF-SRAM and DTCO_F-SRAM for different PU:PD:PG configurations.

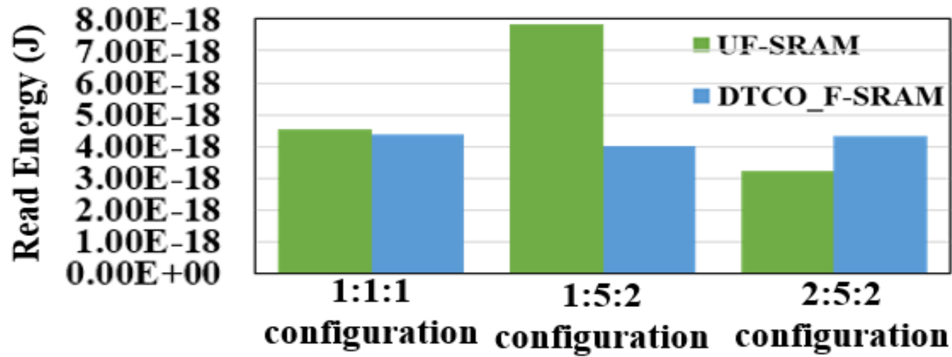


Figure 20: Read energy of different configurations 6T SRAM bitcell.

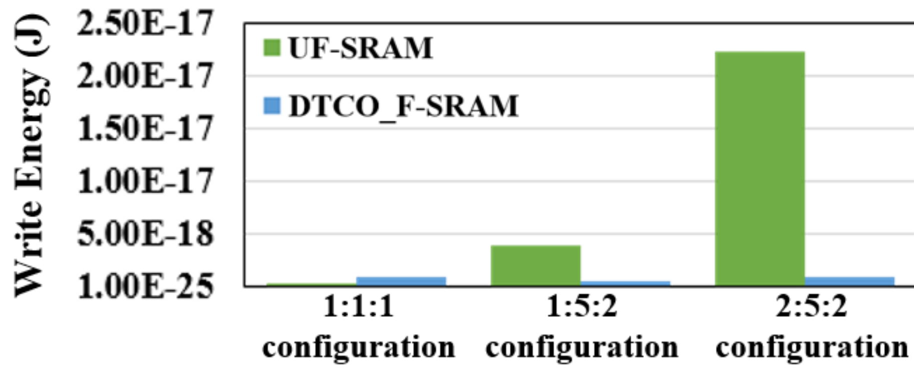


Figure 21: Write energy of different configurations 6T SRAM bitcell.

Table 4: Benchmarking of 6T UF-SRAM and 6T DTCO_F-SRAM Designs [39].

Designs	6T UF-SRAM			6T DTCO_F-SRAM		
Technology	7 nm			7 nm		
Supply	500mV			500mV		
PU: PD:PG	1:1:1	1:5:2	2:5:2	1:1:1	1:5:2	2:5:2
Standby leakage power	852.34 pW	2.719 nW	3.07 nW	27.5 pW	27.5 pW	27.5 pW
Read Power (nW)	1.68	3.06	3.24	2.01	2.036	2.04
Write Power (nW)	1.34	58.63	118.8	5.1	5.09	5.09
Read Delay (ns)	2.68	0.161	0.179	2.77	1.97	2.11
Write Delay (ns)	0.092	0.064	0.187	0.179	0.043	0.174
HSNM (mV)	175.13	182.8	183.26	240.2	240.4	240.4
RSNM (mV)	95.24	136.22	136.47	174.8	175.2	175.3
WSNM (mV)	401.33	421.18	411.15	189.8	190.1	190.3
SVNM (mV)	195.76	204.33	212.88	202.57	202.6	202.62
SINM (µA)	17.96	89.27	84.79	9.60	9.62	9.66
WTV (mV)	229.58	253.64	248.53	232.79	233.01	233.2
WTI (µA)	7.201	23.96	11.92	2.40	2.43	2.44
Area (μm^2)	0.0114	0.019	0.0218	0.0117	0.0212	0.0231

4.4 Conclusion

UF device with DU=1.635 nm and SU=1.09 nm achieve maximum ION/IOFF ratio and was selected to design SRAM bitcells for different configurations. Read stability and write ability of UF-SRAMs are compared with DTCO_F-SRAMs at 500mV supply in 7nm domain. UF-SRAMs have low stability compared to DTCO_F-SRAMs. RSNM of UF-SRAMs degraded by 83.353%, 28.61% and 28.45% for 1:1:1, 1:5:2 and 2:5:2 configurations. Moreover, from combined information of SVNM and SINM it is confirming that the read stability of UF-SRAMs is worse than DTCO_F-SRAMs. However, UF-SRAMs have better write ability than DTCO_F-SRAMs. WSNM of UF-SRAMs improved by 52.7%, 54.86% and 53.71% for 1:1:1, 1:5:2 and 2:5:2 configurations. From combined information of WTV and WTI, we can conclude that the write ability of UF-SRAMs is better than DTCO_F-SRAMs.

CHAPTER 5

COLLABORATIVE PROJECT

This chapter presents collaborative project done with other research mate of Nano and Micro Lab at UMKC. In this project, the main motivation was to design a power-gating configuration of SRAM using Fully Depleted Silicon-on-Insulator (FDSOI). Power saving techniques have become essential for modern digital systems. Large on-chip SRAM memories are used in these systems and therefore it is necessary to optimize SRAM bitcell circuit to minimize the power consumption. In addition to this, it is equally important to design SRAM cell with high reliability and stability. Power gating technique with sleep transistor if applied to SRAM cell will degrade the performance of the cell. In this chapter, Fully Depleted Silicon-on-Insulator (FDSOI) device-based SRAM designs are proposed which eliminate the requirement of sleep transistors to reduce the power consumption. This reduces overall complexity and overheads of power gating memory designs.

5.1 Introduction

Power gating is a promising technique utilized to minimize power consumption in the SRAM designs. Sleep transistors aid in managing the power and thermal effects of the design. Conventional sleep transistor-based power gating configurations are shown in Figure 22. High threshold voltages (V_{TH}) header and footer sleep transistors are utilized to isolate actual supply lines from virtual supply lines. High-V_{TH} sleep transistors are placed between the SRAM bitcells and the supply lines to reduce leakage power during standby. However, these high-V_{TH}

sleep transistors occupy extra area and increases delay and power. In addition, extra wiring for virtual nodes will further increase unwanted RLC issues and IR-drops [50]. To overcome these limitations, double-gate FDSOI [51]-[54] are used to design SRAM bitcell circuit. Double gate FDSOI comprises of two gates whereas the second gate contact (back gate) is created below the substrate. These two gates basically regulate the charges in the channel between the box layer and front gate oxide layer. The idea of double-gate FDSOI technology is to add another conductive layer beneath the SOI device [37]. This design approach eliminates sleep transistors, which reduces the area overheads and improve the performance of the SRAM bitcell. Main idea is to exploit the back gate (BG) bias in double-gate FDSOI to get the required V_{TH} dynamically without using sleep transistors. Since no additional transistors are required for power gating, there is needed to dynamically set high and low V_{TH} values in the same FDSOI device. During write and read lower V_{TH} is preferred for higher gate drive. However, during hold mode, high V_{TH} is preferred to decrease standby leakage power.

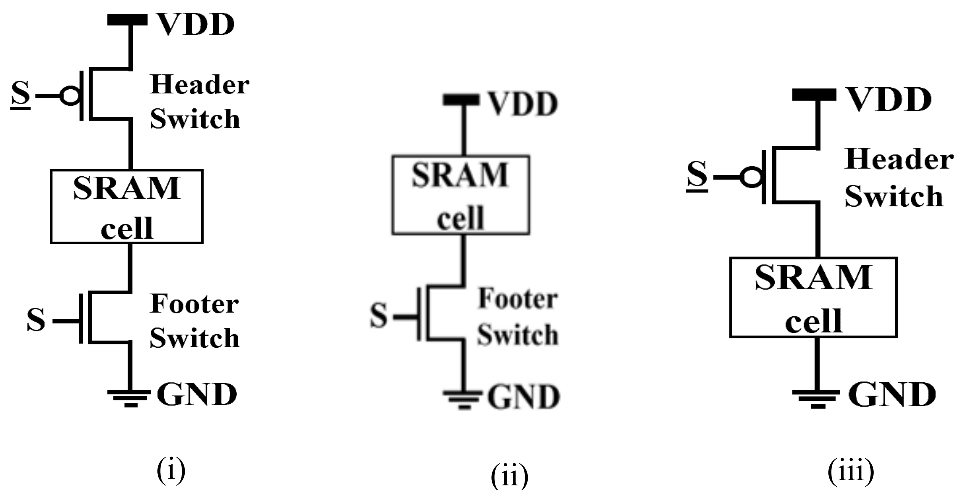


Figure 22: Conventional power gating configuration of SRAM.

5.2 Double Gate FDSOI Device

The double-gate FDSOI device can be viewed as two MOSFETs (front and back) that share same body, drain, and source regions as shown in Figure 23. An additional back gate contact is provided under the substrate. Two gates of the device control the charges in the silicon channels. The silicon film thickness in FDSOI, is typically less or equal to half of the depletion width of the bulk device [55], [56]. Drain current and V_{TH} of the devices, are subjective to the film thickness. Thin films are required to have great control over the performance of the device because the V_{TH} of FDSOI devices are sensitive to the variations in SOI silicon film thickness (Tsi). Moreover, thin SOI film is required to minimize short-channel effects in the SOI MOSFETs [54]. The surface potentials of the FDSOI device at the front and back interfaces are firmly coupled to each other and capacitively coupled to the front-gate and the substrate via the front-gate oxide and buried oxide. Threshold voltage (V_{TH}) of double gate FDSOI is dependent on the BG voltage of FDSOI as shown in Figure 24. V_{TH} of FDSOI is evaluated by equation (1) and (2) [50].

$$V_{TH_F} = V_{FB_F} + 2\Phi_B - \frac{Q_B}{2C_{OX}} - \left(V_{BG} - V_{FB_B} - 2\Phi_B + \frac{Q_B}{2C_{BOX}}\right) \times \frac{C_{SI}C_{BOX}}{C_{OX}(C_{SI} + C_{BOX})} \tag{1}$$

$$Q_B = -qN_A TT_{Si}\ (or) + qN_D TT_{Si} \tag{2}$$

Where V_{FG} and V_{BG} are front and back gate voltages. V_{FB_F} and V_{FB_B} are front and back gate flatband voltages. C_{OX} are front and back gate oxide. C_{BOX} and C_{SI} are buried oxide and depleted silicon film capacitances. Q_B is the area charge density in depleted Si film.

5.3 FDSOI based 6T SRAM Bitcell Design

The conventional 6T SRAM cell has been the industry standard from the beginning of the SRAM era. Reliable read and write operations are the vital concern in SRAM design. Due to the straightforwardness and symmetry of the 6T SRAM cell circuit it is very area efficient. However, in this two bit-line architecture of 6T cell the bit lines are not electrically separated from the storage nodes during the read and write operations. The cell is highly vulnerable to the noise during reads operation. Voltage of the storage node with "0" rises to a higher voltage than ground due to voltage division along access (M5, M6) and pull down (M1, M2) transistors, in the middle of precharged bitlines (BL and BLB) and the ground terminal of the SRAM cell. This situation may end up with reading a wrong value, usually known as read upset. In current micro and nano electronic circuits and systems, the major source of power consumption is the leakage current. This chapter present seven different configurations of double-gate based FDSOI SRAM bitcell designs to minimize leakages and improve performances as shown in Figure 25. Table 5 shows the performance summary of different FDSOI based SRAM bitcell configurations.

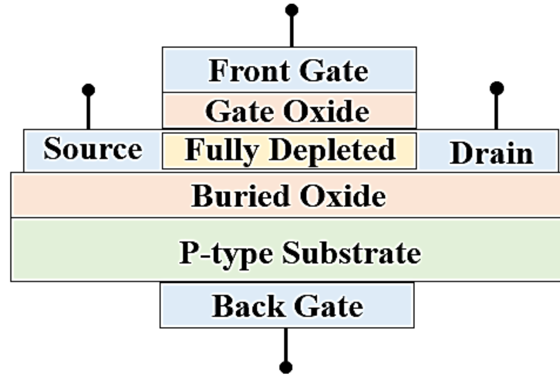


Figure 23: FDSOI MOSFET device

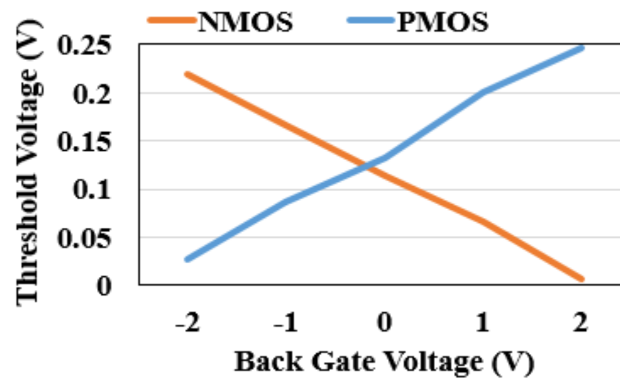
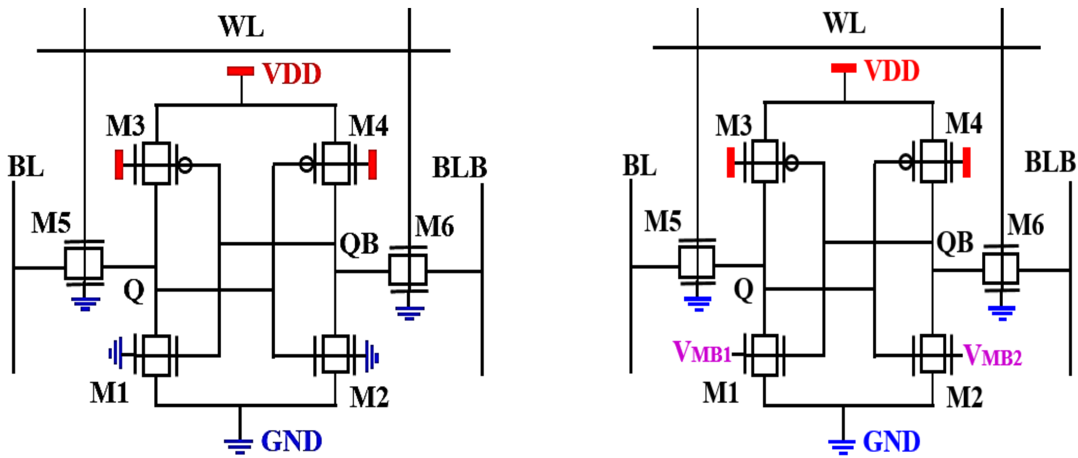
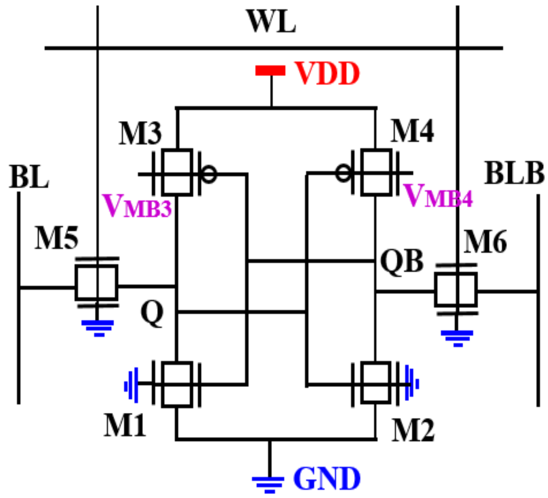


Figure 24: Dependence of threshold voltage upon back gate bias [58].

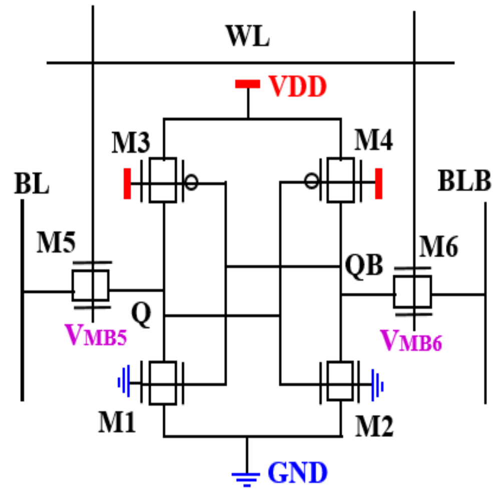


(i) Standard Configuration (C1)

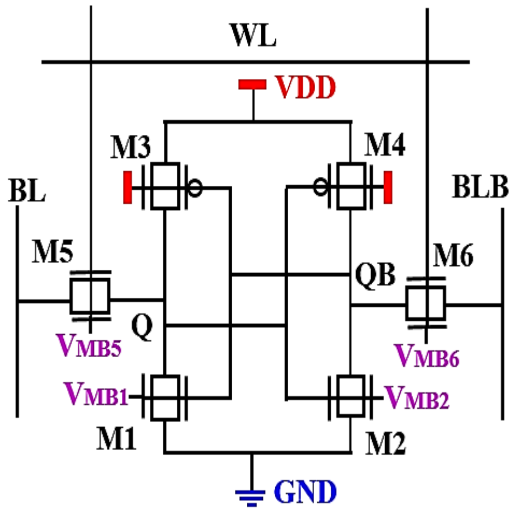
(ii) Configuration-2 (C2)



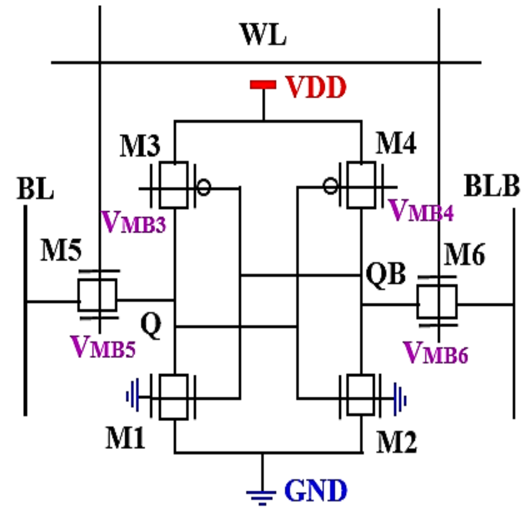
(iii) Configuration-3 (C3)



(iv) Configuration-4 (C4)



(v) Configuration-5 (C5)



(vi) Configuration-6 (C6)

Figure 25: Different configurations of double-gate FDSOI based SRAM bitcell.

Table 5: Performance summary of different FDSOI based SRAM bitcell configurations.[36]

Power gating SRAM bitcell design		(C1)	(C2)	(C3)	(C4)	(C5)	(C6)	(C7)	(C8)
Voltage (V)		1							
Total Power (µW)	Read	12.098	12.451	15.268	11.942	12.322	12.876	12.528	2.323
	Write	40.833	44.65	46.807	46.08	40.199	46.03	49.29	39.966
Standby Leakage Power (nW)		28.77	19.21	49.36	19.23	28.67	49.27	136.98	49.28
Leak-age Curr-ent (A)	Hold	418.96 n	418.96 n	437.16 n	418.96 n	418.96 n	437.16 n	437.16 n	437.15 n
	Read	421.86 n	421.86 n	62.994 µ	421.86 n	485.09 n	66.894 µ	66.894 µ	62.993 µ
	Write	81.89 µ	60.868 µ	170.74 µ	60.853 µ	150.45 µ	177.23 µ	177.23 µ	168.91 µ
Del-ay (nS)	Read	0.415	0.413	0.409	0.365	0.394	0.412	0.360	0.398
	Write	0.462	0.459	0.447	0.409	0.365	0.444	0.46	0.353

Energy (fJ)	Read	5.02	5.142	6.24	4.35	4.85	5.43	4.51	0.924	
	Write	10.88	20.05	20.92	10.88	14.67	20.43	22.67	14.10	
N-curve	SVNM (V)	0.325	0.325	0.348	0.325	0.325	0.348	0.348	0.348	
	SINM (µA)	133.42	133.42	139.95	133.42	133.42	139.95	139.95	139.95	
	WTV (V)	0.5055	0.5055	0.4928	0.5055	0.5055	0.4928	0.4928	0.4928	
	WTI (µA)	51.552	51.552	58.42	51.552	51.552	58.42	58.42	58.42	

Two of the most critical metrics in terms of the reliability and the robustness of the SRAMs are the read stability and the write ability. The N-curve illustrates the stability of the SRAM cell in terms of current. Following setup is made to carry on the analysis. The proposed design is initially set to hold the "0". DC noise source (IIN) is connected to QB of the SRAM cell. Both bit-lines BL and BLB are clamped to VDD. Then a DC sweep is performed on QB to get the current waveform through IIN. This current curve crosses zero at A, B and C as shown in Figure. The part between C and B represents write ability. The voltage difference between C and B is defined as write trip voltage (WTV). It is the voltage required to change the data of cell. The negative peak current between C and B is the write trip current (WTI). It is the current margin of the cell which changes the data stored at the storage node. Similarly, the part between

A and B represents read stability. Static voltage noise margin (SVNM) is the voltage difference between A and B. It is the maximum tolerable DC noise voltage before flipping the content of the cell. The current peak between A and B is the Static current noise margin (SINM). It is the maximum current which can be injected in SRAM cell without flipping the data of cell.

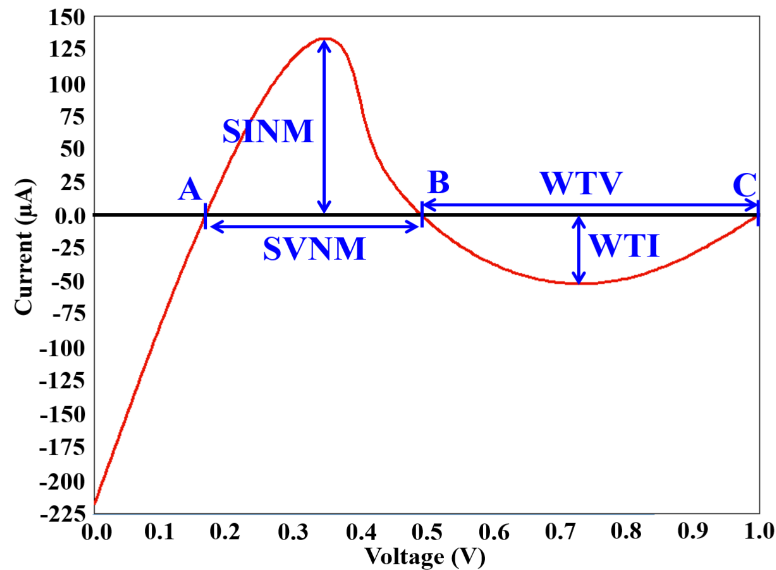


Figure 26: N-curve analysis of C1 configuration SRAM cell.

5.4 Benchmarking of FDSOI based SRAM Cells

Table 7 compares the performance and reliability of different configuration SRAM cells with the standard configuration SRAM cell. The physical significances of benchmarking are discussed below.

- C4 and C8 configuration SRAM cells consume 1.31% and 420.79% less power during read compared to standard C1 configuration SRAM cell. However, C2, C3, C5, C6 and

C7 consume 2.84%, 20.76%, 1.82%, 6.04% and 3.43% more power during read compared to standard C1 configuration SRAM cell.

- C5 and C8 configuration SRAM cells consume 1.58% and 2.17% less power during write compared to standard C1 configuration SRAM cell. However, C2, C3, C4, C6 and C7 consume 8.55%, 12.76%, 11.39%, 11.29% and 17.16% more power during write compared to standard C1 configuration SRAM cell.

- Standby leakage power of C2, C4 and C5 configuration SRAM cells are 49.77%, 49.61% and 0.35% less than standard C1 configuration SRAM cell. Whereas, standby leakage power of C3, C6, C7 and C8 configuration SRAM cells are 41.71%, 41.61%, 79% and 41.62% more than standard C1 configuration SRAM cell.

- Leakage current of C2, C4 and C5 configuration SRAM cells are nearly equal to standard C1 configuration SRAM cell in hold mode. However, leakage current of C3, C6, C7 and C8 are ~ 4.16% more than standard C1 configuration SRAM cell in hold mode.
- During read, leakage current of C3, C6, C7 and C8 configuration SRAM cells are 569.68%, 530.64%, 530.6% and 569.69% less compared to standard C1 configuration SRAM cell. However, leakage current during read for C2, and C4 configurations are nearly equal to C1 configuration, and C5 configuration leakage current during read is 13.03% more than standard C1 configuration SRAM cell.

- During write, leakage current of C2, and C4 configuration SRAM cells are 34.54% and 34.57% less compared to standard C1 configuration SRAM cell. However, leakage current during write for C3, C5, C6, C7 and C8 configurations are 52.04%, 45.57%, 53.79%, 53.7% and 51.52% more than standard C1 configuration SRAM cell.

- C2, C3, C4, C5, C6, C7 and C8 configuration SRAM cells read 0.48%, 1.47%, 13.7%, 5.33%, 0.73%, 15.28% and 4.27% faster than standard C1 configuration SRAM cell.

- C2, C3, C4, C5, C6, C7 and C8 configuration SRAM cells write 0.65%, 3.367%, 12.96%, 26.58%, 4.05%, 0.43% and 30.88% faster than standard C1 configuration SRAM cell.

- Compared to standard C1 configuration; C4, C5, C7 and C8 configuration SRAM cells consume 15.4%, 3.51%, 11.31% and 443.29% less energy during read. However, energy consumed by C2, C3 and C6 configuration SRAM cells are 2.37%, 19.55% and 7.55% more than standard C1 configuration SRAM cell during read.

- Write energy consumption of C4 configuration SRAM cell is 0.02% less than standard C1 configuration SRAM cell. Whereas, all the other configurations have higher written energy consumption compared to standard C1 configuration SRAM cell.

- From combined SVNM and SINM information, it can be concluded that C3, C6, C7 and C8 configuration SRAM cells have better read stability than standard C1 configuration SRAM cell. However, C3, C6, C7 and C8 configuration SRAM cells have lower write ability compared to the standard C1 configuration SRAM cell.

5.5 Conclusion

In this chapter, different performance metrics and stability of double-gate FDSOI based SRAM bitcell designs is evaluated. From the analysis, it is observed that C8 configuration SRAM cell consumes 443.29% less read energy and write 51.52% faster compared to standard C1 configuration SRAM cell. C4 configuration SRAM cell have least write energy. Moreover, the standard configuration (C1) reads and writes slower compared to other configuration SRAM cells. Among all the configurations, C7 reads fastest. Therefore, from the analysis, it is observed that C8 configuration SRAM cell is more suitable for low power and high-speed applications.

CHAPTER 6

INTERNSHIP EXPERIENCE AT INTEL AND MARVELL SEMICONDUCTOR

6.1 Intel Internship Experience

Solid state drives are smaller, faster, reliable, and affordable used for storing all data. It is a type of computer storage. SSDs serve up data faster, can boot your system, switch between tasks, and launch apps quicker. If you use a laptop for work, personal hobbies, gaming, or for entertainment sooner or later you'll need to consider the ways of storing all that data. Most of us are familiar with the capacity of our computer hard disk drives and how we need a backup drive as insurance against losing any of our irreplaceable files, but storage goes beyond that and is constantly evolving. Thus, solid state drives are smaller, faster, reliable, and affordable. These SSDs access data so quickly, game software designs can evolve so that the game can access new assets on a frame-by-frame basis while the game is happening. That means less waiting for game players and dramatically reduced delays.Every new generation of SSDs will allow to store more data per bit. As the per-bit storage increases, data density increases, and costs continue to decrease. Smaller, faster, and more affordable, SSDs will continue to be the storage solution of choice by computer users who need reliable performance. A PCIe SSD (PCIe solid-state drive) is a high-speed expansion card that attaches a computer to its peripherals. PCIe, which stands for Peripheral Component Interconnect Express, is a serial expansion bus standard. PCIe slots can have different sizes, based on the number of bidirectional lanes that connect to it. The number of PCIe lanes per SSD determines the speed of data transfer. A 16-lane device built on the PCIe 3.0 specification can support approximately

32 gigabytes per second. If maximum performance for frequent file transfers is needed, PCIe is likely the most efficient option. Format specifications for PCIe-based devices are developed and maintained by the PCI Special Interest Group (PCI-SIG). PCIe 3.0, was released on November 2010. PCIe 4.0 was released in 2017 and doubles the bandwidth of the previous version. In May 2019, PCI-SIG announced the release of PCIe 5.0.

Figure 27: Intel Solid State Drive

As an Intern , I played an important role in validatIng PCIe-based SSD. I performed Electrical and System Validation for Solid State Drives and ensured it performance meets all PCI SIG specifications. At Intel, we always try to improve computing at all levels and anticipate our customers' needs. With our most advanced Intel PCIe SSDs, we are working with companies that design and manufacture computing systems for businesses, content creators, and video games to identify and support new ways of improving storage and the overall user experience.

6.2 Marvell Semiconductor Inc Internship Experience

The Marvell ThunderX2 ARM server processors are designed to provide cloud and high-performance computing in datacenters by providing the next level of computing performance. The ThunderX2 product family includes multiple SKUs that easily handle the most demanding compute, storage and networking workloads in the cloud and HPC (high performance compute) data centers.

Figure 28: Thunder X2 Server Processor.

My internship project at Marvell was to develop Voltage frequency curve for processor at Turbo for high speed and low power performance. As a post silicon validation intern, my important role was to collect and analyze voltage, frequency and temperature data using data analysis tools across PVT corners. Voltage-Frequency Curve analysis was done with improvement in yield and power management for ThunderX2 Server Processors. I also performed Electrical PCIe Characterization for processors and ensured it performance meets all standard specifications.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Summary of Research Work

Modern world technologies and Data centers CPU heavily rely on memories. In order to satisfy these requirement, emerging devices like FinFET devices are utilized to design memories. FinFET devices overcome the MOSFET short channel effect challenges. The Static Random-Access Memory (SRAM) has a significant performance impact on the current Data center server systems. Hence, memories ie SRAM (Static Random-Access Memory) with high speed and low power is desired inside a CPU to provide better performance and reliability.

Scaling of technology has increased serious challenges like the short channel effects (SCEs) in the bulk CMOS devices. To overcome these issues, FinFET devices are introduced. FinFET offers better gate control, higher ION, better scalability and therefore, improved performance and reliability compared to the conventional CMOS designs. Different types of FinFET devices are proposed to overcome the width quantization issue in FinFET. In recent years, many Underlapped FinFET devices were proposed to have better control of the SCEs in the sub-nanometer technologies. Underlap on either side of the gate increases effective channel length as seen by the charge carriers. Consequently, source-to-drain tunneling probability is improved. This overall increases the performance of the device. Hence, Underlapped FinFET based SRAMs has become a capable solution to a more robust and energy efficient SRAM cell design. There is another type of FinFET ie Design co optimized FinFET. DTCO_F follow the design rules released in kit. The PDK provides standard SRAM cell with special spacing rules and low leakages. PDK fins are 32nm in height, 6.5nm thick and 7nm in width. It is observed

that the n-type DTCO_F has a lower ION compared to the n-type UF. However, the DTCO_F offers a higher ION-IOFF ratio compared to the UF.

The results and their impact is discussed. Among different existing AUF devices, underlap FinFET device with DU=1.635nm and SU=1.09nm achieve maximum ION/IOFF ratio. With the selected AUF device, comparisons were done with optimized 1:5:2 configuration 6T and 8T SRAM designs in terms of performance, read stability and write ability. It is observed that 6T attains a 44.97% improvement in the read energy compared to 8T AUF SRAM. However, write energy of 6T AUF SRAM worsen by 3.16% compared to 8T AUF SRAM. From the analysis, the optimized 8T AUF SRAM design possesses high stability in ideal case and under process variation compared to the optimized 6T AUF SRAM design.

Moreover, the design of 6T SRAM for different configurations with AUF and DTCO FinFET is also done. It can be seen that the standby leakage power in the DTCO_F-SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations has improved by 31, 99 and 111.63 times compared to UF-SRAMs of the same configurations, respectively. Also, DTCO_F- SRAMs consume less power. Therefore, the DTCO_F devices are better for the low power SRAMs. However, the UF-SRAMs offer 1.03, 12.23 and 11.78 faster read times compared to the DTCO_F SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively. Therefore, the UF-SRAMs are more suitable for high-speed SRAMs. The UF-SRAMs have lower stability compared to the DTCO_F-SRAMs. The RSNM of the UF-SRAMs degraded by 83.353%, 28.61% and 28.45% for 1:1:1, 1:5:2 and 2:5:2 configurations. Moreover, from the combined information of SVNM and SINM it is confirmed that the read stability of the UF-SRAMs is worse than that of the DTCO_F-SRAMs. However, the UF-SRAMs have better write ability. The WSNM of the UF-

SRAMs has improved by 52.7%, 54.86% and 53.71% for 1:1:1, 1:5:2 and 2:5:2 configurations. From the combined information of WTV and WTI, we can conclude that the write ability of the UF-SRAMs is better than that of the DTCO_F-SRAMs. From the analysis, it can be concluded that Asymmetrical Underlapped FinFET is better for high speed applications and DTCO FinFET for low power applications. Hence, both FinFETs offers a promising direction for future applications for high performance and low power.

7.2 Direction of Future Research

In this thesis, AUF and DTCO FinFET based conventional 6T and 8T SRAM bitcell designs are presented. In the future, SRAM memory system comprising of 1MB SRAM bitcell array along with precharging circuit, row decoder, column decoder and sense amplifier can be designed with both AUF and DTCO FinFETs. Later, analysis can be done to benchmark these memory systems.

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VITA

Athiya Nizam is currently pursuing her master's degree in Electrical Engineering from University of Missouri Kansas City (UMKC), Kansas City, Missouri. Currently, she is working as a Graduate technical intern at Intel Corporation and graduate research assistant at Micro and Nano Electronics Lab, UMKC. She also worked as a summer intern at Marvell Semiconductor Inc. Her research interests include designing SRAM bit cell design at lower technology node with high performing device FinFET. Nizam was awarded with "Dean's international scholarship award" for Master program at UMKC and Graduate Assistant Fund fellowship by UMKC Women council. She has also published conferences in IEEE S3S and ANTS.

She received her B.E. degree in electrical and electronic engineering from Osmania University, Hyderabad, India.