NOVEL HIGH PERFORMANCE ULTRA LOW POWER STATIC RANDOM ACCESS MEMORIES (SRAMS) BASED ON NEXT GENERATION TECHNOLOGIES

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By

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NOVEL HIGH PERFORMANCE ULTRA LOW POWER STATIC RANDOM ACCESS MEMORIES (SRAMS) BASED ON NEXT GENERATION TECHNOLOGIES

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University of Missouri - Kansas City, 2019

ABSTRACT

Next Big Thing Is Surely Small: Nanotechnology Can Bring Revolution. Nanotechnology leads the world towards many new applications in various fields of computing, communication, defense, entertainment, medical, renewable energy and environment. These nanotechnology applications require an energy-efficient memory system to compute and process. Among all the memories, Static Random Access Memories (SRAMs) are high performance memories and occupies more than 50% of any design area. Therefore, it is critical to design high performance and energy-efficient SRAM design. Ultra low power and high speed applications require a new generation memory capable of operating at low power as well as low execution time. In this thesis, a novel 8T SRAM design is proposed that offers significantly faster access time and lowers energy consumption along with better read stability and write ability. The proposed design can be used in the conventional SRAM as well as in computationally intensive applications like neural networks and machine learning classifiers [1]-[4]. Novel 8T SRAM design offers higher energy efficiency, reliability, robustness and performance compared to the standard 6T and other existing 8T and 9T designs. It offers the advantages of a 10T SRAM without the additional area, delay and power overheads of the 10T SRAM. The proposed 8T SRAM would be able to overcome many other limitations of the conventional 6T and other 7T, 8T and 9T designs. The design employs single bitline for the

write operation, therefore the number of write drivers are reduced. The defining feature of the proposed 8T SRAM is its hybrid design, which is the combination of two techniques: (i) the utilization of single-ended bitline and (ii) the utilization of virtual ground. The single-ended bitline technique ensures separate read and write operations, which eventually reduces the delay and power consumption during the read and write operations. It's independent read and write paths allow the use of the minimum sized access transistors and aid in a disturb-free read operation. The virtual ground weakens the positive feedback in the SRAM cell and improves its write ability. The virtual ground technique is also used to reduce leakages. The proposed design does not require precharging the bitlines for the read operation, which reduces the area and power overheads of the memory system by eliminating the precharging circuit. The design isolates the storage node from the read path, which improves the read stability. For reliability study, we have investigated the static noise margin (SNM) of the proposed 8T SRAM, for which, we have used two methods – (i) the traditional SNM method with the butterfly curve, (ii) the N-curve method A comparative analysis is performed between the proposed and the existing SRAM designs in terms of area, total power consumption during the read and write operations, and stability and reliability. All these advantages make the proposed 8T SRAM design an ideal candidate for the conventional and computationally intensive applications like machine learning classifier and deep learning neural network.

In addition to this, there is need for next generation technologies to design SRAM memory because the conventional CMOS technology is approaching its physical and performance boundaries and as a consequence, becoming incompatible with ultra-low-power applications. Emerging devices such as Tunnel Field Effect Transistor (TFET)) and Graphene Nanoribbon Field Effect Transistor (GNRFET) devices are highly potential candidates to overcome the

limitations of MOSFET because of their ability to achieve subthreshold slopes below 60 mV/decade and very low leakage currents [6]-[9]. This research also explores novel TFET and GNRFET based 6T SRAM. The thesis evaluates the standby leakage power in the Tunnel FET (TFET) based 6T SRAM cell for different pull-up, pull-down, and pass-gate transistors ratios (PU: PD: PG) and compared to 10nm FinFET based 6T SRAM designs. It is observed that the 10nm TFET based SRAMs have 107.57%, 163.64%, and 140.44% less standby leakage power compared to the 10nm FinFET based SRAMs when the PU: PD: PG ratios are 1:1:1, 1:5:2 and 2:5:2, respectively. The thesis also presents an analysis of the stability and reliability of sub-10nm TFET based 6T SRAM circuit with a reduced supply voltage of 500mV. The static noise margin (SNM), which is a critical measure of SRAM stability and reliability, is determined for hold, read and write operations of the 6T TFET SRAM cell. The robustness of the optimized TFET based 6T SRAM circuit is also evaluated at different supply voltages. Simulations were done in HSPICE and Cadence tools. From the analysis, it is clear that the main advantage of the TFET based SRAM would be the significant improvement in terms of leakage or standby power consumption. Compared to the FinFET based SRAM the standby leakage power of the T-SRAMs are 107.57%, 163.64%, and 140.44% less for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively. Since leakage/standby power is the primary source of power consumption in the SRAM, and the overall system energy efficiency depends on SRAM power consumption, TFET based SRAM would lead to massive improvement of the energy efficiency of the system. Therefore, T-SRAMs are more suitable for ultra-low power applications.

In addition to this, the thesis evaluates the standby leakage power of types of Graphene Nanoribbon FETs based 6T SRAM bitcell and compared to 10nm FinFET based 6T SRAM bitcell. It is observed that the 10nm MOS type GNRFET based SRAMs have 16.43 times less

standby leakage power compared to the 10nm FinFET based SRAMs. The double gate SB-GNRFET based SRAM consumes 1.35E+03 times less energy compared to the 10nm FinFET based SRAM during write. However, during read double gate SB-GNRFET based SRAM consume 15 times more energy than FinFET based SRAM. It is also observed that GNRFET based SRAMs are more stable and reliable than FinFET based SRAM.

APPROVAL PAGE

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CHAPTER 1

INTRODUCTION

"Minute Things with Great Supremacy: Nanotechnology can Bring Revolution." Nanotechnology leads the world towards many new applications in various fields of computing, communication, defense, entertainment, medical, renewable energy and environment. Nanotechnology in healthcare has the potential to change medical science intensely. These nanotechnology applications require energy efficient memory system to compute and process. Among all the memories, Static Random Access Memories (SRAMs) are high performance memories and occupies more than 50% of any design area [6]. Therefore, it is critical to design high performance and energy-efficient SRAM design.

1.1 SRAM Current Market and Applications

In 2013, Cypress commitment to the SRAM market (refer Table 1) with investments in new product development for next generation of high-performance synchronous SRAMs to extend the architecture. In 2012, Cypress acquired Ramtron to add F-RAM (ferroelectric RAM) products to Cypress nvSRAM (nonvolatile SRAM) products, giving Cypress the market's leading RAM portfolio. The following table summarizes the markets and applications related to Cypress products in this segment:

Table 1: Cypress SRAM market and applications

Markets	Applications
Consumer, networking, industrial	Consumer electronics, switches and routers, test equipment, automotive and industrial electronics.
Base station, networking	Enterprise routers and switches, wireless base stations, high bandwidth applications and industrial and defense electronics.
Servers, industrial	Redundant array of independent disk (RAID) servers, point of sale terminals, set-top boxes, copiers, industrial automation, printers, single-board computers and gaming.

SRAM finds its application in many biomedical fields. For instance, medical imaging is the practice of generating visual images of the inner body for medical examination of some organs or tissues. It finds hidden structures below the skin and bones and diagnose the disease. Medical imaging also has a record of normal anatomy to differentiate and identify abnormalities. It incorporates radiology which utilizes the imaging technologies (X-ray radiography, magnetic resonance imaging, ultrasound, etc.) Until 2010, 5 billion medical imaging studies had been conducted worldwide. These imaging devices require a huge amount of memory to keep the database and to do the computation to identify abnormalities. These applications require a new generation emerging technologies based memory, which is capable to operate at low power, as well as has very little execution time. The purpose of this research is to design Novel Static Random Access Memory (SRAM) based on Emerging technologies for high speed and ultra low power applications.

Another interesting application of SRAMs is Machine Learning (ML). ML is a very computationally intensive way to study and scrutinize huge amounts of information and data to identify different trends and behavioral patterns. Machine-learning models are complex and require high milli-joules of energy per decision. Machine learning inference can be broken down to feature extraction and classification. From the available dataset, features and sets of weight can be learned. In this way, a complete system is trained or learned. Deep neural networks (DNN) or deep learning use these learned features. DNN is a widespread procedure of machine learning. It gives better accuracy by mapping input to a high-dimensional space. For instance, a convoluted neural network (AlexNet), which is a deep learning neural network for image classification. SRAM has a vital role in modern deep learning applications, which require intensive memory access. AlexNet uses SRAM for neuron computation that involves numerous memory read and write operations to support very large amounts of data to be read from the memory for each neuron computation. AlexNet is comprised of eleven layers. The most computationally intensive layers are five convolution layers and two fully connected layers. In addition to this, AlexNet has three max pooling layers and one soft-max output layer. In the convolution layer, the input of each neuron is dependent on the convolution of the neuron in the previous layer's sliding window along with the convolution weight summed with bias. For each neuron in a fully connected layer, its input is the sum of the products of each neuron in the previous layer with the network weight plus bias. Initially, information of the neurons and their related weight and bias are read from the memory. This is followed by the multiplication and accumulation (MAC) operation. The outcome of the MAC is forwarded to the non-linear function σ, which is realized using the look-up table [1]-[4]. Finally, the output of the neuron is written back into the memory again. During these steps, an enormous amount of data is read

from the SRAM for the computation of each neuron. In the case of the convolution layer, the size of the sliding window can be as high as 11x11. In addition to this, a corresponding weight and bias are also read from the SRAM. However, for fully the connected layer, the output of all the neurons from the previous layer should be read, which nearly total 4096 in number are for the AlexNet. Along with the neurons, their corresponding network weights and biases should also be read from the SRAM. Special attention should be given to lower the delay, power consumption, and variation of the SRAM for the deep learning applications, where the data processing speed is a crucial aspect. The run time of the algorithm depends heavily on the SRAM speed. Therefore, the SRAM access time, energy efficiency and reliability are very critical for deep learning neural networks.

In order to lower power consumption and reduce memory accessing time, recent works have improved the machine learning classifier architectures. The modified architectures integrate the computation into the memory itself. In previous designs, data storage and computation are combined in a conventional 6T SRAM array, where a 5-bit feature vector is used to drive the word-line (WL). The bitcells store the binary weights (± 1). The bitcell current is the product of the value of the feature vector and the weight stored in the bitcell. The currents in the column sum to the bitline (BL or BLB) as shown in Figure 1. However, the conventional 6T SRAM bitcell is highly vulnerable to read upset. Since the stability and the reliability of the conventional 6T SRAM is low, there is a high probability of reading the wrong value and the overall performance and reliability of the entire in-memory classifier (Conventional 6T SRAM array) scheme of Figure 1 will be reduced. The proposed 8T SRAM is expected to be a better candidate for both the machine learning classifier and deep neural networks, because it would provide high speed access, low power consumption, and higher robustness. These benefits of the proposed 8T

SRAM compared to the conventional 6T, conventional 8T and other existing 7T, 8T, 9T, and 10T designs for these types of computationally intensive applications will be clear in the subsequent chapters.

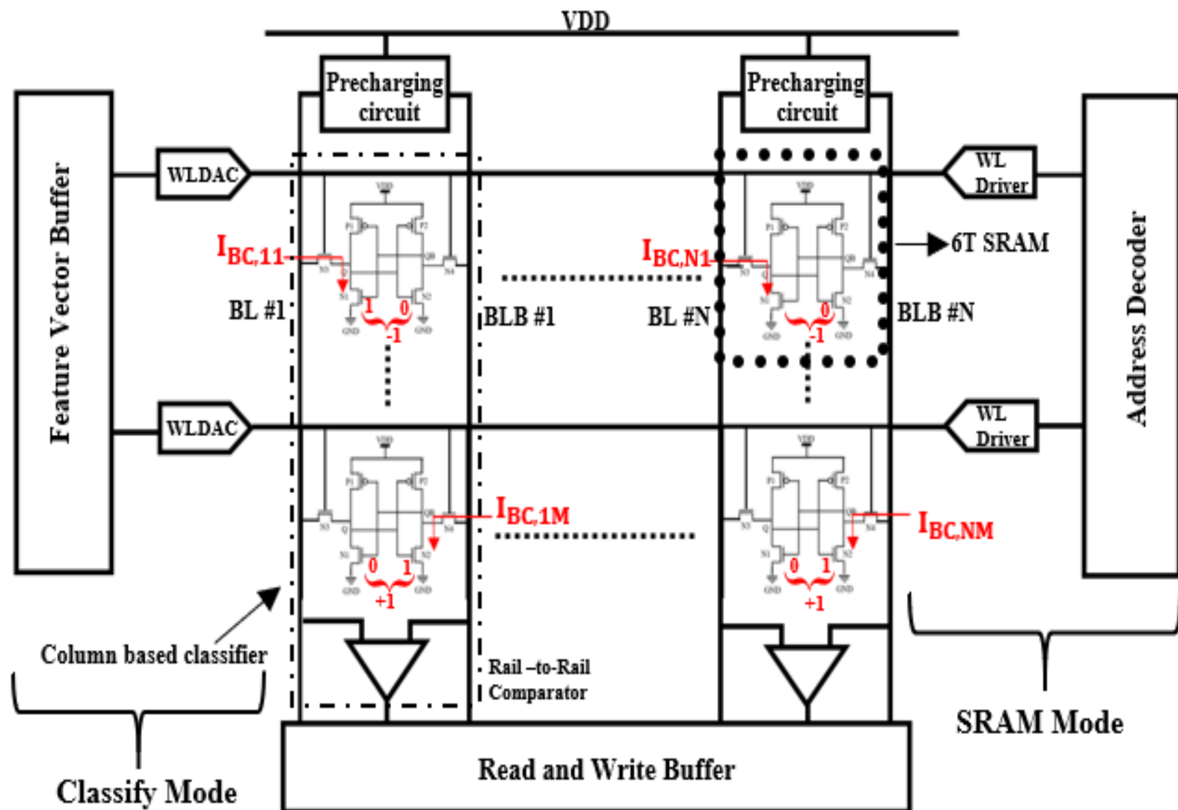


Figure 1: In-memory classifier (Conventional 6T SRAM array) architecture with two modes of operation and column-based classifiers.

1.2 Limitation of existing SRAM designs

The conventional 6T SRAM cell has been the industry standard from the beginning of the SRAM era. Reliable read and write operations are the key considerations in SRAM design. Due to the simplicity and symmetry of the 6T SRAM cell circuit, it is very area efficient. However, special attention should be given for properly sizing the transistors to avoid read and write upsets,

because the design is based on strict sizing ratios among the six transistors to ensure a stable read and write operations. In the conventional 6T SRAM, two bitlines are used to store and read the data. In the two bitline architecture of the 6T cell, the bitlines are not electrically separate from the storage nodes during the read and write operations. This leads to inadvertent toggling of data stored in the cross-coupled inverter during the read operation. This increases the chance of errors known as read upset. Apart from this, during the read operation, the voltage of the storage node with logic "0" increases to a certain value based on the voltage division between the access and the pull-down transistors. An increase in the voltage at the storage node with logic "0" leads to a decrease in the voltage of the storage node with logic "1" because of the positive feedback characteristic. However, this enhancement in the voltage cannot flip the data of the cell. Therefore, the read operation is done successfully. However, the write operation requires a strong access transistor to write the data. The write ability of the cell is reduced if the minimum size access transistors are used. This challenge is referred as the read and write access transistor sizing conflict. Besides, the 6T SRAM cell fails to operate in low-power and ultra-low-power (subthreshold) regions because of the precharging requirement during its operation, process variation, reduced voltage level, and lower noise margin. As improvements over the conventional 6T SRAM cell, many designs of 7T, 8T, 9T, and 10T SRAM cells have been proposed. These designs use different techniques to improve the functionality and the stability of the SRAM cell. Some of these techniques are (i) using a separate read mechanism, (ii) feedback cutting, (iii) asymmetric design, and (iv) one-sided access.

1.3 Problem Statement

Ultra low power and high speed applications require a new generation memory capable to operate at low power as well as has very less execution time. However, the conventional CMOS

technology is approaching its physical and performance boundaries and consequently, becoming incompatible with ultra-low-power applications. Emerging devices such as Tunnel Field Effect Transistor (TFET), Fin Field Effect Transistor (FinFET) and Graphene Nanoribbon Field Effect Transistor (GNRFET) devices are highly potential candidates to overcome the limitations of MOSFET because of their ability to achieve subthreshold slopes below 60 mV/decade and very low leakage currents [6]. In addition to this, scaling of technology have increased serious challenges like the short channel effects (SCEs) in the bulk CMOS devices. Emerging technologies offers better gate control, higher ION, better scalability and therefore, improved performance and reliability compared to the conventional CMOS designs. For energy efficient circuit design moving to emerging technology platform would be a very promising option. Further improvements in system power consumption can be achieved through circuit optimization. Especially for SRAM, which occupies up to 70% of the total die area and imposes the majority of the power consumption, circuit-level optimization would lead to huge gains regarding energy efficiency, performance, and reliability.

Current interconnect technology (metal wire and low-κ dielectric) is approaching its fundamental physical and material limits, beyond which it can no longer support the signal communication bandwidth required at nanoscale under increased thermal, power and noise constraints. Hence a new SRAM memory system design is required to replace the conventional memory system design. The existing Standard 6T SRAM system uses two bit lines (BLs) and one word line (WL) for the read and write operations. During read operation for the existing design precharging circuit is used to charge bitlines high. Then read operation is carried out. Total time required for read operation in existing memory design include precharging time, cell access time, sense amplifier time and read output time. The proposed memory system does not

require precharging during read operation. Therefore, the total time of the memory system, as well as the area of the memory system, is reduced. In addition to this, the total power consumption of the proposed memory system is also reduced.

In this thesis, we propose a novel Static Random access Memory System which eliminates the precharge circuit and there is no need to precharge the BLs before the read operation. Therefore, significant savings of power consumption can be achieved. This is a huge improvement over the existing Static Random Access Memory designs, which needs to precharge all the BLs every time irrespective of whether a read operation is performed or not.

1.4 Why emerging technologies?

Continuous scaling of semiconductor devices have increased short-channel effects, reduced gate control, exponentially increase in leakage currents and severe process variations. From the past three decades, conventional CMOS technology is approaching its physical and performance boundaries and as a consequence, becoming incompatible with ultra-low-power applications. The exponential increase in the number of transistors has increased the total power consumption of the modern hardware. Limiting supply voltage is an efficient method to lower the power consumption because it decreases the dynamic power in quadratic order and the standby leakage power in linear order. However, lower supply voltage dictates reducing the threshold voltage (V_{TH}), which leads to the exponential increase of the I_{OFF} in the conventional MOSFET circuits. Also, the fundamental thermionic limit of 60 mV/decade for the subthreshold swing of the MOSFET devices restricts the supply voltage scaling and achievable I_{ON}/I_{OFF} ratio. Tunnel Fiedl Effect Transistors (TFET) devices are promising for ultra-low-power applications because of the ability to achieve subthreshold slopes below 60 mV/decade and low leakage currents. Tunnel

FET (TFET) devices are highly potential candidates to overcome the limitations of CMOS/MOSFET because of the ability of TFET to achieve subthreshold slopes below 60 mV/decade and very low leakage currents [5]-[15]. Moreover, scaling related challenges like the short channel effects (SCEs) in the bulk CMOS devices have led to the introduction of the Fin Field Effect Transistors (FinFETs). FinFET offers better gate control, higher I_{ON}, better scalability and therefore, improved performance and reliability compared to the conventional CMOS designs. Among the double gate devices, the quasiplanar FinFET structure gained considerable attention because of the ease of the fabrication process [7].

In addition to these technologies, Carbon based field effect transistors (FETs) have appeared as the promising next-generation devices because of their exceptional electrical properties. Moreover, these devices have good integration capabilities through new fabrication techniques [1]–[3]. Most widely researched carbon based FETs are carbon nanotube FETs (CNFETs) and graphene nanoribbon FETs (GNRFETs). In contrast to CNTs, GNRs are developed through silicon- compatible, transfer-free, and in situ process [20, 22, 23]. Therefore, GNR based circuit designs have no alignment and transfer-related problems as experienced by CNT-based circuits. In order to design energy efficient system, moving to GNR technology platform would be a very promising option. Particularly for static random access memories (SRAMs), which occupies more than 50% of the total die area and imposes the majority of the power consumption. Since fabrication expertise of GNRFETs based SRAM is still at initial phase, SRAM bitcell designing has been playing a significant role for evaluating futuristic graphene based SRAM designs.

Most of the electronics and digital designs overall performance is heavily dependent on the memory. Static Random Access Memory (SRAM) occupies more than 50% of the total die area

and imposes the majority of the power consumption [24], [25]. For energy efficient circuit design moving to these emerging technologies would be a very promising option.

CHAPTER 2

BACKGROUND

Exponential increase in number of transistors, have increased the density and the total power consumption of the system. Moreover, the scaling of technology have degraded the performance of CMOS designs because of the short channel effects (SCEs). In sub nanometer technologies, emerging technologies have better gate control and therefore, achieves better performance than CMOS designs. In addition to this, these devices possess high ION and better scalability in contrast to bulk CMOS [1] - [3]. Therefore, it is necessary to optimize the SRAM bitcell for better performance, read stability and write ability [5]. This chapter provides detail dicussion on different emerging technologies. In addition to this, the chapter provides a brief background of the existing SRAM cell designs. Multiple groups proposed many SRAM designs that utilizie different transistor count per SRAM bitcell. Consequently, depending upon the transisitor count these cells are known as 6T, 7T, 8T, 9T and 10T cells. In the next few subchapters, we briefly discussed the most widely investigated SRAM cells from each research group.

2.1 Tunnel field effect transistor (TFET)

TFET devices are promising for ultra-low-power applications because of the ability to achieve subthreshold slopes below 60 mV/decade and low leakage currents. Tunnel FET (TFET) devices are highly potential candidates to overcome the limitations of CMOS/MOSFET because of the ability of TFET to achieve subthreshold slopes below 60 mV/decade and very low leakage

currents [5], [7]. Many different TFET designs based on the conventional and emerging technologies have been proposed. However, some of the fabricated group III-V materials based TFETs have gained more attention because of the compositional variety of the tunable tunneling-barrier heights and potential feasibility to be integrated into the current and emerging application systems.

Table 2 provides a summary of the n-type group III-V materials based TFETs [8], [9]. For energy efficient circuit design moving to TFET technology platform would be a very promising option. Further improvements in system power consumption can be achieved through circuit optimization. Especially for SRAM, which occupies up to 70% of the total die area and imposes the majority of the power consumption, circuit-level optimization would lead to huge gains regarding energy efficiency, performance, and reliability.

Among the available TFET devices, GaSb/InAs heterojunction TFET (Hetro-j TFET) is an outstanding choice due to its broken-gap band alignment, which leads to large drive current [11]. In [12], vertical double-gate GaSb–InAs source-underlapped n-TFET and p-TFET are proposed. The source of the n-TFET is underlapped with n^+ InAs layer as shown in Figure 2. Whereas, the source of the p-TFET is underlapped with p^+ GaSb layer as shown in Figure 3. These devices have vertical architecture and are more promising than the lateral devices in the sub-10 nm domain because of the channel length scaling issues [13]. Underlapped Hetro-j TFET has better characteristics than the conventional non-underlapped Hetro-j TFET. For the gate voltage swing of 500mV, I_{OFF} and I_{ON} of the 10nm underlapped and non-underlapped n-TFETs are 0.3 nA/µm and 0.9 nA/µm. However, I_{ON} of both the underlapped and non-underlapped n-TFETs are 235 µA/µm for the same gate voltage swing. The 10nm underlapped p-TFET has even better characteristics in contrast to the conventional p-TFET. I_{OFF} of the p-TFET is 1.5 nA/µm, which is 66.66 times less than I_{OFF} of the traditional p-TFET (100 nA/µm). I_{ON} of the underlapped and

non-underlapped p-TFETs are 210 µA/µm for the same gate voltage swing [12]. Based on low I_{OFF} characteristic, the underlapped TFETs are better for designing the SRAM circuit [12], [14] and [20].

Table 2: Benchmarking of existing TFET technologies [8], [9].

Reference	**Source-Channel Material**	**EOT (nm)**	$V_{ON} - V_{OFF}$	$\frac{I_{ON}}{I_{OFF}}$	S_{MIN} (mV/dec)	S_{EFF} (mV/dec)
Zhou [7]	GaSb-InAs	1.3	1.5	6000	200	400
Zhou [8]	InP-InGaAs	1.3	1.75	45000	93	310
Mohata [9]	GaAsSb-InGaAs	1.75	1.5	17000	230	350
Zhao [10]	In0.7Ga0.3As	1.2	2	200000	84	380
Li [11]	AlGaSb-InAs	1.6	1.5	1600	125	470
Dewey [12]	In0.53Ga0.47As	1.1	0.9	70000	58	190

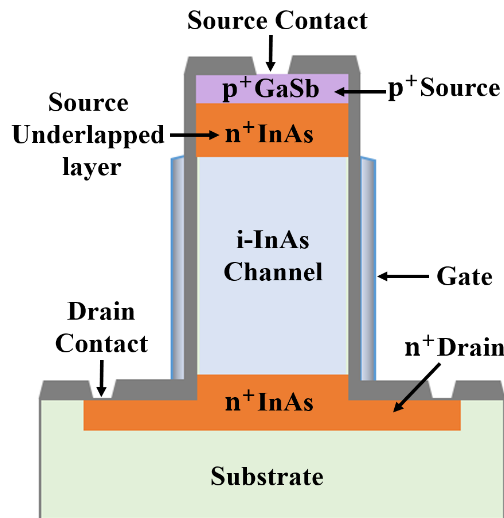


Figure 2: n-TFET device having n^+- doped underlap layer of InAs between source and channel.

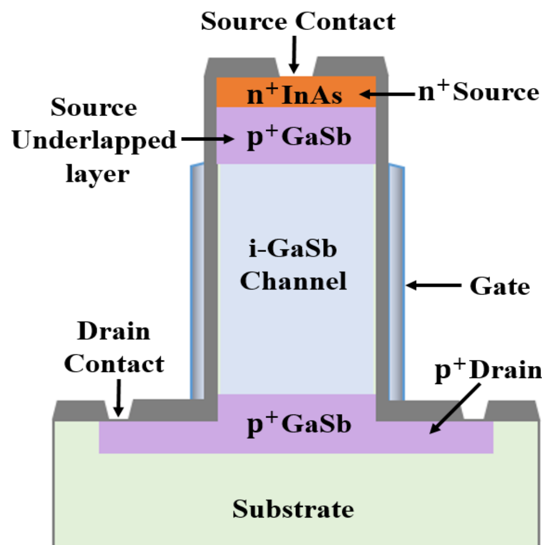


Figure 3: p-TFET device having n^+- doped underlap layer of GaSb between source and channel.

2.2 Graphene NanoRibbon FET (GNRFET)

Graphene is a single atomic layer of graphite with honeycomb crystal lattice. A two-dimensional graphene sheet has zero band gap and behave as metallic, which can not be turned ON or OFF. Graphene is patterned into one-dimension graphene nano-ribbons (GNRs) with widths less than 10 nm, to open the energy gap and make graphene a good semiconductor. Band

gap of a GNR is inversely proportional to the width (W_{CH}), which is dependent on the number of dimer lines (N), where $W_{CH} = (N + 1).\sqrt{3}\times 0.144/2$ nm [23], [24]. The band structure of GNRs gradually returns to 2D graphene sheet with the increase in the width of GNR. Based on the edge geometry, GNRs are classified in two types: (a) Armchair-GNR (AGNR) and (b) Zigzag-GNR (ZGNR). Band gap in AGNR gradually decreases with the increases in N. For $N = 3p$ and $= 3p + 1$ $(p \in N)$, the band gap is finite and GNR behave as semiconductor. For $N = 3p + 2$, the band gap is negligible and GNR behave as metal. In ZGNR, GNR shows metallic properties when the edges are pristine. The band gap in ZGNR can be opened with rough edges or passivating with hydrogen atoms [36], [38]. For this work, we designed SRAM cell based on double gate SB-GNRFET with armchair edge geometry as shown in Figure 4.

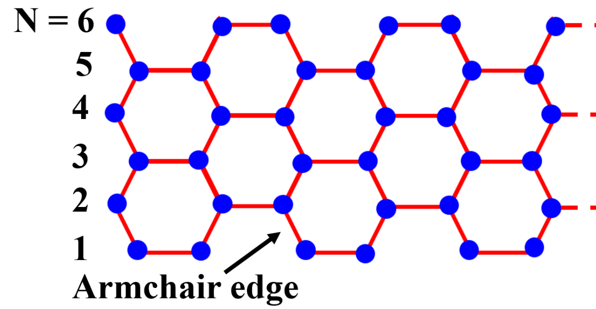
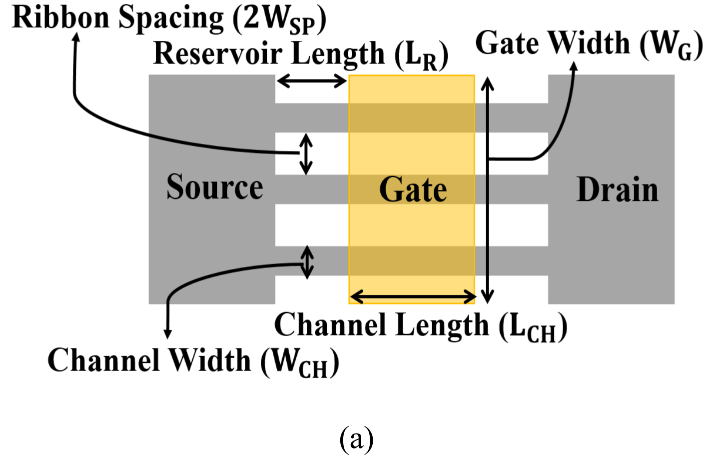


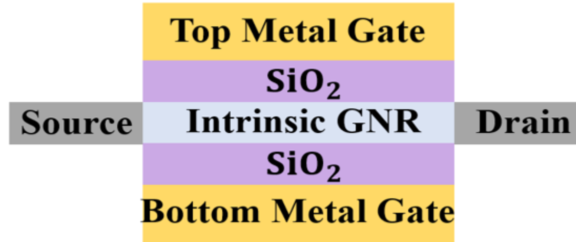
Figure 4: Lattice structure of an AGNR with $N = 6$ [23], [24].

There are two types of GNRFETs: (a) SB-type and (b) MOS-type. In MOS-GNRFETs, the channel and the reservoirs (drain, source) are made of graphene. The reservoirs are heavily-doped with donors (acceptors), resulting in an N-type (P-type) GNRFET. In MOS-GNRFETs, the current is dominated by electron or hole conduction, depending on the doping of reservoirs. Whereas, in SB-GNRFET the drain and source are metal and the channel is made of graphene, which result in Schottky barriers at the graphene-metal junctions [23], [24]. SB-GNRFET have an ambipolar I-V curve with minimum current at $V_{GS} = 1/2V_{DS}$ [31], [32]. Multiple GNRs are

connected paralled in GNRFET to improve the drive strength of the device. Undoped GNR segments are placed below the gate, whereas heavily doped GNR segments are placed between the gate and the source/drain terminals. Reservoirs are the doped regions whereas the intrinsic region represents the channel as shown in Figure 5(a) and Figure 5(b).



(a)



(b)

Figure 5: (a) Top view (b) Cross-section of GNRFET device.

2.2.1 Schottky barrier type GNRFET (SB-GNRFET)

In SB-GNRFET, the Schottky barrier is present on the interface of metal and graphene. The charge transport mainly due to tunneling phenomenon through the barriers instead of thermionic conduction. The Schottky barrier profile near the interface have an exponential form of $E_{SB}(z) = \Phi_{SB} \times e^{-z/\lambda_{SB}}$, where the z-axis is the channel direction, Φ_{SB} is the barrier height and λ_{SB} is the scale length, as shown in Figure 3. At mid-gap, $\Phi_{SB} = {}^{1}/_{2}\, E_g$, where E_g is the band gap.

Tunneling phenonmenon is derived by the transmission probability $T(E)$ of the carrier as shown in equation (1), based on Wentzel-Kramers-Brillouin approximation.

$$T(E) = \begin{cases} e^{-2\int_{z_1}^{z_2} \sqrt{(2M_\alpha/h^2)(E_{SB}(z)-E)dz}} , & E \leq \Phi_{SB} \\ 1 , & E > \Phi_{SB} \end{cases} \tag{1}$$

where M_α is the effective mass, h is the reduced Planck's constant, z_1 and z_2 are the classical turning points [33]. $T(E)$ becomes unity if the carrier has higher energy than Φ_{SB}. Figure 6 shows Schottky barrier profile and transmission probability. The channel direction is represented as *z*-axis and energy (*E*) on the other axis. *EF* is the Fermi level on the source side and *EC* is the conduction band edge. Φ_{SB} is the SB height, while $\Phi_{SB,eff}$ is the effective SB height after approximation, with the red-shaded area being the SB profile after approximation. λ_{SB} is the scale length of the exponential SB profile and d_{SB} is the effective SB thickness.

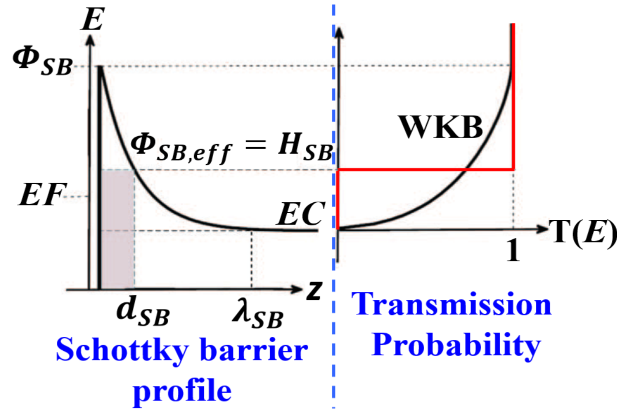


Figure 6: Schottky barrier profile and transmission probability of GNRFET.

The channel charge (Q_{CH}) of SB-GNRFET is derived from the electron density n_α and hole density p_α of each sub-band α coming from the drain (D) and the source (S) as shown in equation (2).

$$Q_{CH} = \frac{qL_{CH}}{2}\sum_{\alpha}[-n_{\alpha,S} + p_{\alpha,S} - n_{\alpha,D} + p_{\alpha,S}] \quad (2)$$

Figure 7 is the equivalent SPICE circuit of GNRFET model with three parallel GNRs. Each GNR is represented as transistor. Fringing fields between the gate and the reservoirs introduces two parasitic capacitances (C_{GD} and C_{GS}) given by equation (3).

$$C_{G,D} = C_{G,S} = 1.26\times10^{-10}W_G(0.8 - 0.2T_{OX} + 0.015T_{OX}^2) \quad (3)$$

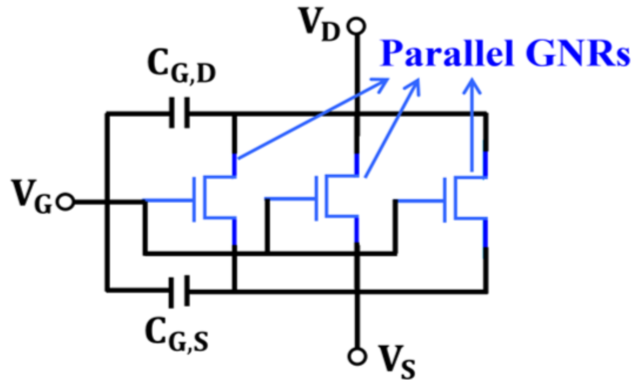


Figure 7: SPICE equivalent circuit ofSB type GNRFET device.

2.2.2 MOSFET type GNRFET (MOS-GNRFET)

The device structure of MOSFET-type GNRFET is shown in Figure 8. Multiple GNRs are connected paralled in GNRFET to improve the drive strength of the device. The ribbons have armchair chirality. Undoped GNR segments are placed below the gate, whereas heavily doped

GNR segments with doping fraction (f_{dop}) are placed between the gate and the source/drain terminals. Doped regions are called reservoirs whereas the intrinsic region represents the channel. The channel charge (Q_{CH}) of GNRFET is obtained by analyzing the band diagram. The equivalent SPICE circuit of GNRFET model with three parallel GNRs is shown in Figure 9. Each GNR is represented as transistor. Fringing fields between the gate and the reservoirs introduces two parasitic capacitances (C_{GD} and C_{GS}) given by equation (2).

$$C_{GD} = C_{GS} = 1.26\times10^{-10} W_G (0.8 - 0.2T_{OX} + 0.015T_{OX}^2) \quad (2)$$

Where W_G is the gate width and T_{OX} is the gate oxide thickness.

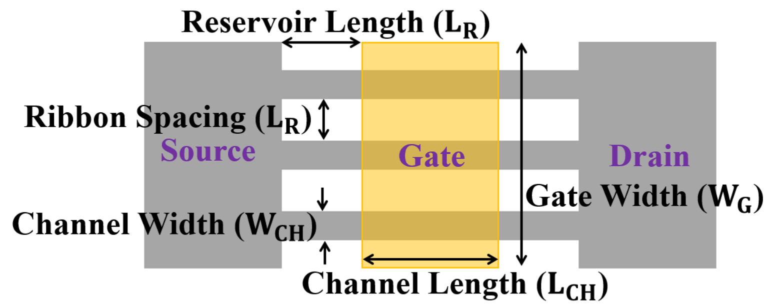


Figure 8: Cross-section of MOS type GNRFET device [23], [24].

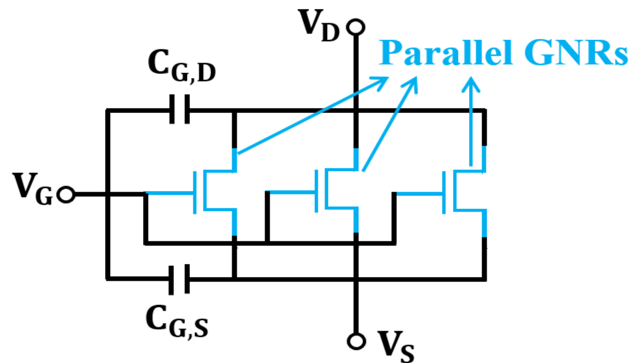


Figure 9: SPICE equivalent circuit of MOS type GNRFET device.

Figure 10 shows the band diagram of GNRFET for $V_{GS} > 0$ and $V_{DS} > 0$. Fermi levels at the source (E_{FS}) and the drain (E_{FD}) are both above the conduction band because the source and the drain are heavily doped and have high electron densities. When V_{DS} is low, few holes are available in the channel. But when V_{DS} increases, the conduction band on the drain side ($E_{C,D}$) goes below the valence band of the channel ($E_{V,CH}$), and holes tunnel from the drain into the channel. Channel charge (Q_{CH}) is determined by aggregating electron and hole densities and multiplying by electron charge(q). The channel potential (Ψ_{CH}) is negative of intrinsic energy level(E_i). Hence, the conduction band is $E_C = \varepsilon_\alpha - q\Psi_{CH}$ and the valence band is $E_V = -\varepsilon_\alpha - q\Psi_{CH}$. In addition to this, Fermi level at source/drain equals to applied voltage. Therefore,$E_{FS} - E_C = -qV_S - (\varepsilon_\alpha - q\Psi_{CH})$. The final expression of Q_{CH} is given by equation (4).

$$Q_{CH} = \frac{qL_{CH}}{2}\sum_{\alpha}[-n_\alpha(q\Psi_{CH} - \varepsilon_\alpha - qV_S) - n_\alpha(q\Psi_{CH} - \varepsilon_\alpha - qV_D) + T_r(\Psi_{CH,D}) \cdot p_\alpha(qV_D - q\Psi_{CH} - \varepsilon_\alpha)] \quad (4)$$

Where L_{CH} is channel length, n_α is electron density, p_α is hole density, ε_α is subband edge, α is subband index and $T_r(\Psi_{CH,D})$ is tunneling probability.

The I-V characteristics of GNRFET is shown in Figure 11, for V_{GS} and V_{DS} varrying from 0 to 800mV. Moreover, Figure 6 validates fabricated GNRFET model against the numerical simulations in NanoTCAD ViDES. I_{ON}-I_{OFF} ratio reduces at higher V_{DS}, because Ψ_{CH} increases at higher V_{DS}. This act as a protocol for choosing supply voltage. Maximum I_{ON}-I_{OFF} ratio and higher subthreshold swing are achieved at 500mV supply voltage. Therefore, 500mV supply is opted for designing SRAM bitcell.

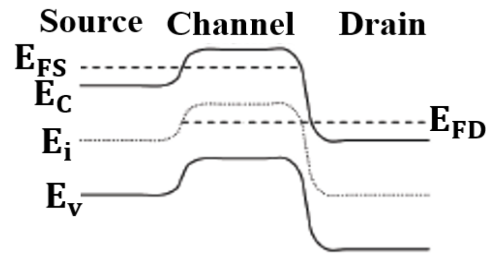


Figure 10: Band diagram of MOS-GNRFET[23], [24].

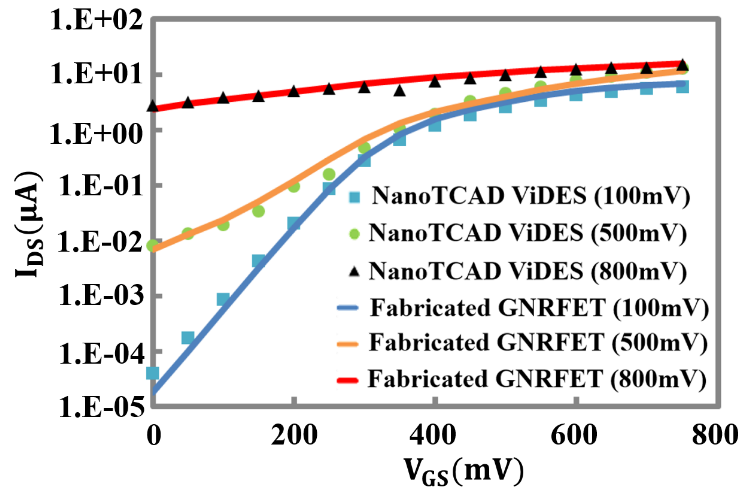


Figure 11: I-V characteristics of GNRFET devices [23], [24].

2.3 Existing SRAM designs

This section provides a brief background of the existing SRAM cell designs.

2.3.1 Conventional 6T SRAM

The conventional 6T SRAM cell as shown in Figure 12 has been the industry standard from the beginning of the SRAM era. Reliable read and write operations are the key consideration in SRAM design. Due to the simplicity and symmetry of the 6T SRAM cell circuit it is very area efficient. However, special attention should be given for properly sizing the transistors to avoid read and write upsets, because the design is based on ratioed logic principle that requires strict

sizing ratios to ensure stable read and write operation. In the conventional 6T SRAM, two bit lines are used to store the data. The two BL architecture in 6T cell makes inadvertent toggling during read operation for cross coupled inverter. This increase the chances of errors during read operation. Besides, 6T SRAM cell fails to operate in the subthreshold region because of the process variation and reduced voltage level. Therefore, 6T SRAM cell is not suitable for ultra-low-power circuits that would be operated in the subthreshold region.

As improvements over the conventional 6T SRAM cell, many designs of 8T, 9T and l0T SRAM cells have been proposed. These designs use different techniques to improve the functionality and stability of SRAM cell. Some of these techniques are (i) using separate read mechanism, (ii) feedback cutting, (iii) asymmetric design, and (iv) one-sided access [46]-[52].

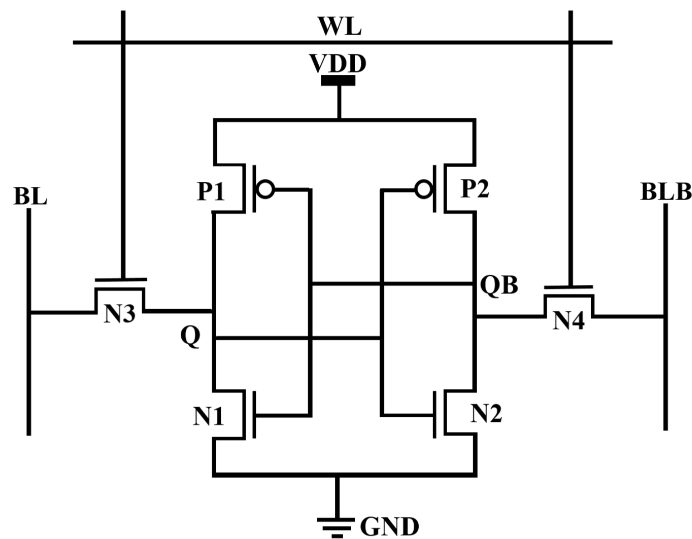


Figure 12: Conventional 6T SRAM bitcell.

2.3.2 Conventional 8T SRAM

In 8T SRAM as shown in Figure 13, there are two additional stack transistors that provide the access to the cell through the additional read bit-line (RBL). It has two dedicated word-lines (WWL and RWL). Everything else is similar to the standard 6T SRAM. The reading operation

of this 8T SRAM is separated from the rest of the cell, which increases the read static noise margin (RSNM). Higher noise margin ensures better read stability and robustness. The read operation of 8T SRAM does not disturb the storage data of cell. However, 6T SRAM is vulnerable to read upset, because in 6T the access transistor pulls the “0” storage node above the ground, which degrades the SNM.

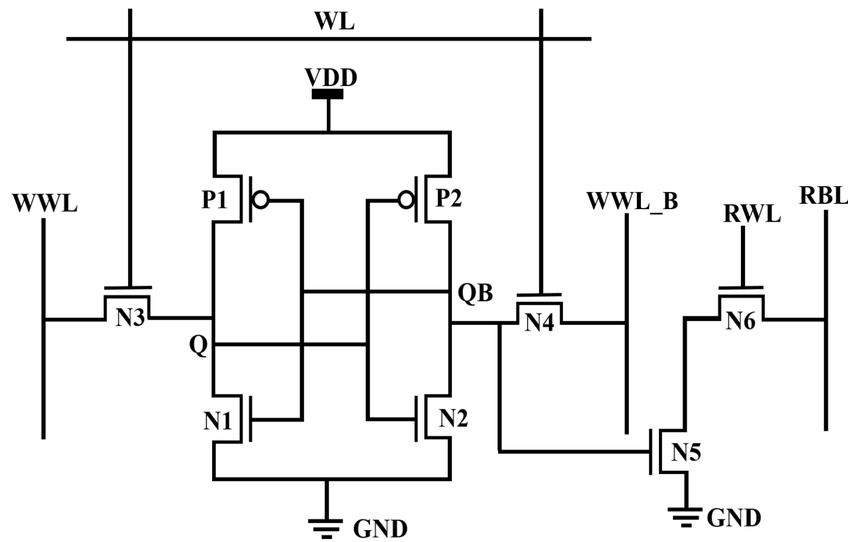


Figure 13: Conventional 8T SRAM bitcell.

The performance of 8T SRAM during the read operation is determined by the strength of the read stack transistors. To improve the read stability of 6T SRAM cell both halves of the cells should be enlarged. But in 8T SRAM, the read stability can be improved by increasing the size of the stack transistors only. However, the design of this 8T SRAM cell is still ratioed and its write operation is still similar to the conventional 6T SRAM.

2.3.3 9T SF-SRAM

There are several designs that utilize 9 transistors per cell. One of the most widely investigated 9T SRAM cell is the 9T Supply-Feedback SRAM (9T SF-SRAM) as shown in Figure 14, which consists of an addition supply gating transistor (M9) compared to the 8T SRAM

cell described above. Everything else is similar to the 8T SRAM. To increase the write ability, 9T SRAM employs supply feedback approach. This approach is executed by connecting M9 in the feedback loop with the storage node (Q).

This weakens the pull up path of the cell during the write operation. As a consequence, flipping of the cell data is much easier during the write operation. Moreover, the internal gating generates a small voltage drop at the drain of M9 during the hold stage. This results in lower leakage currents at the expense of the reduction in hold static noise margin (HSNM). Besides, the extra transistor (M9) increases the area and reading time. Power consumption of 9T SRAM is also higher than the previous designs. Also, due to the asymmetric circuit construction, the complexity and area consumption of this design would be much higher [10].

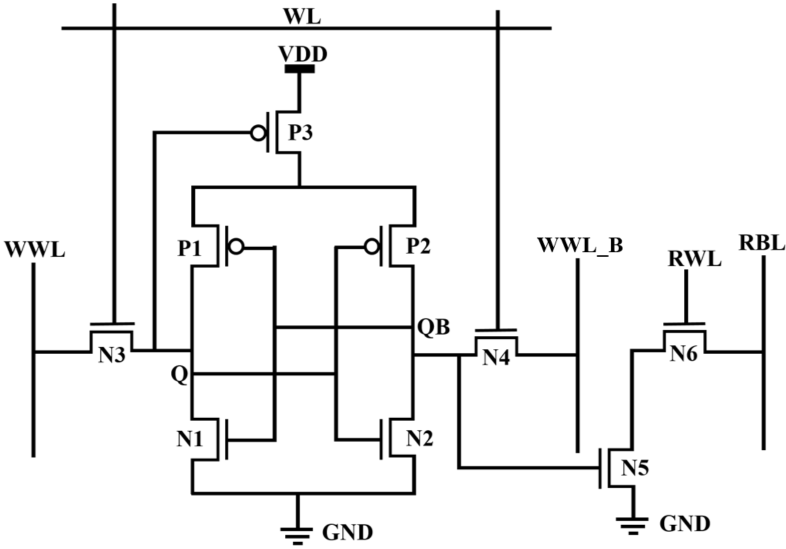


Figure 14: 9T SF-SRAM bitcell.

2.3.4 10T Single-Ended SRAM

The conventional 6T, 8T and 9T SRAM designs require pre-charging of the bit-lines during the read operation. This pre-charring imposes serious energy and timing constraints on the design and operation of high-density and high-capacity SRAM applications. Figure 15 shows the circuit

of a non-precharge 10T SRAM with a single-ended read BL. It is similar in structure to the 8T SRAM. There are two additional PMOS transistors (P3 and P4) as shown in Figure 15. It is a combination of the standard 6T SRAM cell, an inverter and a transmission gate. RWL controls the NMOS transistor (N6) at the transmission gate and RWL' controls the PMOS transistor (P4) at the transmission gate, which is the inverted signal of the read WL (RWL). As RWL and RWL' are activated, the transmission gate is triggered and the stored node gets coupled to RBL through the inverter [45]. In this 10T SRAM design, the precharge circuitry is eliminated, because the inverter fully charges/discharges the RBL. No power is consumed by the RBL if new arrived data is similar to the previous state. Therefore, 10T single-ended SRAM cell consumes no additional power if consecutive "0"s or "1"s are read out. The charge and discharge powers are only consumed if the readout data is different from the previous state. The transient probability on RBL is 50% for 10T single-ended SRAM in a sequence of random data, thereby reducing power consumption significantly during the read operation [52]. However, additional devices and required wirings impose higher area overheads compared to 8T and 9T SRAMs.

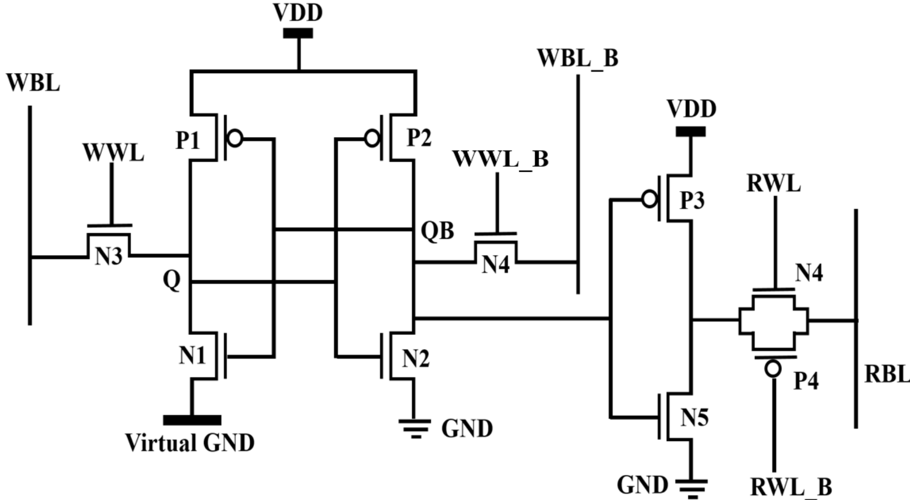


Figure 15: 10T Single-Ended SRAM bitcell.

CHAPTER 3

NOVEL HIGH PERFORMANCE ULTRA LOW POWER SRAM DESIGN

Lower power consumption and better reliability for individual memory bitcells, as well as overall memory systems are critical for high speed and dense memories. SRAM occupies a large part of the digital system and it is necessary to optimize SRAM cells because the performance of the system extensively relies on memory. In [46]-[52], different SRAM designs are presented to lower power consumption and improve stability and reliability of SRAM based systems. We propose a new hybrid 8T SRAM design by combining the single-ended bitline and the virtual ground techniques. The proposed design separates the read and the write operations, lowers the power consumption, and improves the noise margin compared to the conventional 6T and other existing 7T, 8T and 9T SRAM designs. The proposed design uses a virtual ground - a technique that weakens the positive feedback and improves the write-ability of the cell. The proposed circuit is much simpler in design and operation and more energy efficient.

3.1 Novel design promising attributes

The proposed 8T SRAM design has similar attributes like the 10T SRAM. The design eliminates pre-charging circuit, as the inverter fully charges/discharges the read bit-line (RBL) as shown in Figure 16(a) and Figure 16(b). As a result, a significant reduction can be achieved in power consumption and the overall area of the memory system. This is a huge improvement over the standard 6T SRAM and other 7T, 8T and 9T SRAM cells, all of which require pre-charging of the bit lines during the read operation that increases power consumption of the memory cell significantly. Therefore, the proposed 8T SRAM cell design offers the robustness

and energy efficiency of the previously proposed 10T SRAM cell design [52] without the additional area overheads for the extra devices. To provide a clear picture of the prospects of the proposed 8T SRAM cell, we have compared the power and area overheads with the other conventional SRAM designs, which is discussed in later section.

One of the key attributes of the proposed hybrid 8T SRAM is its disturb-free read operation. In the conventional 6T SRAM cell, two bitlines (BL) and one wordline (WL) are used during the read and write operations. In our design, only one BL and one WL are used. As a result, the power consumption during the read and write operations of the proposed design is lower. The proposed hybrid 8T SRAM design employs single-ended read and write operations. Its independent read and write paths allow the use of the minimum sized access transistors. In the conventional SRAM cells, this freedom of selecting minimum size access transistors is absent. The transistors size and layout of the proposed 8T and conventional 6T bitcell are shown in Figure 17(a) and Figure 17(b). An inadvertent read upset is a common problem for the conventional 6T SRAM cell. At smaller technology nodes (sub-45nm) it becomes worse, and the conventional 6T SRAM shows lower read stability and write ability. However, the hybrid design offers higher read stability and write ability in the sub-45nm region because the proposed design is free from the errors suffered by the conventional SRAMs. Higher immunity of the proposed 8T hybrid SRAM cell to the read upset is obtained by employing the inverter (P3-N5), which isolates the storage node (QB) from the read bitline (RBL) as shown in Figure 16(a). Therefore, the readout of the node QB can be performed without disturbing the stored data.

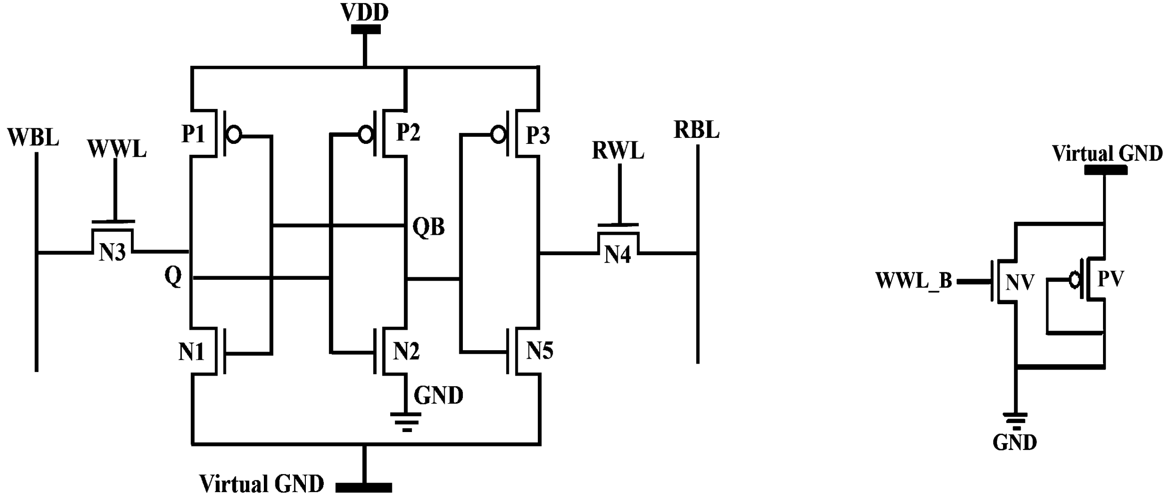
The defining feature of the proposed 8T SRAM is its hybrid design approach. The proposed design is the combination of two techniques: (i) utilization of single-ended bitline for separate read and write operations, which eventually reduces delay and power consumption during the read and write operations and (ii) utilization of virtual ground that weakens the positive feedback

and improves the write ability of the cell. The virtual ground technique is also used to reduce leakages. Precharging the bitlines has been an integral part of the SRAM operation. A separate circuit or arrangement is needed in the SRAM memory system to perform the precharging. The proposed 8T SRAM eliminates the precharging circuit because the inverter (P3-N5) charges/discharges the RBL as in the case of the 10T SRAM [52]. Therefore, the memory system based on the proposed 8T SRAM does not require external precharging. The proposed design has similar attributes to the 10T SRAM [52], but its overhead is significantly less than the 10T design. In Section VI, we show the implementation of an 8T 16Kb SRAM array to illustrate that the read operation of the proposed hybrid design does not need external precharging, which is a considerable improvement over the conventional 6T and other 7T, 8T and 9T designs, all of which require precharging of the bitlines during the read operation. Elimination of the precharging circuitry reduces the power consumption and the overall area of the memory system significantly. To highlight the prospects of the hybrid 8T SRAM, we compared the power consumption and the area overhead with the other existing SRAM designs in later section.

3.2 Write operation of the proposed 8T SRAM Cell

Since the proposed design is single ended, during the write operation the write wordline (WWL) is high while the read wordline (RWL) and the WWL_B (refer to Figure 16(b)) are low. As a result, the access transistor N3 is turned on while N4 is off and the write operation remains electrically separated from the read operation. Additionally, one of the cross-coupled inverter (P1-N1) employs virtual ground [39] to improve the write ability of the cell. As WWL_B is low, the NV transistor of the virtual ground circuit is off (refer to Figure 16(b)). Now, the virtual ground node is connected to the source of the PV transistor of the virtual ground circuit. The VSS of the inverter P1-N1 (first cross-coupled inverter of the bitcell) is connected to the virtual ground

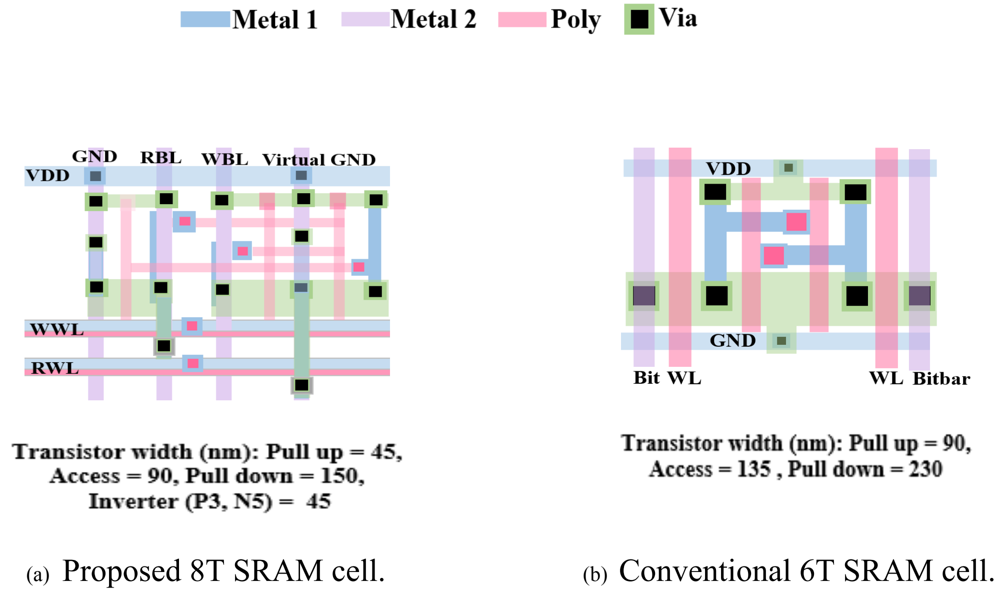
whereas, VSS of the inverter P2-N2 (second cross-coupled inverter of the bitcell) is connected to the actual ground during the write (refer to Figure 16(a)). Since, the virtual ground source is connected to the PMOS (PV), which is a bad pull-down device the virtual ground will never reach perfect zero during the write operation, which weakens the feedback of the inverters (P1-N1 and P2-N2) and aids in the write operation of the hybrid SRAM cell. It eventually improves the WSNM of the design. Let us consider that Q = '1' and we want to write a '0'. WWL is high, which turns on N3 and a write driver pulls write bitline (WBL) low. Once Q falls low, QB goes high as a result of the feedback. Similarly, to write '1' the WBL is set to high. The virtual rails are shared among the neighboring cells to reduce the power and area overheads. Sharing virtual rails between the cells in the same column imposes additional power consumption due to the leakage and dynamic currents in higher activity nodes, therefore the rail is shared in the same row. Figure 18 shows the architecture of the proposed design, in which the virtual ground rail is shared among the cells in the same row.



(a) Proposed hybrid 8T SRAM cell schematic.

(b) Virtual ground node schematic [39].

Figure 16: Proposed Hybrid 8T SRAM cell



(a) Proposed 8T SRAM cell.

(b) Conventional 6T SRAM cell.

Figure 17: Layout of SRAM bitcell designs.

3.3 Read operation of the proposed 8T SRAM cell

During the read operation, the RWL is activated (which turns on the N4 transistor), the WWL_B is high and the virtual ground node is connected to the source of the NMOS transistor (NV) as shown in Figure 15(b). Since NMOS is a good pull-down device, the feedback of the inverters (P1-N1 and P2-N2) becomes stronger at this stage. The WWL is low, which switches off the transistor N3. As a result, the read operation remains separated from the write operation. Under this condition, the inverter (P3-N5) isolates the storage node QB from the read bit line (RBL), which keeps the stored value at QB undisturbed during the read operation leading to higher read static noise margin (RSNM). During the read operation, the virtual ground nodes are connected to the ground to retain the stored data in strong feedback. Figure 19 shows the transient analysis of the proposed 8T bitcell. It utilizes local read bitline architecture [43], [44] as shown in Figure 18. The memory system architecture operates at a reduced bitline voltage swing from 0V to VDD/2.

Hence, the proposed 8T bitcell has a smaller delay compared to the conventional 6T bitcell employing differential read operation. Besides, the write '1' delay of the hybrid 8T bitcell is greater than the conventional 6T bitcell because the proposed design is a single-ended circuit. Table 3 provides the delay and worst leakage current comparison between the conventional 6T and the proposed 8T bitcells at 1V supply voltage.

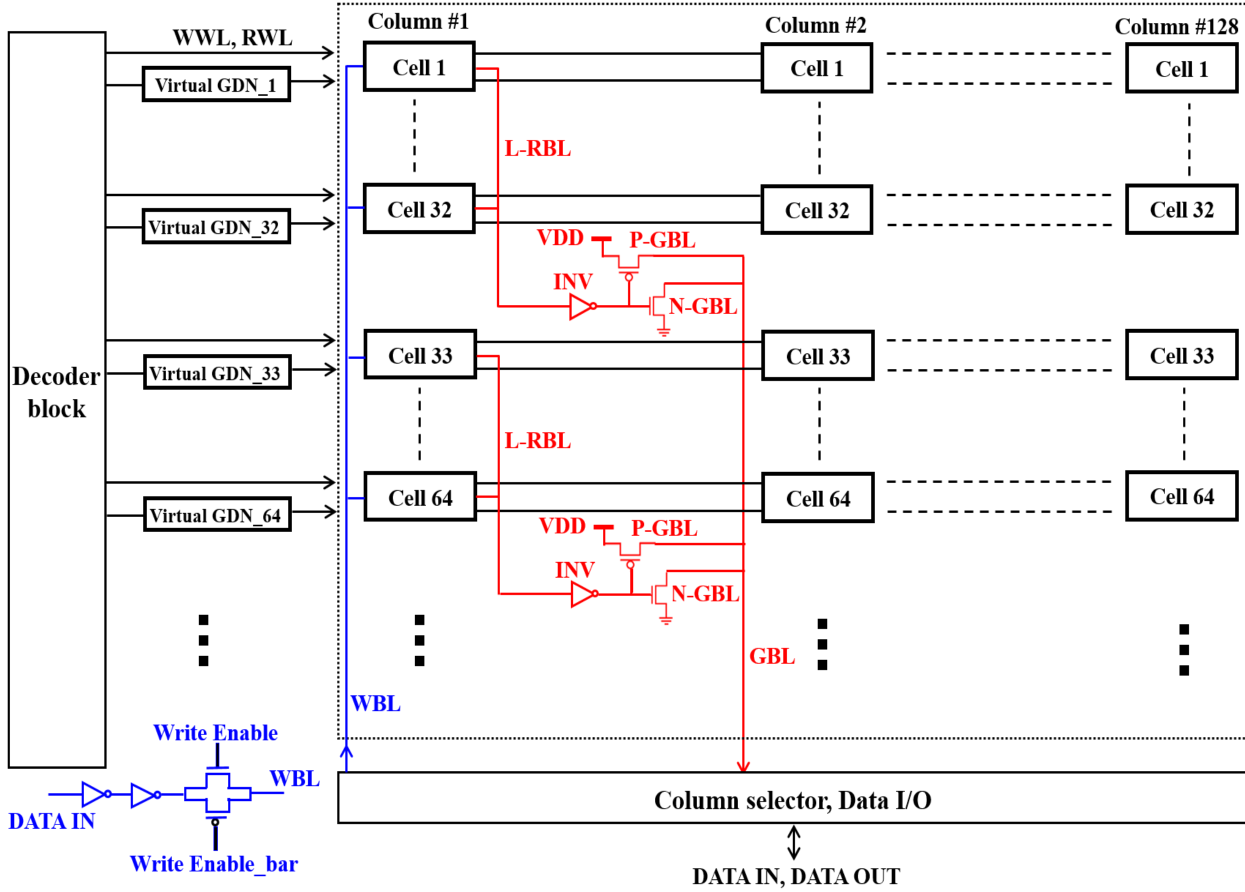


Figure 18: Proposed 8T SRAM memory system architecture.

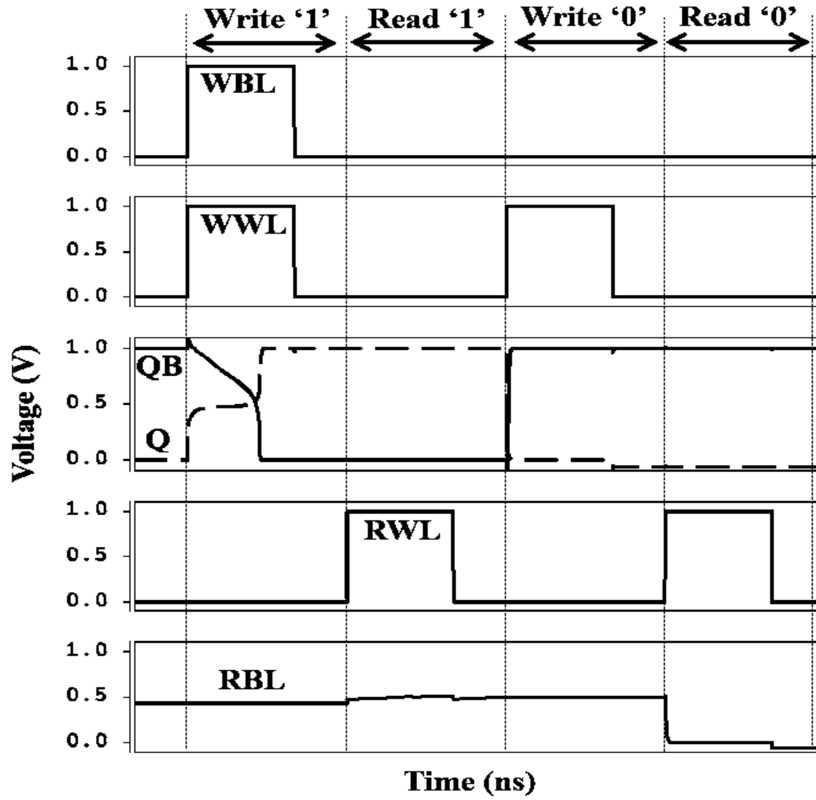


Figure 19: Transient analysis of proposed 8T SRAM bitcell.

Table 3: Delay and leakage current of conventional 6T and proposed 8T SRAM bitcell, at 1V.

SRAM bitcell			6T	Proposed 8T	Improvement
Delay (ps)	Write	0	57.4	15.8	72.47%
		1	68.7	107.3	-38.6%
	Read	0	23.4	14.2	39.32%
		1	30.13	25.8	17.12%
Worst Leakage Current (pA)	Write		328.6	267.3	18.65%
	Read		284.8	257.8	9.5%
	Hold		240.25	250.90	-4.24%

3.4 Reliability and robustness of the proposed 8T cell

The read stability and the write ability are the two most critical metrics to measure the reliability and the robustness of SRAM cells. We analyzed the reliability and the robustness of the proposed 8T SRAM using widely accepted methods [16], [17]. The ability to retain data in the cross-coupled inverters of the SRAM cell is expressed as the static noise margin (SNM). With the reduction of the supply voltage (VDD), the read operation becomes more destructive, and the cell is highly prone to read upset. However, it is recommended to lower VDD to minimize the power consumption of the SRAM cell leading to lower robustness and speed [45]. For the SRAM reliability analysis, three different SNM figures are relevant. These are the Hold Static Noise Margin (HSNM), Write Static Noise Margin (WSNM) and Read Static Noise Margin (RSNM). Figure 20 compares the HSNM of the conventional 6T, conventional 8T and the proposed hybrid 8T SRAMs at different supply voltages. During the hold mode, the WWL and RWL are deactivated, and the access transistors are turned off. The data is retained at the storage nodes Q and QB. Figure 21 compares the RSNM of the conventional 6T, conventional 8T and the proposed 8T SRAMs at different supply voltages. The RSNM of the proposed 8T SRAM is high because of the following reasons. First, the RBL is not precharged during the read operation and therefore, there is no voltage available on the RBL to destroy the data at the storage node QB. Second, the inverter (P3-N5) isolates the node QB from the RBL and prevents any leakages from the RBL to disturb the data at QB. Figure 22 compares the WSNM of the conventional 6T and the conventional 8T SRAMs with the proposed 8T SRAM at different supply voltages. The WSNM of the proposed 8T SRAM is high because its write circuit is electrically separated from the read circuit (the two circuits are activated independently by the WWL and RWL, respectively). Additionally, the virtual ground used during the write operation

weakens the positive feedback, which further improves the write ability. We also used the N-curve method to investigate the read stability and the write ability of the proposed SRAM as shown in Figure 23. This method illustrates the stability of the SRAM cell in terms of current.

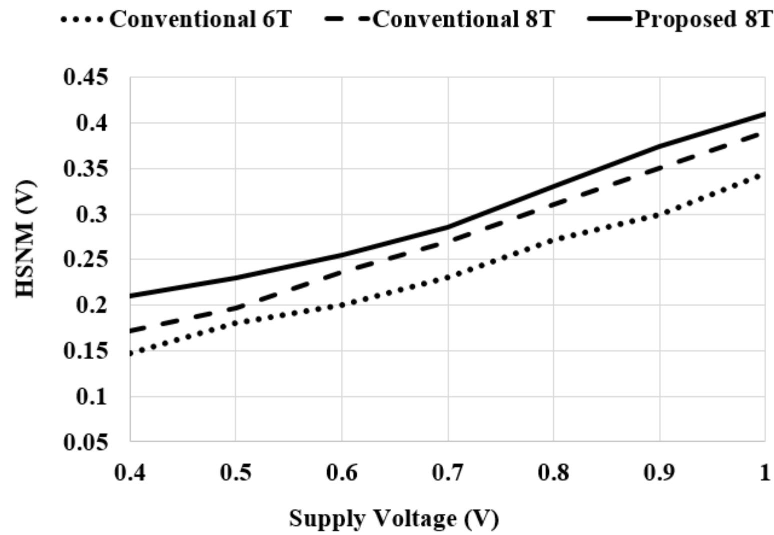


Figure 20: Variation of HSNM at different supply voltage.

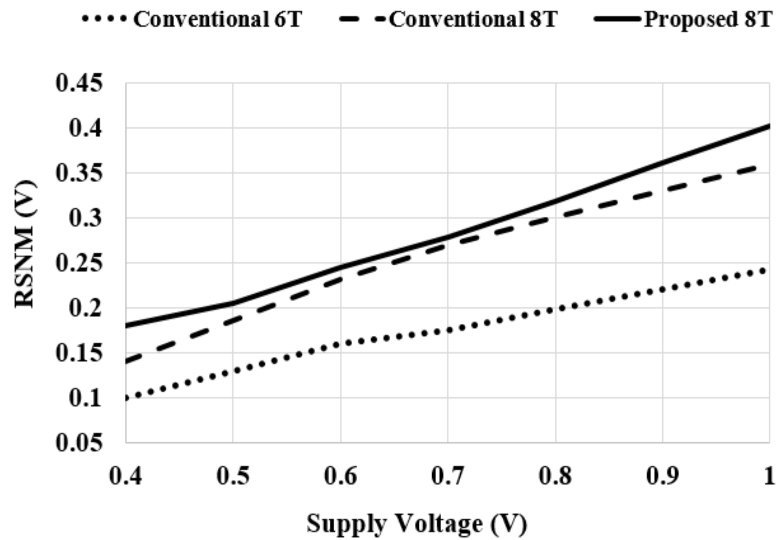


Figure 21: Variation of RSNM at different supply voltage.

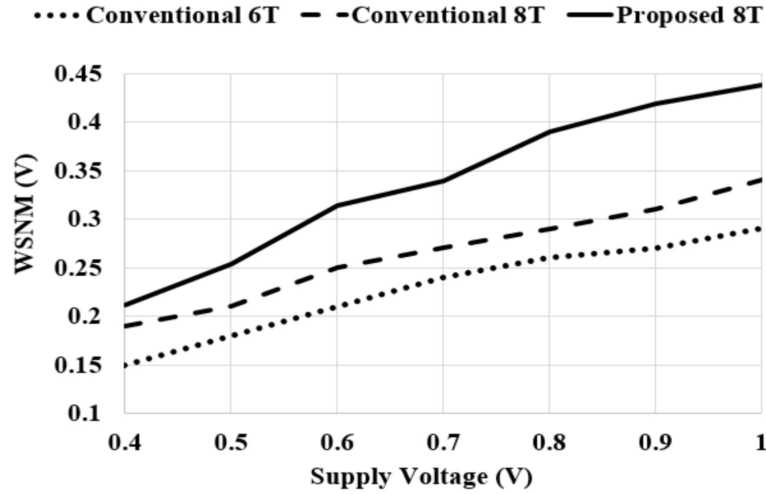


Figure 22: Variation of WSNM at different supply voltage.

Table 4 provides a comparative analysis of the conventional 6T and the proposed 8T SRAMs based on the N-curve method. To further illustrate that the proposed 8T SRAM has higher reliability and robustness compared to other SRAM cells, we have calculated the RSNM of the existing 6T, 7T, 8T, 9T and 10T SRAM cells at 0.4V supply voltage (the worst case) as shown in Figure 24. It is observed that the proposed SRAM design offers better RSNM compared to most of the SRAM designs. Only one 9T and one 10T cells presented in [51] and [52] offer slightly better RSNM compared to the proposed 8T SRAM. However, it is important to keep in mind that these two (9T and 10T) designs have higher overheads.

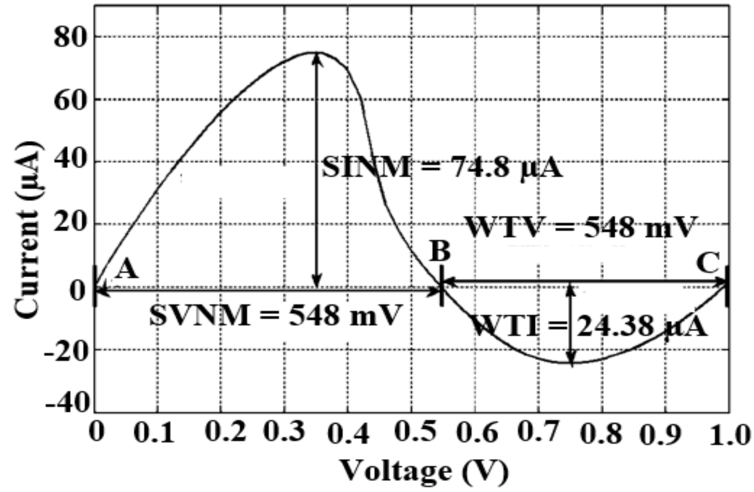


Figure 23: N-curve simulation result for 8T SRAM.

Table 4: N-curve parameters of the proposed 8T SRAM cell.

N curve metrics	6T SRAM	Hybrid 8T SRAM	% Improvement of write ability in the proposed 8T SRAM.
SVNM (mV)	282	548	94.33%
SINM (µA)	53.6	74.8	39.5%
WTV (mV)	718	452	37.05%
WTI (µA)	96.4	24.38	74.7%

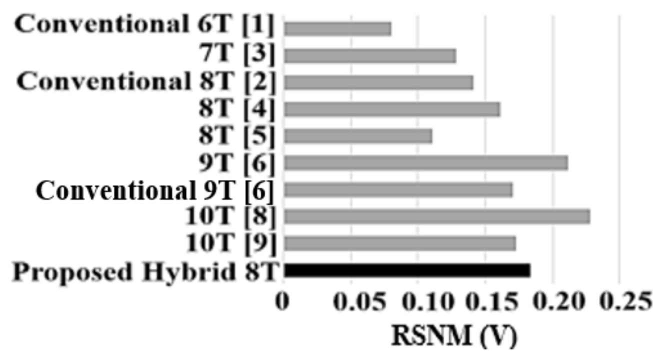


Figure 24: RSNM comparison of different SRAM cells at 0.4V supply voltage.

3.5 Power and area overhead of the proposed 8T cell

This section provides a comparison of the power consumption and area overhead in the proposed hybrid 8T and other existing SRAM designs. Table 5 data reveal that the proposed 8T SRAM cell is significantly more energy efficient than the previous cells.

Table 5: Power consumption analysis of SRAM bitcell at 1V supply voltage.

SRAM bitcell design	Write Power (nW)	Read Power (nW)
Conventional 6T [46]	18.02	4.37
7T [39]	15.08	4.37
Conventional 8T [10]	18.02	8.75
Proposed Hybrid 8T	**16.87**	**1.82**
Conventional 9T [50]	78.63	96.24
9T [10]	64.03	0.96
10T [51]	87.18	17.17

Table 6 provides a comparative analysis of the area overheads of different SRAM cells. We implemented the conventional 6T and the proposed 8T using 45nm technology node. The bitcell area information of the existing 8T and 10T designs implemented in 45nm technology is taken from the previous works [10], [52]. It is observed that the area overhead of the proposed 8T SRAM is increased by 1.16 times compared to the conventional 6T SRAM cell. From the published data, it is observed that the area of existing 8T is slightly more than the area of the proposed 8T cell. However, the area of 10T SRAM bitcell is 1.27 times more compared to the proposed SRAM bitcell. Even with the same or slightly higher area overhead, the proposed

hybrid design will be significantly more attractive compared to the existing 6T, 7T, 8T, and 9T designs due to its other positive aspects and advantages, such as, higher robustness, lower power consumption, more straightforward design and simpler operation as explained in the earlier sections. Overall the proposed design would be better than the 10T design due to lower area overhead and circuit complexity.

Table 6: Bitcell area of different SRAM designs in 45nm technology.

Design	Area (μm^2)
Conventional 6T SRAM	1.26 × 0.43
Conventional 8T SRAM [10], [52]	1.55 × 0.41
10T SRAM [52]	1.97 × 0.41
Proposed Hybrid 8T SRAM	**1.47 × 0.43**

3.6 Implementation of a 16Kb SRAM array

This section shows the implementation of a 16Kb SRAM array using the proposed hybrid 8T SRAM cell. The proposed hybrid 8T SRAM design eliminates the precharging circuit of the conventional SRAMs because the inverter in the bitcell charges/discharges the RBL. As a result, the power consumption during the read operation and the overall area of the memory system are significantly less. For the given address, the decoder block selects WWL (RWL) for write (read) operation. The column selector is responsible for selecting the desired column. A common local read bitline (L-RBL) is shared by 32 bitcells in each column. These L-RBLs are connected to the global bitline (GBL) via the inverter (INV), PMOS keeper (P-GBL) and the NMOS (N-GBL) transistor as shown in Figure 18. There are 128 GBLs in the architecture, which are multiplexed to get the DATA OUT. Data is written via WBL through the write drivers. During write '1', both

the WBL and WWL are high, the value is high at node Q and low at node QB. The values at the nodes Q and QB interchange when WBL is low (write ‘0’), and WWL is high. The read operation is performed by triggering the RWL. The value at QB is fed as an input to the inverter (P3-N5) (refer to Figure 16(a)). During read ‘1’, the value at node QB is low, and the output of the inverter (P3-N5) is high. The output of the inverter gradually charges the L-RBL once the RWL is triggered. The L-RBL eventually charges GBL through P-GBL and the data is read out via DATA OUT. During read ‘0’, the value at QB is high, which discharges the L-RBL and eventually turns on N-GBL, which then discharges GBL. The transient response of proposed 8T 16Kb SRAM is shown in Figure 25. The proposed array design features a fast access time of 598.4ps (1.9ns) and lowers energy consumption of 3.51fJ/‘0’bit (9.76fJ/‘1’bit). The access time for ‘1’ is higher than the access time for ‘0’ in the proposed memory system architecture. However, the access time for ‘1’ in the hybrid 8T memory system architecture design is insignificant compared to the access time of other existing SRAM architectures, because the proposed architecture does not require additional time to precharge the read bitline as required in the conventional memory system architectures.

3.7 Robustness of novel 8T SRAM bitcell against process variations and critical charge

With the shrinking of technology nodes and reduction of VDD, the process and parametric variations impose a significantly higher and more prominent impact on the performance and reliability of the integrated circuits [55], [56]. Increasing process variations lead to a higher failure probability and a lower yield in SRAM design process. Therefore, for memory design, it is critical to know these process corners to secure optimum performance and reliability. Figure 26 provides the comparison of the RSNM in the proposed 8T and the conventional SRAMs at

different process corners FF (fast NMOS, fast PMOS), SS (slow NMOS, slow PMOS), TT (typical NMOS, typical PMOS), FS (fast NMOS, slow PMOS) and SF (slow NMOS, fast PMOS).

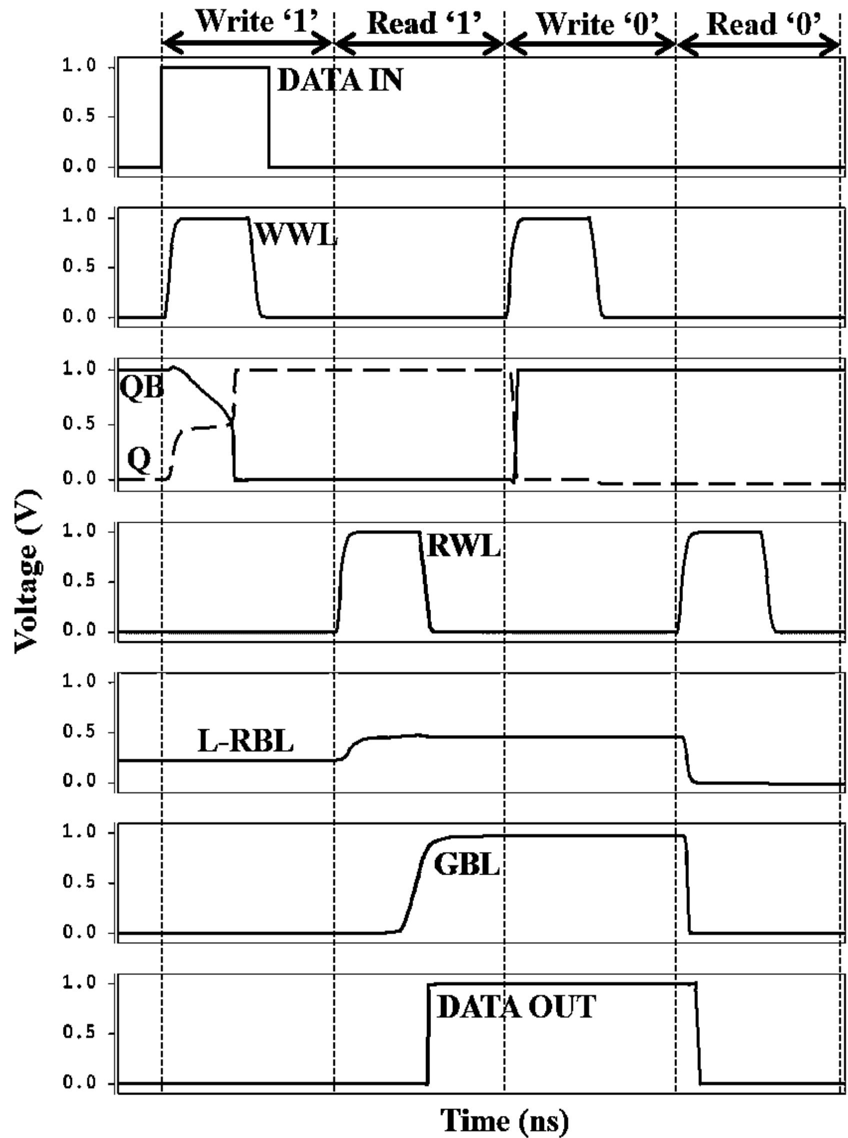


Figure 25: Transient analysis of hybrid 8T 16Kb SRAM array.

It is observed that the proposed hybrid 8T SRAM has higher RSNM values at different process corners. The performance of the proposed 8T SRAM does not degrade when compared

to the conventional SRAMs, even at the FS corner (worst). The RSNM value of the proposed 8T SRAM at the FS corner reduces only to 3.9% compared to the TT corner. However, for the conventional 6T and 8T SRAMs, the RSNM at the FS corner reduces to 7.52% and 5.34%, respectively, compared to the TT corner. The percentage variation of the RSNM in the proposed hybrid 8T SRAM is less than the conventional 6T and 8T SRAMs.

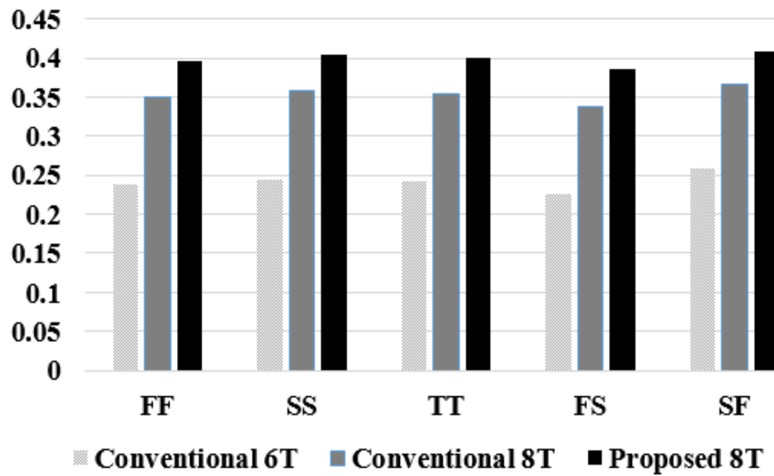


Figure 26: RSNM of SRAM cells at different process corners.

Another critical parameter is the temperature variation. Logic errors or functional failures might occur due to the temperature variation across the communicating blocks residing on the same chip [57]-[59]. Figure 27 shows the variation of the SNM values with the temperature at 1V supply voltage. The SNM of SRAM bitcells degrades with the increase in temperature. However, the stability of the proposed hybrid 8T SRAM is higher compared to the conventional SRAM bitcells at all temperatures.

Monte Carlo simulations are performed on the proposed hybrid SRAM design to evaluate the process variations. For simulation, the threshold voltage (VTH) is modeled as a ±10%

Gaussian distribution with variation at the ±3σ level. Figure 28 shows the Monte Carlo simulations of the proposed hybrid SRAM cell with 1000 samples at 1V supply voltage. The simulation results show that with process variation, the worst RSNM of the proposed hybrid 8T SRAM is 1.62 and 1.05 times better than conventional 6T and 8T SRAM in the ideal case. Similarly, the worst WSNM of the proposed 8T SRAM is 1.24 and 1.04 times better than the conventional 6T and 8T SRAM in the ideal case. Double exponential pulse current model is used to determine the critical charge (Q_{crit}) of the proposed cell. The injected current pulse is shown in Figure 29. The Q_{crit} of proposed 8T bitcell is 19.2fC.

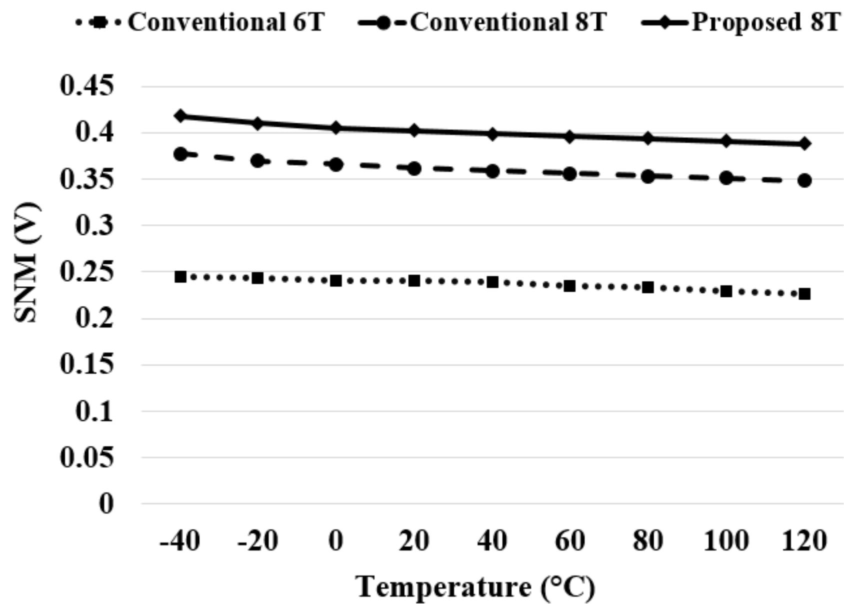
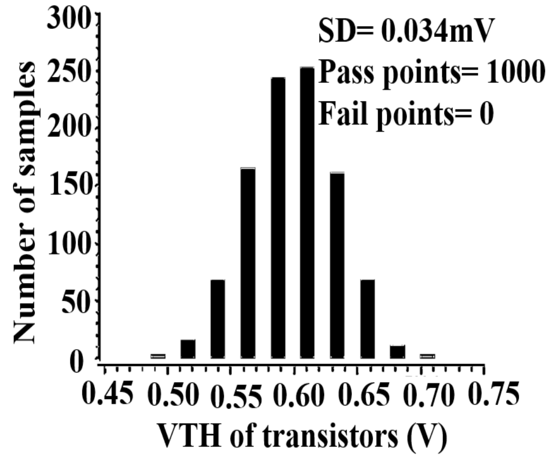
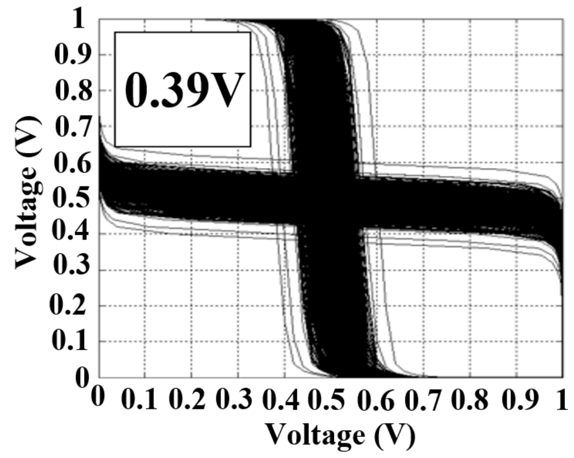


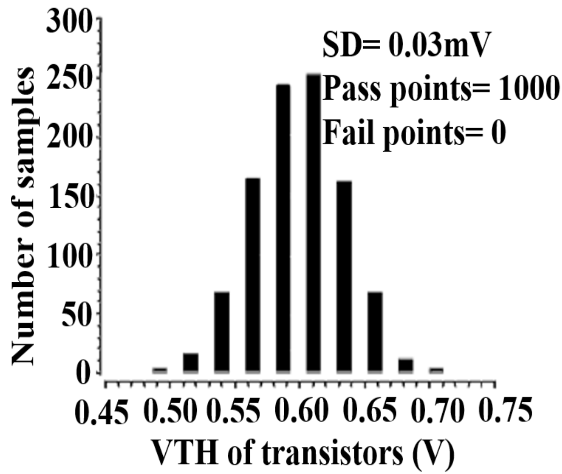
Figure 27: SNM of SRAM cells at 1V with different temperatures



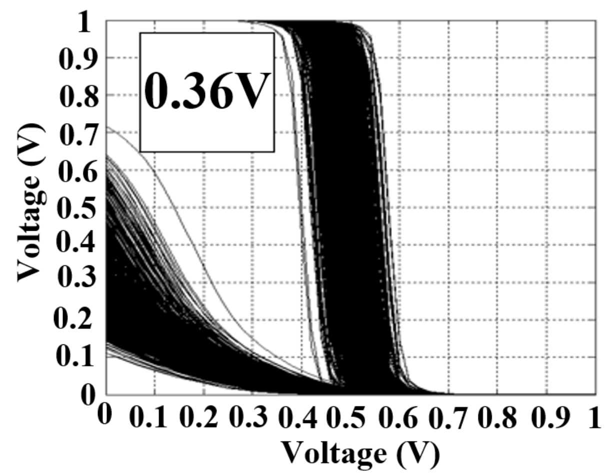
(a)Monte Carlo simulation for read, with 0 fail and 1000 pass points.



(b) RSNM of hybrid 8T SRAM under process variation.



(c) Monte Carlo simulation for write, with 0 fail and 1000 pass points.



(d) WSNM of hybrid 8T SRAM under process variation.

Figure 28: SNM analysis of hybrid 8T SRAM under process variation.

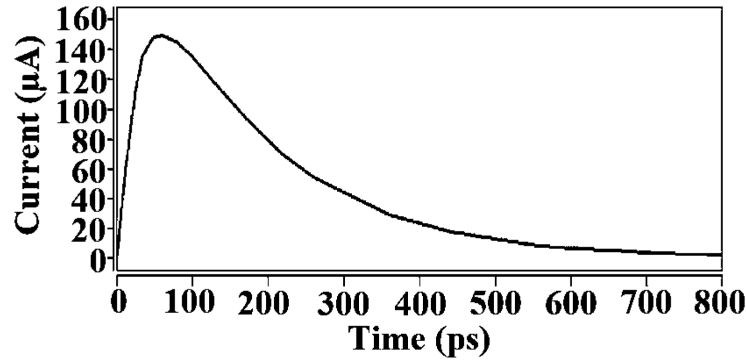


Figure 29: Injected current pulse profile.

3.8 Summary

In this chapter, a new hybrid 8T SRAM design is proposed. It offers higher energy efficiency, reliability, robustness, and performance compared to the conventional 6T and other existing 7T, 8T, 9T and 10T designs. It offers the advantages of a 10T SRAM without the additional area, delay and power overheads of the 10T SRAM. The proposed hybrid 8T SRAM can overcome many other limitations of the existing SRAM designs. One of the critical features of the new design is the elimination of the bitline precharging requirement during the read operation. In the conventional SRAM, precharging of the bitlines imposes power overhead and additional circuit complexity. All the simulations, layouts and analyses in this chapter are performed using 45nm technology. A comparative analysis is performed between the proposed and the existing SRAM designs in terms of area, total power consumption during the read and write operations, and stability and reliability. The individual cell area of the proposed hybrid 8T SRAM is 1.16 times more than that of the conventional 6T SRAM when implemented in 45nm. However, the area of the proposed cell is less than other existing SRAM designs. The implemented 16Kb SRAM array using the proposed 8T SRAM cell features a fast access time of 598.4ps (1.9ns) and a lower energy consumption of 3.51fJ/‘0’bit (9.76fJ/‘1’bit). Monte Carlo simulations are performed on

the proposed hybrid SRAM design to evaluate the impact of the process variations, and it is observed that the proposed SRAM is more robust towards the process and parametric variations. Other issues like bit-interleaving and half-select cells need to be investigated to validate the commercial feasibility of the proposed hybrid 8T SRAM design. Our future work will cover these unresolved issues.

CHAPTER 4

TUNNEL FET BASED SRAM DESIGN

The Static Random Access Memory (SRAM) has a significant impact on the overall power consumption and energy efficiency of any micro and nanoelectronic application or system. SRAM consumes a considerable amount of power in the idle state. As a consequence, the leakage power is one of the most critical metrics in SRAM designs. One of the promising emerging device for ultra low power application is Tunnel FET (TFET). This chapter covers design and analysis of TFET based SRAM.

4.1 Stability of T-SRAM

The retention of data at the storage nodes (Q and QB shown in Figure 30) of the SRAM cell is a challenging issue in the standby mode as well as during the read operation. Since the technology is scaling, the supply voltage of the cell is also reduced, which in turn affects the stability of the SRAM cell. The stability of the SRAM circuit depends on the Static Noise Margin (SNM). It is the minimum DC noise voltage (V_n) required to flip the data at the storage nodes. An equivalent circuit for the SNM definition comprises of two DC noise voltage sources [16]. These noise sources (V_n) are placed in series with the cross-coupled inverters as shown in Figure 16. SNM can be determined graphically by plotting the voltage transfer characteristic (VTC) of the inverters (Inv1 and Inv2). The VTC of Inv2 is superimposed on the inverse VTC of Inv1.

Then the square with the largest length nested between inverters' VTCs (butterfly curve) is equal to the SNM of the cell [17].

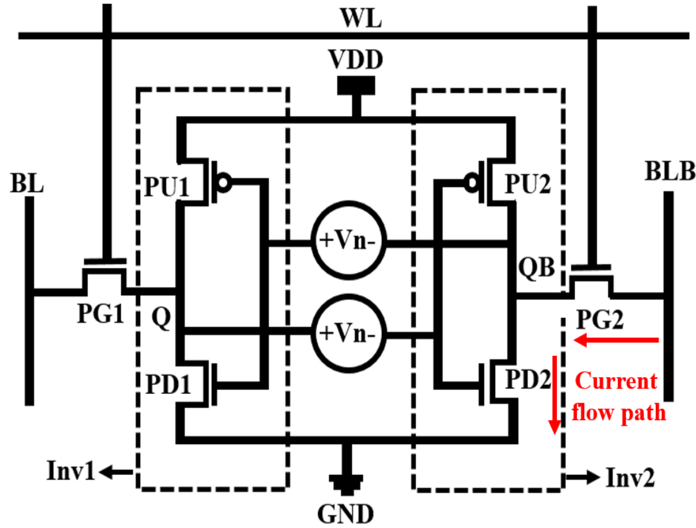


Figure 30: Simulation setup for the SNM evaluation of the 6T TFET SRAM cell [15].

Three different SNM figures are significant in determining the robustness of the SRAM cell. These are the Hold Static Noise Margin (HSNM), the Write Static Noise Margin (WSNM) and the Read Static Noise Margin (RSNM). During the hold mode, the wordline (WL) is low, and the pass-gate (PG) transistors are *OFF*. The data are retained at the storage nodes. RSNM is evaluated during the read access. During the read operation, bitlines (BL and BLB) are precharged to *VDD* or *VDD*/2, and the WL is high, and the PG transistors are *ON*. HSNM and RSNM of T-SRAMs are shown in Figure 31 and Figure 32, respectively.

The HSNM and RSNM are directly dependent on the width ratio of the PD and PG transistors of the cell. This ratio is known as the cell ratio (CR) or beta ratio. In an ideal case, the butterfly curves restrict the maximum length of a side of the square to 0.5*VDD*, which is the maximum limit for the SNM. Therefore, supply voltage scaling limits the stability of the SRAM cell. SNM

degrades with the scaling down of *VDD* as shown in Figure 33 and Figure 34. It is observed that T-SRAM with PU: PD: PG = 2:5:2 configuration achieves the maximum HSNM compared to other configurations at different supply voltages. However, The RSNM of the T-SRAMs with 1:5:2 and 2:5:2 configurations are approximately the same at different supply voltages. Both the HSNM and RSNM are the least for 1:1:1 configuration T-SRAM.

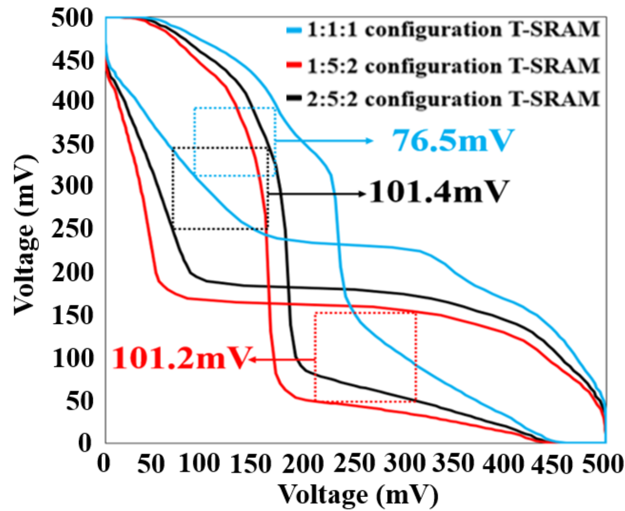


Figure 31: HSNM of T-SRAMs for different PU:PD:PG configurations at 500mV supply.

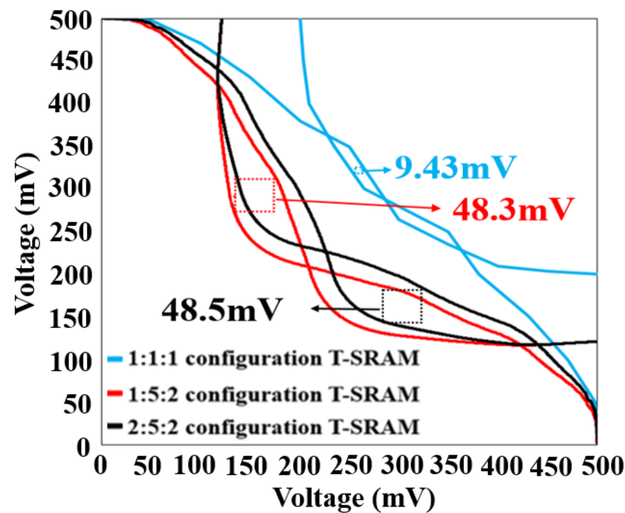


Figure 32: RSNM of T-SRAMs for different PU:PD:PG configurations at 500mV supply.

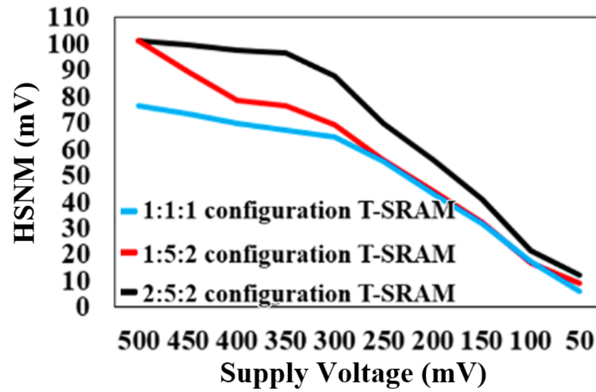


Figure 33: HSNM of T-SRAMs for different PU:PD:PG configurations at different supply.

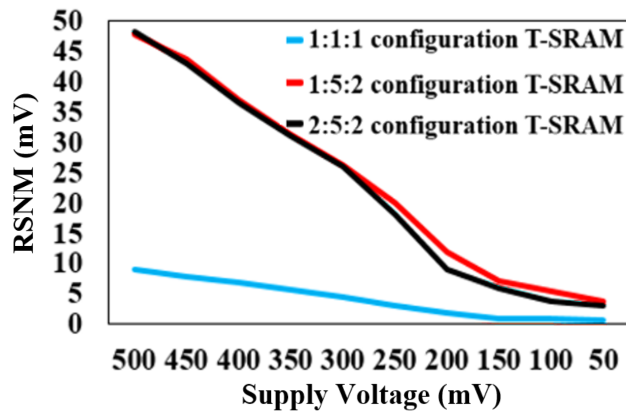


Figure 34: RSNM of T-SRAMs for different PU:PD:PG configurations at different supply.

4.2 Write ability of the T-SRAM

The WSNM indicates the write ability of the cell and is evaluated during the write operation. During the simulation, the WL is kept high, and the data is driven through the bitlines. The WSNM is estimated using the voltage transfer characteristics (VTC) of the inverters PU1-PD1 and PU2-PD2 as shown in Figure 35. VTCs of the two inverters are not similar since the BLB is driven high and the BL is set to ground. The side of the largest square nested inside the two curves represents the WSNM of the SRAM cell.

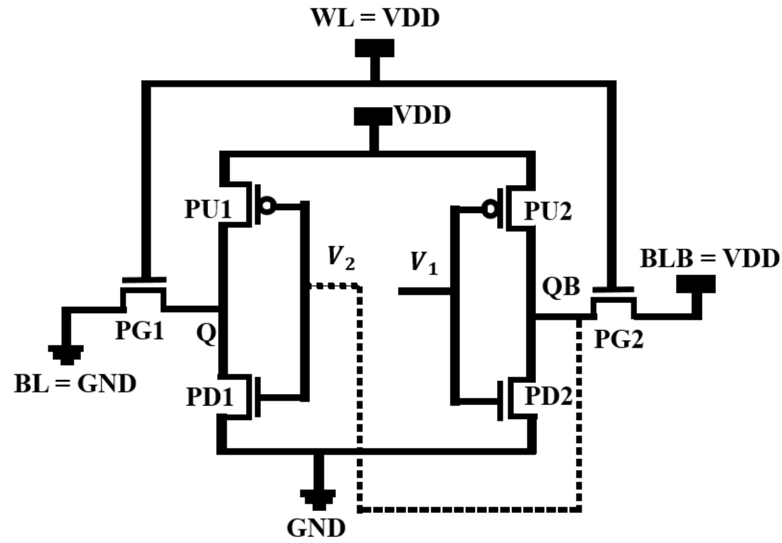


Figure 35: Simulation arrangement for the WSNM evaluation of T-SRAM.

In T-SRAM, the write operation is performed by the single pass-gate transistor PG2. Therefore, to achieve high WSNM, the pass-gate transistors (PG1 and PG2) must be stronger than the pull-down transistors (PD1 and PD2). The WSNM of T-SRAMs for different PU: PD: PG configurations are shown in Figure 36. The WSNM degrades with the reduction of the supply voltage as shown in Figure 37. It is observed that 1:1:1 configuration T-SRAM achieves maximum WSNM at different supply voltages.

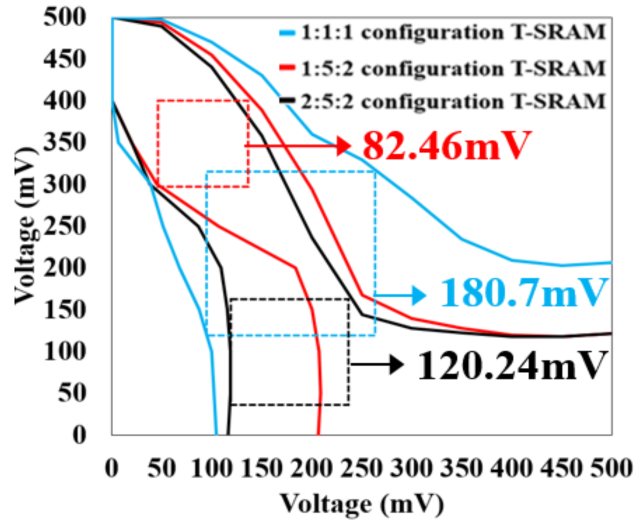


Figure 36: WSNM of T-SRAMs for different PU:PD:PG configurations at 500mV.

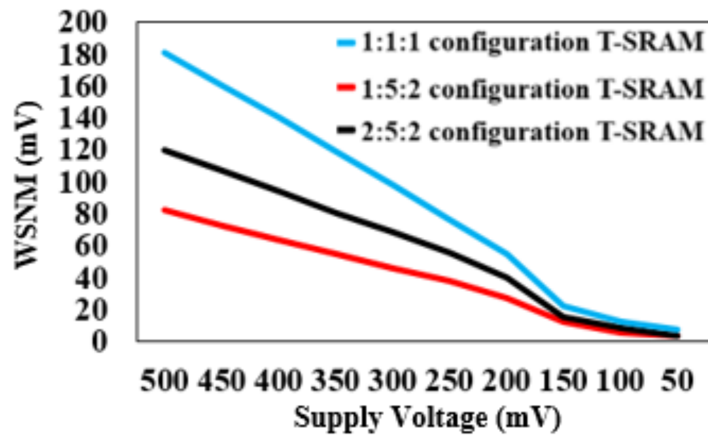


Figure 37: WSNM of T-SRAMs for different PU:PD:PG configurations at different supply.

4.3 N-curve analysis of the T-SRAM

The N-curve is an alternative method used to determine the read stability and the write ability of the SRAM. This method illustrates the stability of the SRAM cell in terms of the current. For simulation, both bitlines are clamped to *VDD,* and the WL is triggered. A voltage sweep from 0V to 500mV is applied at the storage node with data value “0”, and the corresponding current

curve is obtained. The current curve crosses zero at A, B, and C for different configurations of the T-SRAMs as shown in Figure 38. A and C are the two stable points, and B is the meta-stable point. If B coincides with A, then destructive read can happen easily. The part between A and B represents the read stability of SRAM. The static voltage noise margin (SVNM) is the voltage difference between A and B. It is the maximum tolerable DC noise voltage at the storage node with data value "0" before its content flip. The current peak between A and B is the static current noise margin (SINM). It is the maximum current, which can be injected into the SRAM cell without flipping the data of the cell. Read stability of SRAM cell can be determined accurately with combined SVNM and SINM information. N-curve is also employed to determine the write ability of the SRAM. Write trip current (WTI) is the negative peak current between C and B. It is the current margin of the cell for which the data at the storage node changes. Write-trip voltage (WTV) is the required voltage drop to flip the content of the storage node with data value "1" when both the bitlines are clamped at *VDD*. It corresponds to the voltage difference between B and C.

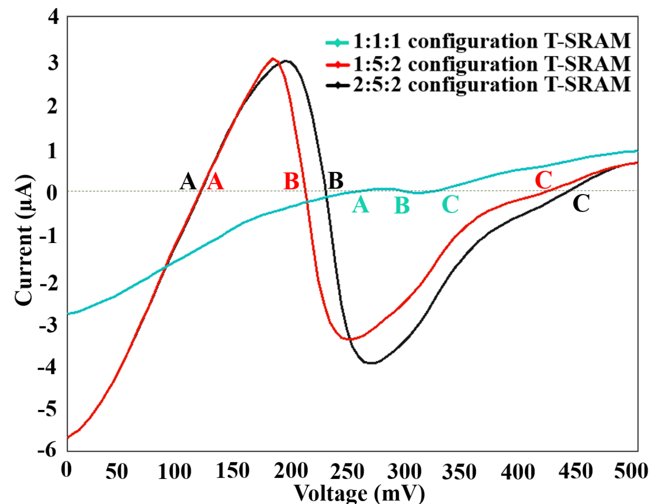


Figure 38: N-curve analysis of TFET based SRAMs for different PU:PD:PG ratio configurations at 500mV supply voltage.

Table 8 provide N-curve parametric values for different PU: PD: PG configurations of the T-SRAMs at the 500mV supply voltage. Monte Carlo simulations were performed for the T-SRAMs to evaluate process variations. For simulation, V_{TH} was modeled as a ±5% Gaussian distribution with the variation set at the ±3σ level. Figure 39 and Figure 40 show the Monte Carlo simulations for 1:5:2 and 2:5:2 configurations of the T-SRAMs with 2000 samples at the 500mV supply voltage. The simulation results show that with the process variation the worst SVNM, the worst SINM and the worst WTV for 1:5:2 configuration of the T-SRAM are 1.01, 11.86 and 1.9 times better than the 1:1:1 configuration of the T-SRAM in the ideal case, respectively. Similarly, for the 2:5:2 configuration of the T-SRAM cell the worst SVNM, the worst SINM and the worst WTV are 1.13, 6.91 and 3.90 times better than the 1:1:1 configuration of the T-SRAM in the ideal case, respectively.

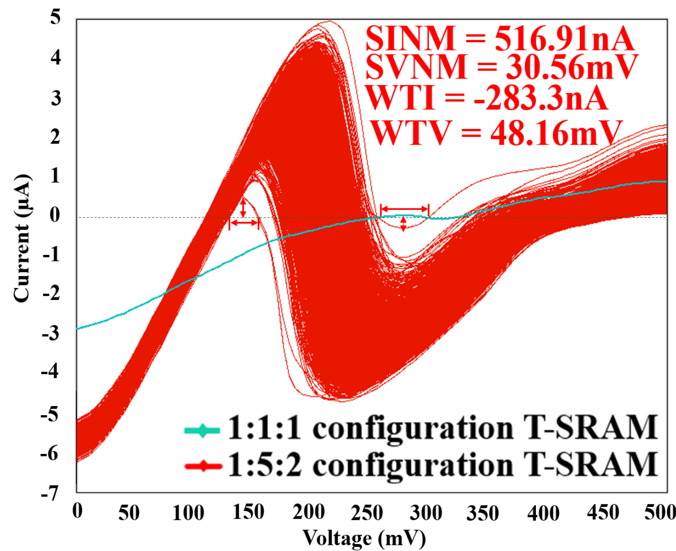


Figure 39: N-curve analysis of 1:5:2 configuration TFET based SRAM under parametric variation.

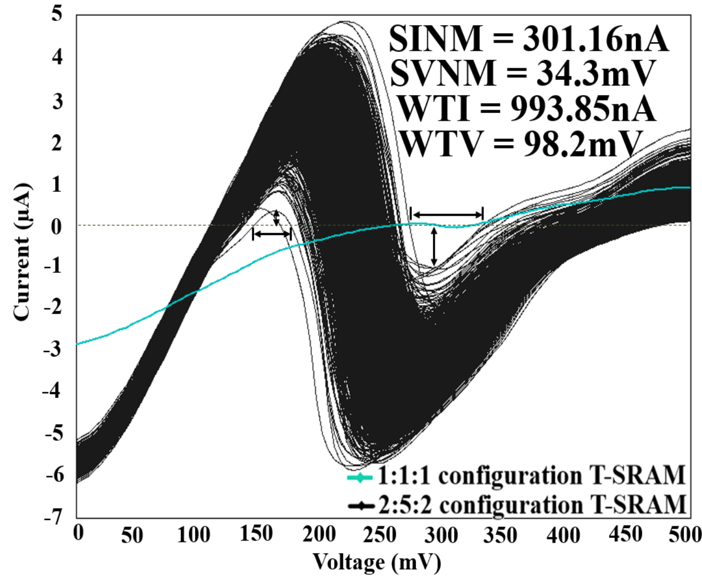


Figure 40: N-curve analysis of 2:5:2 configuration TFET based SRAM under parametric variation.

4.4 Benchmarking of T-SRAMs

TFET based 6T SRAM cells (T-SRAM) have lower area than FinFET based 6T SRAM cells (F-SRAM). The TFET devices used for designing SRAM cells have vertical architecture and fin structure. The area of T-SRAMs and F-SRAMs are evaluated following the study in [15], [21] and [22]. Table 7 compares the performance of the T-SRAM and the F-SRAM.

Table 7: Performance summary of T-SRAM and F-SRAM

Design	T-SRAM		
Technology	10 nm		
Supply Voltage	500mV		
PU:PD:PG	1:1:1	1:5:2	2:5:2

Density	High	Intermediate	Low
Dynamic Write Power (nW)	0.562	3.62	4.159
Write delay (nS)	0.377	0.346	0.43
Dynamic Write Energy(J)	2.11 E-19	1.25 E-18	1.79 E-18
Dynamic Read Power (nW)	1.792	12.728	15.357
Read delay (nS)	16.56	5.502	5.494
Dynamic Read Energy(J)	2.96 E-17	7.02 E-17	8.43 E-17
Area (μm^2)	0.014	0.026	0.031

From Table 7, it is observed that the T-SRAMs are slower than the F-SRAMs because I_{ON} of the FinFET devices is higher than the TFET devices. However, I_{ON}-I_{OFF} ratio of the TFET devices are higher than the FinFET devices. Hence, the TFET SRAMs have low standby leakages and are more energy efficient. In this chapter, we performed a detailed comparative analysis between the T-SRAMs and F-SRAMs as illustrated in TABLE 3. Important aspects of the benchmarking are as follow:

- The standby leakage power of the T-SRAMs are 107.57%, 163.64%, and 140.44% less than the F-SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively. This is one of the major advantages of the TFET based SRAM.

- The HSNM of the T-SRAMs are 4.97%, 5.02% and 1.01% more compared to the F-SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively.

- The RSNM of the T-SRAMs are 41.8% and 37.36% more compared to the F-SRAMs for 1:5:2 and 2:5:2 configurations, respectively. However, RSNM of the T-SRAM is 24.07% less compared to the F-SRAM when the PU:PD:PG ratio is 1:1:1.

- The WSNM of the T-SRAMs are 143.27% and 53.3% less compared to the F-SRAMs for 1:1:1 and 2:5:2 configurations, respectively. However, WSNM of the T-SRAM is 24.8% more compared to the F-SRAM when the PU:PD:PG ratio is 1:1:1.

- SVNM, SINM and WTV of the F-SRAMs are higher than the T-SRAMs.

- WTI of the T-SRAMs are improved 181.3, 5.01 and 8.6 times compared to the F-SRAMs for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively.

Table 8: Benchmarking between 10 nm 6T T-SRAM and 10 nm 6T F-SRAM.

Design	T-SRAM		
Supply Voltage	500mV		
PU:PD:PG	1:1:1	1:5:2	2:5:2
Standby leakage power (nW)	1.73	3.74	4.55
HSNM (mV)	76.5	101.2	101.4
RSNM (mV)	9.43	48.3	48.5
WSNM(mV)	180.7	82.46	120.24
SVNM (mV)	30.3	93.05	108.96

SINM (A)	43.58n	3.02μ	2.97μ
WTV (mV)	25.12	216.23	213.64
WTI (A)	-55.7n	-3.41μ	-3.97μ

4.5 Summary

From the analysis, it is clear that the main advantage of the TFET based SRAM would be the significant improvement in terms of leakage or standby power consumption. Compared to the FinFET based SRAM the standby leakage power of the T-SRAMs are 107.57%, 163.64%, and 140.44% less for 1:1:1, 1:5:2 and 2:5:2 configurations, respectively. Since leakage/standby power is the primary source of power consumption in the SRAM, and the overall system energy efficiency depends on SRAM power consumption, TFET based SRAM would lead to massive improvement of the energy efficiency of the system. Therefore, T-SRAMs are more suitable for ultra-low power applications. Here, we have analyzed seven different metrics (HSNM, RSNM, WSNM, SVNM, SINM, WTV and WTI) related to the reliability and robustness of the SRAMs. The read stability and the write ability of TFET and FinFET based SRAMs are evaluated for different PU:PD:PG ratio configurations. From the stability analysis, we can conclude that the T-SRAMs have better HSNM and RSNM compared to the F-SRAMs. However, the WSNM of the T-SRAMs is lower than the F-SRAMs. Most of the TFET device structures are still at the exploration stage, whereas the FinFET devices are already matured and in commercial fabrication stage. There are many material compositions and structural characteristics related factors of the TFET devices that need to be optimized to improve the reliability of the circuits and systems implemented by using these devices.

CHAPTER 5

GRAPHENE NANORIBBON FET BASED SRAM DESIGN

This chapter presents implementation and analysis of double gate SB-GNRFET based SRAM cell (G-SRAM). Moreover, the chapter provide detail benchmarking of G-SRAM and FinFET based SRAM cell (F-SRAM).

5.1 Selection of design paramaters for designing G-SRAM

Supply voltage of 500mV is opted for designing SRAM cell, because higher subthreshold swing and maximum I_{ON}-I_{OFF} ratio are achieved at this particular value [23], [24]. The next most important parameter is dimer lines (N), which affect the band gap and eventually the I_{ON}-I_{OFF} ratio as shown in Figure 41. Table 9 shows different categories of *N* based on I_{ON}-I_{OFF} ratio. Category-2 is more suitable for designing SRAM cell because of high I_{ON}-I_{OFF} ratio. Further, it is important to have low *N* value, as the width of GNR (W_{CH}) is depended on *N*. Therefore, N = 6 is opted for designing G-SRAM cell with the purpose to have low cell area.

Table 9: Categories of GNRs Based on Ion-Ioff Ratio With Respect to N.

Category	Dimer lines (N)	Band Gap	I_{ON}-I_{OFF} ratio
1	8, 11, 14 and 17	Small	Low
2	6, 7, 9, 10, 12, 13, 15, 16 and 18	Large	High

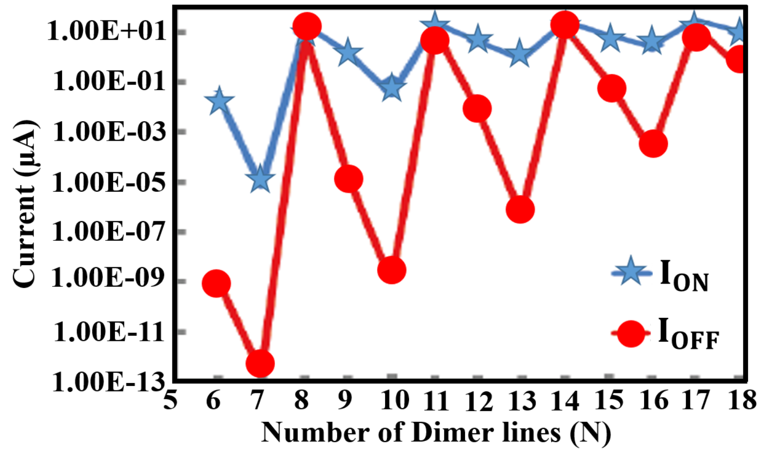


Figure 41: Variation of I_{ON} and I_{OFF} current with respect to *N* [23], [24].

5.2 Design and Analysis

From the starting of SRAM memory era, 6T SRAM is the most popular high density SRAM circuit. Figure 42 shows 6T SRAM cell design based on GNRFET. Reliable read and write operations are the crucial consideration in SRAM design. Due to the simplicity and symmetry of the 6T SRAM cell circuit it is very area efficient. However, special attention should be given for properly sizing the transistors to avoid read and write upsets, because the design is based on strict sizing ratios among the six transistors to ensure stable read and write operation. In the 6T SRAM, two bit lines are used to store and read the data. In this two bit-line architecture of 6T cell the bit lines are not electrically separated from the storage nodes during the read and write operations. This leads to inadvertent toggling of data stored in the cross-coupled inverter during the read operation. This increase the chances of error known as read upset. Apart from this, during read operation the voltage of storage node with logic “0”, increases to a certain value based on the voltage division between access and pull-down transistors. Increase in the voltage at storage node with logic “0”, leads to decrease in the voltage of storage node with logic “1”

because of the positive feedback characteristic. Yet, this enhancement in the voltage cannot flip the data of cell. Therefore, read operation is done successfully. However, write operation require strong access transistor to write data. Write ability of the cell reduces if minimum size access transistors are used. This challenge is referred as read and write access transistor sizing conflict. Due to the simplicity and symmetry of the 6T SRAM cell circuit it is very area efficient. However, special attention should be given for properly sizing the transistors to avoid read and write upsets, because the design is based on strict sizing ratios among the six transistors to ensure stable read and write operation. Table 10 shows the transistor width of G-SRAM.

Stability of the cell is a major concern while designing a new SRAM cell. Stability refers to the immunity of a cell against the noise to retain the data at the storage nodes Q and QB. It quantifies the maximum amount of the noise voltage SRAM cell can withstand without flipping the data at Q and QB [36]. For SRAM reliability analysis three different SNM figures are relevant. These are Hold Static Noise Margin (HSNM), Write Static Noise Margin (WSNM) and Read Static Noise Margin (RSNM).

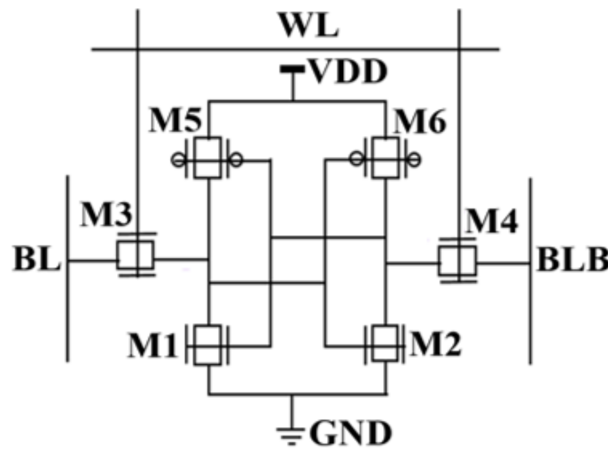


Figure 42: Schematic of 6T AUF SRAM cell.

Figure 43 shows the comparison of HSNM and RSNM of G-SRAM cell. The reliability and the robustness of the SRAM cell are investigated using greatly accepted N-curve method [16], [17]. This approach is used to determine the read stability as well as to measure the write ability. The N-curve illustrates the stability of the SRAM cell in terms of current. This current curve crosses zero at A, B and C as shown in Figure 44. The part between C and B represents write ability. The voltage difference between C and B is defined as write trip voltage (WTV). It is the voltage required to change the data of cell. The negative peak current between C and B is the write trip current (WTI). It is the current margin of the cell which changes the data stored at the storage node. Similarly, the part between A and B represents read stability. Static voltage noise margin (SVNM) is the voltage difference between A and B. It is the maximum tolerable DC noise voltage before flipping the content of the cell. The current peak between A and B is the Static current noise margin (SINM). It is the maximum current which can be injected in SRAM cell without flipping the data of cell [12]. Table 11 provides the N-curve parametric details of different configuration SRAM cells.

Table 10: Transistor width of 6T SRAM Bitcell.

SRAM cell	G-SRAM
Transistors	Number of GNRs
Pull up (M5, M6)	1
Access (M3, M4)	2
Pull down (M1, M2)	5

The uneven edges of SB-GNRFET result in a phenomenon called line edge roughness (p_r), which affects the properties of GNRs [19], [20]. p_r characterized the probability that any atom

on the edges of a GNR is removed. The removal of atoms has two effects on sub-bands and *N*. This disrupts the ballistic transport of device. Therefore, Monte Carlo simulations were performed to evaluate process variations of G-SRAM. For simulation, p_r was modeled as a ±1% Gaussian distribution with the variation set at the ±3σ level. Figure 45 show the Monte Carlo simulations of the G-SRAM with 1000 samples at 500mV supply voltage. The simulation results show the worst SVNM, the worst SINM, the worst WTV and the worst WTI respectively, under process variation.

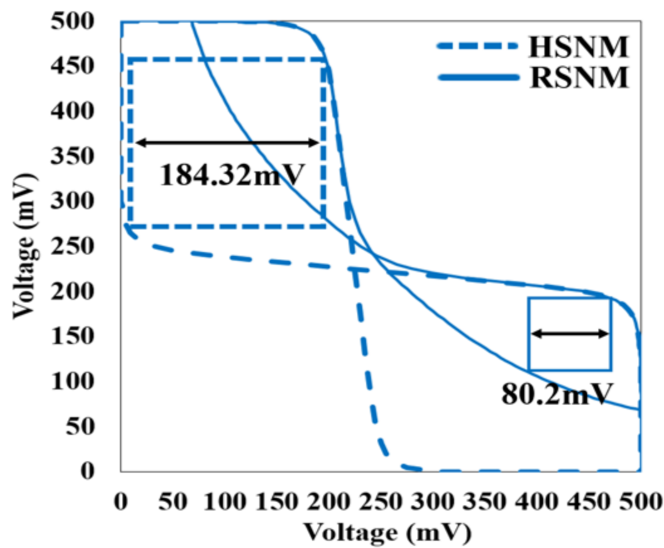


Figure 43: HSNM and RSNM analysis of SB type G-SRAM.

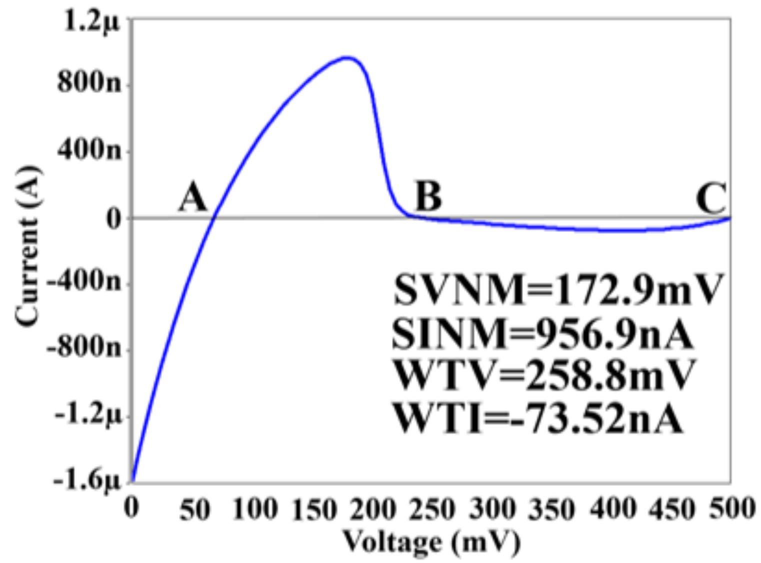


Figure 44: N-curve analysis of SB type G-SRAM.

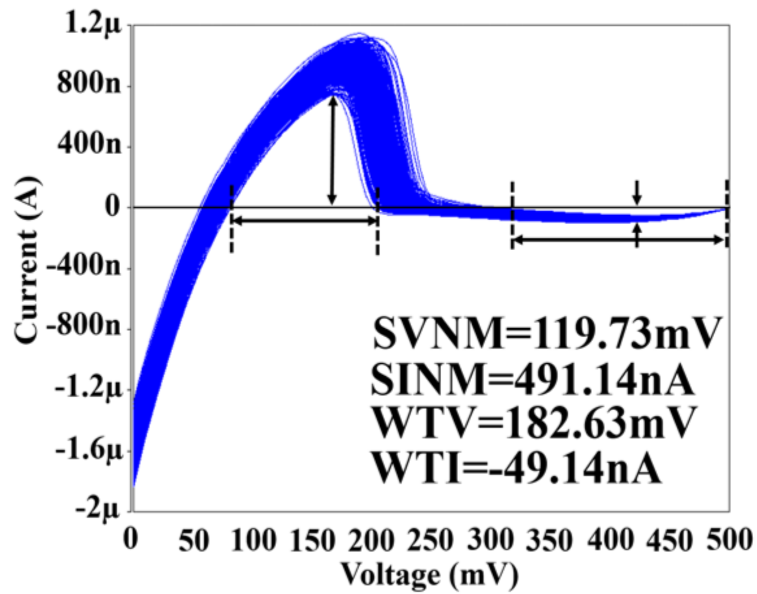


Figure 45: N-curve analysis of SB type G-SRAM under process variation.

5.3 Stability and reliability of MOS type G-SRAM bitcell

Stability of the cell is a major concern while designing a new SRAM cell. Stability refers to the immunity of a cell against the noise to retain the data at the storage nodes Q and QB. It quantifies the maximum amount of the noise voltage SRAM cell can withstand without flipping the data at Q and QB. SNM is extracted from the voltage transfer characteristics (VTC) of the two cross-coupled inverters in the memory cell. These cross-coupled inverters are in positive feedback connection. VTC of one of the inverters in the feedback loop is superimposed to the inverse VTC of another inverter in loop. The resulting plot is known as the butterfly curve. SNM of the memory cell is then extracted by placing the largest possible square in the butterfly curve. For SRAM reliability analysis three different SNM figures are relevant. These are Hold Static Noise Margin (HSNM), Write Static Noise Margin (WSNM) and Read Static Noise Margin (RSNM). Figure 46 shows the comparison of HSNM and RSNM of cell. Two of the most critical metrics in terms of the reliability and the robustness of the SRAMs are the read stability and the write ability. The reliability and the robustness of the SRAM cell are investigated using greatly accepted N-curve method. This approach is used to determine the read stability as well as to measure the write ability. The N-curve illustrates the stability of the SRAM cell in terms of current. Following setup is made to carry on the analysis. The proposed design is initially set to hold the “0”. DC noise source (I_{IN}) is connected to QB of the SRAM cell. Both bit-lines BL and BLB are clamped to VDD. Then a DC sweep is performed on QB to get the current waveform through I_{IN}. This current curve crosses zero at A, B and C as shown in Figure 47. The part between C and B represents write ability. The voltage difference between C and B is defined as write trip voltage (WTV). It is the voltage required to change the data of cell. The negative peak current between C and B is the write trip current (WTI). It is the current margin of the cell which

changes the data stored at the storage node. Similarly, the part between A and B represents read stability. Static voltage noise margin (SVNM) is the voltage difference between A and B. It is the maximum tolerable DC noise voltage before flipping the content of the cell. The current peak between A and B is the Static current noise margin (SINM). It is the maximum current which can be injected in SRAM cell without flipping the data of cell. Table 11 provides the N-curve parametric details of different configuration SRAM cells. Monte Carlo simulations were performed for the T-SRAMs to evaluate process variations. For simulation, f_{dop} was modeled as a ±5% Gaussian distribution with the variation set at the ±3σ level. Figure 48 show the Monte Carlo simulations of the G-SRAM with 2000 samples at the 500mV supply voltage. The simulation results show that with the process variation the worst SVNM, the worst SINM and the worst WTV for 1:5:2 configuration of the T-SRAM are 1.01, 11.86 and 1.9 times better than the 1:1:1 configuration of the T-SRAM in the ideal case, respectively.

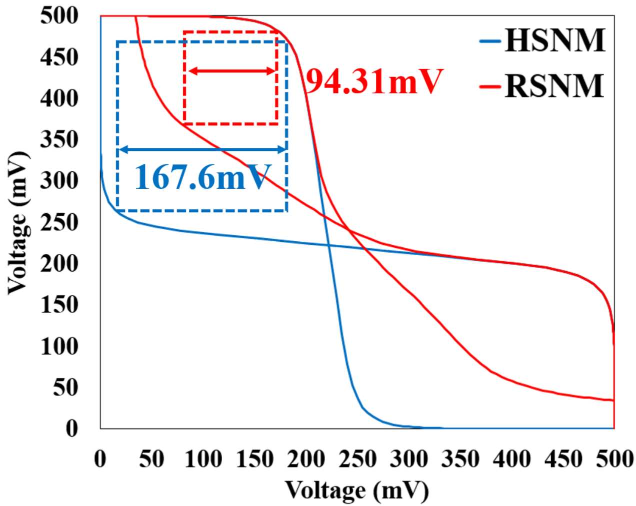


Figure 46: HSNM and RSNM analysis of MOS type G-SRAM at 500mV supply.

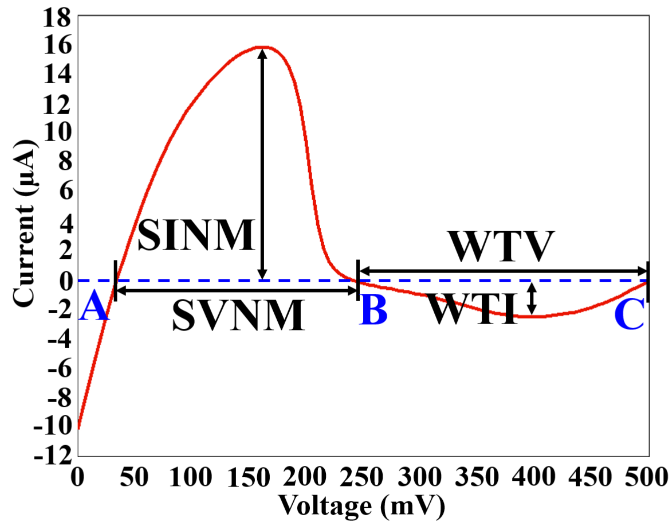


Figure 47: N-curve analysis of MOS type G-SRAM cell.

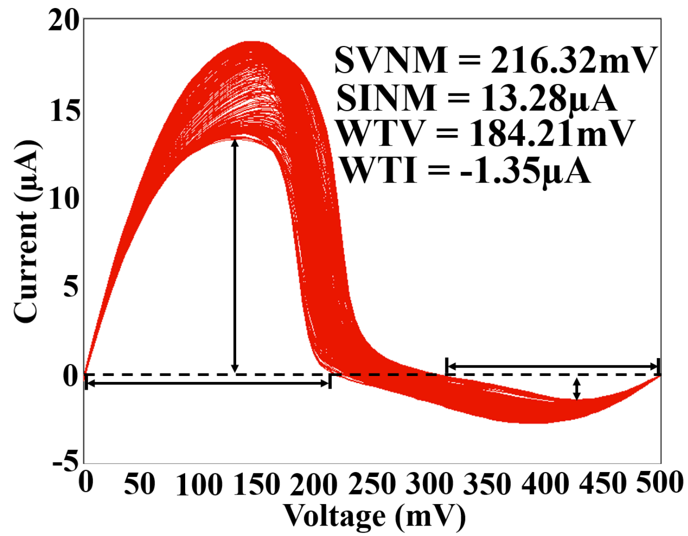


Figure 48: N-curve analysis of MOS type G-SRAM cell under process variation.

Table 11: Performance summary of MOS-SRAM and SB-SRAM

Design		MOS type G-SRAM	SB type G-SRAM
Technology		10 nm	
Supply Voltage		500mV	
PU:PD:PG		1:5:2	
Standby leakage power (nW)		14.84	45.23 p
Read	Power (nW)	267.7	48.7
	Delay (nS)	2.953	32.19
	Energy(J)	7.9E-16	1.56E-15
Write	Power (nW)	351.44	3.58
	Delay (nS)	0.42	0.019
	Energy(J)	1.47E-16	6.8E-20
HSNM (mV)		167.6	184.32
RSNM (mV)		94.31	80.2
WSNM(mV)		243.5	232.46
SVNM (mV)		239.11	172.9
SINM (μ A)		15.88	959.9 n
WTV (mV)		192.52	258.89
WTI (μ A)		-4.62	-73.52 n

5.4 Summary

From the analysis, it is clear that the main advantage of the double gate SB-GNRFET and MOS-GNRFET based SRAMs would be the significant improvement in terms of leakage or standby power consumption. Compared to the FinFET based SRAM the standby leakage power of the SB-GNRFET and MOS-GNRFET are 5E+03 and 16.43 times less. Since leakage/standby power is the primary source of power consumption in the SRAM, and the overall system energy efficiency depends on SRAM power consumption SB-GNRFET and MOS-GNRFET based SRAM would lead to massive improvement of the energy efficiency of the system. Therefore, SB-GNRFET and MOS-GNRFET is more suitable for ultra-low power applications. Finally, from the stability analysis, we can conclude that the G-SRAM have better stability compared to the F-SRAM.

CHAPTER 6

DOUBLE-GATE FDSOI BASED SRAM DESIGNS

Power saving techniques have become essential for modern digital systems. Large on-chip SRAM memories are used in these systems and therefore it is necessary to optimize SRAM bitcell circuit to minimize the power consumption. In addition to this, it is equally important to design SRAM cell with high reliability and stability. Power gating technique with sleep transistor if applied to SRAM cell will degrade the performance of the cell. In this chapter, Fully Depleted Silicon-on-Insulator (FDSOI) device based SRAM designs are proposed which eliminate the requirement of sleep transistors to reduce the power consumption. This reduces overall complexity and overheads of power gating memory designs.

6.1 Introduction

Power gating is a promising technique utilized to minimize power consumption in the SRAM designs. Sleep transistors aid in managing the power and thermal effects of the design. Conventional sleep transistor based power gating configurations are shown in Figure 49. High threshold voltages (V_{TH}) header and footer sleep transistors are utilized to isolate actual supply lines from virtual supply lines. High-V_{TH} sleep transistors are placed between the SRAM bitcells and the supply lines to reduce leakage power during standby. However, these high-V_{TH} sleep transistors occupies extra area and increases delay and power. In addition this, extra wiring for

virtual nodes will further increase unwanted RLC issues and IR-drops [61]. To overcome these limitations, double-gate FDSOI [62]-[65] are used to design SRAM bitcell circuit. This design approach eliminates sleep transistors, which reduces the area overheads and improve the performance of the SRAM bitcell. Main idea is to exploit the back gate (BG) bias in double-gate FDSOI to get the required V_{TH} dynamically without using sleep transistors. Since no additional transistors are required for power gating, there is need to dynamically set high and low V_{TH} values in the same FDSOI device. During write and read lower V_{TH} is preferred for higher gate drive. However, during hold mode, high V_{TH} is preferred to decrease standby leakage power.

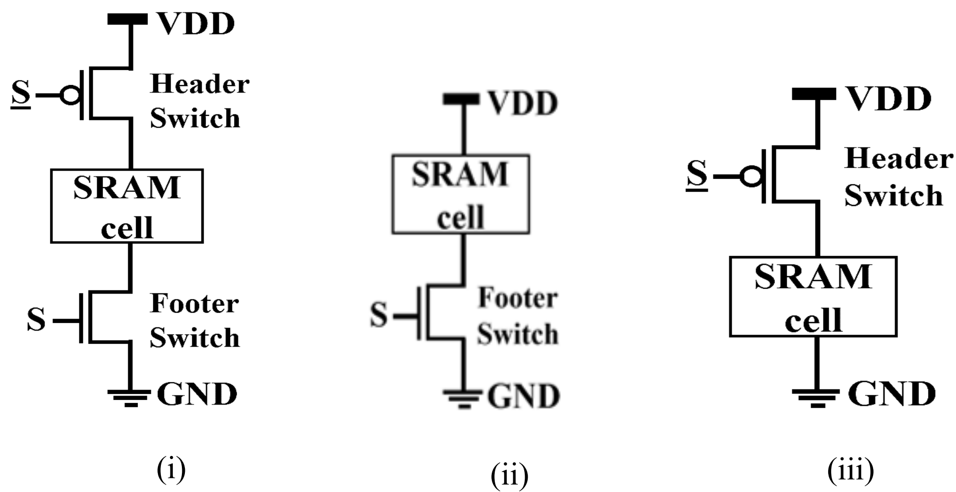


Figure 49: Conventional power gating configuration of SRAM.

6.2 Double Gate FDSOI Device

The double-gate FDSOI device can be viewed as two MOSFETs (front and back) that share same body, drain, and source regions as shown in Figure 50. An additional back gate contact is provided under the substrate. Two gates of the device control the charges in the silicon channels. The silicon film thickness in FDSOI, is typically less or equal to half of the depletion width of

the bulk device [66], [67]. Drain current and V_{TH} of the devices, are subjective to the film thickness. Thin films are required to have great control over the performance of the device because the V_{TH} of FDSOI devices are sensitive to the variations in SOI silicon film thickness (Tsi) [67]. Moreover, thin SOI film is required to minimize short-channel effects in the SOI MOSFETs [62]. The surface potentials of the FDSOI device at the front and back interfaces are firmly coupled to each other and capacitively coupled to the front-gate and the substrate via the front-gate oxide and buried oxide [67]. Threshold voltage (V_{TH}) of double gate FDSOI is dependent on the BG voltage of FDSOI as shown in Figure 51. V_{TH} of FDSOI is evaluated by equation (1) and (2) [61].

$$V_{TH_F} = V_{FB_F} + 2\Phi_B - \frac{Q_B}{2C_{OX}} - \left(V_{BG} - V_{FB_B} - 2\Phi_B + \frac{Q_B}{2C_{BOX}}\right) \times \frac{C_{SI}C_{BOX}}{C_{OX}(C_{SI} + C_{BOX})} \quad (1)$$

$$Q_B = -qN_A TT_{Si}\ (or) + qN_D TT_{Si} \quad (2)$$

Where V_{FG} and V_{BG} are front and back gate voltages. V_{FB_F} and V_{FB_B} are front and back gate flatband voltages. C_{OX} are front and back gate oxide. C_{BOX} and C_{SI} are buried oxide and depleted silicon film capacitances. Q_B is the area charge density in depleted Si film.

6.3 FDSOI based 6T SRAM Bitcell Design

The conventional 6T SRAM cell has been the industry standard from the beginning of the SRAM era. Reliable read and write operations are the vital concern in SRAM design. Due to the straightforwardness and symmetry of the 6T SRAM cell circuit it is very area efficient.

However, in this two bit-line architecture of 6T cell the bit lines are not electrically separated from the storage nodes during the read and write operations. The cell is highly vulnerable to the noise during read operation. Voltage of the storage node with "0" rises to a higher voltage than ground due to voltage division along access (M5, M6) and pull down (M1, M2) transistors, in the middle of precharged bitlines (BL and BLB) and the ground terminal of the SRAM cell. This situation may end up with reading a wrong value, usually known as read upset. Detail explanation of 6T SRAM bitcell operations are available in [68] for interested readers. In current micro and nano electronic circuits and systems, the major source of power consumption is the leakage current. This chapter present seven different configurations of double-gate based FDSOI SRAM bitcell designs to minimize leakages and improve performances as shown in Figure 52. Table 12 shows the performance summary of different FDSOI based SRAM bitcell configurations.

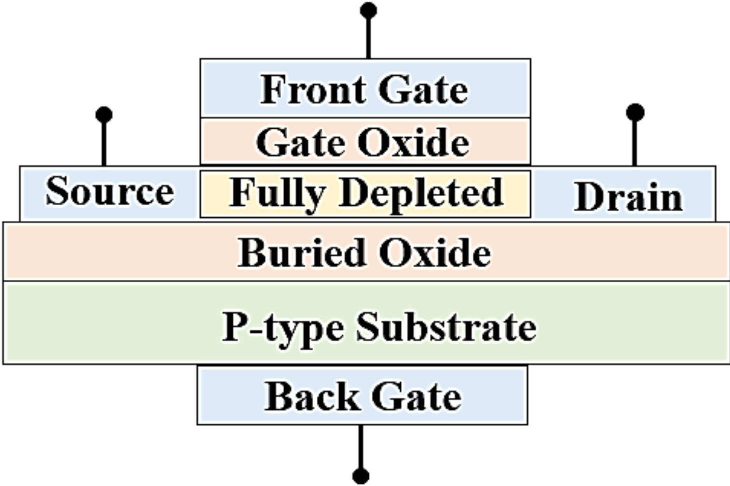


Figure 50: FDSOI MOSFET device [62]-[65].

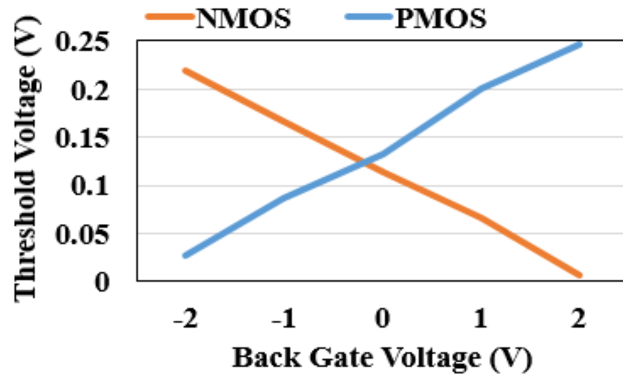
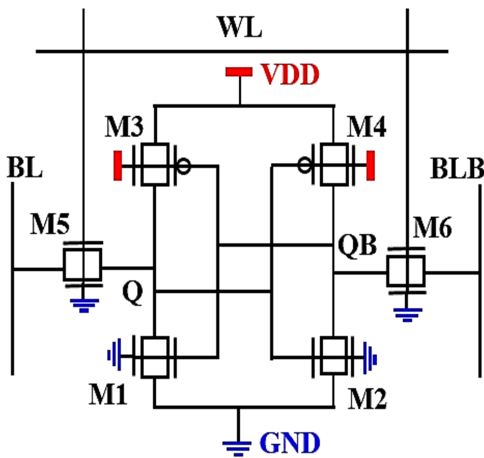
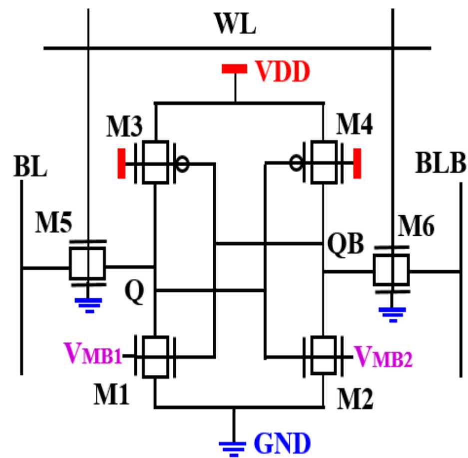


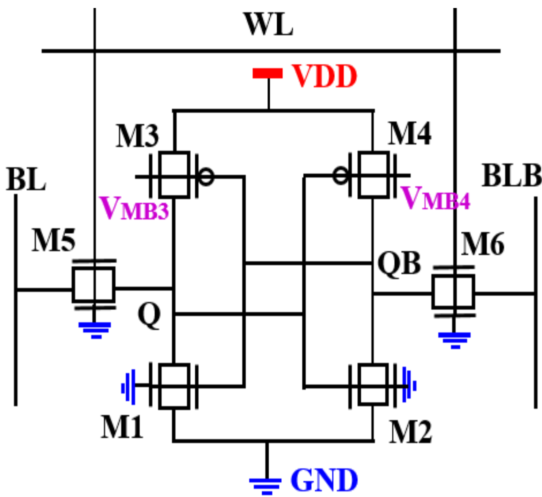
Figure 51: Dependence of threshold voltage upon back gate bias [61].



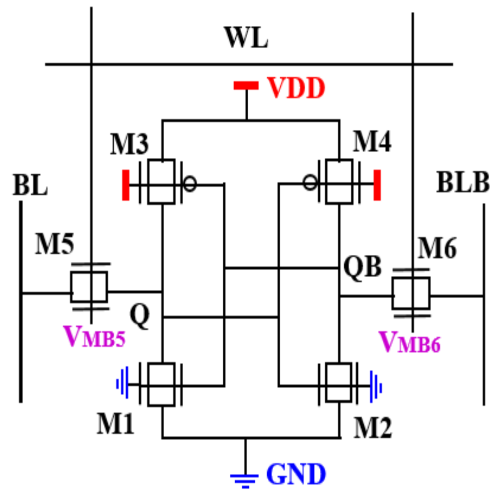
(i) Standard Configuration (C1)



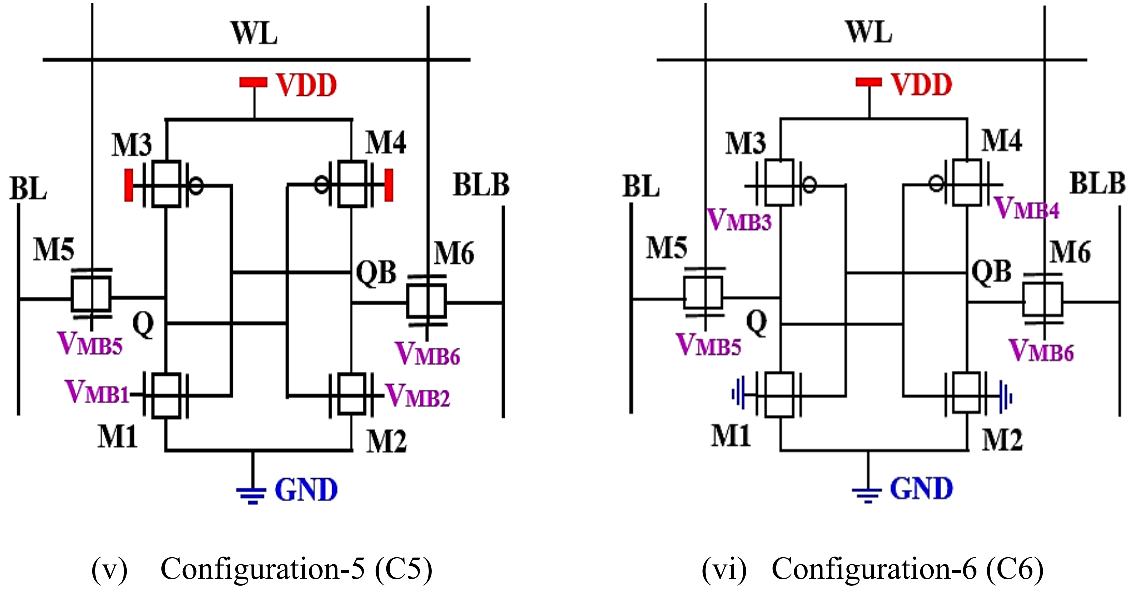
(ii) Configuration-2 (C2)



(iii) Configuration-3 (C3)



(iv) Configuration-4 (C4)



(v) Configuration-5 (C5)   (vi) Configuration-6 (C6)

Figure 52: Different configurations of double-gate FDSOI based SRAM bitcell.

Table 12: Performance summary of different FDSOI based SRAM bitcell configurations.

Power gating SRAM bitcell design		(C1)	(C2)	(C3)	(C4)	(C5)	(C6)	(C7)	(C8)
Voltage (V)		1							
Total Power (μW)	Read	12.098	12.451	15.268	11.942	12.322	12.876	12.528	2.323
	Write	40.833	44.65	46.807	46.08	40.199	46.03	49.29	39.966

Standby Leakage Power (nW)		28.77	19.21	49.36	19.23	28.67	49.27	136.98	49.28
Leak-age Curr-ent (A)	Hold	418.96 n	418.96 n	437.16 n	418.96 n	418.96 n	437.16 n	437.16 n	437.15 n
	Read	421.86 n	421.86 n	62.994 µ	421.86 n	485.09 n	66.894 µ	66.894 µ	62.993 µ
	Write	81.89 µ	60.868 µ	170.74 µ	60.853 µ	150.45 µ	177.23 µ	177.23 µ	168.91 µ
Del-ay (nS)	Read	0.415	0.413	0.409	0.365	0.394	0.412	0.360	0.398
	Write	0.462	0.459	0.447	0.409	0.365	0.444	0.46	0.353
Ener-gy (fJ)	Read	5.02	5.142	6.24	4.35	4.85	5.43	4.51	0.924
	Write	10.88	20.05	20.92	10.88	14.67	20.43	22.67	14.10
N-curve	SVNM (V)	0.325	0.325	0.348	0.325	0.325	0.348	0.348	0.348
	SINM (µA)	133.42	133.42	139.95	133.42	133.42	139.95	139.95	139.95
	WTV (V)	0.5055	0.5055	0.4928	0.5055	0.5055	0.4928	0.4928	0.4928

WTI (μA)	51.552	51.552	58.42	51.552	51.552	58.42	58.42	58.42

Two of the most critical metrics in terms of the reliability and the robustness of the SRAMs are the read stability and the write ability. The N-curve illustrates the stability of the SRAM cell in terms of current. Following setup is made to carry on the analysis. The proposed design is initially set to hold the “0”. DC noise source (IIN) is connected to QB of the SRAM cell. Both bit-lines BL and BLB are clamped to VDD. Then a DC sweep is performed on QB to get the current waveform through IIN. This current curve crosses zero at A, B and C as shown in Figure 53. The part between C and B represents write ability. The voltage difference between C and B is defined as write trip voltage (WTV). It is the voltage required to change the data of cell. The negative peak current between C and B is the write trip current (WTI). It is the current margin of the cell which changes the data stored at the storage node. Similarly, the part between A and B represents read stability. Static voltage noise margin (SVNM) is the voltage difference between A and B. It is the maximum tolerable DC noise voltage before flipping the content of the cell. The current peak between A and B is the Static current noise margin (SINM). It is the maximum current which can be injected in SRAM cell without flipping the data of cell.

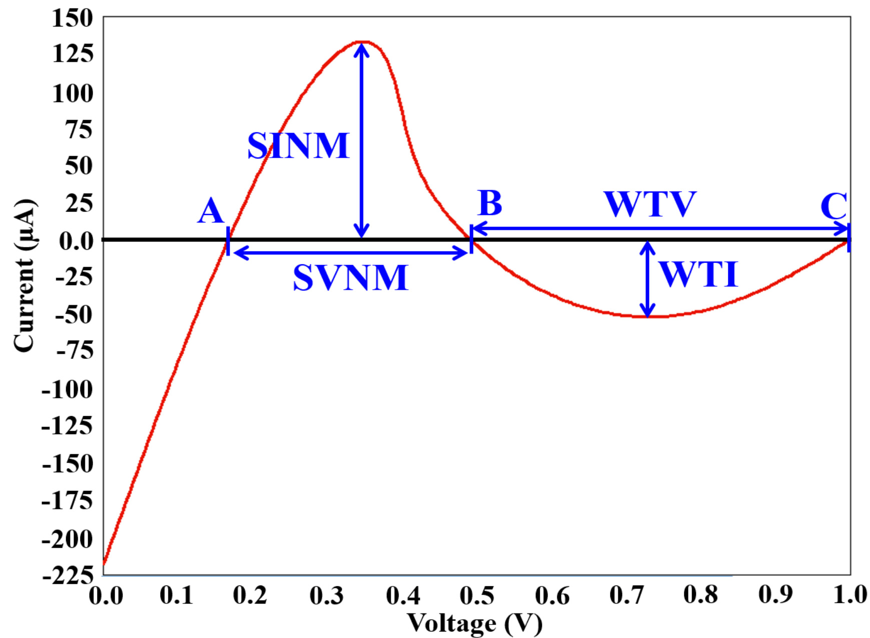


Figure 53: N-curve analysis of C1 configuration SRAM cell.

6.4 Benchmarking of FDSOI Based SRAM cells

Table 7 compares the performance and reliability of different configuration SRAM cells with the standard configuration SRAM cell. The physical significances of benchmarking are discussed below.

- C4 and C8 configuration SRAM cells consume 1.31% and 420.79% less power during read compared to standard C1 configuration SRAM cell. However, C2, C3, C5, C6 and C7 consume 2.84%, 20.76%, 1.82%, 6.04% and 3.43% more power during read compared to standard C1 configuration SRAM cell.

- C5 and C8 configuration SRAM cells consume 1.58% and 2.17% less power during write compared to standard C1 configuration SRAM cell. However, C2, C3, C4, C6 and C7

consume 8.55%, 12.76%, 11.39%, 11.29% and 17.16% more power during write compared to standard C1 configuration SRAM cell.

- Standby leakage power of C2, C4 and C5 configuration SRAM cells are 49.77%, 49.61% and 0.35% less than standard C1 configuration SRAM cell. Whereas, standby leakage power of C3, C6, C7 and C8 configuration SRAM cells are 41.71%, 41.61%, 79% and 41.62% more than standard C1 configuration SRAM cell.

- Leakage current of C2, C4 and C5 configuration SRAM cells are nearly equal to standard C1 configuration SRAM cell in hold mode. However, leakage current of C3, C6, C7 and C8 are ~ 4.16% more than standard C1 configuration SRAM cell in hold mode.
- During read, leakage current of C3, C6, C7 and C8 configuration SRAM cells are 569.68%, 530.64%, 530.6% and 569.69% less compared to standard C1 configuration SRAM cell. However, leakage current during read for C2, and C4 configurations are nearly equal to C1 configuration, and C5 configuration leakage current during read is 13.03% more than standard C1 configuration SRAM cell.

- During write, leakage current of C2, and C4 configuration SRAM cells are 34.54% and 34.57% less compared to standard C1 configuration SRAM cell. However, leakage current during write for C3, C5, C6, C7 and C8 configurations are 52.04%, 45.57%, 53.79%, 53.7% and 51.52% more than standard C1 configuration SRAM cell.

- C2, C3, C4, C5, C6, C7 and C8 configuration SRAM cells read 0.48%, 1.47%, 13.7%, 5.33%, 0.73%, 15.28% and 4.27% faster than standard C1 configuration SRAM cell.

- C2, C3, C4, C5, C6, C7 and C8 configuration SRAM cells write 0.65%, 3.367%, 12.96%, 26.58%, 4.05%, 0.43% and 30.88% faster than standard C1 configuration SRAM cell.

- Compared to standard C1 configuration; C4, C5, C7 and C8 configuration SRAM cells consume 15.4%, 3.51%, 11.31% and 443.29% less energy during read. However, energy consumed by C2, C3 and C6 configuration SRAM cells are 2.37%, 19.55% and 7.55% more than standard C1 configuration SRAM cell during read.

- Write energy consumption of C4 configuration SRAM cell is 0.02% less than standard C1 configuration SRAM cell. Whereas, all the other configurations have higher write energy consumption compared to standard C1 configuration SRAM cell.

- From combined SVNM and SINM information, it can be concluded that C3, C6, C7 and C8 configuration SRAM cells have better read stability than standard C1 configuration SRAM cell. However, C3, C6, C7 and C8 configuration SRAM cells have lower write ability compared to the standard C1 configuration SRAM cell.

6.5 Conclusion

In this chapter, different performance metrics and stability of double-gate FDSOI based SRAM bitcell designs is evaluated. From the analysis, it is observed that C8 configuration SRAM cell consumes 443.29% less read energy and write 51.52% faster compared to standard C1 configuration SRAM cell. C4 configuration SRAM cell have least write energy. Moreover, the standard configuration (C1) reads and writes slower compared to other configuration SRAM cells. Among all the configurations, C7 reads fastest. Therefore, from the analysis, it is observed that C8 configuration SRAM cell is more suitable for low power and high-speed applications. Our future work will include detail analysis of SRAM array with different FDSOI based SRAM bitcell configurations.

CHAPTER 7

NOVEL CNTFET AND MEMRISTOR BASED DIGITAL DESIGNS

Multi-valued logic (MVL) gates are expected to be the future platforms for the beyond-binary circuits and systems. We propose a novel standard ternary inverter (STI) design based on carbon nanotube FET (CNTFET) and memristor. There have been many approaches like resistive load and multi-threshold designs to implement ternary logic gates. The implementation of the MVL technologies is challenging using the existing standard CMOS technology due to its scaling related issues in the sub-nanoscale regime. For example, the resistive load MVL implementations would consume excessive chip area. One of the advantages of the proposed design is the fact that the threshold voltage of the CNTFET can be adjusted by varying the chirality vector. Memristor behaves like a resistor outside a specific frequency range, and it has the potential to offer significantly lower leakage and power dissipation compared to the conventional resistor. Performance and stability of the proposed design have been compared to the existing CNTFET based design.

7.1 Introduction

One of the major challenges of the computing system design in nanoscale regime is the interconnect limitation. Majority of the delay, power consumption and noise are contributed by the interconnect lines in the conventional binary logic system used to design integrated circuits.

Increasing information density and processing speed would be impossible in near future if we stay in binary platform [69]. To implement very high-density logic and information system, we need to rely on multi-valued logic (MVL) technologies. Ternary logic provides exponentially higher data density with the lower circuit and interconnect overheads leading to lower parasitic effects, power consumption and delay. As a result, the ternary logic can perform the serial-parallel arithmetic operations at much higher speed compared to the binary logic [69].

Many different MVL approaches like the resistive load and multi-threshold designs have been proposed [69]-[73]. These conventional CMOS technology-based approaches suffer from scaling related limitations like short channel effects. The resistive load MVL technique imposes very high area overhead. Carbon Nanotube Field Effect Transistor (CNTFET) is a very promising technology that can exploit the excellent material and electrical properties of CNTs to overcome the limitations of the CMOS devices. CNTs provide ballistic transport of the charge carriers in the channel leading to lower propagation delay and power consumption. Memristor (or memory resistor) is a two-terminal passive element with a unique non-linear feature, which is not observed in other two-terminal components like resistors, inductors, or capacitors. It behaves as a linear resistor above specific frequency [74], and it has lower leakage and power dissipation compared to the conventional resistor. In multi-threshold CMOS design, the threshold voltage (VTH) is adjusted by applying different bias voltages. In CNTFET, we can achieve different VTH by varying the diameter (chirality vector) of the CNTs. In [72], (Figure 44a), a ternary logic gate design is proposed using CNTFET and the conventional resistor. This design requires two CNTFETs and two 100kΩ resistors. In this design, large resistors are employed to meet the current requirement of the CNTFETs. These large resistors inside the logic gates would impose severe parasitic effects and very high area and power overheads [72]. Usage

of physical resistors for logic design is fundamentally very challenging and inefficient. A new ternary logic gate based only on CNTFETs has been proposed in [75] (Figure 44c). Here the issues related to large resistors are eliminated by employing P-type transistor load. This design requires three P-type and three N-type CNTFETs. We propose a new ternary inverter design using only two CNTFETs and two memristive devices (Figure 45a). The circuit of the proposed ternary inverter contains one P-type and one N-type CNTFETs. The number of CNTFET devices is reduced, and the resistors are replaced by the memristors. The new design will lead to lower area and power consumption, and higher stability and reliability of the logic states in the proposed ternary logic gate compared to the existing STI concepts [72], [75]. In this chapter, different performance metrics of the proposed design are compared to the existing designs using 900mV supply voltage (VDD).

7.2 Fundamentals of Ternary Logic

The conventional binary logic system has only two logic states '0' and '1', which is a radix 2 logic system. If the radix value is more than 2, it is called as multivalued logic. Thomas Fowler introduced an alternate method of computation using a ternary logic system, which can be classified as balanced (-1, 0, 1) and unbalanced (0, 1, 2) ternary logic system [76]-[79]. Table 13 shows the fundamental operations of ternary logic, where $a_i, a_j \in \{0, 1, 2\}$ [70]. The inverter is the most elementary block of any digital design. It has one input (V_{in}) and one output (V_{out}). Three different types of ternary inverters are available based on the output equations as shown in Table 14.

Table 13: Fundamental operatrions of Ternary Logic [66].

Operation	Equation
OR	$\mathrm{A_i} + \mathrm{A_j} = \max\{\mathrm{A_i}, \mathrm{A_j}\}$
AND	$\mathrm{A_i} \cdot \mathrm{A_j} = \min\{\mathrm{A_i}, \mathrm{A_j}\}$
NOT	$\overline{\mathrm{A_i}} = 2 - \mathrm{A_i}$

Table 14: Different types of Ternary Inverters.

Ternary Inverter	Standard Ternary Inverter (STI)			Positive Ternary Inverter (PTI)			Negative Ternary Inverter (NTI)		
Output Equation	$V_{out} = 2 - V_{in}$			$V_{out} = \begin{cases} 2 & if\ V_{in} = 0 \\ 0 & if\ V_{in} \neq 0 \end{cases}$			$V_{out} = \begin{cases} 2 & if\ V_{in} = 0 \\ 0 & if\ V_{in} \neq 0 \end{cases}$		
Input (V_{in})	0	1	2	0	1	2	0	1	2
Output (V_{out})	2	1	0	2	2	0	2	0	0

7.3 Beyond CMOS Nano Devices

7.3.1 Carbon Nanotube Field Effect Transistor (CNTFET)

Carbon nanotubes (CNTs) are graphene sheets rolled in cylindrical structure. One of the key defining parameters of the CNTs is chirality, which depends on the rolling angle of the graphene sheet. CNT is a very promising material for field effect transistor (FET) design. CNTFET

provides ballistic transport of the charge carriers in the channel, which improves the propagation delay and power consumption of the device. Additionally, CNTFET has good material and electrical properties, which make it a promising alternative to the CMOS devices. CNTs come in two different forms – single-wall CNT (SWCNT) and multi-wall CNT (MWCNT). The SWCNT is preferred to design ternary logic gates. It has only one cylinder and therefore, the manufacturing process is simpler [71]. The chirality vector, represented as a pair of integers (n,m), determines whether SWCNT behaves as a conductor or a semiconductor. A CNT is metallic for n=m or n-m=3i, where i is an integer. Else, it behaves like a semiconductor. The diameter (D_CNT) and threshold voltage (V_TH) of CNT can be determined using equations (3) and (4) [76], [80] and [81].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{3}$$

$$V_{TH} = \frac{aV_\pi}{\sqrt{3}eD_{CNT}} \tag{4}$$

Here, $\mathrm{a_0} = 0.142\mathrm{nm}$ is the inter-atomic distance between each carbon atom and its neighbor, $\mathrm{a} = 2.49\mathrm{A}°$ is carbon-to-carbon atom distance, $\mathrm{V_\pi} = 3.033\mathrm{eV}$ is carbon $\pi - \pi$ bond energy, and e is electron charge. By varying CNTFET chirality vector or $\mathrm{D_{CNT}}$, V_{TH} can be controlled. In the CNTFET design, undoped CNT segments are placed below the gate, whereas heavily doped CNT segments are placed between the gate and the source/drain terminals as shown in Figure 54. This arrangement reduces the series resistance during the ON state.

7.3.2 Memristor

Memristors are a passive two-terminal element with variable resistance (memristance) introduced by Leon Chua in 1971. According to Leon, memristance (M) is the missing relation between the flux ($\varnothing$) and the charge (q) as shown in equation (5) [82], where $\varnothing(q)$ defines the relation of the flux and the charge of the memristor, charge $q(t)$ is the state variable and $M(q(t))$ is called the memristance.

$$\mathrm{M}(\mathrm{q}(\mathrm{t})) = \mathrm{d}\varnothing(\mathrm{q})/\mathrm{dq} \quad (5)$$

Linear dopant memristor model [77], [78] is used to design the ternary logic circuits. One of the potential ways to fabricate a memristor is to place a thin film of TiO_2 sandwiched between Platinum (Pt) metallic contacts [78]. Memristor has two layers as shown in Figure 55. The intrinsic TiO_2 layer (R_{OFF} region) have high resistivity, while the doped TiO_2 layer (R_{ON} region) is highly conductive. The electric field applied across the memristor is responsible for the change in the width of the doped region (W). The full width of the TiO_2 layer is represented as D. The width of the R_{ON} region determines the state variable ($x = W/D$) and its resistance. The total resistance of memristor depends on the current as well as the direction of current passing through it. The value of resistance varies with the change in the direction of current as shown in Figure 56. The linear model is governed by equation (6), where, v is the voltage applied across the memristor, i is the current flowing through the memristor, M is the memristance, μ is the drift mobility of charges and x is the state variable that defines the ON state for allowed values between the unity and the OFF state for zero.

$$v = M(x)i$$

$$M(x) = R_{ON}x + R_{OFF}(1 - x)$$

$$x(i) = \frac{\mu R_{ON}}{D^2} i(t) \quad (6)$$

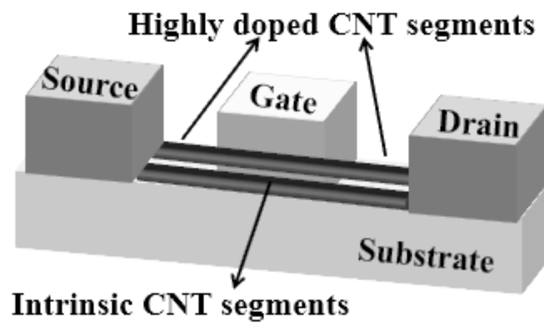


Figure 54: Fundamental structure of CNTFET.

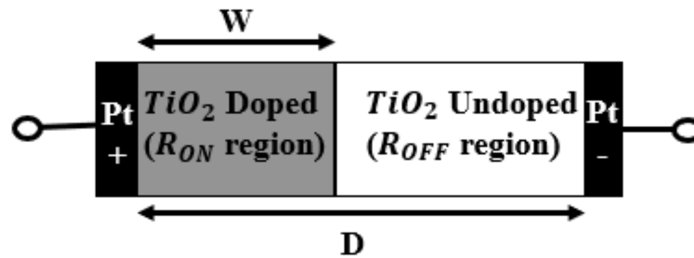
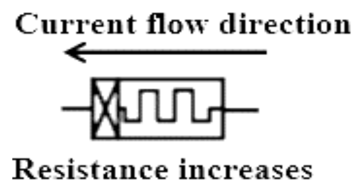
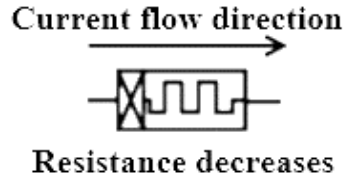


Figure 55: Device structure of Memristor.



(a)



(b)

Figure 56: Behavior of the memristor with respect to the direction of the current flow.

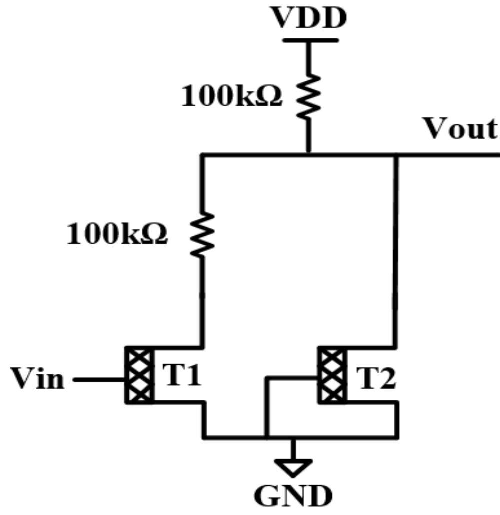
7.4 Existing CNTFET Standard Based Ternary Inverter (STI) Design

7.4.1 CNTFET and Resistor based STI Design

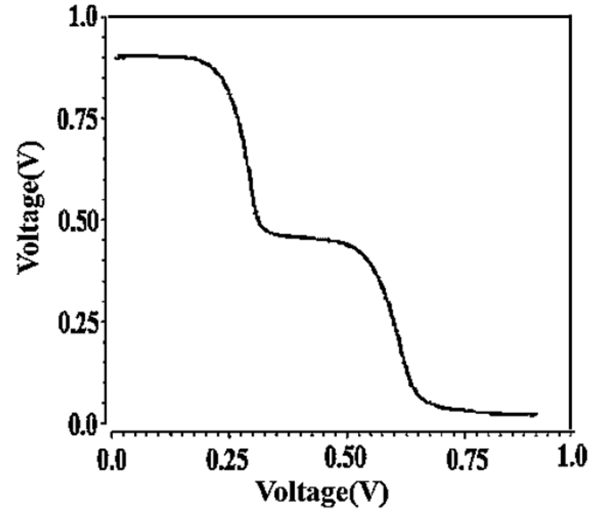
Dual-diameter CNTFETs and resistors are employed in [72]. The schematic and the voltage transfer characteristic (VTC) of the STI presented in [72] are shown in Figure 57(a) and Figure 57 (b). The diameter of the transistors T1 and T2 are 1.487nm and 0.783nm, and the V_{TH} of the transistors T1 and T2 are 290mV and 550mV, respectively, according to equation (4). Two 100kΩ resistors are employed in the design to meet CNTFETs current requirement. These large resistors significantly increase the area and power consumptions of the STI.

7.4.2 CNTFET based STI Design

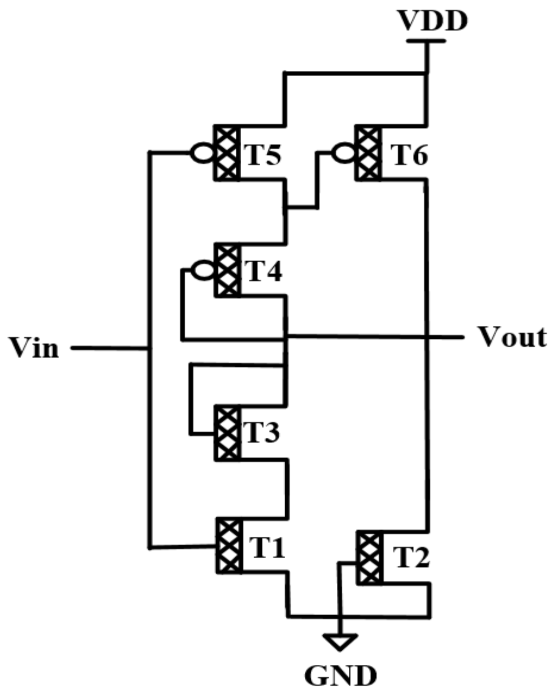
In [75], the requirement of the large resistance as in [72] is eliminated by employing P-type transistor load. However, the number of the CNTFETs in the design increases. The design uses six dual-diameter CNTFETs. The schematic and the VTC of the device proposed in [75] are shown in Figure 57(c) and Figure 57(d). The diameter of the transistors are T1 = T5 = 1.487nm, T2 = T6 = 0.783nm, and T3 = T4 = 1.018nm. Therefore, according to equation (4), the V_{TH} of the transistors T1, T2, T3, T4, T5, and T6 are 289mV, 559mV, 428mV, -0.289mV, -559mV and -428mV, respectively.



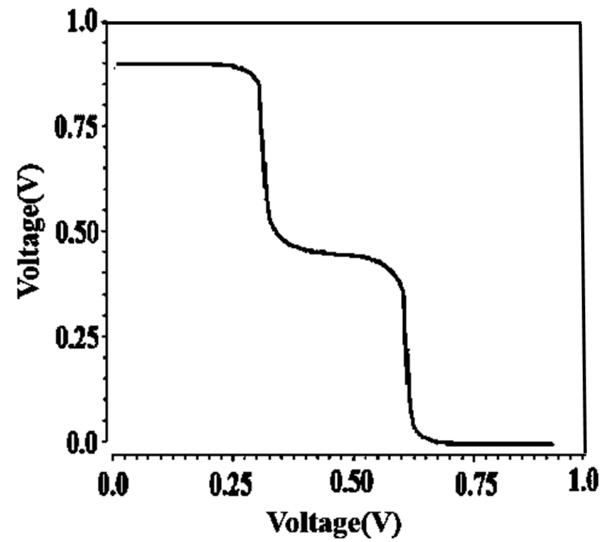
(a)



(b)



(c)



(d)

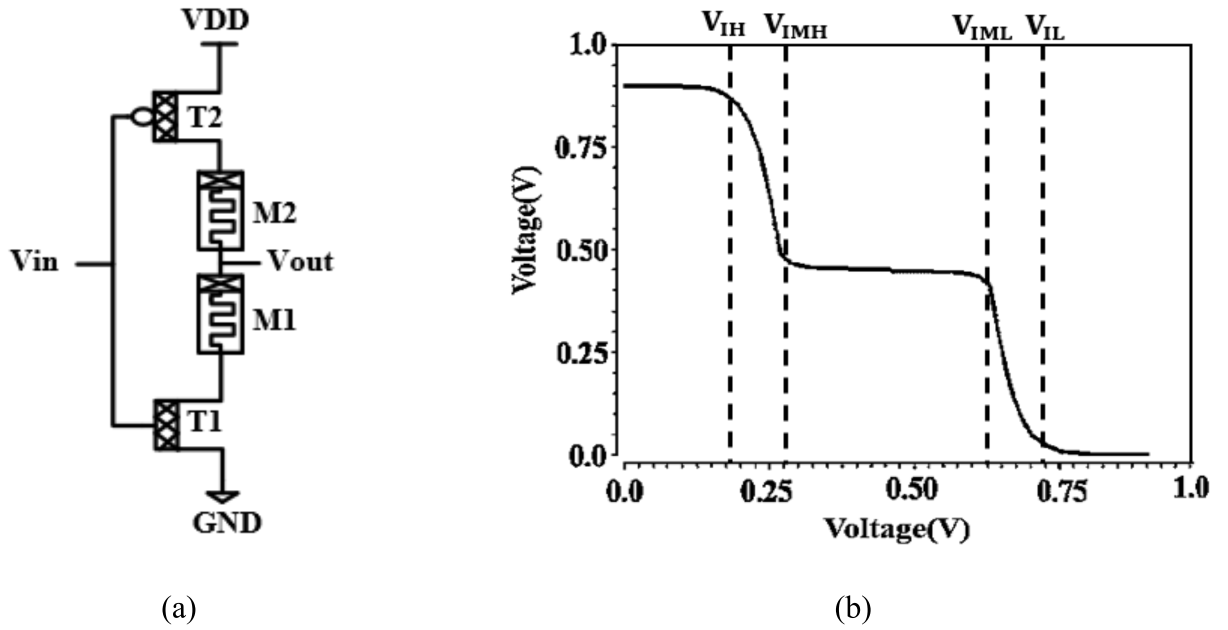
Figure 57: (a) Schematic of CNTFET and Resistor based STI [72] (b) VTC of CNTFET and Resistor based STI [72], (c) Schematic of CNTFET based STI [75], (d) VTC of CNTFET based STI [75].

7.5 Proposed CNTFET and memristor based STI design

The proposed STI uses two single-diameter CNTFETs and two memristors. The schematic and the VTC of the proposed design are shown in Figure 58(a) and Figure 58(b). The requirement of a large resistance is eliminated by utilizing two memristors (M1 and M2) that separate the drains of the CNTFETs (T1 and T2) and behave as resistors. As we know, memristors behave as nonlinear devices with hysteresis property for a specific frequency range and above that frequency range memristors act like a linear resistor. In the proposed design, the memristors behave as resistors. To satisfy this need, we selected memristors that show resistive behavior above 1Hz [74] so that the proposed STI can be used for any practical application. The benefits of utilizing the resistive behavior of the memristors instead of using actual resistors are the minimization of area overheads and power consumption, and the improvement of stability of the logic states.

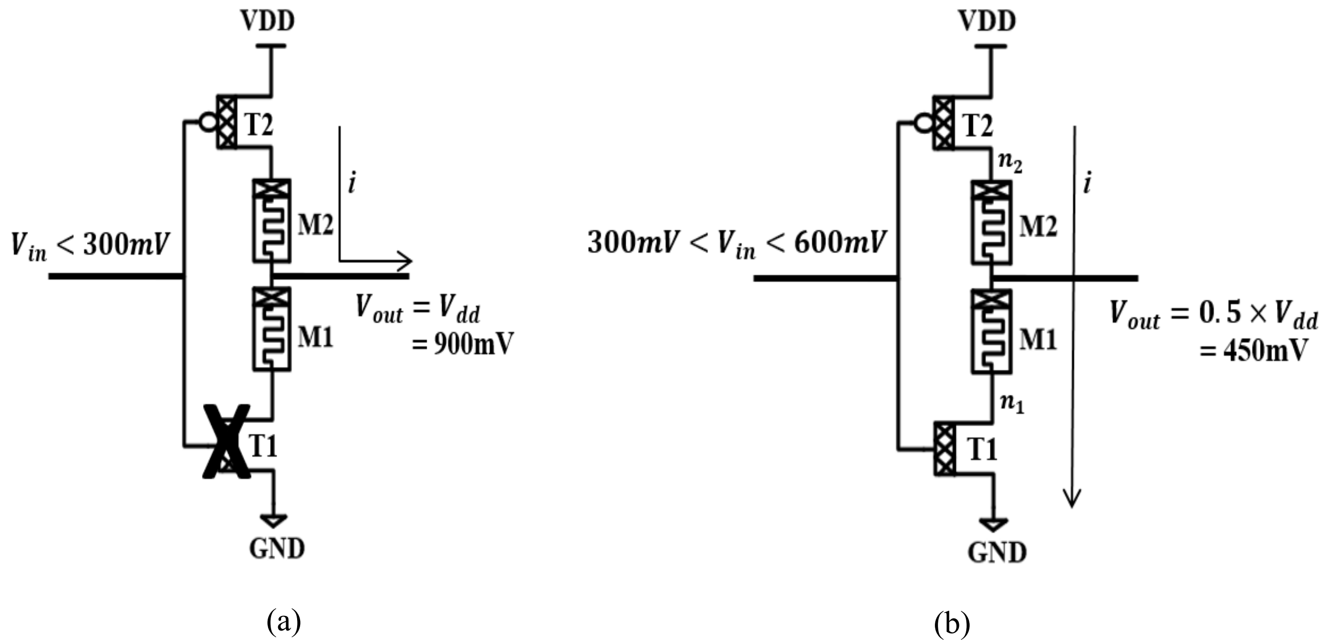
The chirality of the CNTFETs are (19, 0). According to equation (3) and (4), the diameter of T1 and T2 is 1.487nm, and the V_{TH} of T1 and T2 are 289mV and -289mV, respectively. The supply voltage of the proposed design is 900mV. Therefore, the voltage value below 300mV corresponds to the logic "0", the voltage value between 300mV and 600mV corresponds to the logic "1", and finally, the voltage value above 600mV corresponds to the logic "2". Initially, when the input voltage (V_{in}) is lower than 300mV, T2 is ON, and T1 is OFF as shown in Figure 59(a). Therefore, the output voltage (V_{out}) is 900mV, corresponding to logic 2. Once V_{in} is greater than 300Mv, both T1 and T2 are ON. The direction of the current flow is the same for both M1 and M2. Therefore, both memristors act as equal resistors and produce voltage drop from n_2 to V_{out} and from V_{out} to n_1 as shown in Figure 59(b). As a consequence, V_{out} = 450mV, which is equal to half of V_{DD}. When V_{in} increase above 600mV, T1 is ON, and T2 is OFF, as shown in

Figure 59(c). Now V_{out} is pulled down to zero. The transient response of the proposed STI design as shown in Figure 59(d). Table 15 shows the different logic state of the STI.

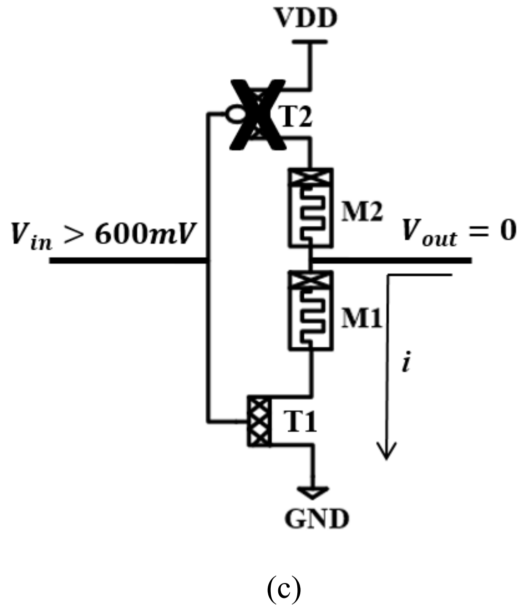


(a) (b)

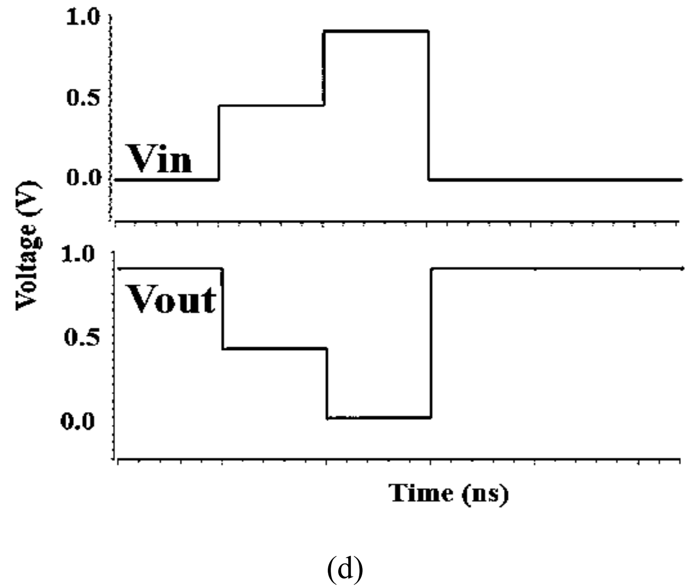
Figure 58: (a) Schematic of proposed CNTFET and Memristor based STI and (b) VTC of proposed CNTFET and Memristor based STI.



(a) (b)



(c)



(d)

Figure 59: (a) Working of proposed STI when $V_{in} < 300$mV, (b) Working of proposed STI when 300mV $< V_{in} <$ 600mV, (c)Working of proposed STI when $V_{in} >$ 600mV and (d) transient analysis of proposed STI design.

Table 15: Logic States of Proposed STI

Voltage level (mV)	Logic Value
0	0
½ V_{DD} = 450	1
V_{DD} = 900	2

7.6 Performance Analysis of the proposed STI

The power delay product (PDP) is used as the figure of merit to investigate the performance of the proposed STI. The analysis is carried on a pair of STIs connected as a buffer. The average power is calculated by taking the average of the power consumption of the two STIs, and the

average delay is calculated as the mean of the delays for 0→1, 1→2, 2→1 and 1→0 transitions. The proposed STI achieves 16.37 times and 65.48 times improvement of the PDP compared to [72] and [75], respectively, as shown in Figure 60.

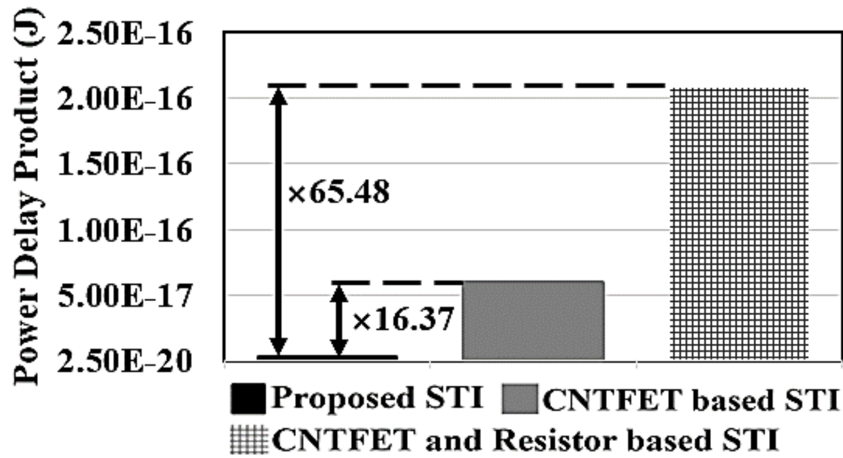


Figure 60: Power delay product comparison of proposed and existing STI designs [72] and [75].

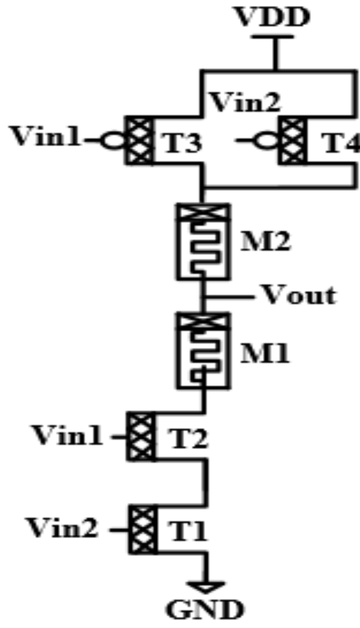
7.7 Robustness of the Proposed STI

The stability of the logic gate is determined from the cross-coupled inverter pair circuit by employing butterfly curve method. In ternary logic, four noise margins (NMH, NMMH, NMML, and NML) are defined at four voltage points (VIH, VIMH, VIML, and VIL). The SNM of the STI is the smallest one among the four noise margins (NMH, NMMH, NMML, and NML) [83]. Table 16 presents the benchmarking of the proposed and the existing STI designs regarding the SNM.

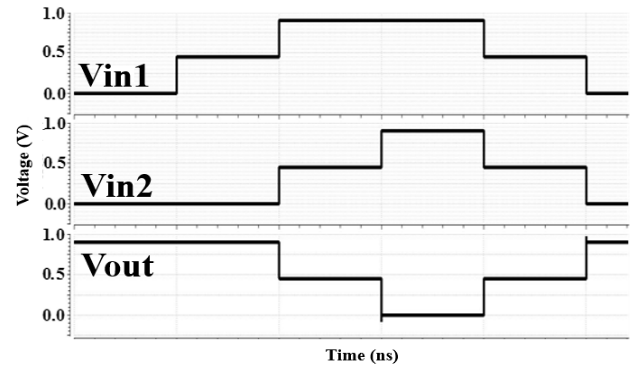
Table 16: Benchmarking between proposed and existing STI

STI Designs		Proposed	CNTFET and Resistor based [72]	CNTFET based [75]
Supply Voltage		900mV		
CNTFET Technology		32nm		
Noise Margin (mV)	NM_H	159	165	238
	NM_{MH}	140	5.2	6.4
	NM_{ML}	141	5.8	7
	NM_L	154	165	240
SNM (mV)		140	5.2	6.4

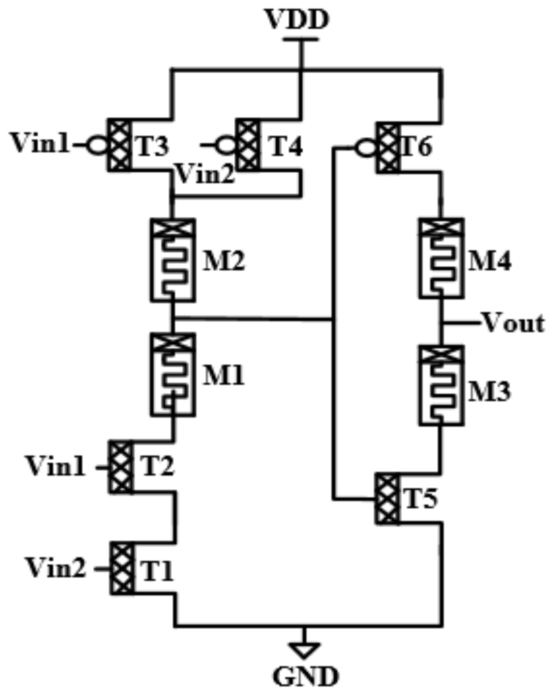
Similarly, different ternary logic gates T-NAND, T-NOR, TAND and T-OR are designed, as shown in Figure 61. Table 17 outlines the truth table of T-NAND and T-NOR gates. Table 18 provides a comprehensive performance summary of different proposed ternary logic gates. The power delay product (PDP) is determined for different ternary logic gates, as shown in Figure 62.



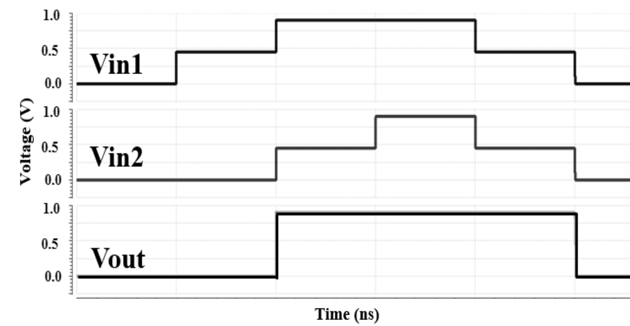
(a)



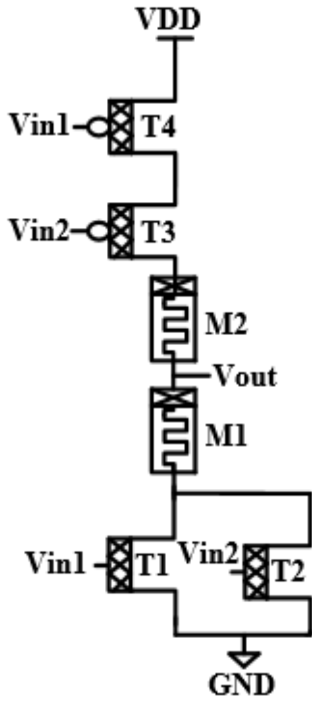
(b)



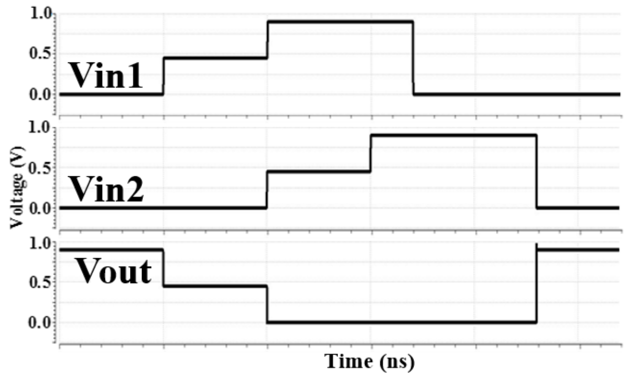
(c)



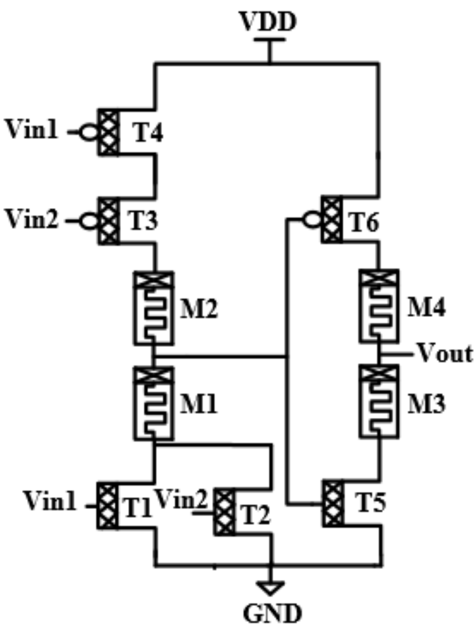
(d)



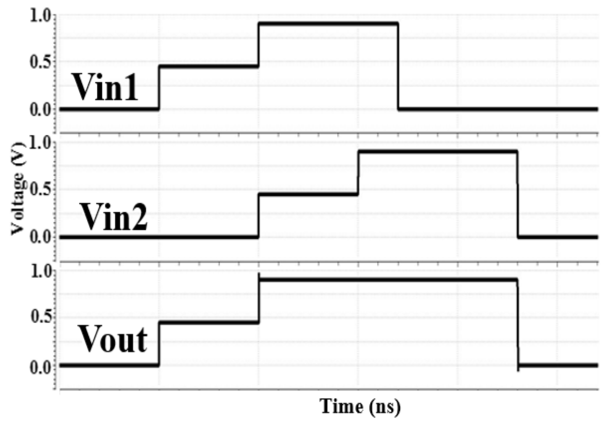
(e)



(f)



(g)



(h)

Figure 61: Schematic and transient analysis of (a) T-NAND, (b) T-AND, (c) T-NOR and (d) T-OR

Table 17: Logic states of proposed ternary logic.

Input (Vin1)	Input (Vin2)	T-NAND (Vout)	T-NOR (Vout)
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

Table 18: Performance summary of proposed ternary logic gates.

Logic Gate	Chirality	Power (nW)	Delay (ns)
T-Inverter	(19,0) for all logic gates CNTFETS	0.81	0.072
T-NAND		357.4	0.005
T-NOR		235.5	0.004
T-AND		148.3	0.011
T-OR		336.3	0.009

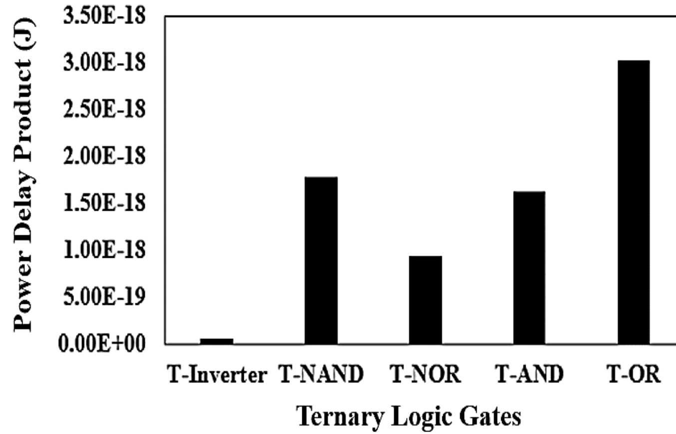


Figure 62: Power Delay Production of proposed ternary logic gates.

7.8 Proposed Unbalanced Ternary SRAM

The proposed ternary SRAM (T-SRAM) design utilizes the two cross-coupled TI and a pair of access transistors to read and write the data as shown in Figure 63. The proposed T-SRAM design utilizes a pair of access transistors to avoid the threshold voltage drop and ensure that correct data is written into the memory cell or read from the memory cell. The access gates are controlled by wordlines (WL and WLB). The data (Logic-0, Logic-1 or Logic-2) is stored at storage nodes Q and Q_B.

7.8.1 Write operation of proposed T-SRAM

Bitlines (BL and BL_B) are used to write data at storage nodes Q and Q_B of T-SRAM cell, via access transistors (T1 and T2). Once the wordline is triggered, data is written in T-SRAM cell depending upon the value at bitlines. When BL=0mV (logic-0) and BL_B=900mV (logic-2), transistors T4 and T5 are in ON state and the transistors T3 and T6 are in OFF state. Therefore, the voltage at storage node Q is 0mV (logic-0) and at storage node Q_B is 900mV

(logic-2). Similarly, voltage at Q (Q_B) will be 900mV (0mV) when BL=900mV (BL_B=0mV). For both BL and BL_B at 450mV (logic-1) transistors (T3, T4, T5 and T6) will be in the linear region. The direction of the current flow is now the same for all memristors (M1, M2, M3 and M4). These memristors act as equal resistors and produce a voltage drop (similar to inverter operation in section-I). Therefore, the voltage at Q and Q_B is 0.45mV (logic-1). Figure 64 shows the write operation of the proposed T-SRAM bitcell.

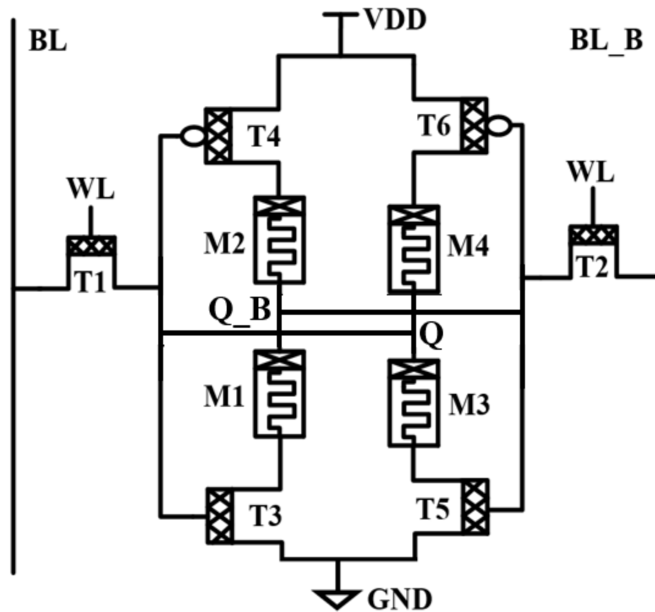


Figure 63: Proposed Ternary Memory Cell.

7.8.2 Read operation of proposed T-SRAM

The read operation of the T-Memory cell is similar to the conventional binary 6T SRAM cell. During the read cycle, the bitlines are precharged to Logic-2. Once the bitlines are precharged, the wordlines are asserted to read from the memory cell. The stored value at the storage nodes (Q and Q_B) is passed to the bitlines (BL and BL_B) via access transmission

gates. Depending upon the value stored at the storage node (Q and Q_B) the bitlines (BL and BL_B) remains at V_{DD} or start discharging. Figure 65 shows the read operation of the proposed T-SRAM bitcell.

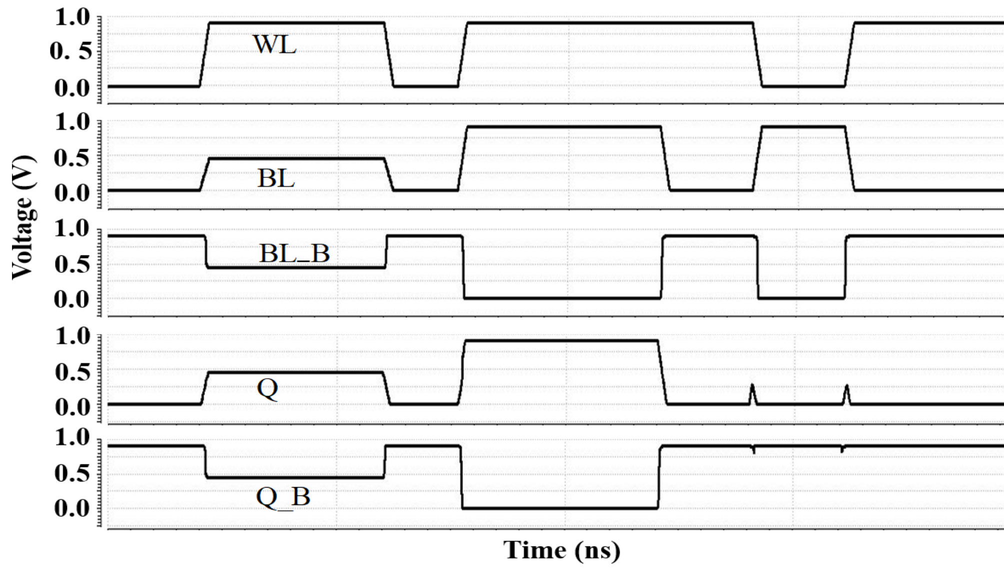


Figure 64: Write operation of the proposed T-SRAM bitcell.

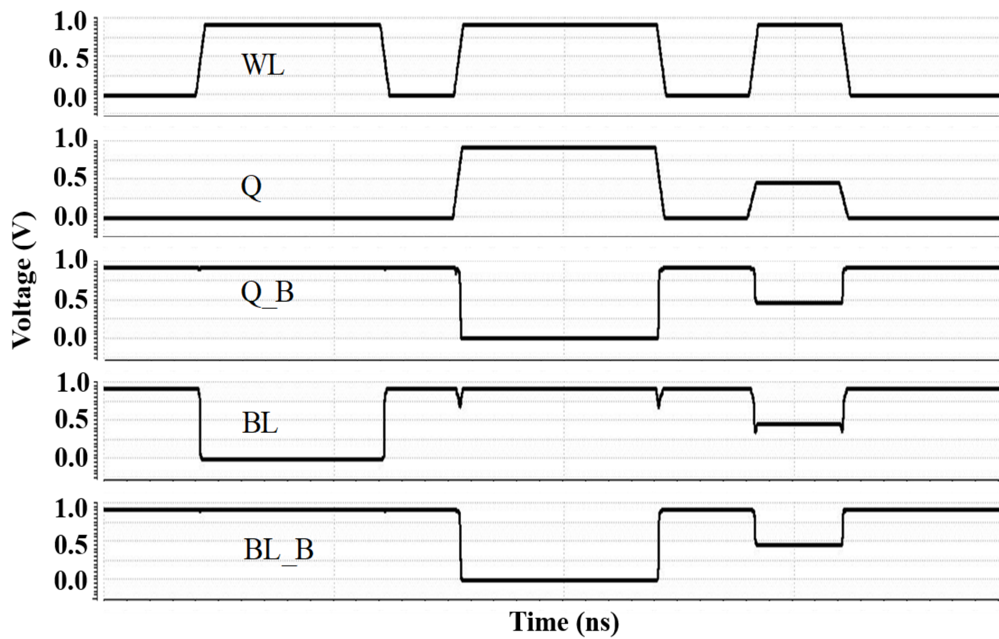


Figure 65: Read operation of proposed T-SRAM bitcell.

7.9 Performance and stability of T-SRAM

Table 19 summarizes the read and write delay of the proposed T-SRAM bitcell. The ternary logic has a different logic level change. 0➔1, 0➔2, 2➔0, 2➔1, 1➔2 and 1➔0. The write delay is the time required to pass the data via BL (BL_B) to the storage node Q (Q_B), when the WL line is high. It is calculated from 50% of the rising edge of WL to 50% of rising or falling edge of the storage node. Similarly, the read delay is the time required to read the data from the storage node to the output node, when the WL is high. It is measured from 50% of the WL rising edge to 50% of the rising or falling edge of the storage node.

The stability of the T-SRAM bitcell is determined by using the butterfly curve method. The Static Noise Margin (SNM) is determined graphically by plotting the VTCs of the inverter pair on top of each other. The square with the largest length nested between the butterfly curve represents the SNM. In ternary logic, four noise margins (NM_H, NM_{MH}, NM_{ML} and NM_L) are defined as shown in Figure 66. The SNM of the T-SRAM is the smallest one among the four noise margins [88]. Table 20 presents the benchmarking of the proposed and the existing T-SRAM design in terms of the SNM. It is observed that the proposed T-SRAM design offers higher stability compared to the existing T-SRAM design. The SNM of the proposed T-SRAM is 95.43% better compared to the design proposed in [87].

Table 19: Performance summary of proposed ternary SRAM bitcells.

Delay (ps)		Proposed	[83]
Write	0 → 1	81.5	113.1
	0 → 2	96.2	20.64
	1 → 0	250	7.18
	1 → 2	141	5.82
	2 → 0	124	10.90
	2 → 1	112	95.91
Read	0	3.4	127.6
	1	126	39
	2	142	135.3

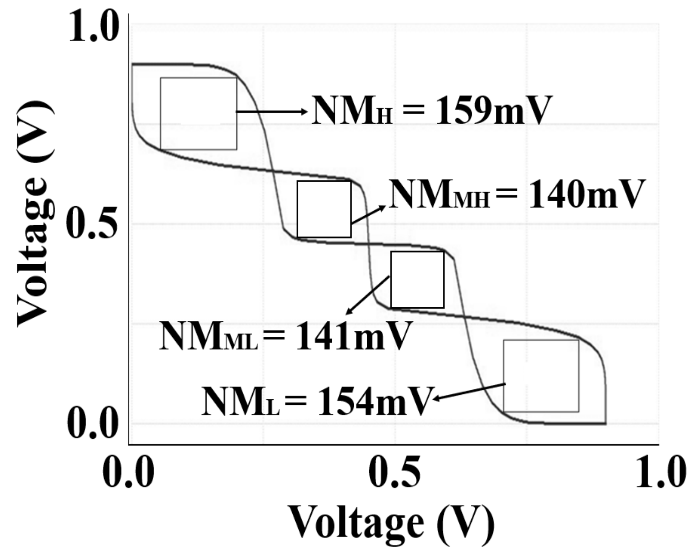


Figure 66: Static noise margin (SNM) of proposed T-SRAM.

Table 20: Benchmarking between proposed and existing standard ternary inverter.

STI designs		Proposed	[87]
Supply voltage (mV)		900	
CNTFET technology (nm)		32	
Noise Margin (mV)	NM_H	159	238
	NM_{MH}	140	6.4
	NM_{ML}	141	7
	NM_L	154	240
SNM (mV)		140	6.4

7.10 Conclusion

In this chapter, we proposed new ternary logic gates and SRAM bitcell designs based on CNTFET and memristor technologies. Theoretically, efficiency and the performance of MVL circuits is better compared to the boolean logic circuits because MVL design uses more than one state, utilizes few gates and reduced interconnect lines. Moreover, it is more convenient to use ternary logic compared to the other MVL logics because of the design simplicity. But at the same time, it is important to remember that these proposed ternary designs are purely conceptual, and the analysis is based on the available simulation models of CNTFET and the memristor. Fabrication related data cannot be obtained because these emerging technologies are still in the exploratory phase. However, these post-CMOS technologies exhibit outstanding characteristics and have the ability to replace the standard conventional CMOS technology that suffers from short channel effects and many other scaling related challenges. Previous studies have proved

that conventional CMOS devices would not be suitable for the multi-valued-logic (MVL). CNTFET is a promising alternative to implement MVL circuit. Existing ternary logic designs [82], use large resistors with CNTFETs would impose excessive area overheads and parasitic effects. Also, the RC-delay and the power consumption would be very high with large resistors in the logic gates. Besides, ternary logic designs in [72] and [75] require too many CNTFETs for each logic gate, which would make the operation very complicated. The proposed ternary logic gate designs have a simple structure with few device elements and achieve better PDP compared to other existing MVL designs. For instance, the proposed TI design offers 16.37 times and 65.48 times better performance in terms of PDP compared to the designs proposed in [72] and [75], respectively. Based on the proposed TI, we designed T-SRAM bitcell which also offers higher stability compared to the existing designs. The SNM of the proposed T-SRAM is 95.43% better compared to [83]. Multiple studies related to the compatibility and fabrication of these emerging devices are under progress. Researchers have continued to explore circuits and systems based on CNTFET and memristor [89], [90], because the performance of CNTFET-memristor based designs are expected to be better than the existing matured technologies. Although there is ambiguity regarding these post-CMOS devices, due to the upsurge of interest and ground-breaking research to adopt these exotic technologies in future applications, we are very optimistic that the community will find practical ways to implement these designs.

CHAPTER 8

CONCLUSION

8.1 Summary of research work

A new hybrid 8T SRAM design is proposed. It offers higher energy efficiency, reliability, robustness, and performance compared to the conventional 6T and other existing 7T, 8T, 9T and 10T designs. It offers the advantages of a 10T SRAM without the additional area, delay and power overheads of the 10T SRAM. The proposed hybrid 8T SRAM can overcome many other limitations of the existing SRAM designs. One of the critical features of the new design is the elimination of the bitline precharging requirement during the read operation. In the conventional SRAM, precharging of the bitlines imposes power overhead and additional circuit complexity. All the simulations, layouts and analyses in this paper are performed using 45nm technology. A comparative analysis is performed between the proposed and the existing SRAM designs in terms of area, total power consumption during the read and write operations, and stability and reliability. The individual cell area of the proposed hybrid 8T SRAM is 1.16 times more than that of the conventional 6T SRAM when implemented in 45nm. However, the area of the proposed cell is less than other existing SRAM designs. The implemented 16Kb SRAM array using the proposed 8T SRAM cell features a fast access time of 598.4ps (1.9ns) and lower energy consumption of 3.51fJ/‘0’bit (9.76fJ/‘1’bit). Monte Carlo simulations are performed on

the proposed hybrid SRAM design to evaluate the impact of the process variations, and it is observed that the proposed SRAM is more robust towards the process and parametric variations.

8.2 Future research direction

For the proposed 8T SRAM project, issues like bit-interleaving and half-select cells need to be investigated to validate the commercial feasibility of the proposed hybrid 8T SRAM design. Future work can be done on these unresolved issues.

In the case of multi-valued logic projects, numerous studies related to the compatibility, scaling, and fabrication of these emerging devices are in progress. Researchers have continued to explore circuits and systems based on CNTFET and memristor because the performance of CNTFET-memristor based designs is expected to be better than the existing matured technologies. Although there are many unknowns and uncertainties regarding these post-CMOS devices, due to the surge of interest and ground-breaking research to adopt these exotic technologies in future applications, I am very optimistic that the community will find practical ways to implement these designs.

Besides, in this thesis, 6T SRAM bitcell design based on emerging technologies was presented. In the future, these bitcell designs [91]-[95] can be converted to a 1MB bitcell array. These designs can also be utilized for emerging biomedical [96], [97] and high-speed low-power applications.

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