Investigation of Multiple-valued Logic Technologies for Beyond-binary Era

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Computing technologies are currently based on the binary logic/number system, which is dependent on the simple on and off switching mechanism of the prevailing transistors. With the exponential increase of data processing and storage needs, there is a strong push to move to a higher radix logic/number system that can eradicate or lessen many limitations of the binary system. Anticipated saturation of Moore's law and the necessity to increase information density and processing speed in the future micro and nanoelectronic circuits and systems provide a strong background and motivation for the beyond-binary logic system. In this review article, different technologies for Multiple-valued-Logic (MVL) devices and the associated prospects and constraints are discussed. The feasibility of the MVL system in real-world applications rests on resolving two major challenges: (i) development of an efficient mathematical approach to implement the MVL logic using available technologies, and (ii) availability of effective synthesis techniques. This review of different technologies for the MVL system is intended to perform a comprehensive investigation of various MVL technologies and a comparative analysis of the feasible approaches to implement MVL devices, especially ternary logic.

CCS Concepts: • **General and reference → Surveys and overviews**; • **Hardware → Circuit optimization**; **Transistor-level synthesis**;

Additional Key Words and Phrases: Multiple-valued logic (MVL), ternary logic, resonant tunneling diode (RTD), single electron transistor (SET), fin field effect transistor (FinFET), fully depleted silicon on insulator (FDSOI), quantum dot gate field effect transistor (QDGFET), memristor, carbon nano tube field effect transistor (CNTFET), graphene nano ribbon field effect transistor (GNRFET), memcapacitor, metal-insulator transition (MIT)

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1 INTRODUCTION

With the exponential increase of the quantity and density of information, the demands for extremely high data processing speed and storage requirements are rapidly moving beyond what binary logic-based digital systems can offer. Binary logic-based computing machines are expected to face an enormous challenge in the near future due to the severe thermal and reliability problems. To mitigate these inevitable limitations of the binary systems, researchers have already started exploring different multiple-valued logic and memory devices. Before the semiconductor device technology came into existence, the electrical switching system relied on electromagnetic relays and its derivatives. Though the simplest form of relays was binary, there were also some multiposition devices, which were used in the telephone system, railroad traffic control, and some industrial applications. The design of such systems was not firmly based upon any structured mathematical or synthesis technique. With the introduction of solid-state devices, the use of switching devices with two distinct states became prevalent and versatile. There were some initial efforts to develop multiple-state devices (e.g., Rutz commutating transistor), multiple-frequency oscillator concept of Edson, multiple-phase devices (e.g., the parametron), and multi-aperture square-loop ferrite devices, and so on. A ternary computer named SETUN was built in 1958 [1]. During the 1960s, numerous other projects were undertaken to manufacture ternary logic gates, arithmetic circuits, and memory cells. In 1973, a complete ternary machine named TERNAC and also a software emulator was designed [2]. With the arrival of the Bipolar Junction Transistor and later the Metal Oxide Semiconductor (MOS) transistors, these early developments in the field of multi-state devices faded away from academic research and industrial development arenas [3]. However, as the binary logic system is approaching the end-of-the-roadmap, there has been a renewed interest in exploring multiple-state devices for logic and memory applications. Compared to a binary logic system, the multiple-valued logic holds many advantages. It allows a single digit to contain more data than binary. Consequently, on- and off-chip wiring density would decrease, leading to smaller and simpler chips with lower pin-count. Table 1 shows the density of information that can be held by binary (2-valued), ternary (3-valued), and quaternary (4-valued) logic systems for different numbers of bit combinations.

For our general arithmetic and algebraic calculations, we use decimal or base "10" number system, and for all digital applications, we now use binary or base "2" system. Theoretically, the most appropriate base to work with is neither base "2" nor "10" [4]. For any numerical system, the number of digits required to express a specific value is inversely proportional to the radix number. If N is the range of number, R is the radix, and d is the required number of digits, which is rounded to the subsequent integer value, then the relationship can be expressed by Equation (1):

$$\begin{aligned} N &= R^d \\ \Rightarrow logN &= d \times logR \\ \Rightarrow d &= \frac{logN}{logR}. \end{aligned} \tag{1}$$

The cost or the complexity of the system hardware C can be assumed to be proportional to the digit capacity ($R \times d$). Then from Equation (1), it can be derived that

$$\begin{aligned} C = k(R \times d) &= k\left[R \times \frac{logN}{logR}\right] \\ \Rightarrow C &= k\left[R \times \frac{logN}{logR}\right]. \end{aligned} \tag{2}$$

Table 1. Table Showing the Density of Information by 2-, 3-, and 4-Valued Logic

Highest Possible data that can be contained by:	Binary (R=2)	Ternary (R=3)	Quaternary (R=4)
1 bit	$2^1 = 2$	$3^1 = 3$	$4^1 = 4$
2 bit	$2^2 = 4$	$3^2 = 9$	$4^2 = 16$
3 bit	$2^3 = 8$	$3^3 = 27$	$4^3 = 64$
4 bit	$2^4 = 16$	$3^4 = 81$	$4^4 = 256$

Here k is the constant of proportionality. If Equation (2) is differentiated with respect to R, then it can be shown that for the least value of cost C, radix number R is equal to $e = 2.72$. Considering the nearest integer to the value of e, it can be said that that $R = 3$ or a ternary system would be more cost-effective than $R = 2$ or a binary system. If under a different assumption it is considered that C is independent of the system radix R, then Equation (2) can be re-written as Equation (3):

$$C = k \times d = k \left[\frac{logN}{logR} \right]. \tag{3}$$

From Equation (3), it is evident that the circuit cost or complexity C steadily decreases with the increase of radix R. Also, in this case, a ternary system is more cost-effective than a binary system [3]. At present, the MVL arithmetic circuits are not used in the industry directly. But the research in this field creates a path for an unforeseen opportunity. As most of the devices in the real-world are in binary nature, it might take some time to be accustomed to the MVL system, but the concept of MVL is already introduced in several fields. In the sector of network routing [5] for IPv4 and IPv6, Ternary Content-addressable Memories (TCAMs) have been used for decades [6]. Generally, the TCAMs are designed using conventional SRAM or DRAM with additional circuitry. Lately, large flash memories having multiple bits per cell have been realized [7]. The notion of communicating data using symbols that carry more than one bit of information has been used for a long time in wireless and in some wireline communication systems, which use large complex-valued signal constellations like Quadrature Amplitude Modulation and Quadrature Phase Shift Keying. Currently, this technique is being used to increase the speed of chip-to-chip and optical communications by using PAM (Pulse Amplitude Modulation) [7]. In the Ethernet protocol, M-ary PAM is already in use [8]. Another successful commercialization of MVL is the StrataFlash from Intel [9, 10]. A fair amount of work on Multiple-valued Logic (MVL) has been done by different researchers, because MVL technologies hold high potentials to significantly enhance the capabilities of the binary logic-based circuits and systems. The scopes for MVL devices are profound and can be categorized into two primary approaches. The first approach uses multiple-valued logic as the background platform to solve binary problems more efficiently. The second approach is to design entirely new types of circuits and systems that would directly process and provide output signals with more than two unique values. Researchers are exploring both prevailing and emerging device technologies for these two approaches. However, MVL technologies are expected to face some critical challenges. For example, with the continuous decrease of technology nodes that are operated at a lower voltage (around 1.2 V as VDD and 0 V as ground), it would be quite challenging to maintain three or more distinct voltage levels with sufficient intermediate voltage gaps to maintain multiple logic states under severe noise constraints. Considering the prevalence of MOSFET technology, it would be prudent to utilize it to implement higher radix systems while exploring completely new technologies for MVL systems. However, the interconnect-centric power,

Table 2. Logic Levels for an Unbalanced Ternary Logic System

Logic level	Logic symbol
0	0
0.5*VDD	1
VDD	2

Table 3. Logic Levels for a Balanced Ternary Logic System

Logic level	Logic symbol
− VDD	−1
0	0
VDD	1

Table 4. Definition of Different Kinds of Ternary Inverter

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

performance, and reliability limitations of MOSFET technology make it less appealing for MVL devices. The goals of this article are to explore different aspects of MVL design and study the various technologies that are being used for the implementation of MVL circuits. To achieve these goals in a meaningful way, a certain number of topics were excluded or very briefly discussed that are of interest but not fundamental to our purpose. Here, the scope of the MVL system for the memory circuit is not described extensively. Few other pieces of literature are present where the MVL memory is explained and reviewed [7, 11]. The use of MVL as a platform to solve binary logic problems are also excluded. Also, different MVL synthesis techniques are discussed very briefly, as these are purely theoretical. In addition to the applications mentioned above, MVL devices also have a great promise for quantum computation. Quantum computing uses quantum mechanical properties such as interference, superposition, and entanglement to perform computation, which is coarsely analogous to a classical computer [12]. The use of the MVL system in the field of quantum computing has been reviewed and discussed in References [13–15]. The rest of the article is organized as follows. Section 2 presents the basic information and definition of MVL. Section 3 highlights different technologies that have been used to implement an MVL device. Section 4 provides a comparative analysis of different technologies. Finally, Section 5 concludes the article with a brief overview of future directions.

2 FUNDAMENTALS OF MULTIPLE-VALUED-LOGIC

The multiple-valued logic system is composed of "R" distinct logic levels, where $R > 2$. The base 2 or binary numeric system has two distinct values known as "true and false" or "1 and 0" or "high and low." The MVL system may consist of a set of any number of logic levels that are represented by some signal variables, such as, current, voltage, or charge. These sets of values can be illustrated using any of the two conventions: unbalanced and balanced. An unbalanced system is the extension of the binary number system in a single direction, for instance, 0, 1, 2, 3. . . (R-2), (R-1); and the balanced system needs an odd radix $R = 2K+1$, with the values (-K), (1-K) . . . −1, 0, 1. . ., (K-1), K [16]. According to the definition above, a ternary logic system would have three values to represent false, true, and undefined states [17]. Tables 2 and 3 show the representation of basic unbalanced (0, 1, 2) and balanced (−1, 0, 1) ternary logic systems, respectively. Ternary inverters can be implemented in three different ways: standard, positive, and negative. The logic symbol and the truth table for different types of ternary inverters are given in Table 4. Table 5 shows basic ternary logic functions, such as OR, AND, XOR, and Half Adder. A ternary function $f(X)$ containing n variables $\{X_1, X_2 \ldots, X_n\}$ can be described as a logic function mapping from $\{0, 1, 2\}^n$ to {0, 1, 2}, where $X = \{X_1, X_2 \ldots, X_n\}$. The elementary algebraic operations of ternary logic can be described using Equations (4), where $X_i, X_j = \{0, 1, 2\}$ [18]:

$$X_i + X_j = max(X_i, X_j), \tag{4a}$$

$$X_i \cdot X_j = min(X_i, X_j), \tag{4b}$$

$$\bar{X_l} = 2 - X_i. \tag{4c}$$

Here, + and • represent the OR and AND operations, respectively, and – represents the arithmetic subtraction.

Table 5. Basic Logic Functions of a Ternary System

Input		OR	AND	XOR	Half Adder	
X1	X2				SUM	CARRY
0	0	0	0	0	0	0
0	1	1	0	1	1	0
0	2	2	0	2	2	0
1	0	1	0	1	1	0
1	1	1	1	1	2	0
1	2	2	1	1	0	1
2	0	2	0	2	2	0
2	1	2	1	1	0	1
2	2	2	2	0	1	1

Table 6. K-map for Sum and Carry

Sum			
X1\X2	0	1	2
0		1	2
1		2	
2	2		1
Carry			
X1\X2	0	1	2
0			
1			1
2		1	1

For a multiple-valued logic system, the function minimization techniques become more complex with the increase of radix. In the case of ternary, the minimization is a little bit complicated than that of binary but the use of Karnaugh map (K-map) for binary can be extended to ternary with little modification. In Reference [19], a method to minimize a ternary function with the help of a K-map is presented. From Table 5, the K-map for the Sum and Carry of a ternary half adder can be derived as in Table 6 and Equations (5).

The equation for representing the sum and carry from the k-map is written as

$$Sum = 2 \times (X_1^2 X_2^0 + X_1^1 X_2^1 + X_1^0 X_2^2) + 1 \times (X_1^1 X_2^0 + X_1^0 X_2^1 + X_1^2 X_2^2), \tag{5a}$$

$$Carry = 0 + 1 \times (X_1^2 X_2^1 + X_1^1 X_2^2 + X_1^2 X_2^2). \tag{5b}$$

Besides K-map, there are other synthesis techniques for MVL like Galois Field Polynomials, Arithmetic Polynomials, and Linear Cellular Arrays [20]. In Galois Field Polynomials, an arbitrary logic function with m-values and n-variables is characterized by m^n different polynomial expressions or polarities, and an optimum representation is obtained. The coefficients of the polynomials can be attained with the help of direct and inverse Reed-Muller Transforms over Galois Field [19, 20, 21]. Arithmetic Polynomial is similar to Galois Field Polynomials, where different polarities can also be obtained using direct and inverse arithmetic transform matrices. In Linear Cellular Arrays, the m-valued and n-variable logic function f is partitioned into a set of subvectors, then the multiple-valued variable is encoded into new binary variables called pseudo-variables and the function f is represented by an arithmetic expression based on those pseudo-variables [19, 20]. In Reference [22], a mapping method is proposed in which the synthesis problem is formulated as a mapping from an input matrix to an output matrix. An approach for computing and analyzing MVL has been proposed in Reference [20], which is applicable and adaptable to any multiple-valued function. The process can be divided into three different steps: domain selection, linear regression, and pattern matching for deriving selection criteria. In the domain selection stage, the domain for the input, and output and parametric constants are fixed. After the selection of domain, linear regression is carried out on the input combinations through which a linear equation is derived that fits the majority of function outputs. On the residual unmatched outputs, linear regression is done again so that a set of linear expressions is obtained. Once all the outputs of the functions are matched with a particular linear expression, this step continues. For the third stage, based on the sets of linear expressions obtained in Stage 2, individual selection conditions for individual expressions in the sets are derived. For a particular input combination, the hardware must be able to select the correct linear expression from the sets, through the selection conditions derived,

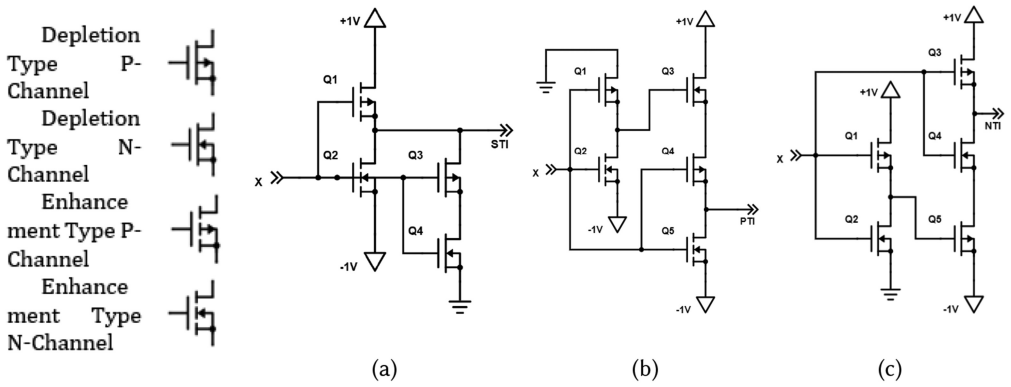


Fig. 1. Schematic diagram of (a) STI, (b) PTI, and (c) NTI [30].

to obtain the correct output. It proposes a visual pattern-matching scheme for the derivation of the selection conditions. Besides all these above-mentioned methods, various other synthesis techniques are available [23, 24]. Several MVL synthesis tools and techniques have been proposed and tried out for years, for example, Multiple-Valued Sequential Interactive Synthesis or MVSIS [25] and ABC [26]. Another low-level language tool named BLIV-MV is also available, which describes the MVL circuits in such a way that the logic synthesis tool can understand it [27].

3 DIFFERENT TECHNOLOGIES FOR MVL

The initial efforts to implement ternary and other MVL devices and circuits had been based on CMOS technology. Subsequently, many new initiatives have been started by the research community to explore MVL device and circuit implementations using Resonant Tunneling Diode (RTD), Single Electron Transistor (SET), Fin Field Effect Transistor (FinFET), Fully Depleted Silicon on Insulator (FDSOI), Quantum Dot Gate Field Effect Transistor (QDGFET), Carbon Nano Tube Field Effect Transistor (CNTFET), Graphen Nano Ribbon Field Effect Transistor (GNRFET), Memristor, Metal Insulator Transition (MIT) material-based memcapacitance technologies. In this section, a brief overview of various technologies and techniques for ternary logic design is provided.

3.1 MOSFET-based Ternary Logic

3.1.1 Operating Principle. The main reason behind selecting MOSFET for ternary logic would be its simplicity and compatibility with the prevalent semiconductor process. Mouftah and Jordan (in 1974) and others (in later periods) demonstrated that binary CMOS circuits can be converted to ternary circuits with little effort and without requiring any new types of transistors [28, 29, 30, 31, 32]. The threshold voltages of MOSFET can be easily changed during the fabrication process, which can be used as a means to create multiple voltages or current levels required in the MVL device. Two different techniques have been explored in this regard. The first one is to use a combination of enhancement and depletion type of MOSFETs in the same circuit [30, 31, 33] and the second one is to use only enhancement type MOSFETs along with some resistors to implement a voltage divider to obtain multiple voltage levels [29, 32].

Figure 1 shows the circuit diagrams of the STI, NTI, and PTI, respectively, implemented using the first technique [30]. For the STI, the output shows a balanced standard ternary inverter, i.e., for the input logic level of 1, 0, and −1, the output will have a value of −1, 0, and 1, respectively. When the input is of high value (logic 1), $Q1$ will be off, whereas $Q2$ will be on; and $Q3$ will be off though $Q4$ will be on. This setup will keep the output node at a low value (−1 V). For the low

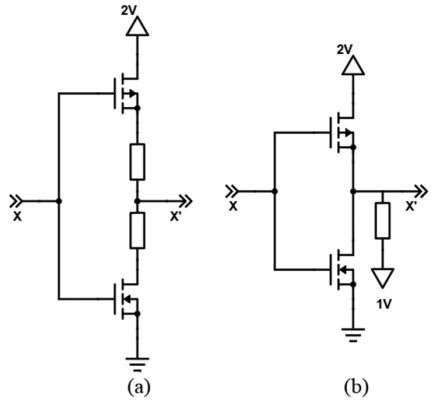


Fig. 2. Standard Ternary Inverter using (a) two resistors, (b) one resistor [29].

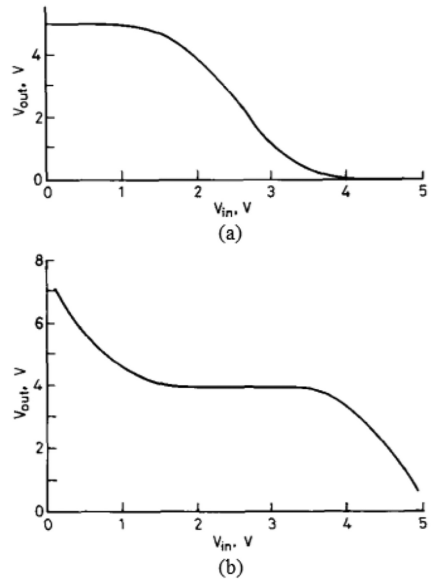


Fig. 3. (a) Transfer characteristics with two resistors, (b) transfer characteristics with one resistor [29].

input voltage (logic −1), $Q1$ and $Q3$ remain on, whereas $Q2$ and $Q4$ become off and the output becomes high. For an intermediate input value, $Q1$ and $Q2$ will remain off and $Q3$ and $Q4$ will be on, thus connecting the output to the ground (logic 0). The condition for the STI circuit to work is as shown in Equations (6), where ±V = value of the power supply, V_T = threshold voltage of the enhancement MOS transistors, and V_P = pinch-off voltage of the depletion devices:

$$V < V_T < 2, \tag{6a}$$

$$0 < V_P < V. \tag{6b}$$

Figure 2 shows the ternary circuits with only enhancement type MOSFETs and resistors. Here, resistors are inserted in between the transistors to get the required intermediate voltage level [29]. Figure 3 shows the DC transfer characteristics of the circuit of Figure 2. The same circuit can be constructed without using the resistors and controlling the threshold voltage [34]. All these

techniques and circuits can be extended to implement ternary NAND, NOR, ALU, adder, multiplier, and so on, complex circuits [30, 31, 34, 35].

3.1.2 Analysis. Among all the technologies, MOSFET is the oldest one to be explored for the MVL device, mainly because MOSFET-based MVL devices would be compatible with the current process. The prevailing binary CMOS circuits can be modified into ternary circuits with a new type of transistor. As threshold values of MOSFET transistors are easily changed during the fabrication, multiple voltage or current levels can be created. In a current-mode circuit, logic levels are usually defined by different currents, which are the integer multiples of the reference current. Currents are possibly being scaled, copied, and algebraically sign changed by the simple current mirror. Frequently used Linear-sum operation can be performed by wiring, which results in the reduced number of active devices in the circuit. Many prototype chips of the current-mode CMOS circuits have fabricated in the past showing better performance as compared to the corresponding binary-circuits [36–38]. It is to be believed that current-mode designs provide a much better noise margin than voltage-mode CMOS design. Some of the major benefits of binary CMOS logic are zero-static power dissipation for stable states and almost similar output impedance in either state. However, in the CMOS MVL circuits, these positive properties are not achievable. CMOS MVL circuits are generally categorized by rail-to-rail current flow in one or more than one static state and the higher output impedance in 1 state as compared to other states. There have been two solutions proposed to these problems recently. In the current-mode CMOS Multiple-Valued Logic circuits, dual-rail source-couple logic is introduced [37]. The use of complementary input pairs and the source-coupled logic allows high-speed circuits with lower power dissipation. Another alternative solution is, where the low-power and low-voltage, current-mode MVL circuits are to be designed by using the neuron-MOS transistor. Another major problem with CMOS MVL circuits is unlike Binary CMOS circuits, they are not self-restored. The level restoration circuit has to be utilized for every block of a certain number of stages for recovering signals. To solve this problem the new self-restored architecture is presented, which uses both voltage-mode binary circuit and current-mode MVL circuit to implement MVL functions and to restore the output signal simultaneously [37]. Binary gates are to be used within design architecture so that the binary-MVL or MVL-binary conversion circuits are not necessary to interface with binary circuits. The average size of resulting circuits is around 50% smaller than previously proposed MVL circuits, whereas average power dissipation and time delays are comparable. The voltage-controlled CMOS MVL circuits are expected to share the three key advantages of the CMOS binary circuits—0 static power dissipation in stable states, low output impedance in stable states, and the elimination of the passive elements (resistors). Any multiple-valued signal can be transmitted through a CMOS transmission gate. In contrast with the bipolar junction transistors, the ability to change the threshold voltage of the MOS transistors simplifies the task of responding to a multilevel input signal. The first CMOS ternary circuits were proposed in 1974. Since then, a lot of novel work has been done with a different perspective for the implementation of CMOS-based ternary circuit design.

With the continuing scaling of CMOS technology, different short dimension effects are introduced such as Carrier velocity saturation and mobility degradation, Drain-induced Barrier Lowering (DIBL), punch-through, hot carrier effects, etc [39]. If the channel length is small enough to compare with the source and drain depletion region, then the magnitude of these short channel effects increases manifold. Due to these effects, the leakage current flows more easily through the channel and the turning off the transistor becomes difficult. That is why newer designs involving newer methods and emerging technologies are sought by researchers to alleviate the challenges.

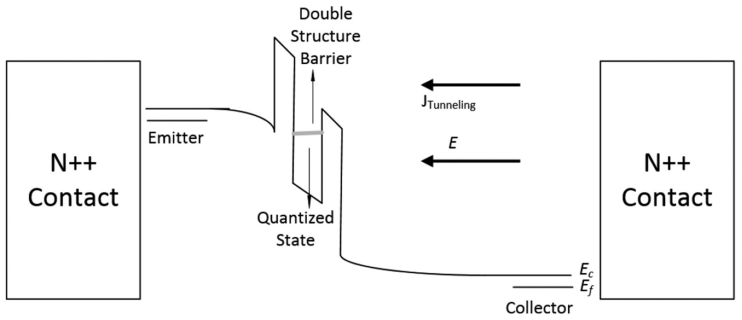


Fig. 4. Resonant Tunneling Diode operation. The shaded region in the double-barrier structure represents the quasi-bound state in the quantum well [40].

3.2 Resonant Tunneling Diode (RTD)-based Ternary Logic

3.2.1 Operating Principle. A Resonant tunneling diode is a device in which there are different semiconductor materials, which are present in alternate layers. Tunneling of electrons through different resonant states at certain energy levels causes the flow of current inside the device. The current-voltage (I-V) curve of an RTD demonstrates the negative differential resistance (NDR) feature. The decreasing part of the current curve with respect to the voltage gives rise to the negative differential resistance. This characteristic is very crucial to the circuit implementation as it can offer different voltage-controllable logic levels corresponding to the peak and valley currents. It consists of two heavily doped contacts made of a semiconducting material with a narrow energy gap (e.g., GaAs). These two contacts constitute the emitter and collector region. In between them, there are two barriers made of a comparatively larger bandgap material (e.g., AlGaAs). These two barriers encompass a quantum well, which is made of a relatively smaller bandgap material as shown in Figure 4 [40]. This type of structure is called a Double Barrier Quantum Well (DBQW) structure. Before applying any forward bias, the majority of the electrons and holes create an accumulation layer in the emitter and collector region, respectively. With the application of a forward voltage bias, an electric field is generated. This field forces the electrons to travel from the emitter region to the collector by the process of tunneling through the scattered states inside the quantum well. Due to the tunneling of electrons through these quasi-bound energy states, a current is created. As the number of electrons in the emitter with the same energy as the quasi-bound state increases, more electrons become able to tunnel through the quantum well. This results in an increase of current corresponding to the applied voltage. At a particular point, the energy level of the emitter electrons matches the energy level of the quasi-bound state. At that point, the current reaches its maximum value and resonant tunneling is said to happen. The occurrence of the resonant tunneling is observed at a certain resonant energy level, which depends on the corresponding doping level and the quantum well width. As the applied bias keeps on increasing, more electrons obtain too much energy than the energy of the quantum well and the amount of current starts decreasing. After reaching a specific applied voltage, the current rises again due to the substantial thermionic emission where the electrons can tunnel through the non-resonant energy levels as well. The current at the minimum valley is termed as leakage current. This phenomenon is demonstrated in Figure 5, which was drawn using a simulation tool in nanoHUB [41]. Different ternary and quaternary logic gates and memory devices have been proposed using different circuitry [42–44]. Among all of these, a very famous technique is the use of different combinations of up and down literals to produce multiple-valued outputs. These literals can be obtained by using circuits called monostable-to-bistable transition logic elements (MOBILE) [44, 45]. Two

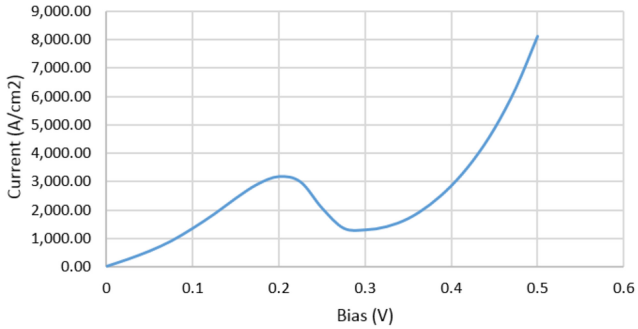


Fig. 5. RTD I-V characteristics.

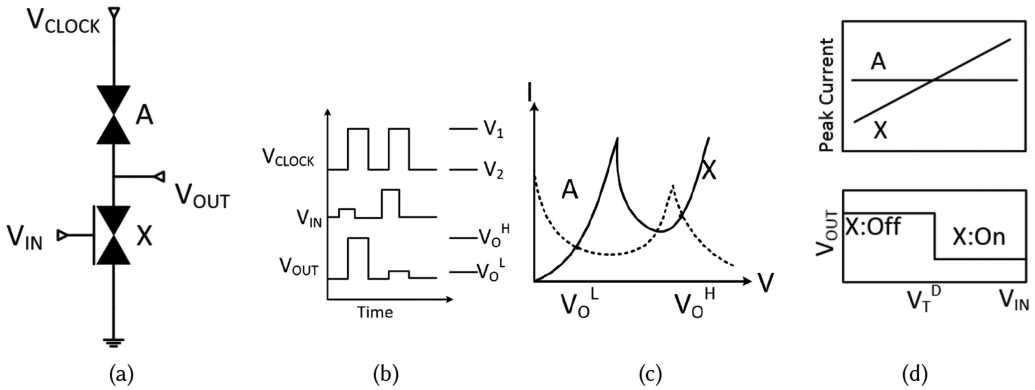


Fig. 6. (a) Circuit diagram of a down literal MOBILE, (b) Voltage vs. time graph of the operation, (c) current-voltage curve showing the bistable state, and (d) peak currents as a function of the input voltage [44].

RTD's connected in series combination creates a MOBILE, as shown in Figure 6. Here, X has a gate that can module the peak current by controlling the voltage. The output voltage curve for the respective input voltage can be seen in Figure 7(b). V_1 is considered for low voltage and V_2 is for high voltage. When $V_{CLOCK} = V_1$, both the RTD's are ON and the circuit is in the monostable state. When $V_{CLOCK} = V_2$, the circuit transfers to a bistable state. V_2 is selected in such a way that either A or X switches to OFF state from ON state when V_{CLOCK} is set to V_2. Depending on the ON and OFF states of A and X, high or low voltages can be seen in the output.

Here, the peak current of X increases with an increase in gate voltage V_{IN}. If $V_{IN} < V_{TD}$, then the peak current of X is less than the peak current of A, which changes the state of X from ON to OFF. Thus the output voltage is found to be V_{OH} (High). Again, when $V_{IN} > V_{TD}$, the peak current of A is smaller than that of X. For that, A switches to OFF state making the output V_{OL} (low). Similarly, an up literal can be obtained in a manner shown in Figure 7.

By combining these up and down literals any transfer characteristics with multiple thresholds and multiple outputs can be presented. In Reference [44], a ternary inverter was proposed using the combination of two down literals. In Figure 8(a), the circuit configuration of a ternary inverter using only down literals is given. Here, one down literal is composed of A and X with a threshold voltage of V_{T1}, and another pair of is consisted of B and Y, which has the threshold voltage V_{T2}. Peak current of A is smaller than the peak current of B. When $V_{CLOCK} = V_2$ (high), and $V_{IN} < V_{T1}$, the output is at the highest value (2). When $V_{T1} < V_{IN} < V_{T2}$, A, and Y are switched off, which

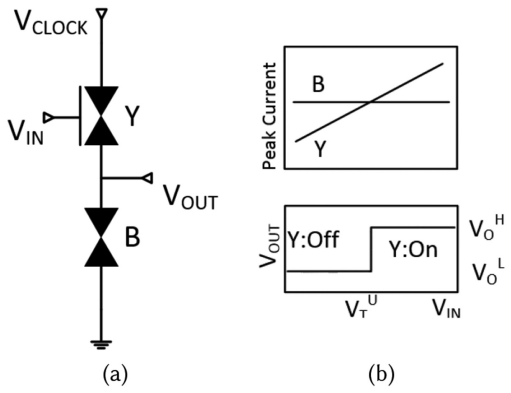


Fig. 7. (a) Circuit configuration of an up literal MOBILE. (b) Peak currents as a function of input voltage and transfer characteristics of up literal [44].

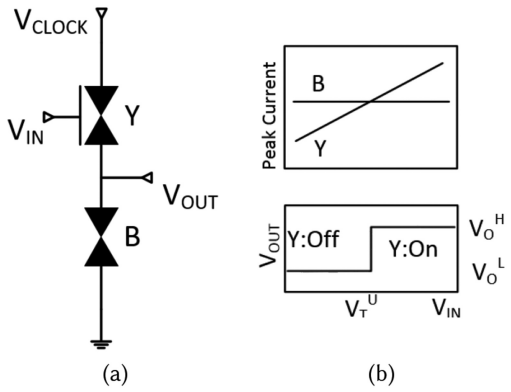


Fig. 8. (a) Circuit configuration of ternary inverter and (b) peak currents as a function of input voltage and transfer characteristics of a ternary inverter [44].

Table 7. Operating Conditions of a Ternary Inverter

V_{IN}	Switched OFF RTDs	V_{OUT}
$V_{IN} < V_{T1}$	X, Y	2
$V_{T1} < V_{IN} < V_{T2}$	A, Y	1
$V_{IN} > V_{T2}$	A, B	0

results in an intermediate output voltage (1). For $V_{IN} > V_{T2}$, A and B are switched off and the output becomes low (0). The operating conditions and different states are summarized in Table 7.

Along with basic gates, complex ternary gates using RTD have been proposed in different literature, for example, adder [42], Analog-to-Digital converter [43], pre-decoder [46], Programmable Logic Array or PLA [47], and so on. Few other ways combine the RTD with some other technologies like High Electron Mobility Transistors (HEMT), HBT (Heterojunction Bipolar Transistor), or MODFET (Modulation Doped field-Effect Transistor) to produce multiple-valued logic circuits [44, 48].

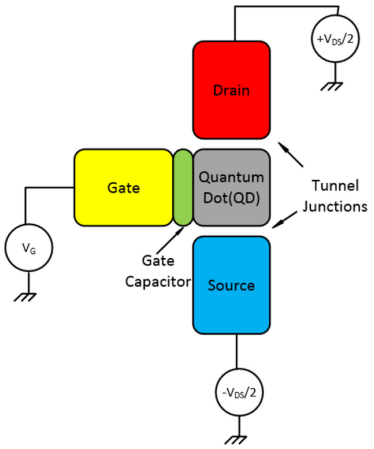


Fig. 9. Single electron transistor [50].

3.2.2 Analysis. Due to the lack of suitable dedicated devices, Multiple-valued logic circuits have not been extensively established commercially by the industry. Most of the multiple-valued circuits are of the threshold type, which uses conventional active devices such as bipolar transistors or field-effect transistors. Similar to analog circuits, these threshold type circuits also suffer from the same type of limitations in terms of noise margin and circuit complexity, which usually slows down the circuit operation. Whereas the RTD possesses some unique characteristics like folding I-V characteristics and high-speed operation owing to the tunneling effect. Due to these unique characteristics, RTD is considered to be a viable candidate for multiple-valued digital applications [42]. Though RTD holds a major possibility in the field of multi-valued logic, recent works on these are very rare. Most of the works regarding RTD-based MVL are date in the '90s. The need for completely new circuitry and technology might be the reason for it. There are few instances of literature work in the field of RTD fabrication though it is not mature enough to reach the full potential. Very precise thickness control is required to ensure the uniformity through the whole wafer. The output power of RTD is also limited, which requires an amplifier or other drivers [40].

3.3 Single Electron Transistor-based Ternary Logic

3.3.1 Operating Principle. SET is such a device, which is based on Coulomb Blockade Effect. A SET comprises two electrodes that work as the drain and the source. These electrodes are connected through tunnel junctions to a Quantum Dot (QD), which is also called the island. A third electrode, known as the gate, which is capacitively coupled to the island can be used to control the electrical properties of the island. The structural diagram of a SET can be seen from Figure 9 [49].

Figure 10 shows the working principle of a SET in terms of energy levels. In the absence of an applied external bias (Figure 10(a)), a blocking state prevails. Here, no available energy levels of the island are in the range of tunneling for the electrons in the source contact (in red). All the available or lower energy levels are occupied beforehand. Upon application of a positive voltage (Figure 10(b)), the energy levels are lowered for the island electrode. At that point, the emitter electron (green 1) can tunnel through a previously vacant energy state of the island (green 2) to the drain electrode (green 3). Here it inelastically scatters and moves to the drain electrode Fermi level. The separation between the energy levels of the island electrode is ΔE, which gives rise to a self-capacitance C of the island, which can be defined by Equation (7):

$$C = \frac{e^2}{\Delta E}. \tag{7}$$

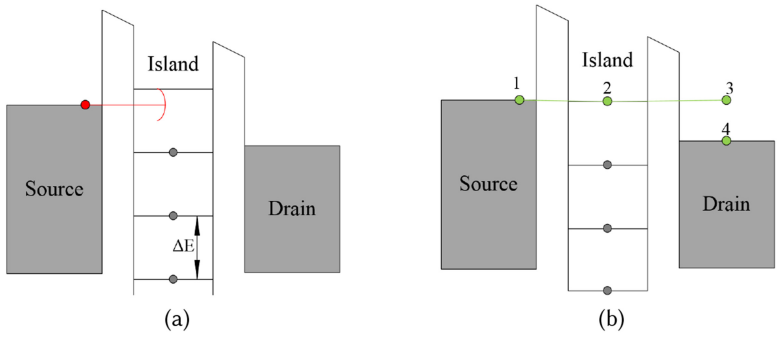


Fig. 10. Left to right: energy levels of source, island, and drain in a single-electron transistor for the (a) Blocking state and (b) Transmitting state [50].

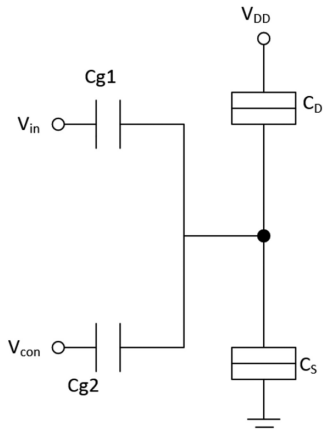


Fig. 11. Dual gate SET [52].

One of the key characteristics of a SET device is the possibility to include multiple gates that provide options to have an adjustable threshold voltage. Figure 11 demonstrates a dual gate SET, where C_{g1} and C_{g2} are the gate capacitances of gate 1 and gate 2, respectively, and C_D and C_S are the tunnel junction capacitors of the drain and source. One gate is used as the voltage input port and the other gate is defined as the threshold voltage adjusting port. The inputs for these two gates are V_{in} and V_{con}, respectively. The voltage on the island V_{island} controls the current flowing through two tunnel junctions and can be represented by Equation (8):

$$V_{island} = \frac{1}{C_\Sigma}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne). \tag{8}$$

Here, $C_\Sigma = C_{g1} + C_{g2} + C_D + C_S$ and n is the number of electrons on the island [51]. Considering the inherent threshold voltage of the island to be V_{th}, the condition for turning the SET on is

$$V_{island} > V_{th} \tag{9a}$$

$$\Rightarrow \frac{1}{C_\Sigma}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne) > V_{th} \tag{9b}$$

$$\Rightarrow V_{in} > \frac{C_\Sigma V_{th} - C_{g2} V_{con} - C_D V_{DS}}{c_{g1}}. \tag{9c}$$

Hence, the gate threshold voltage can be defined by Equation (10):

$$V'_{in} > \frac{C_{\sum} V_{th} - C_{g2} V_{con} - C_D V_{DS}}{c_{g1}}. \tag{10}$$

Using the concept of SET, a design is proposed in Reference [52] to implement basic ternary gates. Here, two different SET with two different threshold voltages V_{th1} and V_{th2} are used. The input voltage level is set in such a way that the voltage less than V_{th1} is considered to be logic "0," the voltage higher than V_{th2} is considered to be logic "2." And the intermediate voltage between V_{th1} and V_{th2} is considered to be logic "1." In Reference [53], new designs of ternary logic gates and ternary adder are proposed by merging the SET and MOS transistors. More arithmetic circuits like an adder, multiplier, and so on, circuits using are proposed in References [54, 55]. Some quaternary logic gates along with quaternary memory cells are proposed in Reference [56].

3.3.2 Analysis. SET offers very low power consumption, compact size, high operating speed, simpler circuits and operation, and straight to the co-integration with the traditional CMOS circuit [45]. The use of multiple gates makes it possible to have a variable threshold voltage that can be used for the design of MVL. To operate the SETs at the room-temperature large quantities of the monodispersed nanoparticles (lesser than 10 nm in the diameter) should be synthesized. However, as it is very difficult to fabricate the large quantities of SETs using traditional optical lithography and semiconductor processes. It is also very difficult to fabricate the SETs and link the SETs with the outside environment [57]. The major drawbacks are poor current drive capability as compared to CMOS devices and the need for low-temperature operation [58]. Also, the background charge problem is another major downside.

3.4 Quantum Dot Gate Field Effect Transistor-based Ternary Logic

3.4.1 Operating Principle. A quantum dot is a minuscule configuration of electrons enclosed in a three dimensional potential well and the size of the well is in the range of the size of de Broglie wavelength of electrons. Any quarantined atom or a multimolecular collection of atoms can also be called quantum dots. A quantum dot exhibits similar discrete, quantized energy levels like an atom and sometimes called an "artificial atom." By controlling the dimension of the quantum dots, the energy levels can be modified.

The structure of the QDGFET is similar to the MOSFET and can be fabricated using the conventional CMOS fabrication process that makes this technology more practical and appealing [59]. In a QDGFET, on top of the gate oxide layer, there are two layers of QDs. Upon application of a gate voltage, the charge carriers from the inversion channel move through the gate insulator to the QD layers through resonant tunneling, thus creating a new intermediate state in between the two stable states. The device structure of a QDGFET is shown in Figure 12(a).

The QDs that are deposited in the gate area is composed of nanocrystals of silicon (Si) or geranium (Ge), which are cladded by their oxide. Due to the presence of tunnel oxide enclosing the semiconductor nanocrystal, the charge leakage is reduced [61]. For a QDGFET, when gate voltage V_{GS} is increased, due to the effect of resonant tunneling, the threshold voltage V_{th} also increases, keeping the overdrive voltage $V_{GS} - V_{th}$ constant. The threshold voltage of a QDGFET can be expressed with Equation (11) [59]:

$$V_{Teff} = \begin{cases} V_T, & V_{GS} < V_{g1}, \\ V_T + \alpha(V_{GS} - V_{g1}), & V_{g1} < V_{GS} < V_{g2}, \\ V_T + \alpha(V_{g2} - V_{g1}), & V_{GS} > V_{g2}, \end{cases} \tag{11}$$

where V_{g1} and V_{g2} are, respectively, the lower and upper threshold voltage of the intermediate state and they are dependent on device structure. Within the range of V_{g1} and V_{g2}, the threshold voltage

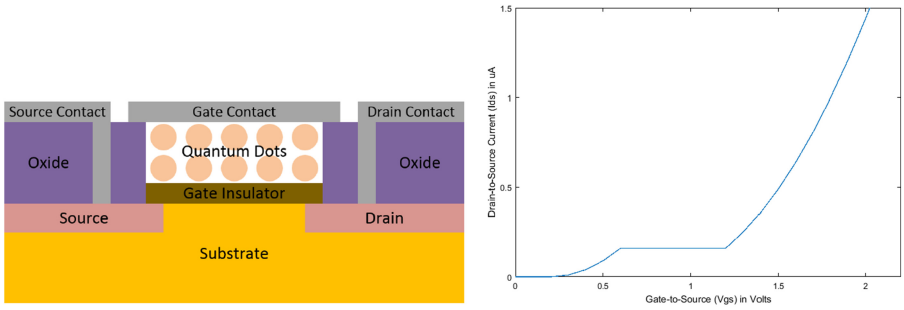


Fig. 12. (a) Structural diagram of QDGFET [60], (b) IDS vs. VGS in QDGFET.

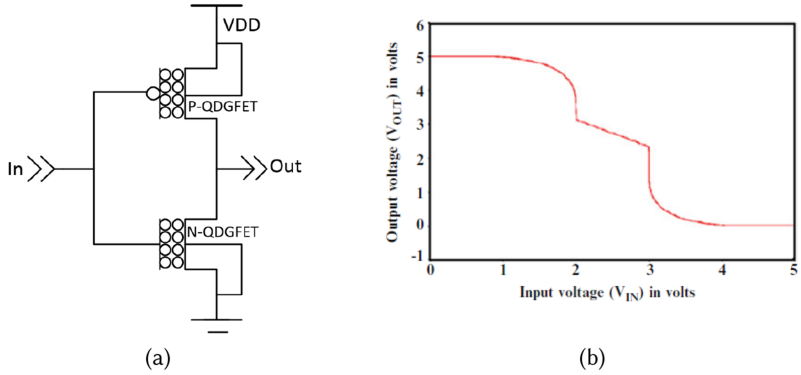


Fig. 13. (a) STI using QDGFET, (b) Transfer characteristics of QDGFET-based STI [62].

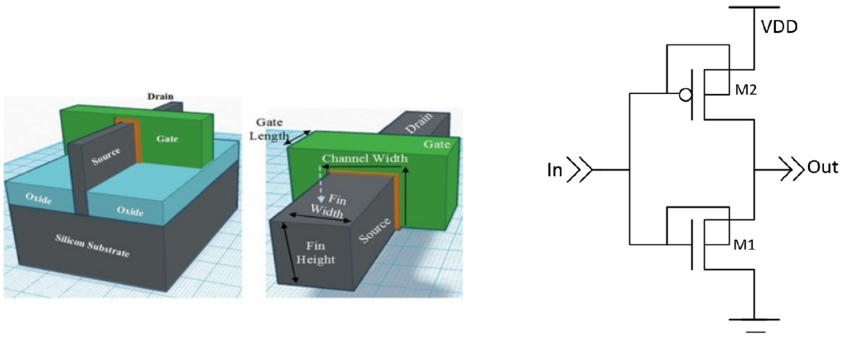
changes linearly with the gate voltage, and the rate of linearity depends on the value of α. When $\alpha = 0$, the device acts as a simple FET, and for $\alpha = 1$, the threshold voltage changes linearly with V_{GS}. The value of α can be controlled by changing the thickness of the insulator or by changing the size and number of dots [60]. And the drain current equation is [59]

$$I_D = \begin{cases} 0, & V_{GS} < V_{Teff}, \\ \frac{W}{L} C_o \mu (V_{GS} - V_{Teff} - \frac{V_{DS}}{2}) V_{DS}, & V_{DS} < V_{GS} - V_{Teff}, \\ \frac{W}{L} C_o \mu \frac{(V_{GS} - V_{Teff})^2}{2}, & V_{DS} > V_{GS} - V_{Teff}. \end{cases} \tag{12}$$

The graph derived from the drain current equation is shown in Figure 12(b). Figure 13 shows a CMOS representation of a standard ternary inverter using QDGFET and its transfer characteristics.

Similarly, ternary NAND, NOR, and so on, basic gates along with some combinational circuits have been designed using QDGFET in References [59, 61]. Being similar in the circuit diagram and fabrication process, QDGFET-based ternary circuits can be easily produced by prevailing binary logic gate architecture.

3.4.2 Analysis. QDGFET has a similar structure and operating principle to the SET. However, unlike SET, QDGFET does not suffer from the background charge problem. Moreover, it can be designed in the same way as the CMOS, reducing the design complexity to implement MVL logic. Despite all the advantages, more research is needed to be done in the field of QDGFET to come



(a) (b)

Fig. 14. (a) FinFET Structure [39], (b) FinFET-based STI [63].

to a secure conclusion. A limited number of literature is found on the fabrication as well as the circuit development of QDGFET.

3.5 Fin Field Effect Transistor-based Ternary Logic

3.5.1 Operating Principle. Whenever a lower node technology is introduced, it introduces different kinds of short dimension effects like carrier velocity saturation and mobility degradation, DIBL, punch-through, hot carrier effects, and so on. In a conventional CMOS system, the gate has lower control of the channel as it is situated far from the channel. One way to alleviate this situation is to make the channel above the substrate making a fin-like structure. The gate is wrapped around the fin-shaped channel giving better control of the channel. This gives rise to a vertical channeled device called FinFET in contrast to the horizontal channel of planer MOSFET. For FinFET, the height of the fin plays a crucial role in determining the channel width. The channel width L for FinFET can be derived using Equation (13) [39]:

$$L = 2 \times Fin_{Height} + Fin_{Width}. \tag{13}$$

FinFET can also be used to design ternary logic circuits. However, there are very few efforts to implement FinFET-based ternary logic. In terms of the working principle, the FinFET is identical to the conventional MOSFET. Therefore, the ternary or other multiple-valued logic implemented using FinFET would have a similar operating principle. However, due to better gate control in FinFET, it is anticipated that FinFET-based MVL would be more reliable compared to the conventional MOSFET-based MVL. Some of the ternary logic and adder designs based on FinFET are illustrated in References [63–65].

3.5.2 Analysis. FinFET devices are introduced by the industry to address the challenges associated with lower-node planar MOSFET technology [66]. FinFET is a very promising and the latest mass-produced Si-based transistor used in the production of microprocessor type VLSI circuits and systems. FinFETs have significantly better performance in terms of V_{th}, speed, and leakage because of the major geometrical change in the design of the channel. The increased control over the channel region through the wrapped up gate [67], the use of multiple-gate, body biasing, multiple supply voltages [68], and so on, gives a better threshold voltage control in FinFET devices that can be utilized to implement MVL devices. FinFETs are 3-D structures that need high aspect ratio etching with the non-uniform pitches or locally varying pitches, which is complex. Thus, FinFETs possess significant numbers of Restricted Design Rules. The body biasing

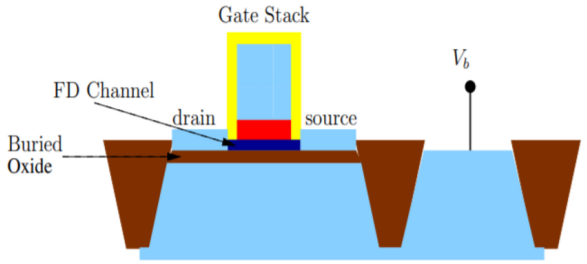


Fig. 15. Structural diagram of an FDSOI [8].

techniques are commonly used in planar which are less effective in FinFETs due to fully depleted channels. Accurate FinFET parasitic extraction is more complicated [69].

3.6 Fully Depleted Silicon on Insulator-based Ternary Logic

3.6.1 Operating Principle. Fully Depleted Silicon-on-Insulator (FD-SOI), is a planar process technology, which differs from a bulk-CMOS process in terms of an ultra-thin layer of insulator called the buried oxide, which is insulated from the channel. In an FDSOI, this oxide layer is placed on top of the base silicon. And then a very thin silicon film creates the transistor channel. As the silicon layer is very thin, no doping is needed for the channel, which makes the transistor fully depleted [70]. The structural diagram of an FDSOI is given in Figure 15. The advantages of a standard FDSOI are: Superior Junction capacitance, Higher Electro-static control of the channel in comparison to bulk CMOS, better threshold voltage (V_{th}) variation as the channel is not doped [71]. The transistor can be controlled through two independent gates. By the process of Reverse Body Biasing (RBB), the threshold voltage can be controlled to a great extent, which is not possible for bulk CMOS [8].

The technique of threshold voltage control enables FDSOI to be tried in the field of multiple-valued logic. Few literatures is present on the sector of FDSOI-based MVL design [9, 71, 72].

3.6.2 Analysis. FDSOI devices are one of the possible solutions for the scaling effects of conventional MOS technology. In the conventional MOS device, as the channel length shrinks, the gate cannot fully control the channel. This results in an increased sub-threshold leakage between drain and source. The structure of an FDSOI ensures more control of the gate over the channel, which results in lower leakage current [67]. One of the disadvantages of the SOI device is self-heating. In FDSOI, the active thin body, which is composed of silicon oxide, is a good thermal insulator. The power consumed by the active region during operation cannot dissipate easily. This effect increases the temperature of the thin body, which in turn reduces the mobility of the device. Another disadvantage of FDSOI is the difficulty of fabricating the thin body wafers [39]. Similar to FinFET, FDSOI fabrication technology is very matured and started to appear at an industrial level. But in the case of FDSOI-based MVL designs, most of the works done are very recent and at an initial stage.

3.7 Carbon Nano Tube Field Effect Transistor-based Ternary Logic

3.7.1 Operating Principle. Carbon Nano Tube (CNT) is made of a rolled-up graphene sheet. The rolling angle of the graphene sheet is known as chirality, which defines the behavior of the CNT's. Depending on the chirality vector (two variables, n and m, are commonly used to represent the chirality), a CNT can act as a metal or semiconductor. If $n = m$ or $n\text{-}m = 3i$ (where i is an integer value), then the CNT provides metallic behavior and if $n\text{-}m > 3i$, then the CNT shows semiconducting behavior. For a single-walled CNT, the relationship between the chirality (m,n)

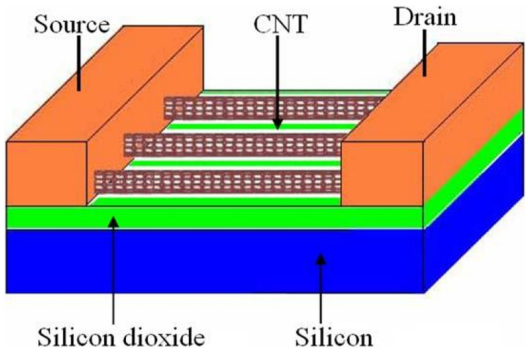


Fig. 16. Fundamental structure of a CNTFET [73].

and tube diameter (D_{cnt}) can be expressed as in Equation (14):

$$D_{cnt} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi}. \tag{14}$$

Here, $a = 2.49\ A^{\circ}$, which is the interatomic distance between two neighboring atoms. The chiral angle can be defined as in Equation (15) [74]:

$$\theta = tan^{-1}\frac{\sqrt{3}n}{2m + n}. \tag{15}$$

There exists quite a similarity between I-V characteristics of a CNTFET and a MOSFET. The threshold voltage of a device can be described in terms of the voltage required to turn the device ON. In the case of the CNTFET, the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half-bandgap that is an inverse function of the diameter [75]:

$$V_{th} \approx \frac{Eg}{2e} = \frac{aV\pi}{\sqrt{3} * eD_{cnt}}. \tag{16}$$

The parameter Vπ (3.033 eV) is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{cnt} is the diameter of a CNT. For a chirality vector of (19,0), the D_{cnt} is found to be 1.487 nm. Putting all the values in Equation (16), V_{th} is found to be 0.293 V. Considering m in the chirality vector to be 0, it can be derived from Equations (14) and (16) that the threshold voltage of the CNTFET is inversely proportional to the diameter of the CNT as well as the chirality vector n if the CNT:

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{cnt2}}{D_{cnt1}} = \frac{n_2}{n_1}. \tag{17}$$

Figure 16 gives a structural diagram of a CNTFET. Like a conventional CMOS, CNTFET also has four terminals. Here, the channel region is consisting of an undoped semiconducting carbon nanotubes or CNTs, which is present under the gate region. And some heavily doped CNT segments are placed between gate and source/drain to permit for a low series resistance in the on-state.

The main advantage of using CNTFET in a logic circuit is the opportunity of using transistors with different threshold voltage in the same circuit. Using this concept, two different standard ternary inverters (STI) were proposed in References [75, 76], which has their own merits and demerits. The proposed design in References [75, 76] is shown in Figures 17(a) and 17(b), respectively. In Figure 17(a), two CNTFETs with diameter $d_1 = 1.4$ nm and $d_2 = 0.5$ nm are used. As a result, the threshold voltages of the two CNTFETs are $V_{th1} = 300$ mV and $V_{th2} = 840$ mV, respectively. Two resistors both with the value 100 kΩ are used. When the input voltage is less than 300 mV, both the transistors are in off-state and the output voltage is equal to V_{dd} (1.5 V). For input voltage

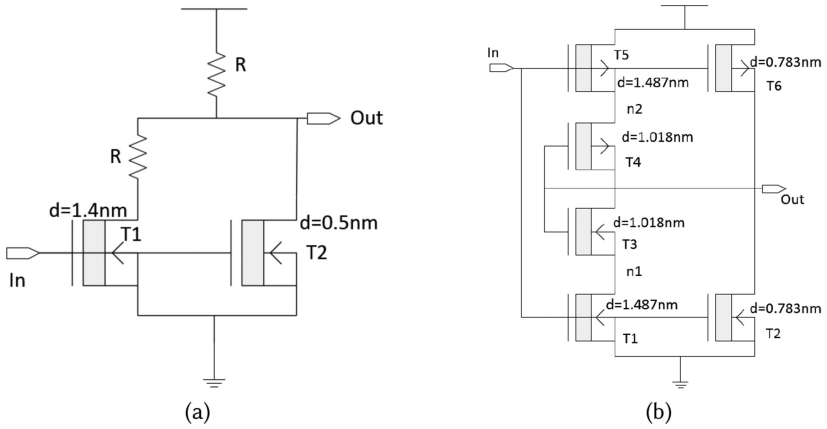


Fig. 17. Design of CNTFET-based inverter (a) [76], (b) [75].

greater than 300 mV, transistor $T1$ becomes on and the output voltage reaches the value near to $V_{dd}/2$. As input voltage becomes equal to V_{th2}, the second transistor is turned on and the output reaches an almost zero state. The proposed design in Reference [75] uses six transistors, which can be observed from Figure 17(b). The properties of the six transistors are given below:

- The chiralities of the CNTs used in $T1/T5$, $T2/T6$, and $T3/T4$ are (19, 0), (10, 0), and (13, 0), respectively.
- The diameters of $T1/T5$, $T2/T6$, and $T3/T4$ are 1.487, 0.783, and 1.018 nm, respectively.
- The threshold voltages of $T1$, $T2$, and $T3$ are 0.289, 0.559 and 0.428 V, respectively.
- The threshold voltages of $T5$, $T6$, and $T4$ are −0.289, −0.559, and −0.428 V, respectively.

As the input voltage is increased from low to high (low being 0 V and high being 0.9 V), primarily the input voltage is lower than 300 mV. This turns ON both the transistors $T5$ and $T6$, and both $T1$ and $T2$ are turned OFF; the output voltage is 0.9 V, i.e., logic 2. When the input voltage rises to a value greater than 300 mV, $T6$ is OFF and $T5$ is still ON and $T1$ is ON and $T2$ is OFF. The diode connecting the CNTFETs $T4$ and $T3$ generates a voltage drop of 0.45 V in-between node $n2$ and output and in between output and node $n1$ due to the threshold voltages of $T4$ and $T3$. Therefore, the output voltage takes a value of half of the power supply voltage, i.e., 0.45 V. From Table 2, it is seen that half V_{dd} represents logic 1. Once the input voltage goes above 0.6 V, both $T5$ and $T6$ are OFF, and $T2$ is ON to pull the output voltage down to zero. The transition from high to low is similar to the low to high transition. Besides this, there is another six-transistor-based design for the ternary inverter, which has been used by much other literature [77]. Based on the above-mentioned techniques, different other logic gates such as NAD, NOR, XOR can be constructed. Besides these, several other complex arithmetic circuits like the adder, multipliers, and so on, are also proposed in References [18, 78–82].

3.7.2 Analysis. CNTFET has characteristics that are qualitatively like silicon MOSFETs, and therefore, most of the conventional MOSFET circuits can be converted to CNTFET-based designs [83]. CNTFET's are a promising alternative for traditional bulk silicon-based MOSFET for the high-performance and low power designs because of its ballistic transport and low OFF-current properties. Also, in a CNTFET threshold voltage (Vth) is determined by CNT diameter; therefore, the multi-threshold design is accomplished by utilizing CNTs having different diameters (chirality) in a CNTFET [76]. Even though there are lots of merits to CNTFET-based electronics, it also comes

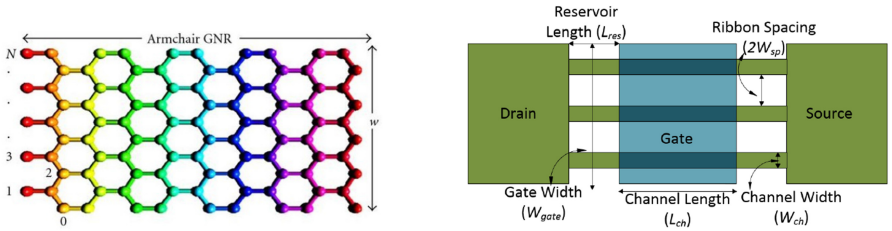


Fig. 18. (a) Width of an Armchair GNR with respect to Dimer lines [89], (b) A multiple (three) ribbon Armchair GNRFET [90].

with several challenges [84]. Further scaling is one of the challenges. Another challenge is multi-level interconnects, for instance, various metal layers are still unavailable with CNT.

3.8 GNRFET-based Ternary Logic

3.8.1 Operating Principle. Graphene is a two-dimensional sheet of carbon atoms tightly packed into a honeycomb lattice. It is a zero-band-gap material by nature. Graphene Nanoribbon (GNR) is narrow strips of graphene with widths below 50 nm [85]. Depending on the edge structure, GNR can be of two types: zigzag and armchair. While zigzag edged GNR always shows metallic characteristics, the armchair edged GNR can be either semiconducting or metallic, depending on the ribbon width. Figure 18 exhibits the structure of an Armchair Graphene Nanoribbon with N number of Dimer lines. The number of dimer lines (N) in a GNR strongly controls the semiconducting property of the GNR. The GNR shows semiconducting property mostly when $N = 3p$ or $3p+1$, p being an integer [86, 87]. Based on N, the width of a GNR can be expressed as in Equation (18), where a_{c-c} signifies the lattice constant and the value is equal to 0.142 nm [88]:

$$W_{GNR} = (N-1)\frac{\sqrt{3}}{2}a_{c-c}. \tag{18}$$

GNRFETs with GNR channels show complete switched off transistor state and large on-off current rations [86]. GNRFET contains another property of controlling the threshold voltage with regard to the width of the GNR. Based on the advantages of GNRFET technology, it is utilized for designing the proposed low voltage ternary logic gates circuit topology. Figure 18(b) represents a multiple (three) ribbon channel GNRFET. Different designs have been proposed using GNRFET for the implementation of ternary logic [91–95] and quaternary logic [96].

3.8.2 Analysis. The operating principle of GNRFET circuits is quite similar to the CNTFET circuit. As a result, it possesses all the benefits of CNTFET circuits in the application of MVL. The main advantage of GNRFET above CNTFET is the planner structure and fabrication similarity to MOSFET. In terms of the ternary circuit, GNRFET has been proved to be better in terms of noise margins, power consumption, and fastness [93]. However, the fabrication of GNRFET is still at an early stage. Line edge roughness is a common issue for the fabrication of a Graphene ribbon. Lots of research is going on for the simulation of precise and even-edged ribbon [97, 98].

3.9 Memristor-based Ternary Logic

3.9.1 Operating Principle. An alternative way to implement MVL circuits is to utilize resistors to achieve multiple voltage levels. However, the electrical properties of the resistor-based MVL circuits are not desirable [29]. Memristors are a good alternative to resistors for ternary-circuit design, because memristors are capable of handling more than two states with minimal hardware.

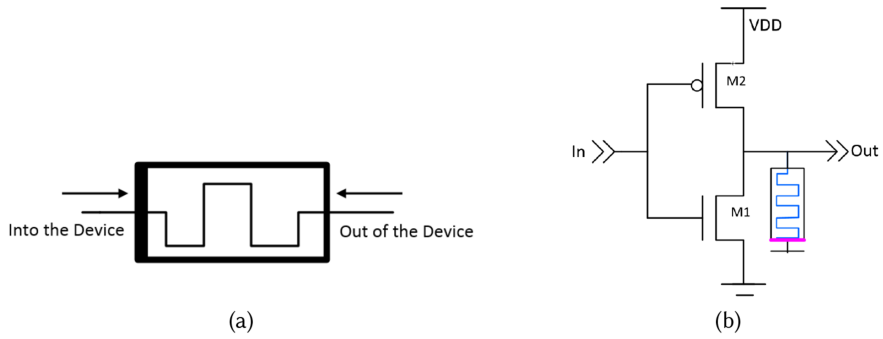


Fig. 19. (a) Memristive device symbol [99], (b) ternary inverter using MOSFET and Memristor [100].

Memristor is a nonvolatile passive memory element, which can retain its information even if there is no power supply, which is introduced by Chua Leon in 1971. The memristor is defined in terms of a non-linear functional relationship between magnetic flux $\phi_M(t)$ and the total amount of electric charge $q(t)$:

$$f(\phi_M(t), q(t)) = 0. \tag{19}$$

The correlation between $\phi_M(t)$ and $q(t)$, being the derivative of one with respect to other is depended on the value of either of them, hence the value of each memristor is characterized by its memristance function, which describes the charge-dependent rate of change of flux with charge. The change in the memristance is based on the history of the device:

$$M = \frac{d\phi}{dq}. \tag{20}$$

Figure 19(a) represents the symbol for a memristor symbol. The thick black line on the left side of the device represents the polarity of the device. If the current flows into the device, then the resistance of the device decreases, which can be defined as R_{on}. If the current flows out of the device, then the resistance increases and can be described as R_{off}. Formally, a current-controlled time-invariant memristive system is represented by:

$$\frac{dx}{dt} = f(x, i), \tag{21}$$

$$v(t) = R(x, i) \times i(t), \tag{22}$$

where x is an internal state variable, $i(t)$ is the memristive device current, $v(t)$ is the voltage of the memristive device, $R(x,i)$ is the memristance, and t is time [99]. A memristor is a very suitable alternative to resistive load ternary designs. A design to implement basic ternary logic gates like inverter, NAND, and NOR gates using MOSFET and memristor are given in Reference [100]. A diagram of a memristor-based ternary inverter is seen in Figure 19(b). Here, the memristor replaces the large resistors of a resistive-load MOSFET-based ternary logic design (Figure 2(b)). Besides these, memristor-based ternary logic circuits and adder is proposed in References [100, 101, 102].

3.9.2 Analysis. Though the concept of memristor had been proposed in 1971 [103], the use of memristor in ternary logic is quite new. A lot of scopes are present to implement MVL with the help of memristor technology. Until now, a hybrid of memristors along with some other technology has been tried. For instance, References [100, 102] work on MOSFET-memristor hybrid, whereas References [90, 104] work on a hybrid of CNTFET-memristor.

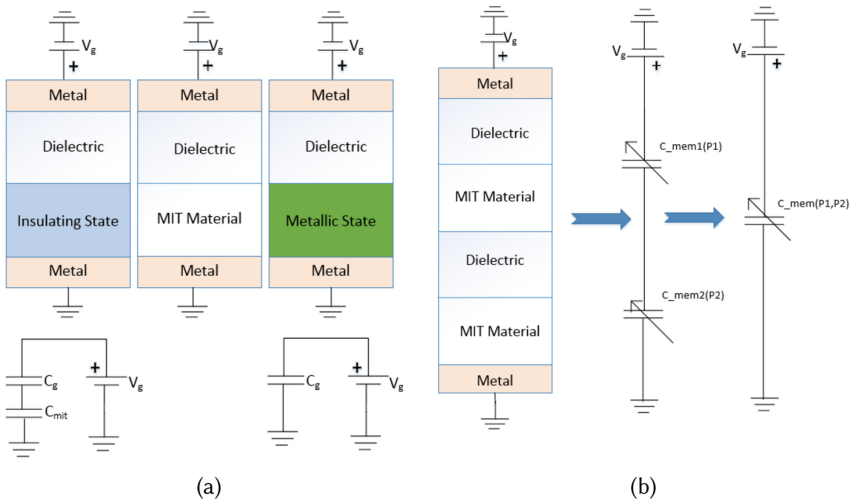


Fig. 20. (a) Proposed device structure in Reference [105], its virtual states, and schematic for metallic and insulating state of MIT material. (b) Vertically cascaded structure for three states with its equivalent schematics.

3.10 Ternary Logic Using Metal Insulator Transition Material-based Memcapacitive Modelling

3.10.1 Operating Principle. Memcapacitor are nonlinear capacitors with immediate response. Memcapacitor has the memory capacity and can exhibit different capacitance value upon applying any kind of external incentives like pressure, voltage, or current. Due to the presence of the memory holding capability, it can show different levels of capacitance with respect to time. Just like Memristor memcapacitor possess the capabilities to store data without the power source, which proves it to be a useful alternative for the multi valued design. Using MIT material is one of the ways to attain memcapacitance in a device. MIT is the property of some material that makes it possible for the material to switch between metal to insulating state with the application of external incitements like pressure, voltage, or temperature. This MIT behavior is one of the ways to achieve memcapacitive. A device is proposed in Reference [105], which utilizes MIT material to generate a memcapacitor-based ternary device. In that paper, the percolation phenomenon was used to describe this MIT phenomenon. Figure 20(a) shows the structural diagram. The structure consists of two metal electrodes, between which there is a layer of a dielectric material and a single layer of MIT material. When the gate voltage is applied to the top electrode, a charge puddle is created in the MIT layer, which transforms the insulating layer to a metallic state and thereby creates a continuous conducting channel.

Here, C_g represents the capacitance value introduced between the gate and the dielectric due to the presence of the gate voltage. And C_{mit} is the capacitance value of the MIT layer. The percolation probability, p varies between the values 0 to 1 and has a critical value $p_c = 0.4$. Within the range of $0 \leq p \leq p_c$ the MIT layer stays in the insulator region. And for the range of $p_c \leq p \leq 1$, the layer moves to the metallic region. The memcapacitance value can be expressed with respect to the percolation probability by Equation (23):

$$C_{mem}(p) = C_{total} + (C_g - C_{total}) \times p(t). \tag{23}$$

A simple cascading of the structure of Figure 20(a) can be used for generation of a ternary valued device, which is shown in Figure 20(b). The memcapacitance values of the upper and lower MIT

layer can be expressed by Equations (24) and (25):

$$C_{mem_1}(p) = C_{total_1} + (C_{g1} - C_{total_1}) \times p_1(t), \tag{24}$$

$$C_{mem_2}(p) = C_{total_2} + (C_{g2} - C_{total_2}) \times p_2(t). \tag{25}$$

Here, p_1 and p_2 are the percolative states of the upper and lower MoS_2 layers, respectively. The total memcapacitance C_{mem} of cascaded structure is equivalent to the series combination of C_{mem_1} and C_{mem_2}, which is shown in Equation (26):

$$C_{mem}(p_1, p_2) = \frac{C_{mem_1} \times C_{mem_2}}{C_{mem_1} + C_{mem_2}}. \tag{26}$$

Molybdenum disulphide (MoS_2) was used as MIT material in Reference [105]. The same experimentation was done with GNR to produce the similar results [106].

3.10.2 Analysis. The concept of a memcapacitor-based ternary device is very novel.The advantage of the device is the simplicity to attain the ternary logic cell by simply cascading the binary logic cell and the ability to work in psec range. The major drawback of this technology is that it is still at a conceptual stage. A lot more research is needed to compare it with other technologies. And the structural difference with CMOS technology makes the fabrication process far more complicated.

4 COMPARATIVE ANALYSIS OF DIFFERENT MVL TECHNOLOGIES

The theoretical understanding of MVL has been around since the beginning of the 20th Century. Research on many different technologies and implementation approaches for MVL devices has been going on for the last four decades. A summary of the findings of Section 3 regarding the prevailing technologies in the MVL system is given in Table 8. The summary is given in terms of circuit development, techniques used to implement the MVL circuits, advantages, and drawbacks of the respective technologies.

A comparative analysis of power and delay of the basic logic gates as well as the half adder for different technologies is given in Table 9. It needs to be mentioned that not all the technologies are developed to the same level in terms of fabrication maturity or circuit development. And different literature used different simulation conditions and software for measuring the power and delay values. The authors tried their best to encapsulate the values that are under a similar working condition and maintain a uniform standard. Several other literatures propose other complex arithmetic circuits like a full adder, multiplier, decoder, encoder, and so on, but that are not compared here because of the unavailability of enough material to compare.

5 CONCLUSION

The exponential progress of the prevailing computing system is supposed to face some complications in terms of data density and physical challenges. If they cannot meet the newer demands, then new computing paradigms will then be much needed. The present research works involving newer computing paradigms will be useful at that time. This article shows the different techniques used in designing the multiple-valued logic besides explaining the basic concept of multiple-valued logic. Moreover, it also explains the detailed description of different techniques on a device level and circuit level to design ternary valued logic. The technologies explained in the article can be divided into two major categories. One is the prevailing technologies like MOSFET, FinFET, FD-SOI, SET, and RTD. And another one is emerging technologies like Memristor, CNTFET, QDGFET, GNRFET, and so on. Among the prevailing technologies, MOSFET, SET, and RTD have been tried for a long time. Though SET and RTD hold huge promise in the field of MVL, using a whole

Table 8. A Summary of Different Technologies for MVL Designs

	Circuit Development	Implementation Technique	Advantages	Drawbacks
MOSFET	Basic logic gates as well as complex arithmetic circuits are available. Mostly on higher node technologies.	1. Combination of Depletion and Enhancement type MOSFET. 2. Enhancement type MOSFET along with resistors.	Currently prevailing technology which results in the best-matured fabrication process.	Saturation of Moore's law in lower node forces to look for more advanced technology like FinFET, FDSOI, etc.
RTD	Basic logic gates and few arithmetic circuits are developed.	Using Up/Down Literals	The concept of RTD is prevailing for a long time. Folding I-V characteristics makes it a very promising candidate for the MVL system.	There are very few current works involving RTD-based MVL.
SET	Basic logic gates and few arithmetic circuits are developed.	Using Multiple gates to obtain controllable threshold voltage	The threshold voltage is easily controllable through the multiple gates.	The challenges of fabrication of SET using the prevailing process is still a major issue. Few recent works are being done on SET-MOS hybrid technology.
QDGFET	Few designs have been proposed for QDGFET-based logic gates and arithmetic circuits.	Threshold voltage control	The simulation results show a very promising outcome.	More work needs to be done to estimate all the pros and cons of QDGFET-based MVL. Very few instances of fabrication of QDGFET is available.
FinFET	Though FinFET is a very promising technology for the MVL system, the circuit designs are not developed. Most of the available works are on simple logic gates like an inverter.	Threshold voltage control	The fabrication of FinFET found on the industrial level. In the case of lower node technology, FinFET is expected to alleviate the challenges associated with MOSFET.	Fewer research on FinFET-based MVL design.
FDSOI	Very few complex arithmetic circuits are proposed to this day. Few designs for MVL FPGA (Field Programmable Gate Arrays) have been proposed.	Threshold voltage control through the back gate.	Matured fabrication technology, lower short channel effects, etc.	MVL circuit development is not matured. Heating problems and difficulty to fabricate thin bodies.
CNTFET	A significant number of designs are available for basic logic gates as well as complex arithmetic circuits.	Threshold voltage control through the control of the chirality values of the CNT.	In the developed fabrication process, an ample amount of study is available for CNTFET.	Fabrication complexity like gate alignment challenge and incompatibility to planner technology.
GNRFET	Basic logic gates and few arithmetic circuits are developed.	Threshold voltage control through the control of the width of the GNR.	Due to the planer structure, it has the potential to use in the existing MOSFET fabrication process.	Few fabrication challenges like line edge roughness are present. The fabrication process is currently developing.
Memristor	Few designs have been proposed for Memristor-based logic gates and arithmetic circuits.	Replacement of Resistor in MOSFET-based designs.	Currently, Memristor is being extensively researched for its numerous potential applications.	The fabrication of hybrid of MOSFET-Memristor or CNTFET-Memristor is on a preliminary level.
Metal-insulator Transition (MIT) material-based memcapacitive modeling	Circuit-level implementation is not developed.	Changing memcapacitance of the device using Metal to insulator transition method.	The use of a two-terminal device is an interesting concept which contributes to a very simple operating mechanism.	Most of the work is on a conceptual level.

Table 9. Comparative Analysis of MVL Designs for Different Technologies

	Gates	Inverter			NAND			NOR			Half-Adder		
	Technology	Delay	Power	PDP	Delay	Power	PDP	Delay	Power	PDP	Delay	Power	PDP
[31]	MOSFET	17.3n	133n	2.3f									
[107]	MOSFET	26.6p	0.24n	0.006a	40.9p	0.27n	0.0011a	42.6p	0.27n	0.012a			
[108]	45nm MOSFET	1.14p	0.065u	0.07a		0.19m			0.21m				
[56]	SET	80p	0.92n	0.074a	70p	0.41n	0.028p	100p	0.44n	0.044a			
[59]	22nm QDGFET	11.9p	0.13n	0.001a									15a
[61]	32nm QDGFET	1.1p	24n	0.026a									
[65]	120nm FinFET	1.13p	800n	0.9a	40n	1.87u	75f				7.7n	1.9n	12.8a
[63]	32nm FinFET	12n	3.4n	42a	60n	8.7n	522a	14n	13.5n	190a			
[91]	32nm FinFET	31.2p	12.6u	39.5a	46.4p	16.6u	771.9a	45.6p	17.2u	785a			
[72]	32nm FDSOI (Quaternary)	6.1p	4p	0.02z	15n	0.3p	4.47z	45p	8.07p	0.36z			
[18]	16nm CNTFET	11p	88.6n	0.98a	3p	100.8n	0.3a	2p	100n	0.2a	116.5p	3.5u	411a
[80]	16nm CNTFET	8.9p	260n	2.3a									
[81]	20nm CNTFET										241.8p	497n	117.4a
[82]	32nm CNTFET										28.4p	880n	25a
[78]	7nm CNTFET	155.3p	145.7p	0.02a		148.3p			367.7p				
[79]	CNTFET										16.5p	249n	4.11a
[109]	CNTFET	12.5p	0.27a	3.43									
[110]	32nm CNTFET (Quaternary)	102.7p	1.69u	173.5a									
[91]	32nm GNRFET	30.2p	8.1u	24.6a	59p	1.6u	93.5a	47.8p	1.6u	78.4a			
[92]	32nm SB-GNRFET	1.6p	22.2u	34.9a	129n	33u	0.426p	9n	27u	0.15p			
[95]	16nm GNRFET	13p	23.22n	0.302a	5.2p	27.5n	0.14a	3.33p	27.42n	0.1a			10a
[96]	15nm GNRFET (Quaternary)	0.22p	11.8u	2.59a									

*Delays and powers are explained in terms of powers of 10. "n," "p," "f," "a," and "z" denote nano (10^{-9}), pico (10^{-12}), femto (10^{-15}), atto (10^{-18}), and zepto (10^{-21}), respectively.

new technology that is completely different from the present CMOS technology would be a huge step. And it can lead to a different fabrication complexity that was not seen with MOSFET technology. FinFET and FDSOI, however, improves the limitations that come with MOSFET without having to modify lots of fabrication techniques. In addition to this, they are already been used in place of MOSFET in different sectors. However, among the emerging and futuristic technologies, carbon-based transistors hold the most potential for implementing MVL. Though CNTFET has been the topic of interest for a longer time than GNRFET, GNRFET has the advantages of a planner structure, which makes it a more suitable substitute for MOSFET. But in terms of fabrication,

the maturity of CNTFET is very much well ahead of GNRFET and other emerging technologies. The major drawback of the MVL system is the abundant usage of the binary system on most of the computing system. It might not be possible for the MVL system to replace the binary system at once, but MVL has already started to make its way, especially in terms of MVL memory. As the operating voltage of the memory system is still high compared to the arithmetic system, the problem associated with the low operating voltage for MVL is not a big issue here. Also, in the case of arithmetic circuits, ternary and quaternary logic circuits have been proposed, which was proven to give very good results with low operating voltage.

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