FAULT DIAGNOSIS AND CONDITION MONITORING OF POWER ELECTRONIC COMPONENTS USING SPREAD SPECTRUM TIME DOMAIN REFLECTOMETRY (SSTDR) AND THE CONCEPT OF DYNAMIC SAFE OPERATING AREA (SOA)

A DISSERTATION IN
Electrical Engineering
and
Mathematics

Presented to the Faculty of the University of
Missouri-Kansas City in partial fulfillment of
the requirements for the degree

DOCTOR OF PHILOSOPHY

by
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M.S., Electrical Engineering,
University of Missouri-Kansas City, 2020

Kansas City, Missouri
2021

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ABSTRACT

Fault diagnosis and condition monitoring (CM) of power electronic components with a goal of improving system reliability and availability have been one of the major focus areas in the power electronics field in the last decades. Power semiconductor devices such as metal oxide semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) are considered to be the most fragile element of the power electronic systems and their reliability degrades with time due to mechanical and thermo-electrical stresses, which ultimately leads to a complete failure of the overall power conversion systems. Therefore, it is important to know the present state of health (SOH) of the power devices and the remaining useful life (RUL) of a power converter in order to perform preventive scheduled maintenance, which will eventually lead to increased system availability and reduced cost. In conventional practice, device aging and lifetime prediction techniques rely on the estimation of the meantime to failure (MTTF), a value that represents the expected lifespan of a device. MTTF predicts expected lifespan, but cannot adequately predict failures attributed to unusual circumstances or continuous overstress and premature degradation. This inability is due in large part to the fact that it considers the device safe operating area (SOA) or voltage and

current ride-through capability to be independent of SOH. However, we experimentally proved that SOA of any semiconductor device goes down with the increased level of aging, and therefore, the probability of occurrence of over-voltage/current situation increases. As a result, the MTTF of the device as well as the overall converter reliability reduces with aging. That said, device degradation can be estimated by accomplishing an accurate online degradation monitoring tool that will determine the dynamic SOA. The correlation between aging and dynamic SOA gives us the useful remaining life of the device or the availability of a circuit. For this monitoring tool, spread spectrum time domain reflectometry (SSTDR) has been proposed and was successfully implemented in live power converters. In SSTDR, a high-frequency sine-modulated pseudo-noise sequence (SMPNS) is sent through the system, and reflections from age-related impedance discontinuities return to the test end where they are analyzed. In the past, SSTDR has been successfully used for device degradation detection in power converters while running at static conditions. However, the rapid variation in impedance throughout the entire live converter circuit caused by the fast-switching operation makes CM more challenging while using SSTDR. The algorithms and techniques developed in this project have overcome this challenge and demonstrated that the SSTDR test data are consistent with the aging of the power devices and do not affect the switching performance of the modulation process even the test signal is applied across the gate-source interface of the power MOSFET. This implies that the SSTDR technique can be integrated with the gate driver module, thereby creating a new platform for an intelligent gate-driver architecture (IGDA) that enables real-time health monitoring of power devices while performing features offered by a commercially available driver.

Another application of SSTDR in power electronic systems is the ground fault prediction and detection technique for PV arrays. Protecting PV arrays from ground faults that lead to fire hazards and power loss is imperative to maintaining safe and effective solar power operations. Unlike many standard detection methods, SSTDR does not depend on fault current, therefore, can be implemented for testing ground faults at night or low illumination. However, wide variation in impedance throughout different materials and interconnections makes fault location more challenging than fault detection. This barrier was surmounted by the SSTDR-based fault detection algorithm developed in this project. The proposed algorithm was accounted for any variation in the number of strings, fault resistance, and the number of faults. In addition to its general utility for fault detection, the proposed algorithm can identify the location of multiple faults using only a single measurement point, thereby working as a preventative measure to protect the entire system at a reduced cost.

Within the scope of the research work on SSTDR-based fault diagnosis and CM of power electronic components, a cell-level SOH measurement tool has been proposed that utilizes SSTDR to detect the location and aging of individual degraded cells in a large series-parallel connected Li-ion battery pack. This information of cell level SOH along with the respective cell location is critical to calculating the SOH of a battery pack and its remaining useful lifetime since the initial SOH of Li-ion cells varies under different manufacturing processes and operating conditions, causing them to perform inconsistently and thereby affect the performance of the entire battery pack in real-life applications. Unfortunately, today's BMS considers the SOH of the entire battery pack/cell string as a single SOH and therefore, cannot monitor the SOH at the cell level. A healthy battery string has a specific impedance between the two terminals, and any aged cell in that string will change the impedance value. Since

SSTDR can characterize the impedance change in its propagation path along with its location, it can successfully locate the degraded cell in a large battery pack and thereby, can prevent premature failure and catastrophic danger by performing scheduled maintenance.

APPROVAL PAGE

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ACKNOWLEDGEMENTS

This research work was partially supported by the National Science Foundation (NSF) grant# 1947410, University of Missouri System FastTrack grant, and School of Graduate Studies research grant program, University of Missouri-Kansas City (UMKC).

Firstly, I would like to express my sincere gratitude to my advisor, Dr. Faisal Khan who has been extremely supportive since the days I started working at the Missouri Center for Advanced Power (MCAP). His expertise was invaluable in formulating the research questions and methodology. His insightful feedback pushed me to sharpen my thinking and brought my work to a higher level. He always encouraged me whenever I felt depressed because of not getting a successful outcome, even though I was working hard. On top of that, Dr. Khan inspired me to take the lead of my own research projects that improved my independent research skills and developed persistence in me to learn new skills in a very short period of time. He is one of the smartest people I came to know, and I could not have imagined having a better advisor and mentor for my Ph.D. study. I hope that I could be as lively, enthusiastic, and energetic as Dr. Khan.

Apart from my Ph.D. supervisor, I would not forget to express the gratitude to the rest of my Ph.D. committee members Dr. Yong Zeng, Dr. Masud Chowdhury, Dr. Ahmed Hassan, Dr. Ghulam Chaudhry, and Dr. Kamel Rekab for their advice, support, and guidance throughout my degree. I would also like to thank the outside reader of my Ph.D. committee, Dr. Mohammed Alam for his advice and suggestions in my research in the field of fault diagnosis of photovoltaic systems. Special thanks should be given to Dr. Anthony Caruso for his extensive personal and professional guidance. He also provided me with the great

opportunity to work in collaboration with talented, passionate, and diverse individuals of the Missouri Institute of Defense and Energy (MIDE) that allowed me to have unique learning experiences, especially in terms of time and project management.

I would also like to thank my fellow lab mates Abu Hanif, Wasek Azad, and Swagat Das for the fun-time we spent together, for the sleepless nights that enabled us to complete tasks before deadlines, for stimulating the discussions, and for happy distractions to rest my mind outside of my research.

Last but not the least, I am grateful to my parents and siblings for remembering me in their prayers for my ultimate success. My hard-working parents have sacrificed their lives for me and provided unconditional love and care. Nobody has been more important to me in the pursuit of my Ph.D. than the members of my family- my wife Mitaly Biswas and my little son Liam Roy. Mitaly was always with me in all difficult times I have come across. Whatever I write in the acknowledgments will never do justice to the sacrifices she has made for me to make my research work a priority in our lives and achieve my objective without any obstacle in the way.

DEDICATION

To my parents, my elder brother, and my wife, without them I would have been nothing.

.

CHAPTER 1

1 INTRODUCTION

Power semiconductor switching devices such as metal oxide silicon field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) are indispensable elements in any power conversion system, especially where heavy but critical power is required. Unfortunately, these power semiconductor devices are failure-prone and when they fail, results can be catastrophic. Therefore, it is of paramount importance to predict the device failures before they happen which will reduce the maintenance cost and can potentially save human lives. The mean time to failure (MTTF) represents the expected lifespan of the device although it cannot adequately predict unusual circumstances or continuous overstress and premature degradation which makes the power switch fail before its MTTF. In practice, the MTTF of the device as well as the overall converter reliability decreases when a device undergoes aging [1]. For a long time, we knew about this fact, but we have not yet pinpointed the reason(s). According to our study and experimental validation in our laboratory, the safe operating area (SOA) of any semiconductor device goes down with the increased level of aging, and this observation explains why the reliability or MTTF of an entire circuit exponentially drops with aging. SOA is a well-known device parameter that indicates the device's ride-through-capability against over-voltage and over-current situations [2]. In all calculations, MTTF predicts the constant value of SOA of power switching devices, and the overall reliability of the circuit simply becomes the probability of an abnormal condition to occur and the probability of other device failures. However, SOA of any semiconductor device is age-dependent rather than static as considered in reported literature to-date, and this age-dependent SOA is the underlying reason for device failure especially when the device is subjected to

accidental over-voltage/current [3]. Based on the outcome of this breakthrough research, the following chronological order/steps are involved in the process of finding out the remaining useful life (RUL) of a power semiconductor device:

a) Accidental over-voltage and current can damage both a healthy and aged device although the probabilities would be different. A healthy (new) device may override multiple overstressed situations, but an aged device is less likely to override those anomalies. This is the underlying reason for the increased failure rate of a circuit once the devices are aged.

b) In all calculations, we assume the SOA of a device to be constant. According to our recent test results, SOA changes with aging, i.e. SOA goes down with higher aging.

c) Remaining life of a switch is a function of SOA.

d) Therefore, the remaining life goes down with higher aging.

e) For high-power devices such as MOSFETs and IGBTs, aging is caused by bond wire detachment, cracks in the bond wire interface, voids in the wafer and other packaging issues. By knowing the device health using online condition monitoring (CM), it is possible to accurately estimate aging.

f) Therefore, by accomplishing (e), we can estimate aging. By knowing aging, we can determine dynamic SOA. *The correlation between aging and dynamic SOA gives us the useful remaining life of the device or the availability of a circuit*.

Fig. 1.1 demonstrates the above-mentioned steps chronologically. Finding the remaining life of a power converter is the ultimate objective to ensure the uninterrupted operation of a power electronic system. Therefore, online state-of-health (SOH) monitoring/ CM of semiconductor devices need to be performed to measure the level of aging, which can be used to identify the dynamic SOA, and thus, to predict the MTTF of the overall circuit. SOH

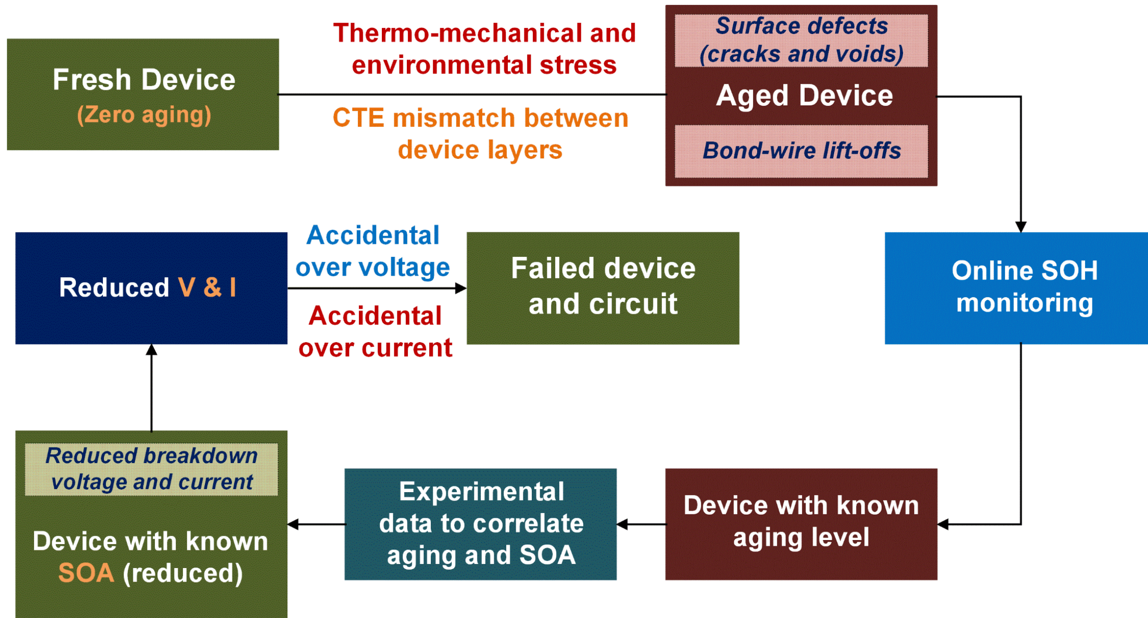


Figure 1.1 Block diagram of the proposed steps involved in the work strategy in determining remaining lifetime estimation of power semiconductors.

estimation or CM of power switches is a fairly well-established area, although better accuracy is still needed [4]–[7]. Variations in electrical parameters (i.e. ON-state channel resistance ($R_{DS(ON)}$), collector-emitter voltage in saturation ($V_{CE(SAT)}$), gate-source threshold voltage ($V_{GS(TH)}$), gate leakage current (I_{GSLK}), transconductance or saturation current, or switching turn ON (T_{ON}) and turn OFF (T_{OFF}) times, etc.) carry the degradation information in most of the chip-and package-related failures such as gate structure degradation, wire-bond lift offs, solder fatigues and so on [7]–[17]. The research to date is primarily focused on characterizing the device degradation using both direct and indirect methods of measuring the above-mentioned aging precursors. Traditional CM methods for power converters are based on failure precursor measurement of power devices [20]–[28], system identification [29], [30], data-driven or model analysis [31], [32], and so on [12], [33]. Among them, precursor measurement-based CM methods require additional noise-immune, high-resolution sensors and digital controllers,

which may not be cost-effective. Other methods require either an advanced signal processing algorithm or a large number of training data which increases the computational burden.

To overcome the limitations of real-time power converter health monitoring techniques, reflectometry-based method has recently been proven to become a good candidate because this technique does not depend on the direct measurement of the traditional on-site parameters and sensors to detect device aging levels, and therefore reduces the measurement error. Different reflectometry-based methods have long been used for detection and locating faults in transmission lines, and a comparative study summarizing different reflectometry methods for fault detection in electrical wiring has been discussed in [34]. Among the known reflectometry techniques, spread spectrum time-domain reflectometry (SSTDR) provides several advantages such as low-cost fault detection in powered/live cables, very high noise immunity, embedded solutions, etc. over the other reflectometry-based techniques [34]–[39]. The incident signal of SSTDR is a high-frequency sine modulated pseudo-noise sequence (SMPNS), and the corresponding reflections may identify faults and characterize the level of aging by determining the changes in the impedance in its propagation path. Each type of device degradation leads to various impedance changes inside a power device such as $R_{DS(ON)}$, gate-source capacitor impedance ($Z_{eq,GS}$), and so on, therefore, this unique feature makes SSTDR an excellent candidate for estimating any device's SOH. Recently, the SSTDR-based technique has been proposed in [40]–[44] for estimating the level of aging associated with power semiconductor switches. However, these techniques could only estimate the device SOH while it was in full conduction mode. Therefore, these methods are only effective while the device is isolated from the circuit and subjected to a dedicated characterization setup with no modulation applied at the gate. That being said, the fast impedance variations in the SSTDR signal

propagation path due to high-frequency PWM switching of a live semiconductor device makes interpretation of the SSTDR reflection extremely difficult. The algorithm proposed in this paper demonstrates that SSTDR data can be implemented to overcome such limitations resulting in faithful aging detection in power semiconductor switches during the converter operation.

In this research, we performed several case studies regarding real-time SOH estimation or CM of power devices in live converter circuits. First, an H-bridge single-phase grid-tied PV inverter was considered where the SSTDR incident signal has been applied across its ac output terminal nodes [45]. Using the experimental results, we were able to successfully characterize the degradation level in multiple MOSFETs from this single measurement point. Later, the SSTDR test signal (SMPNS) was applied across the gate-source interface of a power semiconductor device in buck converters [46], [47] and a three-phase dc-ac inverter [48]–[50], respectively. Due to the simple implementation of the SSTDR test signal into the gate-source interface, the SSTDR scheme can potentially be embedded into commercial gate drivers offering built-in-self-test capability which will eliminate the need for a separate CM module leading to significant system-level savings. This CM hardware embedded gate driver module can be termed as Intelligent Gate Driver Module (IGDM). This IGDM will make the CM possible for high voltage converters because the gate terminal always remains at a lower potential than that of the collector/emitter side and the driver module needs to be connected to the low voltage gate-side anyway. Last but not the least, connecting SSTDR hardware to the low voltage gate terminal will help in designing it for significantly lower ratings which will considerably reduce the cost of the overall CM hardware.

As of today, there is no similar technology that can combine the level of aging (determined by SSTDR) and the corresponding change in SOA yielding the true SOA of a device without destroying it. Estimating the remaining life will allow for scheduled maintenance of any high-power converter thus enabling reduced maintenance cost. Known availability will help to select the proper converter for any specific application, and the estimation of dynamic SOA will allow the operator to choose whether the converter could be operated at full power level.

In addition to CM of live semiconductor power devices, SSTDR can be used for detecting and locating ground faults in photovoltaics (PV) array [51], [52]. PV arrays in solar PV systems are vulnerable to various types of fault occurrences and among them, ground faults are considered to be the most common fault and are reported to be one of the major reasons behind catastrophic failures resulting in electrical fires and shock hazard [53]. According to the U.S. National Electrical Code-690 (NEC-690), PV array must be protected against ground fault detection and interruption (GFDI) fuses [54]–[57]. However, even with the use of this standard protection device in a PV system, faults occurring in a PV array may remain undetected, especially when the fault current falls within the blind spot range because of the low irradiance and high fault impedances [53], [58], [59]. Apart from ground-fault detection devices, several ground fault detection techniques have been proposed in recent years [60]–[73], and most of them require several on-site parameters such as voltage, current, irradiance level, temperature, etc., for accurate fault detection. Dependency on the measurement of these parameters may result in false detection since a change in weather condition, partial shading, etc. often affects these parameters and thus the *I–V* characteristics/MPPT of the PV panel [53], [74]–[81]. In contrast, SSTDR can become an excellent candidate for PV array fault detection,

especially for testing ground faults at night or low illumination, because this method does not use traditional on-site parameters and sensors to detect faults. A healthy PV array has a specific impedance between node pairs, and any ground fault changes these impedance values which can be characterized by SSTDR. However, the wide variation in impedance throughout the entire PV system, which is caused by the use of different materials and interconnections makes PV fault detection more challenging while using SSTDR. In this research, an algorithm centered around SSTDR has been developed that can overcome this challenge and can detect the ground fault in PV arrays with any variation in the number of PV strings, the number of faults (single or double), and values of fault impedances [52].

This manuscript also presents a cell-level SOH measurement technique based on SSTDR that can identify the location and amount of aging of a degraded cell in a large Li-ion battery pack [82]. Li-ion batteries have become the most popular sources of energy storage for today's electric vehicles and renewable energy systems due to their higher energy density, lower self-discharge rate, reduced size, and weight compared to other rechargeable batteries [83]. Depending on the application, a large number of Li-ion cells (tens or hundreds) are connected in series-parallel combinations in a single pack to meet the high-power and voltage demand [84]. However, like other battery chemistries, Li-ion batteries suffer from performance degradation over time with the increased number of charging and discharging cycles, elevated temperatures and so on. Because of the inconsistency in the manufacturing process or non-uniform operating conditions, the initial SOH of one or more cells can be different that affects the performance of the entire battery pack in real-life applications [85]. Therefore, cell level SOH along with the respective cell location is a crucial metric for the battery management system (BMS) to predict the remaining useful lifetime of the entire battery pack and avoid

unwanted failures and catastrophic hazards in battery systems. Unfortunately, today's BMS cannot monitor the SOH at the cell level. To confront this issue, we propose to use SSTDR as a signature to quantify the SOH of the aged cell along with its location information in a large battery pack using its unique ability to characterize the age-related impedance variation in any device. The proposed method can determine the SOH of both the individual cells and the overall battery pack using a single measurement point that helps to monitor the remaining life in a lithium-ion battery pack and facilitate timely and cost-effective maintenance.

In Chapter 2, a literature review on the origin of degradation in power semiconductor devices is given at the beginning which is followed by a literature review on the origin of degradation in Li-ion cell in large battery pack along with the causes of ground fault occurrence in PV array system. Chapter 2 also discusses the limitations of existing aging measurement techniques of live power devices in power converters and Li-ion battery packs, and ground fault detection techniques in PV arrays. The fundamentals of the proposed SSTDR-based methods to detect faults and aging in power electronic components have been introduced in Chapter 3. To perform CM of power devices in live power converters in a laboratory environment, reference failure tests and reliability data such as test data for devices under tests (DUTs) of known aging levels are necessary [31]. However, these devices are meant to last for millions of cycles under normal and ideal operating conditions. To accelerate the fatigue process, accelerated aging tests are widely recognized, and had been demonstrated by many research groups. Chapter 4 discusses the test set-up for accelerated aging of power MOSFETs developed in the laboratory. An industry-standard accelerated battery cycling test was also performed to induce degradation in Li-ion cells and this process has been illustrated in chapter 4 as well. Chapter 5 summarizes the CM technique of a single-phase H-bridge grid-tied PV

inverter applying SSTDR test signal across the ac output node. Chapter 5 also describes the CM technique of DC-DC converters and a 3-phase power inverter applying SSTDR embedded PWM signal across the gate-source interface. SSTDR-based CM technique in a live H-bridge PV inverter and DC-DC converters was performed at the cost of a large amount of SSTDR data acquisition for the purpose of error reduction where the error is caused by the rapid variation in impedance throughout the entire live converter circuit due to the fast-switching operation. An advanced statistical algorithm has been incorporated in order to analyze the large number of SSTDR test data which has been discussed in detail in Chapter 5. In contrast, such limitations of data-intensive computing can be overcome by a little modification in the switching scheme inside a three-phase inverter, and this dissertation has presented this concept in detail in Chapter 5 as well. PV ground fault detection and location technique based on SSTDR has been presented in Chapter 6. A cell-level SOH estimation technique based on SSTDR capable of identifying aged cells in a large lithium-ion battery pack has been described in detail in Chapter 7. Chapter 8 demonstrated how the SOA of a power semiconductor device is impacted by aging and corresponding experimental results have been documented. In addition, a case study showing the relationship between dynamic SOA and the probability of occurring a failure for a specific circuit is investigated in Chapter 8. Finally, Chapter 9 summarizes the work presented in this dissertation. Future directions of the research on fault diagnosis and CM of power electronic components are also provided in the final chapter (Chapter 9).

CHAPTER 2

2 BACKGROUND STUDY AND LITERATURE REVIEW

2.1 Degradation Assessment and Precursor Identification of Power Semiconductor Device in Live Power Converters

A power converter is an integral part of most consumer and industrial products needing electric power. Various segments such as upcoming all-electric aircraft industry, existing motor drive market, space mission, electric automotive, health sector, renewable energy market, high voltage direct current (HVDC) substation and many others require the use of power converters. Power converters are built from one or more power semiconductor devices (typically MOSFET or IGBT), capacitors, inductors, and low power controller circuits. Among various components of a power converter, the power semiconductor device has been reported to be the most failure-prone element. In an industry-based survey conducted in [86] (shown in

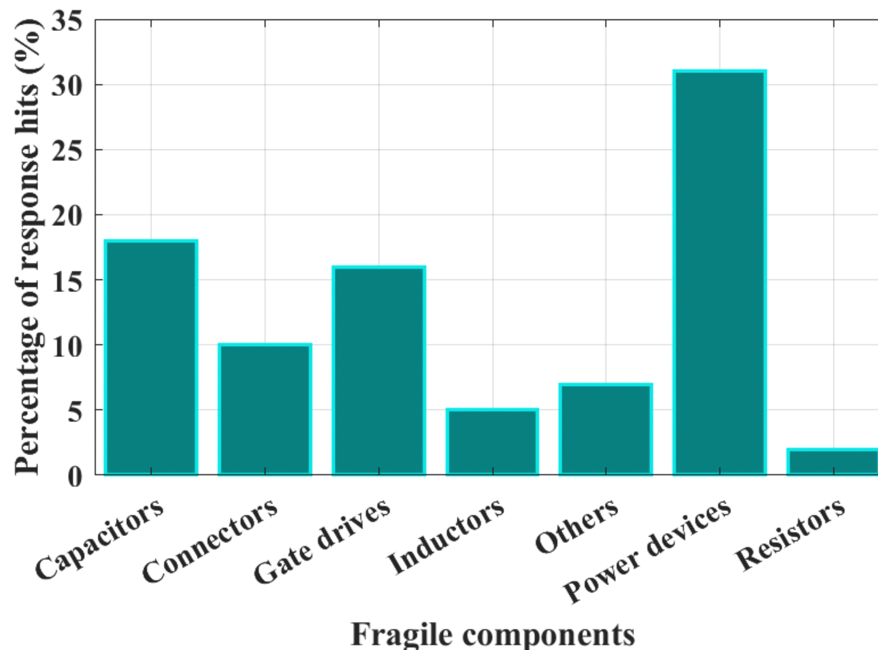


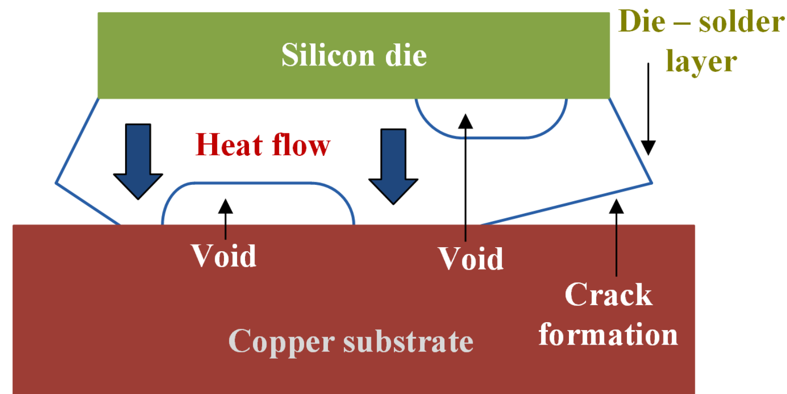
Figure 2.1 Survey of different components responsible for converter failure [86].

Fig. 2.1), about one-third of the responders answered that the power semiconductor device is the most fragile component in the power electronic system. Reliability of these critical components degrades with time due to mechanical and thermo-electrical stresses during regular operation, therefore downgrading the performance or even complete failure of the overall power conversion systems. The statistics found in [87] show that degradation in power devices accounts for 55% of the power converter failures. Therefore, the reliability and performance of the power converters greatly depend on these power semiconductor devices. By conducting condition monitoring (CM), it is possible to assess the degradation of power semiconductor switches, which eventually can predict failures before they happen. This failure prediction can prevent unwanted system shutdown due to the failures and can estimate the remaining life of live power converters.

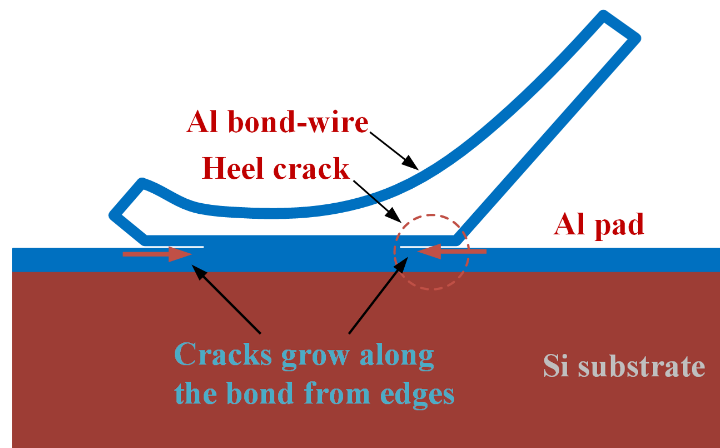
2.1.1 Degradation Mechanism and Effect of Aging on Measurable Parameters

Two types of failure mechanisms typically exist in power semiconductor switches. They are (1) chip-related failure and (2) package-related failure. Chip related failures are caused by electrical overstresses (EOS), electrostatic discharge (ESD), latch-up and triggering of parasitic, hot carrier injection, electromigration, aluminum bond pad reconstructions, and so on [7], [8]. Chip-related aging involves gate-oxide degradation, which cumulatively shifts the gate-source threshold voltage ($V_{GS(TH)}$), gate leakage current (I_{GSLK}), transconductance or saturation current, or switching turn ON and turn OFF times, etc. [9]–[12]. In addition, trapped charges in the gate oxide layer and Si/SiO_2 interface due to gate oxide degradation cause positive $V_{GS(TH)}$ shift and decrease electron mobility, leading to the increase in the device ON-state channel resistance ($R_{DS(ON)}$) [88]. Moreover, aluminum bond pad reconstruction and metallization cause chip degradation, which eventually increases the $R_{DS(ON)}$. The increase in

$V_{GS(TH)}$ also increases the equivalent series resistance (ESR_{GS}) leading to an increase in the gate-source capacitor impedance ($Z_{eq,GS}$) [13], [14]. Although chip related degradation causes ultimate device failure, package related failure mechanisms are most frequently observed in power devices [7]. The main driving forces acting on package related degradation are the mismatches in the coefficient of thermal expansion (CTE) between different materials in the chips and packages. These mismatches lead to mechanical stress throughout the packaged device under temperature swing through regular power and thermal cycling. As shown in Fig. 2.2, owing to this CTE mismatch, cracks, and voids in the die-attach layer between Si and Cu



(a)



(b)

Figure 2.2 (a) Formation of cracks and voids in a power MOSFET due to aging and (b) wire bonding failure [7].

die, and the bond wire and chip interface are formed, resulting in the bond wire lift-off and soldier fatigue [7], [8], [89], [90]. Reduced number of bond-wires, cracks, and voids will impede the heat dissipation throughout the device, and thus thermal impedance (Z_{th}), as well as junction temperature (T_j), will increase which can be determined by the increase in the device on-state channel resistance ($R_{DS(ON)}$) and on-state collector-emitter voltage ($V_{CE(ON)}$) [7], [8], [15]–[17], [89].

2.1.2 Existing Aging Measurement Techniques and Their Limitations

According to recent literature studies, measuring the failure precursors of the power devices, analyzing the model of the degradation process and using system identification are explored to continuously monitor the condition of the power converters. In [20], [21], [24]–[26], $V_{CE(ON)}$ and/or $R_{DS(ON)}$ measurements have been carried out to perform device health monitoring. Although these precursors ($V_{CE(ON)}$ and $R_{DS(ON)}$) can be measured using specially designed sensors, changes in these quantities are significantly small relative to their OFF-state counterparts, and these sensors often need electrical isolation to block the high DC-link voltage. Therefore, the direct measurement of these parameters is not practical and cost-effective for many high voltage applications and could result in low-resolution measurements. It is of paramount interest to detect and track the variation of $V_{CE(ON)}$ and/or $R_{DS(ON)}$ without introducing additional sensors or circuitry. Thermal resistance and junction temperature-based CM technique [22], [28] can detect solder fatigue inside the packaging of a power module, however, direct measurement of junction temperature is impractical and can only be applied during the idle state of the converter. Switching transients such as turn-ON and turn-OFF time-based health monitoring methods proposed in [23] and [27] respectively, can characterize device failure mechanisms along with gate driver circuit degradation. However, the direct

measurement of switching transients, often in the range of tens of nanoseconds, requires a very high bandwidth and noise immune transient detection circuit with a high-resolution sensor. Recently, other CM methods for gate degradation detection based on Miler Plateau gate voltage [33] and gate leakage current ($I_{GS\mathrm{LK}}$) measurement [12] have been proposed. Like the direct measurement of switching transients, a high-resolution detection circuit with high bandwidth is needed for the above-mentioned gate-signal-based CM methods [12], [33], which is very difficult to implement due to the compromise needed between the measurement resolution and signal bandwidth. Moreover, the instrumentation amplifier must withstand a large common-mode voltage and is required to offer a very high common-mode rejection ratio (CMRR) even at a very high switching frequency. Although switching transient and gate-signal-based CM methods can be integrated into the gate-drivers to make them intelligent, the above-mentioned drawbacks along with their ability to only detect gate degradation inhibit their wide range of applications. All of these methods need external sensors to collect aging precursor data that require the use of additional probes, complex hardware as well as digital controllers, which may not be cost-effective. Therefore, CM techniques without using internal sensors are indeed highly desirable. System-identification-based CM technique can be implemented without any additional sensors other than those required for the operation of the converter and with minimal additional digital hardware [29], [30]. However, this technique requires an advanced signal processing algorithm which increases the computation burden. Moreover, derivation of precursor information from external measurements requires establishing an accurate relationship between the device condition and the measurable system performance, otherwise, the variable operating condition of a converter system may produce false results. The data-driven or model-based CM approach proposed in [31], [32], is based on

the comparisons of estimated and measured variables that require a large number of training data, and they also have a poor estimation of specific variables in different operating conditions.

In order to overcome these limitations of real-time power converter health monitoring techniques, spread spectrum time domain reflectometry (SSTDR) based aging detection techniques have been proposed in [40]–[44] because of its low voltage characteristics, very high signal to noise ratio, and the ability to perform in both the low-frequency and high-frequency environment. Previous SSTDR based CM methods were only able to detect device degradation while the converter operates in an idle state (constant input at the gate), therefore the technique cannot be implemented in live power converter applications (PWM switching). Moreover, these methods required SSTDR test signals to be applied across the drain-source terminals of a power MOSFET or collector-emitter terminals of an IGBT with the help of external SSTDR hardware, which could be unsuitable in high voltage circuits. As described in Chapter 4, all these limitations can be overcome by adopting either of the two schemes: (i) incorporating advanced statistical analysis in SSTDR data interpretation, and (b) synchronizing the SSTDR test signal (SMPNS) with the PWM gate signal (across the gate-source interface) as well as modifying the switching scheme with better flexibility. Most importantly, CM from the gate-source interface allows us to monitor the high voltage converter easier and safer than it was in the past. This feature also helps in designing the SSTDR hardware for significantly lower ratings since the gate terminal is always at a lower potential compared to the drain/collector. Last but not least, due to the ability to synchronize the SMPNS code with the PWM gate signal, the proposed technique can be integrated with the gate driver module, thus making it intelligent. No similar technology involving gate driver with built-in

SOH/CM module presently exists and chapter 3 described the detailed features of this proposed intelligent gate-driver architecture.

2.2 PV Ground Fault Detection

According to the International Energy Agency (IEA), the world's total renewable energy-based power capacity is expected to increase by 50% between 2019 and 2024. This is an increase of 1,200 GWs, equivalent to the current total power capacity of the United States. Of that global total power capacity, 60% is expected to come from solar/photovoltaic (PV) energy, the fastest-growing source of renewable energy in nearly every country around the world [91]. PV energy's popularity stems from the lower costs for installation and operation of PV systems and its ability to replace conventional finite energies that are harmful due to carbon emissions into our ever-warming atmosphere. Despite the attractiveness of the PV technology, PV systems can experience faults that often go unnoticed and can cause catastrophic failure in the power system. These faults decrease electrical power output as well as degrade module properties [92]. Based on their locations, three types of failures in PV systems are studied in power electronics: faults on PV arrays [53], [77], [78], [93], failures in power conditioning systems [94], [95], and disturbances in the utility interconnections (such as islanding, and so on) [96], [97]. However, recent fire events initiated by the catastrophic failures in PV arrays have been drawing the attention of researchers toward this area [98], [99]. Among all possible major faults that happen in the PV arrays such as ground faults, line-to-line faults, arc faults, hot-spot formation, and open circuit faults, ground faults are considered to be the most common faults in PV systems and are reported to be one of the major reasons behind catastrophic failures resulting in electrical fires and shock hazard [53], [58], [59].

2.2.1 Reasons for PV Ground Faults

The ground fault is the undesirable condition of current flowing through the unintentional low resistance path between a current-carrying conductor (CCC) and an equipment grounding conductor (EGC)/earth. In addition to CCCs, a PV array has several non-current-carrying conductors (NCCCs) such as module frames, mounting racks, metal enclosures, distribution panels, the chassis of end-use appliances, and power converters [55]. No current flows through these paths under normal operating conditions, but a nonzero current exists in any path during faults. All these NCCCs are connected through the EGC, and the use of EGC is mandated by National Electrical Code (NEC) 690.43 regardless of the nominal voltage of the PV system in order to protect people and other living animals from being electrocuted [54]–[56]. There are several potential reasons for ground faults such as (a) cable insulation damage during the installation due to aging, chewing done by rodents, water leakage, and corrosion, etc., (b) ground fault within the PV modules caused by degraded sealant, oxygen and water vapor penetration into the module, and (c) accidental short circuit inside the PV combiner box, often at the time of installation [55], [56], [74].

2.2.2 Standard Ground Fault Protection Devices and Their Limitations

PV array installations can be divided into two categories: grounded and ungrounded [55], [56]. In grounded systems, at least, one of the CCCs needs to be connected to the EGC using a ground-fault detection and interrupter (GFDI) fuse in order to detect the presence of any accidental circulating current path, and this is termed as system grounding. PV systems with system grounding are known as grounded, and this category is prevalent in the U.S.; an example of this grounding-type is illustrated in Fig. 2.3. However, there are alternative ground-fault protection schemes, which are more common outside the U.S. including residual current

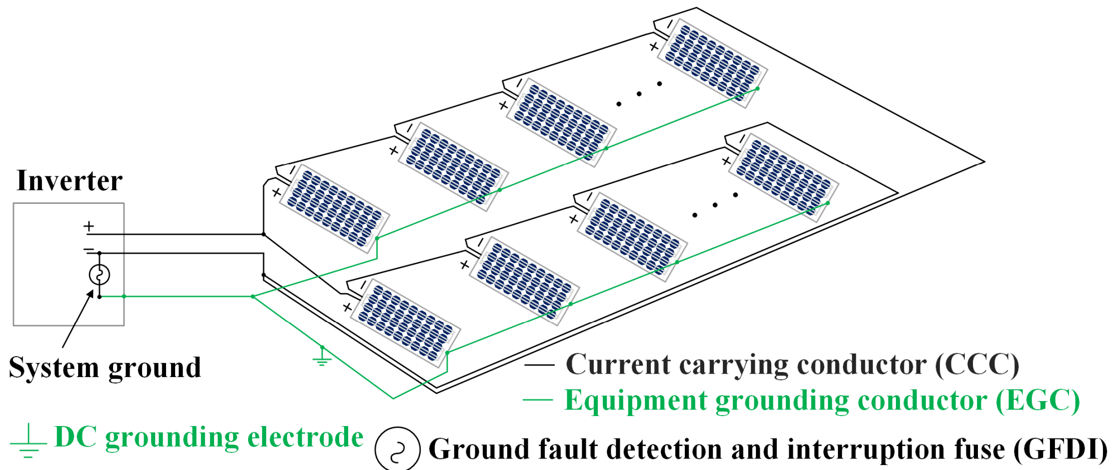


Figure 2.3 Typical grounding diagram of PV arrays. The GFDI fuse (system ground) is usually installed inside the PV inverter in a grounded PV array, and system grounding is absent in an ungrounded PV array [53].

monitoring devices (RCD) and dc insulation resistance (Riso) measurements [51], [53]. These ground-fault protection systems often are used on ungrounded (floating) PV systems that do not have a connection between a CCC and ground.

In general, ground fault detection devices are based on passive fuses, isolation impedance measurements, or differential current measurement methods, and these ground-fault protection devices suffer from several limitations [53], [57]. For instance, a ground fault may remain undetected when the fault current falls within the blind spot range because of the low irradiance and high fault impedances [53], [57]–[59]. This phenomenon is known as the blind spot of the detection device, i.e., when the fault current magnitude is less than the tripping/melting current of this device preset. Recent fire events on April 5, 2009, in Bakersfield, CA, USA, and April 16, 2011, in Mount Holly, NC, USA, resulted from undetected ground faults within the blind spot range [98], [99]. In both of these fire events, a double ground fault occurred. The first ground fault occurred between the negative CCC and

EGC and resulted in current flow through the GFDI fuse, although the current magnitude was below the rated current of the installed fuse, and this fault remained undetected for an indefinite amount of time. The second ground fault within the same array resulted in a flow of 952A of current through the EGC and ignited fire before the fault current was cleared by the overcurrent protection fuse. Leakage current in the system may lead to the blind spot of the detection device. Sufficient leakage current may flow through the system if it is designed poorly, especially during the presence of high relative humidity [100]. This leakage current may flow in the opposite direction of the ground fault current resulting in the reduced magnitude of the current through the GFDI and IMD devices which may remain undetected [58], [98]. Additionally, RCDs may be affected by external electrical noise resulting in nuisance tripping of the system [101].

2.2.3 Existing Ground Fault Detection Techniques and Their Limitations

Apart from ground-fault detection devices, several ground fault detection and mitigation techniques have been proposed in recent years that are based on comparisons of estimated and measured variables, pattern recognition using signal processing, machine learning analysis, and so on. Platon *et al.* proposed an online fault detection method based on the differences between measured and estimated ac power output from a modeled PV system [60]. A "fractional-order color relation classification" based fault detection method has been introduced in [61] where a fractional-order dynamic error (FODE) is calculated to measure the power degradation caused by the fault. In [62], a "descriptive and inferential statistic" has been conducted on the population of the energy generated from the PV inverters equipped with each PV subarray to identify the faulty part of the plant. A wireless sensor-based fault detection technique, which detects fault by comparing expected values with measured values of

operating voltages and currents of PV panels, is introduced in [63], [64]. A fault diagnosis technique for the PV panel is presented in [65], where several intrinsic parameters are estimated based on modified particle swarm optimization (MPSO) by sampling the dynamic panel voltage and current. The fault in the panel can be detected if there is any change in the estimated parameters from their initial values. Saleh *et al.* presented a fault detection method, based on the magnitudes and wave-shape characteristics of voltage signals of the PV modules, which needs two voltage transducers in each string [66]. All of these methods are computation-intensive and need external sensors to collect the data. Moreover, machine-learning techniques based on prerecorded and on-site data have been proposed in [67], [68] and require a large amount of training data along with external sensors. Again, both the machine-learning-based and comparison-based fault detection techniques need accurate PV models to estimate circuit parameters. However, the models designed for specific environmental conditions are not capable of simulating the characteristics of the PV performance under different environmental conditions, and thus, may result in false detection in these cases [67]–[71]. Therefore, these models have to be configured properly to get the correct estimated values. Yi and Etemadi [72] presented a pattern-recognition-based fault detection method that utilizes fuzzy inference systems (FIS) to detect the faults with the help of extracted necessary signal features from a multiresolution signal decomposition (MSD) technique. Though this method uses fewer sensors compared to the machine learning methods, it needs a series of filters that make the system more expensive. The authors of [73] utilized the difference in voltages between the healthy module in the faulty string and the module in the healthy string to locate the faulty module. This computation-intensive method needs to update the software programs of the existing commercial converters with additional voltage sensors. Wang *et al.* proposed a high-

impedance ground-fault (HIGF) detection scheme of PV arrays using the common-mode (CM) current spectrums of the CM model of the full-bridge inverter [69]. This model-based fault detection technique needs to be updated for different configurations of PV arrays and experiences difficulties in determining the stray and parasitic parameters.

Most of these existing ground fault detection techniques require several on-site parameters such as voltage, current, generated power, irradiance level, temperature, humidity, etc., for accurate fault detection. Changes in any of these parameters may affect the I–V characteristics/MPPT of the PV panel making the fault detection techniques more challenging especially for those methods that rely on the I–V characteristics of the PV module [53], [74]–[81]. Therefore, a method that does not use traditional on-site parameters and sensors to detect faults is highly desirable to overcome these limitations in PV array fault detection techniques. SSTDR based fault detection method could be an excellent candidate to overcome such limitations since it only relies on the fault-related impedance variations rather than the traditional on-site parameters and sensors.

2.3 Detection of Degraded Cell in a Li-ion Battery Pack

Electric vehicles (EVs) and hybrid EVs (HEVs) as well as the battery energy storage of renewable energy generations (such as wind and solar PV plants) use a large number of Li-ion cells connected in series and parallel to meet their stringent power and energy requirements [84]. The Li-ion battery packs usually constitute the single largest cost (81% of the total powertrain cost) of the entire vehicle [102], and thus prolonging the battery life is crucial to saving the maintenance costs.

2.3.1 Origin of Cell-level Degradation in a Li-ion Battery Pack

Like other battery chemistries, Li-ion batteries suffer from performance degradation over time. Because of the inconsistency in the manufacturing process or non-uniform operating conditions, the initial SOH of one or more cells is different [85]. Uneven SOH at the cell level leads to the existence of different resistance paths and temperature gradients that will create an uneven current distribution in the system. These factors can accelerate further degradation in the cells in a cascading manner, and eventually, the entire battery pack loses capacity, becomes unreliable, and even may lead to catastrophic failure [85], [103]. Therefore, the location information of individual cells along with their aging level in a large Li-ion battery pack is indispensable since it can help us to estimate the SOH of the entire battery pack and thus predicting its remaining useful lifetime (RUL).

2.3.2 Limitations of Existing Li-ion SOH Estimation Methods

The capacity and internal impedance are considered to be the two main precursors of the SOH of a battery [84], [104]. An aged battery experiences loss in capacity and an increase in internal impedance. For instance, the automotive manufacturers consider the end of life (EOL) of a lithium-ion battery if the capacity degrades by 10%-20% of its nominal capacity, or if the internal impedance increases by 160 % of its initial value at the same SOC and operating temperature [104]. A considerable number of methods on battery SOH monitoring and prognosis based on characterizing these two precursors have been reported that measure the traditional parameters such as load current, terminal voltage, surface temperature and so on. These methods can be roughly divided into five groups: namely offline open-loop direct methods [105], state-observer methods [106], signal processing methods [107], model-based [108] and data-driven based regression methods [109]. Open-loop direct methods suffer from

poor accuracy since the load profile and environmental conditions rarely follow the aging test dataset from which the SOH estimation model is derived. Again, state-observer methods require a huge computational task that makes them unsuitable for on-board SOH estimation. Similarly, signal processing techniques are not suitable for online SOH monitoring in real application since they require batteries must be charged or discharged with a constant current. Lastly, the model-based and data-driven based regression methods estimate the battery SOH using statistical learning methods that require the historical data, and the SOH prediction accuracy greatly suffers from the quantity and quality of the selected training dataset. However, none of these battery health monitoring and prognosis methods can monitor the SOH at the cell level and thus identify the location of the degraded cell in a large battery pack.

CHAPTER 3

3 FUNDAMENTALS OF SPREAD SPECTRUM TIME DOMAIN REFLECTOMETRY (SSTDR): A NEW METHOD FOR TESTING ELECTRONICS LIVE

3.1 Basic Concepts of Reflectometry

Reflectometry is a well-known technique in electromagnetics, and it has been successfully used for detecting and locating faults in transmission lines and aircraft wirings [34]–[39]. Reflectometry is based on the reflection of an electrical signal at any impedance discontinuity in a transmission line. As illustrated in Fig. 3.1, any incident signal (V_0^+, I_0^+) is sent down the line and a portion of the signal (V_0^-, I_0^-) is reflected back if it finds any impedance mismatch from the characteristic impedance (Z_0) of the line. Characteristic impedance, Z_0, is defined as the ratio between the voltage and current of the incident or the reflected wave as follows:

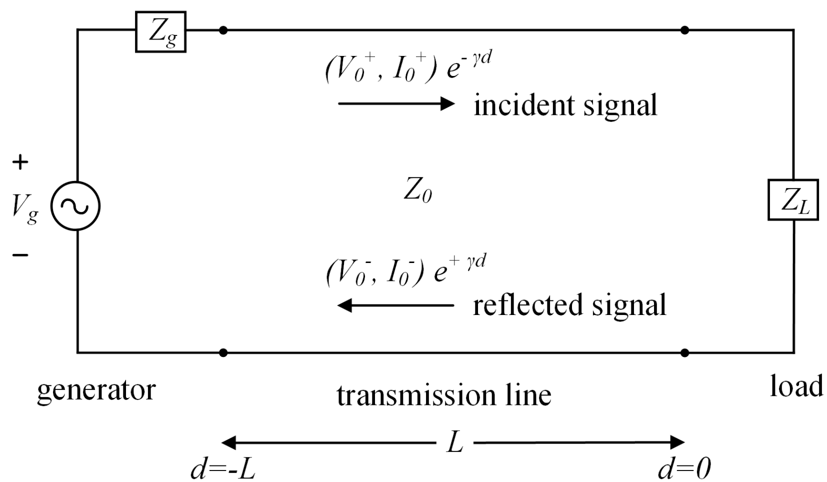


Figure 3.1 Schematic diagram of a transmission line of length L and characteristic impedance equal to Z_0. A generator circuit is connected at one end (d=-L), and other end (d=-0) is connected to load Z_L.

$$Z_0 = \sqrt{\frac{R' + jwL'}{G' + jwC'}} = \frac{V_0^+}{I_0^+} = \frac{V_0^-}{I_0^-} \tag{3.1}$$

Here, R' (Ω/m), L' (H/m), G' (S/m), and C' (F/m) are per unit length resistance, inductance, conductance, and capacitance of the transmission line, respectively. The ratio between the reflected and incident voltage signals is known as the reflection coefficient (ρ), which is a measurement of how much signal is reflected back [defined in (3.2)]:

$$\rho = \frac{V_0^-}{V_0^+} = \frac{Z_\mathrm{L} - Z_0}{Z_\mathrm{L} + Z_0} \tag{3.2}$$

Here, Z_0 is the characteristic impedance and Z_L is the impedance at the point of impedance discontinuity (impedance of the load/device under test, fault, etc.).

3.2 SSTDR Operation

Based on the incident signal used in the field, several reflectometry-based fault detection methods exist. Among them, spread spectrum time domain reflectometry (SSTDR) uses a sine modulated pseudo-noise sequence (SMPNS) as the incident signal which is generated by modulating a pseudo-noise code (PN code) with a high-frequency carrier sine wave. PN code consists of randomly generated 1s and 0s where each 1/0 is known as a chip [34]–[38]. The frequency of the carrier sine wave is also known as the center frequency of SSTDR. To calibrate the system without any difficulties, the frequency of the carrier sine wave is maintained the same as the chip rate (f_C=1/T_C) of the PN code [37], [38]. The chip rate of the PN code is defined as the number of chips generated each second, and the length of the PN code is defined as the number of chips after the sequence is repeated. SSTDR can be implemented in several ways as discussed in [37], [38], [110], [111], and a simple schematic diagram is shown in Fig. 3.2.

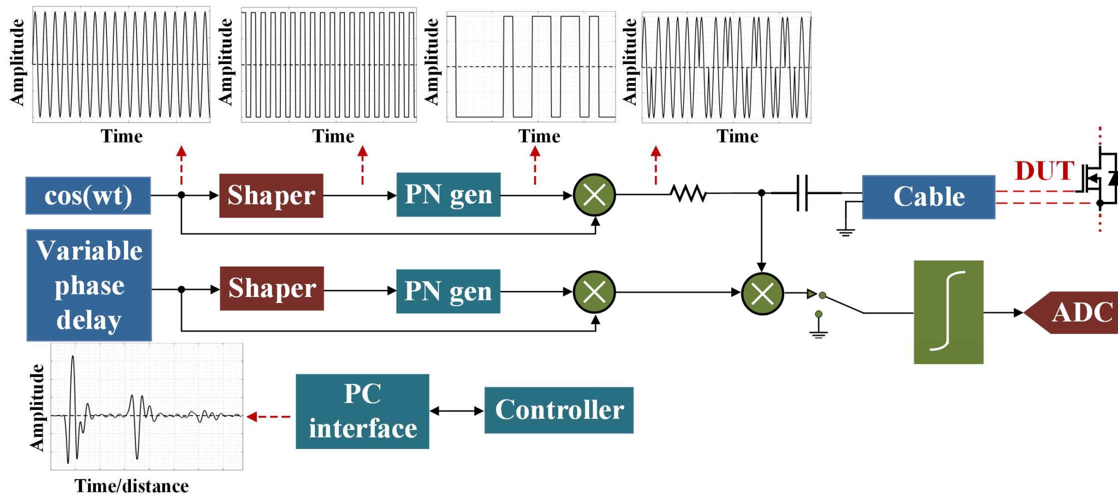
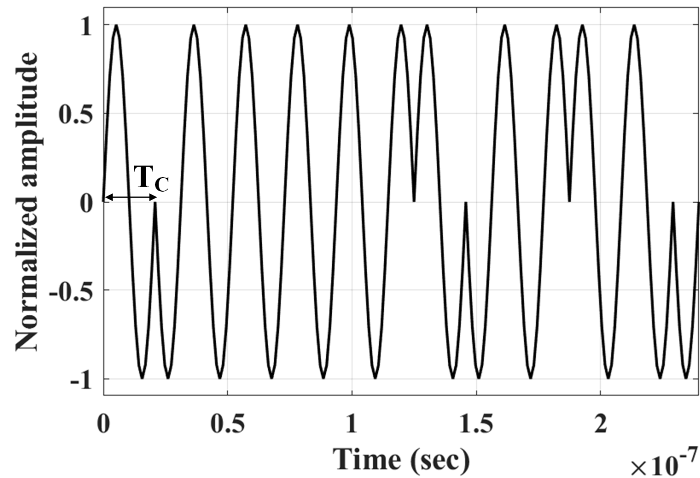
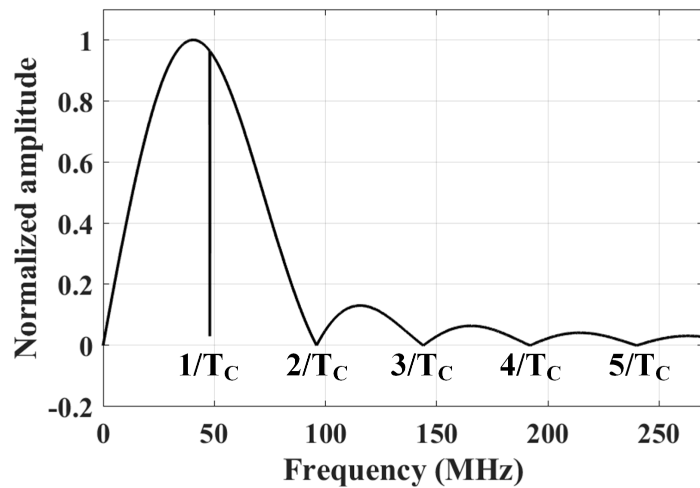


Figure 3.2 Schematic diagram of the SSTDR mechanism [36].

As shown in Fig. 3.2, a sine wave generator is used as a master system clock, and this generator's output is converted to a square wave via a shaper, and the resulting square wave drives a PN sequence generator (PN gen). The output of the PN generator is multiplied with the initial sine wave, generating the SMPNS which is basically a direct sequence spread spectrum (DSSS) binary phase shift keyed (BPSK) signal. This SMPNS is sent down the wire, and the signal is reflected back if it finds any impedance discontinuity against the characteristic impedance of the propagation path. This reflected signal is cross-correlated with the delayed copies of the incident signal with the help of a variable phase delay, and a lobe is generated at a time delay in the autocorrelation plot that corresponds to the distance from the source terminal to the impedance mismatch at the load terminal. A lobe with a positive peak indicates a positive reflection coefficient ($\rho > 0$, if $Z_L > Z_0$) and a negative peak indicates a negative reflection coefficient ($\rho < 0$, if $Z_L < Z_0$).



(a)



(b)

Figure 3.3 Incident signal of SSTDR with carrier/center frequency equal to 48 MHz: (a) time-domain representation (a portion of one entire SSTDR sequence is shown here), and (b) frequency-domain (FFT) representation (only the upper side band is shown here).

An example of the SSTDR generated incident signal and the corresponding fast Fourier transformation (FFT) is shown in Fig. 3.3. The FFT of the PN code is similar to a "sinc" function where the width of the main lobe is twice the chip rate of the PN code. The Fourier transform of the incident signal is similar to a double sideband suppressed carrier signal where the signal has a large spectral distribution since the sinusoidal signal has been used as the

modulating signal here. From Fig. 3.3 (b), it is evident that the main lobe shifts further away from 0 Hz once the carrier frequency increases. Since the power in the noise is usually centered around 0 Hz, increasing the carrier frequency of the SSTDR signal will lead to producing less power in the cross-correlation of an SSTDR signal with noise, which will eventually increase the signal-to-noise ratio (SNR) of the system. Therefore, among various reflectometry methods, SSTDR shows the best signal to noise ratio. This ability, in particular, is critical to detect impedance discontinuities due to faults or changes in the device aging levels when the converter is live. In addition, SSTDR sends down a significantly lower amplitude signal (usually around or below 100 mV and lowest could be 22 mV) that can be placed on top of the existing signals (digital, analog, high-frequency PWM, etc.) at a level much below the noise margin and yet still being able to detect and analyze the SSTDR reflected response [46]. Having the best SNR along with its low voltage characteristics leads to its excellent performance in the live circuit among other reflectometry methods. An example field-programmable-gate-array (FPGA)-based SSTDR evaluation kit W50A0071, which is an R&D product from Livewire Innovation, has been shown in Fig. 3.4. This hardware works in two modes: (i) static and (ii) intermittent. In static mode, it requires external triggering for initializing each scan meaning it scans just for once after the trigger initialization. In contrast, intermittent tests scan the system continuously to detect short duration impedance change in the SSTDR signal propagation path. The time taken to create and log the autocorrelation data for each scan is approximately 4ms which is supposed to be equal to the total time of response, processing, and post-processing.

Any change in the aging level in a DUT or fault in the system yields impedance discontinuity in the SSTDR propagation path. This implies that the impedance of the SSTDR

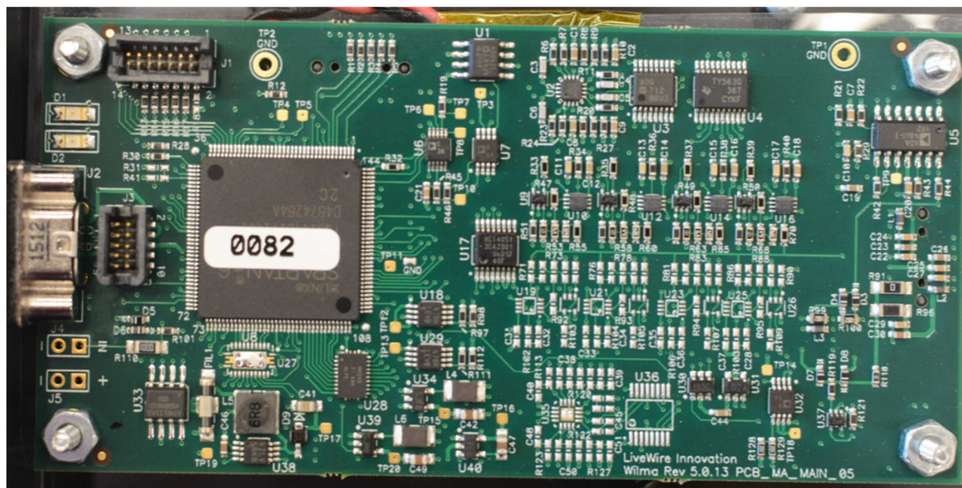
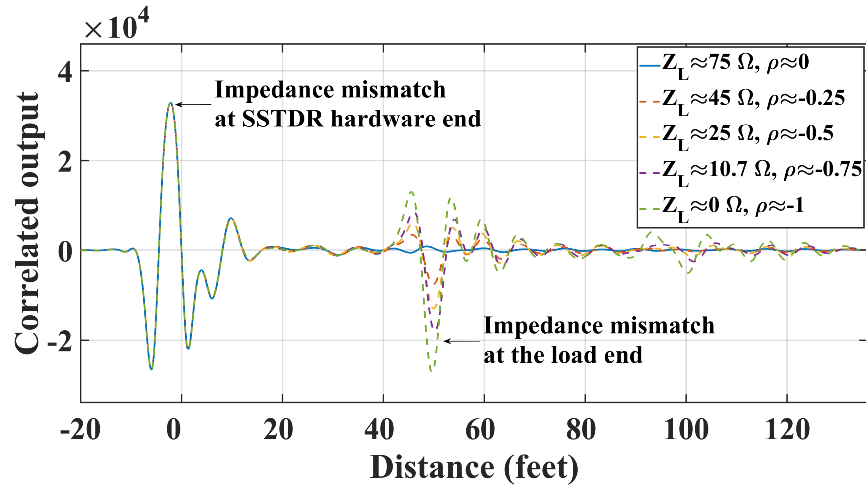


Figure 3.4 Photograph of the FPGA-based SSTDR hardware (an R&D product from Livewire Innovation).

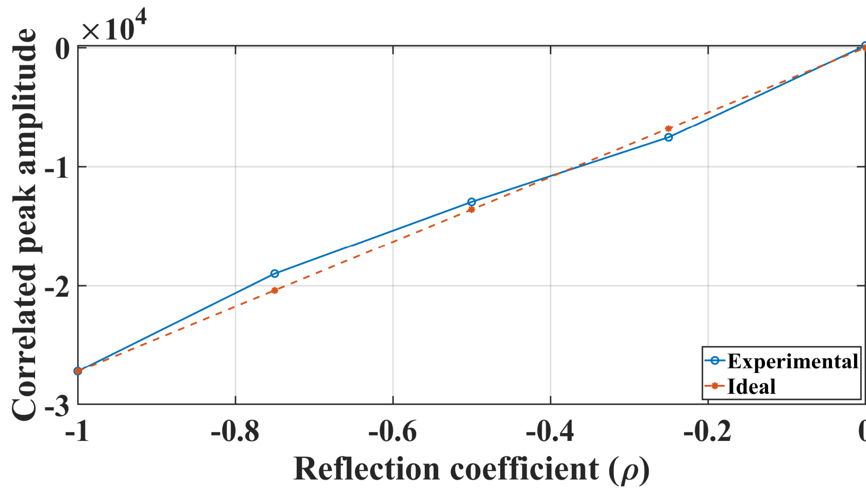
propagation path will be different for any aging or faults in the system from its healthy counterpart. This impedance discontinuity can be characterized by the corresponding change in the SSTDR auto-correlation signature. For example, each type of device degradation leads to various impedance changes of the failure precursor parameters such as $R_{DS(ON)}$, $Z_{eq,GS}$ inside a power device which will change the impedance of the SSTDR propagation path. Similarly, age-related impedance variations in a Li-ion cell inside a battery pack will change the impedance of the SSTDR propagation path as well. In the same vein, a healthy PV array has a specific impedance between node pairs, and any ground fault changes the impedance values which can be characterized by SSTDR. Section 3.3 discusses the influence of the failure precursor parameters on SSTDR due to device aging.

3.3 Influence of the Failure Precursor Parameters on SSTDR Due to Device Aging

From (3.2), it is evident that the reflection coefficient is negative ($\rho < 0$) for $Z_L < Z_0$ and positive ($\rho > 0$) for $Z_L > Z_0$. Fig. 3.5 (a) shows the different correlation curves that have been generated while applying 48 MHz SSTDR signal passing through a 50 feet RG-6/U



(a)



(b)

Figure 3.5 (a) Variation in correlated amplitudes for the different values of reflection coefficients ($\rho \leq 0$) and load impedances ($Z_L \leq Z_0$) (for 50 feet long, 75 Ω co-axial cable), and (b) variation in the corresponding correlated peak amplitudes for the different values of reflection coefficients ($\rho \leq 0$).

coaxial cable having a characteristic impedance of 75-Ω. The first lobe in the autocorrelation plot is due to the impedance mismatch at the hardware end and the second lobe, considered as the main lobe, is due to the impedance mismatch at the load end. The peak value of the main lobe, coined as "auto-correlated peak amplitude", changes with a change in the reflection coefficient. Fig. 3.5 (b) shows the linear relationship between the auto-correlated peak

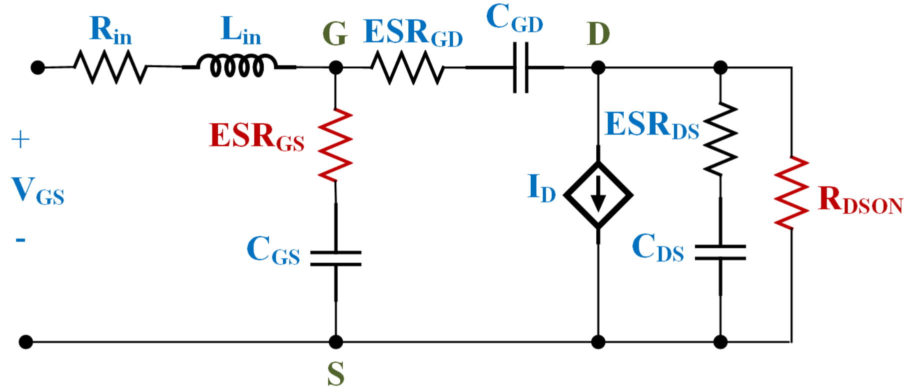


Figure 3.6 Simplified equivalent circuit of a power MOSFET [112].

amplitudes and the corresponding reflection coefficient obtained from Fig. 3.5 (a). From these two plots, it is evident that when $\rho \leq 0$, an increased value in Z_L leads to less negative auto-correlated amplitude (or lower magnitude). Since the $R_{DS(ON)}$ and $Z_{eq,GS}$ of a power semiconductor switch is significantly less than that of the SSTDR test cable and the lumped network of the converter circuit, the auto-correlated peak amplitude will be negative ($\rho < 0$), and the increased $R_{DS(ON)}$ and $Z_{eq,GS}$ due to the aging will lower the magnitudes of the auto-correlated amplitudes. For instance, let us consider the equivalent circuit of a MOSFET shown in Fig. 3.6 [112]. Since $R_{DS(ON)}$ and $Z_{eq,GS}$ will increase with aging, the equivalent impedance of an aged device is higher compared to that of a healthy device seen from the gate-source interface. Let the equivalent impedance for a healthy MOSFET seen from gate and source be $Z_{GS,H}$ and with aging, this impedance is increased to $Z_{GS,A}$, then if the change in these two measurements is denoted by ΔZ_{GS}, we can express this value as shown in (3.3) below:

$$\Delta Z_{GS} = Z_{GS,A} - Z_{GS,H} \tag{3.3}$$

The reflection coefficient, ρ presented in (3.2), will give the impression of this difference in impedance, and a non-zero value of ΔZ_{GS} will illustrate the aging of the device. For instance, Fig. 3.7 shows the various reflections for different aging levels (corresponding

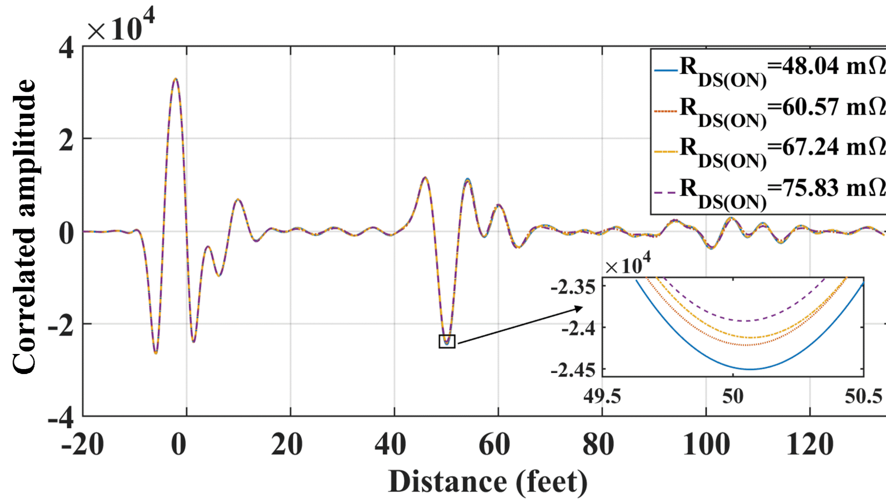


Figure 3.7 Correlated amplitude variation for different aging levels (corresponding to different values of $R_{DS(ON)}$) of a power MOSFET in a buck converter.

to different values of $R_{DS(ON)}$) of the MOSFET in a buck converter, which was obtained applying a 48 MHz SSTDR signal across the gate-source interface. This test was conducted in a static condition meaning no PWM was applied.

3.4 Aging Detection from the Gate-Source Interface: A Platform for Intelligent Gate-Driver Architecture

In previous SSTDR based CM methods, SSTDR test points required to be connected across the collector and emitter terminals of the IGBT or drain and source terminals of a MOSFET, which could be unsuitable in high voltage circuits [40]–[44]. In addition, these methods required a complete shutdown of the converter circuit for testing and therefore was not practical for a live power converter system. According to Section 3.3, it is possible to perform aging detection from the gate-source interface which can easily overcome these limitations in addition to creating a provision for the development of an intelligent gate-driver architecture with an in-built degradation monitoring unit. No similar technology involving a gate driver with a built-in SOH module presently exists, and once completed, the intelligent

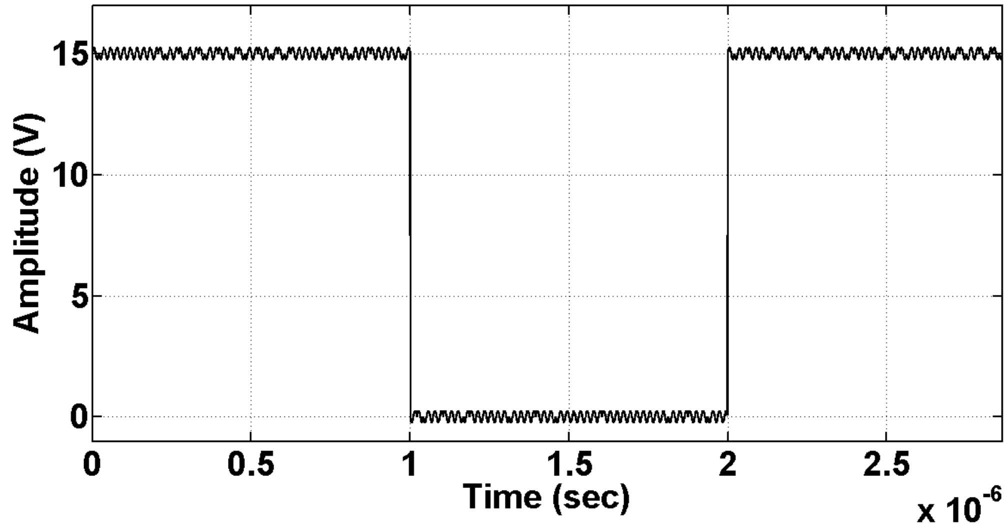


Figure 3.8 A 100 mV (p-p), 48 MHz SSTDR incident signal superimposed on a 15 V, 500 kHz PWM sequence (with a 50% duty cycle).

gate driver circuit can estimate the degradation associated with the IGBT or MOSFET and potentially predict any future failure. While performing aging detection from the gate-source interface, SMPNS is superimposed with the gate PWM signal of a power device and the reflected signals from the age-related impedance discontinuities can be processed to measure the degradation level of the devices. Inside the SSTDR hardware, the SSTDR incident signal (SMPNS) has a typical voltage level of 100 mV or below, and the lowest could be as small as 22 mV. This low amplitude signal with a center frequency of up to 48 MHz embedded in PWM sequence will act as a low-voltage high-frequency noise on top of the 15 V (or 18 V for SiC MOSFETs) PWM gate signal; therefore, it will not impact the normal switching operation of the circuit. A 48 MHz, 100 mV(p-p) SSTDR incident signal superimposed on a 500 kHz, 15 V PWM signal (50 % duty cycle) is shown in Fig. 3.8 for reference. In a nutshell, the proposed SOH embedded gate driver architecture will serve the following purposes:

(i) Unlike the collector/drain terminal, the gate terminal is always accessible and remains at the lower voltage level. This allows us to monitor the high voltage converter easier

and safer than it was in the past and helps in designing the SSTDR hardware at a much lower rating.

(ii) The rapid variation in impedance throughout the entire live converter circuit caused by fast switching makes CM more challenging while using SSTDR. The proposed CM scheme integrated into a gate driver module will allow us to characterize the aging level in a live power device by synchronizing the SSTDR test signal with the PWM gate signal and modifying the switching scheme with better flexibility.

(iii) This proposed feature will allow the system to be monitored autonomously and provide built-in-self–test capability which eliminates the need for separate SOH modules leading to significant system-level savings.

3.4.1 Tentative Implementation Plan of the Intelligent Gate Driver Module

This sub-section will provide a brief overview of the integration feasibility of the SSTDR circuit into a gate driver module. The SSTDR technology is fully compatible with FPGA and/or application-specific integrated circuit (ASIC) integration. We used the FPGA SSTDR evaluation kit W50A0071 in this project which is an R&D product from Livewire Innovation. The working principle of the SSTDR mechanism is already given in Fig. 3.2 of Section 3.2. The digital subsystem of this SSTDR evaluation kit includes the sine-wave oscillator/generator, variable phase delay circuit, shaper, and pseudo-noise (PN) sequence generator. Each component of the digital sub-system can be implemented by FPGA technology. The most common method to generate a sinusoidal signal is to use look-up tables or FPGA manufacturer's free libraries. PN sequences are widely used in communication systems which are often generated by linear feedback shift register (LFSR) with Maximum Length (ML) Feedback Polynomial using FPGA technology [113]–[115]. The output of the

PN generator is mixed/multiplied with the sinusoidal carrier signal and the total signal from the cable (including any digital data or AC signals on the cable, and any reflections observable at the receiver) is fed into an *analog sub-system* namely correlator circuit consisting of control circuitry, multiplier, and an integrator. The received signal and the reference signal are multiplied in the multiplier circuit, and the result is fed to the integrator. The output of the integrator is sampled with an analog-to-digital converter (ADC) and processed in a computer. The multiplier circuit can be implemented by a CMOS mixer such as the well-known Gilbert cell multiplier that includes only two resistive loads and 8 (eight) NMOS transistors [116]–[119].

The architecture and fabrication of a conventional gate drive circuit are way straight forward and could be easily implemented with the use of FPGA and analog components. Depending on the current rating, the driver module comes with an on-board isolated dc-dc converter and level shifter (digital part). The most critical component in a gate driver is the current buffer (analog part) located at the final stage of the circuit to achieve a faster slew rate across the gate and emitter terminals of an IGBT and/or gate and source terminal of a MOSFET. The other blocks are used to achieve various supplementary features.

Please note that the SSTDR hardware used in our experiments is an R&D product developed by Livewire Innovation with the help of FPGA technology aiming at validating the proof of concept and transferring the technology fast enough to the manufacturers for designing an ASIC solution of the SSTDR technology. Using this FPGA-based technique, the digital part of the SSTDR unit along with the gate driver circuit can be designed and implemented inside the FPGA chip. Design and fabrication of the analog part of the SSTDR and the rest of the gate driver circuit can be implemented using discrete components. A conceptual representation of

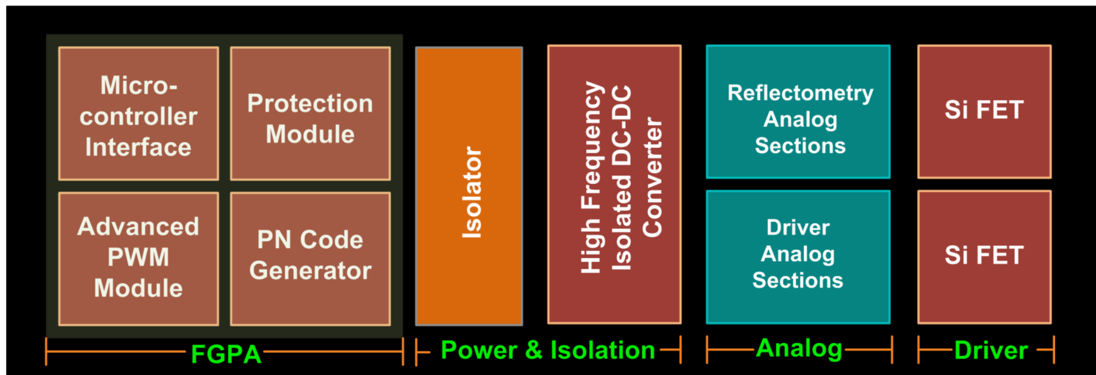


Figure 3.9 Tentative layout of the proposed intelligent gate driver module.

the tentative circuit board layout of the intelligent gate driver module (IGDM) is shown in Fig. 3.9.

There is no denying that ASIC implementation of the proposed intelligent gate driver module is preferred for commercial manufacturing because ASIC chip facilitates small size and lightweight of such instrumentation that allows us to place CM hardware inside a gate driver module with minimal impact. Moreover, ASIC implementation is power efficient and suited for very high-volume mass production compared to FPGA which implies that ASIC chip is very cost-effective. In fact, recently, Livewire Innovation has developed and launched their mixed-signal SSTDR-ASIC technology where the digital and analog sub-system of the SSTDR mechanism except the processor unit (fed by the output of the integrator unit) have been implemented inside ASIC System-on-Chip (SoC). The processing unit can be implemented inside the FPGA or any microcontroller technology. A simplified block diagram of the ASIC integration pathway, coined as "Livewire IC", is shown in Fig. 3.10 [120]. Nowadays, ASIC

Figure 3.10 A simplified block diagram of the SSTDR-ASIC integration pathway, coined as "Livewire IC" [120].

technology is well matured and can easily implement the above-mentioned SSTDR functional blocks. Last but not least, since today's gate drivers are compatible with ASIC technology [121], the SSTDR-ASIC and gate driver-ASIC can easily be integrated into a single SoC and can be treated as intelligent gate driver module with an in-built degradation monitoring unit.

CHAPTER 4

4 ACCELERATED AGING TEST BENCH: DESIGN AND IMPLEMENTATION

To perform degradation detection of power electronic components in a laboratory environment, reference failure tests and reliability data such as test data for devices under tests (DUTs) of known aging levels are necessary [31]. However, under normal and ideal operating conditions of real-life application, these devices are meant to last for millions of cycles before the failure happens. In such situations, it is not feasible to wait for devices to fail under normal operation in order to compute the time to failure. Therefore, accelerated aging tests are widely recognized to accelerate the fatigue process and help to identify the aging precursors in a shorter time [122]. An accelerated aging test is an essential tool in reliability, particularly for products having an expected lifetime is in the order of thousands of hours like power semiconductor devices and batteries [123]. Section 4.1 will discuss the test set-up for accelerated aging of power MOSFETs developed in the Missouri Center for Advanced Power (MCAP) laboratory. An industry-standard accelerated battery cycling test was also performed to induce degradation in Li-ion cells and this process has been illustrated in Section 4.2.

4.1 Active Power Cycling Test Bench for Power MOSFETs

The accelerated aging test is an indispensable technique for investigating the reliability-oriented issues of power semiconductor devices. It can be performed for different purposes such as testing device reliability, studying failure mechanisms, detecting weak links in the device packaging, estimating application-specific lifetime, etc [122]. In this research, accelerated aging was implemented to create a library of test data for DUTs of known aging levels that were used later to perform the CM of power devices in live converter circuits. In

general, the two most common methodologies of accelerated aging tests are adopted in literature: thermal cycling test and power cycling test [5], [122]. These methods aim at inducing chip and package-related degradation in power devices in an accelerated manner. During power cycling tests, devices undergo temperature swing (ΔT) caused by injecting a high current through the device in a controlled periodic manner. This ΔT causes different layers inside the device to expand at different rates because of their different coefficients of thermal expansion (CTE), creating mechanical stress throughout the device [90], [122]. Unlike power cycling, the ΔT in thermal cycling is generated externally by the virtue of a thermal chamber or hot plate [5], [124]. Nevertheless, power cycling tests are considered the standard test for accelerated aging since they are closer to the actual operation of the device including both the conduction and switching [5], [122].

In this research, accelerated power cycling tests were implemented in a custom-designed testbed, which was capable of applying electro-thermal stresses to multiple discrete power MOSFETs simultaneously. The accelerated aging was conducted in two separate phases, and devices aged through these separate phases were used as DUTs in two separate case studies of degradation detection of live power converters discussed in chapter 5. Please note that the method of accelerated aging was similar in both phases where the temperature swing (ΔT) during this electro-thermal process was achieved by injecting a high current through the device in a controlled manner (as shown in Fig. 4.1).

During the ON-time (t_{ON}) of each power cycle, devices were injected with the current until its case temperature (T_C) goes up to its upper limit ($T_{C,max}$) whereas, during the OFF-time

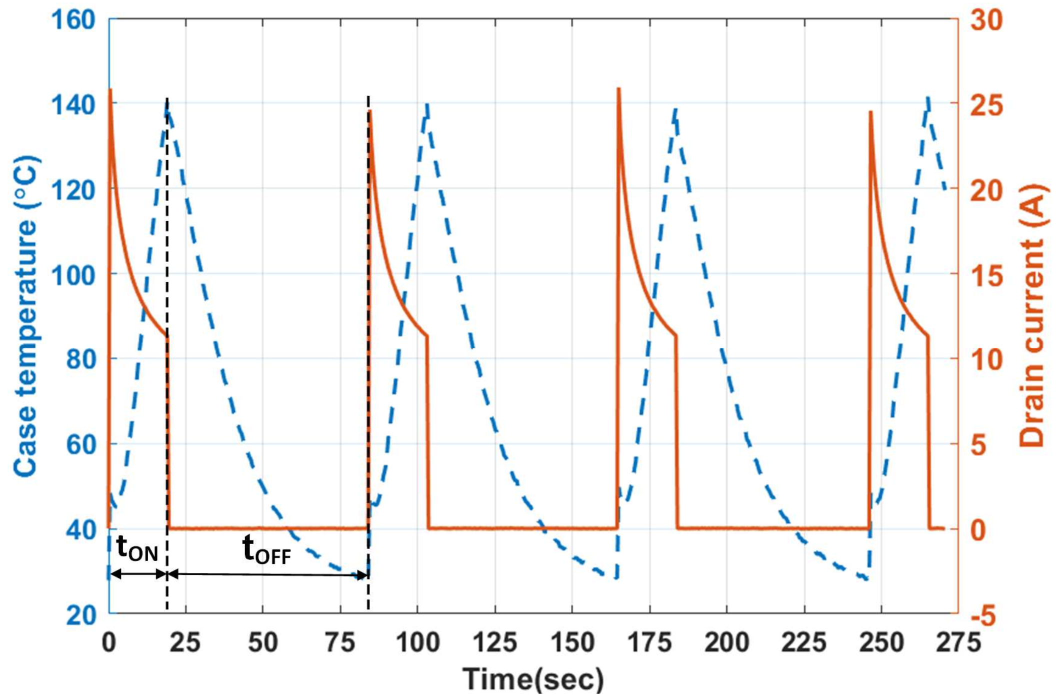
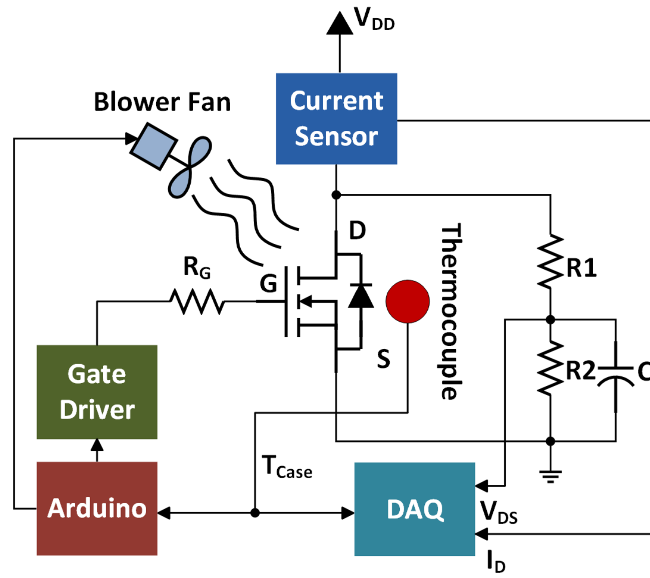


Figure 4.1 Case temperature and drain current swing of the DUT during power cycling test of phase-2.

(t_{OFF}), the devices were allowed to be cooled down until the T_C falls to its lower limit ($T_{C,min}$). The temperature swing (ΔT) between the $T_{C,max}$ and $T_{C,min}$ were maintained constant throughout the aging process for a certain device. Since the power supply voltage was maintained the same during the t_{ON} of the device, the thermal impedance, as well as the $R_{DS(ON)}$ of the device, increased gradually from their initial values once the device's temperature increased from the room temperature, resulting in a gradual decrease in the current from its instantaneous high value. During this test, LabJack T-7 Pro data acquisition system (DAQ) was used to measure and record drain-source voltage (V_{DS}), drain current (I_D) and case temperature (T_C) of each switch. These measurements were taken in order to determine the $R_{DS(ON)}$ of the switches. Case temperature (T_C) was measured using an IR thermocouple from OMEGA. The schematic and the photograph of the aging station are given in Fig. 4.2. Fig. 4.3 shows the thermal image captured during the aging process. A large number of power MOSFETs were aged using this



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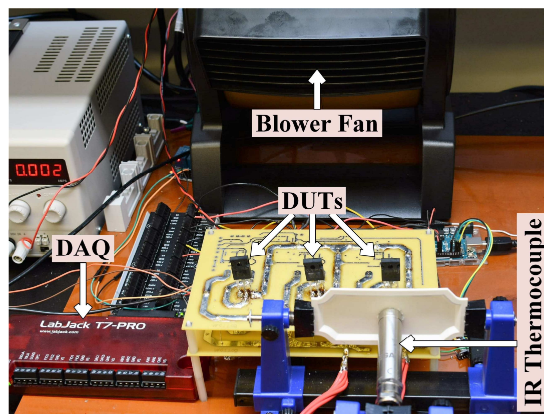

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Figure 4.2 (a) Schematic and (b) photograph of the experimental set-up for accelerated aging test.

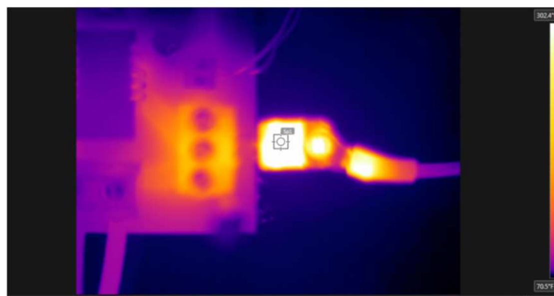


Figure 4.3 Thermal image captured during the aging process.

Table 1 Summary of the accelerated aging parameters

Phase	MOSFET	$T_{C,min}$/ $T_{C,max}$ (°C)	ΔT (°C)	t_{ON}/ t_{OFF} (sec)	N_f	$\Delta R_{DS(ON)}$= MOSFET $R_{DS(ON)}$- Initial $R_{DS(ON)}$ (mΩ)
1	M_{HP1}	-	-	-	-	0
	M_{AP1}	210/230	20	4/20	2844	38.5
2	M_{HP2}	-	-	-	-	0
	M_{AP2_L1}	30/110	80	14/57	5945	7.19
	M_{AP2_L2}	30/140	110	20/65	6000	12.53
	M_{AP2_L3}	30/110	80	14/57	10500	19.20
	M_{AP2_L4}	30/140	110	20/65	12500	27.79

- *M_{HP1}=Healthy MOSFET in phase-1, M_{HP2}=Healthy MOSFET in phase-2*
- *M_{AP1}=Aged MOSFET in phase-1*
- M_{AP2_L1}=*Aged MOSFET with aging level-1 in phase-2*
- M_{AP2_L2}=*Aged MOSFET with aging level-2 in phase-2*
- M_{AP2_L3}=*Aged MOSFET with aging level-3 in phase-2*
- M_{AP2_L4}=*Aged MOSFET with aging level-4 in phase-2*
- *Initial $R_{DS(ON)}$ of M_{HP1} is 70.4 mΩ and M_{HP2} is 48.04 mΩ*

accelerated aging station and the aging parameters such as the applied ΔT, number of power cycles (N_f), $T_{C,min}$, $T_{C,max}$, t_{ON}, t_{OFF}, and the resultant increase in the $R_{DS(ON)}$ ($\Delta R_{DS(ON)}$) of some of these devices are summarized in Table 1. A detailed description of the two phases of the aging process is given below:

Phase-1: A 300V-40A rated N-channel Si power MOSFET (HiPerFET™ power MOSFET in a TO-247 package) was electro-thermally aged with a temperature gradient (ΔT) of 20°C where $T_{C,max}$ and $T_{C,min}$ thresholds were maintained at 230°C and 210°C, respectively. The t_{ON} and t_{OFF} times were recorded as 4 sec and 20 sec, respectively. In addition, when the aging process started, the drain current was recorded as 12.8 A at $T_{C,min}$ and 9.2 A at $T_{C,max}$.

After 2844 power cycles, the $R_{DS(ON)}$ of the DUT changed from 70.4 mΩ to 108.9 mΩ ($\Delta R_{DS(ON)}$= 38.5 mΩ). This higher value of $R_{DS(ON)}$ is a clear indication of the device's aging, and this aged device was used as the DUT for CM of a single-phase H-bridge grid-tied PV inverter described in Section-5.1 of Chapter 5 (case study 1).

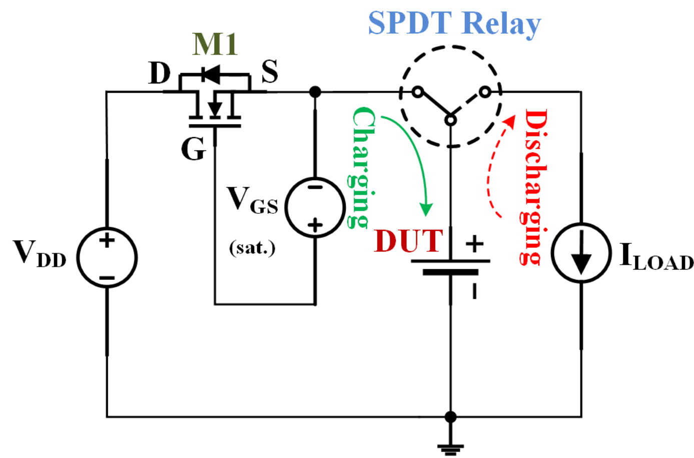
Phase-2: In this phase, multiple N-channel Si MOSFETs were electro-thermally aged with similar ratings (600 V, 50 A, MDmesh™ DM2 power MOSFET in a TO-247 package). For instance, as shown in Fig. 4.1, the MOSFET with aging level-2 (M_{AP2_L2}) was power cycled with ΔT of 110°C where $T_{C,max}$ and $T_{C,min}$ were maintained at 140°C and 30°C, respectively. Initially, during a given cycle, the drain current was recorded as 25 A at $T_{C,min}$ whereas it was measured as 11.3 A at $T_{C,max}$. The dissipated power was recorded to be ~20.39 W in each cycle. The aging process was continued for 6,000 cycles, and it was found that the change in $R_{DS(ON)}$ was 12.53 mΩ. In phase 2, when the switch was turned OFF, a cooling fan (axial fan) was activated to expedite the cooling process. The devices aged in this phase were used as the DUTs in CM of live DC-DC converters and three-phase inverters described in Section 5.2 (case study 2).

The majority of the studies concerning the reliability of power MOSFET identify increased $R_{DS(ON)}$ as a precursor of aging due to active power cycling [30], [88], [125]. Therefore, $R_{DS(ON)}$ increment will refer to the severity of device degradation throughout this paper, although the direct relationship between device aging level and $R_{DS(ON)}$ is still unknown [8], [16].

4.2 Accelerated Battery Cycling Test Bench for Li-ion Cells

A battery cycling test was performed at ambient temperature. The charging current was maintained constant by operating a power MOSFET in the saturation region whereas a constant

current load was used for constant discharging current. To be specific, the accelerated aging was carried out by charging the battery at 2 C-rate (5 A) until the voltage reaches the cell upper voltage limit of 4.2 V while discharging was carried out at a rate of 8 C (20 A) until the voltage drops to a cut-off voltage of 2.5 V. A high current automotive relay was controlled to switch between the charging and the discharging cycle. The temperature was maintained constant using the Delta 9064 temperature chamber. The schematic diagram and the photograph of the Li-ion battery aging station used in this experiment have been shown in Fig. 4.4, and the battery



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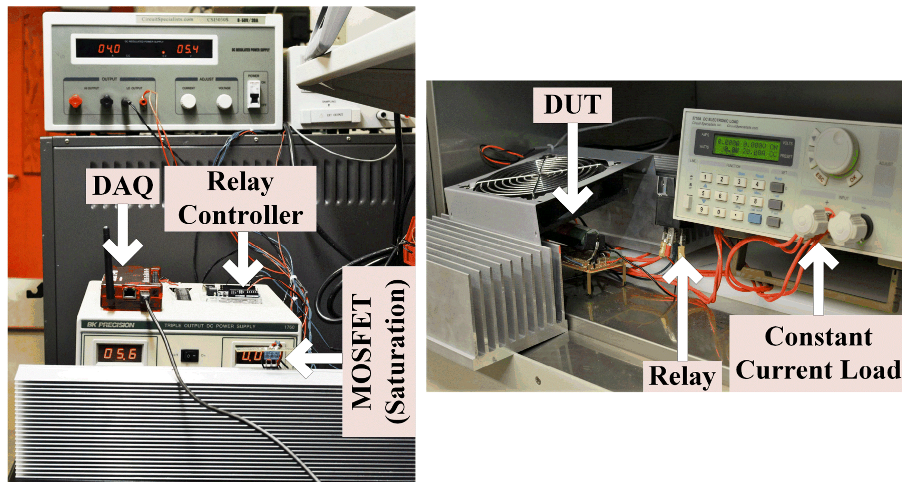


(b)

Figure 4.4 Battery aging station, (a) schematic and (b) photograph.

parameters are shown in Table 2. The battery slowly fades in capacity with cycle number, as shown in Fig. 4.5. The cycling test was continued for 336 cycles, and we observed 7.195% reduction in the capacity of the battery at the same SOC and operating temperature.

Table 2 Battery parameters (Samsung INR 18650-25R)

Parameters	Value
Nominal capacity	2500 mAh
Nominal voltage	3.6 V
Low cut off voltage	2.5 V
Upper limited voltage	4.2 V
Max. charge current	5.0 A
Max. discharge current	20 A
Initial internal resistance (mΩ)	~ 22.15 (DC) ~ 13.20 (AC)

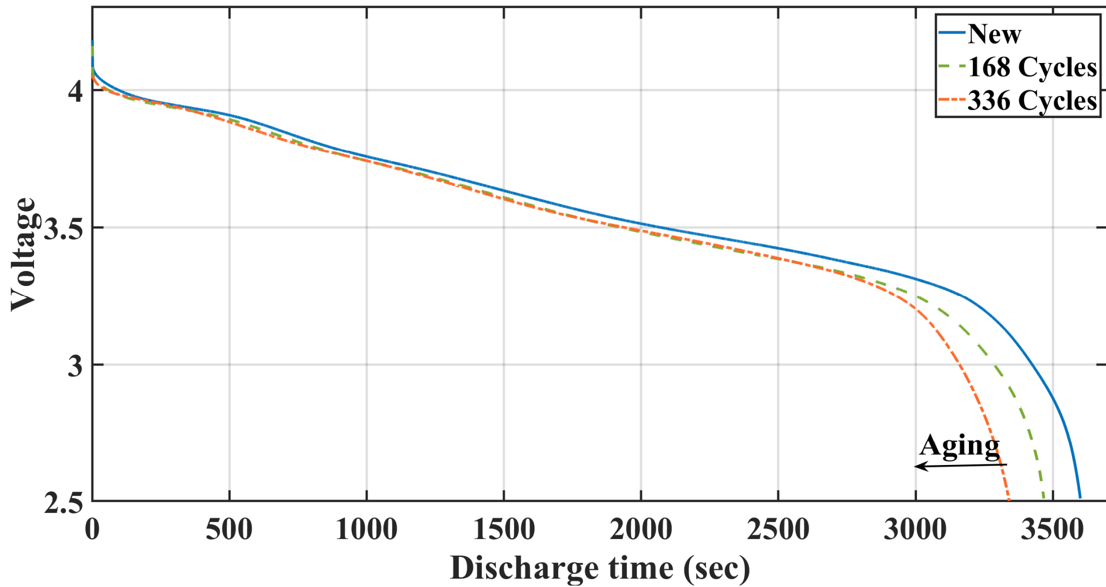


Figure 4.5 Discharge profile of a Li-ion cell after different charging-discharging cycles.

CHAPTER 5

5 CONDITION MONITORING OF POWER SWITCHING DEVICES IN LIVE POWER ELECTRONIC CONVERTERS USING SSTDR

Power semiconductor switches undergo degradation due to environmental and electro-thermal stresses resulting in an impedance variation within the device. This impedance variation can be characterized using spread spectrum time domain reflectometry (SSTDR). A condition monitoring (CM) algorithm for live power converter circuits using SSTDR has been introduced in this chapter. SSTDR has been successfully used for locating transmission line faults and detecting device degradation in power converters while the converters are in an idle state. However, during real-time operation, the devices are switched at high pulse width modulation (PWM) frequency, and therefore, the impedance throughout the entire converter circuit changes fast enough to make the SSTDR-based CM more challenging. This chapter addresses these shortcomings by proposing a novel solution using either an advanced statistical analysis for data interpretation or a little modification in the switching scheme. Several case studies have been discussed where SSTDR test signal (SMPNS) was applied at various test nodes in four different circuits: a single-phase H-bridge PV inverter, DC-DC buck converter as well as DC-DC synchronous buck converter, and a three-phase inverter. In case study-1 described in Section-5.1, a single-phase H-bridge grid-tied PV inverter was considered where the SMPNS has been applied across its output terminal nodes. Using the experimental results, we were able to successfully characterize the degradation level in multiple MOSFETs from this single measurement point. Later in case study-2 narrated in Section-5.2, the SMPNS was applied across the gate-source interface of a MOSFET in a single switch buck converter as well as a synchronous buck converter and a three-phase dc-ac inverter, respectively. The

experimental results demonstrate that the proposed method can successfully characterize the aging of the power devices without affecting the switching performance of the modulation process even the test signal is applied across the gate-source interface of the power MOSFET. This implies that the SSTDR-based CM unit can be embedded with a gate drive circuit since the driver module needs to be connected to the gate-side anyway.

5.1 Case Study-1: Condition Monitoring of a Single-Phase H-bridge Grid-Tied PV Inverter Applying SSTDR Signal Across AC output Node

The grid-tied PV inverter is one of the key components in the PV based renewable energy system where inverters contribute to more challenging reliability issues because of their complicated switching schemes and the use of different component types with dissimilar aging characteristics [126]. In PV based power system, the inverter itself usually has a much shorter life (~10 years) than the PV module (more than 20 years) [126], and 36% of lost energy is occurred due to inverter failures as opposed to 5% loss occurred by the PV module failures [127]. Therefore, making the PV inverter more reliable is the key to prevent the unwanted loss of potential energy production in PV power systems. In this case study, the proposed CM algorithm was implemented in a 700 W H-bridge single-phase PV inverter where two SSTDR hardware test points, TP-1 and TP-2, as shown in Fig. 5.1, has been connected across AC output nodes.

5.1.1 Equivalent Path Impedances

Throughout this dissertation, the term "path impedance" will be used to refer to the equivalent path impedance between the test points seen by the SSTDR test signals. In order to determine the path impedances across the ac output nodes under various operating states, the

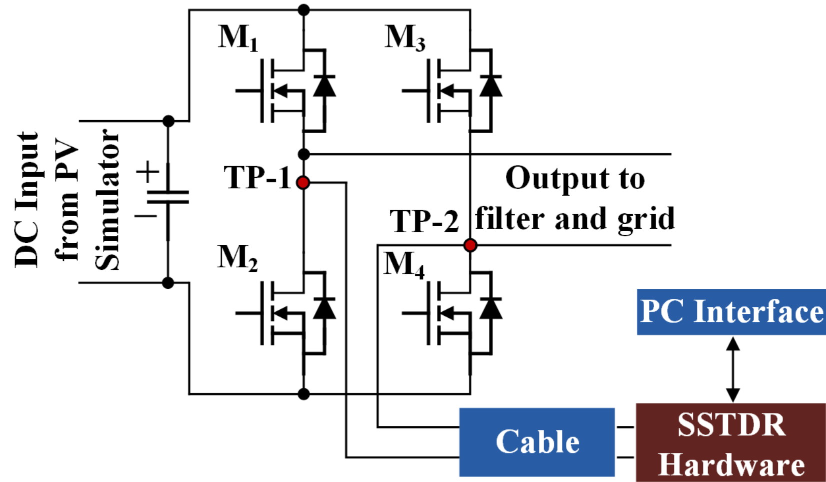


Figure 5.1 SSTDR test diagram for detecting device degradation in a single-phase H-bridge grid-tied PV inverter.

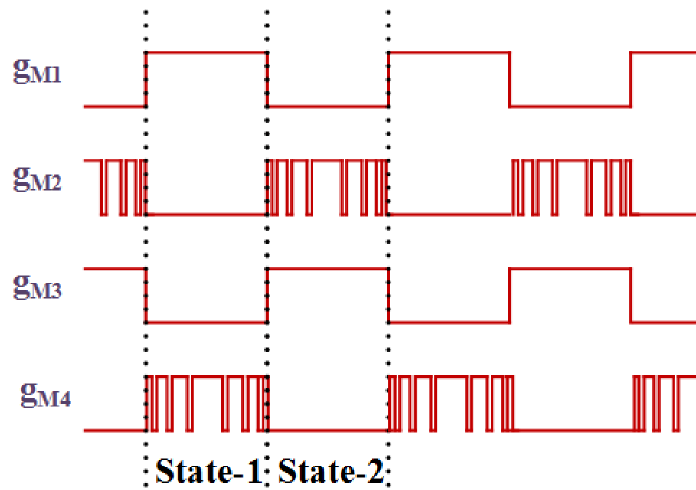


Figure 5.2 Switching scheme used in the single-phase H-bridge grid-tied PV inverter under test.

modulation scheme or switching states (ON/OFF) of the PV inverter under test was studied [45]. It is worth mentioning that in order to minimize the switching loss, the MOSFET pair M_1 and M_3 are switched at grid fundamental frequency using 60 Hz square wave mode in a complementary fashion whereas the other switch pair M_2 and M_4 are switched using 20 kHz sine modulated PWM (SPWM) mode (please see Fig. 5.2). As a result, at each 60 Hz cycle,

two switching states were found, and each of which was further divided into two sub-states without considering the dead-band and the switching transients (please see Table 3). That being said, the conduction states or path impedances change rapidly between the two sub-states

Table 3 Switching states of the PV inverter

State	Sub-State	M_1	M_2	M_3	M_4
1	a	ON	OFF	OFF	PWM (OFF)
	b	ON	OFF	OFF	PWM (ON)
	a	OFF	PWM (OFF)	ON	OFF
2	b	OFF	PWM (ON)	ON	OFF

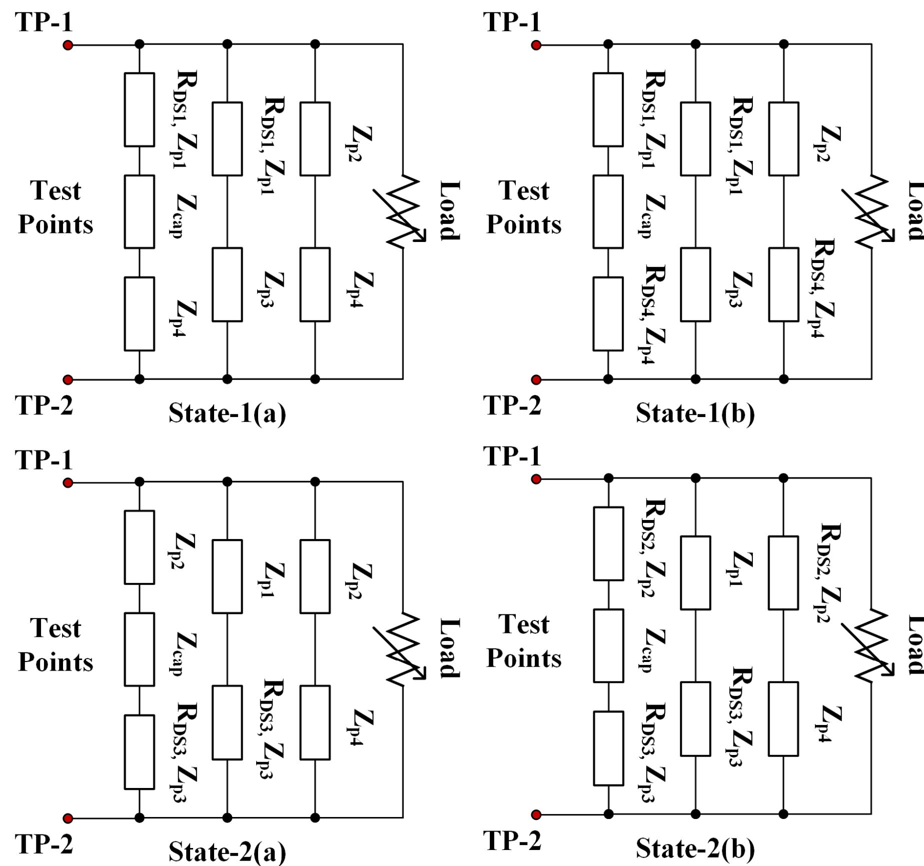


Figure 5.3 Various equivalent SSTDR impedance paths inside the PV inverter. Here, Z_{cap}= impedance of the DC bus capacitor, R_{DS}= ON-state channel resistance of the MOSFET, and Z_p= lumped impedance due to the parasitic capacitances of the MOSFET.

where the maximum time duration of each sub-state is 1/20kHz = 0.05ms. The resulting path impedances corresponding to these switching states are shown in Fig. 5.3.

It is well understood that $R_{DS(ON)}$ and $Z_{eq,GS}$ of a MOSFET increases with the higher level of aging which will increase each path impedance of corresponding sub-states. Evidently, this increase in the equivalent impedance affects the propagation of the SSTDR signal. For instance, any degradation in M_1 will affect sub-state 1(a) and 1(b). In the same way, changes in $R_{DS(ON)}$ of M_3 will affect sub-states 2(a) and 2(b). Sub-state 2(b) and 1(b) will be affected by the change in the value of $R_{DS(ON)}$ of M_2 and M_4, respectively.

5.1.2 Experimental Set-up and Results

The experimental test set-up for CM of the PV inverter is shown in Fig. 5.4 with SSTDR test-points connected across its AC output terminals. Two sets of data are required to detect the aging of a MOSFET: one is for a healthy device (baseline or reference), and the second one is for the aged device. Five groups of tests were conducted to identify the device aging and the first group was considered as the baseline when the inverter with all healthy MOSFETs was scanned in intermittent mode at 24 MHz SSTDR signal. In a similar way, the

Figure 5.4 Experimental test set-up for condition monitoring of H-bridge grid-tied PV inverter under test.

other four groups (group 1-4) were created, however this time, each new MOSFET was replaced by the aged MOSFET, one at a time. Thus, in group 1, 2, 3 and 4, the aged MOSFET (M_{AP1}, $\Delta R_{DS(ON)}$=38.5 mΩ) was used to replace the healthy MOSFETs- M_1, M_2, M_3 and M_4, respectively. A number of continuous scans at each reading were carried out, and at each scan, the negative auto-correlated peak amplitude of the main lobe (corresponding to the distance of the DUT from the SSTDR hardware end) was considered. However, it was observed that within each reading, the autocorrelation peak values generated for the MOSFET with the same aging level were not identical and showed some variations.

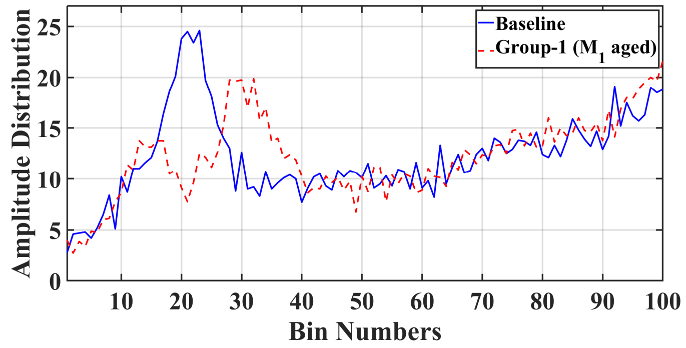
This type of variation in the autocorrelation peak is expected when the impedance change occurs faster than the time taken to process the autocorrelation data for each scan. This processing time for the SSTDR hardware used in this work is approximately 2ms. As mentioned earlier, in our experiment, each path impedance changes within 0.05ms, and that is why we observed such variations in the auto-correlated peak values. One feasible solution to overcome this issue is by re-designing the SSTDR hardware so that the data processing time is lower than the time interval between two consecutive path impedance changes. Unfortunately, such a re-design of this commercial hardware is beyond the scope of this research. That being said, when the MOSFETs are switched at a frequency higher than the 250 Hz (i.e. $T/2$= 2ms at 50% duty cycle), it can progressively increase the difficulty level to differentiate between the healthy and aging data from a limited number of scans, and such a brief switching event would add a very little contribution to the aging detection.

From a statistical point of view, the average error due to this random variation in auto-correlated peak data can be significantly reduced over many scans. That is to say that the accumulation of a large SSTDR dataset from several switching events would eventually help

in reducing the above-mentioned variations. Therefore, data recorded for multiple and consecutive switching events could produce a distinguishable and repeatable signature in the results. This approach of collecting a large dataset for a reasonable time can be significantly useful in identifying the degradation in power devices when they are switched at a high frequency. An aging detection algorithm is developed within the scope of this project based on the histogram of such a large number of auto-correlated peak amplitudes which will be described in the following subsection.

5.1.2.1 Histogram/Amplitude Distribution

Ten readings were taken for each group, and the inverter was scanned at 24 MHz SSTDR signal several times to take each reading. The corresponding auto-correlated peak amplitudes of each reading was divided into one hundred (100) intervals, termed as "bins", in descending order (from higher magnitudes to lower magnitudes). Each bin contains the number count or occurrences of auto-correlated peak amplitudes within a specific range. The frequency distribution of the peak amplitudes in each bin for the ten readings were averaged and coined as '**amplitude distribution**'. The resultant amplitude distribution for each group was compared with the baseline and plotted in Fig. 5.5. Interestingly, there was a rightward shift from the baseline for each group of these bin plots. The rightward shift of the amplitude distribution indicates that the correlated peak amplitudes with lower magnitudes have higher counts for the aged MOSFET compared to the baseline. This is due to the fact that the aged MOSFET has a higher equivalent impedance (combined effect of the increased value of $R_{DS(ON)}$ and $Z_{eq,GS}$) than the healthy device, and this change in the equivalent impedance is experienced by the SSTDR signal which in turn generates correlated peak amplitudes with lower magnitudes. That is why the later bin numbers of an aged MOSFET have higher counts than



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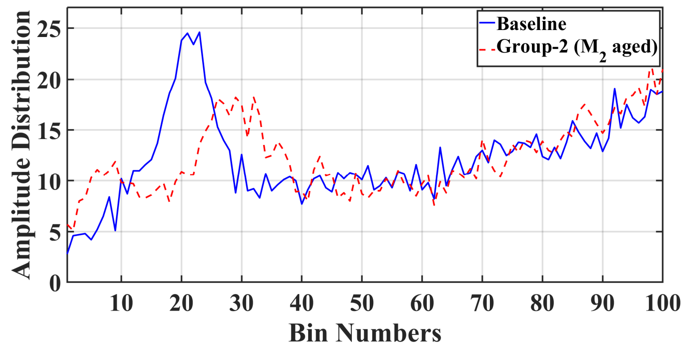

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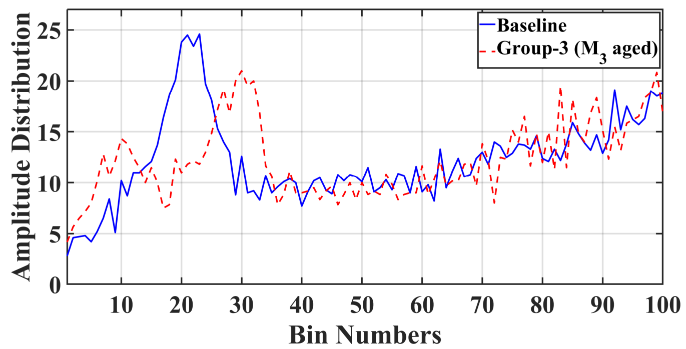

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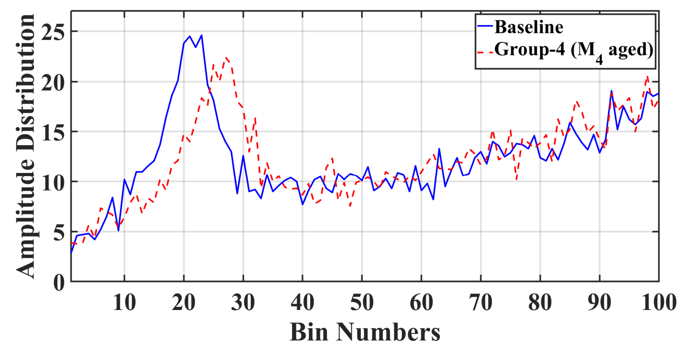

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Figure 5.5 Amplitude distribution-comparison between baseline and an aged MOSFET at (a) M_1 position: aged M_1 (Group 1), (b) M_2 position: aged M_2 (Group 2), (c) M_3 position: aged M_3 (Group 3), and (d) M_4 position: aged M_4 (Group 4).

that of the healthy device. Therefore, this rightward shift clearly indicates that the combined effect of $Z_{eq,GS}$ and $R_{DS(ON)}$ has increased in an aged MOSFET. Interestingly, variations exist in the amount of rightward shift in the amplitude distribution from the baseline for the aged MOSFETs in group-1, group-2, group-3, and group-4 since the distances of the corresponding MOSFETs are different from the SSTDR test points.

5.2 Case Study-2: Condition Monitoring of Power Converters using SSTDR Embedded PWM Sequence

Previous SSTDR based CM methods required SSTDR test signals to be applied across the drain-source terminal of a power MOSFET or collector-emitter terminal of an IGBT [40]–[44]. As explained in the previous section, SSTDR test points could also be connected across the inverter's AC output terminals, which could be unsuitable for high voltage operation. However, in case study-2, device CM was performed while applying sine modulated PN sequence (SMPNS) embedded PWM signals across the gate-source interface of a MOSFET in DC-DC converters and a three-phase power inverter. As mentioned in Section 3.4 of Chapter 3, aging detection from the gate-source interface creates a provision for the development of an intelligent gate-driver architecture with an in-built degradation monitoring unit. Additionally, this unique feature also helps in designing CM hardware for significantly lower ratings and makes CM possible for high voltage converters since the gate terminal is always at a lower potential compared to the drain/collector.

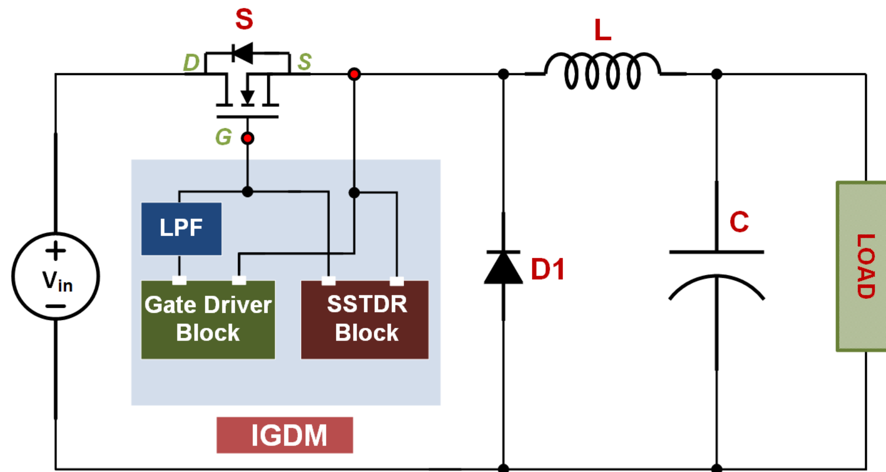
5.2.1 Degradation Detection of Power Devices in a Live DC-DC Converter

CM was performed for both a single switch buck converter and a synchronous buck converter. First, SMPNS embedded PWM sequence was applied across the gate-source terminal of a MOSFET in a single switch buck converter, and corresponding reflections were

recorded and analyzed to detect the aging level in the connected MOSFET. Later, SMPNS embedded PWM sequence was applied across the gate-source terminal of the high side MOSFET in a synchronous buck converter, and it was apparent that this arrangement could measure the degradation in both MOSFETs, one at a time, from a single measurement point. This feature of the proposed method eliminates the need for a separate sensor/accessible nodes/CM monitoring module/intelligent gate driver module for detecting degradation in each device of a power converter circuit leading to significant cost savings.

5.2.1.1 Condition Monitoring of a Single Switch Buck Converter

SSTDR scheme was applied across the gate-source terminal of the MOSFET inside a live single switch buck converter. Two sets of data were taken: one for a healthy MOSFET and one for an aged MOSFET MOSFET (M_{AP2_L1}, $\Delta R_{DS(ON)}$=7.19 mΩ). The MOSFET was aged applying electro-thermal stresses in phase-2 of the accelerated power cycling tests described in Section 4.1 of Chapter 4. The switching frequency of the converter was 20 kHz with a duty cycle of 41.77 %. Fig. 5.6 shows the schematic diagram and the photograph of the test setup. SSTDR scan was performed multiple times in each reading using three different center frequencies, i.e. 48 MHz, 24 MHz and 12 MHz. Ten (10) readings were obtained for the new and the aged MOSFET, respectively and the resultant auto-correlated peak amplitudes were collected and analyzed to identify device aging. Table 4 listed the lowest and highest magnitudes among these peak amplitudes along with their average values for each SSTDR frequency. It was also apparent that the correlated amplitude is higher for lower SSTDR frequencies. As already discussed in Section 3.3 of Chapter 3, the magnitudes of the average values of the SSTDR peak amplitudes were smaller than the baseline once the ON-state channel resistance ($R_{DS(ON)}$) and the equivalent gate-source impedance ($Z_{eq,GS}$) increase. However, like



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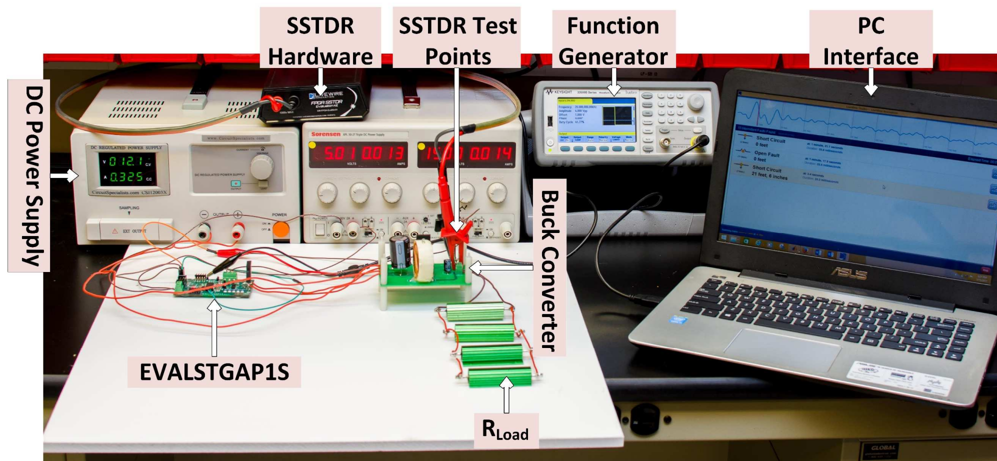


(b)

Figure 5.6 Experimental set-up for condition monitoring of a single switch buck converter: (a) schematic, and (b) photograph.

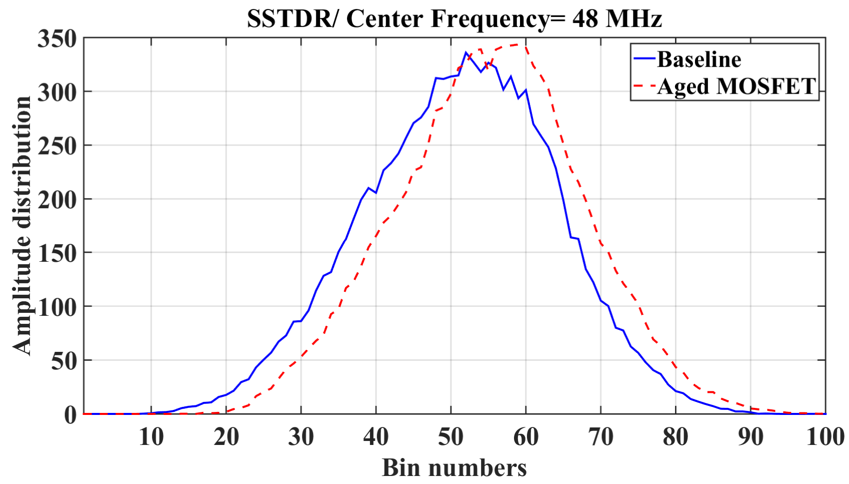
Table 4 SSTDR test results for different frequencies

Magnitude of the Peak Amplitude	SSTDR Frequencies					
	48 MHz		24 MHz		12 MHz	
	Healthy	Aged	Healthy	Aged	Healthy	Aged
Lowest	3310	3165	3577	3343	7287	4064
Highest	8492	8047	9793	9021	18464	17237
Average	5739	5676.4	6779.9	6180.4	12628	11498

SSTDR test-results obtained in the H-bridge PV inverter (discussed in Section 5.1.2), the SSTDR auto-correlated amplitudes for the buck converter showed some variations with the same aging level. This is due to the fact that two operating states of the converter can be considered depending on the ON/OFF state of the MOSFET (ignoring the turn OFF and turn ON switching transients) and these two operating states result in two path impedances that change way faster than 2ms time interval due to high frequency PWM switching. Therefore, the proposed aging detection algorithm developed for case study-1 (discussed in Section 5.1.2) based on the histogram of a large number of auto-correlated peak amplitudes has been adopted here as well. The entire data set was divided into 100 bins based on their amplitudes of descending order as per the range between the lowest and highest values for both the healthy (baseline) and the aged MOSFET. The histogram of each reading of the corresponding bins was averaged and the resultant amplitude distribution for each SSTDR frequency has been plotted in Fig. 5.7. Similar to the amplitude distribution obtained for the H-bridge PV inverter, there exists a pattern for each SSTDR frequencies in these plots, and the rightward shift from the baseline indicates that the correlation data with lower magnitudes in the population have higher counts for aged MOSFET compared to the baseline. This clearly indicates that the combined effect of $Z_{eq,GS}$ and $R_{DS(ON)}$ has increased in an aged MOSFET.

5.2.1.2 Condition Monitoring of a Synchronous Buck Converter: Aging Detection of Multiple Switching Devices from a Single Measurement Point

To perform CM of a synchronous buck converter, SSTDR hardware probes were connected across the gate-source of the converter's high side MOSFET (S_1). Fig. 5.8 shows the schematic diagram and the photograph of the test setup. The switching frequency of the converter was 10 kHz with a duty cycle of 50%. Three groups of tests were conducted to verify



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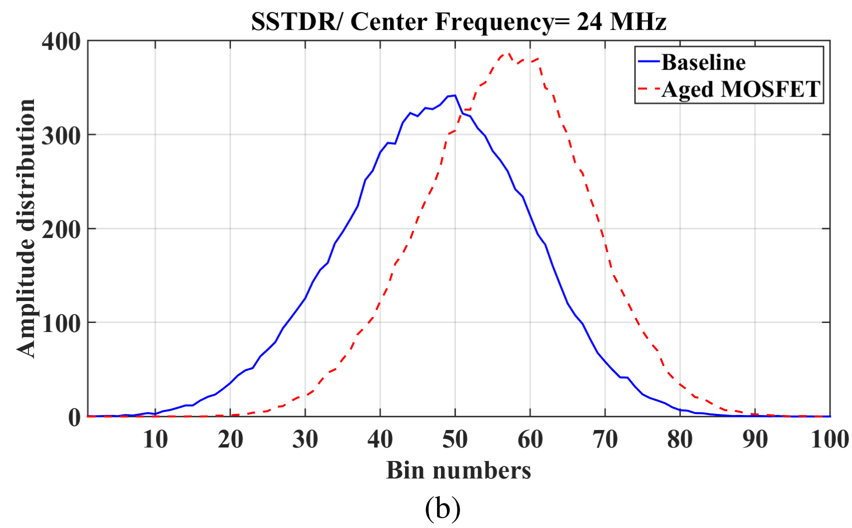

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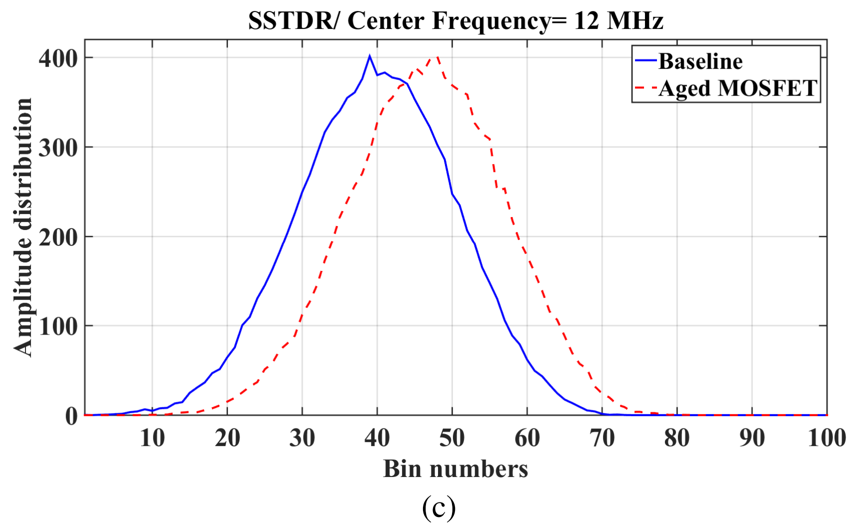

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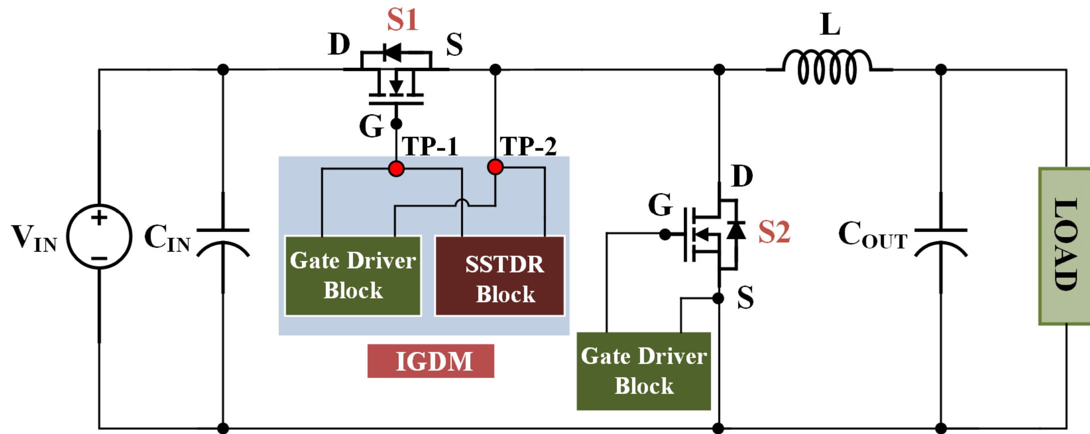
Figure 5.7 Amplitude distribution comparisons for single switch buck converter for SSTDR frequencies: (a) 48 MHz, (b) 24 MHz, and (c) 12 MHz.



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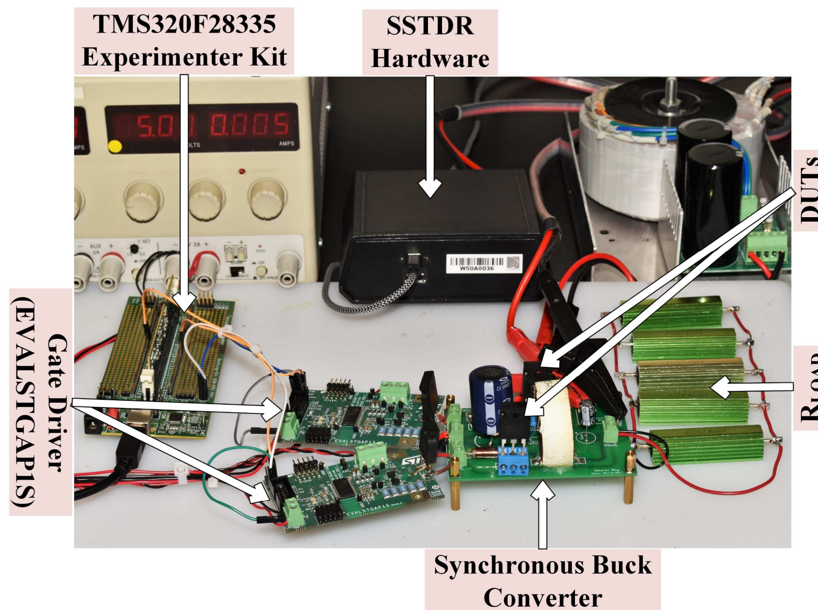


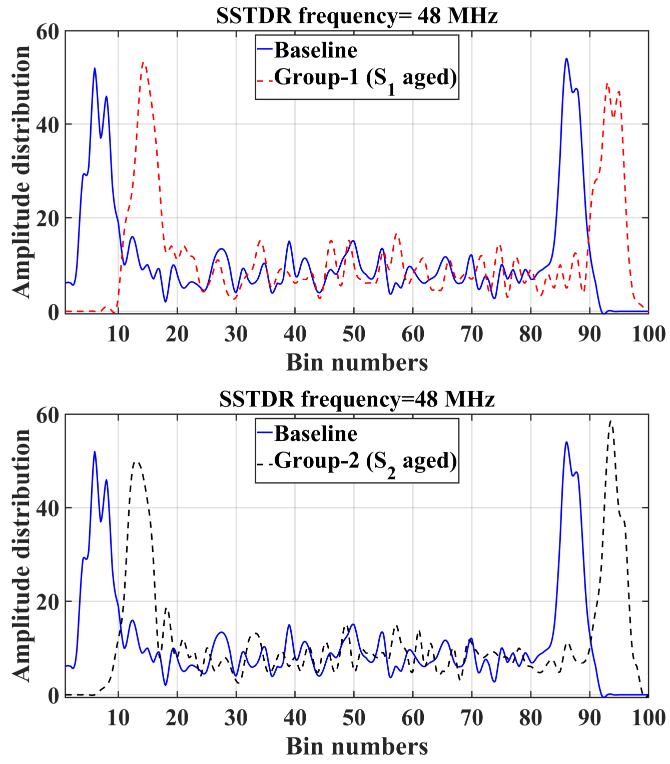
(b)

Figure 5.8 Experimental set-up for condition monitoring of a synchronous buck converter: (a) schematic, and (b) photograph. Here, IGDM= intelligent gate driver module.

the proposed SSTDR algorithm. The first group was considered as a baseline when all MOSFETs were healthy. Then the aged MOSFET (M_{AP2_L4}, $\Delta R_{DS(ON)}$= 27.79mΩ) was sequentially inserted at two different locations inside the converter; high side and low side (one MOSFET at a time) and considered as group 1 and group 2, respectively. In each test-group,

the SSTDR scan was performed multiple times with two carrier frequencies (48 and 24 MHz), and ten (10) readings were obtained in each group. The resultant auto-correlated peak amplitudes were collected and analyzed to identify device aging. As expected, the SSTDR auto-correlated amplitudes for a synchronous buck converter showed some variations with the same aging level. This is due to the fact that two path impedances are possible in a synchronous buck converter due to two switching states: (i) S_1 is ON, S_2 is OFF (state-1), (ii) S_1 is OFF, S_2 is ON (state-2) provided that the dead-band state and switching transients of each MOSFET are ignored, and these path impedances change way faster than 2ms time interval due to high PWM switching. Therefore, the proposed aging detection algorithm developed for H-bridge PV inverter and single switch buck converter based on the histogram of a large number of auto-correlated peak amplitudes has been adopted here as well. The entire set of auto-correlated peak values for each reading was divided into 100 bins based on their amplitudes of descending order. The histogram of each reading of the corresponding bins was averaged for each group and the resultant amplitude distribution has been plotted in Fig. 5.9. Similar to the amplitude distribution obtained for the H-bridge PV inverter and single switch buck converter, there is a rightward shift from the baseline for each group in the bin plots. This indicates that the correlated peak amplitudes with lower magnitudes have higher counts for the aged MOSFET compared to the baseline. This clearly indicates that the combined effect of $Z_{eq,GS}$ and $R_{DS(ON)}$ has increased in an aged MOSFET. Interestingly, a small variation exists in the amount of shift in the amplitude distribution from baseline for group-1 and group-2 since the distances of the two MOSFETs from the SSTDR test points are different.

Above-mentioned experimental results demonstrate that the developed method can perform online degradation monitoring of multiple devices from a single gate-source interface



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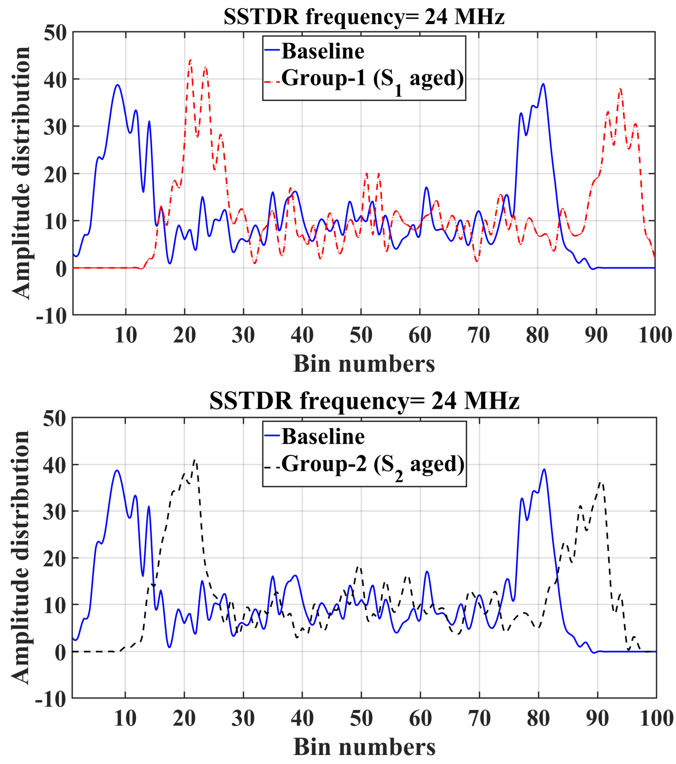


(b)

Figure 5.9 Comparison of amplitude distributions for synchronous buck converter: (a) SSTDR frequency= 48 MHz, and (b) SSTDR frequency= 24 MHz.

of a power device. This feature will eliminate the need for a separate intelligent gate driver/ CM module for detecting degradation in each device, thereby saving a significant system-level cost. Since there is a shift in the amplitude distribution from baseline for MOSFETs at two different locations, this method can potentially identify the locations of aged MOSFETs from a single measurement point.

5.2.2 Degradation Detection of Power Devices in a Live Three-Phase Inverter

Three-phase power inverters are commonly used in electric vehicles, motor drives, aircraft, and many other applications [128]. Many of these applications support precious human lives and therefore, it is of paramount importance to design a highly reliable system. Like many other power converters, three-phase inverters fail in operation due to one or more unpredicted operational conditions and natural degradation in their power switches. For instance, almost 70% of faults in power inverters of variable speed-drives occur due to degradation in power electronic switches [129]. Therefore, continuous CM of these power inverters can be used to schedule maintenance before serious deterioration or break-down occurs.

5.2.2.1 A Modification in the Switching Scheme: Better Accuracy and Flexibility in Condition Monitoring of a Live Three-Phase Inverter

A conventional two or three-level three-phase inverter has six switches, and therefore when the inverter switches operate at several kHz switching frequency, there will be multiple path impedances for SSTDR signal in a complete switching cycle. Due to a higher number of impedance paths in a given switching interval, the rate of variations in these complex path impedances will be higher compared to a single-phase H-bridge PV inverter and DC-DC converter [48], [50]. Therefore, a three-phase inverter will require larger number of SSTDR test datasets (compared to the other topologies mentioned earlier) in order to reduce the effect

of variation in auto-correlated peak data due to fast path impedance change caused by high-frequency PWM switching.

One possible way to overcome this issue is to reduce the switching frequency at system fundamental frequency (for example, 60 Hz) for a fraction of a second, and this will meet the requirement of minimum time interval needed for SSTDR hardware (i.e. > 2ms) to avoid the variations in the SSTDR readings generated for the same aging level. For instance, if the inverter operates at 60 Hz square wave mode for a very short time period (a very few cycles such as 5-6 cycles), SSTDR based CM method will have the following advantages:

(i) When the inverter operates at 60 Hz square wave mode with a 50% duty cycle, the path impedance changes three times in each half-cycle (i.e., ~$T/2$=8.33ms) (see Fig. 5.10).

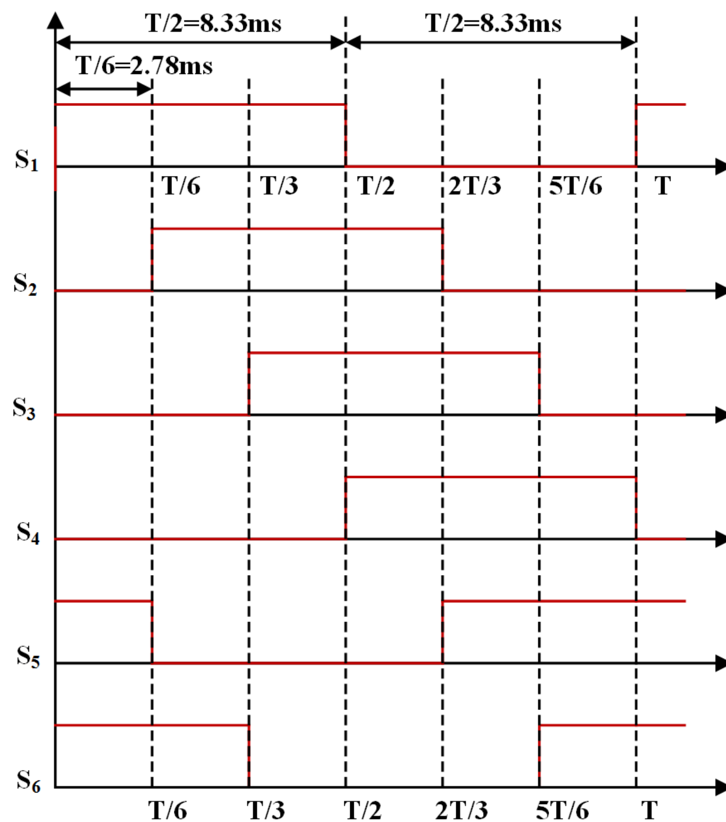


Figure 5.10 A 60 Hz square wave mode switching scheme of a three-phase inverter.

This implies that the time interval between two consecutive path impedances is ~ 2.78ms which eliminates the SSTDR hardware limitation.

(ii) 60 Hz square mode operation will require significantly less amount of data in order to successfully detect the device aging compared to kHz range switching mode since it will reasonably reduce the variation in auto-correlation peak data.

(iii) A smaller number of required data will greatly decrease the computational time for data processing demanded by the CM hardware.

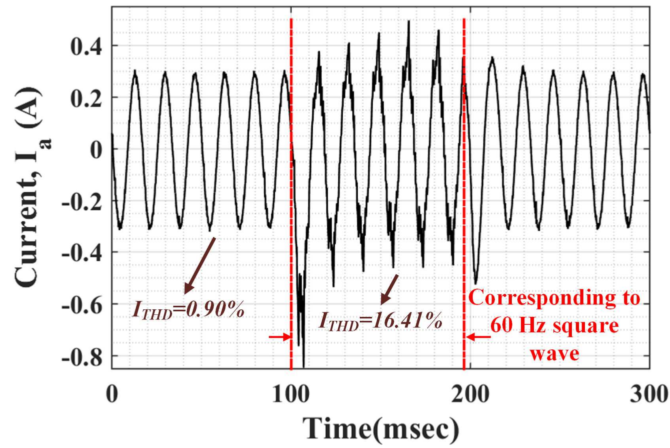
(iv) Inverter output will have a fundamental frequency of 60 Hz which matches the main's frequency in the USA.

Operating the inverter permanently in 60 Hz square wave mode will produce higher harmonic contents at the output compared to the operation in SPWM mode. Therefore, the square wave operation for a prolonged time period is not a practical way to generate ac output either in grid-parallel or standalone configuration. Using the proposed technique, the inverter is intended to operate in square wave mode for a brief period, and the motor will experience this higher total harmonic distortion (THD) level only for a fraction of a second (such as 100ms). This short time period is negligible compared to the starting time of the motor, which is typically a few seconds for a large motor, and during this startup time, a motor may experience even higher harmonics and 8-10 times higher currents than its rated current [130]. This startup time could be exploited to determine the SOH of the inverter because the fundamental frequency of the motor is much smaller than 60 Hz during startup. This low-frequency operation provides more time for the CM hardware and added flexibility to schedule the CM scheme. Therefore, the inclusion of a temporary square wave operation will have

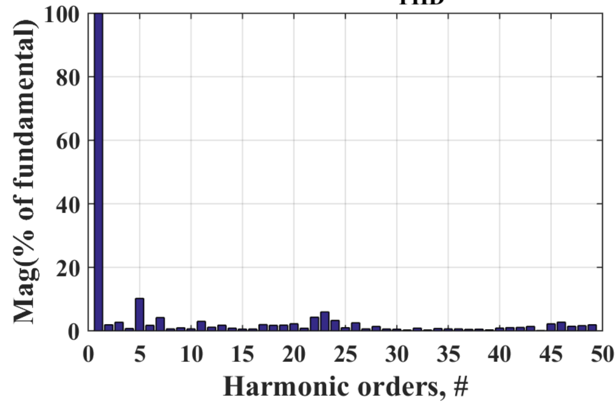
negligible or no impact on the motor's operation although it provides a clear benefit to accurately estimate the SOH.

To observe the effect of operating the inverter without any modulation, a ¼ hp three-phase induction motor was powered by a 30 kHz SPWM inverter operated momentarily in a 60 Hz square wave mode. The inverter runs at 30 kHz SPWM mode during normal operation and was allowed only once to run for 100ms in 60 Hz square wave mode. This 100ms window is used to take necessary SOH measurements although this small window has no effect on the operation of the inverter, which we have experimentally verified. The resultant a-phase current (I_a) is plotted in Fig. 5.11 (a). There is a slight increase in current during this 100 ms window because no current feedback controller was used. However, this change in the current level is reasonably below the inrush current threshold of a typical induction motor and did not have any meaningful impact on the RPM of the motor. We need to keep in mind that the motor did not have any load or torque inertia. Therefore, with load, the corresponding change due to this square wave operation will be even smaller.

It is apparent that the current waveform has some level of distortions (please see Fig. 5.11). *However, the inverter was operated in 60 Hz square wave mode momentarily, and the minimum time required for a "very short period" harmonic content measurement is 3s according to IEEE standard 519* [131]*; therefore the resultant current distortion of 100ms duration is of no consideration and can be treated as transient disturbances commonly prevalent in power systems.* Yet, the inverter was allowed to operate for 3s in 60 Hz square wave mode to measure (<u>not for condition monitoring</u>) the THD in line current (I_a), and the corresponding harmonic spectra are shown in Fig. 5.11 (b), which can be compared with the corresponding harmonic spectra of 30 kHz SPWM operation (please see Fig. 5.11 (c)). This 3s



(a)



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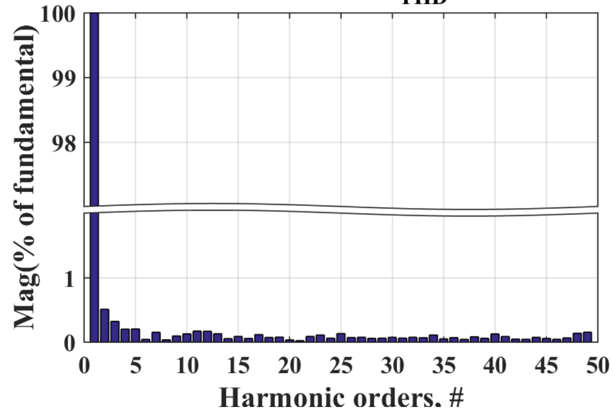


(c)

Figure 5.11 (a) a-phase current waveform of the three-phase induction motor at two different switching modes of the inverter, (b) corresponding I_{THD} at 60 Hz square wave mode, and (c) corresponding I_{THD} at 30 kHz SPWM mode.

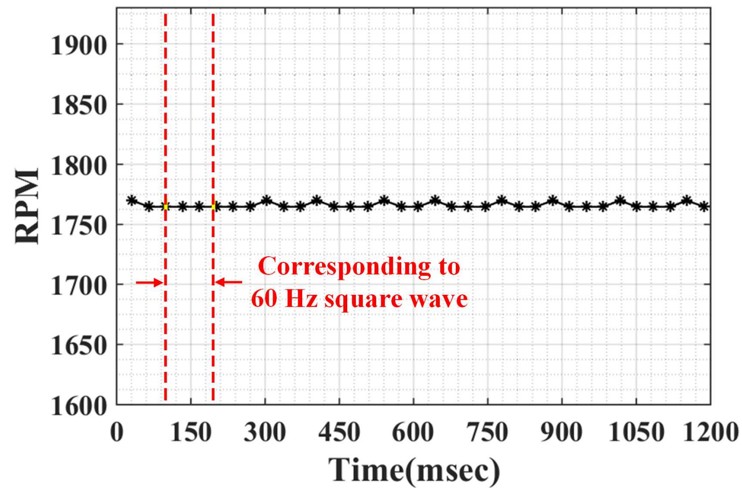


Figure 5.12 RPM of the 3-phase induction motor at two different switching modes of the inverter.

window was used for conducting the harmonic analysis only, and in real SOH measurement, only a 100ms window is needed. The RPM of the motor remains almost unaffected in both cases of momentary 60 Hz square wave and 30 kHz SPWM operation (refer to Fig. 5.12). In addition, if the inverter runs with a feedback controller, changes in the RPM, if there is any, would be quickly stabilized, which has not been implemented in our case, and this implementation was beyond the scope of this project. On top of that, when the line suffers such common disturbances for a short period of time, the inertia of large machines will maintain a constant speed. Furthermore, if the motor is running a generator in a motor-generator set, the flywheel adds more inertia to increase the ride through time that maintains the power supply for several seconds under such disturbances. This method is equally applicable to grid-tied inverters since grids are designed to be stiff to withstand such momentary disturbances which are very common in power systems [132]. In fact, a similar kind of modulation can be found in [133] where the DUT does not switch during a certain time of the fundamental period of the inverter to guaranty the accuracy of the precursor parameter measurements.

5.2.2.2 *Quantifying Degradation Levels in a Power Device of a Live Three-Phase Inverter*

In the previous studies, the auto-correlated SSTDR amplitudes obtained for the healthy device and aged device with one aging level were compared and plotted in order to demonstrate the feasibility of the proposed method. This section will document the investigation of SSTDR data associated with a degraded MOSFET having *different aging levels* of a live three-phase inverter.

A three-phase inverter prototype (testbed) that was designed and built to implement the proposed CM technique is shown in Fig. 5.13. A 48 MHz SMPNS signal was applied across the gate-source of the bottom MOSFET (S_4) of the inverter's first leg as shown in Fig. 5.14. The inverter was being operated continuously at 30 kHz SPWM mode. However, during

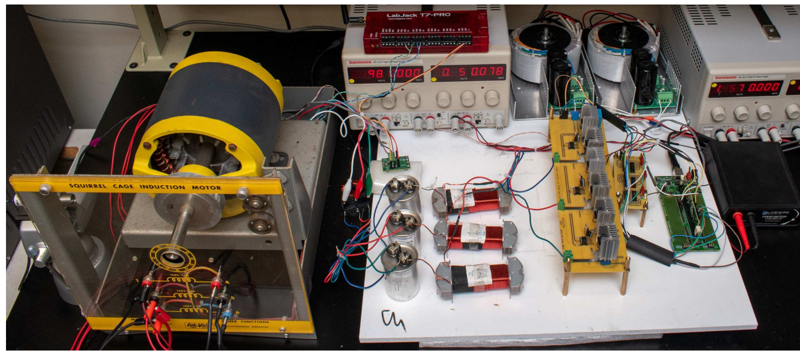


Figure 5.13 Prototype of a three-phase inverter running an induction motor.

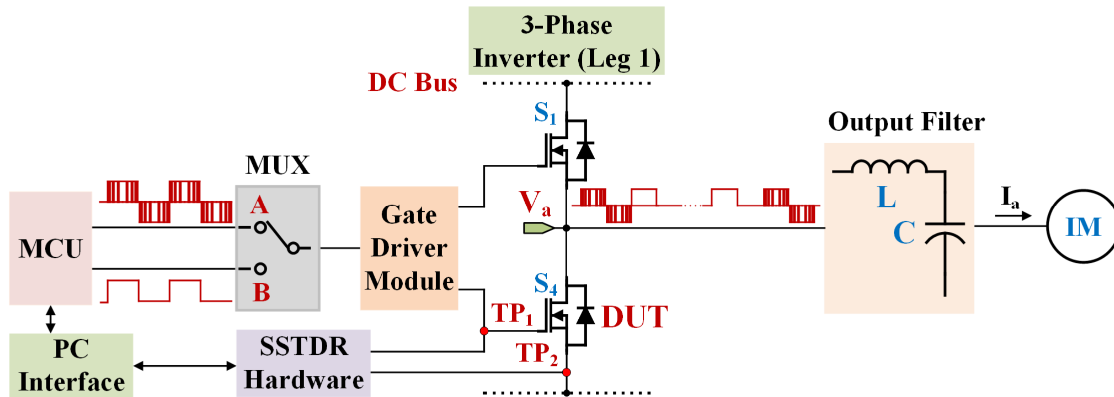
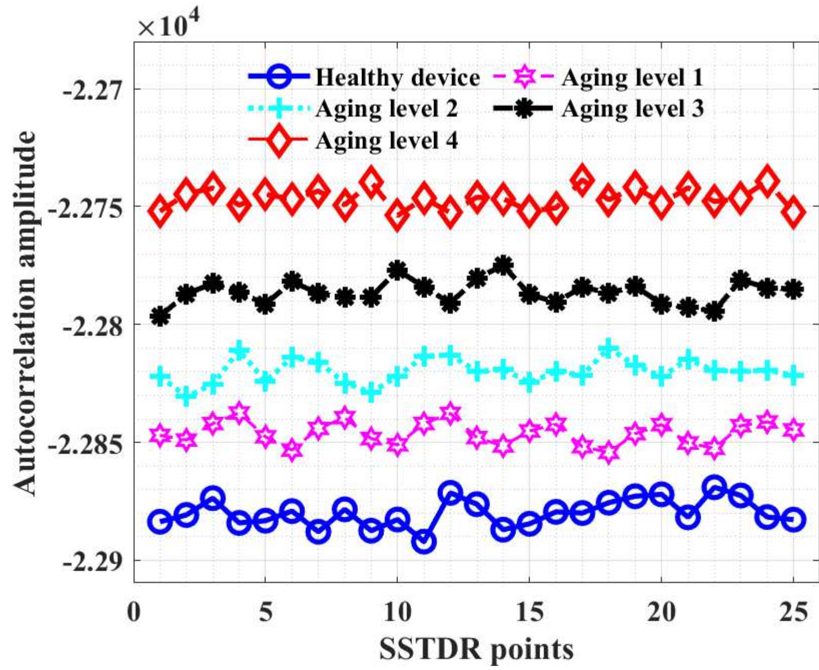
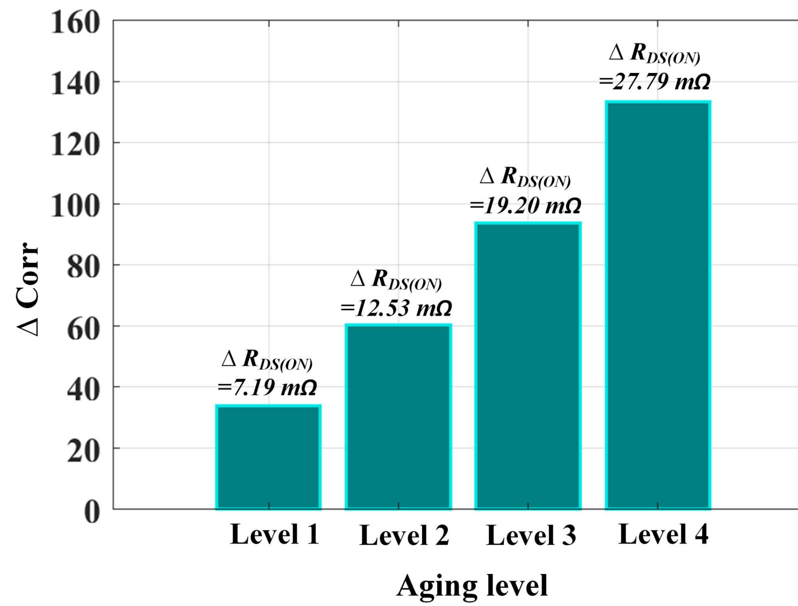


Figure 5.14 Block diagram of the proposed synchronization scheme where SSTDR signal is synchronized with 60 Hz square wave gate signal at Leg 1 of the inverter.

SSTDR measurement, the 60 Hz square wave mode was activated for a duration of 100ms to monitor the SOH of the MOSFET at S_4 position. The gate signals (30 kHz SPWM and 60 Hz square wave) were multiplexed and the SSTDR signal (SMPNS) was synchronized accordingly with the 60 Hz square wave signal. In each 60 Hz cycle, four auto-correlated peak amplitude data were recorded leading to a total of 25 data points (approx.) over 100ms time interval. An auto-correlated baseline with the 100ms duration was created for the inverter with all (6) fresh MOSFETs. Similarly, the resultant auto-correlated peak amplitudes were recorded for a 100ms period with an aged MOSFET having four aging levels, one at a time, at position S_4. The MOSFET was aged applying electro-thermal stresses in phase-2 of the accelerated power cycling tests described in Section 4.1 of Chapter 4. Here, aging level 1, aging level 2, aging level 3, and aging level 4 represent a change in the $R_{DS(ON)}$ from the initial $R_{DS(ON)}$ of the healthy MOSFET by 7.19 mΩ (M_{AP2_L1}), 12.53 mΩ (M_{AP2_L2}), 19.2 mΩ (M_{AP2_L3}), and 27.79 mΩ (M_{AP2_L4}), respectively. The resultant SSTDR auto-correlated peak amplitude data have been plotted in Fig. 5.15 (a) and the non-zero differences among the auto-correlated peak amplitudes corresponding to the baseline and different aging levels clearly indicate the aging of the S_4-MOSFET. As expected, SSTDR auto-correlated peak data have decreasing magnitudes with the increasing aging levels (aging level 4> aging level 3> aging level 2> aging level 1> healthy device/baseline). In addition, the amplitude differences between the averages of all baseline data and the auto-correlated peak data corresponding to each aging level (denoted as $\Delta Corr$) have been recorded and plotted as a bar plot in Fig. 5.15 (b). This plot shows that the amplitude difference between the baseline and the auto-correlated peak data corresponding to an aged MOSFET becomes larger with the level of aging. Therefore, it is



(a)



(b)

Figure 5.15 (a) SSTDR correlated peak amplitude data for multiple aging levels of S_4-MOSFET, and (b) changes in the average SSTDR correlated peak amplitude data for multiple aging levels of S_4-MOSFET. Here, initial $R_{DS(ON)}$ of the healthy MOSFET is 48.04 mΩ.

evident that this proposed technique can determine the level of aging by measuring the SSTDR reflection data-higher the aging, lower the reflection data.

5.2.2.3 Aging Detection of Multiple Power Devices in a Live 3-Phase Inverter using a Single Access/ Measurement Point

This section proposes a condition monitoring (CM) method based on SSTDR that can detect the aging level of multiple devices at different locations, although it requires only the gate-source interface of a single device to connect the SSTDR test probes. Therefore, the proposed method can save additional computation/processing time as well as reducing the number of access nodes and/or CM modules to perform the health monitoring of all individual devices in a three-phase inverter leading to significant cost savings.

SSTDR test signal of carrier frequency 48 MHz was applied across the gate-source of the top MOSFET (S_1) of the inverter's first leg as shown in the schematic diagram of Fig. 5.16. At first, the inverter was running with all fresh MOSFETs, and the corresponding SSTDR test data were recorded. After that, SSTDR data were recorded by replacing the healthy MOSFETs

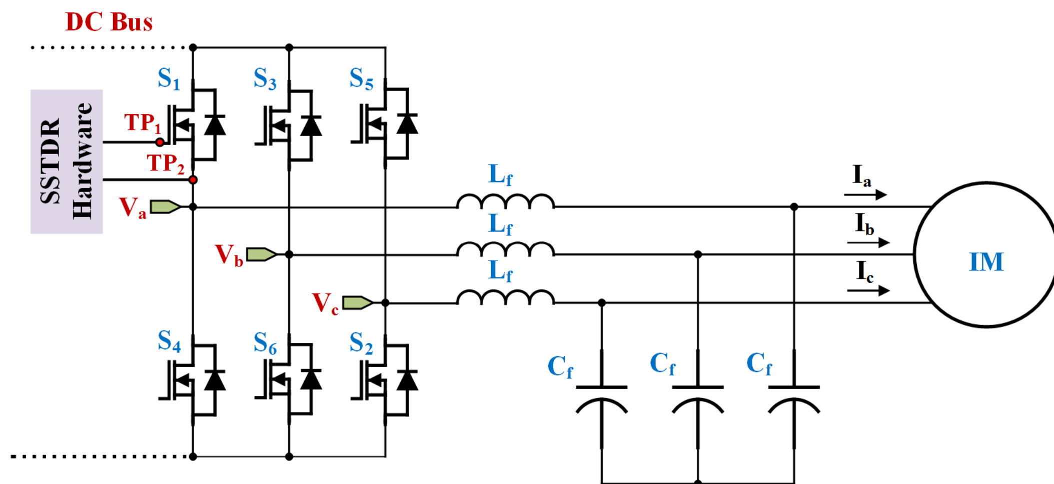


Figure 5.16 Schematic of the three-phase inverter prototype connected with an induction motor. Here, SSTDR test signal is synchronized with 60 Hz square wave gate signal of S_1 MOSFET.

with an aged MOSFET (M_{AP2_L4}, $\Delta R_{DS(ON)}$= 27.79mΩ) in all six locations (S_1, S_2, S_3, S_4, S_5, and S_6), one at a time. It is worth mentioning that during SSTDR measurement, the inverter was temporarily operated without PWM for a fraction of a second (such as 100ms) at a fundamental frequency of 60 Hz. A MUX was used to select between the two gate signals (30 kHz SPWM and 60 Hz square wave) in a similar way shown in Fig. 5.14.

In each 60 Hz cycle, four auto-correlated amplitudes were recorded leading to a total of 25 data points (approx.) over a 100ms time interval. An auto-correlated baseline was created while the inverter was running with all healthy MOSFETs. After that, the healthy MOSFETs in three random locations (S_1, S_3, and S_6) were replaced with the aged device (one at a time) to record the corresponding SSTDR auto-correlated amplitudes. These data are plotted in Fig. 5.17 and the non-zero differences among the auto-correlated amplitudes corresponding to the baseline and the aged device (at different locations) clearly indicate the aging of the MOSFET. Interestingly, the magnitude of the auto-correlated peak amplitude associated with the aged

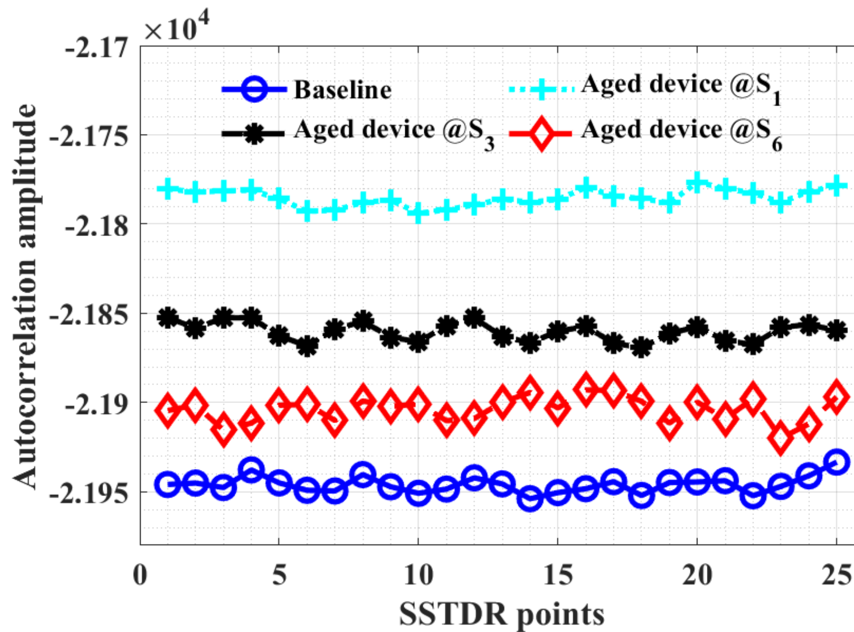


Figure 5.17 SSTDR correlated amplitude data for baseline and aged MOSFET at three different locations.

device located at S_1 is lowest whereas the magnitude of the auto-correlated peak amplitude associated with the aged device located at S_6 is highest (auto-correlated magnitude for aged MOSFET at position $S_1 <$ aged MOSFET at position $S_3 <$ aged MOSFET at position $S_6 <$ healthy device/baseline) because the device at S_6 is physically located further away from location S_1 compared to location S_3 (please see Fig. 5.16). According to [34], [37], when $\rho \leq 0$, the magnitude of the auto-correlated peak amplitude increases as the reflected signal attenuate. Since the reflected signal weakens or attenuates over the distance, the magnitude of the auto-correlated peak amplitude associated with the aged device gradually increases if it is positioned further from the SSTDR test points. SSTDR test data were recorded for the remaining switches as well from the same test nodes (gate-source interface of S_1 device). To visualize the above-mentioned phenomenon, a combined bar plot taking the average of auto-correlated amplitudes of each device for all six locations (S_1, S_2, S_3, S_4, S_5, and S_6) is shown in Fig. 5.18. Interestingly, the auto-correlated amplitudes corresponding to the aged MOSFETs that are located close to each other have smaller differences between them compared to differences between the aged MOSFETs located farther away. This small difference in the auto-correlated amplitude offers smaller headroom to reliably distinguish the aging information of these MOSFETs. Please note that distance resolution of the autocorrelation increases with an increase in carrier frequency [34], [37]. However, the commercial SSTDR hardware used in this experiment can produce a maximum carrier frequency of 48 MHz. That being said, with this 48 MHz of the carrier frequency, SSTDR would produce more reliable results when (i) the aged device is located closer to the test points, and (ii) the aged devices are located farther from each other. One possible way to pinpoint the location of each aged device with better reliability is to take another

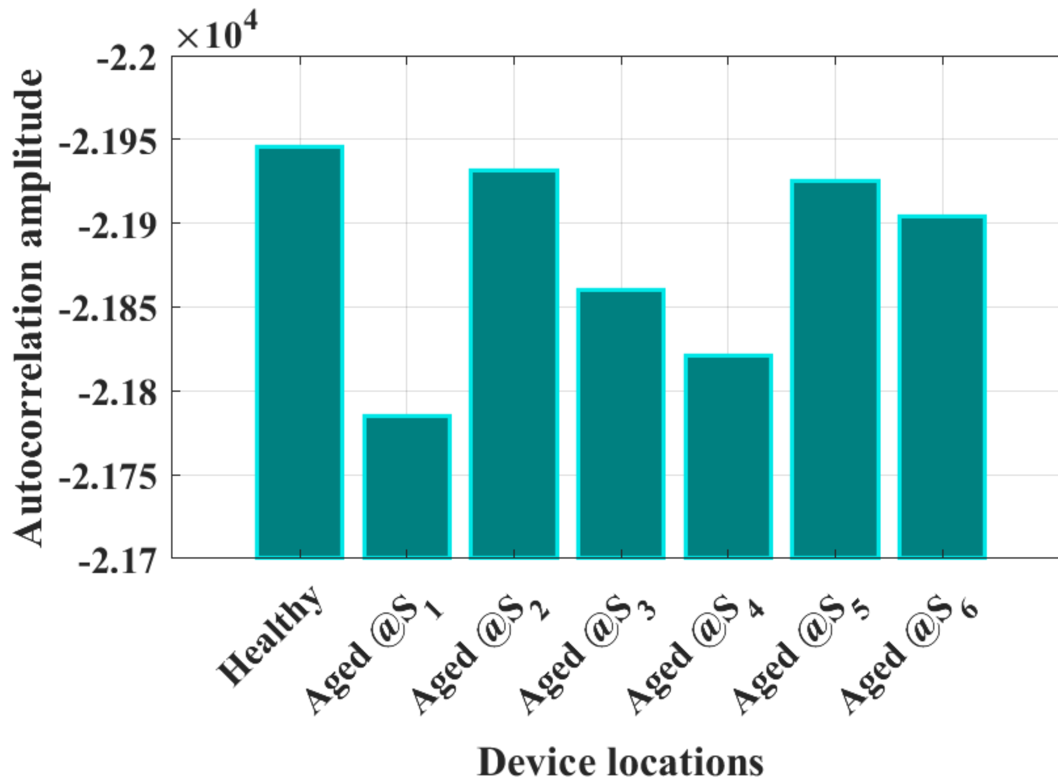


Figure 5.18 Average SSTDR correlated amplitude data for healthy and aged MOSFET located at all six locations.

set of SSTDR auto-correlated amplitude readings from some other location, if possible, from the S_2 position since it is located farthest from the S_1 position.

5.3 Discussion

The feasibility of using SSTDR for CM of power devices has been discussed in two separate case studies provided in Section 5.1 and Section 5.2, respectively. The proposed SSTDR based CM technique can successfully detect device degradation in a live H-bridge PV inverter and DC-DC converters at the cost of a large amount of SSTDR data acquisition for the purpose of error reduction. In contrast, a little modification in the switching scheme can

overcome such limitations inside a three-phase inverter, and this dissertation has presented this concept in detail.

The proposed method is based on the change in $R_{DS(ON)}$ due to the device aging, and $R_{DS(ON)}$ is a function of junction temperature (T_j). Therefore, measurements need to be taken at identical electrical and temperature conditions. Otherwise, the relationship between the $R_{DS(ON)}$ along with its corresponding SSTDR data and temperature is required to be stored in a look-up table (LUT). A calibration procedure should be conducted to update this LUT both for electrical loading and T_j to compensate for operating condition dependencies [4], [6], [30], [88]. Some studies attempted to compensate for T_j using electrothermal and/or loss models [134]–[136], while others have carried out case temperature measurement as a substitute [24], [137], [138]. In addition, commercial solutions presently exist, which uses temperature sensors directly integrated into the power chip structure [139]. CM is easier to be implemented under similar operating conditions if the current level can be controlled and the average junction temperature is relatively stable [88]. For applications with frequent start-stop, it is possible to run the algorithm at the startup under similar operating conditions [30]. As stated earlier, exploiting this startup time to determine the SOH of the inverter provides more time for the CM hardware and adds flexibility to schedule the CM scheme. In addition, as the change in $R_{DS(ON)}$ due to the device aging progress slowly, evaluating it throughout the long-time intervals is a reasonable approach [30].

5.4 Conclusion

This chapter presents an SSTDR based in-situ degradation detection technique applicable to live power switches in various power converter topologies. The difference in the auto-correlated amplitudes obtained for the healthy devices and aged devices can be capitalized

to determine device degradation; a bigger difference indicates higher degradation. The proposed technique has been implemented in several power converters including DC-DC converters and a three-phase motor drive. Until today, the SSTDR-based SOH monitoring techniques are only able to detect device degradation while the converter operates in an idle state, therefore the technique cannot be implemented in live power converter applications. In contrast, the methods proposed in this paper can estimate the SOH of a power device regardless of its operating states (live or idle). Furthermore, aging detection from the gate-source interface creates a provision for the development of an intelligent gate-driver architecture with an in-built degradation monitoring unit. Although the tests were carried out to detect aging in power MOSFETs, this technique is equally suitable for other power devices such as IGBTs and silicon carbide (SiC) MOSFETs. We strongly believe the outcome of this research will create a paradigm shift in the field of online SOH monitoring not only by incorporating the CM hardware into the gate driver architecture but also by significantly reducing the human errors associated with the traditional precursor parameter-based aging detection methodologies. The gate driver manufacturing industries will be greatly benefitted from the outcome of the research by adopting this intelligent gate driver concept. Therefore, this research will create a seminal impact in the reliability sector, and the lifetime of the power converters can be greatly increased by performing scheduled maintenance, which will eventually increase the run time of the power modules and reduce maintenance costs.

CHAPTER 6

6 AN IRRADIANCE-INDEPENDENT, ROBUST GROUND-FAULT DETECTION SCHEME FOR PV ARRAYS BASED ON SSTDR

A healthy PV array has a specific impedance between node pairs, and any ground fault changes this impedance. Since spread spectrum time domain reflectometry (SSTDR) can characterize the impedance discontinuities in its propagation path along with their locations, it can become an excellent candidate for PV array ground fault detection. However, the presence of multiple reflections occurring at different mismatches and interconnections inside the PV system makes interpretation of the time-domain reflection extremely difficult to detect the presence of a ground fault in PV arrays. A fault detection algorithm using SSTDR introduced in this paper demonstrates that SSTDR data can be implemented to overcome such limitations resulting in faithful detection of ground faults in PV arrays. Most importantly, the proposed fault detection scheme can detect ground fault at night or low illumination, because this method does not use traditional on-site parameters such as the amplitude of the fault current. In addition, a comprehensive analysis has been conducted for the first time to investigate the impact of different parameters, i.e., carrier signal frequency, fault resistance, irradiance, number of faults, and number of strings on the observed result.

6.1 Ground Fault Detection Algorithm

The proposed ground-fault detection algorithm was implemented at the Distributed Energy Technologies Laboratory (DETL) of Sandia National Laboratories (SNL) (see Fig. 6.1). A PV string consisting of seven, series-connected PV modules from Sanyo was interfaced with the SSTDR hardware (WILMA LWG40414), as depicted in the schematic diagram in Fig. 6.2. The dimension of each module was 51.9 × 34.6 × 1.8 in. Each module was connected in

Figure 6.1 Test set-up used at DETL of SNL.

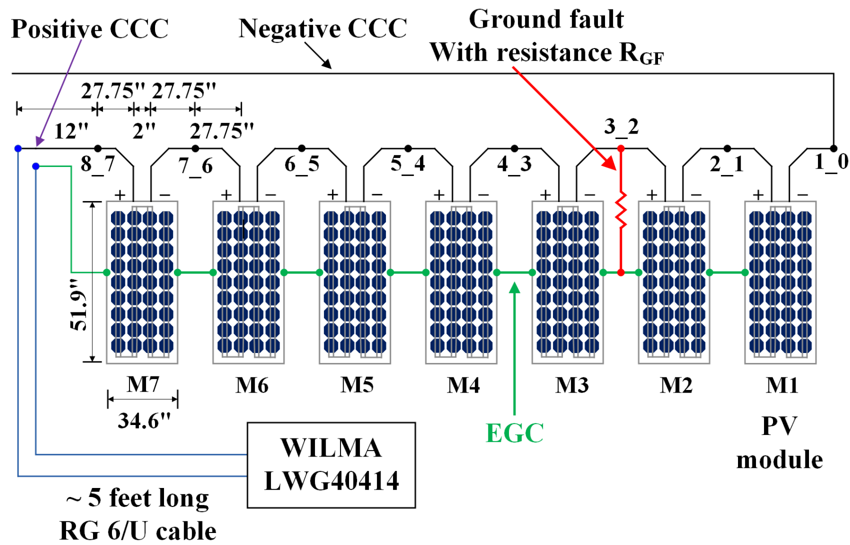


Figure 6.2 Schematic diagram of the test setup (physical dimensions are not drawn according to scale).

series through 55.5-in cable, where each fault location was exactly halfway between the adjacent module. Specifications of the PV modules are listed in Table 5. The positive CCC and the EGC of the PV string were connected to the output terminals of the SSTDR board. The ground-fault detection algorithm developed within the scope of this research is based on the three steps described in the following subsections, and a flowchart of this algorithm is shown in Fig. 6.3. In order to avoid needless disconnections during monitoring the system for ground

faults, it is advisable to have the SSTDR system permanently connected to the device under test.

Table 5 Specification of a PV module used in the test setup (at 1000 W/m^2, 25ºC cell temperature)

Maximum power (P_{max})	200 W
Short circuit current (I_{sc})	3.83 A
Open circuit voltage (V_{OC})	68.7 V
Maximum power current (I_{pmax})	3.59 A
Maximum power voltage (V_{pmax})	55.8 V

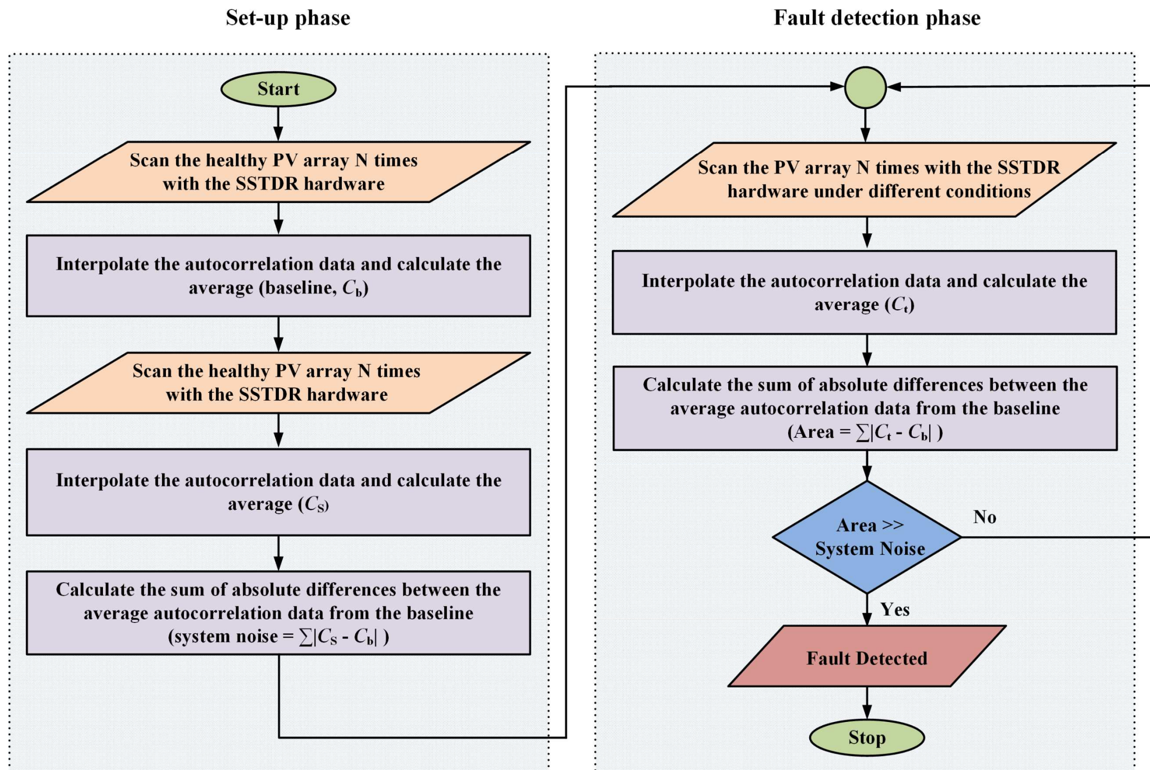


Figure 6.3 Flowchart of the ground-fault detection algorithm.

6.1.1 Baseline Creation

Every PV array has different reflection patterns, and it is necessary to create a baseline for each array under consideration. This will work as a reference to detect ground faults later. In order to create the autocorrelation baseline (C_b), the PV string without any ground fault was scanned in static mode for five times (i.e., $N = 5$), and autocorrelation plots were interpolated at the rate of 10 using interp () function in MATLAB. If C_i (i=1, 2, 3, 4, 5) are the interpolated autocorrelation vectors, C_b is defined as

$$C_b = \frac{\sum_{i=1}^{N} C_i}{N} \tag{6.1}$$

The baseline plot with a carrier/center frequency of 750 kHz is shown in Fig. 6.4. The abscissa of the autocorrelation plot has been represented in the form of time delay since the velocity of propagation through the PV string is unknown and is expected to vary throughout the PV string. For our algorithm, the average of these five autocorrelation plots for each center

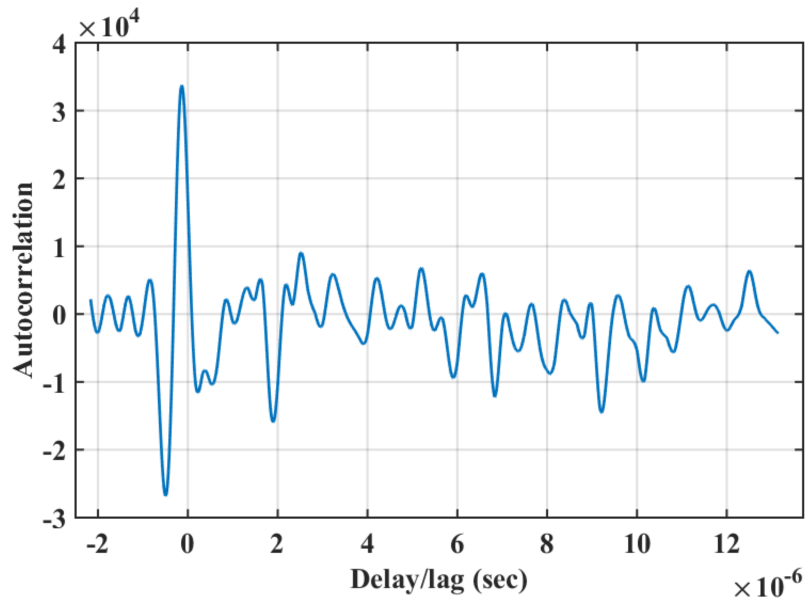


Figure 6.4 Baseline autocorrelation plot for ground-fault detection with center frequency 750 kHz.

frequency is considered as a baseline for differentiating PV array without ground fault (healthy PV array) and with ground fault. It should be noted that both the scan number (N) and interpolation rate (M) have been chosen arbitrarily, and the time taken to create the autocorrelation baseline for each scan was approximately 4ms. The net processing time for implementing the algorithm (except scanning the system) depends on the sampling rate and the computational speed of the digital signal processor block. However, a higher number of scans or interpolation rate is recommended provided the system can handle a big amount of data.

6.1.2 System Noise Estimation

The autocorrelation data generated by the SSTDR hardware for the same setup are not identical and show some variations, as shown in the error plot for a carrier frequency equal to 750 kHz in Fig. 6.5. These variations in the autocorrelation plot are expected because of the thermal noise, noise generated from the analog to digital conversion, etc. Considering this fact, SSTDR was applied N times to the same PV array, and the autocorrelation data were interpolated and averaged (C_s). Each baseline data point calculated in the previous subsection (C_b) was subtracted from the calculated average data, and the absolute values of the differences were considered. The sum of the absolute differences between the average autocorrelation data and the baseline is considered as an estimate of system noise (N_s) as shown in (6.2) since both values were collected for the same healthy PV string. To facilitate the real-time monitoring of the PV array, C_s needs to be periodically measured, and therefore, N_s will be updated accordingly.

$$N_s = \sum_{i=1}^{k} | C_{s,i} - C_{b,i} | \quad (6.2)$$

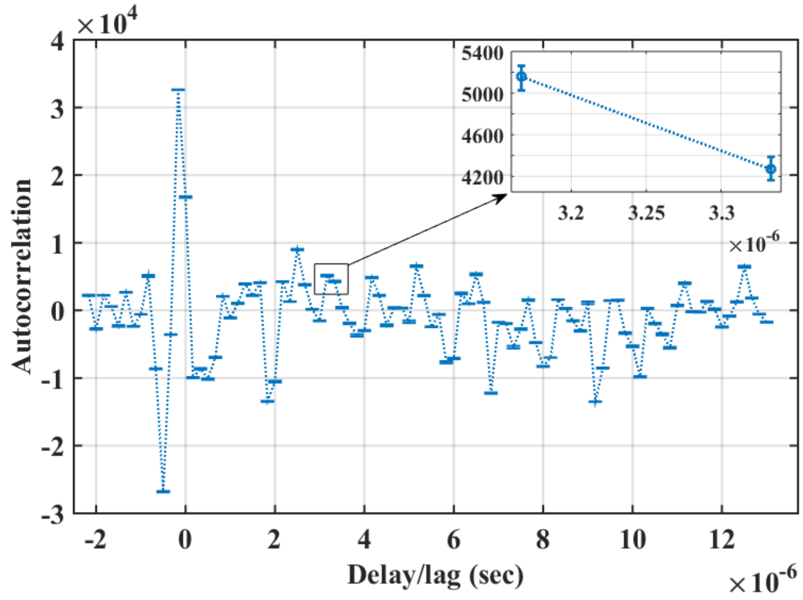
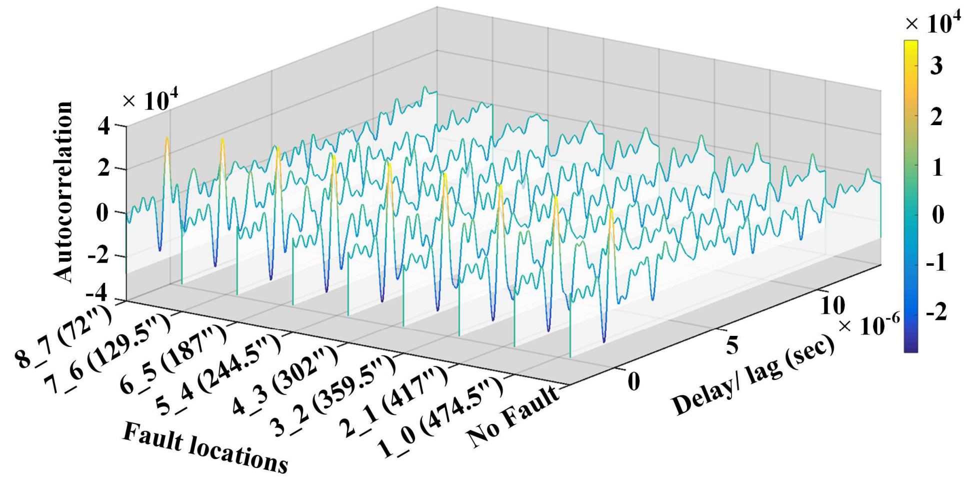


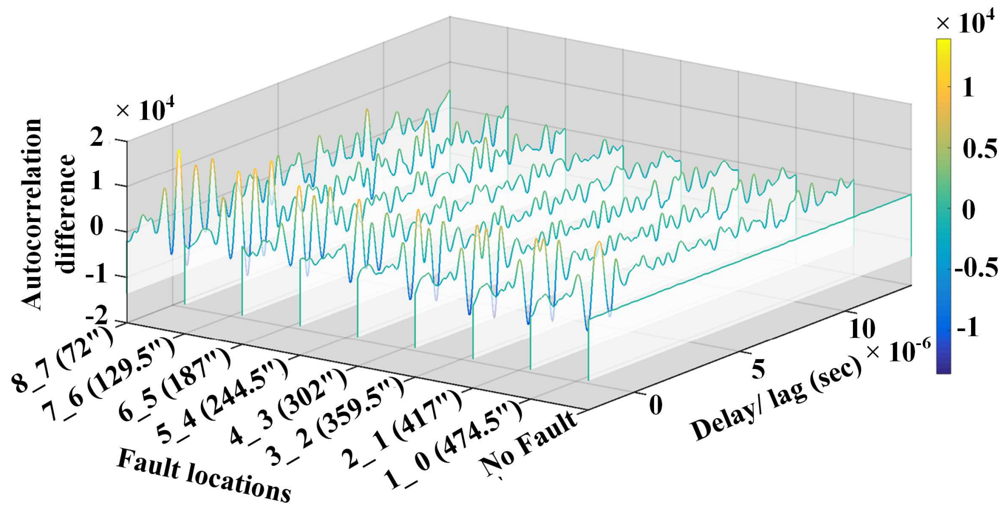
Figure 6.5 Error plot of autocorrelation data for center frequency of 750 kHz.

6.1.3 Fault Detection

Artificial ground faults were created at different nodes between the modules using a 0.5-Ω fuse to validate the fault detection algorithm. The PV string was scanned *N* times with ground faults at different nodes, as shown in Fig. 6.2, and the average autocorrelation plots (C_t) were generated for faults at different locations in the PV string. The absolute values of the element-wise differences between the average autocorrelation plot with ground fault in a specific location and the baseline were calculated, and the sum of these absolute differences has been termed as the "area" in this manuscript. The area (*A*), as defined in (6.3), for ground faults at different locations in the same PV string along with the system noise is shown in Fig. 6.6 for a center frequency equal to 750 kHz, and it was apparent that the PV array generates



(a)



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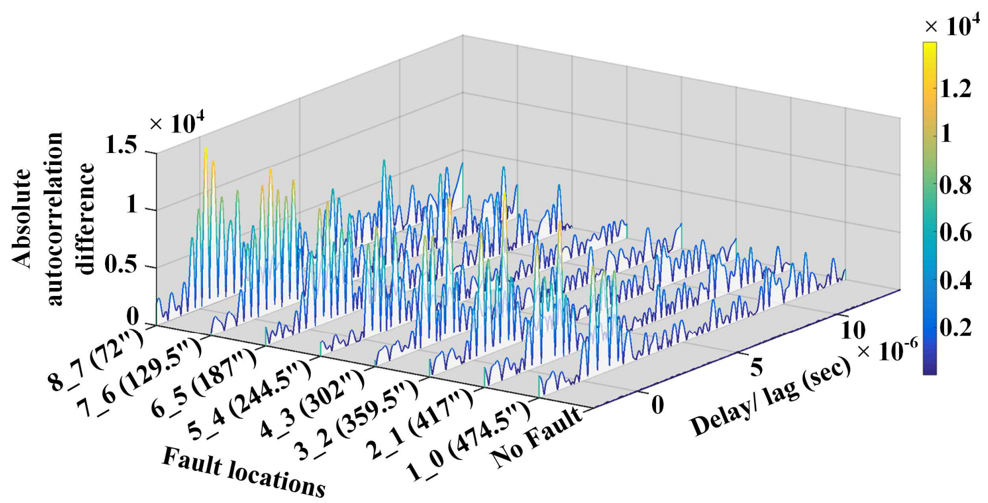

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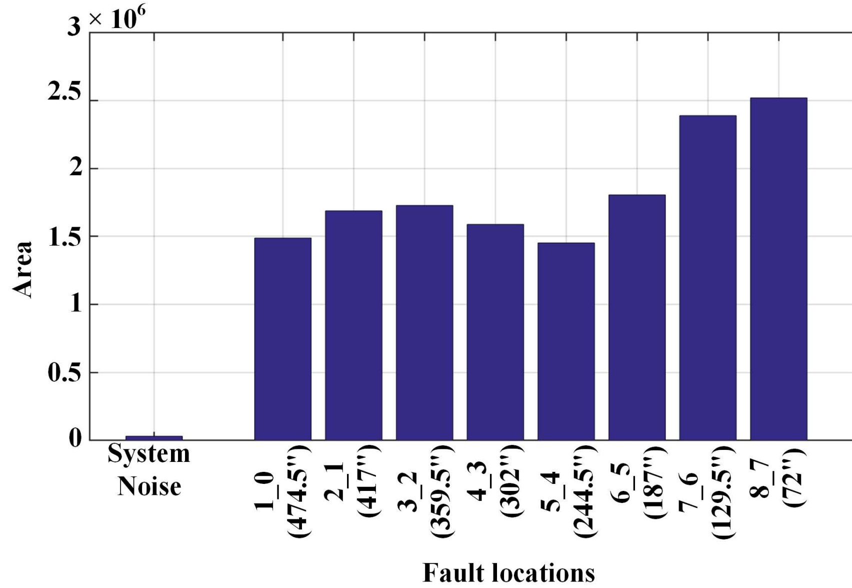


(d)

Figure 6.6 (a) Average autocorrelation plot using the same PV string without any ground fault and ground fault at different locations, (b) differences between average autocorrelation data and the baseline, (c) absolute values of the differences, (d) sum of absolute values of the differences.

an area that is higher than the last updated system noise whenever there is a ground fault in the array.

$$Area = \sum_{i=1}^{k} | C_{t,i} - C_{b,i}| \tag{6.3}$$

6.2 Impact of Different Parameters on Ground Fault Detection Algorithm

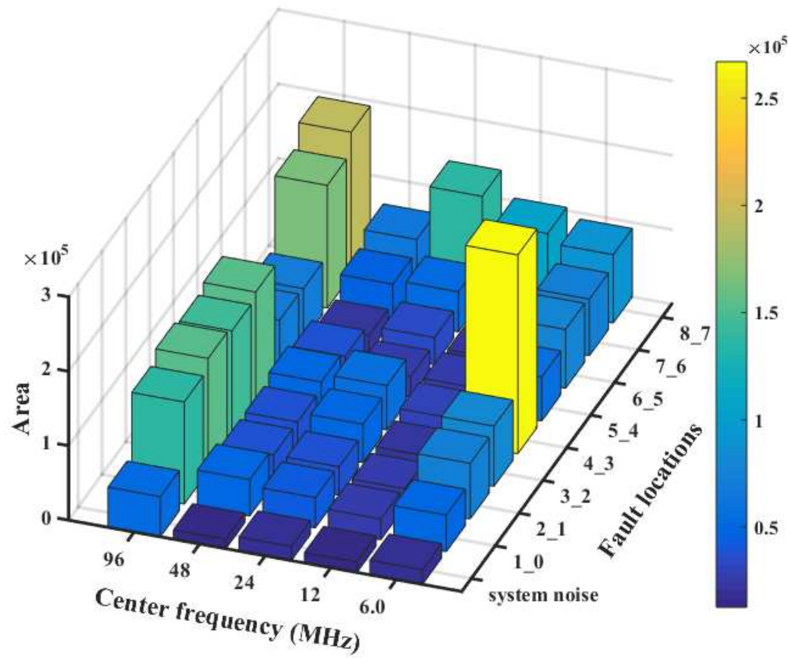
The autocorrelation data in an SSTDR-based fault detection method depends on numbers of parameters that affect the impedances (either Z_0 or Z_L) in the propagation paths of SSTDR signals. For instance, the number of connected strings (series or parallel), number of simultaneous faults, fault resistance, number of interconnections within the system, impedance variation throughout the array, PV cell material, metal conductors and frames of the PV module, and method by which SSTDR hardware is connected with the PV array, etc., lead to complex distributed capacitances and other parasitic components between the CCC and the

ground. Since the algorithm is based on the differences between the average autocorrelation readings for the healthy and faulty PV array, the parameters that remain unchanged in both the healthy and faulty PV arrays, have little or no impact on the fault detection capability of the proposed algorithm. Moreover, the attenuation of the SSTDR signal depends on its velocity of propagation, distance to the fault, characteristic impedances of its propagation path, the length of the PN code, center frequency, etc. [34]. Unfortunately, quantifying the impact of these parameters as well as the attenuation of SSDTR signal (where a large number of impedance variations and branch network is present throughout the PV array) is beyond the scope of this research. The influence of different parameters, i.e., the center frequency of SSTDR, fault resistance, solar irradiance, parallel strings, and double ground fault on the robustness of the algorithm are discussed the following subsections.

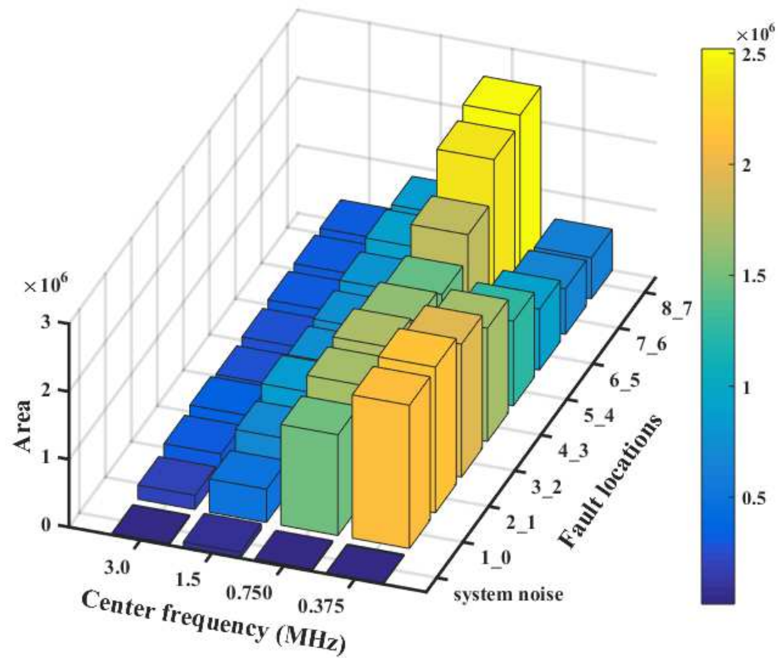
6.2.1 Impact of Carrier Frequency

The spectral distribution of the signal is highly dependent on the center (carrier) frequency because the generated PN code and the chip rate of the PN code vary in proportion to the center frequency [37]. The width of the main lobe of the Fourier transform of the incident signal is twice the center frequency, and most of the energy of the incident signal is confined within that bandwidth. The power density of the incident signal spreads over a wider bandwidth with an increase in center frequency, and thereby, the response (reflected signal) is expected to vary with the variation in the center frequency.

The area under the absolute average autocorrelation difference plots for the same PV string with ground faults at different nodes (for different SSTDR carrier frequencies) and fault resistance equal to 0.5-Ω are shown in Fig. 6.7. Since the lower frequency signals travel further into the system, and the SSTDR signals need to propagate through both long cables and (lossy)



(a)



(b)

Figure 6.7 Area under absolute autocorrelation difference plots for healthy PV string (system noise) and ground faults at different locations in the PV string using 0.5-Ω resistor with different center frequencies: (a) center frequencies from 96 to 6 MHz and (b) center frequencies from 3 to 0.375 MHz.

PV modules, center frequencies lower than 6 MHz produce more reliable results compared to higher center frequencies for ground faults in the PV string. As an example, in Fig. 6.7 (a), the area with ground fault at location 6_5 is lowest and it is only 1.29 (approx.) times the system noise for a center frequency equal to 96 MHz. For 6, 3, 1.5, 0.7, and 0.375 MHz, these ratios are about 2.5, 7.96, 5.54, 48.04, and 31.89, respectively.

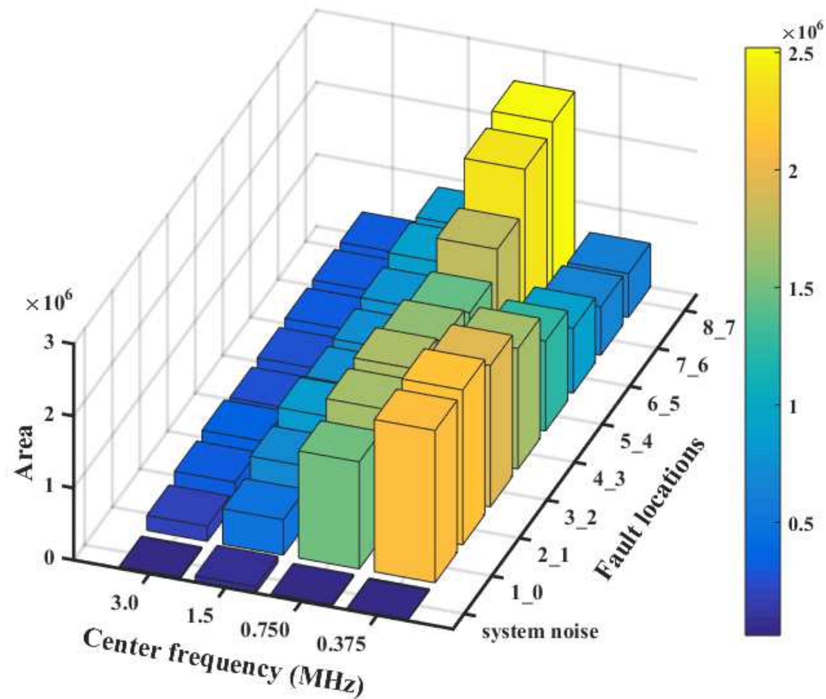
An extensive impedance domain mapping is required to explain the pattern of variation in areas at different locations. However, we decided to concentrate on the center frequency range of 375 kHz–3 MHz so that no erroneous fault is detected by the system.

6.2.2 Impact of Fault Resistance

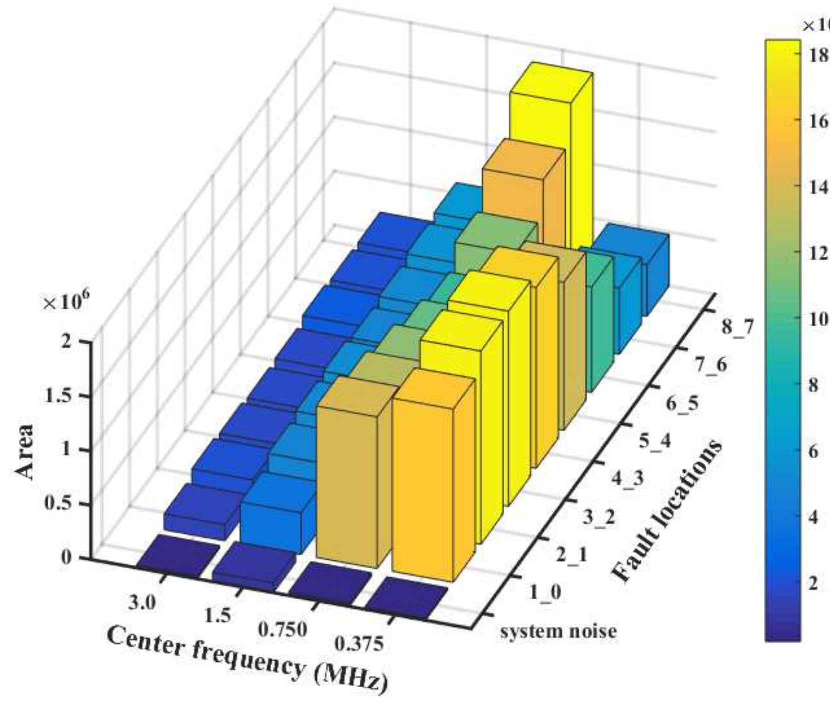
The ground-fault resistance is an important aspect in a fault detection scheme since it may create a fault within the blind spot of the GFDI fuse. Ground faults usually range from tenth of an ohm to tens of kiloohms depending on the reason behind the onset of the fault [59]. High-resistance faults may happen due to corrosion bridge or insulation failure, and their impedance degrades over time. Moreover, high-impedance fault current may not be high enough to cause significant damage to the system and may easily go undetected. In fact, the fault current of lower magnitude under low irradiance level, which might go undetected, can be high enough to cause catastrophic damage due to added current of subsequent faults. In contrast, low-resistance fault increases the current through the fault path, which eventually increases the possibility of a fire. Moreover, the high-resistance fault current remains almost the same at different irradiance levels, whereas current in low-impedance fault path linearly changes with higher irradiance making the fault detection even more critical [59]. Therefore, within the scope of this research, low-resistance ground faults were created at different locations in the PV string for the following fault resistances: 0.5, 5, and 10-Ω. The

autocorrelation area plots for different fault resistances and center frequencies (375 kHz–3 MHz) are shown in Fig. 6.8. The same baseline and system noise were used for all fault resistances since these two parameters (baseline and system noise) are independent of the fault resistance. A healthy PV string has a very high resistance from any point on the CCCs to the EGC (greater than the fault resistances), which will lead to the value of reflection coefficient, ρ less than 0 (zero) [from (3.2)]. Therefore, it is expected that the area under the autocorrelation plot will decrease with the increase in fault resistance for the same center frequency and fault location.

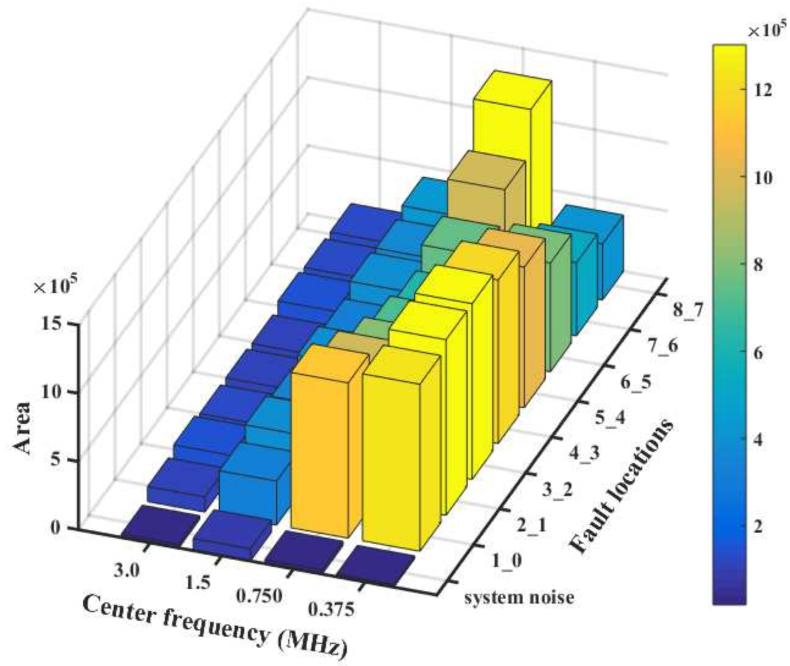
The experimental results revealed that the overall area under the curve typically decreases once the fault impedance goes up. As an example, the area corresponding to the center frequency equal to 0.75 MHz and fault location 5_4 decreases from 1.451×10^6 for 0.5-Ω to 0.9529×10^6 for 5-Ω, and then, to 0.6221×10^6 for 10-Ω fault resistance. Even at 10-Ω



(a)



(b)



(c)

Figure 6.8 Area plots for center frequencies 3.0, 1.5, 0.75, 0.375 MHz and fault resistances: (a) 0.5-Ω, (b) 5-Ω, (c) 10-Ω.

fault impedance, the area under the curve was 20.59 times higher than the system noise of 0.9529×10^6. This indicates that the proposed algorithm can detect faults even with a very high fault impedance. The travel paths of SSTDR incident and reflected signals are different for faults at different locations, and the propagation velocity throughout the PV string can be different too. Therefore, the position of the autocorrelated amplitudes, and thus, the autocorrelated area will be different for different locations. That being said, the experimental results summarized in this section conclude that the presence of a ground fault can be confidently detected for center frequencies less than 6 MHz regardless of the fault resistance (0.5, 5, and 10-Ω).

6.2.3 Impact of Parallel Connected Strings

In a larger PV array, multiple PV strings are likely to be connected in parallel, and it may not be feasible to disconnect all the parallel strings for ground-fault detection purposes. To verify the algorithm, two PV strings were connected in parallel at the same facility and ground faults were created at different interconnecting nodes in one of the PV strings using a 0.5-Ω resistor, as depicted in Fig. 6.9. Baseline autocorrelation plots for single string and two parallel strings without any ground faults are shown in Fig. 6.10 for center frequency 1.5 MHz. Since the SSTDR propagation path impedances for a single string and two parallel strings are different, there are some differences observed between these autocorrelation plots. Ground faults were created in one of the parallel strings, and area plots for different center frequencies (0.375–3 MHz) are shown in Fig. 6.11.

In every fault condition, the area plot height is significantly higher than the system noise (no-fault). Therefore, it can be concluded from the 3-D bar plot that SSTDR can be used for ground-fault detection in parallel-connected PV modules as effectively as in a single PV

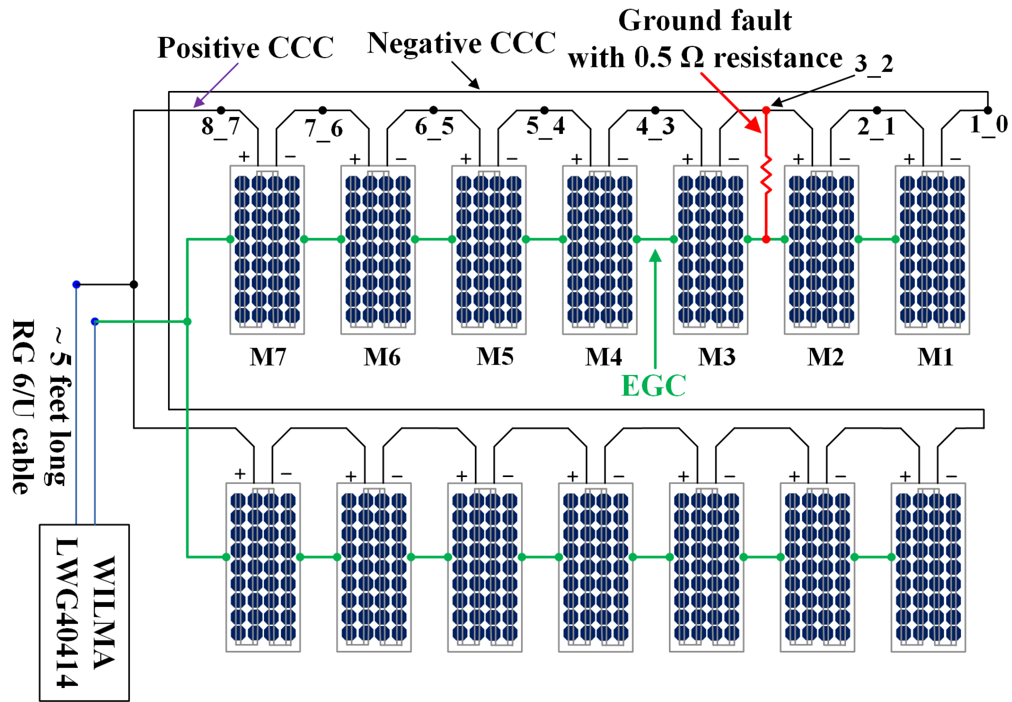


Figure 6.9 Schematic diagram of the test setup for two parallel strings.

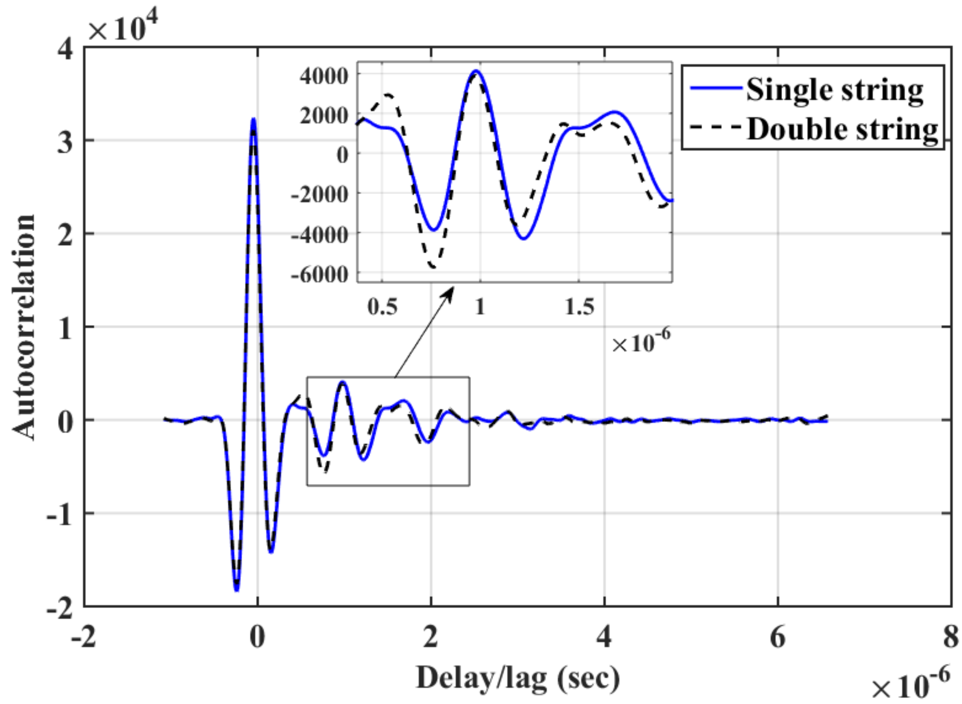


Figure 6.10 Comparison of baseline autocorrelation plots for single string and double string.

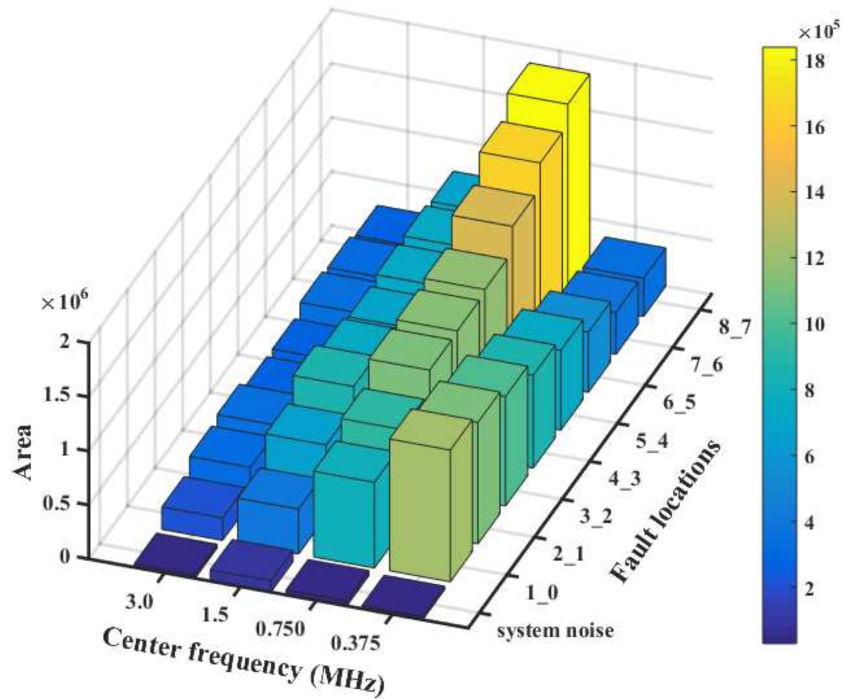


Figure 6.11 Area plot for PV array consists of two parallel strings with and without ground faults.

string. Moreover, the location of the faulty string using SSTDR can also be determined, since the algorithm can detect the ground fault in parallel-connected strings, and each string can be tested with respect to its own baseline by disconnecting the parallel connection to detect ground faults after a ground fault has been observed in the array.

6.2.4 Impact of Solar Irradiance

Change in the solar irradiance leads to nominal changes in the electrical equivalent impedance of the solar cells and this change in the impedance works in favor of the reflectometry-based fault detection schemes. In order to investigate the feasibility of ground fault detection using SSTDR at night or with low irradiance, a test was performed in a laboratory environment (<5 W/m^2 solar irradiance) with a PV string consisting of seven 100-W series-connected PV modules. Table 6 contains the specifications of the PV modules under test. A test setup similar to the schematic shown in Fig. 6.2 was built, and ground faults were

Table 6 Specification of a PV module used in the laboratory environment (at 1000 W/m^2, 25 cell temperature)

Maximum power (P_{max})	100 W
Short circuit current (I_{sc})	5.75 A
Open circuit voltage (V_{OC})	22.5 V
Maximum power current (I_{pmax})	5.29 A
Maximum power voltage (V_{pmax})	18.9 V

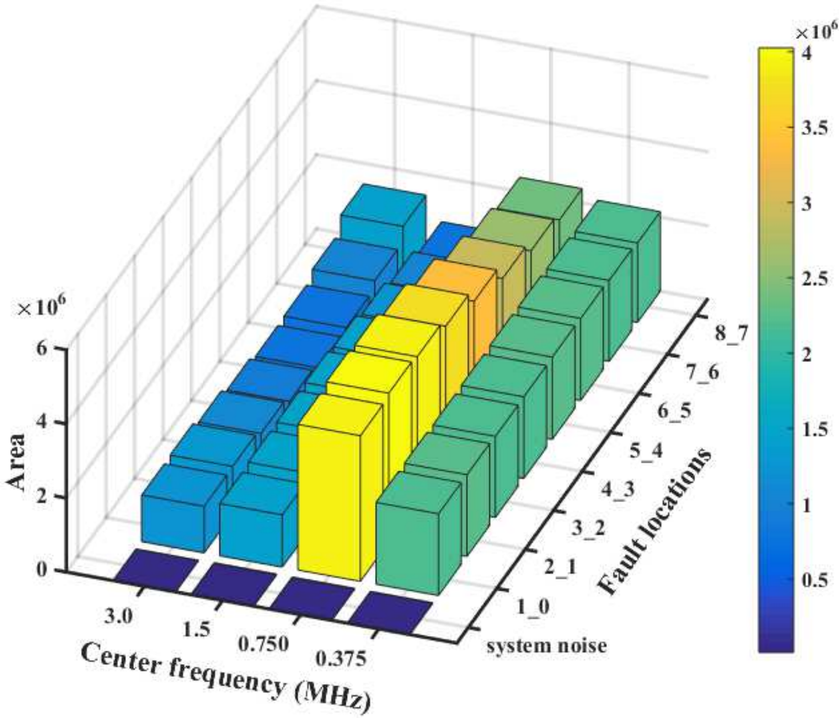


Figure 6.12 Area plot for PV string inside laboratory with and without ground fault.

created at different nodes of the PV string by creating a short-circuit connection. Similar tests were performed as described in Section 6.1 and the results are shown in Fig. 6.12. It is worth mentioning that the PV modules used in the laboratory environment were smaller than the outdoor PV modules described in Section 6.1. Therefore, the equivalent lumped impedance parameters (*R', L', C', and G'*) of both the indoor and outdoor modules are different leading

them to have different patterns for the same center frequency. However, it can be concluded from Fig. 6.12 that the proposed algorithm can detect ground faults at night or low illumination as confidently as at regular illumination.

6.2.5 Double Ground Fault

Due to the blind spot of the detection device during the night, a ground fault remains undetected and a second ground fault occurs which can be very devastating. The proposed technique could be successfully used in a double ground fault situation. A double ground fault test was carried out using the same PV string described in Section 6.2.4 inside the laboratory facility since double ground fault creation in an outdoor PV string is not safe and could set fires. During the indoor experiment, two short circuits were created at 8_7 and 6_5 (arbitrarily chosen locations) positions, and the PV string was scanned using the SSTDR hardware. The

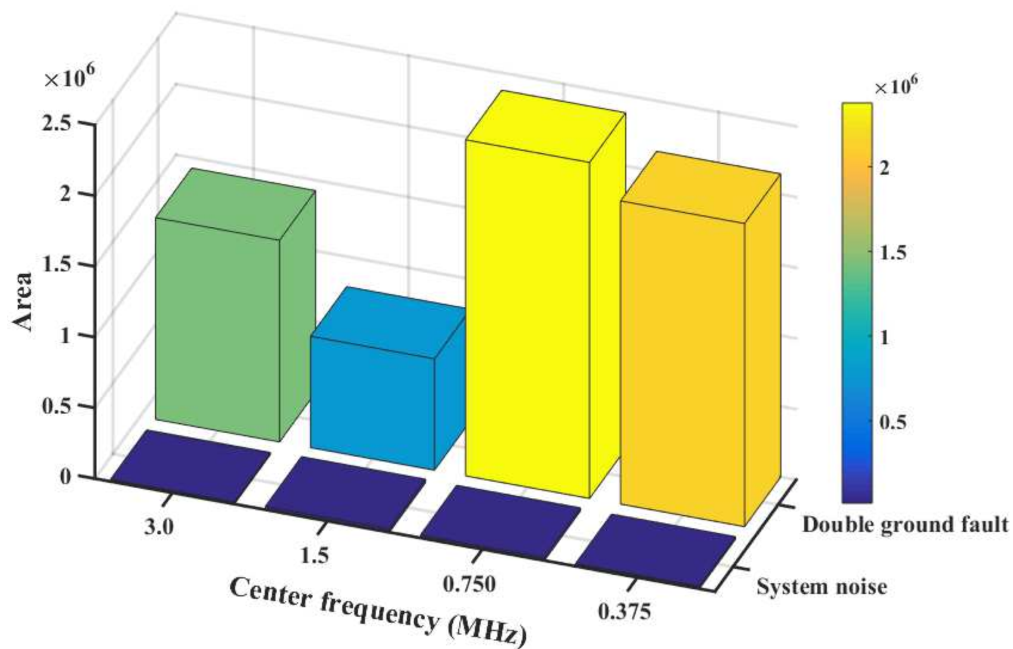


Figure 6.13 Area plot for PV string with and without double ground fault for different center frequencies.

results are shown in Fig. 6. 13 which shows that a double ground fault generates a higher area under the absolute autocorrelation difference plot than the system noise and can be detected confidently using SSTDR.

6.3 Conclusion

A novel SSTDR-based ground-fault detection algorithm has been presented in this chapter. Detection of ground faults in PV arrays using reflectometry is challenging because hundreds of interconnections and impedance mismatches exist inside a single PV string. The proposed algorithm has been successfully used for detecting ground faults in PV arrays. Moreover, this technique can be implemented for testing ground faults at night or at low illumination, i.e., when the PV array is expected to generate no power. This unique feature makes the proposed technique extremely powerful and effective compared to any existing methods. This paper has presented the feasibility of using the SSTDR-based algorithm with any variation in the number of strings, fault resistance and number of faults, and the proposed method can effectively detect complex fault conditions as well. Based on the finding through various research projects pertinent to SSTDR, it is expected that this SSTDR-based fault detection scheme will create a new standard in the power engineering community.

CHAPTER 7

7 DETECTION OF DEGRADED/AGED CELL IN A LI-ION BATTERY PACK USING SSTDR

This chapter presents a cell-level state of health (SOH) measurement technique based on spread spectrum time domain reflectometry (SSTDR) that can identify the location and amount of aging of the degraded cell in a large battery pack. Variations in SOH of the lithium-ion (Li-ion) cells in a series-parallel connected battery pack are unavoidable because of the manufacturing tolerances and non-uniform operating conditions. As a result of this, uneven SOH in the cells connected in a series-parallel combination can lead to affect the performance of the entire battery pack. Therefore, cell level SOH along with the respective cell location is a crucial metric for the battery management system (BMS) to predict the remaining useful lifetime (RUL) of the entire battery pack. Today's BMS considers the SOH of the entire battery pack/cell string as a single SOH and therefore, cannot monitor the SOH at the cell level. A healthy battery string has a specific internal impedance between the two terminals, and any aged cell in that string will change the impedance value. Since SSTDR can characterize the impedance change in its propagation path along with its location, it can successfully locate the degraded cell in a large battery pack.

7.1 Experimental Set-up for Locating Aged Cell in a Series Connected Battery Pack

The specifications of the Li-ion cell under test are already given in Table 2 (Section 4.2 of Chapter 4). Six of such Li-ion cells were connected in series and the SSTDR hardware was connected to the positive and negative terminals of this series connected 6-cell battery pack as shown in Fig. 7.1. Each cell is denoted as C_{i_j} where the subscripts i and j denote the

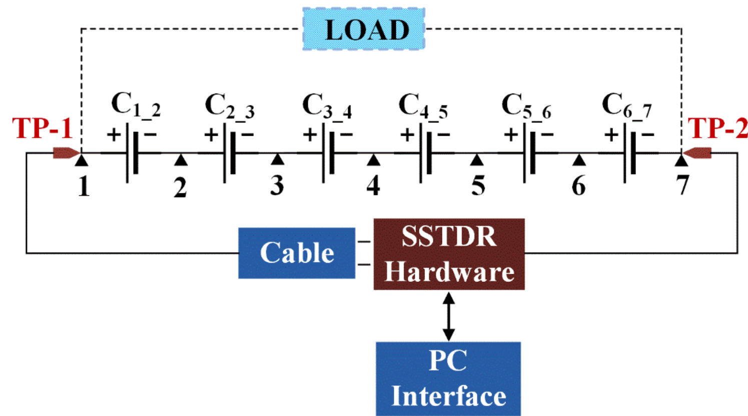


Figure 7.1 SSTDR hardware connected with a series-connected battery string of 6 (six) Li-ion cells.

corresponding adjacent node numbers. Throughout this dissertation, the location of each cell, C_{i_j} will be denoted as location-i_j. The SSTDR hardware used in this experiment can generate SSTDR signals with carrier frequencies from 375 kHz to 48 MHz. The distance resolution of the autocorrelation increases with an increase in carrier frequency, and since the distance between two adjacent cells in battery pack is very small, we select two highest available carrier frequencies such as 48 and 24 MHz to conduct these experiments.

7.2 Location Detection of Individual Aged Cells Using SSTDR

It is to be noted that every battery string has different reflection patterns, and it is necessary to create a baseline for each string (when all cells are healthy) under consideration. This baseline will act as a reference to detect the location of an aged cell. To create this baseline, the entire battery string with all new/healthy cells was scanned in static mode 10 times, and autocorrelation plots were interpolated at the rate of 10 in MATLAB. These 10 readings (auto-correlated data) were averaged and denoted as the baseline, S_b. After creating the baseline, each new cell at location-1_2, location-3_4, and location-4_5 in the string was replaced by an aged cell, ***one at a time***. For instance, the battery string with an aged cell at location-1_2 (the

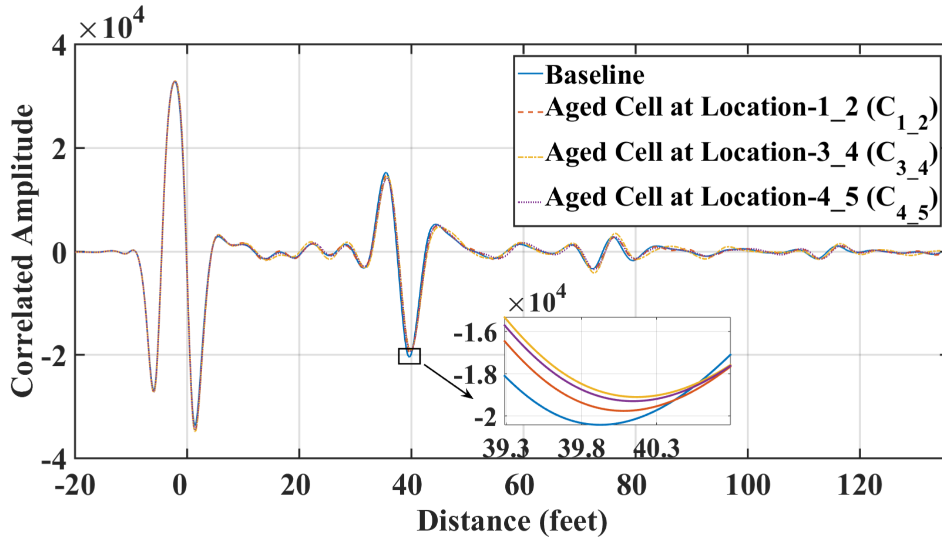


Figure 7.2 Variation in correlated amplitudes for healthy battery string and battery string with an aged cell at different locations (for a 40 feet long cable connected to the string).

remaining five cells were new/healthy) was scanned 10 times and the generated auto-correlated data was averaged. The same test procedure (scanning the string 10 times) was carried out for aged cell at locations 3_4 and 4_5. Fig. 7.2 shows the autocorrelation data for healthy battery string as well as the autocorrelation data for battery string with an aged cell at different locations (one at a time), and we can clearly distinguish the average autocorrelation peak response of a battery string with a single aged cell. Since the distances between two adjacent aged cells are less than the blind spot error distance, it is impractical to detect the location of the aged cell based on the location of the autocorrelated peak amplitude. Blind spot error occurs when the two adjacent impedance mismatches are less than a minimum distance resolution because of the small-time delay [34].

7.2.1 Proposed Algorithm

To overcome this limitation, similar to the algorithm developed for PV array fault detection, a robust algorithm has been developed to locate the aged cells in a series-connected

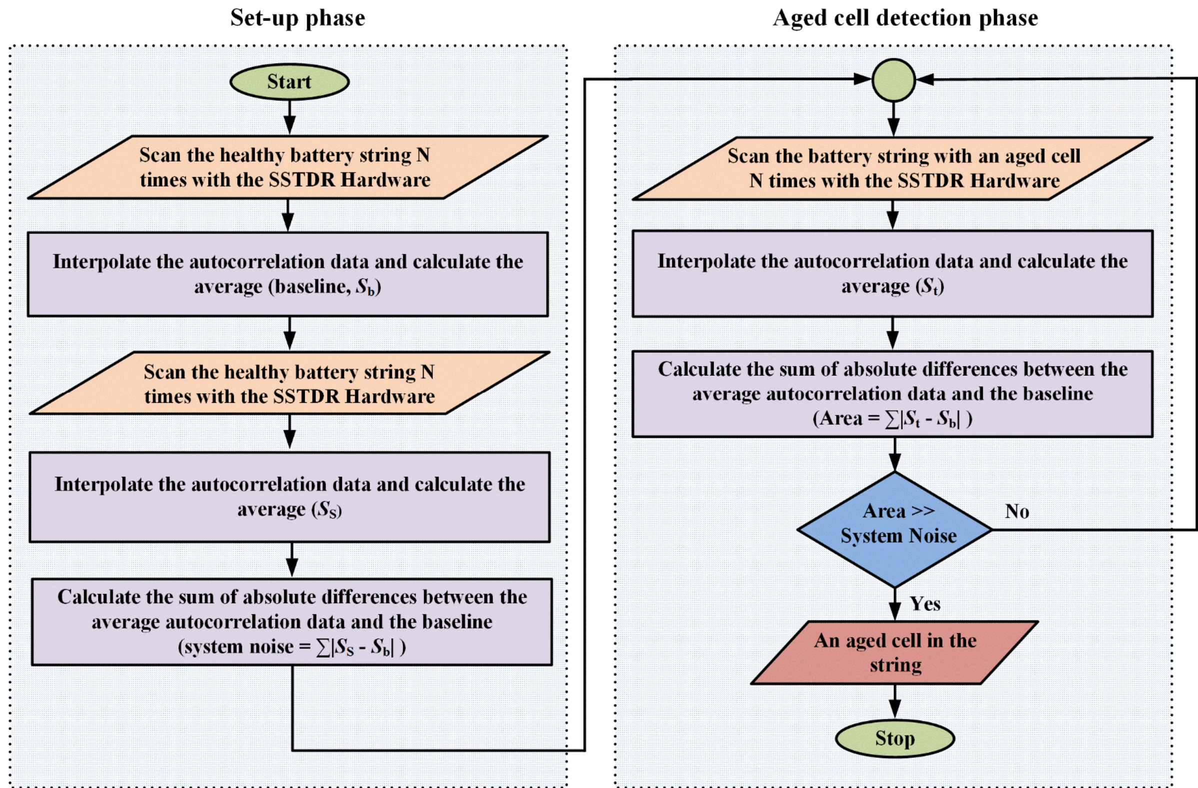


Figure 7.3 Flowchart of the proposed algorithm for aged cell detection in a large battery pack using SSTDR.

battery string. The algorithm developed within the scope of this research is described in the following paragraphs, and a flowchart of this algorithm is shown in Fig. 7.3.

The autocorrelation data generated by the same healthy battery string show some variations due to thermal noise, hardware error, connection error, noise generated from the ADC, etc. Considering these factors, the same healthy battery string was scanned 10 times, and the autocorrelation data were interpolated and averaged (S_s). Each baseline data point calculated in the previous subsection (S_b) was subtracted from the calculated average data, and the absolute values of the differences were considered. The sum of the absolute differences between the average SSTDR autocorrelated data (S_s) and the baseline (S_b) is considered as an

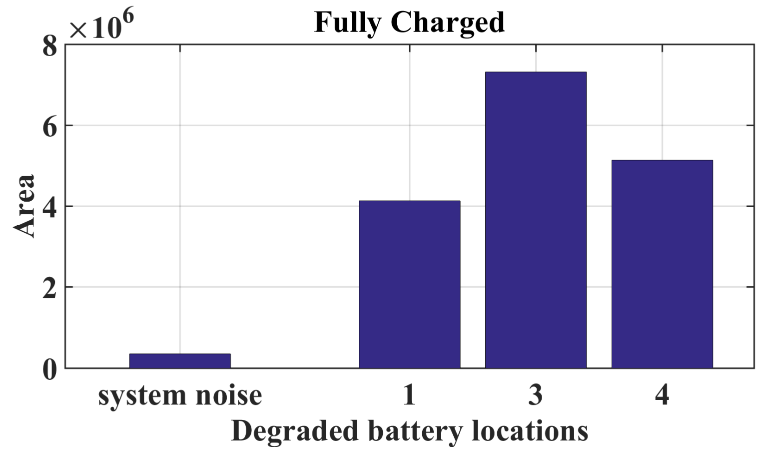
estimate of system noise (N_s) as shown in (Eq. 7.1) since both values were collected for the same healthy battery string.

$$N_s = \sum_{i=1}^{k} |S_{s,i} - S_{b,i}| \quad (7.1)$$

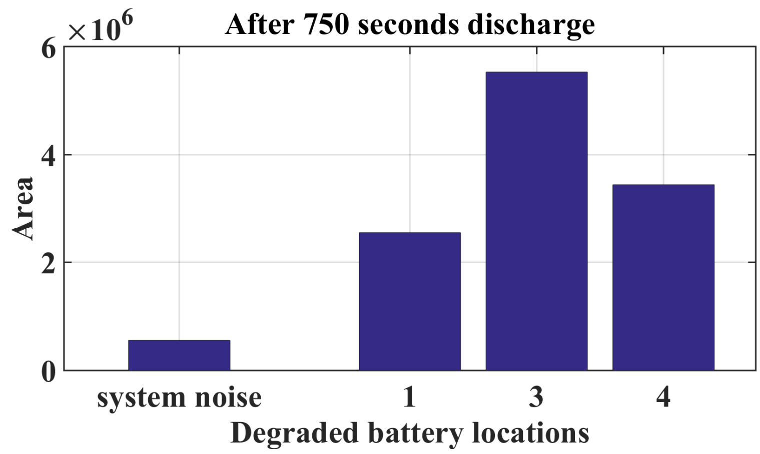
Here, k represents the length of the auto-correlated dataset, and the subscript i represents the i-th element of the corresponding dataset. In a similar way, the sum of the absolute differences between the average auto correlated plots for the battery string with an aged cell at different locations (S_t) and baseline (S_b) was calculated and coined as 'area' (Eq. 7.2), and this area quantifies the amount of reflected signal from the aged cell.

$$area, A = \sum_{i=1}^{k} |S_{t,i} - S_{b,i}| \quad (7.2)$$

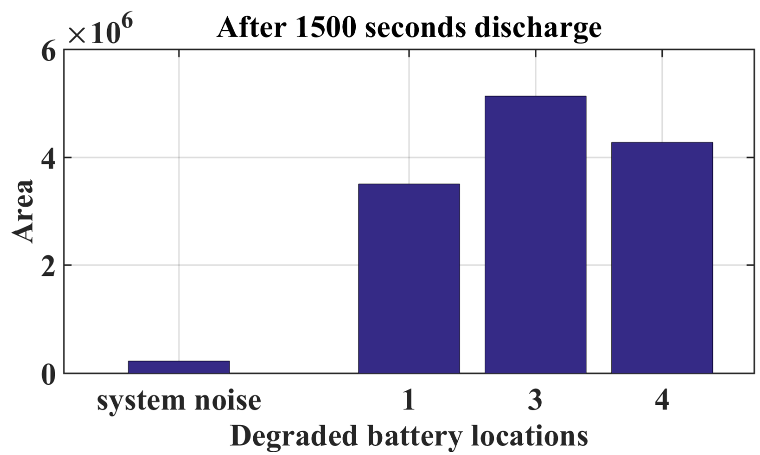
The area, defined in (7.2), for the battery string with an aged cell at different locations along with system noise has been shown in Fig. 7.4 and Fig. 7.5 for 48 and 24 MHz SSTDR center frequency, respectively. SSTDR data has been taken for three different battery SOC conditions: (a) battery string fully charged, (b) battery string discharged for 750 seconds, and (c) battery string discharged for 1500 seconds. From these plots, it is apparent that the area (A) generated by the battery string with the aged cell at different locations is higher than the system noise, thus validating the analysis. Moreover, the auto-correlated area meaning the amount of reflections for the aged cell at different locations is different, and it follows a consistent pattern. The overall area under the curve or, the total amount of reflected signal for the aged cell at location 1_2 is less than the other two areas. However, the reflection from the aged cell at location 3_4 is higher than the reflection from the aged cell at location 4_5. The explanation of this phenomenon yet to be done which needs to extract the exact transmission-line model parameters of the battery pack. However, the presence of multiple reflections occurring at different mismatches inside a battery pack makes the extraction of the exact transmission-line



(a) fully charged

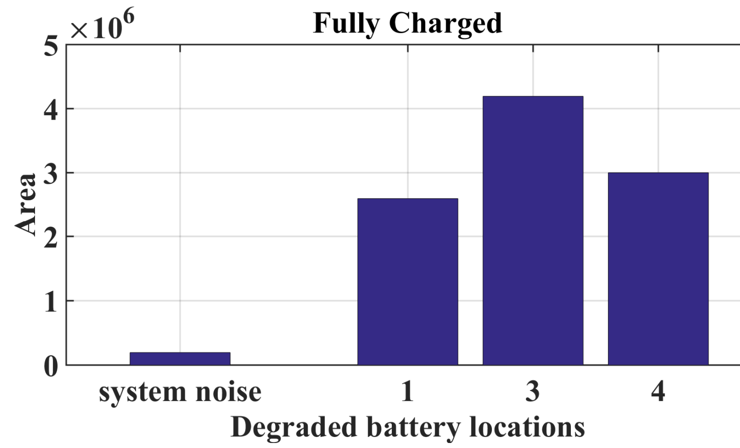


(b) 750 seconds discharged

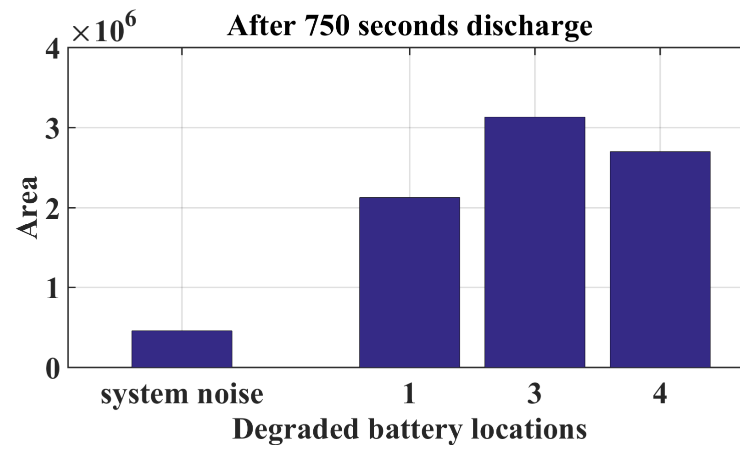


(c) 1500 seconds discharged

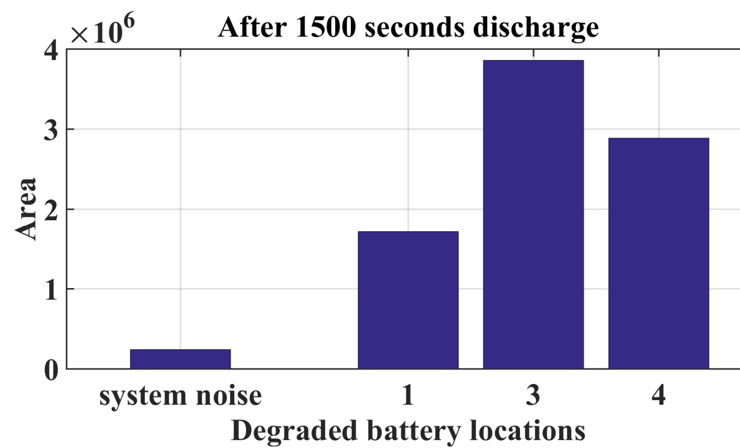
Figure 7.4 Area plots for the battery string with aged cell at different locations along with system noise for 48 MHz center frequency under different SOC conditions.



(a) fully charged

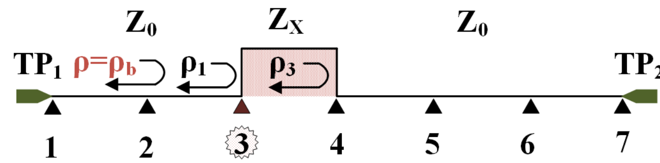


(b) 750 seconds discharged



(c) 750 seconds discharged

Figure 7.5 Area plots for the battery string with aged cell at different locations along with system noise for 24 MHz center frequency under different SOC conditions.



Aged cell at location 3_4

Figure 7.6 Impedance discontinues in SSTDR propagation path for aged cell at location 3_4.

model parameters and hence the interpretation of the time-domain reflection extremely difficult. For example, Fig. 7.6 shows the conceptual schematic diagram including the impedance discontinues in the SSTDR propagation path for an aged cell at location 3_4. Please note that this simplified impedance diagram was built considering: (i) the algorithm is based on the differences between the baseline and the area for an aged cell at different locations and (ii) multiple interconnections such as metal conductors and frames of the cells, SSTDR cables, and many more interconnections have been ignored. Here, the characteristic impedance of a healthy cell is considered as Z_0 and that of an aged cell is considered as Z_x ($Z_x>Z_0$ due to aging).

7.3 Conclusion

A new reflectometry-based technique has been presented in this chapter to detect the level of aging and location of a degraded cell in a series-connected Li-ion battery string. Existing battery health monitoring techniques can only determine the overall health of the string. In contrast, the initial results prove that SSTDR could be effectively used to solve this long-standing problem. Therefore SSTDR based cell level SOH measurement can be an excellent add-on feature for a BMS to guarantee the safety and reliability of the entire battery system.

CHAPTER 8

8 DYNAMIC SAFE OPERATING AREA (SOA) OF POWER SEMICONDUCTOR DEVICES

This chapter investigates the effect of aging on the safe operating area (SOA) of a power semiconductor device. SOA is a critical parameter to design a power converter circuit, and it indicates the robustness of the device. It defines the I–V boundary in which a power semiconductor device can be safely operated [2]. The mean time to failure (MTTF) represents the expected lifespan of the device although it cannot adequately predict the failures. During abnormal operating conditions, a power electronic circuit may experience high-voltage and high-current beyond normal operating values. As of today, the SOA of a device is conservatively chosen in a circuit meaning a certain percentage of headroom is initially allocated so that the power device may ride through accidental over-voltage/current situations before a complete failure (either short or open) takes place. In general, it is assumed that the SOA remains constant, and the overall reliability of the circuit simply becomes the probability of an abnormal condition to occur and the probability of other device failures. According to our study and experimental validation in our laboratory, SOA of any semiconductor device such as MOSFET goes down with the increased level of aging, and this observation explains why the reliability of an entire circuit exponentially drops with aging. For a long time, we knew the fact that MTTF decreases with the increased aging of the converter switches [1], but we never questioned why. However, the impact of aging on SOA is ultimately responsible for this time-dependent failure rate of a circuit. In a nutshell, by knowing the aging level, it is possible to estimate the dynamic or real-time SOA of a device, and thus, the overall reliability of the

circuit can be determined. By doing this, the scheduled maintenance can be performed more accurately, which is expected to reduce unwanted downtime.

8.1 A Case Study Showing How Reduced SOA Can Reduce Availability

A grid-connected converter circuit, as shown in Fig. 8.1, often experiences accidental over-voltage due to lightning and surges, different faults, inductive switching transients caused by switching OFF large inductive loads and/or energizing capacitor banks [132]. In addition, stray inductance in a circuit, as well as the device/circuit parasitic inductance, contribute to overshoot, ringing and impulsive over-voltages of power devices in switching applications [142]. For example, as shown in Fig. 8.2, despite having a sufficiently large dc-link capacitor, the supply line impedance along with the circuit/device stray and parasitic inductances cause considerable voltage spikes at the dc bus during inverter operation. These voltage spikes appear across the switches, and thus, these switches experience accidental over-voltage than they were

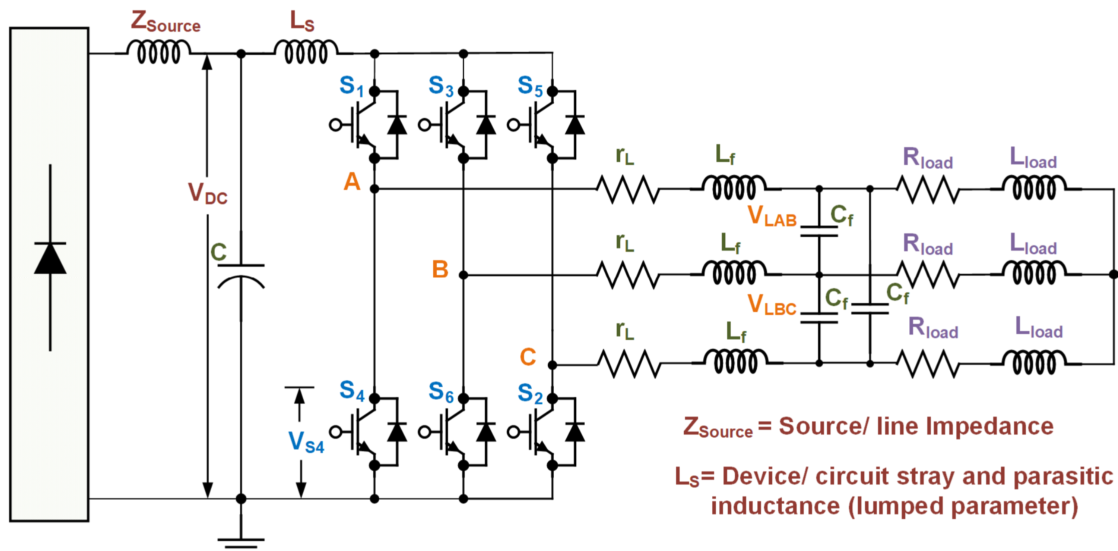


Figure 8.1 Schematic of a grid-connected three-phase voltage source inverter.

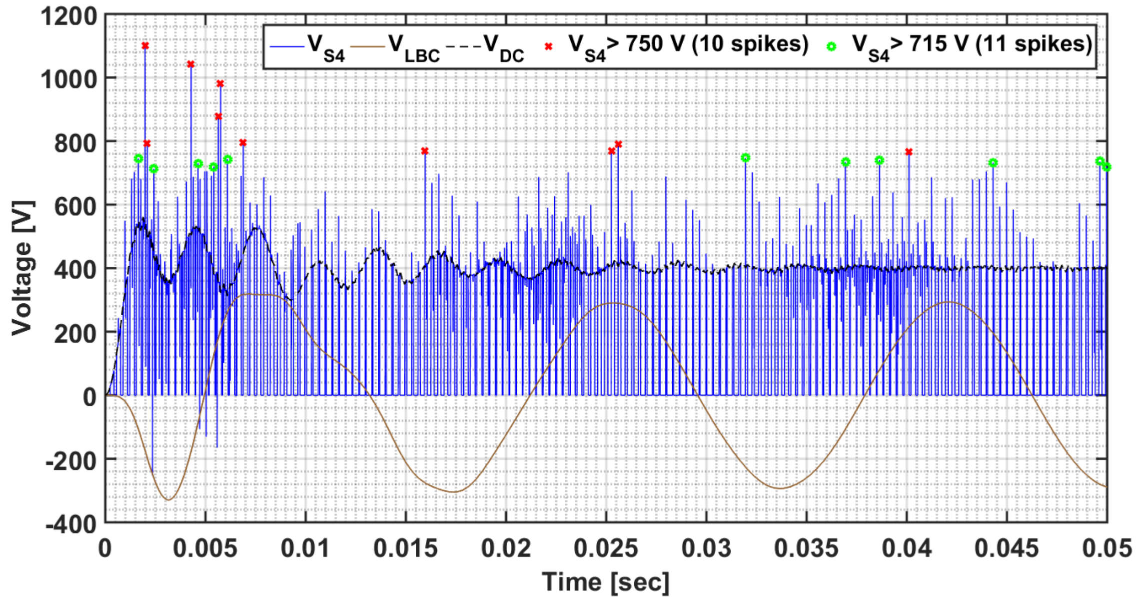


Figure 8.2 Simulation waveforms showing accidental overvoltage situations across switch S_4 of the three-phase inverter.

originally intended for. Interestingly, a healthy (new) switch may override multiple overstressed situations, but an aged device is less likely to do that since the SOA goes down with higher aging. For instance, let us consider a switch (S_4) with two aging conditions, and they have safe operating voltages of 750 V (healthy) and 715 V (aged), respectively. According to the simulation results in Fig. 8.2, switch S_4 experiences a considerable number of voltage spikes within three 60-Hz cycles. Twenty-one (21) of these incidents are higher than 715 V meaning they will exceed the maximum safe operating voltage of the aged device, whereas the healthy switch only experiences ten (10) overvoltage situations. Therefore, the probability of happening a failure is more than twice for an aged device.

8.2 The Relationship Between Aging and Dynamic SOA

8.2.1 Why Aging Reduces Maximum Safe Operating Voltage

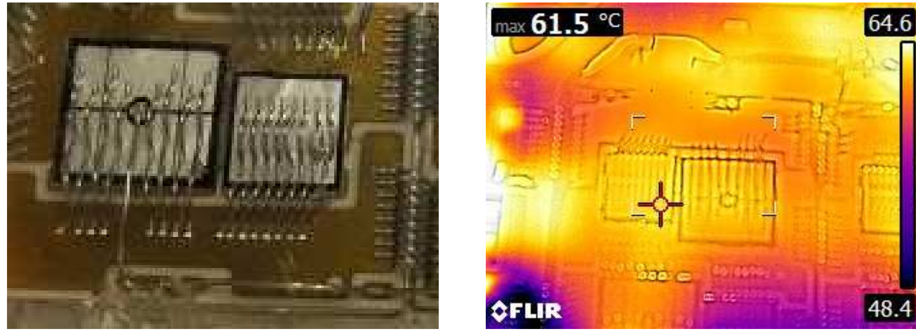
Power semiconductor devices are subjected to repetitive power and thermal stresses in normal operation. As shown in Fig. 2.2 of Chapter 2, cracks and voids in the die-attach layer

between the Si and Cu die and at the bond wire and chip interface are formed because of the differences in coefficient of thermal expansions (CTEs) in different materials/layers, resulting in the bond wire lift-off. Reduced number of bond-wires, cracks, and voids impede the heat dissipation throughout the device, and thus thermal impedance, as well as junction temperature will increase [7], [8], [90], [143]. Furthermore, an increase in the junction temperature could induce hot spots and excess heat in the affected areas of the power devices. This trapped heat will accelerate the cascading effect of impact ionization, which will reduce the device's safe operating voltage [90], [144]. Impact ionization is a carrier multiplication process by which more electron-hole pairs are generated due to strong Coulombic interactions between charge carriers when a reverse voltage exceeding the critical electric field is applied [145]. This process is cascaded very quickly in a chain-reaction-type manner, producing a large number of free electrons and thus a huge current. This huge current leads to the dissipation of a substantial amount of power across the device resulting in the destruction of the device. Moreover, localized electric field is increased in the device due to the cracks and voids formation that may lead to accelerated impact ionization as well.

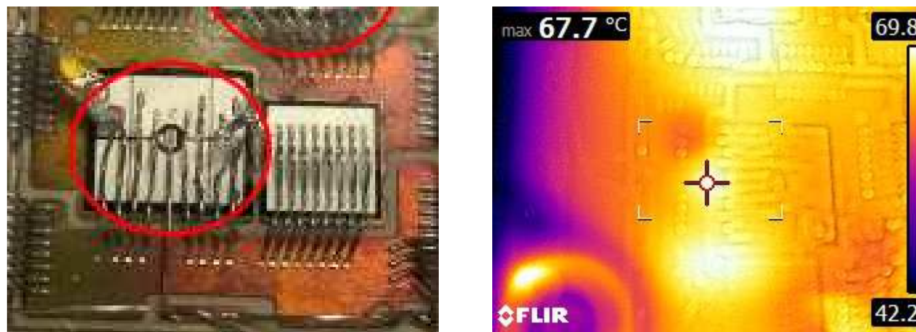
Besides forming voids, cracks, etc., other morphological surface defects such as initial solder microstructure, reconstruction of aluminum surface and substrate metallization, intermetallic compounds are formed while the device undergoes aging. According to [146]–[148], morphological and crystallographic surface defects can cause premature reverse breakdown due to the localized enhancement of electric fields.

8.2.2 Why Aging Reduces Maximum Safe Operating Current

The reduction in the maximum safe operating current can be understood from the bond wire lift-off-related aging in an IGBT module. Aging causes damage to bond wires and



(a) Healthy device



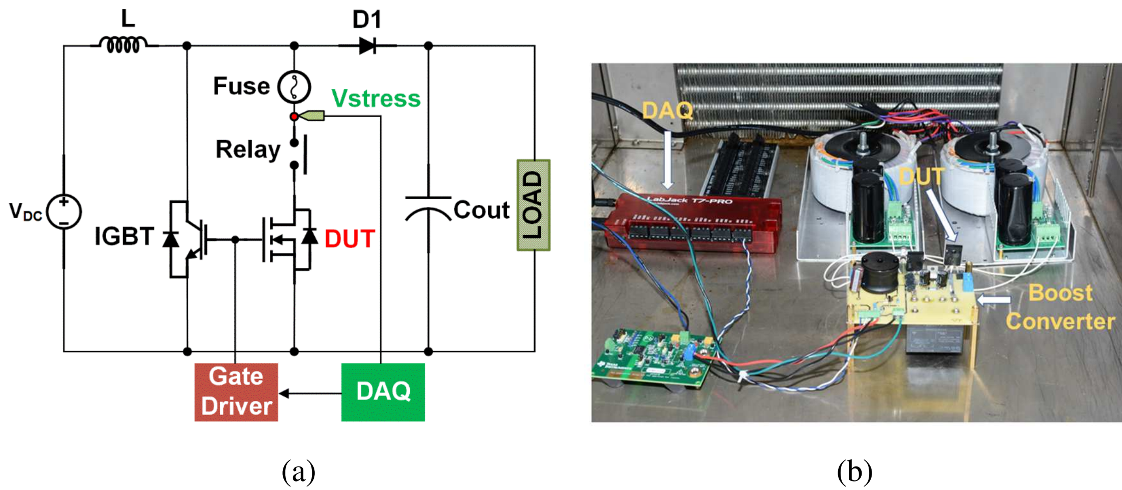
(b) Aged device

Figure 8.3 Bond wire lift off and corresponding current crowding. Test data generated by experiment. The red circle shows damaged bond wires.

introduces current crowding leading to a rise in the substrate temperature (shown in Fig. 8.3). The resultant fewer number of bond wires need to carry the rated current which is higher than that of a healthy module. Therefore, the rated current needs to be adjusted to a lower magnitude to keep the devices in a healthy state. Otherwise, this overstress situation will increase the likelihood of additional bond wire lift-offs, heel crack, and even cascaded device failure.

8.2.3 Experimental Set-up and Results: Characterizing Maximum Safe Operating Voltage as a Function of Aging

Fig. 8.4 (a) and 8.4 (b) show the schematic diagram and photograph of the initial experimental setup of the destructive test in order to characterize the device's maximum safe operating voltage as a function of aging. Voltage above the device's rated operating voltage



(a) (b)

Figure 8.4 (a) Schematic diagram and (b) photograph of the experimental set-up for maximum safe operating voltage determination

boundary was applied to induce damage, and it was done by placing the switch at the low-switch side of a boost converter with proper protection circuit (see Fig. 8.4 (a)). A 1200 V IGBT was used as a controller switch of the boost converter. The DUT was connected in series with a fuse and a relay (which is maintained normally open) and this combined branch was connected in parallel with the IGBT. The voltage stress above the rated operating voltage of 600 V (from datasheet) was applied on the DUT with an incremental step of 5 V by closing the relay. The relay was closed for 100ms at each voltage level. When the device enters the breakdown voltage region, a huge current starts flowing from the drain to the source, which is disrupted by the fuse to protect the overall converter.

Five healthy and four aged MOSFETs with known aging levels were tested. The MOSFETs were aged using the same active power cycling test described in Section 4.1 of Chapter 4. Using active power cycling, electro-thermal stresses were applied to four N-channel power MOSFETs (M_1, M_2, M_3 and M_4) with similar characteristics (600V-50A). The applied thermal gradients, number of power cycles and the resultant increase in the device ON-

Table 7 Summary of the accelerated aging parameters

MOSFET	ΔT (°C)	N_{Cycles}	$\Delta R_{DS(ON)}$
M_1	80 °C	13100	41.77%
M_2	80 °C	9525	40.72%
M_3	80 °C	6350	32.81%
M_4	110 °C	10667	55.19%

resistance ($\Delta R_{DS(ON)}$) are summarized in Table 7. After the destructive test using the boost converter, all of the MOSFETs, both healthy and aged, enter their breakdown region at levels significantly higher than their rated voltage. This is due to the fact that the power semiconductor device ratings are chosen conservatively meaning a power device may ride through several abnormal conditions. The corresponding experimental results have been shown in Fig. 8.5. The top line shows the variation in safe operating voltages for healthy MOSFETs and the bottom line shows the same for aged MOSFETs. It clearly shows that the aged MOSFETs suffer from early failures, and the variation in safe operating voltages (between healthy and aged MOSFETs) was close to 40 V. It is very likely that SiC MOSFETs

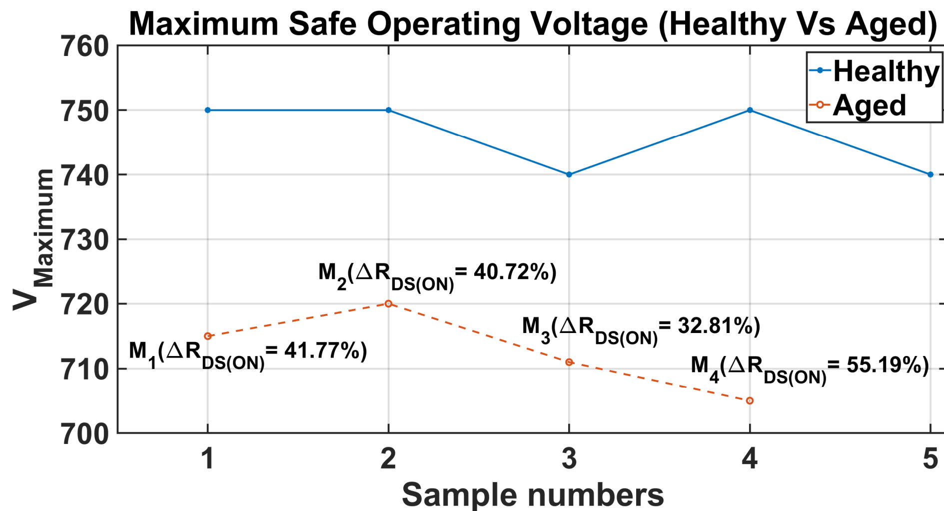


Figure 8.5 Experimental results showing reduced maximum safe operating voltage of an aged MOSFET, $V_{maximum}$= maximum safe operating voltage.

and Si IGBTs will exhibit similar patterns. Because of the limited availability of aged devices, the initial experiments were conducted only with Si MOSFETs, and the high cost of larger IGBTs was the underlying reason to limit this destructive test to Si MOSFETs only. However, a similar experiment could be conducted to understand the aging-dependent maximum current carrying capability of these devices as well.

8.3 Conclusion

This chapter demonstrated how the safe operating area (SOA) of power semiconductor devices is impacted by aging. The experimental results show that the SOA of a power semiconductor device goes down with aging, and this observation explains why the reliability of an entire circuit exponentially drops with degradation inside the device. Therefore, by knowing the level of aging, we can determine the dynamic SOA of the device and estimate the remaining life of it accurately, and this will allow for scheduled maintenance of any high-power converter. This capability will eventually enable us to reduce maintenance and operational cost by ensuring higher availability.

CHAPTER 9

9 CONCLUSION AND FUTURE RESEARCH

Finding the remaining useful life (RUL) of a power converter is the ultimate objective to ensure the uninterrupted operation of a power electronic system. This manuscript presents a comprehensive solution to determine the real-time state of health (SOH) and RUL of a power semiconductor device in a live power converter using an online in-situ, non-invasive technique based on spread spectrum time domain reflectometry (SSTDR) and the knowledge of dynamic safe operating area (SOA). We demonstrated that device degradation can be estimated by accomplishing an accurate online degradation monitoring tool namely SSTDR, which will determine the dynamic SOA. In addition, we presented proof-of-concept results demonstrating the SOA of a power semiconductor device goes down with aging, and this observation explains why the reliability of an entire circuit exponentially drops with degradation inside the device. Future work will focus on developing an accurate lifetime prediction model of the device by establishing the correlation between aging and dynamic SOA which can eventually determine the availability of a circuit. In fact, the overall availability of a circuit depends on the SOH of an individual component as well as the cumulative aging of all the components present in the circuit. Since different converter circuits impose a different number of over-current or over-voltage situations on their power devices, it is envisioned that an aged device with degraded SOA will exhibit a different probability of failures in different converter circuits. To be specific, the probability will depend upon available voltage and current headroom, nature of the circuit, type of the control loop, load variation, and so on. Another part of the future research, therefore, defines the relationship between dynamic SOA and the probability of occurring a failure for a specific circuit. So far, the experimental method to derive a correlation

between aging and dynamic SOA was limited to the destructive test of the power devices. However, to eliminate the effect of part-to-part/process variations within the test samples, maximum safe operating voltage measurement using the leakage current method will be carried out in the future. In this leakage current method, an increasing reverse voltage will be applied across the collector-emitter of an IGBT or the drain-source of a MOSFET, until a certain leakage current is reached that indicates that the device is in the breakdown. Our future research also includes conducting experiments to understand the aging-dependent maximum current carrying capability of the power switching devices.

In order to estimate the dynamic SOA, we performed CM of the semiconductor device using SSTDR. Unlike traditional CM methods, the proposed SSTDR-based CM method does not require measuring any failure precursor parameters and therefore, can overcome measurement uncertainties in live power converters. Until today, the SSTDR-based CM techniques are only able to detect device degradation while the converter is in an idle state, therefore the technique cannot be implemented in live power converter applications. In contrast, the methods proposed in this manuscript can estimate the SOH of a power device regardless of its operating states (live or idle). SSTDR embedded PWM signal was applied at the gate terminal of the power device and the corresponding reflected signal was processed to autonomously measure the device's level of degradation. Aging detection from the gate-source interface allows us to monitor the high voltage converter easier and safer than it was in the past. In the same vein, this creates a provision for the development of an intelligent gate-driver architecture with an in-built degradation monitoring unit. Therefore, future work includes embedding the SSTDR-based CM block with the gate driver circuit which can easily be accomplished by implementing digital parts both from the gate driver and SSTDR units on a

field-programmable gate array (FPGA) and the analog parts using discrete components. The use of the FPGA will allow us to transfer the technology fast enough to a potential manufacturer, who will eventually design an ASIC solution to build the overall driver module. This intelligent gate driver module will serve many purposes pertinent to CM of power devices, and some of them are provided below:

(1) Synchronization of the SSTDR test signal with the PWM gate signal will be much easier than using separate discrete components (i.e., MUX, SSTDR module, etc.).

(2) Modification of the switching scheme with better flexibility will be possible.

(3) Error in SSTDR data due to fast switching of power converters can be eliminated by lowering the data processing time using an advanced signal processing algorithm or similar technology.

(4) Allow us to use a longer PN code and increase the carrier frequency in order to increase the effective bandwidth of the system. By doing so, the SSTDR-based CM method can be made extremely sensitive (to locate small impedance changes), and extremely precise in both space and time.

As discussed in Section 3.3 of Chapter 3, SSTDR test signal experiences the combined effect of the increased value of ON-state channel resistance ($R_{DS(ON)}$) and gate-source equivalent impedance ($Z_{eq,GS}$) due to device aging. Therefore, it is not possible to differentiate the root cause of the degradation using the proposed CM method, and hence, the natural direction for future research includes the effort on the decoupling of gate-oxide and channel degradation, possibly by extracting the transmission-line model parameters of the SSTDR propagation path, taking multiple measurements at different gate-voltage levels, and so on.

In summary, this research on estimating the RUL of a power converter provides an advanced reliability framework leading to a new real-time health monitoring tool incorporating SSTDR and the dynamic SOA concept. The outcome of this research will significantly improve the lifespan of the power converters by performing preventive scheduled maintenance, which will eventually lead to increased system availability and reduced cost. Last but not the least, the developed technique can also be applied to other power devices such as insulated gate bipolar transistors (IGBTs) and silicon carbide (SiC) MOSFETs and future research will include such implementation of the proposed method.

This manuscript also presents a PV array fault detection algorithm using the SSTDR method. PV array fault detection using SSTDR is challenging because of wide variations in impedance discontinuities in the SSTDR propagation path which is caused by the use of different materials and interconnections inside the PV system. In this research, we developed an algorithm centered around SSTDR that was able to overcome this challenge and demonstrated the feasibility of using SSTDR to detect the ground faults in PV array with any variation in the number of PV strings, number of faults (single or double) and value of fault impedances. Most importantly, the proposed SSTDR based fault detection scheme can detect ground fault at low irradiance, even in the absence of sunlight which may remain undetected using the conventional GFDI fuses and protection schemes. Another interesting finding of this research was that this method can determine the location of multiple faults from a single measurement point. To date, there exists hardly any existing protection scheme that can faithfully locate multiple faults without using separate sensors/protection devices for each PV string. Our proposed algorithm can reduce these costs, making the detection scheme one of only a few existing techniques within the field capable of identifying multiple fault locations

from a single point. Therefore, the proposed PV array fault detection technique would provide good guidance for the standard makers, and solar panel and solar inverter manufacturers.

In an equal endeavor, an SSTDR-based technique has been presented in this manuscript to detect the level of aging and location of a degraded cell in a series-connected Li-ion battery string. Existing battery health monitoring techniques can only determine the overall health of the string, leaving it vulnerable to capacity and performance failures caused by cascading degradation in the individual cells due to their uneven initial SOH. Therefore, our developed tool that can determine the SOH of individual aged cells along with their locations within Li-ion battery packs could be an excellent add-on feature for BMS to guarantee the safety and reliability of the entire battery system. Future work includes investigating the validity of the proposed algorithm by carrying out the experiment in a series-parallel battery string with cells having different levels of aging. Since the amount of reflection depends on the amount of impedance change, it is possible to quantify the SOH of the aged cells along with their location information and future work should investigate how to address this issue.

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