ON-CHIP VOLTAGE REGULATOR– CIRCUIT DESIGN AND AUTOMATION

A Dissertation in
Electrical and Computer Engineering
and
Computer Science

Presented to the Faculty of the University
of Missouri–Kansas City in partial fulfillment of
the requirements for the degree

DOCTOR OF PHILOSOPHY

by

FARID UDDIN AHMED

Master of Science (M.Sc) in Electrical and Computer Engineering,
University of Missouri-Kansas City, Missouri, USA, 2020

Kansas City, Missouri
2021

ON-CHIP VOLTAGE REGULATOR– CIRCUIT DESIGN AND AUTOMATION

Farid Uddin Ahmed, Candidate for the Doctor of Philosophy Degree

University of Missouri–Kansas City, 2021

ABSTRACT

With the increase of density and complexity of high-performance integrated circuits and systems, including many-core chips and system-on-chip (SoC), it is becoming difficult to meet the power delivery and regulation requirements with off-chip regulators. The off-chip regulators become a less attractive choice because of the higher overheads and complexity imposed by the additional wires, pins, and pads. The increased I2R loss makes it challenging to maintain the integrity of different voltage domains under a lower supply voltage environment in the smaller technology nodes. Fully integrated on-chip voltage regulators have proven to be an effective solution to mitigate power delivery and integrity issues. Two types of regulators are considered as most promising for on-chip implementation: (i) the low-drop-out (LDO) regulator and (ii) the switched-capacitor (SC) regulator. The first part of our research mainly focused on the LDO regulator. Inspired by the recent surge of interest for capless voltage regulators, we presented two fully on-chip external capacitor-less low-dropout voltage regulator design.

The second part of this proposal explores the complexity of designing each block of the regulator/analog circuit and proposed a design methodology for analog circuit synthesis using simulation and learning-based approach. As the complexity is increasing day-by-day in an analog circuit, hierarchical flow mostly uses for design automation. In this work, we focused mainly on Circuit-level, one of the significant steps in the flow. We presented a novel, efficient circuit synthesis flow based on simulation and learning-based optimization methods. The proposed methodology has two phases: the learning phase and the evaluation phase. Random forest, a supervised learning is used to reduce the sample points in the design space and iteration number during the learning phase. Additionally, symmetric constraints are used further to reduce the iteration number during the sizing process. We introduced a three-step circuit synthesis flow to automate the analog circuit design. We used Hspice as a simulation tool during the evaluation phase of the proposed methodology. The three most common analog circuits are chosen: single-stage differential amplifier, operational transconductance amplifier, and two-stage differential amplifier to verify the algorithm. The tool is developed in Python, and the technology we used is 0.6um. We also verified the optimized result in Cadence Virtuoso.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled "On-chip Voltage Regulator– Circuit Design and Automation," presented by Farid Uddin Ahmed, candidate for the Doctor of Philosophy degree, and hereby certify that in their opinion it is worthy of acceptance.

Supervisory Committee

Masud H Chowdhury, Ph.D., Committee Chair
Department of Computer Science Electrical Engineering

Yugyung Lee, Ph.D., Co-discipline Advisor
Department of Computer Science Electrical Engineering

Ghulam Chaudhry, Ph.D., Committee Member
Department of Computer Science Electrical Engineering

Ahmed Hassan, Ph.D., Committee Member
Department of Computer Science Electrical Engineering

Cory Beard, Ph.D., Committee Member
Department of Computer Science Electrical Engineering

CONTENTS

ABSTRACT iii

LIST OF ILLUSTRATIONS ix

LIST OF TABLES xii

ACKNOWLEDGEMENTS xiii

Chapter

1 INTRODUCTION 1

1.1 Motivation 1

1.2 Thesis Objective 3

2 ON-CHIP POWER DELIVERY SYSTEM 7

2.1 Background 7

2.2 Voltage Regulator Classification 11

3 FUNDAMENTALS OF ON-CHIP VOLTAGE REGULATOR 21

3.1 Low-dropout Voltage Regulator (LDO) 21

3.2 Switched Capacitor Voltage Regulator 24

4 LDO DESIGN IN 45NM TECHNOLOGY 30

4.1 Proposed LDO Design 30

4.2 Modeling Frequency Response of The Proposed Design 37

4.3 Simulation and Result Analysis 40

4.4 Comparison with Prior Works 46

5 LDO DESIGN IN 180NM TECHNOLOGY 52
5.1 Proposed LDO Design 52
5.2 Modeling Frequency Response of The Proposed Design 57
5.3 Simulation and Result Analysis 59
5.4 Comparison with Prior Works 62
5.5 Application 63
6 ANALOG DESIGN AUTOMATION 66
6.1 Background 66
6.2 Analog design Flow 68
7 PROPOSED ANALOG DESIGN METHODOLOGY 75
7.1 Methodology 75
7.2 Implementation of the proposed methodology 82
7.3 Result and Analysis 89
8 ENERGY EFFICIENT FDSOI AND FINFET BASED POWER GATING CIRCUIT USING DATA RETENTION TRANSISTOR 93
8.1 Background 93
8.2 Characteristics of Devices 95
8.3 Working Principle of Proposed Design 98
8.4 Benchmarking between FDSOI and FinFET based NAND logic gate . . . 100
9 CONCLUSIONS & FUTURE WORK 103
9.1 Summary 103
9.2 Future Work 104

REFERENCE LIST 106

VITA 121

LIST OF ILLUSTRATIONS

Figure		Page
1	Different distributed power delivery system (a) off-chip implementation (b) having on-chip linear regulators with external on/off-chip switching regulators (c) having on-chip switching regulators with only one external on/off-chip switching regulator.	9
2	Block diagram of (a) series Linear Regulator and (b) shunt Linear Regulator.	14
3	Example of step-down (a) switched-inductor converter and (b) switched-capacitor converter.	15
4	Different Switched-capacitor regulator topology	17
5	Basic structure of an LDO	22
6	Basic structure of an SC regulator	25
7	A simple 4-phase interleaved SC converter	26
8	Block diagram of (a) traditional LDO and (b) proposed design.	31
9	Schematic diagram of EA, CS and buffer.	32
10	Schematic diagram of supply independent biasing network.	34
11	Output current of the supply independent biasing network.	35
12	Transistor level layout of the proposed design.	37
13	Small signal equivalent circuit of the EA and CS stage	38

14 Reference tracking response of the regulator with a step in the input reference voltage from 900mV to 1.0V. 41
15 Load transient response of the proposed regulator with a step of load current from 0 to 15mA. 42
16 Output voltage regulation for various reference voltages and loads. 43
17 Line regulation of the proposed design. 44
18 Output voltage with respect to load current. Output starts to distort for $V_{ref} > 1.0$V. 44
19 Frequency response of the loop consists of EA and CS stage. 45
20 PSRR plot of the Proposed LDO Design. 46
21 Corner Analysis of the Proposed design with step load for (a) typical (b) fast-fast and (c) slow-slow. 48
22 Corner Analysis of Proposed design for PSRR (a) typical (b) fast-fast and (c) slow-slow. 49
23 Block Diagram of proposed design in 180nm 52
24 Schematic of Error Amplifier Circuit 53
25 Schematic diagram of supply independent biasing network. 54
26 Output current of the supply independent biasing network. 54
27 Schematic of Voltage follower/Buffer Circuit 56
28 Transistor level layout of the proposed design with capacitors 58
29 Small signal equivalent circuit of two stage Error Amplifier 58

30 Load transient response of the proposed regulator with a step of load current from 0 to 20mA. 60
31 Line regulation of the proposed design. 61
32 Frequency response of the two stage error amplifier 62
33 PSRR plot of the Proposed LDO Design. 63
34 Setup Configuration of the proposed memory security 65
35 Analog Design flow highlighting top-down circuit-level design flow [1] [2] 70
36 Proposed circuit synthesis methodology flow 76
37 Relation between iteration number and a) transistor step size b) transistor count. 80
38 Circuit diagram of a Single-stage Differential Amplifier 84
39 Circuit diagram of an Operational Transconductance Amplifier 85
40 Circuit diagram of a Two-stage Differential Amplifier 85
41 Implementation of Random decision forest for Single-stage Amplifier transistor Sizing 88
42 Double gate FDSOI device 95
43 FinFET device on a SOI structure. 96
44 Threshold Voltage Dependence upon back gate bias for FDSOI. 97
45 Power gating technique using sleep transistor and data retention transistor for any Logic Module. 99
46 Power gating technique using sleep transistor with data retention transistor for 2-input NAND gate. 101

LIST OF TABLES

Tables		Page
1	Summary of differences between Linear and switching regulator	20
2	Design Parameters of Fig. 9	33
3	Specifications of the Proposed LDO	36
4	Corner analysis value for PMOS and NMOS pass transistor	47
5	Corner analysis value of the step response at different temperature	47
6	Comparison with Prior Work	51
7	Specifications of the Proposed LDO	57
8	Comparison with Prior Work	64
9	Three set of Design Specifications	83
10	Accuracy of three different classification algorithm	89
11	Iteration number and execution time of the proposed methodology for three diferent topology	90
12	Result comparison between specifications achieved from Hspice and Cadence Simulation	91
13	Modes of operation depending on control signal.	100
14	Performance summary of FDSOI and SOI-FINFET based NAND gate.	102

ACKNOWLEDGEMENTS

Foremost, I would like to express my sincere gratitude to my advisor Prof. Masud H Chowdhury for the continuous support of my Ph.D study and research, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. I could not have imagined having a better advisor and mentor for my Ph.D study.

Besides my advisor, I would like to thank the rest of my thesis committee: Prof. Yugyung Lee, Prof. Ghulam Chaudhry, Prof. Ahmed Hassan, and Prof. Cory Beard, for their encouragement and insightful comments.

I thank my fellow labmates in Micro & Nano-electronics Lab Group: Abdul Hamid B. Yousuf, Marouf Khan, Moqbull Hossain, Mahmood Uddin Mahood, Liaquat Ali, Hemanshu Shishupal, Athiya Nizam and Zarin Tasnim Sandhie, for the stimulating discussions, for the long days we were working together before deadlines, and for all the fun we have had in the last four years.

I would also like to thank my family: my parents Late Abu Taher Sarker and Farida Akhter, for giving birth to me at the first place and supporting me spiritually throughout my life. Last but not the least, I would like to thank my wife, Zarin Tasnim Sandhie and my daughter, Amayah Fareeza Ahmed for giving me strength and meaning to successfully complete my PhD.

CHAPTER 1

INTRODUCTION

1.1 Motivation

According to the VLSI industry's demand to minimize the power dissipation and meet the current demand for high-performance microprocessors, the dual-VDD microprocessor was proposed [3, 4]. Later, to maximize the utilization of chip area and low power consumption, system-on-chip was introduced. The basic idea is to integrate all computer or other electronic system components into a single chip. As different components require different voltage to operate on-chip, voltage regulation becomes one of VLSI's promising fields. Moreover, due to the dynamic switching power's quadratic dependence and the more than linear dependence of the gate oxide and sub-threshold leakage on the supply voltage, power dissipation is significantly diminished when parts of a microprocessor operating at a lower voltage level. Different approaches are made and proposed for voltage regulation.

Voltage regulators, which are the integral parts of the power delivery systems of all microelectronic circuits and systems, are traditionally off-chip devices placed on the motherboard to deliver regulated voltage to different integrated circuits and components of the systems. Typically, these off-chip regulators are made of power transistors and large passive components like inductors and capacitors with significant footprints, which are not as scalable as the on-chip logic transistors and interconnects. With the introduction

of multi-/many-core chips and system-on-a-chip (SoC), dynamic voltage and frequency scaling (DVFS) has become the standard approach to achieve optimum performance with the minimum number of voltage sources [5]. Different components/cores of the high-performance and high-density chips require different voltages. These voltages often need to be adjusted quickly. Slow off-chip regulators limit the scope of performance energy efficiency improvement. Nowadays, a complex integrated circuit requires an increasing number of voltage domains to increase computational resources by utilizing parallelism within a strict thermal and power budget. Because of this requirement, the extent of the power supply's scalability has become further limited. Slow off-chip voltage regulators would not be able to modify the supply voltages in response to varying on-chip load and activity at nano/picosecond timescale.

The number of cores and on-chip functional blocks are increasing in Soc. There are an increasing need and an inherent benefit to utilizing an individual power supply for each core/functional block to optimize the total chip power and performance. These additional off-chip regulators will increase the power supply impedance due to a separate package power plan and a limited number of pins, which will degrade performance and power efficiency. Additional off-chip regulators also lead to additional costs due to the increased motherboard size and package complexity. The power and performance constrained applications like sensors, and biomedical devices need to overcome these problems. Thus, on-chip voltage regulators have become an indispensable part of the traditional microprocessors' power management scheme. One of the primary objectives of the on-chip voltage regulator is to lower the supply voltages whenever possible. Lower

voltage level leads to a quadratic reduction of dynamic switching power and more than the linear reduction of the sub-threshold and gate leakage power. On-chip regulators can provide fast voltage scaling, and multiple on-chip power domains with various voltage and current specifications [6]. The key motivations to integrate voltage regulators on the chip are: (i) minimizing the conduction and parasitic losses in the power delivery system by reducing the interconnect length between the regulator and the processor, and (ii) reduction of the response time of the feedback control.

For on-chip implementation, two different types of VRs are mostly explored in the recent literature; Switching VR and linear VR. Whereas switching VR offers the highest efficiency, linear VR is free from any switching noise, possesses ripple rejection capacity, low voltage noise, and is less complicated [7]. The linear regulators have the advantages of low output noise, fast response time, and smaller area overhead, but their efficiency is lower compared to the switching regulator.

1.2 Thesis Objective

Due to the exponentially increasing demand for portable and mobile devices, the design complexity in the field of System-on-Chip (SoC) is increasing considerably. The industrial need is concentrated towards high-performance circuit design, which requires very low power but enables high-speed operation [8–10]. In addition to that, the need for a self-regulating power supply or Voltage Regulator (VR) for every functional block is also increasing because it optimizes the total power and performance of the chip by

turning it off during the idle period. Incorporating an off-chip VR lowers the power-efficiency and performance as the power-supply impedance substantially rises owing to the split-package power planes and limited PINs. On the other hand, an on-chip VR saves area and enables power-efficient, high-speed, and secure localized voltage regulation [6]. Due to these reasons mentioned above, on-chip VRs have become a vital portion of a conventional microprocessor circuit's power management scheme along with the power and performance constrained applications like sensors and biomedical devices as it can provide noise and ripple-free supply voltage throughout the complete chip [11] [12].

Two different types of VRs are mostly investigated in the previous literatures, such as: Switch-Cap [13] [14] [15] and linear VR [11] [12] [16] [17]. Whereas switch-cap VR offers the highest efficiency, linear VR is free from any switching noise, possesses ripple rejection capacity, low voltage noise, and is less complicated [7]. Hence, linear voltage regulators are preferable to other types of voltage regulators. Low- DropOut (LDO) is a type of linear VR which can provide output voltage close to the input voltage (the difference between the output voltage and input voltage $<$1V).

Two types of LDO can be found in the literature: analog and digital. Usually, lower technology nodes are used to design digital LDO, whereas higher is preferable for analog [18] [19] [20]. Analog LDO is preferred for on-chip implementation because digital LDO consumes more area and are more complex to design. In this work, we consider only analog LDO, and henceforth the term *LDO* denotes *analog LDO*.

Several researches on Fully integrated LDO VRs are available where the scope of design is mostly confined to technology nodes above 90nm [16] [17] [21] [22] [23] [24].

A limited number of literatures are available for less than 90nm technology nodes as analog blocks' power supply rails become more noise-prone in lower nodes. The low-frequency noise in a MOSFET increases gradually with decreasing gate area. As a result, for a specific W/L ratio, a larger L means a larger W, which results in more gate area and lower noise. Few other drawbacks of working with lower technology nodes are the electromigration process, higher leakage current, quantum effects, etc. To maintain minimal noise and alleviate the issues mentioned above, higher technology node is preferred in analog circuits. Few designs of LDO VR are proposed with 65nm node [21] [25] [26] and some are in 45nm and beyond where mostly Silicon-On-Insulator (SOI) structure are used [27] [28] [29] [30] [31]. Generally, a large capacitor is used at the LDO's output to enhance the Power Supply Rejection Ratio (PSRR). This large capacitor consumes a large area in case of an on-chip implementation and generates a large area-overhead. To alleviate the issue, occasionally, off-chip capacitors are utilized. For the fabrication of a VR block along with the SoC or functional blocks receiving power supply from VR, two different technology processes are needed by the industry, which makes the fabrication process more complicated as SoC is generally implemented in the sub-nm region. In our paper, we propose an external capacitor-less LDO design in 45nm CMOS bulk technology, which offers low power and high PSRR and includes a small on-chip output capacitor. For fabrication, we designed another capless LDO in TSMC 180nm using traditional LDO design concept. The main contributions of this work is as follows:

1. Proposed fully on-chip LDO designs in 45nm and 180nm CMOS technology;

2. Introduced an additional feedback loop in the traditional LDO to improve transient

response and PSRR

3. Designed the LDO with very small active area and wide output range;

4. Presented DC, transient and stability analysis of the proposed design;

5. Presented corner analysis and the effect of temperature variation on the proposed design;

6. Compared proposed designs with the state-of-the-art prior works.

There is an extensive manual work and time involved to design each block of an analog circuit like LDO regulator. To investigate this issue, we explored the analog design flow and proposed a methodology for analog circuit synthesis. We took error amplifier from LDO as an example to implement our methodology. We also developed a tool in python to control the flow of the methodology. The main contributions of this work is as follows:

1. Proposed a fully design methodology for analog circuit synthesis;

2. Introduced two phase optimization for topology selection and transistor sizing

3. Introduced three abstraction level to synthesize analog circuit correctly;

4. Used random forest tree and symmetric constraints to reduce the iteration and find optimize sizing which will eventually reduce flow completion time;

5. Developed a tool to run the proposed methodology in Hspice.

CHAPTER 2

ON-CHIP POWER DELIVERY SYSTEM

2.1 Background

On-chip power management is usually limited to power gating for digital circuits and linear regulators for analog circuits. Power gating can minimize the leakage current while the primary circuit is off. Most of the power gating schemes need additional circuitry to maintain the state of the logic elements during the off state, leading to the extra area and power overheads because of the additional circuitry's switching losses and IR drop. Besides, power gating techniques cannot support dynamic voltage and frequency scaling (DVFS). Linear regulator technology such as the low-drop-out regulator (LDO) mostly able to satisfy these objectives of DVFS for low-noise implementation. However, the linear regulators have low efficiency due to their limited voltage conversion ratio (VCR). Therefore, LDOs are not commonly used for the DVFS scheme and power domains requiring high currents (in SoCs and high-performance microprocessors). LDOs are usually used for analog circuits that require good supply noise rejection, and efficiency is relatively less critical. In these applications, the regulator power consumption is insignificant compared to the whole chip's total power. For applications where higher efficiency and a more comprehensive range of output voltages are critical, the switching regulators are the only alternative. The linear regulators have the advantages of low output noise, fast response time, and smaller area overhead, but their efficiency is lower

compared to the switching regulator. Switching regulators are widely used in power constraint systems due to their higher efficiency and performance [32].

In 2003, on-chip integration of a switching regulator (a high-efficiency monolithic buck-converter [3]) was demonstrated on the same die as a dual-VDD microprocessor. Both the inductive and capacitive components were used in that design. However, on-chip integration of the traditional switching regulators (mostly buck converters) is very challenging due to large inductors in these circuits. Integrating physical inductors inside the chip is very inefficient and costly. Therefore, there has been a growing interest in designing inductor-less or emulated inductor-based switching regulators for on-chip implementation [33]. The active filter-based circuit topology is proposed in 2005 [34] to improve the switching voltage regulator circuit in size and cost perspective. It is theoretically shown that with active filters, it is possible to obtain transfer functions nearly the same as the LC low pass filters with much less area. In 2010, a fully integrated SC converter with different step-down ratios was presented to spread the output voltage range [35]. The primary purpose of this design was to achieve high-power efficiency across a wide range of output voltages. However, the on-chip voltage regulators induce additional problems like added power loss, area consumption, and increased susceptibility to the load current steps. A detailed system-level analysis of fast and per-core DVFS using on-chip switching regulators has been done in [5] to explore the potential benefits of on-chip regulators. The analysis also shows how the overall system power consumption can be reduced, providing fine-grained power management and fast voltage scaling with an on-chip regulator [5].

Some hybrid implementations explored the possibility of integrating the switching

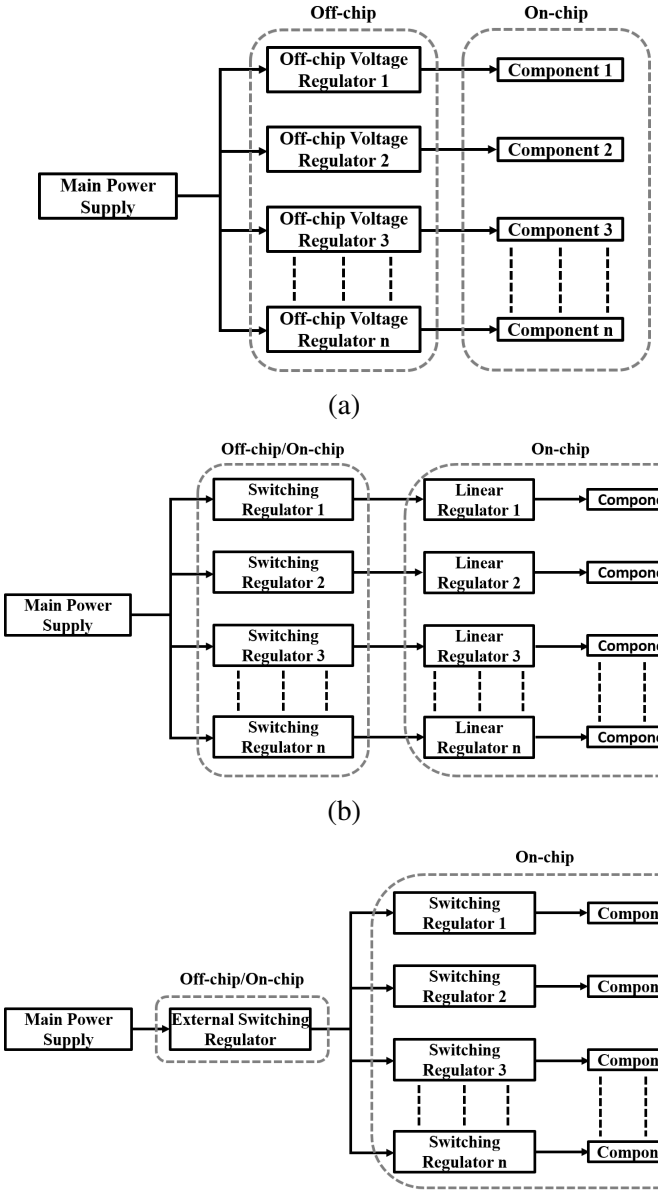


Figure 1: Different distributed power delivery system (a) off-chip implementation (b) having on-chip linear regulators with external on/off-chip switching regulators (c) having on-chip switching regulators with only one external on/off-chip switching regulator.

and the linear regulators to take advantage of both [36–39]. In [38], a hybrid two-stage power delivery system with off-chip buck converters and a tree of on-chip linear regulators has been proposed. These hybrid regulation schemes are expected to be efficient and straightforward in design and achieve higher power efficiency and lower noise, area, and voltage overheads. The regulators generate the desired supply voltage from a higher input voltage, thereby becoming an independent supply source for each voltage domain. As a larger conversion ratio leads to lower efficiency, a power management scheme may have several stages of voltage regulators to step-down the primary supply voltage to some intermediate voltages step-by-step. These intermediate stages may consist of either both linear and switching regulators or only switching regulators. In using both types of regulators, switching regulators should be the first stage to achieve higher efficiency with different conversion ratios. In the last stage, linear regulators supply low noise core voltage to the microprocessors and SoCs' components/cores.

Fig. 1 illustrates how regulators can be implemented to provide distributed power delivery with both on-chip and off-chip implementation using linear and switching regulators. The typical all off-chip regulator implementation is shown in Fig. 1a. Distributed on-/off-chip regulators based power delivery scheme is shown in Fig. 1b, where four external switching regulators are used to supply each independent on-chip LDO regulators designated for one specific voltage domain. Each external regulator has different output voltage and current requirements and supplies to each SoC component through the linear regulator. Fig. 1c shows the distributed delivery system consists of only one switching regulator in the first stage and an array of switching regulators in the second stage. Here,

one switching regulator would step down the primary supply voltage to an intermediate value, and each second-stage switching regulator then supplies the core voltage to each component. The original concept of the on-/off-chip hybrid regulation scheme was presented in [**?**]. It is proposed that the second stage regulators delivering supply voltage to individual core/component should be linear regulators, which would be controlled by the external or internal switching regulators. For the schemes like Fig. 1b and Fig. 1c, the implementation of the first-stage voltage regulators can be either off-chip or on-chip. In the scheme presented in Fig. 1c and [38], with only one single external switching voltage regulator, the motherboard area and circuit overheads used for the power delivery network can be considerably reduced, leading to the improvement of the efficiency of the voltage regulation by 3â4% [5]. However, the active filter based on-chip switching regulators have many functional blocks and very complex circuitry. To reduce the on-chip footprint of these switching regulators, researchers are continually looking for new ways.

2.2 Voltage Regulator Classification

Voltage Regulator (VR) is the most essential component of a power management integrated circuit (PMIC). The main objective of a VR is to provide a fixed DC voltage irrespective of input voltage or load condition. There are three essential components of a Voltage Regulator stage in PMIC; pass elements, a feedback circuit, and a stable reference voltage. The feedback circuit senses the output variations and does the error correction by amplifying the error signal. Then generates a control signal which drives the pass element to minimize the output's error/variation based on the reference voltage.

Voltage regulators can be categorized into Linear Voltage Regulators, Switching Voltage Regulators [32, 40]. In this survey, the transistor is the pass element in all the state-of-the-art works discussed here. Transistors can be operated in three regions to regulate the voltage at the output. These regions are saturation or active, ohmic or linear, and cut-off region. In linear voltage regulators, the pass transistor works in the linear region of its operation during voltage regulation. When the pass transistor operates and switches in-between the cut-off and saturation state, the regulator is called a Switching Voltage regulator.

2.2.1 Linear Voltage Regulator

Linear Voltage Regulators are the original form of regulators in regulating power supplies to the desired output voltage. In a linear voltage regulator, the active pass element (usually a BJT or a MOSFET) is responsible for regulating the output voltage. When a load is connected, the input or load changes will result in a current variation flowing through the transistor so that a fixed voltage is maintained at the output. For the transistor to vary it's current, it must be operated in a linear or ohmic region. A significant amount of wasted power is realized in linear VR, which can be calculated from the difference of input and output voltage. This voltage difference is dropped in the pass element and wasted through heat dissipation. In linear VR, a minimum voltage is needed to get the desired output within the specifications. Often the difference between this minimum input voltage and the output voltage is referred to as dropout voltage. Earlier, linear voltage regulators were sorted into five categories; Positive Adjustable Regulators, Negative

Adjustable Regulators, Fixed Output Regulators, Tracking Regulators, Floating Regulators [32, 40]. In all of these categories, they needed several volts to get the desired output voltage. For a well-established linear VR like LM7805, the value was about 2.5V. Since the output is 5V, at least 7.5V is needed at the input. There is a significant increase in the demand for efficient power supplies in today's world, where designers are trying to minimize the wasted power dissipated as heat. The manufacturers are considering to minimize the dropout voltage to as low as 100mV sometimes. As a result, a new type of linear regulator emerges called a low-dropout (LDO) voltage regulator. Nowadays, if the dropout voltage is less than 1V, it is essentially called LDO. For the rest of the paper, we are considering LDO as linear VR.

Linear Voltage regulators can be categorized based on how the load is connected to the output. They are Series Voltage Regulators; Shunt Voltage Regulators [40].

2.2.1.1 Series Voltage Regulator

In series voltage regulators, the active pass element (transistor) is connected in series with the load. Fig. 2a shows the basic circuit diagram of the series voltage regulator. The load R_L is in series with the pass element. In this circuit, the regulator's output voltage is sensed through the voltage divider network R_1 and R_2 and feedback to the control circuit's input. The control circuit then compares this voltage with a reference voltage. The resulting error signal controls the conduction of the pass element. Irrespective of the load, the output voltage will be maintained by changing the pass element's conduction.

2.2.1.2 Shunt Voltage Regulator

A Shunt voltage regulator is just the opposite of a Series voltage regulator. The pass transistor here is connected in parallel to the load. Along with the voltage divider network, a voltage limiting resistor, R_3, is connected in series with the load. Fig. 2b shows a typical shunt voltage regulator. The transistor's conduction is controlled based on the feedback and reference voltage such that the current through the series resistor remains constant. Though the transistor's current varies with varying loads, the voltage across the load should remain constant. When compared to series regulators, shunt regulators are slightly less efficient but have a more straightforward implementation.

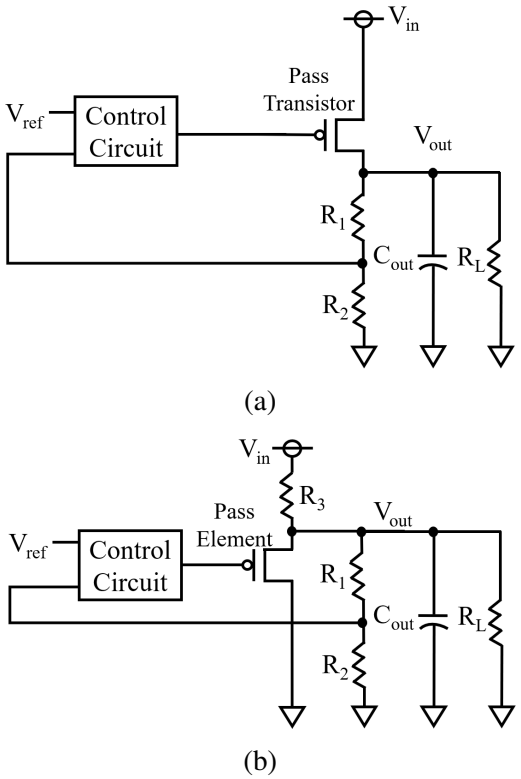


Figure 2: Block diagram of (a) series Linear Regulator and (b) shunt Linear Regulator.

2.2.2 Switching Voltage Regulators

A switching regulator's operation is different from the Linear Regulator because the pass transistor acts as a switch. The pass transistor switches between off state (cut-off region) and on state (saturation region). The output voltage is maintained at a fixed value by controlling the on-time of the pass transistor.

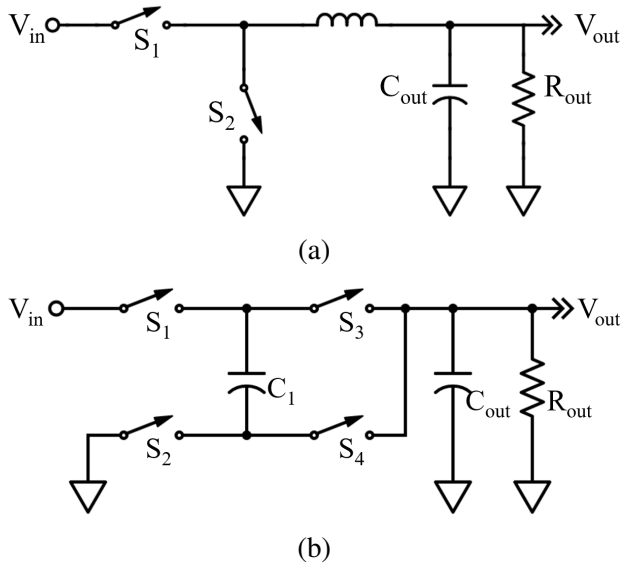


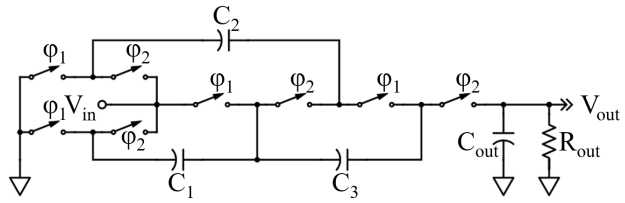
Figure 3: Example of step-down (a) switched-inductor converter and (b) switched-capacitor converter.

Switching regulators are the most promising VR to provide a wide range of output voltages with higher efficiency. In switching regulators, the charge is drawn from the input and stored in one step, and then transferred to the output in the next step. Depending on the storage element, Switching regulators can be classified into two categories based on the energy element [41]; Switched-inductor converter and Switched-Capacitor Converter. Fig. 3 shows two common examples of step-down switching converters using an inductor

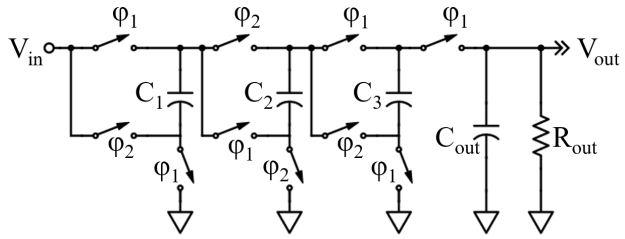
and a switched-capacitor (SC) converter. There is no fundamental limit on these switching converters' efficiency in an ideal state with lossless inductors and capacitors. Between these two types, the switched-capacitor converter is our main focus in this paper.

A capacitor has three operation states; charging, discharging, and idle. A capacitor can get charge from a voltage source or other capacitor connected in the circuit. Similarly, the capacitor can discharge to a load or another capacitor in the circuit. The capacitors which are getting charged from or discharged to another capacitor are called intermediate capacitors. These intermediate capacitors increase the level of energy transfer and conduction loss in the circuit. When the capacitor is not transferring or receiving any charge, it is called an idle state. Depending on the way of charge transfer from source to load, SC converter can be divided into two categories; direct-charging-based converters or indirect-charging-based converters [42].

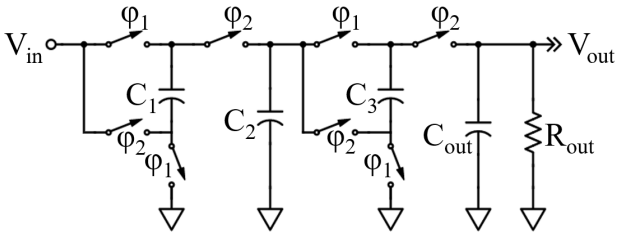
SC-based DC-DC converters typically use five common topologies, including Dickson, Fibonacci, Doubler, Ladder, and Series-Parallel. The first three are considered the up-converter (boost) because the Voltage Conversion Ratio (VCR) of these converters is more than one. The other two topologies (Ladder and Series-Parallel) are down-converter (similar to buck converter) with VCR less than one. Sometimes, Fibonacci and Doubler topologies are called exponential converters because their VCR is exponentially related to the number of capacitors. These implementations support a range of different voltages, but most of the switches are not ground referenced, making them difficult to implement. Ladder and Dickson topologies provide regularity to the power switches and their drivers. In contrast, the Series-Parallel topology has the best capacitor utilization,



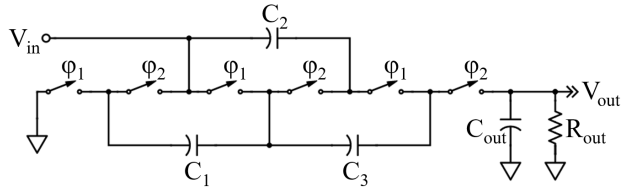
(a) Dickson



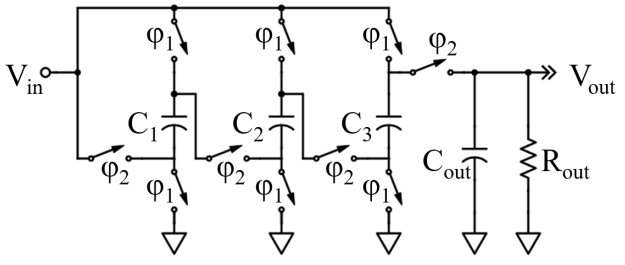
(b) Fibonacci



(c) Doubler



(d) Ladder



(e) Series-parallel

Figure 4: Different Switched-capacitor regulator topology

which means it requires the smallest total capacitance for the same performance compared to other topologies. There are two other metrics named Slow-Switching-Limit (SSL) and Fast-Switching-Limit (FSL) to evaluate and compare different converter topologies' performance [43–46].

The SSL impedance is calculated assuming that the switches, capacitors, and interconnect lines are ideal and have very negligible finite resistance. The FSL occurs when the resistances associated with the switches, capacitors, and the interconnect lines dominate, and the capacitors act effectively as fixed voltage sources. In the FSL, current flow occurs in a frequency-independent piece-wise constant pattern, while the SSL impedance is inversely proportional to switching frequency. A set of charge multiplier vectors are associated with these metrics. The performance of a converter is related to the square of the sum of these charge multiplier coefficients. Topologies with a small sum of these coefficients perform better for a given switch conductance than a topology with a large sum of coefficients. These metrics also depend on the conversion ratios of the regulators. For a conversion factor of 2, all the topologies perform almost equal.

In contrast, for higher conversion ratios, in SSL comparison, Series-Parallel topology performs better than others due to lower output impedance. Moreover, Series-Parallel topologies ensure the best utilization of the capacitors and SSL comparison solely dependent on the elements' capacitance values rather than resistance values. In general, no one topology can perform well in terms of both of these metrics. In SSL and FSL comparison, Series-Parallel topology and Ladder topology performs better than other topologies,

respectively [43]. Some topologies use switches efficiently, and others use capacitors efficiently, but none of the topologies are superior in both aspects. In the CMOS processes, fully integrated SC converter implementations are typically dominated by the capacitor area and performance. Therefore, Series-Parallel topology is the best topology because it is more efficient in capacitor implementation.

The differences between linear and switching voltage regulators are summarized in Table 1.

Table 1: Summary of differences between Linear and switching regulator

	Linear Voltage Regulator	Switching Regulator
Working Principle	Pass element works in the linear region. By controlling the conduction of the pass element, the output voltage is maintained.	Pass element works in the cut-off or saturation region. By controlling the on-off period of the pass element, the output voltage is achieved.
Circuit element	Do not need any storage elements for energy transfer.	Need storage element like inductor or capacitor for energy transfer in one or multiple steps
Advantages	Ease of use, simple design, low cost, free of switching noise, and smaller device size. Robust in over current protection and thermal protection.	Higher efficiency, both step-up or step-down operation is possible. As less power is wasted, less heat emit.
Drawbacks	Low efficiency, only steps down operation is possible. Power is wasted through heat dissipation.	Higher switching noise, bottom plate capacitance loss, complex architecture. Takes more on-chip area than a linear regulator.
Application	1. Suitable for low power applications with low output current where power requirement is not critical. 2. For noise-sensitive applications, especially for radio devices and communications. 3. Time-sensitive applications. 4.Applications, require output voltage is close to the input voltage.	1. Because of the higher efficiency, suitable for applications where power requirement is critical. 2. Thermal sensitive applications. 3. Suitable for both step-up and step-down applications.

CHAPTER 3

FUNDAMENTALS OF ON-CHIP VOLTAGE REGULATOR

3.1 Low-dropout Voltage Regulator (LDO)

PMIC systems are divided into multiple power domains to improve power efficiency, noise isolation and fulfill the purpose of power gating in SoCs. Hence, the required number of voltage regulators are increasing. LDO is used in SoC to provide a stable, noise-free, and accurate output voltage to the components. LDO can be fully integrated into SoCs or work as a standalone PMIC.

3.1.1 LDO Voltage Regulator Architecture

An LDO voltage regulator's basic architecture comprises a voltage reference, an error amplifier, a pass transistor, and a resistor feedback network. LDO has a closed-loop architecture as the system's output is fed back to one of the error amplifier's inputs. So to ensure a stable operation, loop stability analysis should be done. The two necessary stability analysis parameters, gain and phase margin, show if the loop has a stable operating condition in a specific range. An unstable feedback loop can produce ringing, continuous oscillations at the output, which results in a poorly designed voltage regulator.

A traditional LDO VR requires an external capacitor to have an acceptable power supply rejection ratio (PSRR), good transient response, and to ensure the LDO regulator's stability. Along with these advantages mentioned, there are some drawbacks to have an

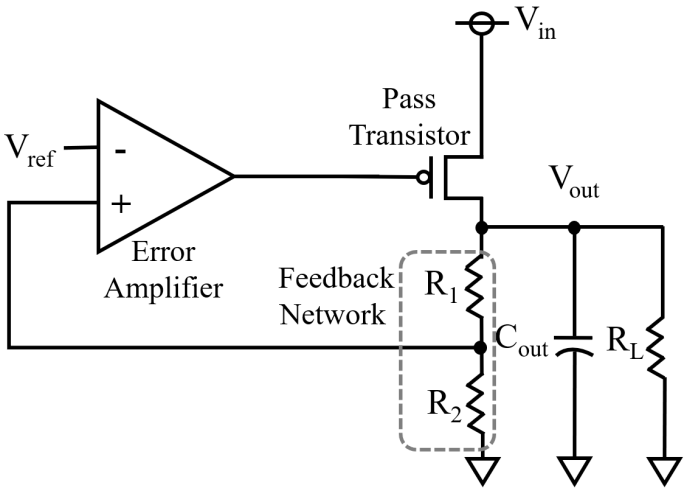


Figure 5: Basic structure of an LDO

external capacitor. The external capacitor usually has higher values, which takes a large area for on-chip implementation. Most of the time, the external capacitor is used as an off-chip element, which decreases the system's long-term reliability and consumes valuable pins in SoC devices. Some external capacitor free design found in literature where the LDO architecture does not require an external load capacitance. These designs are mentioned as "capacitor less" or "capless" LDO VR. The absence of the external capacitor makes fully on-chip implementation possible for LDO VR. Economically it is a tremendous advantage of capless LDO. Nevertheless, transient performance and PSRR become notably degrade in capless architecture. As a result, designers need to overcome significant design challenges to improve the overall performance of LDO.

3.1.2 LDO Voltage Regulator with External Load Capacitor

The off-chip capacitor value can be in the range of a few uF in a typical LDO design. Because of the capacitor's high value, one dominant pole resides at the output, which gives good stability in the overall system. Off-chip capacitors also offer good line and load regulation as well as good power-supply noise rejection. Nonetheless, several practical concerns must be considered when selecting external output capacitors for specific applications. External capacitors are usually bulk and have non-idealities, which can be critical. Two parasitics parameters Effective Series Inductance (ESL) and Effective Series Resistance (ESR), affect the capacitor's performance badly at high frequency.

A capacitor usually has four impedances; ESR, ESL, a large leakage resistor, and the ideal capacitor connected parallel leakage resistor. An ideal capacitor's reactance decreases with increasing frequency. Hence, a minimum ESR is needed so that the total impedance does not go to zero at high frequencies. The total impedance of the output capacitor is calculated from the capacitance and ESR reactance. The dynamic response degrades because of low impedance during the loop stability analysis as the dominant pole reduces phase margin. On the contrary, a large ESR creates a zero that stretches the closed-loop's unity gain frequency, critically worsening the phase margin and making the system unstable.

For stability purposes, the ESR of the output capacitance should be restricted within a particular range of minimum and maximum values. An external load capacitor's wrong selection might cause unnecessary power dissipation, noise, and overall stability problems, which hamper battery and device longevity.

3.1.3 Capless LDO Voltage Regulator

For SoC integrated and discrete applications, the capless LDO VR is an intriguing choice for the designers. Without the external load capacitor, fully on-chip implementation will be possible. Moreover, this can translate into a small digital footprint in the printed circuit board (PCB) area, and lower Bill-of-Materials (BOM) costs.

By not having any external capacitor at the output also brings several advantages for capless LDOs. There will be a reduced number of metal paths, bond wires, external pins and pads, package connections, and a decrease in the cost associated with them. In modern complex systems like SoC, several LDO VRs are typically needed. Therefore, eliminating external output capacitors gives a multiplier effect over these benefits. As there is no external capacitor at the output, there is no dominant pole at the output but a dominant internal pole changing with the load current. So it will be a challenging design problem to provide a stable output voltage across a wide range of load current and load capacitors for capless LDOs.

3.2 Switched Capacitor Voltage Regulator

Switched capacitor regulators are becoming a popular choice in PMIC for their on chip-implementation. Moreover, they offer a reconfigurable output voltage from a single input voltage with higher power conversion efficiency and design flexibility.

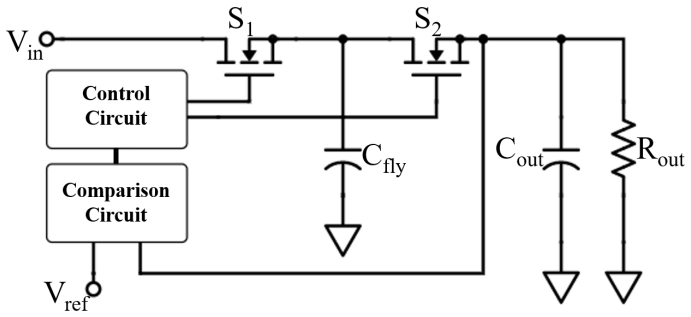


Figure 6: Basic structure of an SC regulator

3.2.1 Switched Capacitor Voltage Regulator architecture

A switch capacitor regulator's basic structure consists of switches, capacitors as storage elements, a comparison circuit, and control circuitry (Fig. 6). By controlling the on/off-time of the switches, capacitors transfers charge from input to output. Depending on the condition of the switches, capacitors will be charged or discharged.

The switches' on-off time is controlled by a pulse-width-modulation(PWM) operation, which is usually controlled by the control circuit. The output of the regulator is fed back to the comparison circuit to compare with a reference voltage. The resultant output then feeds to the control circuit to generate a pulse, which eventually controls the switches to charge and discharge the switches. When output falls below the reference level, on-time increases, and more charges are transmitted from the input side or intermediate capacitor to increase the output level. The on-time reduces when the output voltage reaches the reference level to prevent overshoot at the output.

Interleaving is a widespread technique usually used in SC VR design to minimize the ripple at the output [46]. In this technique, the SC regulator is divided into multiple

smaller units, and clock signals deliver to each unit with a phase shift in between each unit. A simple 4-phase interleaved SC converter is presented in Fig. 7. This technique benefits in multiple ways. It reduces the input current and the output voltage ripples without redundant input and output decoupling capacitors. To minimize the output ripple, typically, there is a need for a large decoupling capacitor in single phase implementation, which incurs a significant on-chip area. Considering N-phase interleaving implementation, whenever an SC regulator's fly capacitor changes state between charging and discharging, fly capacitors in the remaining N-1 phases efficiently act to minimize the decoupling effect so that the output ripple will be less.

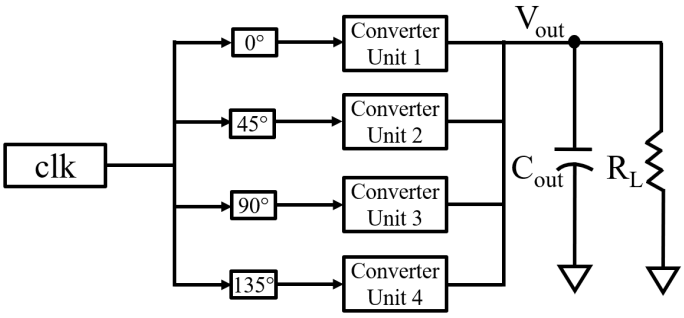


Figure 7: A simple 4-phase interleaved SC converter

The interleaving units' operation is controlled by a single-bound hysteretic control scheme implemented in the feedback loop. The scheme is beneficial for its simple and inherently stable operation and its high bandwidth control. The switches' switching frequency is modulated by this scheme to control the SC converters' equivalent output resistance, which ensures the desired voltage at the output. Switching frequency modulation is a popular regulation technique for on-chip SC converters [44, 45]. The scheme's

basic concept is to generate a trigger signal whenever the output voltage is less than the reference voltage at the clock rising edge. The trigger signal causes the shifted clock signal to change the switches' state in the next unit to provide enough charge to make a rise at the output voltage. If the output is less than the reference voltage, no trigger signal is generated, and all the switches will be in the same state.

3.2.2 Different types of capacitor used in SC Regulator

The SC regulators would be able to take full advantage of monolithic integration [33, 44, 45, 47]. It is anticipated that the SC regulators can provide higher efficiency and minimize interconnect lengths and losses. SC converters consist only of transistors and capacitors, and it is easy to integrate these components inside the chip [45]. However, the SC regulators have some issues like the bottom plate capacitance of the fly capacitors, the conduction and switching losses in the transistors, the transistors' parasitic capacitances, and the Voltage Conversion Ratio (VCR). These factors negatively affect the SC regulators' performance and make it challenging to obtain the desired voltage level, efficiency, power density, and load currents. The bottom plate parasitic capacitance losses of the on-chip capacitors usually limit the peak efficiency of the converter. These losses occur when the SC converters supply the load by charging and discharging the fly capacitors. The charging and discharging of the bottom plate parasitic capacitance in every clock cycle is a non-desirable impact that imposes the losses. Several designs have been proposed to overcome these limitations and achieve higher efficiency and power density.

These design approaches include different capacitors to minimize the parasitic and bottom plate capacitance losses used novel feed-forward control, hysteretic control, and other approaches.

The performance of the SC converters is mostly dependent on the capacitor technology. The most commonly used capacitor technologies are Metal-Oxide-Metal (MOM), Metal-Oxide-Semiconductor (MOS), Metal-Insulator-Metal (MIM), and Deep-Trench capacitors. The fundamental differences among these technologies are in the structure and construction procedure. One of the most crucial factors to design an SC regulator is the fly capacitors' capacitance density. The deep-Trench capacitor is the most suitable one from this perspective because of its inherent 3-D nature that helps achieve larger capacitance using a significantly smaller silicon footprint than the other technologies like MOM, MOS, or MIM. The capacitances obtained from the Deep-Trench technology are more than 100 times denser than the MOS capacitors and thus show a significant improvement in the SC regulators' power density.

The MOM capacitor's capacitance density is 0.2-1fF per μm^2 depending on the number of the metal layers and the pitch between the layers. The MIM capacitor has a capacitance density of 1-3fF per μm^2. However, the Deep-Trench capacitor suffers from large series resistance and poor frequency response and exhibits a slower transient response than the equivalent MOS capacitor. The MOM and MIM structures have relatively low series resistance due to the full metal connections and show linearity, making these two technologies suitable for SC regulators' implementation. For the lower-node technologies, the MOS structure is not suitable for low supply voltage [46]. Some literature

uses another kind of capacitor called ferroelectric capacitor in SC VR for their extremely low bottom plate capacitance and high-density [48]. One of the primary sources of losses in the SC regulator is the parasitic capacitors associated with the technological features and on-chip capacitors' manufacturing process. For the MOS and MIM capacitors, parasitic capacitance from the bottom plate to the substrate can reach several percent of the minimal capacity, which may diminish the regulator's efficiency by 10â15% for some ranges of the operating voltages and currents [46]. Different capacitor technologies can be used for the proposed SC voltage regulator depending on a particular application's specifications and requirements.

CHAPTER 4

LDO DESIGN IN 45NM TECHNOLOGY

In this section, we describe the basic blocks of the proposed LDO along with the design specification.

4.1 Proposed LDO Design

The traditional LDO comprises an Error Amplifier (EA), a pass transistor, and a resistive feedback network, as shown in Fig. 8a [49]. In the proposed design, we replace the resistive network with an extra NMOS pass transistor driven by a common-source (CS) stage. The proposed circuit is shown in Fig 8b. The desired output voltage is achieved by controlling the gate voltage of the two-pass transistors (NMOS and PMOS). A Equivalent Series Resistance (ESR), value of 1 is used here in series of output capacitor for proper modeling.

The purpose of the additional NMOS pass transistor here to get better control of the output voltage regulation and improve the transient response and PSRR. CS stage drives the NMOS based on the amplified output of EA. The NMOS is driven with feedback from the output node with higher amplification leveraging both EA and CS stage, and it is biased in the saturation region.

Note that the reference voltage, V_{ref} is an input to the LDO and is connected to the negative terminal of EA, which comes from a bandgap reference voltage circuit. We

have skipped discussion on the bandgap circuit since that out of the scope of this paper. Details regarding EA, CS, buffer, and pass transistors are given below:

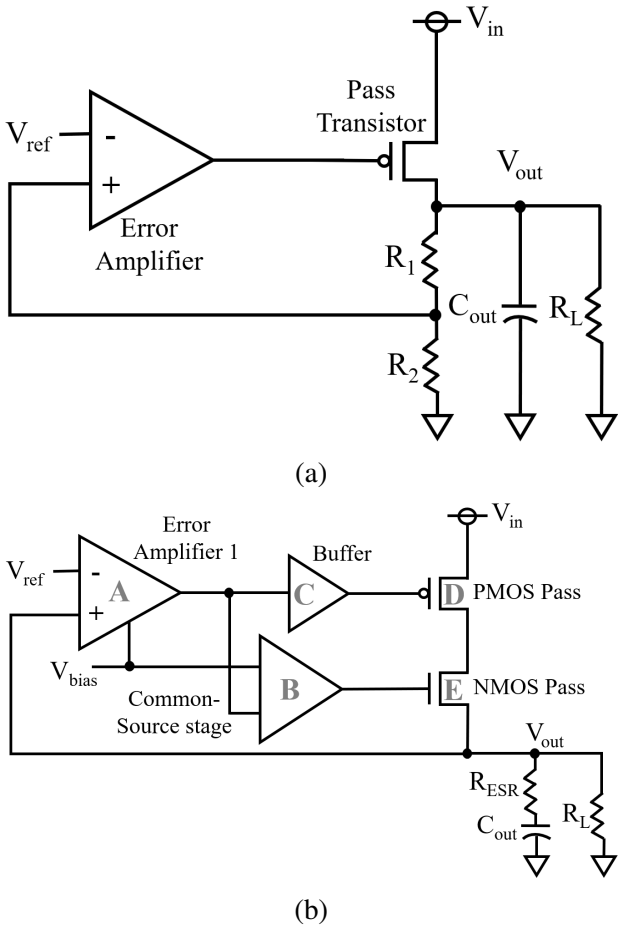


Figure 8: Block diagram of (a) traditional LDO and (b) proposed design.

4.1.1 Error Amplifier (EA) and Common-Source (CS) Stage

The EA (Block A in Fig. 8b) is a differential amplifier having one input as a reference voltage and other input coming from the output node as feedback. The output of the EA stage is connected to M_6 of the common-source (CS) stage (Block B in Fig.

8b). In the first stage, the output is compared with the reference voltage and then feeds to the second stage. CS consists of two transistors. The output of EA also goes through the buffer (Block C) and controls the PMOS transistor. The output of CS is fed to the NMOS pass transistor. As the cascaded structure of EA and CS create a two-pole system, one compensator capacitor (C_1 in Fig. 9) of 18fF value is used for the stability purpose. The M_5 and M_8 are biased with a biasing voltage from a supply independent biasing network. (Fig.10).

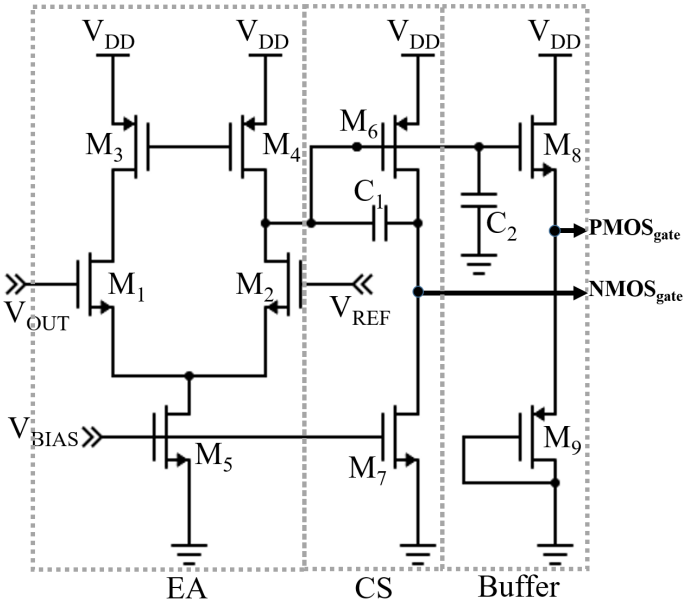


Figure 9: Schematic diagram of EA, CS and buffer.

4.1.2 Biasing Circuit

The biasing network is designed in such a way that it will deliver fixed current irrespective of a range of supply voltage shown in Fig.11. It is a beta-multiplier circuit

Table 2: Design Parameters of Fig. 9

Parameter Name	**Value**
(W/L) of M_1, M_2	16/2
(W/L) of M_3, M_4	40/2
(W/L) of M_5	9/2
(W/L) of M_6	500/2
(W/L) of M_7	53/2
(W/L) of M_8	9/2
(W/L) of M_9	66/2
(W/L) of NMOS Pass	250000/2
(W/L) of PMOS Pass	125000/2
C_1	18fF (on-chip)
C_2	10fF (on-chip)

with a differential pair in between the current mirrors to reduce the sensitivity over supply voltage. A resistor R is having a value of 720 used in the source of M_8 (Fig. 10) to accurately set the output current.

4.1.3 Buffer

A common source follower is used in the proposed design as a buffer stage (Block C in Fig. 8b), which controls the gate voltage of the PMOS pass transistor. The output of the EA drives the buffer stage. A 10fF capacitor (C_2 in Fig. 9) used here as a compensator capacitor between the gate of NMOS (M_9) and ground to reduce the effect of noise.

4.1.4 Pass Transistors

The PMOS pass transistor (Block D in Fig. 8b) is the primary driver switch of the proposed design, and the NMOS pass transistor (Block E in Fig. 8b) is used instead of

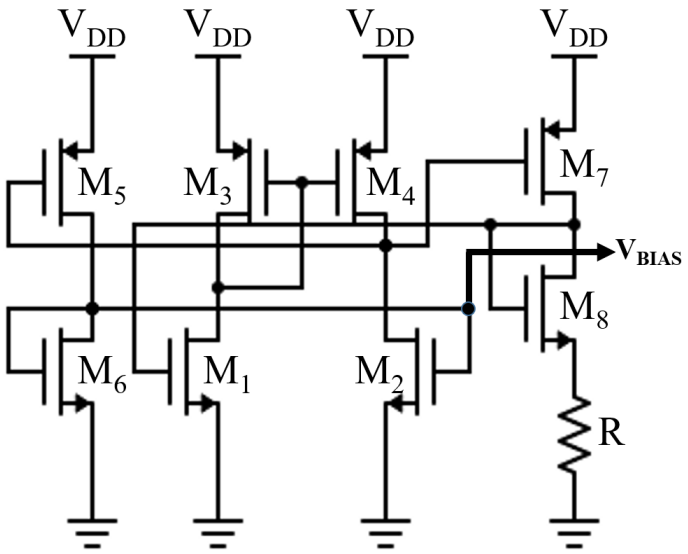


Figure 10: Schematic diagram of supply independent biasing network.

the resistive feedback network. Pass transistors are chosen with considerable sizing value to provide a sufficient amount of current to the load. Depending on the reference voltage, the output voltage is regulated by controlling two pass transistors' gate voltage. The body of the NMOS pass transistor is tied to the source to reduce the body effect.

4.1.5 Simulation Environment

The LDO in this work is designed using 45nm NCSU PDK [50] bulk CMOS technology in Cadence Virtuoso. All the design parameters, such as (W/L) values of all MOSFETs and capacitor values of Fig. 9, are summarized in Table 2.

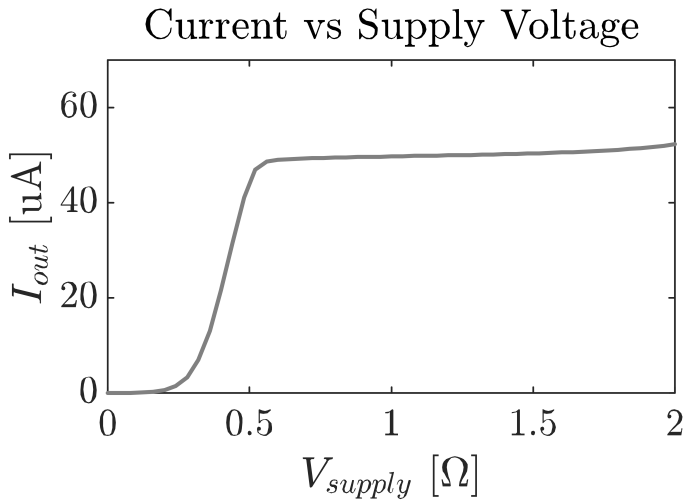


Figure 11: Output current of the supply independent biasing network.

4.1.6 Design Specification

In lower technology nodes, voltage headroom is a critical issue for the analog circuit as the supply voltage is scaling. Therefore, the LDO is designed for minimum output voltage. The proposed design's input voltage range is 1.2V to 2.2V, and it can generate a range of output voltage from 0.4V to 1.0V depending on the reference voltage (output voltage follows the reference voltage). The proposed LDO achieves a minimum dropout voltage of 200mV. The overall specification of the proposed design is summarized in Table 3.

In the proposed design, there are two feedback loops:

Loop-1: Through EA, CS stage, and NMOS. It maintains the DC value of V_{out}. EA sensed the change in output and delivered the amplified feedback to NMOS through the CS stage. If V_{out} suddenly drops, NMOS immediately increases the current through

Table 3: Specifications of the Proposed LDO

Parameter	**Specification**
Input/Output Voltage	1.2V-2.2V/0.4-1.0V
Voltage Overhead	$<$10mV
Line Regulation	2.5 (mv/V)
Load Regulation	0.0089 (mV/mA)
Load Current	15mA (max)
Quiescent Current	309uA
C_{out}	10pF (on-chip)
ΔV_{out}	35mV
Area	$0.0052mm^2$
PSRR	max 65dB @100KHz

it by getting the amplified correction form CS. Therefore, the NMOS contributes to the transient response of LDO.

Loop-2: Through EA, buffer, and PMOS. It improves the transient response of LDO by changing I_{load} rapidly for changes in the load. EA senses any changes in V_{out}. The output of EA changes and delivers feedback to PMOS via the buffer, which corrects the V_{out} by changing the current.

Advantages of additional loop: Threefold improvement we achieved because of the additional loop (Loop-1).

1. The voltage overhead of the output is minimized as output is more controlled by both PMOS and NMOS pass transistors.

2. The noise in the supply is now filtered through the series of PMOS and NMOS pass Transistor. Because of that, PSRR is improved in the proposed design.

3. The NMOS pass transistor in an additional loop improved the transient response of the proposed design.

4.1.7 Layout of the Proposed Design

The layout of the proposed design is implemented in Cadence Virtuoso (Fig. 12). DRC and LVS checks are done with the Caliber tool [51]. The total active area of the design is $214.75um^2$. This does not include area for C_1, C_2 and C_{out}. With all on-chip capacitors, the total calculated area is $0.0052mm^2$. In Fig. 12, all the transistors and the inputs are annotated. Metal 1, Metal 2, and Poly are used here for all cell level layout. Parasitic extractions are not possible due to the limitation of the NCSU PDK (usage is limited to academic purposes only).

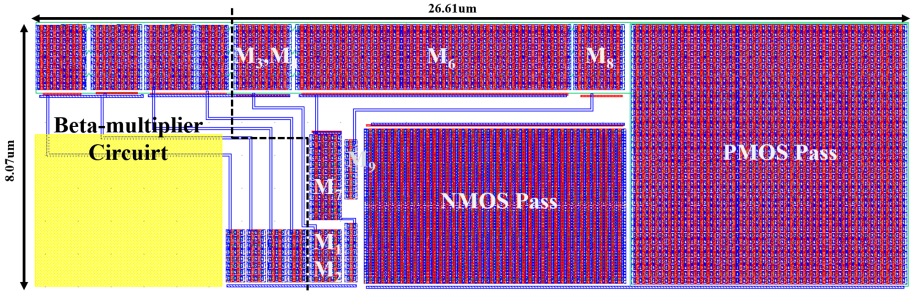


Figure 12: Transistor level layout of the proposed design.

4.2 Modeling Frequency Response of The Proposed Design

In this section, we present the modeling of the proposed design's frequency response using its small-signal equivalent model.

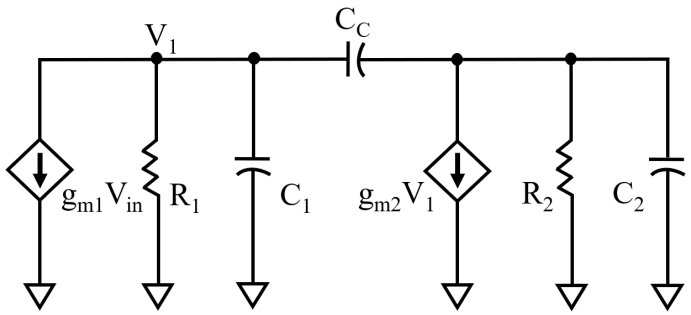


Figure 13: Small signal equivalent circuit of the EA and CS stage

4.2.1 Modeling of Loop 1

The cascaded structure of the EA and CS constructs a second-order two-pole system, leading to instability of the design [52]. Therefore, a compensating capacitor is needed. We have considered a capacitor of 18fF as a miller capacitor between the EA and CS stage in this work. This capacitor creates a large separation between the dominant and non-dominant pole and ensures better stability. The small-signal equivalent model is represented in Fig. 13. The gain and poles equations are presented by 4.1 to 4.7. Here, the dominant pole resides on the output of the EA.

$$R_1 = r_{ds4} \| r_{ds2} \tag{4.1}$$

$$R_2 = r_{ds6} \| r_{ds7} \tag{4.2}$$

$$C_1 = C_{db4} + C_{db4} + C_{gs7} \tag{4.3}$$

$$C_2 = C_{db7} + C_{db6} \tag{4.4}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}R_1R_2(1 - \frac{sC_c}{g_{m2}})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \tag{4.5}$$

$$\omega_{p1}(Dominant) \cong \frac{1}{g_{m2}R_1R_2C_C} \tag{4.6}$$

$$\omega_{p2}(Non - dominant) \cong \frac{g_{m2}}{C_1 + C_2} \tag{4.7}$$

4.2.2 Modeling of Loop 2

There is no need for a miller capacitor for Loop-2 as there is no gain in this configuration. Note that the output impedance of buffer (= $1/g_{m8}$) is lower than that of the compensating and gate capacitor of the PMOS pass transistor since the PMOS is designed with large size. Therefore, the pole moves into the unit-gain frequency of LDO and does not create any stability issue. The buffer's gain is near to unity gain, so the circuit will always be in stable condition.

4.2.3 Effect of output capacitor on Power Supply Retection Ratio

This section explains the effect of output capacitor on power supply rejection ratio (PSRR) and how PSRR changes over frequency. The ratio of the change in input to the output voltage it produces is called PSRR. It quantifies LDO's capability to suppress

ripple on the input voltage. The following equation can specify the PSRR of an LDO:

$$PSRR = 20log\frac{V_{input}}{V_{output}}(dB) \tag{4.8}$$

In our proposed design, the input ripple voltage is divided into output resistance of PMOS and NMOS devices and the output impedance of the LDO. So, equation 4.8 can be written as,

$$PSRR = 20log\frac{r_{dsp} + r_{dsn} + Z_{out}}{Z_{out}}(dB) \tag{4.9}$$

Here, Z_{out} = output impedance, r_{dsp} = output resistance of PMOS Pass and r_{dsn} = output resistance of NMOS Pass. Output impedance is coming from the output capacitor which can be modeled as capacitance value and Equivalent Series Resistance (ESR).

$$Z_{out} = R_{ESR} + \frac{1}{sC_{out}} \tag{4.10}$$

In low frequency, the capacitance value itself is dominant, but in ultra high frequency, ESR is responsible for LDO's PSRR. For low and ultra high frequency, following equations can be derived from equation 4.9 and 4.10 respectively.

$$PSRR = 20log(1 + sC_{out}(r_{dsp} + r_{dsn}))(dB) \tag{4.11}$$

$$PSRR = 20log(1 + \frac{r_{dsp} + r_{dsn}}{R_{ESR}})(dB) \tag{4.12}$$

4.3 Simulation and Result Analysis

In this section, we present the transient, DC, and AC analysis of the proposed design. The corner analysis and effect of temperature variation is also discussed here.

4.3.1 Transient Analysis

Transient response is a metric to evaluate an LDO's performance for the change in the input reference voltage and load current variation (i.e., change in the load impedance).

Fig. 14 shows the load transient performance of the LDO for a step in the reference voltage from 900mV to 1.0V. Note that the output voltage is closely following the reference voltage. The voltage overhead (the difference between the reference voltage and output voltage) for the 900mV-1.0V range is below 10mV.

To evaluate the LDO's load transient response to change in the load current, we consider a step in the load current of 15mA with 10ns for both rise and fall time with the desired regulated V_{out} = 1.0 V. Fig. 15 shows the corresponding result. A change in the V_{out} of 24mV is observed when the load current incurs the step of 15mA.

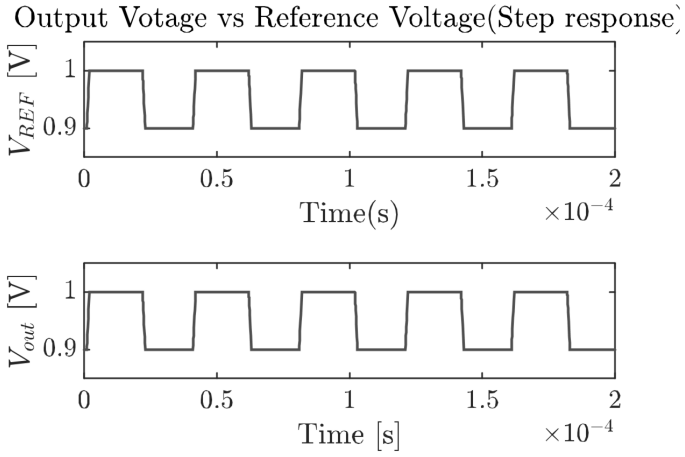


Figure 14: Reference tracking response of the regulator with a step in the input reference voltage from 900mV to 1.0V.

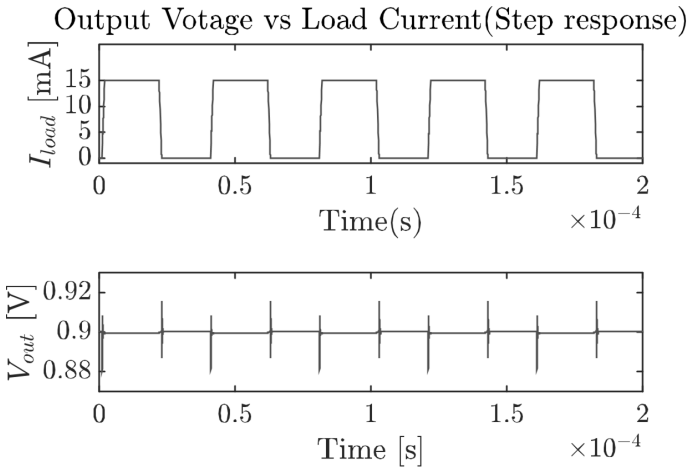


Figure 15: Load transient response of the proposed regulator with a step of load current from 0 to 15mA.

4.3.2 DC Analysis

DC analysis is a metric which evaluates the operating region, line regulation etc. of a LDO. Fig. 16 shows the output voltage regulation for various reference voltages with respect to load current. The output voltage maintains stable irrespective of the load $> 10^2\Omega$.

To evaluate LDO's line regulation, we perform a DC analysis to observe output voltage variation by varying the input supply voltage. Fig. 17 shows the corresponding result. We calculate the line regulation as $\Delta V_{out}/\Delta V_{in} = 2.5$. The simulation result indicates that the quiescent current of the proposed design is 309uA.

Fig. 18 shows the output voltage with respect to load current for various reference voltages. We observe performance degradation (unregulated output) at a high output load current for the reference voltage = 1.1V. Therefore, the LDO operates accurately within

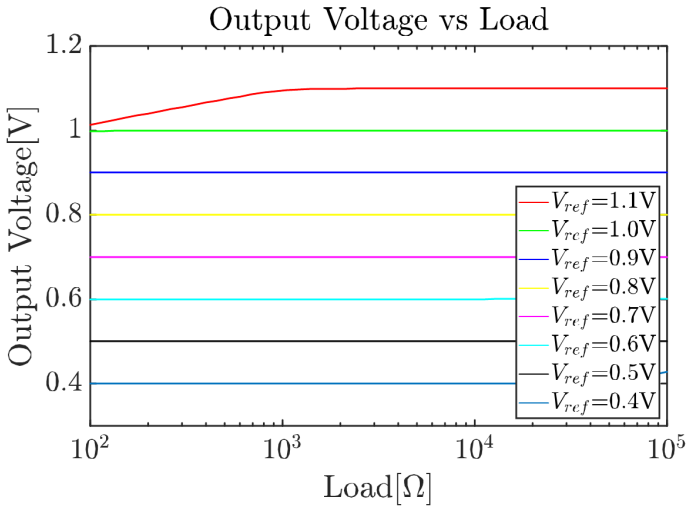


Figure 16: Output voltage regulation for various reference voltages and loads.

the 0.4V-1.0V output range. There is also a slight deviation observed for 0.4V and 0.5V when the load current is below 100uA. The load regulation of the proposed design is measured at 0.0089 (mV/mA).

4.3.3 AC and Stability Analysis

The frequency response of the circuit is presented in Fig. 19. In the design, Butterworth optimization is chosen since precise regulation is required across the passband to regulate the transistors' gate voltages. As depicted by Fig. 19, Butterworth architecture provides maximum passband flatness. The system of EA and CS stage has a 61.59dB gain and 69.9° phase margin. The whole system's overall gain is close to unity as V_{out} is directly fed to EA without any resistive feedback network. It indicates that the overall system is stable under full load conditions.

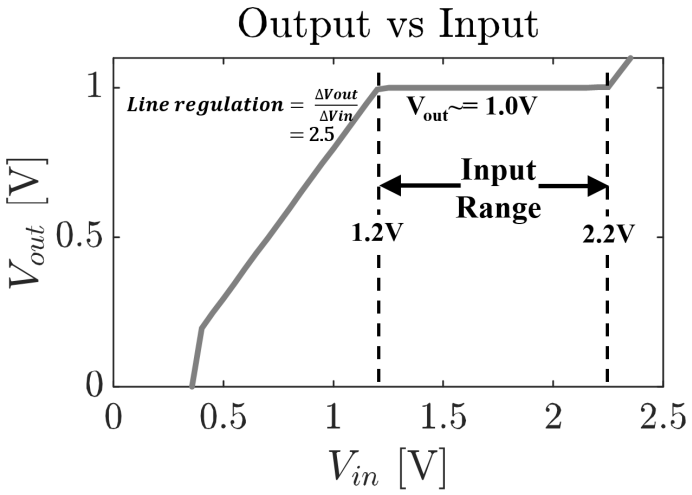


Figure 17: Line regulation of the proposed design.

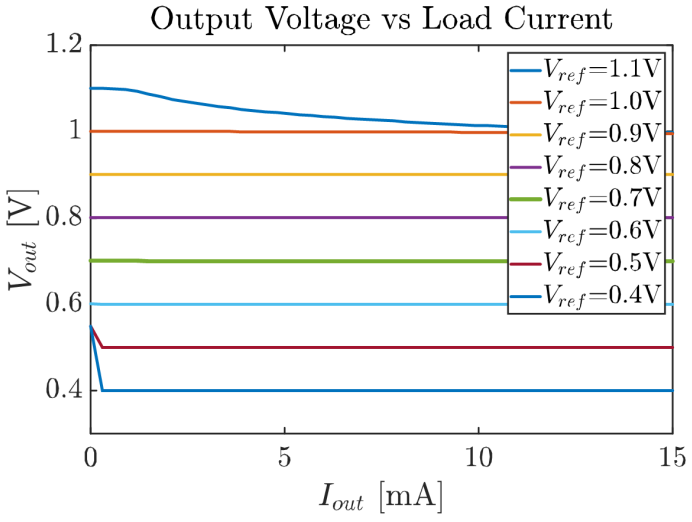


Figure 18: Output voltage with respect to load current. Output starts to distort for $V_{ref} >$ 1.0V.

Fig. 20 shows the PSRR plot of the proposed design for 1mA, 5mA, 10mA, and 15mA of load current. The plot can be divided into two regions. Region 1 is annotated by the LDO active area and shows traditional op-amp gain characteristics [53]. Gain slowly decreases linearly toward the end of Region 1 since the control loop cannot keep up with the gain. The maximum PSRR we observe is 65db until 100KHz for 1mA load current.

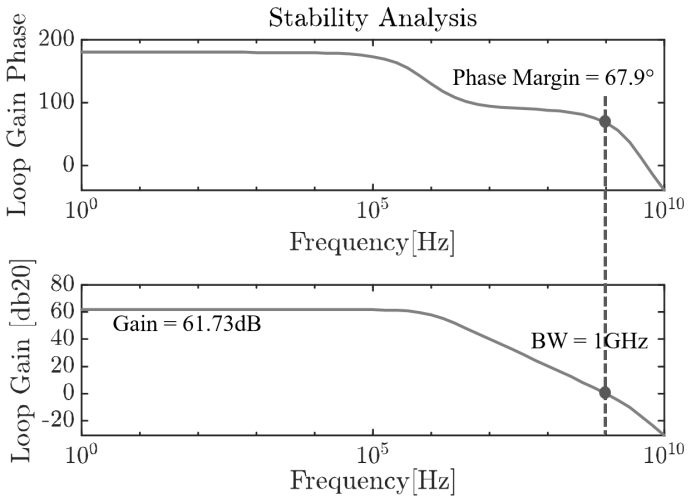


Figure 19: Frequency response of the loop consists of EA and CS stage.

4.3.4 Process Variation Analysis

We did the corner analysis and showed the effect of temperature on the proposed design's output and PSRR. We choose typical, fast-fast(ff) and slow-slow(ss) corners and three temperatures (-5, 27, and 85) to analyze the performance of the proposed design. Note that, fast-slow(FS) and slow-fast model is not available for this NCSU 45nm model. Table 4 shows how V_{th} and β_{eff} value of PMOS and NMOS pass transistor change with temperatures for different corners (using DC analysis).

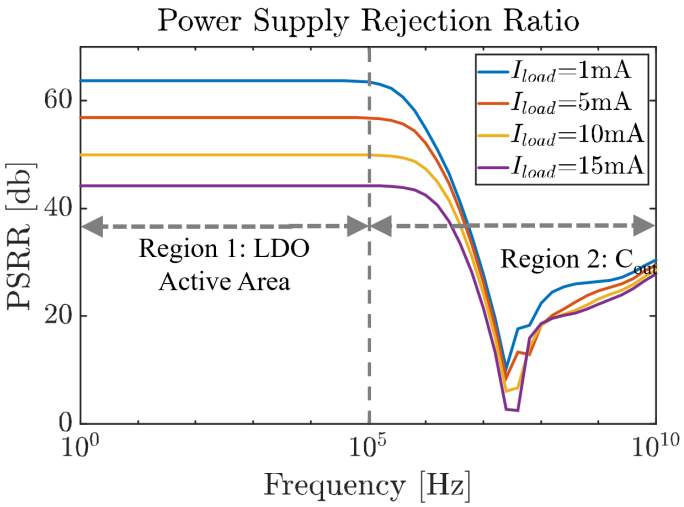


Figure 20: PSRR plot of the Proposed LDO Design.

We also analyzed the step response of the output for those corners and temperatures using transient analysis (Fig. 21). The highest overshoot found 24.84mV for ff-corner at 85°C, whereas the undershoot is 26.12mV for ss-corner at 85°C. The highest settling time found is 2.89uS for ss-corner at -5°C. We observed the PSRR for different corners and temperatures at a pick current of 15mA using AC analysis (Fig. 22). The best PSRR found 55.69dB for ff-corner at -5°C, and the worst is 28.52dB for ss corner at 85°C. The summary of the corner analysis at different temperatures of the proposed design is presented in Table 5.

4.4 Comparison with Prior Works

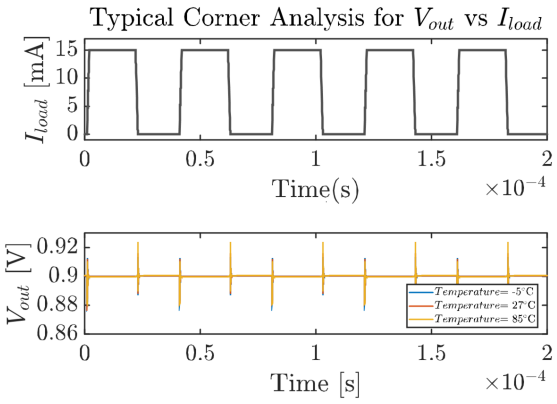
In this section, we present a discussion on the practicality, assumptions, and limitations of the proposed LDO design. A comparative analysis of the proposed LDO with

Table 4: Corner analysis value for PMOS and NMOS pass transistor

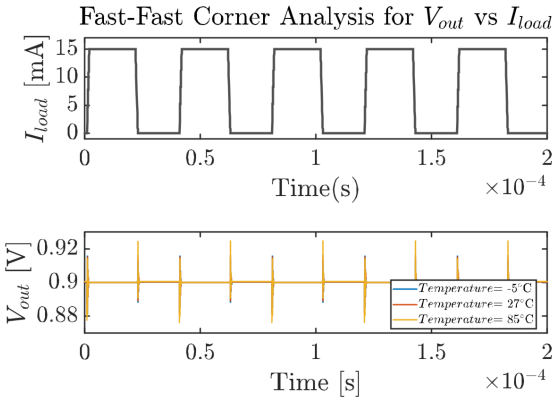
Corner	**PMOS** V_{th}**(mV)**	**NMOS** V_{th}**(mV)**	**PMOS** β_{eff}	**NMOS** β_{eff}	**Temp (°C)**
typical	169.4	231.7	7.765	44.9	27
typical	147.3	223.4	9.715	51.9	-5
typical	182.9	234.8	5.131	32.67	85
ss	213.8	270.1	7.581	46.81	27
ss	192.4	259.6	9.673	54.65	-5
ss	222.8	273.9	4.923	33.28	85
ff	125.7	197.6	8.123	43.47	27
ff	104.1	191.1	9.968	49.86	-5
ff	142.0	199.7	5.482	32.22	85

Table 5: Corner analysis value of the step response at different temperature

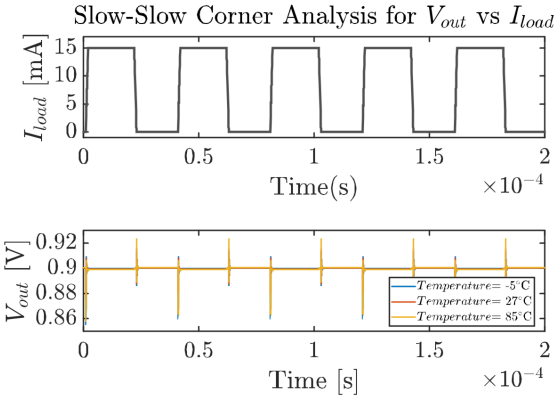
Corner	**Overshoot (mV)**	**Undershoot (mV)**	**Settling time(uS)**	**PSRR(db) @100kHz**	**Temp (°C)**
typical	15.92	19.04	1.24	44.22	27
typical	13.29	19.82	1.58	48.50	-5
typical	23.79	19.96	0.74	37.47	85
ss	13.84	25.02	2.14	34.32	27
ss	13.28	24.23	2.89	38.57	-5
ss	22.79	26.12	1.20	28.52	85
ff	16.25	14.56	0.73	52.39	27
ff	15.92	14.94	0.91	55.69	-5
ff	24.84	19.97	0.45	46.11	85



(a)

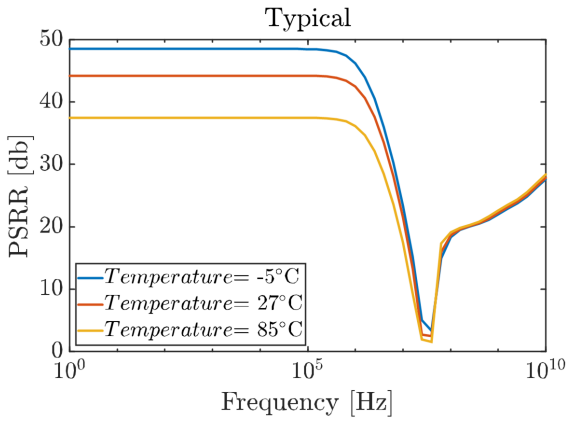


(b)

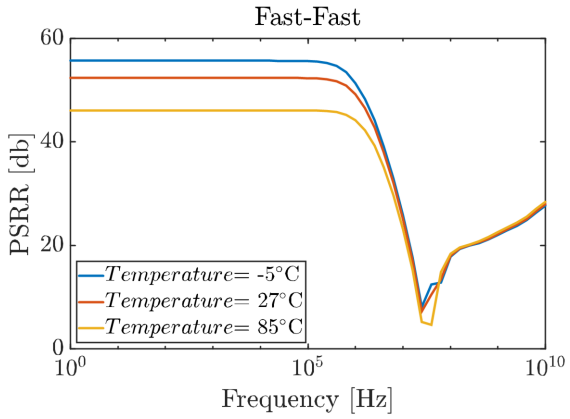


(c)

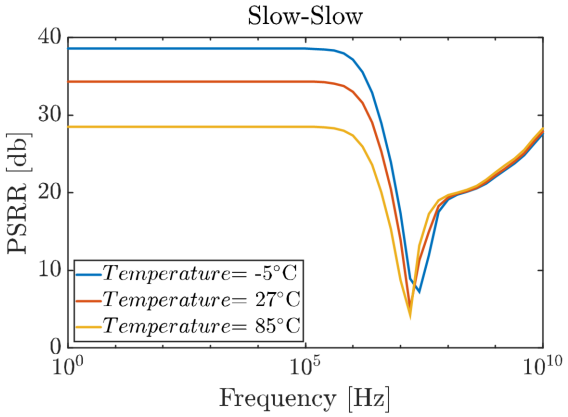
Figure 21: Corner Analysis of the Proposed design with step load for (a) typical (b) fast-fast and (c) slow-slow.



(a)



(b)



(c)

Figure 22: Corner Analysis of Proposed design for PSRR (a) typical (b) fast-fast and (c) slow-slow.

some state-of-the-art prior works is presented in Table 2. As few LDO designs with 45nm technology are available in the literature, we compare with the state-of-the-art LDOs of 40nm, 45nm, and 65nm technologies.

This work offers a variable output range of 0.4-1.0V, which can be obtained by providing an appropriate reference voltage. As some of the key data were not mentioned in the compared prior works, we could not determine the FOM (figure-of-merit). A quantitative analysis is given here for comparison purposes. The line regulation of this work is 1.46X and 14.27X less compared to [25] and [26], respectively and 2.5X more compared to [30]. This work's load regulation is 2.8X less compared to [30], which offers the lowest among the others. The work is having the lowest value of the on-chip output capacitor and therefore has the lowest area. The PSRR of this work is highest compared to other work for up to 100Khz.

Table 6: Comparison with Prior Work

Parameter	[21]EDSSC'12	[30]APCCAS'16	[28]ASSCC'08	[25]CICC'17	[26]ISSCC'14	[31]JSSC'12	**This Work**
	simulated	simulated	measured	measured	measured	measured	simulated
Technology (nm)	65	40	45	65	65	45	45
V_{out} **(V)**	2.7	1.2	0.8	1	1	0.9-1.1	0.4-1.0
V_{drop} **(mV)**	600	300	200	200	150	85	200
Quiescent Current (μ**A)**	N/A	25	N/A	8.33	50	N/A	309
Active Area (mm^2)	N/A	0.036	0.5	0.087	0.023	0.075	0.0052
Max Load (mA)	100	0.4	22.2	25	10	42	15
On-Chip Capacitor (pF)	N/A	80	N/A	10	None	11.2	0.018
On-chip Load Capacitor (pF)	N/A	N/A	N/A	240	130	183	10
ΔV_{out} **(mV)**	N/A	N/A	N/A	45	43	N/A	35
Line Regulation (mV/V)	N/A	1	N/A	3.8	37.1	N/A	2.5
Load Regulation (mV/mA)	N/A	0.025	N/A	0.042	1.1	N/A	0.0089
PSRR (dB)	-65@1KHz -54@1MHz	-43@10MHz	-26@300MHz	-52@1MHz	-22@1MHz	N/A	-65@100KHz

CHAPTER 5

LDO DESIGN IN 180NM TECHNOLOGY

5.1 Proposed LDO Design

For 180nm, we used an additional buffer in the traditional architecture showed in Figure 8a in between the error amplifier and the PMOS pass transistor 23. The desired output voltage is achieved by controlling the gate voltage of the PMOS pass transistor. The purpose of the buffer is to improve the transient response, reduce the noise effect and improve PSRR. Buffer will control the gate voltage of PMOS based on the amplified output of EA. Note that the reference voltage, Vref is an input to the LDO and is connected to the negative terminal of EA, which comes from a bandgap reference voltage circuit.

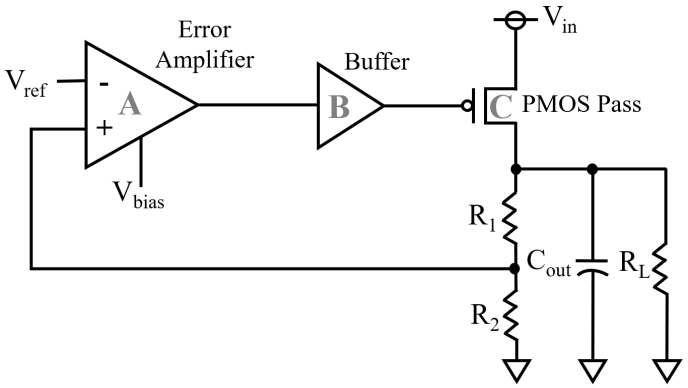


Figure 23: Block Diagram of proposed design in 180nm

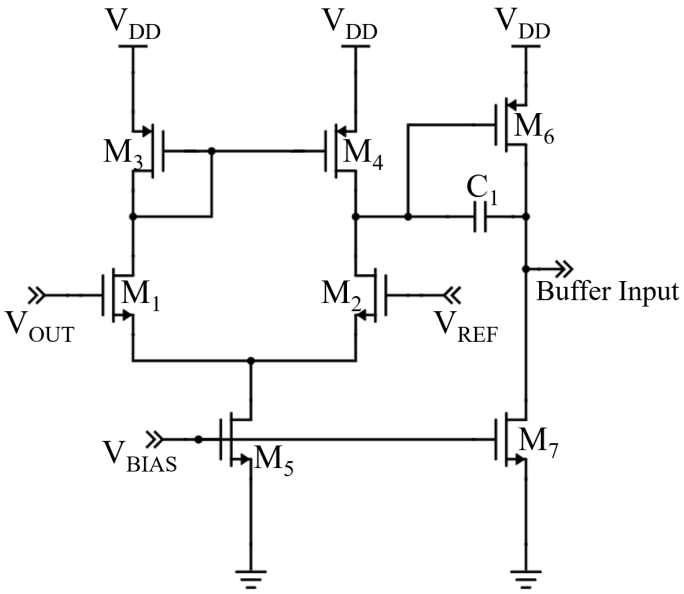


Figure 24: Schematic of Error Amplifier Circuit

5.1.1 Error Amplifier (EA)

Two stage differential amplifier is used here as error amplifier. First stage is a differential pair, and second stage is the common source stage which creates a two-pole system (Figure. 24). A miller capacitor of 500fF is used for stability purpose here. M_5, M_7 are the biasing transistor which are properly biased by biasing network. The error amplifier compares the output voltage of the LDO with reference voltage and generates an error signal which feeds to the buffer.

5.1.2 Biasing Circuit

Biasing Network is basically a beta-multiplier circuit with a differential pair in between the current mirrors to reduce the sensitivity over supply voltage (Figure. 25).

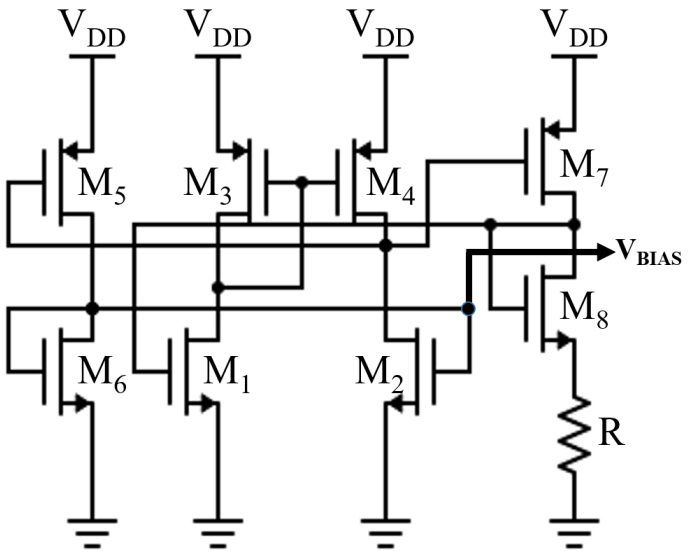


Figure 25: Schematic diagram of supply independent biasing network.

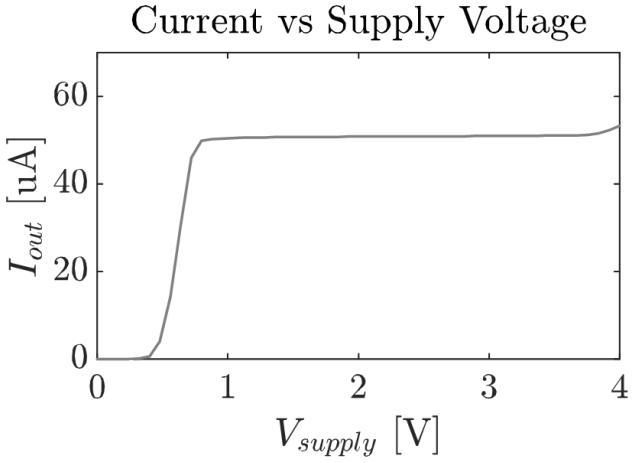


Figure 26: Output current of the supply independent biasing network.

The biasing network is designed to ensure the proper operation of each transistor in the circuit. Linear circuits involving transistors typically require specific DC voltages and currents for correct operation. As an example, for an amplifier, this requirement means that the transistor must stay in the saturation mode and avoid triode or cut-off.

M_1,M_2,M_3 and M_4 are the differential pair and M_5,M_6,M_7 and M_8 constitutes the current (Figure. 26). A resistor R is having a value of 1.35KÎ© used in the source of M8 to accurately set the output current.

5.1.3 Buffer

Buffer circuit is also known as voltage follower. As showed in Figure. 27, M_1 and M_2 compares input and output signal of the buffer and maintains the input voltage at the output. Here, M9 act as a diode-connected load.

5.1.4 Pass Transistors

The PMOS pass transistor is the primary driver switch of the proposed design, Pass transistors are chosen with considerable sizing value to provide a sufficient amount of current to the load. Depending on the reference voltage, the output voltage is regulated by controlling the pass transistor's gate voltage.

5.1.5 Resistive Feedback Network

The regulatorâs output voltage is sensed through the voltage divider network R_1 and R_2 (Figure. 23) and feedback to the error amplifierâs input. Feedback network works as a sample circuit in voltage regulator.

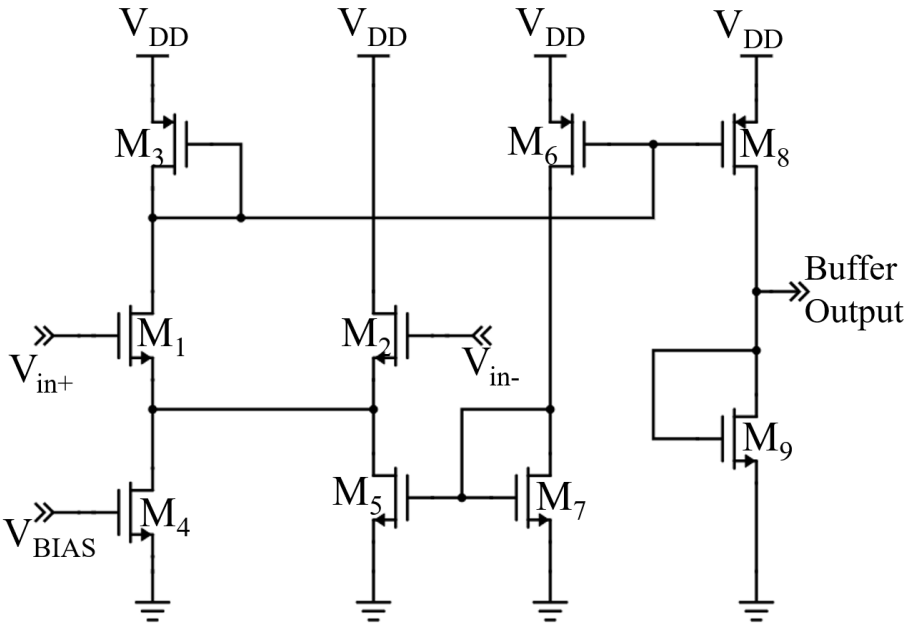


Figure 27: Schematic of Voltage follower/Buffer Circuit

5.1.6 Simulation Environment

The LDO in this work is designed using 180nm TSMC CMOS technology in Cadence Virtuoso. For design rule check (DRC), layout vs schematic (LVS) and paracitic extraction, Calibre is used. The chip is now with MOSIS for fabrication.

5.1.7 Design Specification

The design specification of the proposed design is presented in the table. The supply voltage is 1.8V with a maximum load current of 20mA. A capacitor having a value of only 1pf is used at the output of the design. The proposed LDO achieves a minimum dropout voltage of 200mV. The overall specification of the proposed design is

Table 7: Specifications of the Proposed LDO

Parameter	**Specification**
Input/Output Voltage	1.8V/0.8-1.6V
Voltage Overhead	$<$5mV
Line Regulation	0.043 (mv/V)
Load Regulation	0.0001 (mV/mA)
Load Current	20mA (max)
C_{out}	1pF (on-chip)
ΔV_{out}	2.78mV
Area	$0.018mm^2$
PSRR	max 88dB @100KHz

summarized in Table 7.

5.1.8 Layout of the Proposed Design

The layout of the proposed design is implemented in Cadence Virtuoso (Fig. 12). DRC and LVS checks are done with the Caliber tool [51]. The total active area of the design is $0.018mm^2$. The layout with all the capacitors and transitors are shown in Figure. 28, all the transistors and the inputs are annotated. Metal 1, Metal 2, and Poly are used here for all cell level layout. For capacitor, Metal 5 and Metal 6 are used.

5.2 Modeling Frequency Response of The Proposed Design

In this section, we present the modeling of the proposed design's frequency response using its small-signal equivalent model.

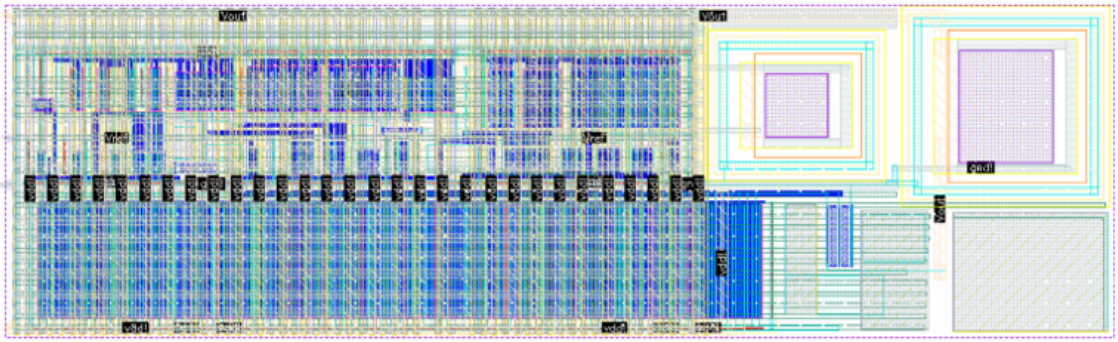


Figure 28: Transistor level layout of the proposed design with capacitors

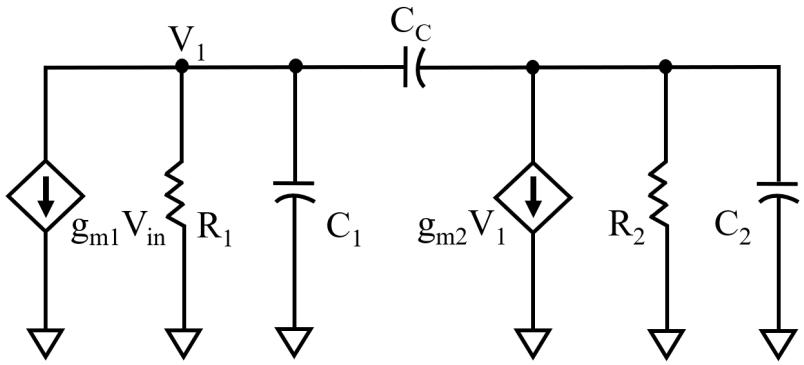


Figure 29: Small signal equivalent circuit of two stage Error Amplifier

The cascaded structure of the differential stage and common-source stage constructs a second-order two-pole system, leading to instability of the design [52]. Therefore, a compensating capacitor is needed. We have considered a capacitor of 500fF as a miller capacitor between two stages in this work. This capacitor creates a large separation between the dominant and non-dominant pole and ensures better stability. The small-signal equivalent model is represented in Fig. 29. The gain and poles equations are

presented by 5.1 to 5.7. Here, the dominant pole resides on the output of the EA.

$$R_1 = r_{ds4} \| r_{ds2} \tag{5.1}$$

$$R_2 = r_{ds6} \| r_{ds7} \tag{5.2}$$

$$C_1 = C_{db4} + C_{db4} + C_{gs7} \tag{5.3}$$

$$C_2 = C_{db7} + C_{db6} \tag{5.4}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m1} g_{m2} R_1 R_2 (1 - \frac{sC_c}{g_{m2}})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \tag{5.5}$$

$$\omega_{p1}(Dominant) \cong \frac{1}{g_{m2} R_1 R_2 C_C} \tag{5.6}$$

$$\omega_{p2}(Non - dominant) \cong \frac{g_{m2}}{C_1 + C_2} \tag{5.7}$$

5.3 Simulation and Result Analysis

In this section, we present the transient, DC, and AC analysis of the proposed design. The proposed design is implemented and simulated in Cadence Virtuoso Simulator using 180nm TSMC CMOS process.

5.3.1 Transient Analysis

Transient response is a metric to evaluate an LDO's performance for the change in the input reference voltage and load current variation (i.e., change in the load impedance).

Load regulation is the capability to maintain a constant voltage (or current) level on the output channel of a power supply despite changes in the supply's load. To evaluate the LDOâs load transient response to change in the load current, we consider a step in the load current of 20mA with 10ns for both rise and fall time with the desired regulated V_{out} = 1.6 V. Fig. 30 shows the corresponding result.The maximum deviation observed is 2.78mV. The load regulation of the proposed design is measured at 0.0001 (mV/mA).

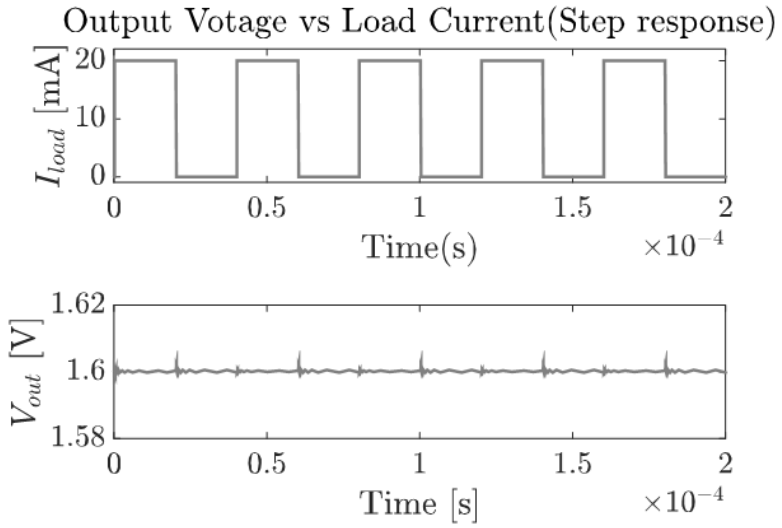


Figure 30: Load transient response of the proposed regulator with a step of load current from 0 to 20mA.

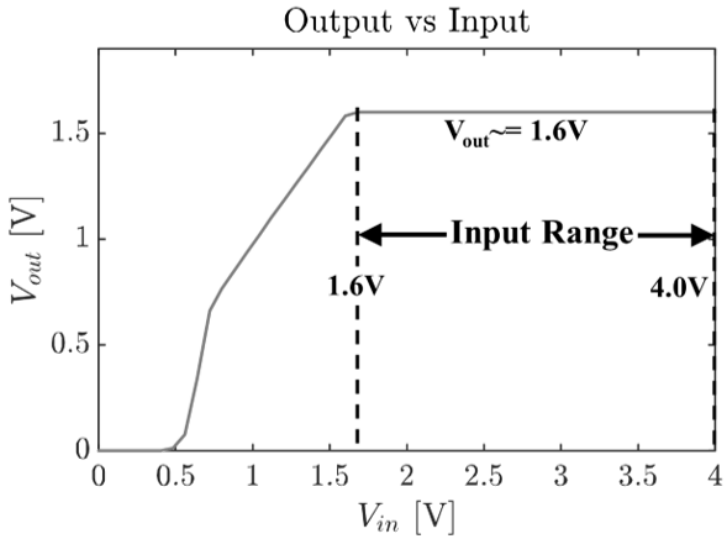


Figure 31: Line regulation of the proposed design.

5.3.2 DC Analysis

DC analysis is a metric which evaluates the operating region, line regulation etc. of a LDO.

Line regulation can be defined as the percentage change in the output voltage for a given change in the input voltage. To evaluate LDOâs line regulation, we perform a DC analysis to observe output voltage variation by varying the input supply voltage.Fig. 31 shows the corresponding result. We calculate the line regulation as 0.0043. That means each voltage change at the input changes the output by only 43mV.

5.3.3 AC and Stability Analysis

The frequency response of the circuit is presented in Fig. 32. In the design, Butterworth optimization is chosen since precise regulation is required across the passband

to regulate the transistors' gate voltages. As depicted by Fig. 32, Butterworth architecture provides maximum passband flatness. The two stage error amplifier has a 73.33 gain and 82.83° phase margin. The whole system's overall gain is close to half as V_{out} is fed to error amplifier through resistive feedback network. It indicates that the overall system is stable under full load conditions.

Fig. 33 shows the PSRR plot of the proposed design for 1mA, 10mA, and 20mA of load current. The maximum PSRR we observe is 88db until 100KHz for 1mA load current.

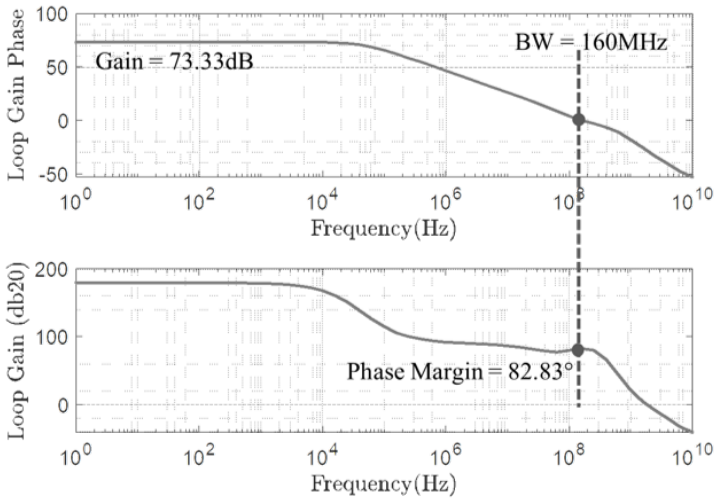


Figure 32: Frequency response of the two stage error amplifier

5.4 Comparison with Prior Works

A comparative analysis of the proposed LDO with some state-of-the-art prior works is presented in Table 2. This work offers a variable output range of 0.8-1.6V,

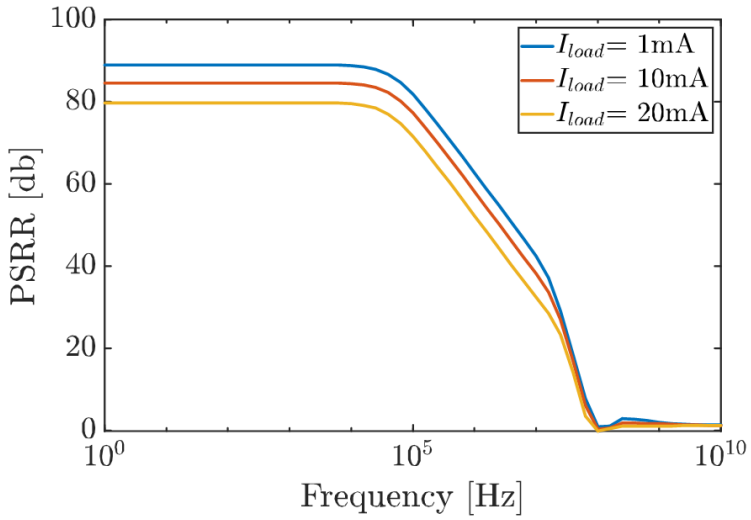


Figure 33: PSRR plot of the Proposed LDO Design.

which can be obtained by providing an appropriate reference voltage. The proposed design shows better result in-terms of line regulation, load regulation and PSRR which are the most important metrices of an LDO regulator. Moreover we get a wide range of output voltage compared to other designs.

5.5 Application

The proposed design of LDO regulator in 180nm is used in a memory security application. This is a collaborative work with the hardware security group of Pennsylvania State University. In this work, security for non-volatile memory is proposed by isolating the power pin from the memory array during read/write operation. The memory is powered through on-chip capacitor banks that act as a battery. This isolation effectively

Table 8: Comparison with Prior Work

Parameter	[54]ISSCL'18	[55]TVLSI'19	[56]TPEL'18	[57]TPE'18	[58]JSSC'14	[59] ISSCL'19	This Work
Technology (nm)	180	180	130	130	180	130	180
Vout (V)	1.4-1.6	1	200	200	1.6	0.53	0.8-1.6
Vdrop (mV)	200	200	1-1.4	1.2	200	50	200
Active Area (mm2)	0.21	0.055	0.0042	0.0046	0.25	N/A	0.018
Max Load (mA)	50	200	25	50	50	3	20
Output Capacitor (pF)	50	100	25	400	100	120	1
âVout (mV)	158	117	284	132	75	120	2.78
Line Regulation (mV/V)	0.857	0.283	2.25	0.3	N/A	29	0.043
Load Regulation (mV/mA)	0.248	0.077	0.17	0.01	0.14	1.2	0.0001
PSRR (dB)	-70@1KHz	-37.3@1MHz	-57@1MHz	-64@1MHz	-70@1MHz	N/A	-88@100KHz

eliminates the side channel signature observed by the adversary (through V_{DD} pin) and thereby, prevents power Side Channel Attack (SCA) with no performance degradation. A VR is used to regulate the output of on-chip capacitor during read/write of the memory. During the charging phase, the V_{DD} source is used to charge a capacitor bank (C). The current observed during capacitor charging does not reveal any sensitive information. Once charged, the V_{DD} pin in isolated and the capacitor voltage is fed to a VR which delivers a constant supply to NVM. Adversary cannot extract side channels since the V_{DD} pin is isolated during the NVM access. The setup is shown in Figure 34.

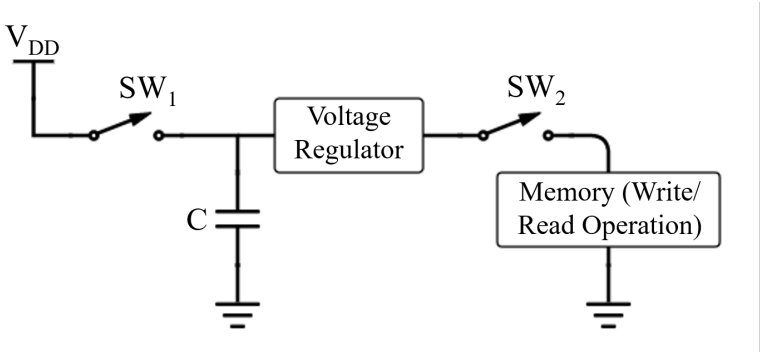


Figure 34: Setup Configuration of the proposed memory security

CHAPTER 6

ANALOG DESIGN AUTOMATION

6.1 Background

Due to the increasing demand for telecommunication/wireless devices in the semiconductor industry, the integration of mixed-signal circuits in System-on-chip(SoC) is booming. Both Analog and RF functions are now integrated into a single chip [60] [61]. The specifications like high performance, low power, low noise, increasing functionality are becoming more stringent in integrated circuits. New technologies are developed to enable an exponential increase in IC density and meet the specifications mentioned above. The complexity of designing an integrated circuit is increasing day-by-day with technology shrinking. Thus the productivity is slowing down. This phenomenon is referred to as the design productivity gap. New Computer-Aided-Design (CAD) tools and methodologies are being developed to improve the designers' productivity and lessen the design productivity gap. Though analog circuit usually occupies a small fraction of the total chip area (less than 20%), the analog circuit's design time is significantly higher than the digital circuit because of the complexity. Besides, digital intellectual property (IP) can be reused, and it is a standard practice supported by well-established automated methodologies and synthesis tools, which enables increasing design productivity.

In analog/mixed-signal designs, there are many rules and strategies associated with the design to achieve the desired specifications. Design methodologies and CAD

tools for analog design are not matured enough to support complex analog design flow. As analog design parameters(such as power dissipation, DC gain, bandwidth, phase-margin, slew rate, noise, power, area, etc.) are more sensitive to the fabrication process than the digital circuit, reuse of analog IP is challenging and costly. Second-order and third-order effects are more crucial in analog circuits than the digital circuit [60] [62]. With multiple parameters, each analog cell produces hundreds or thousands of various performance measures [60]. Therefore, reusing one analog design from one technology to another with the same design parameters requires a redesign of the circuit significantly [62]. As the technology or the project's specification and rule changes, the analog circuit libraries became obsolete for the next generation. Though there is a significant amount of research and progress seen during the last couple of decades, analog design methodologies and tools are still far from a well-developed stage like the digital counterpart.

A clear definition of a hierarchical design flow is essential to handle the increasing complexity of analog and mixed-signal IC design. The analog design automation (DA) tools still cannot support the whole analog design flow as tools only concentrate on each part individually, and they need intervention from experts. Moreover, tools generally address circuit-level synthesis, making it challenging to implement in complex and large circuits. Hence, hierarchical design mostly implements in design methodologies nowadays, just like the manual design approach to applying a divide-to-conquer strategy. The trend to design an automation method will consider three aspects to improve [1]:

- The methodology will have the flexibility to deal with multiple architectures or circuits and interact during the synthesis process.

- The methodology will use different tools and techniques to do various design steps(such as topology selection, circuit sizing, layout etc.).
- The methodology will handle intricate systems and implement strategies having multiple abstraction levels.

For the last few decades, researchers are relentlessly working on finding a complete design methodology and an efficient tool to make the complete analog design automated. Few sizing methodology and tools are developed in [63] [64] [65] [66] [67] [68]. We mainly concentrated on the circuit-synthesis part of the hierarchical analog design automation flow in this work. We proposed an optimization methodology to synthesize an analog circuit accurately and efficiently in each design step (such as topology selection, sizing transistors, etc.). We used one supervised learning method, random forest tree, and the symmetrical constraints to minimize the design space point. The circuit synthesis flow will consume less time and give an optimized solution. The proposed methodology is a combination of learning and simulation-based optimization, which has the flexibility to work with different technologies. We also developed a tool to execute the complete synthesis methodology properly.

6.2 Analog design Flow

Two approaches are usually followed to design an analog system; flat and hierarchical. In a flat approach, the whole circuit is designed altogether. As the analog system's complexity and dimension are increasing day by day, it has become a less popular option among the designers. In a hierarchical approach, designers follow the divide-to-conquer

strategy. The hierarchical approach is divided into two flows: top-down design flow and bottom-up verification flow [62] [2] [69] [70] [71] [72]. Each flow has several levels of steps with a set of design tasks [62] [2] [69] [70]. The hierarchical approach is now widely followed in handling the complexity of analog and mixed-signal integrated circuits. A general design flow of analog/mixed-signal systems is presented in Fig. 35 [1]. A brief description of each step is given below:

6.2.1 System-Level

System-level is the first level of developing an analog/mixed-signal system. At this level, the technology process, the objectives, and the system specifications are addressed. The whole system's structure is designed and partitioned into several high-level building blocks for the next stage. The different system specifications are mapped into intermediate-level parameters that become the lower-level building blocks' specifications in this stage. These partitionings and specifications are validated using different suitable high-level behavioral tools or simulation tools, such as MATLAB, Verilog AMS, etc.

6.2.2 Block-Level

In this stage, the high-level building blocks are translated into functional blocks' architecture to realize the specific behavioral description. These functional blocks are then described separately using appropriate hardware description language (such as VHDL and VHDL- AMS). Then they are tested for the required specifications using different behavioral simulations tools like Ultrasim, NcSim, Hsim, Modelsim, etc.

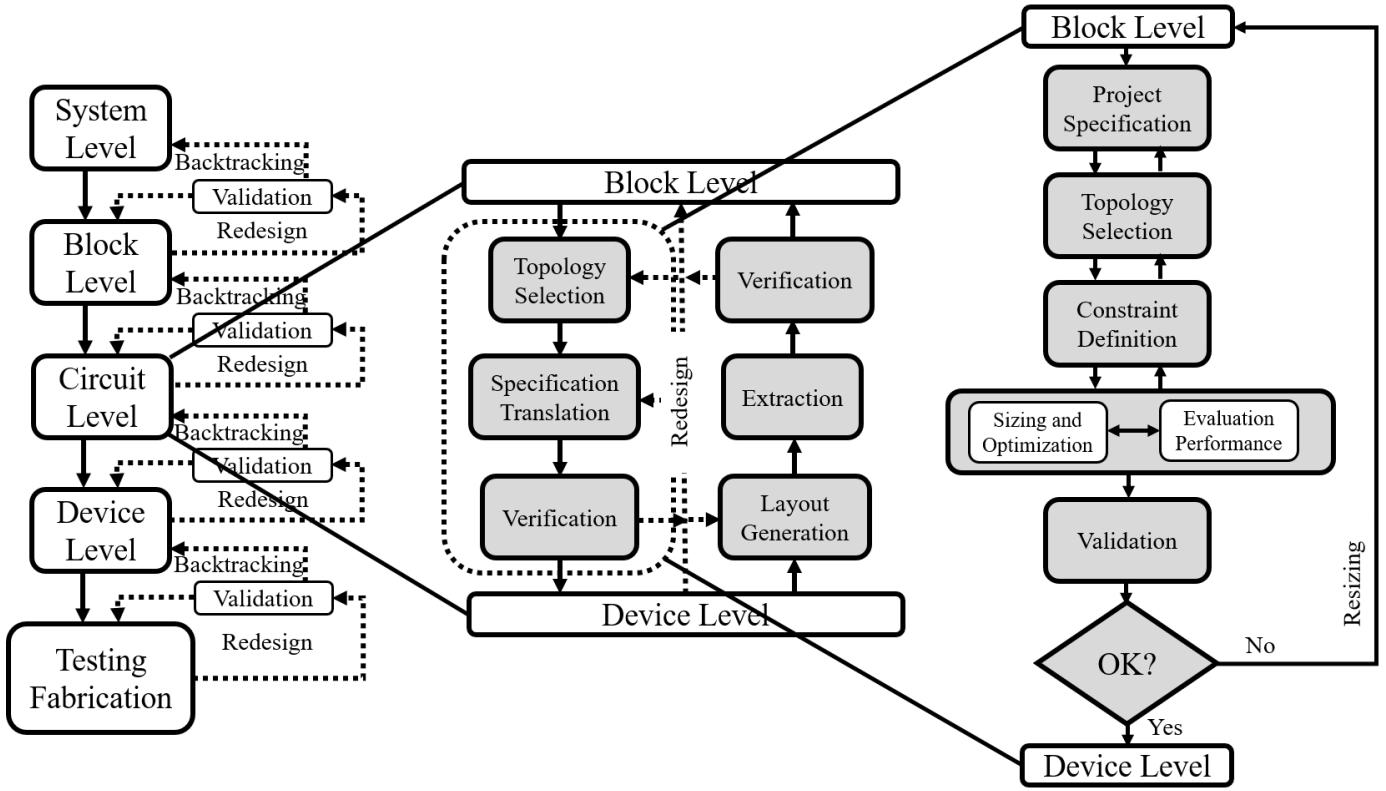


Figure 35: Analog Design flow highlighting top-down circuit-level design flow [1] [2]

6.2.3 Circuit-Level

Here, each analog functional blocks are optimized according to a given optimization process. This optimization process is based on the acquired specifications and technology process from the upper level. It is an iterative process that determines the physical dimensions at the device level. This stage has two primary objectives: to select the appropriate circuit topology and to obtain the proper sizing parameters of the circuit elements. For a robust design, different process variations and device tolerance are taken into account to ensure a high-yield design. The final circuit is then tested against the required performance specifications using circuit-level simulator tools such as HSPICE and Spectre.

6.2.4 Layout hierarchy

During this phase, the optimized functional blocks achieved from the circuit-level schematic are transformed into a multi-layer layout. The circuit layout is the physical representation of the circuit that contains the circuit elements' planar geometric shapes and maintains the design rules specified by the fabrication process. The circuit layout, which is obtainable either manually or automatically, is optimized for minimum area and some other design specifications. A verification phase is then done to check for design rule error known as Design Rules Check (DRC). The DRC is followed by an LVS check (Layout vs. Schematic) where the layout and schematic design is matched for input/output pins. After that, the layout parasitics are extracted, whose effects are checked with circuit simulations so that the circuit performance does not vary substantially from the target

specifications.

6.2.5 Fabrication and Testing

Fabrication and testing is the final stage where IC produces by a series of mask generation. Several precise quality tests are associated with the whole fabrication process to avoid defects in the chip. Test bench, along with a test setup, tests and verifies the circuit's correct operation.

These hierarchical abstraction levels are blended with a top-down and bottom-up approach with a redesign or backtracking iterations [2] [73] as illustrated in Fig. 35. Our primary focus is to implement the design methodology at the Circuit-level of the hierarchical strategy. Hence, we are only discussing the top-down and bottom-up flow at the Circuit-level. The top-down flow has the following steps:

1. Topology selection: The circuit topology is chosen in this step to meet the specifications coming from the system and block level in the hierarchy. The selection can be made manually from a database using heuristic rules. In this method, each topology's feasibility in the database is realized to see if a particular topology can meet the required specification. Another approach is called an optimization-based approach [74], where topology selection is combined with the device sizing step.

2. Specification translation/Sizing: In this step, an optimized design with all the required specifications is sought from the selected topology. The specifications coming from the upper level are translated into the system's sub-blocks and eventually

depend on the transistors' sizing in each sub-block. In higher levels of the design hierarchy, this process implements the block's decomposition under design in a subset of specifications that are passed down in the hierarchy tor each sub-block in such a way that the actual block meets its specs. For the lowest levels in the hierarchy, where the sub-blocks are materialized in single devices (transistors, resistors, etc), circuit sizing occurs according to the performance specs and the selected topology received from upper levels. There are two main approaches: the knowledge-based approach and an optimization-based approach relying on different optimization methods.

3. Synthesis Verification: After proper sizing of the transistors in each block, the simulation and verification start to see if the optimized design meets the required specifications. If the desired performance is achieved, the design flow advances to sub-blocks of the lower level in the hierarchy. Otherwise, the whole flow restarted inside the same hierarchical level for redesign or other hierarchical levels for backtracking.

The bottom-up flow layout performs the next steps:

1. Layout Generation: Physical layout of each sub-block is generated and optimized in this step, considering all the design constraints.

2. Extraction: After successfully passing the DRC and LVS, the layout is extracted to approximate the fabrication's effects on the circuit's performance, called parasitics.

3. Layout verification: In this step, the extracted layout is simulated and verified to

quantify the layout parasitics' effects on the circuit's overall performance. Because of the parasitics, the extracted view simulation might largely deviate from the schematic simulation. In that case, the redesign process will involve the associated blocks in the same or different hierarchy levels.

CHAPTER 7

PROPOSED ANALOG DESIGN METHODOLOGY

7.1 Methodology

In this work, we proposed the design methodology to implement in the circuit-level of the hierarchical flow. The detailed methodology flow is shown in Figure 36. We explained the top-down flow and showed how we could incorporate the bottom-top flow in our proposed methodology.

7.1.1 Topology Selection

One of the critical factors for achieving a high-performance design is choosing an appropriate architecture [75]. Based on the specification parameters, the topology will be selected from a predefined library having a particular group of circuits with the required functionality. The proposed algorithm has two phases: learning and evaluation. The proposed methodology would start with the simplest topology and go ahead with the next one if the first one failed to meet the specification parameters in the learning phase. The predefined library will be prepared with only the possible topologies suitable for the requirement. This preparation will save some computing time by not including unnecessary topology to check.

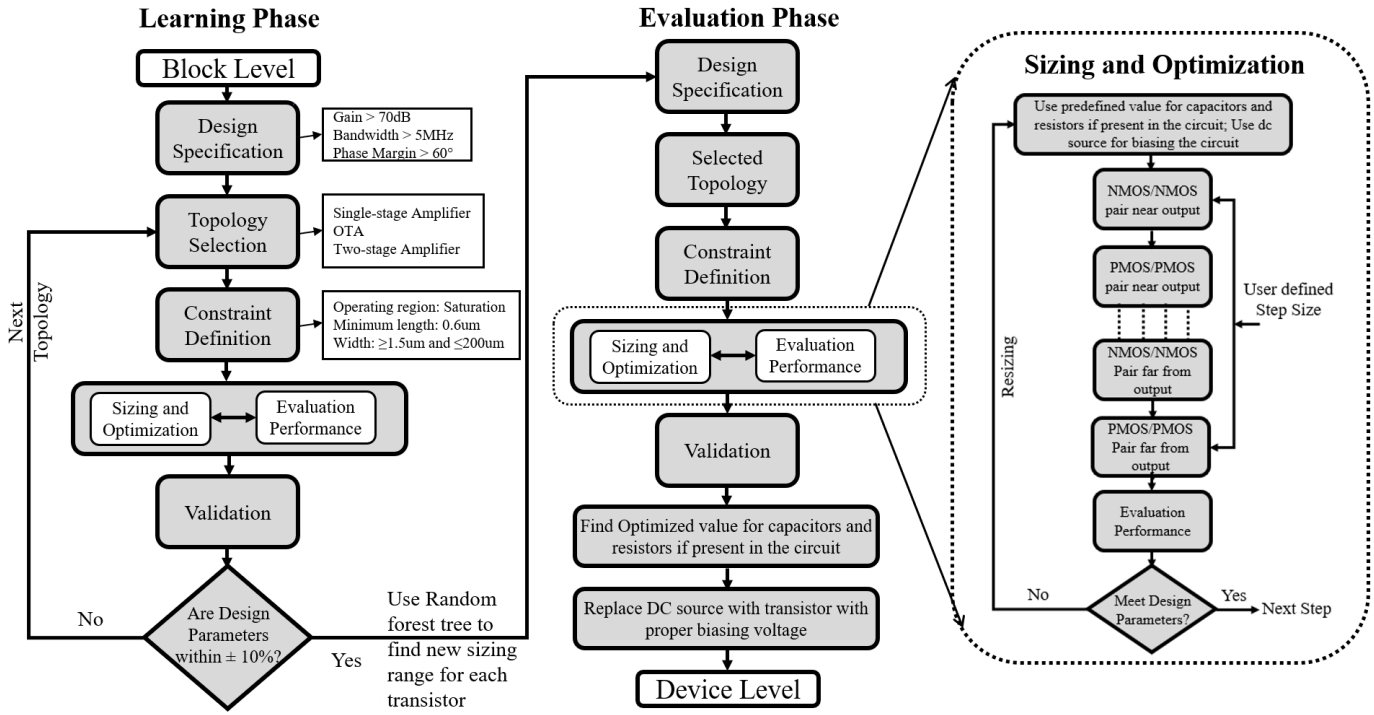


Figure 36: Proposed circuit synthesis methodology flow

7.1.2 Sizing Automation and Performance evaluation:

The device/circuit performance is mostly dependent on the sizing of its transistors. There are two well-known approaches usually practice in the industry for transistor sizing.

7.1.2.1 7.1.2.1 Knowledge-based approach

In this approach, the whole system is considered altogether to characterize and plan how each sub-block should design to meet the overall system specifications [62] [76] [77] [78]. This method's primary purpose is to utilize the designer's knowledge, develop a preliminary design plan with equations, and design tactics to find the sizing to meet specific parameters. This approach's major drawback is the massive overhead regarding defining a new design plan for each new topology and new technology. The whole process is very time-consuming, and getting an optimum solution is not a sure thing.

7.1.2.2 7.1.2.2 Optimization-based approach

An optimization methodology is applied in this approach to complete the design tasks. This method is an iterative process where different transistor-sizing/design variables are used in each iteration until all the design specifications have met. The optimization algorithm explores the design space to find the appropriate sizing for each transistor, and the evaluation tool verifies if all the performance parameters are satisfied. When all the system requirements are satisfied, the transistors' sizes at that iteration use as a solution to design the selected topology. There are three techniques to efficiently guide

the search mechanism to evaluate and minimize the iteration number in the optimization process. These are equation-based optimization, simulation-based optimization, and learning-based optimization.

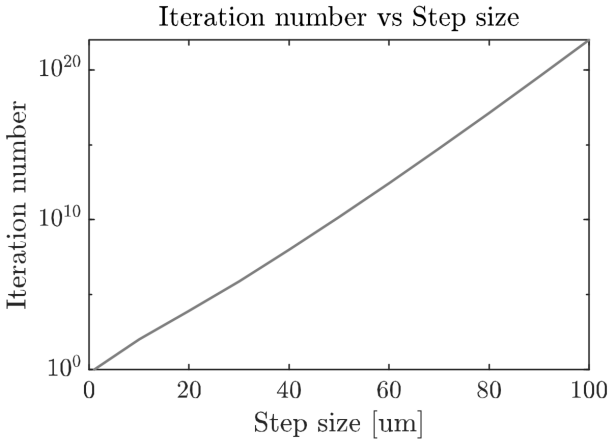
For the sake of time and accuracy, we chose an optimized-based approach. We combined simulation-based and learning-based optimization to develop the algorithm to minimize the iteration number. The algorithm will synthesize and find the optimized value in three-step: find optimized transistor sizing, find other component value, and find the proper size and bias voltage for biasing transistor. The learning phase will have only the first step, but the evaluation phase will have all three steps. The first task is to identify the mutual transistors in the test topology, which will drastically reduce the overall iteration number based on the topology's mutual transistor pair number. A good starting point is critical to get the least number of iterations, leading to less computational time and resources. So instead of choosing a transistor and its size randomly, we choose the transistors pair near the output and gradually go to distant transistors/transistor pairs. In this way, the model can closely observe how the design parameters change and make the algorithm more optimized.

Our proposed methodology's first phase is to create a learning environment and run the flow with a predefined step size. The step size will be chosen based on the transistor number in the circuit. Large step size should be selected if the transistor number is high to reduce the learning phase's iteration number. Then using random forest, we can reduce the design space. Then the flow will continue by using the reduced design space for the evaluation phase. It will save time as well as give an optimized design. If the

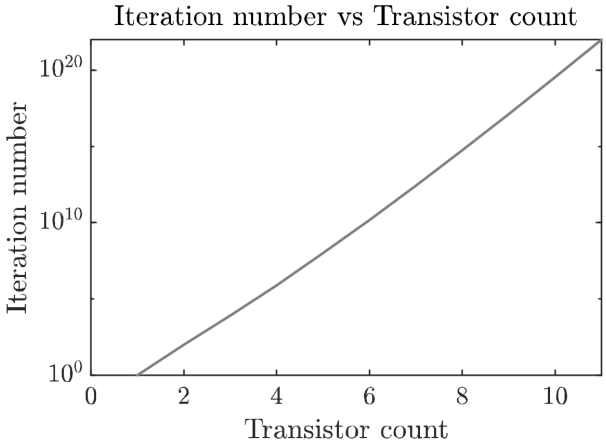
topology has components other than transistors (such as capacitor, resistor), some predefined values will be used for those components during the learning phase. Resistors and capacitors introduce poles and zeroes in the analog circuit. These poles and zeroes affect the phase margin, thus the stability of the whole circuit. These components' value will be identified through iteration during the algorithm's evaluation phase after optimizing the transistors sizing to meet the phase margin requirement. In the end, the biasing transistors will come into the picture and will find the proper sizing for that using simulation in the evaluation phase. If one topology does not meet the design requirement in the learning phase, the following topology will be chosen. In this way, time and resources will be saved by not evaluating a topology with vast design space, which is one of the significant advantages of the proposed methodology.

We used supervised learning to limit the transistor sizing from the initial range to reduce the design space point between the learning and evaluation phases. This way, the whole sizing automation process will go through a lot less number iteration without losing any optimized solution. Random forest tree is supervised learning we used in our methodology to reduce the transistors sizing range.

Random Forest: Random forest or random decision forest is a learning method that operates by constructing multiple decision trees during the training phase of a given dataset. The random forest chooses the decision of the majority of the trees as the final decision. The decision can come out in the mode of classes or mean prediction of the individual trees [79]. Random forest can perform efficiently in an extensive database and give the most accurate result. It can operate on thousands of input variables and can offer



(a)



(b)

Figure 37: Relation between iteration number and a) transistor step size b) transistor count.

to detect variable interaction. These features are highly required to analyze a complex circuit dataset with many transistors where each design specification depends on each transistors' individual and mutual performance. Lastly, Random forest does not overfit, and it is fast to train a dataset. These are reasons for choosing this learning method in our proposed methodology.

How we should choose the step size?: The step of transistor size can be chosen by the user in both phases. With the increase in step size, the computation time decreases as well as the accuracy. Usually, the iteration number to find all the combinations of transistor sizing in topology is a^n, where 'n' is the number of transistors and 'a' is the number of step size. There are eight transistors in the second topology (Figure 39). So with a 5um step size, there will be forty steps, and the total iteration number should be $6.56x10^12$. Even if a condition is put in the usual way based the specifications, there will be no control over the flow, and the user might have to wait for an optimized solution for an indefinite time. The lowest iteration number is also dependent on how the iteration loops are structured. We placed the transistors in different position of the iteration loop and the proposed the way which gave the best result in terms of iteration and time as well. The plot shown in Figure 37 explains how iteration number increases with the transistor count and step size. In the y-axis of the plots, logarithmic data is shown for better visualization. Iteration number will exponentially increase if either transistor step size or count increases. As execution time is proportional to iteration number, if iteration number increases so thus the execution time. Based on the plot, we cay say that if we can decrease the iteration number, we will find the optimized solution in less time. Besides,

step size will also determine the accuracy of the algorithm we are using. The more the step size, the wider will be the design space and the less accuracy we will have. So based on the requirement, user should choose step size carefully.

To incorporate the proposed methodology in bottom-up flow, we need to estimate parasitic in the selected topology and add them during the sizing automation to evaluate the circuit performance properly. To get the estimation, we need to complete the whole top-bottom and bottom-top flow once with the sizes we can get from the proposed methodology's learning phase. We can choose the point closest to the required specification in the design space to pursue the bottom-top flow. We could not verify the bottom-top flow because of the lack of a layout automation tool. That is why this is out of the scope of this work.

7.2 Implementation of the proposed methodology

In this section, we presented the implementation of the proposed methodology. Three sets of specification parameters were chosen, which can be met by an operational amplifier to show how the proposed methodology performs to find an optimized solution. The design specification parameters are summarized in Table I. We are assuming that all the transistors should be operating in the saturation region. We used a fixed length of 0.6um for all the transistors in all topologies, and the biasing current is 25uA.

We consider a single-stage differential amplifier, an operational transconductance amplifier (OTA), and a two-stage differential amplifier for topology selection and include

Table 9: Three set of Design Specifications

Parameters		Specification 1	Specification 2	Specification 3
Technology (um)		0.6	0.6	0.6
Target Topology		Single-stage Differential Amplifier	Operational Transconductance Amplifier	Two-stage Differential Amplifier
Supply voltage (V)		5	5	5
Sizing range (um)	Width	<200	<200	<200
	Length	<1.5	<1.5	<1.5
Minimum Size (um)	Width	1.5	1.5	1.5
	Length	0.6	0.6	0.6
Biasing Current (uA)		25	25	25
Load (fF)		200	200	200
Unity Gain bandwidth (MHz)		>150	>500	>5
DC Gain (dB)		>35	>40	>70
Phase		>60	>60	>60

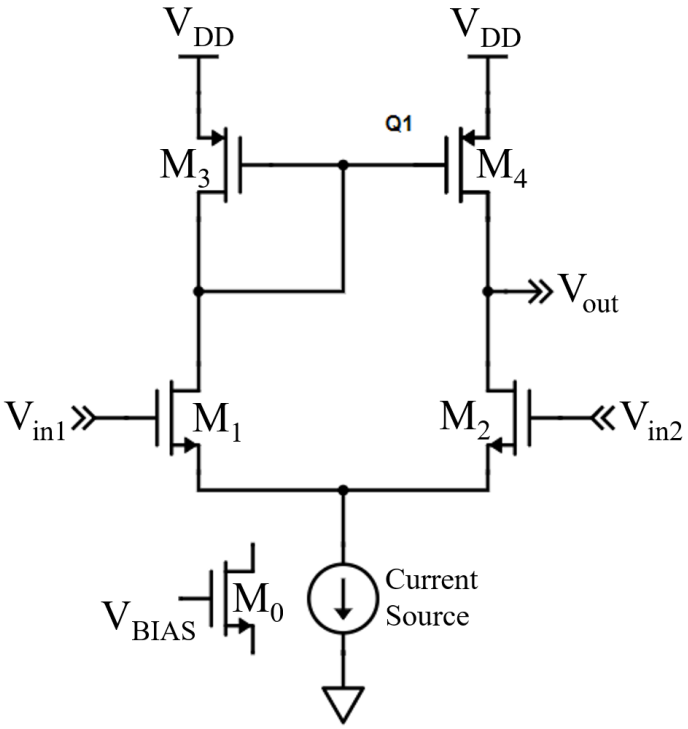


Figure 38: Circuit diagram of a Single-stage Differential Amplifier

them in the predefined library. The specifications are set in such a way that each topology will meet one single specification set. The algorithm will start with the differential amplifier, as this is the simplest one.

The circuit diagram of a single-stage differential amplifier is shown in Figure 38. The circuit consists of two transistors pairs; one pair of NMOS (M1 and M2) and one pair of PMOS (M3, M4). Each mutual pair will have a similar sizing throughout the algorithm. As both the pairs are near the output, the NMOS pair will be in the iteration's inner loop, and the PMOS pair will be in the outer loop. For the learning phase, the step we chose is 30u. The range of the transistors' width will come from the design specifications

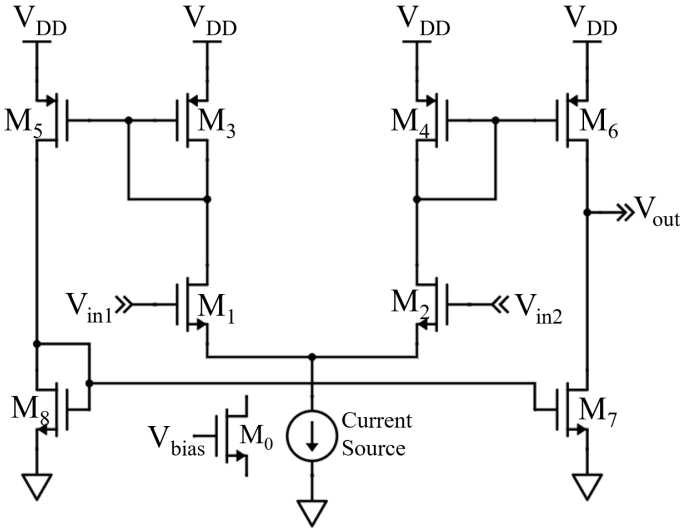


Figure 39: Circuit diagram of an Operational Transconductance Amplifier

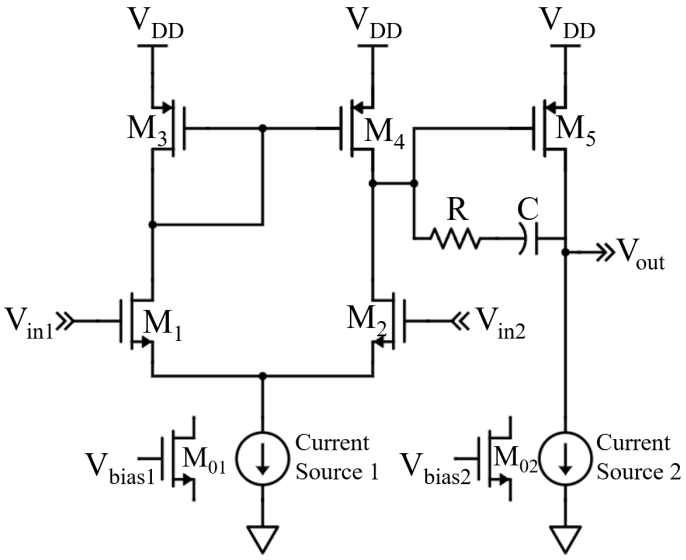


Figure 40: Circuit diagram of a Two-stage Differential Amplifier

parameter. Using the random decision forest, the design space of the transistors' width will decrease. In the evaluation phase, the user can give the step size to get optimized transistors sizing. Here we chose 5u as the sizing step. The single-stage amplifier will meet the first set of design parameters, so the algorithm will not go to the next topology.

The first topology will fail to meet the second set of specifications. The algorithm will determine in the learning phase and eventually choose the second topology and start the learning phase. The circuit diagram of an OTA is shown in Figure 39. There are four pairs of transistors(two NMOS pairs and two PMOS pairs in the schematic. As M6 and M8 are near the output, M7, M8 will be in the inner loop, followed by M5, M6. Then M1, M2, and M3, M4 will be the most outer loop for sizing iteration. As there are four transistors pair, we chose 45u as a sizing step to use a low iteration number during the learning phase. For the evaluation phase, we chose 10u as the step size for achieving optimized sizing. The rest of the settings and methodology flow will be the same as the first topology.

The algorithm will reject the first two topologies during the learning phase and move onto the third topology to meet the third set of specifications. The circuit diagram of the two-stage differential amplifier is shown in Figure 40. Along with two transistor pairs like single-stage, there is an additional transistor (M5), one resistor (R), and one capacitor (C). For the learning phase, a predefined value is chosen for the resistor and capacitor. There will be three iterations because of two transistors pair (M1/M2, M3,/M4) and one transistor (M5). As M5 is near the output, it will be in the inner loop, then M1, M2 in the middle loop, and M3, M4 will be in the outer loop. The algorithm will pursue the

learning and evaluation phase to find the correct sizing of the transistors. The sizing step in learning phase is 30u and 10u is in evaluation phase. Later, two extra loops are needed for the third topology to find the R and C's optimized value after completing the learning and evaluation phase to meet the phase margin requirement.

After finding the optimized sizing and values of the circuit's components, the biasing transistor will replace the biasing current source with proper biasing voltage. A sample random forest decision tree for a single-stage amplifier is shown in figure 41 to show how random forest classification is used in the proposed methodology to find the sizing limit for transistors. As there are two pairs of transistors in the first topology, two decision trees are developed and then combined to get a random forest decision tree. Only one transistor is shown from each pair to develop the tree. The possible outcome is highlighted in bold red color. Note that the tree is developed based on the dataset's point from the learning phase, which gave the specific requirements within $\pm 10\%$.

We organized the dataset obtained from learning phase into two classes. One class represents the data fulfilling the specific requirements within $\pm 10\%$. The rest of them are in class two. We also used two well known classifier support vector machine and naive bias classifier and compared result with random forest algorithm. The accuracy of each algorithm is given in Table 10 and we can say that random forest is performing better than other algorithm.

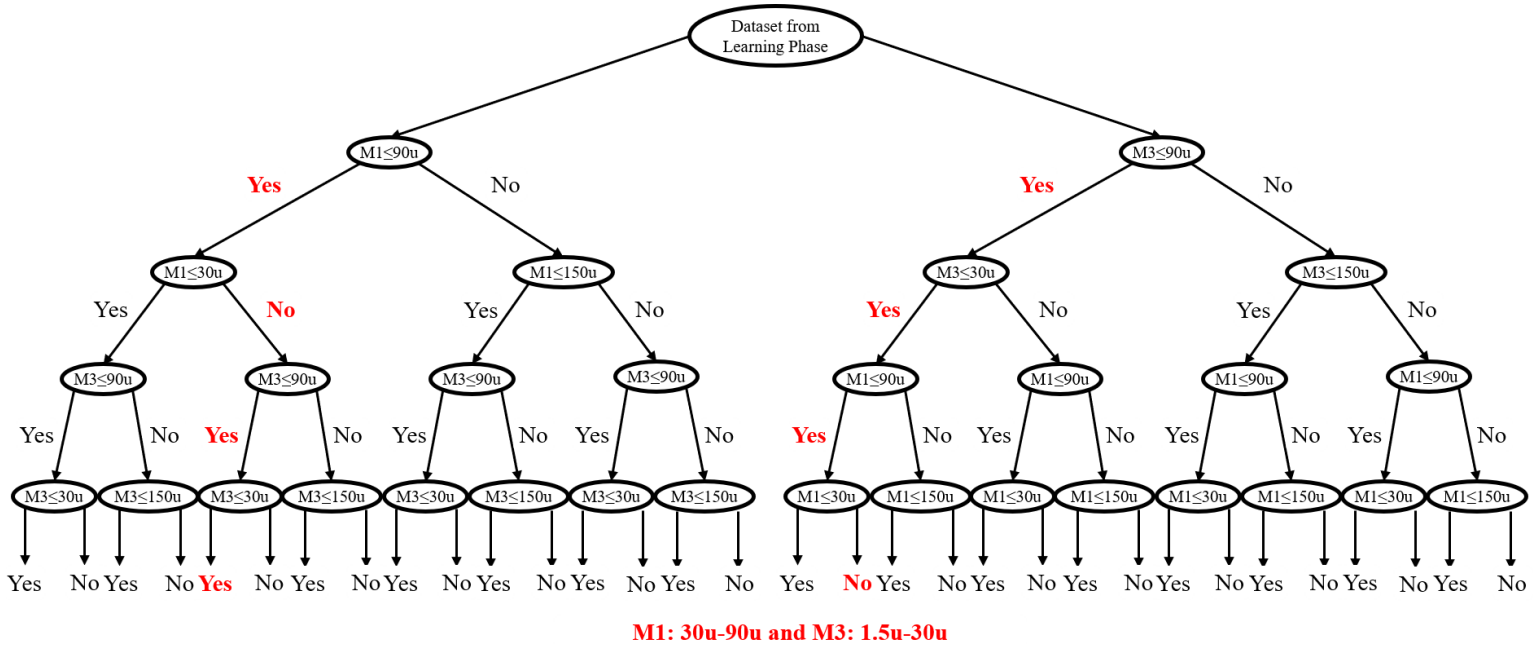


Figure 41: Implementation of Random decision forest for Single-stage Amplifier transistor Sizing

Table 10: Accuracy of three different classification algorithm

Algorithm	**Accuracy**
Naive bias	0.885
Support Vector Machine	0.93
Random Forest	0.993

7.3 Result and Analysis

To control the algorithm flow, we developed a tool using python scripting. For simulation and verification, we used Hspice simulation software. The technology we used here is 0.6um with a 5V supply voltage and 200fF load capacitor. After finding each topology's optimized solution, we verified the result by simulation in Cadence virtuoso. The specifications from Table 9 were used for topology selection and sizing. All the simulations and flow control via the tool is done on an Intel Xeon Linux Machine with 3.10GHz.

Each topology's learning phase and evaluation phase during the sizing algorithm is summarized in Table 11. The table contains the iteration number and time for each phase and showed the reduced sizing limit for each transistor in a topology. The optimized result for each topology coming from the algorithm is verified in Cadence virtuoso. Table 12 presented the specification parameters achieved from Hspice and Cadence simulation with the optimized sizing.

We used Python's Scikit-Learn library to implement the random decision forest in the proposed methodology. After the learning phase, each qualified set of transistors' size used as a dataset to build the random decision forest. A visual representation is presented

Table 11: Iteration number and execution time of the proposed methodology for three diferent topology

		Learning phase				Evaluation phase				Total		
Topology	Transistors	Initial width range	step size	Iteration number	time (s)	New width range	step size	Iteration number	time (s)	iteration number	time	Final size
Single-stage	M1,M2	<200u	30u	81	18.76	30u-90u	5u	14	3.612	95	22.372	30u
	M3,M4	<200u	30u			1.5u-30u	5u					5u
OTA	M1,M2	<200u	45u	625	173.79	45u-90u	10u	81	20.53	706	194.32	75u
	M3,M4	<200u	45u			1.5u-45u	10u					1.5u
	M5,M6	<200u	45u			45u-90u	10u					55u
	M7,M8	<200u	45u			90u-135u	10u					90u
Two-stage	M1,M2	<200u	30u	729	200.45	1.5u-60u	10u	75	18.64	804	219.09	20u
	M3,M4	<200u	30u			30u-90u	10u					50u
	M5	<200u	30u			90u-150u	10u					140u

Table 12: Result comparison between specifications achieved from Hspice and Cadence Simulation

Parameters	Specification 1		Specification 2		Specification 3	
Simulation software	Hspice	Cadence	Hspice	Cadence	Hspice	Cadence
Target Topology	Single-stage Differential Amplifier		Operational Transconductance Amplifier		Two-stage Differential Amplifier	
Supply voltage (V)	5	5	5	5	5	5
Biasing Current (uA)	25	25	25	25	25	25
Unity Gain bandwidth (MHz)	159.87	158.48	535.89	538.56	5.81	5.92
DC Gain (dB)	35.86	35.82	40.04	39.99	72.64	71.3
Phase Margin	74.05	73.11	71.14	68.23	67.46	66.06

in Figure 6 for a single-stage amplifier.

The proposed methodology is entirely dependent on the simulation result. A model file for each transistor type (NMOS and PMOS) is used for simulation. This model file contains all the technology-dependent parameters, and a simulation tool simulates the circuit based on this model file. The whole optimization flow will be the same whether the model file changes or not, and based on the simulation result, the methodology will decide the outcome. As a result, this design methodology can be easily transferable to a different technology node.

CHAPTER 8

ENERGY EFFICIENT FDSOI AND FINFET BASED POWER GATING CIRCUIT USING DATA RETENTION TRANSISTOR

8.1 Background

With the constant scaling of the process technologies, VLSI designers are looking for futuristic way beyond the bulk CMOS to meet the requirements of the industry. Lower node bulk CMOS technologies are experiencing severe short channel effects like mobility degradation, velocity saturation, hot carrier effects, Drain Induced Barrier Lowering (DIBL), back scattering, punch-through etc. To minimize these effects, device structures like Fully Depleted Silicon-on-Insulator (FDSOI) and Fin Field Effect Transistor (FinFET) are currently being used for many applications. The uniqueness of the Silicon on Oxide (SOI) device is the presence of a Buried Oxide layer (BOX) that separates the body of the device from the substrate. The FDSOI and FinFET devices can both be implemented using the BOX structures (see Figure 42 and Figure 43). The main advantage of having the BOX layer is the reduction of the junction capacitance [80]. The reduction of this parasitic capacitance increases the working speed of the device, which in turn gives better performance. The presence of the BOX layer prevents leakage of the charge carriers into the substrate by confining them into the channel itself. This in turn leads to lower power consumption. Several memory designs are proposed in literature with FDSOI and FinFET [81–83]. For energy efficient design, futuristic technology like TFET, CNTFET,

GNRFET etc. are also explored in [84–88]

Leakage currents are the main source of power consumption in the standby mode in high performance integrated circuits. Typically, power gating circuits are used to reduce power consumption and thermal stress due to excessive leakage. Sleep Transistors are usually used in most of the power gating techniques with different configurations to reduce the subthreshold leakage current, which is considered as the major source of the standby power [89]. These sleep transistors, which are added as header and footer switches between the supply lines and the circuits, can be replaced by using double gate FDSOI as logic transistors [90]. The groundbreaking idea of eliminating the sleep transistors and combining the functions of the logic and power gating transistors into the same set of transistors would significantly reduce circuit complexity [90]. However, this new approach is yet to be adopted in the IC design and fabrication process. The technique presented in [90] can be improved and optimized for data retention or minimizing ground bounce noise. In smaller nodes, integrated circuits are becoming even more susceptible to leakages and power supply noises (Ldi/dt noise, IR drop, ground bounce and substrate coupling). The substrate noise is one of the main signal integrity challenges in digital and mixed signal SOCs. Besides, power delivery network introduces the greatest disruption to the substrate in the form of ground bounce. As substrates are highly doped to increase latch-up immunity, they provide a very efficient conduction path for substrate noise, which may lead to large ground bounce. If the value of the voltage surge/droop due to the ground bounce is greater than the noise margin of a circuit, the circuit will give erroneous value or logic level and switch at wrong time [91]. Ground bounce mitigation with

virtual ground scheme is also mentioned in [92]. In this work, we presented a technique where we used a data retention transistor in addition to the header and footer sleep transistors to suppress the ground bounce noise and hold the value during the inactive period of the circuit [93]. We implemented the technique by using FDSOI and FinFET devices and also compared some performance metrics like delay, leakage power and energy between FDSOI and FinFET based implementations using a 2-input NAND gate.

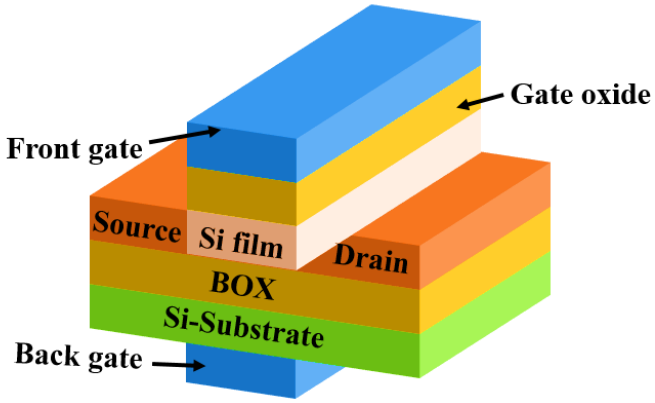


Figure 42: Double gate FDSOI device

8.2 Characteristics of Devices

8.2.1 FDSOI

The simple structure of a double-gate fully depleted SOI FET is depicted in Figure 42. According to the name, it is comprised of two gates whereas the second gate contact (back gate) is created below the substrate. These two gates basically regulate the charges in the channel between the box layer and front gate oxide layer. The idea of double-gate FDSOI technology is to add another conductive layer beneath the SOI device [94].

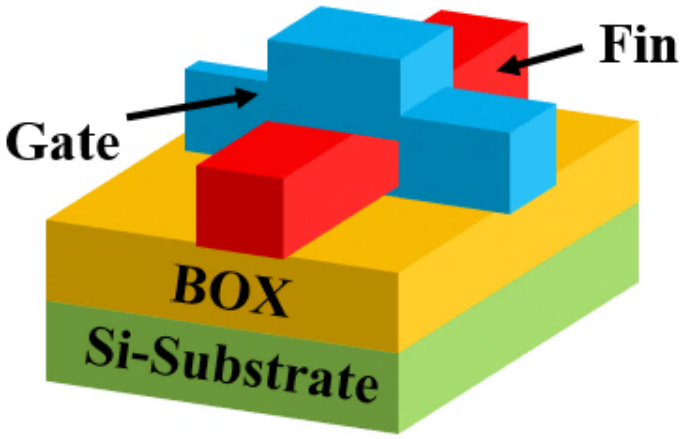


Figure 43: FinFET device on a SOI structure.

There are two categories of commonly used SOI MOSFETs: (i) fully depleted (FD) and (ii) partially depleted (PD) [94]. This work focuses on FDSOI devices for the presented power gating design. The FDSOI ensures much better control of the back-gate on the channel over PDSOI. In the PDSOI, the front surface and channel potential are slightly influenced by the back gate or the substrate.

The silicon film thickness is typically below or equal to half of the depletion width of the bulk device in FDSOI devices [94]. Electrical parameters, especially drain current and threshold voltage of the SOI devices, are influenced by the film thickness. Threshold voltage (VTH) of double gate FDSOI is dependent on the back gate voltage of FDSOI as shown in Figure 3. VTH of FDSOI is given by equation 8.1 and 8.2.

$$V_{TH_F} = V_{FB_F} + 2\phi_B - \frac{Q_b}{2C_{OX}} - (V_{BG} - V_{FB_B} - 2\phi_B + \frac{Q_b}{2C_{BOX}}) \frac{C_{si}C_{BOX}}{C_{OX}(C_{si} + C_{BOX})} \quad (8.1)$$

$$Q_b = -qN_A TT_{SI}(or) + qN_D TT_{SI} \quad (8.2)$$

Where V_{FG} and V_{BG} are front and back gate voltages. V_{FB_F} and V_{FB_B} are front and back gate flatband voltages. C_{OX} is front and back gate oxide. C_{BOX} and C_{si} are buried oxide and depleted silicon film capacitances. Q_b is the area charge density in depleted Si film. From Figure 44, it can be seen that by controlling back gate voltage, we can change the threshold voltage of N-type FDSOI and P-type FDSOI. Threshold voltage is inversely proportional to back gate voltage for N-type devices and directly proportional for P-type devices.

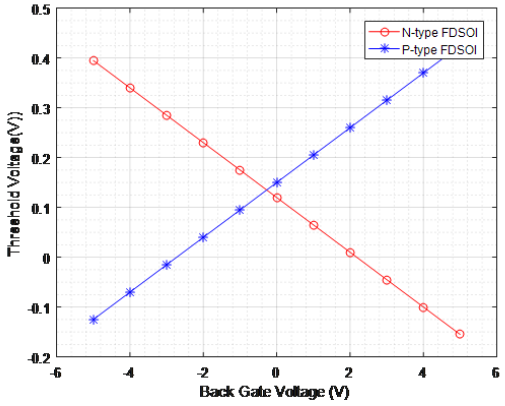


Figure 44: Threshold Voltage Dependence upon back gate bias for FDSOI.

8.2.2 FinFET

FinFET is categorized as a kind of multi-gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET) where a thin silicon film enclosed over the conducting channel and forms the body. The structure of FinFET comprises of a set of fins covered by the gate. The channel length of the device is defined from the thickness of the device. It is basically a non-planar, double-gate transistor. There are two types of FinFET: (i)

Bulk FinFET and (ii) SOI FinFET. The classification of FinFET is based on the âbaseâ onto which it is fabricated. The gate of the FinFET is enclosed around which decreases leakage current thus increases efficiency. In this work, we mainly focused on SOI FinFET which is comparatively less effected by the short channel effects of transistor. In traditional bulk-MOS (planner MOS), the channel is horizontal while in FinFET, it is vertical. So for FinFET, the height of the channel (Fin) defines the width of the device. The drive current of the FinFET is proportional to the width of the channel which means proportional to the height of the Fin. So we can increase the device current by increase the height of the fin. The device current can also be increased by constructing parallel multiple fins connected together. Threshold voltage, which is a dependent variable on depletion region charge, always plays an important role on decreasing leakage current. For double gate FinFET, we can apply a constant DC bias on one gate and use the second gate as input terminal. By changing the DC bias voltage, we can change the depletion region charge to achieve variation in overall threshold voltage.

8.3 Working Principle of Proposed Design

The proposed design using data retention transistor in addition with sleep transistor is implemented in a basic 2-input NAND gate. Figure 45 represents the basic structure of our proposed design. And Figure 46 represents the structure using 2-input NAND gate. There are two control signals: a) CLOCK and b) HOLD and three modes of operation: a) Active b) Hold c) Cut-off. Table 13 represents how these two control signals control different modes of operation. The $\underline{\text{CLOCK}}$ and $\underline{\text{HOLD}}$ in Figure 45 represents the inverse

of CLOCK and HOLD signal.

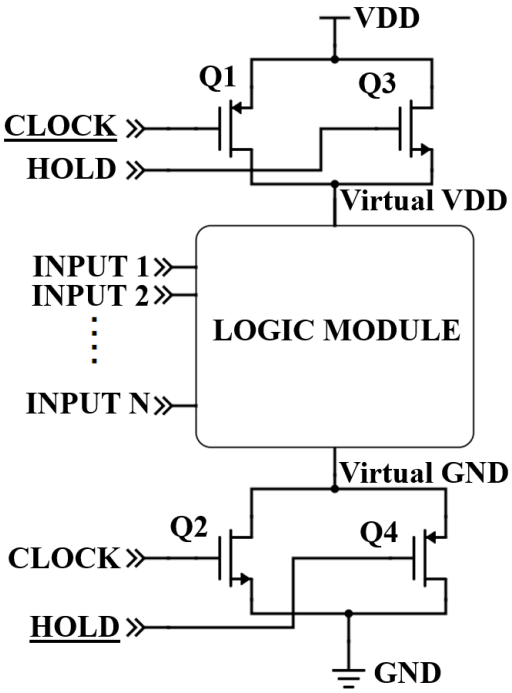


Figure 45: Power gating technique using sleep transistor and data retention transistor for any Logic Module.

Header and footer sleep transistors decreases the leakage of the logic module by introducing virtual VDD and virtual GND but hampers the logic level of the circuit. Therefore, data retention transistor is introduced to retain the original logic level by being active during the inactive period of CLOCK signal. All the back gates/substrates of PMOSs are connected with supply voltage and NMOSs are connected with ground. For FDSOI further leakage reduction is possible by controlling the back gate voltage which will change the threshold voltage of the transistors but that will require additional wiring.

During the active mode, â1â is sent through CLOCK and â0â is sent through

Table 13: Modes of operation depending on control signal.

Modes	CLOCK	HOLD
Active	1	0
Hold	0	1
Cut-off	0	0

HOLD signal. This combination makes the transistor Q1 and Q2 on and Q3 and Q4 off (Figure 45). Due to this the logic module gets full rail to rail supply voltage and it works in a normal mode. In Hold mode, CLOCK is kept at â0â value and HOLD is kept at â1â. In this situation, Q1 and Q2 remain off and Q3 and Q4 are on. As Q3 is a P-type transistor, it is a bad pull-down devices. So a virtual VDD is created which is slightly less the real VDD. And as Q4 is an N-type transistor, it is a bad pull up device. And thus a virtual ground is created which is at a slightly higher value than the real ground. In this mode of operation, the logic module gets a reduced supply voltage. This helps the retention of the data but with a lower power consumption. In the Cut-off mode, â0â is fed through both the CLOCK and HOLD control signal and transistor Q1, Q2, Q3 and Q4 all are in an off state. As a result, the logic module is disconnected from the supply voltage and no current flows through the circuit.

8.4 Benchmarking between FDSOI and FinFET based NAND logic gate

The proposed design is implemented and simulated in Hspice Simulator using 20nm FDSOI process of Leti-UTSOI model files from CEA-Leti and 20nm FinFET of

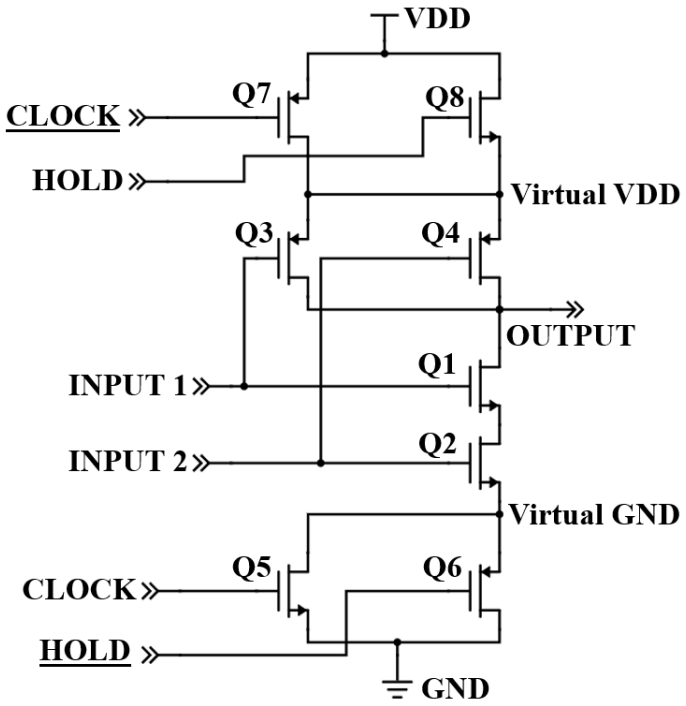


Figure 46: Power gating technique using sleep transistor with data retention transistor for 2-input NAND gate.

PTM-MG model files from ASU. A standard NAND gate is implemented using the proposed design for both FDSOI and FinFET. Table 14 gives the detailed comparative analysis of the design for FDSOI and FinFET. From the table, it is observed that though the design gives better result for FDSOI in terms of propagation delay, the leakage power and total consumed power is far better for FinFET than FDSOI. FinFET-NAND gate consumes 3.75 times less energy compared to FDSOI-NAND gate during active mode. However, FinFET-NAND gate consumes 1.05 times more energy than FDSOI-NAND gate during hold mode. The propagation delay for FinFET is 2ps less than FinFET.

Table 14: Performance summary of FDSOI and SOI-FINFET based NAND gate.

Devices		FDSOI	FinFET
Technology (nm)		20	
Supply Voltage (V)		0.9	
Propagation Delay (ps)		8	10
Leakage Power (pW)	Active mode	162.9	0.77
	Hold mode	101.8	0.58
Total Power (nW)	Active mode	14.34	3.04
	Hold mode	3.11	2.63
Energy Consumption (J)	Active mode	1.14E-19	3.04E-20
	Hold mode	2.5E-20	2.63E-20

CHAPTER 9

CONCLUSIONS & FUTURE WORK

9.1 Summary

The voltage regulator has been an indispensable part of the integrated circuit's power delivery system from the beginning of the technology era. Voltage regulators have evolved from off-chip regulator to on-chip implementation to improve the performance and meet the ever-growing tech industry's requirements. The increasing complexity and more stringent power requirements are continuously pushing researchers to overcome the limitations of on-chip voltage regulators. As the Internet of Things (IoT), biosensors, battery-powered devices are more coming into the picture, power-efficient, fast response, and noise-free supply are in high demand more than ever. To design such a efficient regulator, it takes a significant amount of time and resources to successfully implement it. For the last few decades, researchers are relentlessly working to find an optimized, mature, and less time-consuming tool to automate the analog design process and minimize the design productivity gap.

In this work, we have surveyed a significant number of recent and state-of-the-art literature and compared based on the working principles and different key design parameters (such as efficiency, consumed power, area, etc.) and assembled the findings in this paper. This dissertation has also explained the background and classification of different prevailing LDO and SC VR and compared them based on their operating principle,

advantages/disadvantages, and suitability of their implementation.

We proposed a fully on-chip LDO implementation in 45nm without an external capacitor is proposed. An input voltage of 1.2V is used, and a wide range of 0.4V to 1.2V output voltage is achieved in this proposed design. An additional pass transistor is used instead of a resistor feedback network to reduce the active area and achieve a three-fold improvement. High PSRR, better line, load regulation, and fully on-chip implementation as there is no need for an external capacitor make the proposed design suitable for on-chip implementation as well as in smaller devices.

In addition, we also proposed a external capacitorless fully on-chip LDO implementation in TSMC 180nm and sent it for fabrication. We further utilized the VR design in memory security application.

For analog automation, We presented a robust optimization methodology flow for circuit synthesis and transistor sizing as a possible solution in the Circuit-level of analog hierarchical design flow in this work. We proposed two phases of iteration and used an efficient supervised learning algorithm, random decision forest between those phases to reduce the transistor sizing limit. As a result, the time will not be wasted unnecessarily on evaluating an incapable topology, and the optimized solution can be found in minutes.

9.2 Future Work

As voltage regulator is a fundamental part of an integrated circuit, it has been well studied for many decades. An efficient VR can ensure a stable operation of a whole chip. That is why the study of a more efficient and competent design of VR is still ongoing.

As technology is shrinking as well as the supply voltage, the need for research on on-chip VR in lower node technology is vital and more needed. This paper will help future researchers understand the performance and limitations of on-chip VR and implement the knowledge to design future regulators. The most optimistic implantation of on-chip VR will be a single entity having small, simple, and noise-free designs with a fast transient response and high efficiency.

REFERENCE LIST

[1] M. F. Barros, J. M. Guilherme, and N. C. Horta, *Analog circuits and systems optimization based on evolutionary computation techniques*, vol. 294. Springer, 2010.

[2] G. G. Gielen and R. A. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proceedings of the IEEE*, vol. 88, no. 12, pp. 1825–1854, 2000.

[3] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 3, pp. 514–522, 2003.

[4] B. H. Calhoun and A. P. Chandrakasan, "Ultra-dynamic voltage scaling (udvs) using sub-threshold operation and local voltage dithering," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 238–245, 2005.

[5] W. Kim, M. S. Gupta, G.-Y. Wei, and D. Brooks, "System level analysis of fast, per-core dvfs using on-chip switching regulators," in *2008 IEEE 14th International Symposium on High Performance Computer Architecture*, pp. 123–134, IEEE, 2008.

[6] L. Wang, "High performance distributed on-chip voltage regulation for modern integrated systems," 2018.

[7] "Advantages of Low Dropout REGULATOR [Online]. Available: https://techweb.rohm.com/knowledge/dcdc/s-dcdc/01-s-dcdc/7. Accessed: March 23, 2020," 2018.

[8] H. MartÃnez-GarcÃa and A. Saberkari, "Linear-assisted dc/dc regulator-based current source for led drivers," *Electronics Letters*, 2016.

[9] V. Shirmohammadli, A. Saberkari, H. Martínez-García, and E. Alarcón-Cot, "Ldo-assisted vs. linear-assisted dc/dc converters: A comprehensive study and comparison," in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 105–108, IEEE, 2016.

[10] V. Shirmohammadli, A. Saberkari, H. Martínez-García, and E. Alarcón-Cot, "Integrated power management system based on efficient ldo-assisted dc/dc buck converter," in *2016 IEEE 14th International Conference on Industrial Informatics (INDIN)*, pp. 282–285, IEEE, 2016.

[11] C. Zhan and W. Ki, "Analysis and design of output-capacitor-free low-dropout regulators with low quiescent current and high power supply rejection," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, pp. 625–636, Feb 2014.

[12] F. Yang and P. K. T. Mok, "Fast-transient asynchronous digital ldo with load regulation enhancement by soft multi-step switching and adaptive timing techniques in 65-nm cmos," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, Sep. 2015.

[13] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. BrÃ¤ndli, and P. A. Francese, "A 10 w on-chip switched capacitor voltage regulator with feedforward regulation capability for granular microprocessor power delivery," *IEEE Transactions on Power Electronics*, vol. 32, pp. 378–393, Jan 2017.

[14] N. Butzen and M. S. J. Steyaert, "Scalable parasitic charge redistribution: Design of high-efficiency fully integrated switched-capacitor dcâdc converters," *IEEE Journal of Solid-State Circuits*, Dec 2016.

[15] F. U. Ahmed and M. H. Chowdhury, "An asynchronous reconfigurable switched capacitor voltage regulator," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1110–1113, Aug 2018.

[16] P. M. Furth, S. Krishnapurapu, S. H. Pakala, and M. A. Haque, "A 5.3μa quiescent current fully-integrated low-dropout (ldo) regulator with transient recovery time enhancement," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 9–12, Aug 2013.

[17] Y. . Kim and S. . Lee, "Fast transient capacitor-less ldo regulator using low-power output voltage detector," *Electronics Letters*, vol. 48, pp. 175–177, February 2012.

[18] S. T. Kim, Y. Shih, K. Mazumdar, R. Jain, J. F. Ryan, C. Tokunaga, C. Augustine, J. P. Kulkarni, K. Ravichandran, J. W. Tschanz, M. M. Khellah, and V. De, "8.6 enabling wide autonomous dvfs in a 22nm graphics execution core using a digitally controlled hybrid ldo/switched-capacitor vr with fast droop mitigation," in *2015*

IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, pp. 1–3, Feb 2015.

[19] Y. Lu, Y. Wang, Q. Pan, W. Ki, and C. P. Yue, "A fully-integrated low-dropout regulator with full-spectrum power supply rejection," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, pp. 707–716, March 2015.

[20] Z. K. Ahmed, H. K. Krishnamurthy, C. Augustine, X. Liu, S. Weng, K. Ravichandran, J. W. Tschanz, and V. De, "A variation-adaptive integrated computational digital ldo in 22nm cmos with fast transient response," in *2019 Symposium on VLSI Circuits*, pp. C124–C125, 2019.

[21] Y. Xiao, W. Lu, M. Chen, Y. Zhang, and Z. Chen, "A low noise, fast set-up low-dropout regulator in 65nm technology," in *2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, pp. 1–3, Dec 2012.

[22] S. Heng and C. Pham, "A low-power high-psrr low-dropout regulator with bulk-gate controlled circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, pp. 245–249, April 2010.

[23] S. Lai and P. Li, "A fully on-chip area-efficient cmos low-dropout regulator with fast load regulation," *Analog Integrated Circuits and Signal Processing*, vol. 72, 08 2012.

[24] M. Nasrollahpour and S. Hamedi-Hagh, “Fast transient response and high psrr low drop-out voltage regulator,” in *2016 IEEE Dallas Circuits and Systems Conference (DCAS)*, pp. 1–4, Oct 2016.

[25] Y. Lim, J. Lee, S. Park, and J. Choi, “An extemal-capacitor-less low-dropout regulator with less than â36db psrr at all frequencies from 10khz to 1ghz using an adaptive supply-ripple cancellation technique to the body-gate,” in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, 2017.

[26] Y. Lu, W. Ki, and C. P. Yue, “17.11 a 0.65ns-response-time 3.01ps fom fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 306–307, 2014.

[27] T. J. Thornton, W. Lepkowski, S. J. Wilk, M. Goryll, B. Chen, J. Kam, B. Bakkaloglu, and K. Holbert, “Radiation tolerant mesfet-cmos low dropout linear regulator for integrated power management at the 45nm node,” in *2013 IEEE Radiation Effects Data Workshop (REDW)*, pp. 1–3, 2013.

[28] T. Toifl, C. Menolfi, P. Buchmann, M. Kossel, T. Morf, and M. Schmatz, “A small-area voltage regulator with high-bandwidth supply-rejection using a regulated replica in 45nm cmos soi,” in *2008 IEEE Asian Solid-State Circuits Conference*, pp. 157–160, 2008.

[29] S. K. Singh and G. D. Kanungo, “Ultra-fast cap-less ldo for dual lane usb in 28fdsoi,” in *2015 28th International Conference on VLSI Design*, pp. 254–259, 2015.

[30] L. Wang, W. Mao, C. Wu, A. Chang, and Y. Lian, "A fast transient ldo based on dual loop fvf with high psrr," in *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 99–102, 2016.

[31] J. F. Bulzacchelli, Z. Toprak-Deniz, T. M. Rasmus, J. A. Iadanza, W. L. Bucossi, S. Kim, R. Blanco, C. E. Cox, M. Chhabra, C. D. LeBlanc, C. L. Trudeau, and D. J. Friedman, "Dual-loop system of distributed microregulators with high dc accuracy, load response time below 500 ps, and 85-mv dropout voltage," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 4, pp. 863–874, 2012.

[32] F. U. Ahmed, Z. T. Sandhie, L. Ali, and M. H. Chowdhury, "A brief overview of on-chip voltage regulation in high-performance and high-density integrated circuits," *IEEE Access*, 2020.

[33] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated dc–dc conversion via the switched-capacitor approach," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146–4155, 2012.

[34] C.-H. Wu, L.-r. Chang-Chien, and L.-y. Chiou, "Active filter based on-chip step-down dc-dc switching voltage regulator," in *TENCON 2005-2005 IEEE Region 10 Conference*, pp. 1–6, IEEE, 2005.

[35] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down dc-dc converter with digital capacitance modulation in 45 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, 2010.

[36] S. KÃ¶se and E. G. Friedman, "An area efficient fully monolithic hybrid voltage regulator," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 2718–2721, 2010.

[37] S. KÃ¶se, E. G. Friedman, S. Tarn, S. Pinzon, and B. McDermott, "An area efficient on-chip hybrid voltage regulator," in *Thirteenth International Symposium on Quality Electronic Design (ISQED)*, pp. 398–403, 2012.

[38] J. Gjanci and M. H. Chowdhury, "A hybrid scheme for on-chip voltage regulation in system-on-a-chip (soc)," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 11, pp. 1949–1959, 2011.

[39] G. Yan, Y. Li, Y. Han, X. Li, M. Guo, and X. Liang, "Agileregulator: A hybrid voltage regulator scheme redeeming dark silicon for power efficiency in a multi-core architecture," in *IEEE International Symposium on High-Performance Comp Architecture*, pp. 1–12, 2012.

[40] "Types of voltage regulator [Online]. Available: https://www.electronics hub.org/types-of-voltage-regulators/ Accessed: March 23, 2020," 2018.

[41] H.-P. Le, *Design techniques for fully integrated switched-capacitor voltage regulators*. PhD thesis, UC Berkeley, 2013.

[42] K. Zou, *The topology and voltage regulation for high-power switched-capacitor converters*. PhD thesis, The Ohio State University, 2012.

[43] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE transactions on power electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[44] M. D. Seeman, "A design methodology for switched-capacitor dc-dc converters," tech. rep., UC Berkeley, 2009.

[45] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, 2011.

[46] T. Van Breussegem and M. Steyaert, *CMOS integrated capacitive DC-DC converters*. Springer Science & Business Media, 2012.

[47] Y. K. Ramadass and A. P. Chandrakasan, "Voltage scalable switched capacitor dc-dc converter for ultra-low-power on-chip applications," in *2007 IEEE Power Electronics Specialists Conference*, pp. 2353–2359, IEEE, 2007.

[48] H. P. McAdams, R. Acklin, T. Blake, X.-H. Du, J. Eliason, J. Fong, W. F. Kraus, D. Liu, S. Madan, T. Moise, *et al.*, "A 64-mb embedded fram utilizing a 130-nm 5lm cu/fsg logic process," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 4, pp. 667–677, 2004.

[49] F. U. Ahmed, Z. T. Sandhie, and M. H. Chowdhury, "An implementation of external capacitor-less low-dropout voltage regulator in 45nm technology with output voltage

ranging from 0.4 v-1.2 v," in *2020 IEEE 38th International Conference on Computer Design (ICCD)*, pp. 453–456, IEEE, 2020.

[50] "NCSU 45nm FreePDK:Contents [Online]. Available: https://www.eda.ncsu.edu/wiki/freepdk45:contents. Accessed: March 23, 2020," 2018.

[51] "Physical Verication with Calibre [Online]. Available: https://www.mentor.com/products/ic_nanometer_design/verification-signoff/physical-verification. Accessed: March 23, 2020," 2018.

[52] H. Freeman, "Stability and physical realizability considerations in the synthesis of multipole control systems," *Transactions of the American Institute of Electrical Engineers, Part II: Applications and Industry*, vol. 77, pp. 1–5, March 1958.

[53] "What is PSRR? [Online]. Available: https://www.onsemi.com/blog/industrial-cloud-power/what-is-psrr-part-3 Accessed: March 23, 2020," 2018.

[54] C. Desai, D. Mandal, B. Bakkaloglu, and S. Kiaei, "A 1.66 mv fom output cap-less ldo with current-reused dynamic biasing and 20 ns settling time," *IEEE Solid-State Circuits Letters*, vol. 1, no. 2, pp. 50–53, 2018.

[55] Y. Jiang, D. Wang, and P. K. Chan, "A quiescent 407-na output-capacitorless low-dropout regulator with 0–100-ma load current range," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 5, pp. 1093–1104, 2019.

[56] S. Bu, J. Guo, and K. N. Leung, "A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth¿ 100 mhz in 130-nm cmos," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3232–3246, 2017.

[57] F. Lavalle-Aviles, J. Torres, and E. Sánchez-Sinencio, "A high power supply rejection and fast settling time capacitor-less ldo," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 474–484, 2018.

[58] C.-J. Park, M. Onabajo, and J. Silva-Martinez, "External capacitor-less low drop-out regulator with 25 db superior power supply rejection in the 0.4–4 mhz range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 486–501, 2013.

[59] Z. Wang and S. Mirabbasi, "A 0.58-to-0.9-v input 0.53-v output 2.4-μw current-feedback low-dropout regulator with 99.8% current efficiency," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 1–4, 2019.

[60] D. Leenaerts, G. Gielen, and R. A. Rutenbar, "Cad solutions and outstanding challenges for mixed-signal and rf ic design," in *IEEE/ACM International Conference on Computer Aided Design. ICCAD 2001. IEEE/ACM Digest of Technical Papers (Cat. No.01CH37281)*, pp. 270–277, 2001.

[61] G. G. E. Gielen, "Modeling and analysis techniques for system-level architectural design of telecom front-ends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 360–368, 2002.

[62] N. Horta, "Analog and mixed-signal ic design automation: Synthesis and optimization overview," in *Proc. 5th Conference on Telecommunications, Tomar, Portugal*, 2005.

[63] V. Boos, J. Nowak, M. Sylvester, S. Henker, S. Höppner, H. Grimm, D. Krausse, and R. Sommer, "Strategies for initial sizing and operating point analysis of analog circuits," in *2011 Design, Automation & Test in Europe*, pp. 1–3, IEEE, 2011.

[64] O. Mitea, M. Meissner, L. Hedrich, and P. Jores, "Automated constraint-driven topology synthesis for analog circuits," in *2011 Design, Automation & Test in Europe*, pp. 1–4, IEEE, 2011.

[65] E. Afacan, S. Ay, F. V. Fernandez, G. Dündar, F. Bas, *et al.*, "Model based hierarchical optimization strategies for analog design automation," in *2014 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1–4, IEEE, 2014.

[66] A. Gerlach, J. Scheible, T. Rosahl, and F.-T. Eitrich, "A generic topology selection method for analog circuits with embedded circuit sizing demonstrated on the ota example," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*, pp. 898–901, IEEE, 2017.

[67] K. Settaluri and E. Fallon, "Fully automated analog sub-circuit clustering with graph convolutional neural networks," in *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1714–1715, IEEE, 2020.

[68] V. Krishnamurthy and B. Kim, "Development of analog circuit design automation tool," in *IEEE Southeastcon 2009*, pp. 236–241, IEEE, 2009.

[69] R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C. Clauss, P. Schwarz, and G. Noessing, "From system specification to layout: Seamless top-down design methods for analog and mixed-signal applications," in *Proceedings 2002 Design, Automation and Test in Europe Conference and Exhibition*, pp. 884–891, IEEE, 2002.

[70] H. Chang, E. Charbon, U. Choudhury, E. Felt, A. Demir, E. Liu, E. Malavasi, A. Sangiovanni-Vincentelli, and I. Vassiliou, *A top-down, constraint-driven design methodology for analog integrated circuits*. Springer Science & Business Media, 1997.

[71] C. Toumazou and C. A. Makris, "Analog ic design automation. i. automated circuit generation: new concepts and methods," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, no. 2, pp. 218–238, 1995.

[72] S. Donnay, G. Gielen, W. Sansen, W. Kruiskamp, D. Leenaerts, S. Buytaert, K. Marent, M. Buckens, and C. Das, "Using top-down cad tools for mixed analog/digital asics: a practical design case," in *Modeling and Simulation of Mixed Analog-Digital Systems*, pp. 101–117, Springer, 1996.

[73] R. C. López, F. V. Fernández, Ó. Guerra-Vinuesa, and Á. Rodríguez-Vázquez, *Reuse-based methodologies and tools in the design of analog and mixed-signal integrated circuits*. Springer Science & Business Media, 2007.

[74] W. Kruiskamp and D. Leenaerts, "Darwin: Cmos opamp synthesis by means of a genetic algorithm," in *Proceedings of the 32nd annual ACM/IEEE design automation conference*, pp. 433–438, 1995.

[75] E. Martens and G. Gielen, "Classification of analog synthesis tools based on their architecture selection mechanisms," *Integration*, vol. 41, no. 2, pp. 238–252, 2008.

[76] M. G. Degrauwe, O. Nys, E. Dijkstra, J. Rijmenants, S. Bitz, B. L. Goffart, E. A. Vittoz, S. Cserveny, C. Meixenberger, G. Van Der Stappen, *et al.*, "Idac: An interactive design tool for analog cmos circuits," *IEEE Journal of solid-state circuits*, vol. 22, no. 6, pp. 1106–1116, 1987.

[77] R. Harjani, R. A. Rutenbar, and L. R. Carley, "Oasys: A framework for analog circuit synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8, no. 12, pp. 1247–1266, 1989.

[78] D. Leenaerts, G. Gielen, and R. A. Rutenbar, "Cad solutions and outstanding challenges for mixed-signal and rf ic design," in *IEEE/ACM International Conference on Computer Aided Design. ICCAD 2001. IEEE/ACM Digest of Technical Papers (Cat. No. 01CH37281)*, pp. 270–277, IEEE, 2001.

[79] H. Trevor, T. Robert, and F. Jerome, "The elements of statistical learning," 2009.

[80] I. Chatterjee, E. Zhang, B. Bhuva, M. Alles, R. Schrimpf, D. Fleetwood, Y. Fang, and A. Oates, "Bias dependence of total-dose effects in bulk finfets," *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4476–4482, 2013.

[81] M. U. Mohammed, A. Nizam, and M. H. Chowdhury, "Performance stability analysis of sram cells based on different finfet devices in 7nm technology," in *2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pp. 1–3, IEEE, 2018.

[82] M. U. Mohammed, A. Nizam, and M. H. Chowdhury, "Double-gate fdsoi based sram bitcell circuit designs with different back-gate biasing configurations," in *2018 IEEE Nanotechnology Symposium (ANTS)*, pp. 1–4, IEEE, 2018.

[83] M. U. Mohammed, A. Nizam, and M. H. Chowdhury, "Performance and reliability of asymmetrical underlapped finfet based 6t and 8t srams in sub-10nm domain," in *2018 IEEE Nanotechnology Symposium (ANTS)*, pp. 1–4, IEEE, 2018.

[84] M. U. Mohammed and M. H. Chowdhury, "Design of energy efficient sram cell based on double gate schottky-barrier-type gnrfet with minimum dimer lines," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, IEEE, 2019.

[85] M. U. Mohammed, A. Nizam, L. Ali, and M. H. Chowdhury, "A low leakage sram bitcell design based on mos-type graphene nano-ribbon fet," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, IEEE, 2019.

[86] M. U. Mohammed, R. Vijjapuram, and M. H. Chowdhury, "Novel cntfet and memristor based unbalanced ternary logic gate," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1106–1109, IEEE, 2018.

[87] M. U. Mohammed and M. H. Chowdhury, "Reliability and energy efficiency of the tunneling transistor-based 6t sram cell in sub-10 nm domain," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 12, pp. 1829–1833, 2018.

[88] J. A. Patel, Z. T. Sandhie, and M. H. Chowdhury, "Ternary device using graphene memcapacitor for post binary era," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1130–1133, 2018.

[89] V. Khandelwal and A. Srivastava, "Leakage control through fine-grained placement and sizing of sleep transistors," *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 26, no. 7, pp. 1246–1255, 2007.

[90] E. Ashenafi and M. H. Chowdhury, "A new power gating circuit design approach using double-gate fdsoi," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 8, pp. 1074–1078, 2016.

[91] M. H. Chowdhury, J. Gjanci, and P. Khaled, "Controlling ground bounce noise in power gating scheme for system-on-a-chip," in *2008 IEEE Computer Society Annual Symposium on VLSI*, pp. 437–440, IEEE, 2008.

[92] M. U. Mohammed, N. M. Hossain, and M. H. Chowdhury, "A disturb free read port 8t sram bitcell circuit design with virtual ground scheme," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 412–415, IEEE, 2018.

[93] F. U. Ahmed, Z. T. Sandhie, M. U. Mohammed, A. H. B. Yousuf, and M. Chowdhury, "Energy efficient fdsoi and finfet based power gating circuit using data retention transistor," in *2018 IEEE Nanotechnology Symposium (ANTS)*, pp. 1–4, IEEE, 2018.

[94] I. Y. Yang, C. Vieri, A. Chandrakasan, and D. A. Antoniadis, "Back-gated cmos on soias for dynamic threshold voltage control," *IEEE Transactions on Electron Devices*, vol. 44, no. 5, pp. 822–831, 1997.

VITA

Farid Uddin Ahmed received the B.E. degree in electrical and electronic engineering from Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 2015. He completed his M.S. degree in electrical engineering from the University of Missouri Kansas City (UMKC), Kansas City, Missouri. Currently, he is pursuing his Ph.D. and work as a graduate research assistant at Micro and Nano Electronics Lab and graduate teaching assistant at Computer Science Electrical Engineering Department, UMKC. He works on voltage regulator design and analog design automation. Farid was awarded UMKC School of Graduate Studies Research Grant in 2018. He got the 1st prize in UMKC hack-a-roo 2018.He completed his internship as a graduate intern at Intel in the Optane Memory group. After completing his Ph.D., he will join as Product Development Engineer in the same group as a full-time. He served as an organizing secretary in the UMKC-Bangladesh student association in 2019.