3D MODELING AND INTEGRATION OF CURRENT AND FUTURE INTERCONNECT TECHNOLOGIES

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ABDUL HAMID BIN YOUSUF

B.Sc. University of Dhaka, 2010
M.S. University of Dhaka, 2012

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Abdul Hamid Bin Yousuf, Candidate for the Doctor of Philosophy Degree

University of Missouri-Kansas City, 2021

ABSTRACT

To ensure maximum circuit reliability it is very important to estimate the circuit performance and signal integrity in the circuit design phase. A full phase simulation for performance estimation of a large-scale circuit not only require a massive computational resource but also need a lot of time to produce acceptable results. The estimation of performance/signal integrity of sub-nanometer circuits mostly depends on the interconnect capacitance. So, an accurate model for interconnect capacitance can be used in the circuit CAD (computer-aided design) tools for circuit performance estimation before circuit fabrication which reduces the computational resource requirement as well as the time constraints. We propose a new capacitance models for interconnect lines in multilevel interconnect structures by geometrically modeling the electrical flux lines of the interconnect lines. Closed-form equations have been derived analytically for ground and coupling capacitance. First, the capacitance model for a single line is developed, and then the new model is used to derive expressions for the capacitance of a line surrounded by neighboring lines in the same and the adjacent layers above and below. These expressions are simple, and the calculated results are within 10% of Ansys Q3D extracted values.

Through silicon via (TSV) is one of the key components of the emerging 3D ICs. However, increasing number of TSVs in smaller silicon area leads to some severe negative impacts on the performance of the 3D IC. Growing signal integrity issues in TSVs is one of the major challenges of 3D integration. In this paper, different materials for the cores of the vias and the interposers are investigated to find the best possible combination that can reduce crosstalk and other losses like return loss and insertion loss in the TSVs. We have explored glass and silicon as interposer materials. The simulation results indicate that glass is the best option as interposer material although silicon interposer has some distinct advantages. For via cores three materials - copper (Cu), tungsten (W) and Cu-W bimetal are considered. From the analysis it can concluded that W would be better for high frequency applications due to lower transmission coefficient. Cu offers higher conductivity, but it has larger thermal expansion coefficient mismatch with silicon. The performance of Cu-W bimetal via would be in between Cu and W. However, W has a thermal expansion coefficient close to silicon. Therefore, bimetal Cu-W based TSV with W as the outer layer would be a suitable option for high frequency 3D IC. Here, we performed the analysis in terms of return loss, transmission coefficient and crosstalk in the vias.

Signal speed in current digital systems depends mainly on the delay of interconnects. To overcome this delay problem and keep up with Moore's law, 3D integrated circuit (vertical integration of multiple dies) with through-silicon via (TSV) has been introduced to ensure much smaller interconnect lengths, and lower delay and power consumption compared to conventional 2D IC technology. Like 2D circuit, the estimation of 3D circuit performance depends on different electrical parameters (capacitance, resistance, inductance) of the TSV. So, accurate modeling of the electrical parameters of the TSV is essential for the

design and analysis of 3D ICs. We propose a set of new models to estimate the capacitance, resistance, and inductance of a Cu-filled TSV. The proposed analytical models are derived from the physical shape and the size of the TSV. The modeling approach is comprehensive and includes both the cylindrical and tapered TSVs as well as the bumps.

On-chip integration of inductors has always been very challenging. However, for sub-14nm on-chip applications, large area overhead imposed by the on-chip capacitors and inductors has become a more severe concern. To overcome this issue and ensure power integrity, a novel 3D Through-Silicon-Via (TSV) based inductor design is presented. The proposed TSV based inductor has the potential to achieve both high density and high performance. A new design of a Voltage Controlled Oscillator (VCO) utilizing the TSV based inductor is also presented. The implementation of the VCO is intended to study the feasibility, performance, and real-world application of the proposed TSV based inductor.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a thesis titled "3D Modeling and Integration of Current and Future Interconnect Technologies," presented by Abdul Hamid Bin Yousuf, candidate for the Doctor of Philosophy degree, and certify that in their opinion it is worth of acceptance.

Supervisory Committee

Masud H. Chowdhury, Ph.D., Committee Chair
Department of Electrical and Computer Engineering

Paul Rulis, Ph.D.
Department of Physics

Ghulam Chaudhry, Ph.D.
Department of Electrical and Computer Engineering

Deb Chatterjee, Ph.D.
Department of Electrical and Computer Engineering

Baek-Young Choi, Ph.D.
Department of Computing and Engineering

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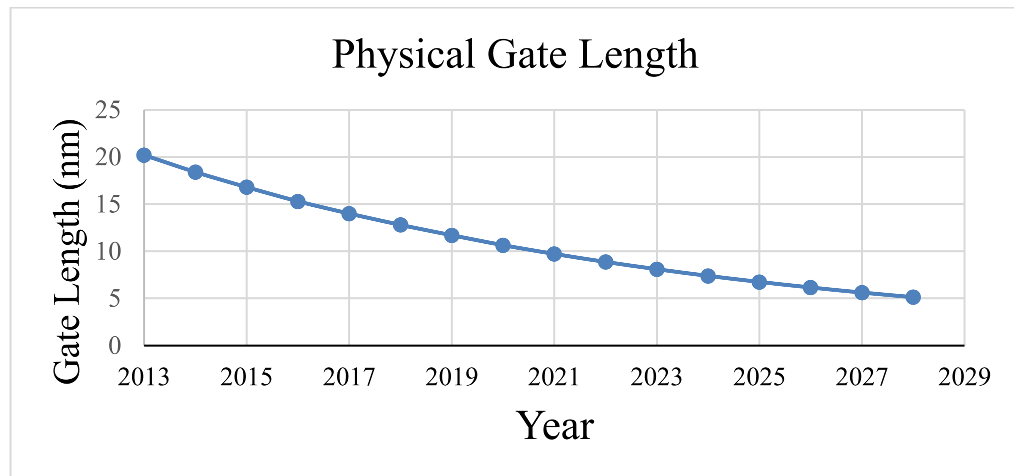
CHAPTER 1

INTRODUCTION

1.1 Interconnect Modeling

To keep up with Moore's law [1], the number of transistors is increasing to accommodate more functionality into a fixed size chip. Only way to achieve that is to scale down the physical dimensions of devices and wires that connects the devices in a chip. In the deep sub nanometer technology, the wire connecting the devices (also known as interconnect) plays a vital role of the chip's overall performance. With scaling down, the devices are becoming faster in every new generation, but the interconnects are getting narrower, so the performance of the interconnects getting worse. We now reach such a point where the interconnect delay is more prominent compared to gate delay and interconnect delay determines the chip performance.



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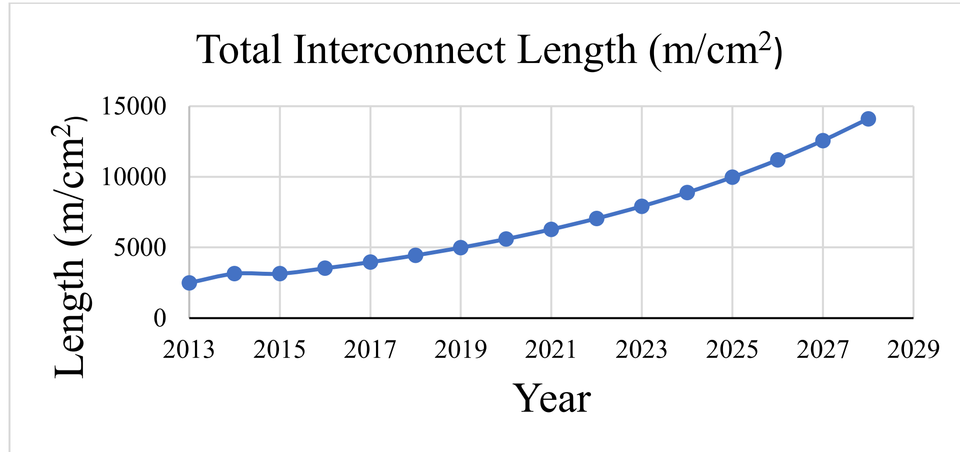

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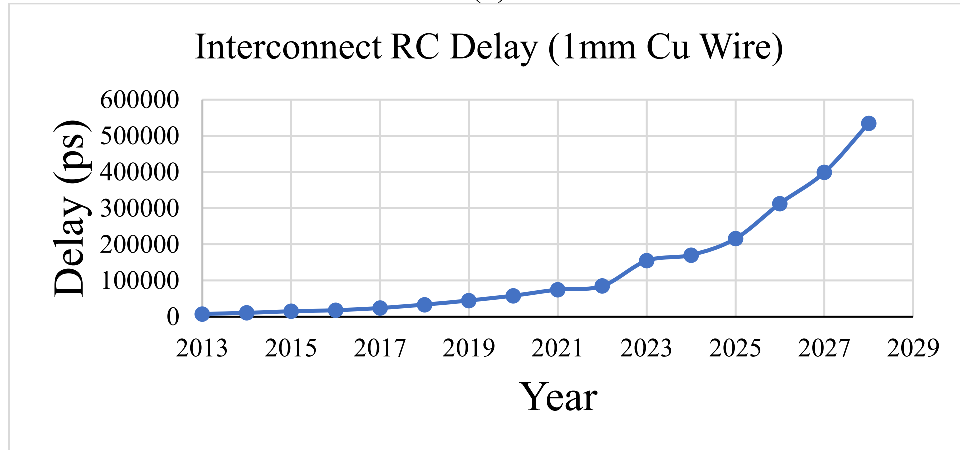


(c)

Figure 1.1.1: IRDS prediction of (a) device scaling down (b) increasing interconnect length and (c) increasing interconnect delay [2, 3].

Figure 1.1.1 shows the roadmap for device scaling and path to overall interconnect performance [2, 3]. With aggressive scaling down of the device, more interconnect is

required to tie them all. Thus, the interconnects are placed very compactly, reducing their pitch (spacing between neighboring interconnect). As the width of interconnect also scaled down with device sizes, to keep up with device performance and reducing the overall resistance of the interconnect, height of the interconnect is increasing with every successive generation increasing their aspect ratio (height/width) as shown in Figure 1.1.2.

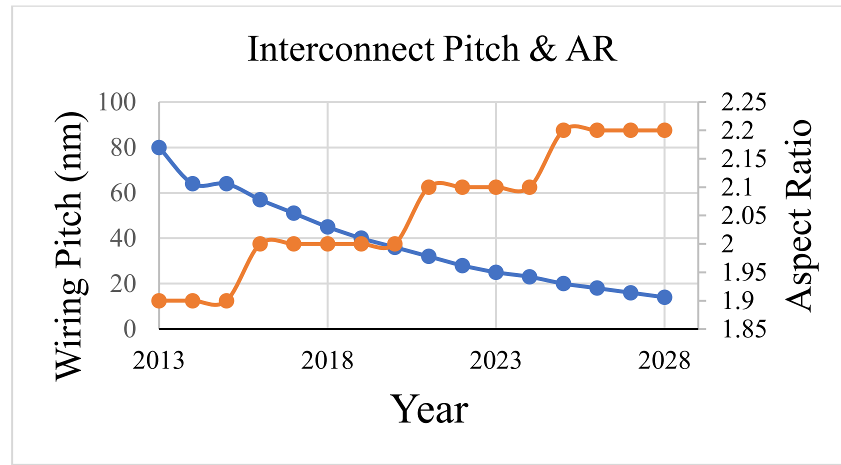


Figure 1.1.2: Prediction for interconnect aspect ratio and pitch.

As the interconnect performance becoming dominant, it is very important to predict the effect of the interconnect performance before chip fabrication. The interconnect performance depends on the resistance and the capacitance of the interconnect. Predicting the resistance of an interconnect is straight forward and depends on the dimension and material of interconnect. Contrary to that predicting the capacitance of an interconnect is very

complex procedure and often depends on different factors. So, it is very important to have an accurate model of interconnect capacitance to correctly predict the interconnect performance.

1.2 3D Integration

The demand for integrating more functionality into a single chip leads to technology scaling so that the number of transistors in a chip can be increased without increasing the chip area. But according to International Roadmap for Devices and Systems (IRDS) technology scaling may not be possible for 2D technology after 2024 [4]. Several leading chip manufacturing labs also known as foundries namely 'GlobalFoundries', halted their production below 7nm as the cost of building and maintaining new manufacturing facilities are beyond anticipation [5]. 3D integration can be a possible solution of this problem as 3D integration promises more functionality and better performance on a similar 2D chip area. It is a step towards 'more than Moore' era.

In general 3D integration means stacking up two or more 2D integrated chip vertically with the through-silicon vias (TSV), interposers, bumps, and micro bumps as shown in Figure 1.2.1. 3D integration promises improve performance, low power, smaller chip area, and reduced manufacturing cost compared to 2D integration. 3D integration comprises technologies such as 'system in package (SiP)', TSV based 3D integrated circuits, monolithic 3D integration etc.

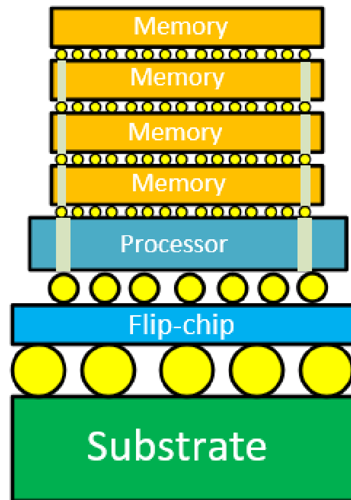


Figure 1.2.1: 3D Integrated Circuit with TSVs, bumps and micro-bumps [2]

TSV based 3D integrated circuits solve one of the biggest problems of 2D integrated circuits currently face – ever increasing interconnect length. Through-silicon via (TSV) is a potential solution to the long interconnect problem as they are connected vertically and much shorter in length. Though shorter in length but their other dimension is large compared to nano scale interconnect, often having radius in 'μm' range. This large structure of TSVs introduces several other problems. So, when one uses TSV based 3D ICs it is important to make sure about the material of the core, material of the insulation layer that surrounds the TSV and characteristics of the interposer through with the TSV goes from one layer to the

next. As TSVs are responsible for supplying the power and signal, knowledge about their electrical and thermal characteristics are also very important.

1.3 Organization

This dissertation consists of seven chapters. Chapter 1 provides a general introduction and overview also layout of the dissertation. Chapter 2 provides the background of current state of interconnect capacitive modeling. Chapter 3 discuss about the capacitance modeling of multi-level interconnect structure. Chapter 4 introduces the performance of TSVs based on the material composition and Chapter 5 tackles with the performance of TSV based on its shape and size. In Chapter 6 electrical characterization of TSVs are discussed and finally Chapter 7 presents the optimization of TSV based inductor for VCO design.

1.4 Dissertation Objective

The main objectives of the dissertation are summarized as follows:

- To provide an accurate capacitance model for sub 22nm technology node.
- Investigate the performance dependence of TSV on its material composition and structure.
- To develop an RLC model of the TSV for the electrical characterization.
- Optimize TSV based inductor for high frequency application.

CHAPTER 2

BACKGROUND OF CAPACITANCE MODELING OF ON-CHIP INTERCONNECT

2.1 Introduction

In the CMOS integrated circuit technology, the wires that connects all the transistors in a system are known as interconnect. In the modern system interconnect plays a very important role and every so often interconnect performance determines the performance of the whole system. In the early ages of VLSI (very large-scale integration), the performance of On-Chip interconnect is mostly overlooked because the performance of the overall integrated system mostly depended on the performance of the transistors. The transistors are very slow compared to modern VLSI technology and the interconnect used to connect all those transistors are wide and thick thus results in very low resistance and they are placed moderately far apart from one another. So, the interconnects were treated as ideal equipotential nodes with lumped capacitance [6].

In the modern deep sub-micron technology, the interconnects are narrower and densely populated. So, the resistance goes high and introduce other parasitic effects such as coupling capacitance between neighboring interconnects which leads to a point where the RC delay of the interconnect line exceeds the gate delay of the transistors. Therefore, when designing a system with modern sub-micron technology node it is very important to have knowledge about the characteristics of the interconnect and their behavior and impact on the performance of the system.

2.2 Interconnect Geometry

Figure 2.2.1 shows two interconnects are placed side by side over a ground plane as in modern CMOS technology. The width of the interconnect is W, height H, length L, the distance from the ground to the interconnect (also known as oxide thickness) T and distance between two interconnects (spacing) S. The term 'pitch' is known as the sum of width and spacing and the height to width $\left(\frac{H}{W}\right)$ ratio is known as 'aspect ratio'.

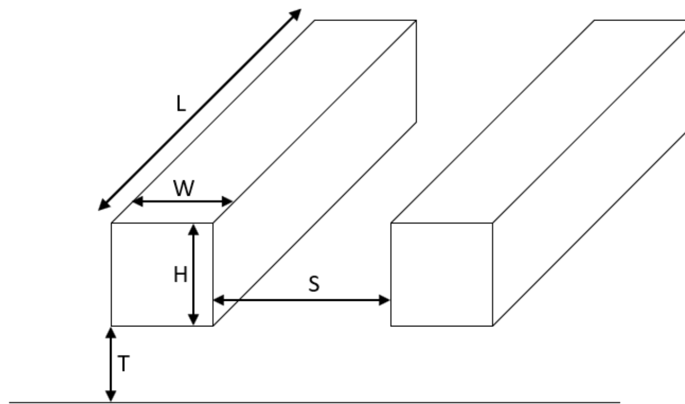


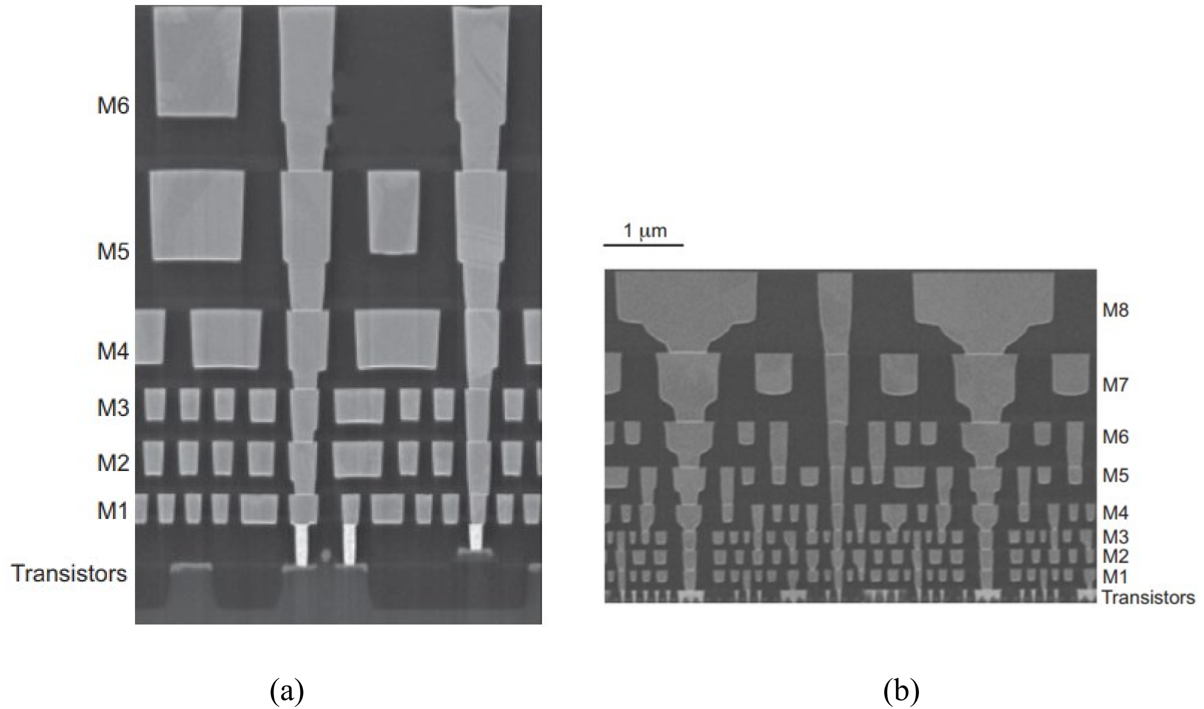
Figure 2.2.1: Geometry of Interconnect

In early VLSI technology only a single layer of interconnect was used to connect all the transistors. Up until 1990s a maximum of two to three metal layers can be found on a system. But modern VLSI systems uses nine (9) or more metal layers because of the number of transistors in the system to connect and the advancement of chemical-mechanical polishing to fabricate several metal layers.

Figure 2.2.2 shows Intel 90 and 45 nm process, where the 90 nm process has six (6) metal layers and 45 nm process has nine (9) metal layers. The metal layers those are closed to the transistors (layer M1, M2) are densely packed and narrow in dimension (high pitch). The upper metal layers wider and offer great pitch. Table 1 shows different dimensions of intel 45nm process.

Table 1
Dimensions of different metal layers in Intel 45nm technology [6]

Layer	$H\ (nm)$	$W\ (nm)$	$S\ (nm)$	$Pitch\ (nm)$
M9	$7\ \mu m$	$17.5\ \mu m$	$13\ \mu m$	$30.5\ \mu m$
M8	720	400	410	810
M7	504	280	280	560
M6	324	180	180	360
M5	252	140	140	280
M4	216	120	120	240
M3	144	80	80	160
M2	144	80	80	160
M1	144	80	80	160



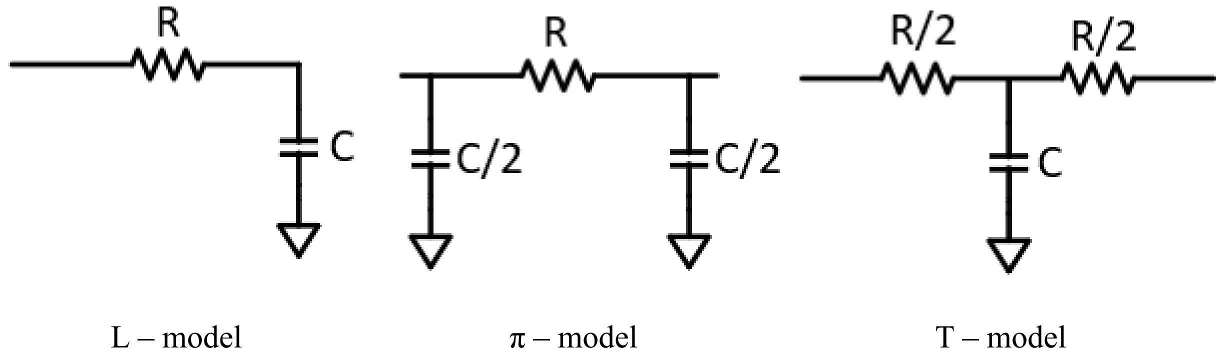
(a) (b)

Figure 2.2.2: Metal stack of Intel's (a) 90nm and (b) 45nm process [6]

2.3 Interconnect Model

An interconnect can be treated as a distributed circuit with resistance and capacitance per unit length [6]. The behavior of interconnect can be approximated by the number of lumped elements. L - model, π - model and T - model are the three standard approximations. Among the three approximation the performance of L – model is worst because to achieve accurate result numerous lumped elements are required. In case of π – model, only three segments are sufficient to achieve 97% accuracy. The accuracy of T – model is like π –

model but it is much slower compared to π – model. So, to use any of the standard model first the model for resistance and capacitance are required.



L – model π – model T – model

Figure 2.3.1: Lumped approximation of distributed RC circuit [6]

2.4 Resistance Model

The model for the resistance of an interconnect is more straight forward compared to capacitance. The resistance of a uniform rectangular interconnect can be formulated as Eq. (1).

$$R = \frac{\rho L}{WH} \tag{1}$$

Where ρ is the resistivity of the interconnect material, L is the length of the interconnect, W is the width of the interconnect and H is the thickness of the interconnect.

Eq. (1) can also be expressed as Eq. (2).

$$R = R_{\diamond} \frac{L}{W} \tag{2}$$

In Eq. (2) $R_{\diamond}(= \rho/H)$ is the sheet resistance and has the unit Ω/square.

2.5 Capacitance Model

The classical formula for calculating the capacitance of a rectangular interconnect over a ground plane is expressed as Eq. (3) also known as parallel plate capacitance.

$$C = \frac{\varepsilon_{ox} WL}{T} \tag{3}$$

Where ε_{ox} is the dielectric constant of the oxide material used between the interconnect and the ground plane. Considering only the capacitance in Eq. (3) for the interconnect model is not sufficient for sub-micron technology as the aspect ratio of the interconnect is higher than previous generations and the interconnect are densely packed. The higher aspect ratio introduces fringing capacitance and the reducing spacing between interconnects produces coupling capacitances become dominant over parallel plate capacitance [3], [2], [7]. The fringing capacitance is very complicated to compute and to get an accurate result a numerical field solver is required. Over the decades, there have been numerous models proposed in the literature to capture interconnect capacitances of high-speed integrated circuits based on empirical, numerical, and analytical methods.

A method is proposed in [8] based on 'sub-area' method. In this method the calculation error was eliminated by divide the system into sub-aera. By using this method, the capacitance of a single interconnect over a ground plane is expressed as Eq. (4).

$$\frac{C_1}{\varepsilon_{ox}L} = 1.15\left(\frac{W}{T}\right) + 2.80\left(\frac{H}{T}\right)^{0.222} \tag{4}$$

Capacitance of three interconnect over a ground plane is expressed as Eq. (5).

$$\frac{C_3}{\varepsilon_{ox}L} = C_1 + 2\left[0.03\left(\frac{W}{T}\right) + 0.83\left(\frac{H}{T}\right) - 0.07\left(\frac{H}{T}\right)^{0.222}\right]\left(\frac{S}{T}\right)^{-1.34} \tag{5}$$

The relative error of this model is less than 10% when $0.3 < \frac{W}{T} < 10$, $0.3 < \frac{H}{T} < 10$ and $0.5 < \frac{S}{T} < 10$.

The model proposed in [9] where a conductor with a rectangular middle part and two hemispherical end section was placed over a ground plane. Eq. (6) shows the expression for the capacitance when $W \geq \frac{H}{2}$ and in Eq. (7) when $W < \frac{H}{2}$.

$$\frac{C}{\varepsilon_{ox}L} = \left[\frac{\left(W - \frac{H}{2}\right)}{T} + \frac{2\pi}{\ln\left(1 + \frac{2T}{H} + \sqrt{\frac{2T}{H}\left(\frac{2T}{H} + 2\right)}\right)}\right] \tag{6}$$

$$\frac{C}{\varepsilon_{ox}L} = \left[\frac{W}{T} + \frac{\pi\left(1 - 0.0543\,\frac{H}{2T}\right)}{\ln\left(1 + \frac{2T}{H} + \sqrt{\frac{2T}{H}\left(\frac{2T}{H} + 2\right)}\right)} + 1.47\right] \tag{7}$$

The model is accurate within 10% when the aspect ratio is less than 2 and $T = H$.

A computationally efficient model was proposed in [10] which is accurate within 6% for aspect ratio less than 3.3. The proposed capacitance model is shown in Eq. (8).

$$\frac{C}{\varepsilon_{ox}L}\left[\frac{W}{T} + 0.77 + 1.06\left(\frac{W}{T}\right)^{0.25} + 1.06\left(\frac{H}{T}\right)^{0.5}\right] \tag{8}$$

Although those models discussed above are still extensively used, but they don’t take into account the aspect ratio of modern interconnect technology (where the height is greater than the width), as a result lacking the accuracy required for current VLSI interconnect capacitance calculation [3]. A two-dimensional numerical solution by Green’s function is used in [11] to calculate the capacitance of a single interconnect in a homogeneous medium. Boundary-element method (BEM) [12] [13] [14] [15] [16], finite element method [17], finite difference method [18], and semi-analytical approaches [19], [20] are also used in the

literature for capacitance modeling of complex interconnect structures. Still, these approaches are computationally expensive, and not suitable to implement in CAD tools. A number of empirical models are proposed in [21] [22] [8] [23] for a specific set of interconnects geometries but these models are complicated and strictly limited to a small number of interconnect configurations. The model proposed in [23] considers fringing capacitance originate from top-wall to ground plane, parallel plate approximation is used to estimate the side-wall fringing capacitance. These models are simple and works well for a conductor with aspect ratio less than 1, the accuracy is not acceptable in the current VLSI technology nodes. Analytical expressions are given in [24] and [9] by modifying the thickness of a rectangular interconnect to a circular cross-section. Expressions in [9] closely follow two-dimensional simulation results, but model is only valid for aspect ratio less than half. The capacitance model discussed in [24] is based on the approximation that the heigh of a interconnect is equal to a diameter of circular interconnect cross-section. It reduces the effective width by half of its thickness. The model is not valid when the aspect ratio of the interconnect is equal to 1, in that case model doesn't converge. Both models in [24] and [9] do not take into account the fringing electric field coming from the top surface of the interconnect. A fringing capacitance model is proposed in [25], which considers the nonlinearities of second-order effects of field interactions. Although the model provides a closed-form solution with good accuracy, the expression is complex to be used in regular circuit analysis. A number of experimental models for capacitance calculation have been

proposed in [26] [27] [28] [29] that estimate on-chip wiring capacitances. The models are based on “charge based capacitance measurements”. Although these methods provide higher accuracy compared to empirical or analytical models, they are useful only for post-manufacturing stages.

CHAPTER 3

ACCURATE MODELING OF INTERCONNECT CAPACITANCE IN MULTILEVEL INTERCONNECT STRUCTURES FOR SUB 22NM TECHNOLOGY

3.1 Introduction

The increasing demand for higher performance and multiple functions lead to smaller devices and increasing chip density, which makes the interconnect role dominant over device performance in nanoscale integrated circuits. Therefore, it is essential to accurately model different capacitive components of interconnect lines to estimate delay and crosstalk noise in early design phases. With continuous scaling, the aspect ratio (height/width) of interconnect has become more than unity. As a consequence, the fringing and the coupling capacitances are becoming dominant over parallel-plate ground capacitance [3], [2], [7]. Moreover, the total overlap capacitance between interconnect lines in the adjacent layers are also getting stronger due to a higher number of metal layers [30].

3.2 Analyzing Electric Field Distribution in Multi-Layer Interconnect Structure

3.2.1 Single Interconnect Line Over A Ground Plane

We have analyzed the electric field distribution of interconnects over the ground plane. We started with a simple structure where there is one interconnect line placed on the ground plane. We observed how electric fields originate from the interconnect and ends up on the ground plane. Figure 3.2.1(a) shows an interconnect line over a ground plane where

the interconnect line is surrounded by an insulating material (SiO_2). In the figure the height (H) of the interconnect is $0.1\mu m$, width (W) is $0.05\mu m$, length of the interconnect is 1μm, and the thickness (T) of the oxide layer (distance between the bottom of the interconnect line and the top of the ground plane) is $0.1\mu m$. Figure 3.2.1(b) shows the electric field distribution in xz-plane for the structure shown Figure 3.2.1(a). The applied voltage is 1V. It is observed from Figure 3.2.1(b) that electric field lines are coming not only from the bottom wall to the ground plane but also from the sidewall as well as from the top to the ground plane. The electric field tends to bend close to the corner of the interconnect line. The electric field line those are originated at the bottom plate and terminate to the ground plane in a straight line are less compared to the lines those are bend at the corner.

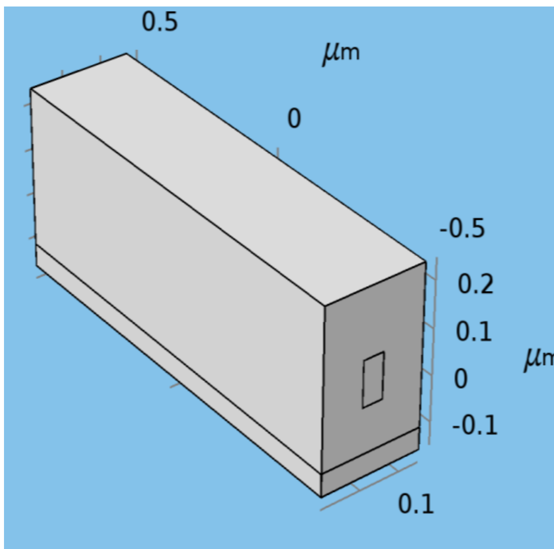
3.2.2 Capacitance Model for A Single Interconnect Line Over the Ground Plane

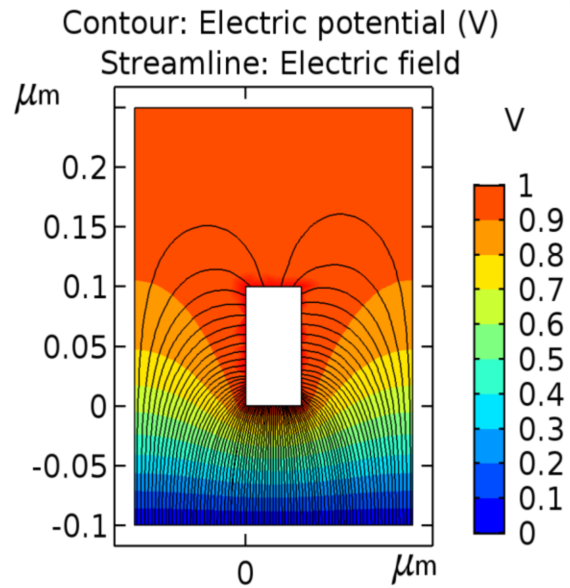
The basic idea behind the self-capacitance model of a single interconnect is effectively analyzing electrical flux lines coming out of that line. From a quick observation of the electric field distribution shown in Figure 3.2.1(b), it is concluded that self-capacitance has mainly three components:

a. Capacitance due to line to ground field.

b. Capacitance due to side wall and top wall fringing field.

c. Capacitance due to corner fringing field.





(a) (b)

Figure 3.2.1: (a) Single interconnect line over a ground plane. The interconnect line is surrounded SiO_2. (b) Electric potential (Contour) and Electric filed distribution for a single interconnect line over a ground plane.

3.2.2.1 Capacitance Due to Line to Ground Field.

The capacitance due to line to the ground field can be easily modeled by the parallel-plate capacitance approximation and can be expressed as Eq. (1) where W is the width of the interconnect, T is the distance between the interconnect and the ground plane (also known as the dielectric thickness), L is the length of the interconnect (not shown in the figures) and ε is dielectric constant.

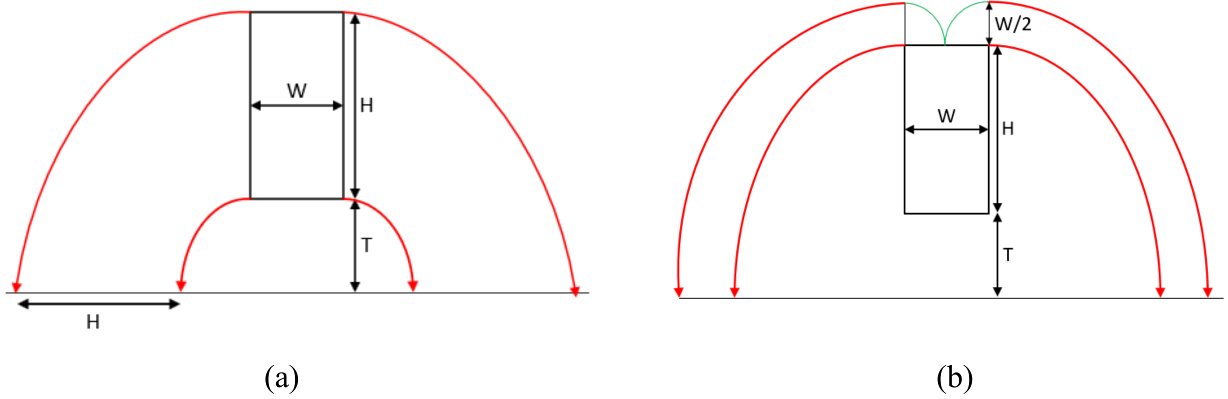
$$\frac{C_{PP}}{\varepsilon L} = \frac{W}{T} \tag{1}$$

3.2.2.2 Capacitance Due To Side Wall And Top Wall Fringing Field

The capacitance due to the fringing field between the sidewall of the interconnect and the ground plane can be approximated by assuming that the electric field originating from the sidewall of the interconnect follows a circular path to the ground. The electric field lines are originating from T (at the bottom of the interconnect) to $H + T$ (at the top of the interconnect). If the length (distance) of the electric field that originates from the bottom of the interconnect to the ground is ${}^{\pi r}/_{2}$ (assuming the radius is r), we can approximate the capacitance due to the fringing fields using Eq. (2).

$$\frac{C_{fringe}}{\varepsilon L} = \int \frac{width}{distance} \tag{2}$$

$$C_{fringe,sidewall} = \int_{T}^{H+T} \frac{dr}{{}^{\pi r}/_{2}} = \frac{2}{\pi} \ln\left(1 + \frac{H}{T}\right) \tag{3}$$



(a) (b)

Figure 3.2.2: (a) Fringing field lines originating from the sidewall of the interconnect line (b) approximate fringing field lines originating from the top wall of the interconnect line.

The capacitance due to the fringing field originating from the top of interconnect can be formulated the same way as we formulate sidewall fringing field capacitance. For simplicity, a portion of the fringing field is not considered (indicated by the green line in Figure 3.2.2(b)) so that the electric field approximated to have a circular path starting from the top of the interconnect $(T + H)$ to the ground, extending to height $(T + H + \frac{W}{2})$. Using Eq. (2) to approximate the top wall fringing capacitance, $C_{fringe,topwall}$ can be expressed as Eq. (4).

$$C_{fringe,topwall} = \int_{H+T}^{H+T+W/2} \frac{dr}{\pi r/2} = \frac{2}{\pi} \ln\left(1 + \frac{W}{2(H+T)}\right) \quad (4)$$

3.2.2.3 Capacitance Due to Corner Fringing Field

Finally, $C_{cornerfringe}$ is the capacitance due to the point charge located at the corner of the bottom of the interconnect. Unlike $C_{fringe,topwall}$ or $C_{fringe,sidewall}$ the electric field lines for $C_{cornerfringe}$ are originated from a single point. So instead of circular electric field approximation, we have to use elliptical field line approximation (as shown in Figure 3.2.3). Assuming the first electric field is very close to the origin ($x \approx 0$), we can approximate the capacitance due to the corner fringing filed as Eq. (5).

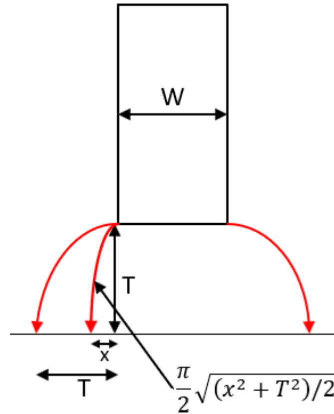


Figure 3.2.3: Approximated electric field lines originating from the corner of the interconnect.

$$C_{cornerfringe} \approx \int_0^T \frac{dx}{\frac{\pi}{2}\sqrt{\frac{(x^2+T^2)}{2}}} = \frac{3\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right) \quad (5)$$

From Eq. (5) we observe that $C_{cornerfringe}$ is constant, but observation from the simulation data indicate that it should increase with decreasing the oxide thickness (T). So $C_{cornerfringe}$ can be expressed as Eq. (6).

$$C_{cornerfringe} = \alpha_1 \frac{3\sqrt{2}}{\pi} \ln\left(1 + \sqrt{2}\right) \tag{6}$$

Where $\alpha_1 = \left(\frac{W}{T}\right)$. As the top corners of the interconnect are far away from the ground plane, they are not considered for the capacitance calculation.

So, the total capacitance between the interconnect and the ground plane is the summation of parallel plate capacitance (C_{PP}), two side-wall capacitance ($C_{fringe,sidewall}$), top-wall capacitance ($C_{fringe,topwall}$) and two bottom corner capacitance ($C_{cornerfringe}$).

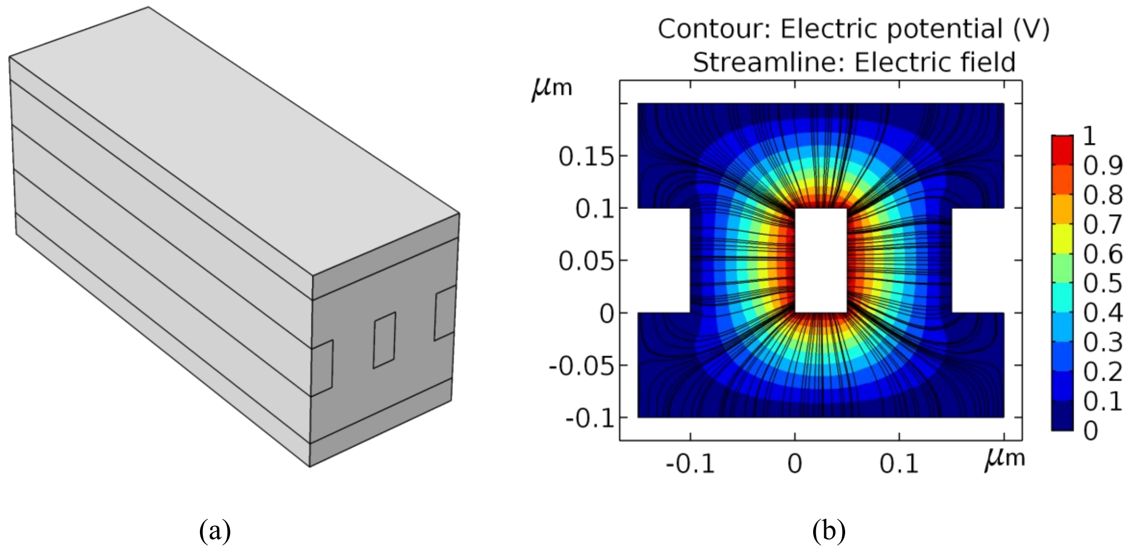
$$\frac{C_{total,single}}{\varepsilon L} = C_{PP} + 2C_{fringe,sidewall} + 2C_{fringe,topwall} + 2C_{cornerfringe} \tag{7}$$

$$\frac{C_{total,single}}{\varepsilon L} = \frac{W}{T} + \frac{4}{\pi} \ln\left(1 + \frac{H}{T}\right) + \frac{4}{\pi} \ln\left(1 + \frac{W}{2(H+T)}\right) + \alpha_1 \frac{6\sqrt{2}}{\pi} \ln\left(1 + \sqrt{2}\right) \tag{8}$$

3.2.3 Three Interconnect Lines Between Two Ground Planes

Figure 3.2.4(a) shows three parallel interconnect lines between two ground planes. In the figure the height (H) of the interconnect is $0.1\mu m$, width (W) is $0.05\mu m$, length of the interconnect is $1\mu m$, the distance between the bottom of the interconnect line and the top of the ground plane (T) is $0.1\mu m$, and the separation (S) between two interconnect lines is $0.1\mu\text{m}$.

To capture the influence of the distance between the bottom plate to the ground plane (insulator thickness T) and separation between neighboring interconnect lines (S), we analyze the different combinations of 'S' and 'T.' Figure 3.2.5 shows two such combinations where (a) $T = 0.1\mu m, S = 0.025\mu m$, (b) $T = 0.025\mu m$, $S = 0.1\mu m$. It has observed that when 'S' is smaller than 'T'$(S < T)$, the field originating from the sidewall of the interconnect no longer ended up on the ground plane. Still, some of the electric field lines that originate from the bottom plate end up on the neighboring bottom plate, as shown in Figure 3.2.5(a). The electric field lines from the sidewall end up on the ground plane occurs when insulator thickness is greater than interconnect separation $(T > S)$, as shown in Figure 3.2.5(b). So, there is a transition point when this transition occurs. We varied 'T' and 'S' from $0.01\mu m$ to $0.5\mu m$ and analyzed each combination and found that electric field lines from the sidewall end up in ground plane when $S > 1.5T$ and electric field lines from the bottom plate of one interconnect lines to the bottom plate of the neighboring interconnect line happens when $S < 1.5T$.

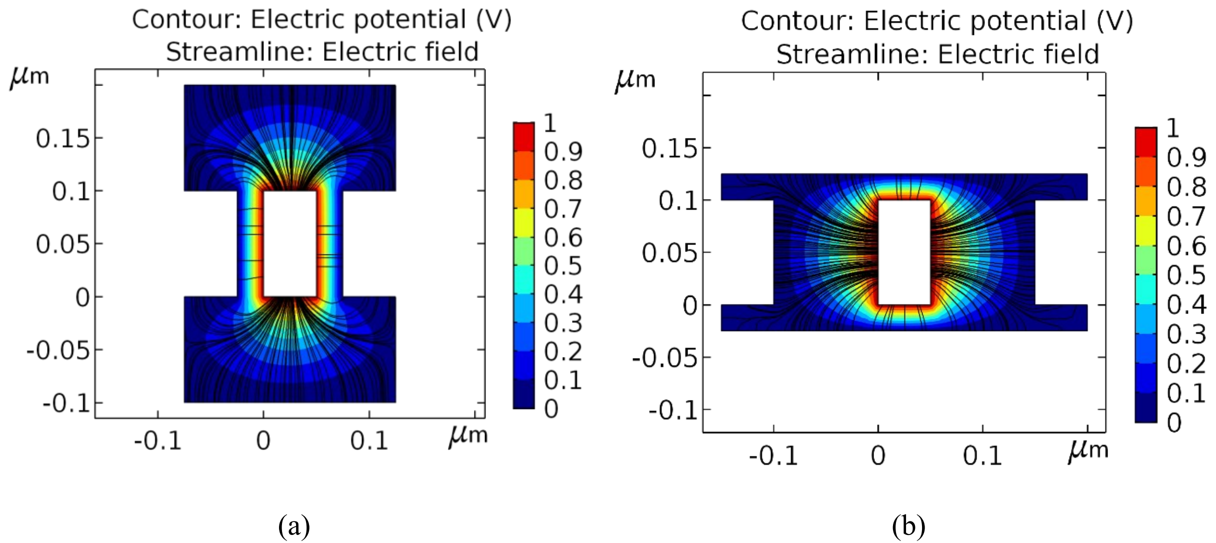


(a) (b)

Figure 3.2.4: (a) Three interconnect lines sandwiched between two ground planes. The interconnect lines are surrounded by SiO_2. (b) Electric potential (Contour) and Electric filed distribution for three parallel interconnect lines between two ground planes. Here insulator thickness $(T) = 0.1\mu m$ and separation (S) between adjacent interconnect is $0.1\mu m$

3.2.4 Capacitance Model of Multiple Lines Between Two Ground Planes

In this subsection, we formulate the expressions of capacitance for multiple lines running in parallel between two ground planes by using the concept developed in the previous subsection. We consider only three lines between ground planes, as shown in Figure 3.2.4(a), where the middle line (the line of interest) is sandwiched between two neighboring lines.



(a) (b)

Figure 3.2.5: Electric field distribution of two parallel interconnect lines over a ground plane for various combination of insulator thickness (T) and separation (S). (a) $T = 0.1\mu m, S = 0.025\mu m$, *(b)* $T = 0.025\mu m, S = 0.1\mu m$.

Since capacitive coupling is a short-range phenomenon, we do not consider the next order neighboring lines beyond the immediate left and then immediately right neighbors while calculating the coupling capacitance of the middle line. We assume that two neighboring lines are grounded to ignore electric flux originating from them since it simplifies the flux distribution of the structure. However, if these two neighboring lines also carry signals (driven by a driver), the effective coupling capacitance will be multiple of that when connected to ground depending on the switching activities of the coupled lined, as discussed in the subsequent section.

Based on the electric field distribution observed in Figure 3.2.5(a),(b), depending on oxide thickness (T) and spacing between neighboring interconnect (S) we can separate the capacitance formulation into two part, a. when $S > \frac{3}{2}T$ and b. when $S < \frac{3}{2}T$.

3.2.5 When the Spacing Between the Interconnect Is Greater Than the Oxide Thickness ($S > \frac{3}{2}T$)

3.2.5.1 Capacitance Due to Line to Ground Field

Bottom side field lines form a parallel-plate capacitance (C_{PP}) with the ground plane like the single line.

$$\frac{C_{PP}}{\varepsilon L} = \frac{W}{T} \tag{9}$$

3.2.5.2 Capacitance Due to Corner Fringing Field

There will be fringing capacitance between the corners of the neighboring interconnect. The corner fringing capacitance will contribute to the total capacitance depending on the insulator thickness and separation between two neighboring interconnects. The $C_{fringe,corner}$ can be evaluated as same procedure as Eq. (6). Eq. (10) shows the resulting formula for $C_{fringe,corner}$.

$$C_{fringe,corner} = \alpha_2 \frac{3\sqrt{2}}{\pi} \ln\left(1 + \sqrt{2}\right) \quad (10)$$

Where $\alpha_2 = \left(\frac{W+S}{T}\right)$.

3.2.5.3 Capacitance Due to Side Wall to Ground Fringing Field

Fringing fields from the smaller segment H_1 form capacitance with the ground. We model this component ($C_{fringe,sidewall}$) like what we have done for the single interconnect case. Unlike the single interconnect case not all the side wall electric field contribute to the sidewall to ground fringing capacitance. A smaller portion of the side wall (H_1), the value of which depends on the separation between interconnect (S) and the oxide thickness (T). The electric field lines at the edge of parallel plates are not precisely straight lines. Figure 3.2.6 shows the electric field lines originated from the segment H_1 of the side wall. The electric field approximated to have a circular path starting from the bottom of the interconnect (T) to the ground, extending to height ($T + H_1$). $C_{fringe,sidewall}$ can be expressed as Eq. (11).

$$C_{fringe,sidewall} = \int_{T}^{T+H_1} \frac{dr}{\pi r/2} = \frac{2}{\pi} \ln\left(1 + \frac{H_1}{T}\right) \quad (11)$$

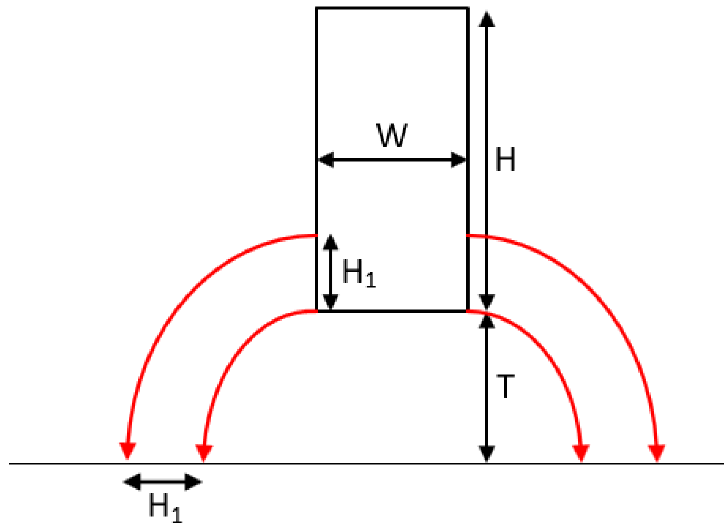


Figure 3.2.6: Approximated electric field lines originating from a portion of the sidewall of the interconnect.

3.2.5.4 Capacitance Due to Side Wall to Bottom Plate Fringing Field

A small portion of electric field from the side of the interconnect ends up on the bottom of the neighboring interconnect. We assume that the segment of the electric field originating from the sidewall that ends on the bottom of the neighboring interconnect is not more than 10%. Figure 3.2.7 shows the electric field that originated from the segment H_2 $(= 0.1H_1)$. To formulate this capacitance, we divide the electric field into two parts. The first section of the electric filed that originate from the sidewall and ends in between the two interconnects (at $S/2$). The electric filed in this section assume to have elliptical shape. Eq. (12) shows the capacitance due to the elliptical portion of the electric field.

$$C_{fringe,side-bottomwall_e} = \int_{H_1}^{H_1+H_2} \frac{dr}{\frac{\pi}{2}\sqrt{\frac{\left(r^2+\left(\frac{S}{2}\right)^2\right)}{2}}}$$

$$C_{fringe,side-bottomwall_e} = \frac{3\sqrt{2}}{\pi}\ln\left(\frac{(H_1+H_2)+\sqrt{(H_1+H_2)^2+\left(\frac{S}{2}\right)^2}}{(H_1)+\sqrt{(H_1)^2+\left(\frac{S}{2}\right)^2}}\right) \quad (12)$$

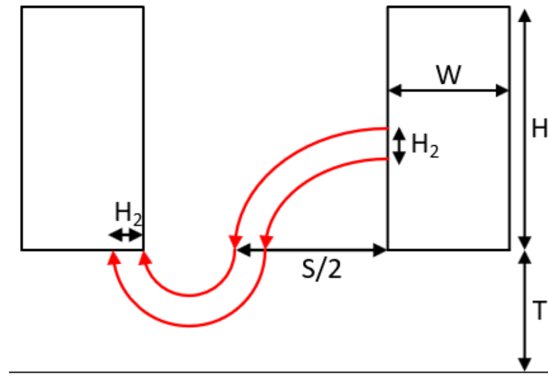


Figure 3.2.7: Approximated electric field lines originating from a portion of the sidewall of the interconnect that ends up on the bottom portion of neighboring interconnect.

In the second section we have a circular electric field pattern. The inner circle assumes to have a diameter $\left(\frac{S}{2}\right)$. Eq. (13) shows the capacitance due to the circular portion of the electric field.

$$C_{fringe,side-bottomwall_c} = \int_{\frac{S}{2}}^{\frac{S}{2}+H_2} \frac{dr}{\pi r} = \frac{1}{\pi}\ln\left(1+\frac{2H_2}{S}\right) \quad (13)$$

So, the total capacitance due to the circular and elliptical field can be represented as Eq. (14).

$$C_{fringe,side-bottomwall} = series(C_{fringe,side-bottomwall_c}, C_{fringe,side-bottomwall_e})$$

$$C_{fringe,side-bottomwall} = series\left(\frac{1}{\pi}\ln\left(1+\frac{2H_2}{S}\right), \frac{3\sqrt{2}}{\pi}\ln\left(\frac{(H_1+H_2)+\sqrt{(H_1+H_2)^2+\left(\frac{S}{2}\right)^2}}{(H_1)+\sqrt{(H_1)^2+\left(\frac{S}{2}\right)^2}}\right)\right) \quad (14)$$

3.2.5.5 Capacitance Due to Side Wall Parallel Plate Field

The remaining electric field that originates from the sidewall ends up on the sidewall of the neighboring interconnect, creating a parallel plate equivalent capacitance as shown in Eq. (15).

$$\frac{C_{PP,sidewall}}{\varepsilon L} = \frac{H-2H_1-2H_2}{S} \quad (15)$$

In summary, the total capacitance of an interconnect line between two neighboring interconnect line and between two grounds can be formulated as Eq. (16), when the separation between the interconnects is greater than the oxide thickness ($S > \frac{3}{2}T$).

$$C_{total} = 2C_{PP} + 4C_{fringe,corner} + 4C_{fringe,sidewall} + 4C_{fringe,side-bottomwall} + 2C_{PP,sidewall} \quad (16)$$

$$\frac{C_{total}}{\varepsilon L} = 2\frac{W}{T} + 4\alpha_2\frac{3\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right) + 4\frac{2}{\pi}\ln\left(1+\frac{H_1}{T}\right) + 2\frac{H-2H_1-2H_2}{S}$$
$$+4series\left(\frac{1}{\pi}\ln\left(1+\frac{2H_2}{S}\right), \frac{3\sqrt{2}}{\pi}\ln\left(\frac{(H_1+H_2)+\sqrt{(H_1+H_2)^2+\left(\frac{S}{2}\right)^2}}{(H_1)+\sqrt{(H_1)^2+\left(\frac{S}{2}\right)^2}}\right)\right) \quad (17)$$

3.2.6 When the Spacing Between the Interconnect Is Less Than The Oxide Thickness ($S < \frac{3}{2}T$)

3.2.6.1 Capacitance Due to Line to Ground Field

When the oxide thickness (T) is greater than the spacing between the interconnect (S), not all the electric fields originating from the bottom of the interconnect ends on the ground plane. A portion of the electric field also ends up on the bottom of the neighboring interconnect as shown in Figure 3.2.5(a) and Figure 3.2.8. We assume the electric field lines

originate from the portion $(W - \alpha_3 W)$ terminate on the ground. The value of α_3 depends on the oxide thickness (T) and the separation (S). α_3 increases if the spacing between neighboring interconnect decreases or the oxide thickness (T) decreases. So, we can express the capacitance due to the line to ground field as Eq. (18).

$$C_{PP} = \frac{(W - \alpha_3 W)}{T} \quad (18)$$

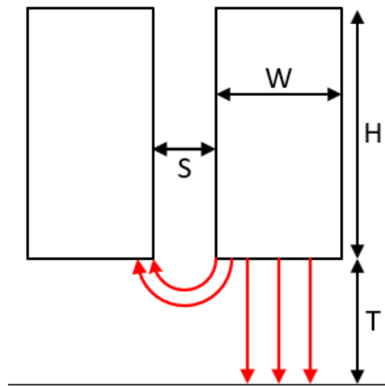


Figure 3.2.8: Approximated electric field lines originating from the bottom of the interconnect. A portion of the electric field lines ends up on the ground and the remaining part ends up on the bottom of the neighboring interconnect.

3.2.6.2 Capacitance Due to Bottom Plate to Bottom Plate Fringing Field

The remaining section of the electric field originates from the middle interconnect ends up in the neighboring interconnect creating a circular path. Eq. (19) shows the capacitance formula for $C_{fringe,bottom-bottom}$.

$$C_{fringe,bottom-bottom} = \int_{S}^{S+\alpha_3 W} \frac{dr}{\pi r} = \frac{1}{\pi} \ln\left(1 + \frac{\alpha_3 W}{S}\right) \quad (19)$$

3.2.6.3 Capacitance Due to Corner Fringing Field

When corners of the neighboring interconnect come close they generates capacitance depending on how close the corners are. Eq. (20) shows the $C_{fringe,corner}$ model.

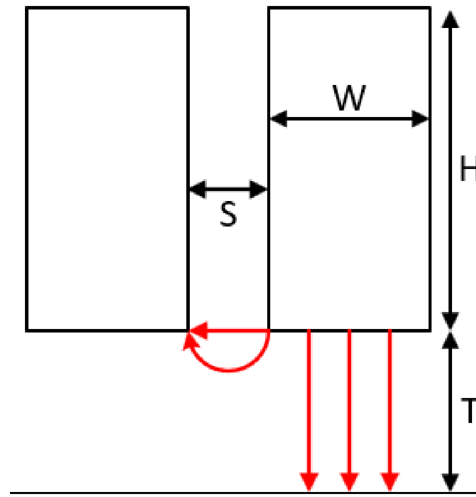


Figure 3.2.9: Electric field generates from the corner of interconnect.

$$C_{fringe,corner} \approx \int_{0}^{S} \frac{dr}{\pi\sqrt{\frac{(r^2 + S^2)}{2}}} = \frac{\sqrt{2}}{\pi} \ln(1 + \sqrt{2}) \quad (20)$$

$C_{fringe,corner}$ depends on the spacing between two interconnects but the model does not reflect that. So, we add a depending variable α_4 whose value depends on the interconnect spacing (S).

3.2.6.4 Capacitance Due to Sidewall-to-Sidewall parallel Field

Capacitance due to sidewall-to-sidewall electric field is basically the parallel plate capacitance where the width equivalent is H (height of the interconnect) and oxide thickness equivalent is spacing (S)

$$C_{PP,sidewall} = \frac{H}{S} \tag{21}$$

In summary, the total capacitance of an interconnect line between two neighboring interconnect line and between two grounds can be formulated as Eq. (16), when the separation between the interconnects is smaller than the oxide thickness ($S < \frac{3}{2}T$).

$$C_{total} = 2C_{PP} + 4C_{fringe,corner} + 2C_{PP,sidewall} + 4C_{fringe,bottom-bottom} \tag{22}$$

$$\frac{C_{total}}{\varepsilon L} = 2\frac{(W - \alpha_3 W)}{T} + 4\frac{\sqrt{2}}{\pi}\ln\left(1 + \sqrt{2}\right) + 2\frac{H}{S} + 4\frac{1}{\pi}\ln\left(1 + \frac{\alpha_3 W}{S}\right) \tag{23}$$

3.2.7 Capacitance Model of Multiple Lines Over a Ground Plane (Special Case)

A special case of the previous section is when multiple interconnect lines placed over a single ground plane. The electric field distribution on the bottom half of the interconnect is exactly same as the previous section, but on the top section as there is no ground plane, we only have corner fringing capacitance and topwall-to-topwall fringing capacitance as shown in Figure 3.2.10.

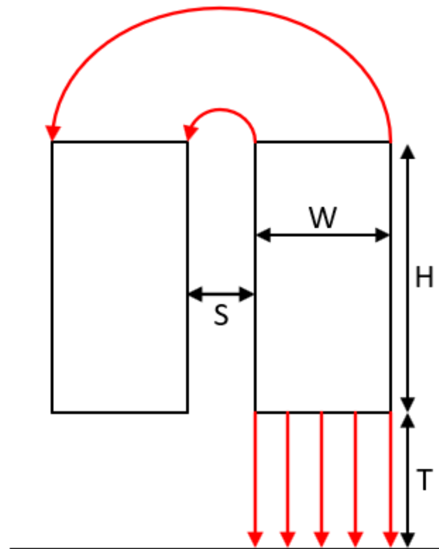


Figure 3.2.10: Electric field distribution of multiple interconnect line over a single ground plane.

The corner fringing field and the topwall-to-topwall fringing field can be formulated as Eq. (24) and Eq. (25).

$$C_{fringe,corner-top} \approx \int_{0}^{S} \frac{dr}{\pi\sqrt{\frac{(r^2+S^2)}{2}}} = \frac{\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right) \times \alpha_5 \tag{24}$$

$$C_{fringe,topwall-topwall} = \int_{S}^{S+W} \frac{dr}{\pi r} = \frac{1}{\pi}\ln\left(1+\frac{W}{S}\right) \tag{25}$$

So the total capacitance when $S > \frac{3}{2}T$ is the summation of C_{PP}, $C_{fringe,corner}$, $C_{fringe,topwall-topwall}$, $C_{fringe,corner-top}$, $C_{fringe,sidewall}$, and $C_{fringe,side-bottomwall}$ as shown in Eq. (26).

$$C_{total} = C_{PP} + 2C_{fringe,corner} + 2C_{fringe,sidewall} + 2C_{fringe,side-bottomwall} + 2C_{PP,sidewall} + 2C_{fringe,corner-top} + C_{fringe,topwall-topwall}$$

$$\frac{C_{total}}{\varepsilon L} = \frac{W}{T} + 2\alpha_2\frac{3\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right) + \frac{2}{\pi}\ln\left(1+\frac{H_1}{T}\right) + 2\frac{H-H_1-H_2}{S}$$
$$+2series\left(\frac{1}{\pi}\ln\left(1+\frac{2H_2}{S}\right), \frac{3\sqrt{2}}{\pi}\ln\left(\frac{(H_1+H_2)+\sqrt{(H_1+H_2)^2+\left(\frac{S}{2}\right)^2}}{(H_1)+\sqrt{(H_1)^2+\left(\frac{S}{2}\right)^2}}\right)\right)$$
$$+2\alpha_5\frac{\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right) + \frac{1}{\pi}\ln\left(1+\frac{W}{S}\right) \quad (26)$$

Total capacitance when $S < \frac{3}{2}T$ is the summation of C_{PP}, $C_{fringe,corner}$, $2C_{PP,sidewall}$, $C_{fringe,bottom-bottom}$, $C_{fringe,topwall-topwall}$ and $C_{fringe,corner-top}$ as shown in Eq. (27).

$$C_{total} = C_{PP} + 2C_{fringe,corner} + 2C_{PP,sidewall} + 2C_{fringe,bottom-bottom} + 2C_{fringe,corner-top}$$
$$+C_{fringe,topwall-topwall}$$

$$\frac{C_{total}}{\varepsilon L} = \frac{(W-\alpha_3 W)}{T} + 2\frac{\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right) + 2\frac{H}{S} + 2\frac{1}{\pi}\ln\left(1+\frac{\alpha_3 W}{S}\right) + 2\alpha_5\frac{\sqrt{2}}{\pi}\ln\left(1+\sqrt{2}\right)$$
$$+\frac{1}{\pi}\ln\left(1+\frac{W}{S}\right) \quad (27)$$

3.3 Model Validation

An extensive comparative study is done in this section to check the accuracy of the derived analytical expressions. To justify the accuracy of the proposed model for all capacitance components, we calculate capacitances using our model and Ansys Q3D field solver for various interconnect dimensions. In the calculation, we consider local interconnect (where the capacitive coupling is prominent) of length $L = 1\mu m$ and relative dielectric constant $\varepsilon_r = 4$.

From the comparison in Figure 3.3.1, it is observed that the proposed model for interconnect configuration in Figure 3.2.1, closely matches Ansys Q3D results having a maximum error of less than 10%. To verify the results for multiple interconnects between two ground planes we varied the spacing between interconnect from $10nm$ to $500nm$ keeping the oxide thickness fixed at 100nm. We compare both the coupling capacitance and the ground capacitance with the values obtained from Q3D and maximum error when compared is about 6% as shown in Figure 3.3.2. In Figure 3.3.3 ground and coupling capacitance is compared with the values extracted from Q3D and here also the error margin is less than 8%.

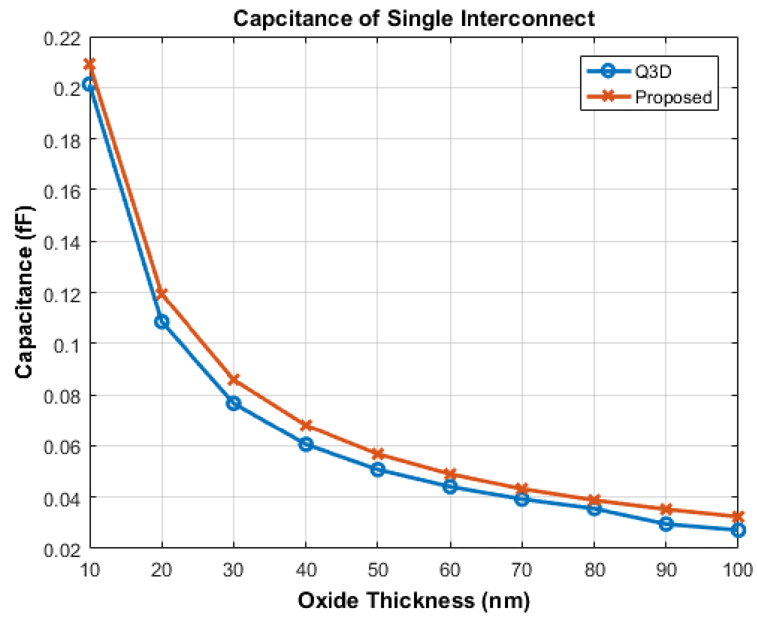
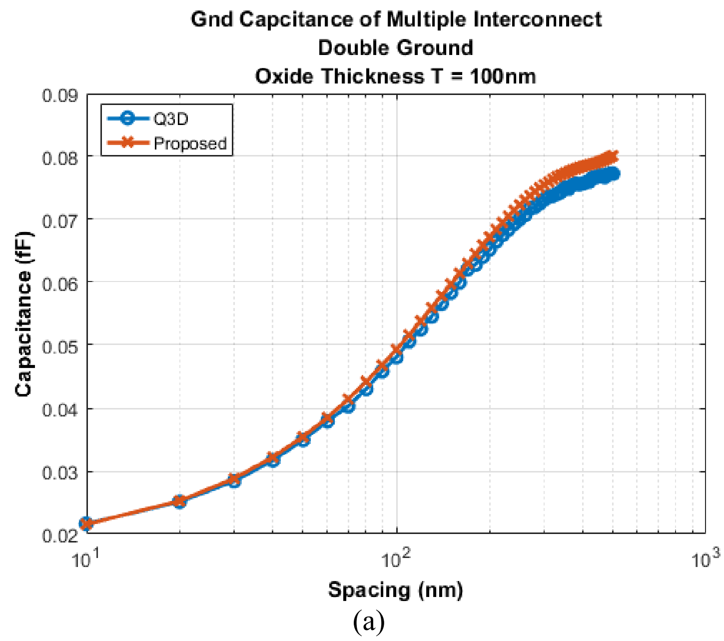
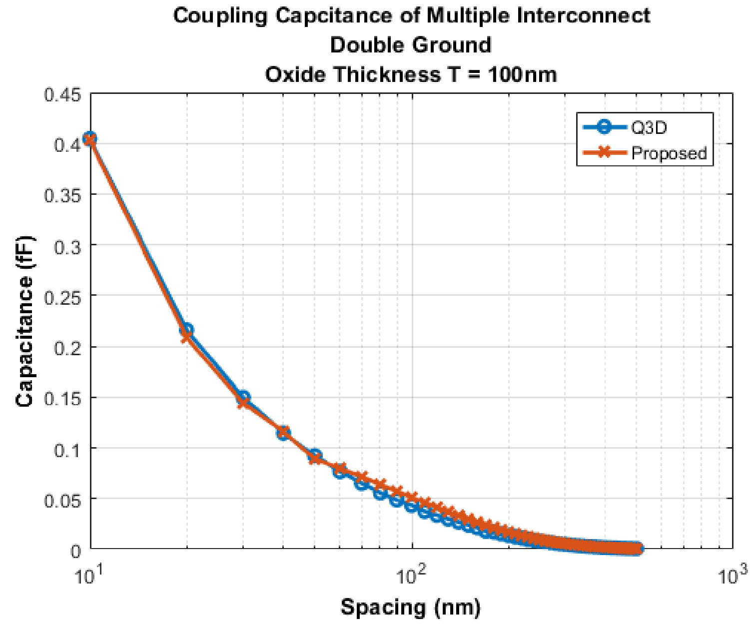


Figure 3.3.1: Total capacitance of single interconnect over a ground plane

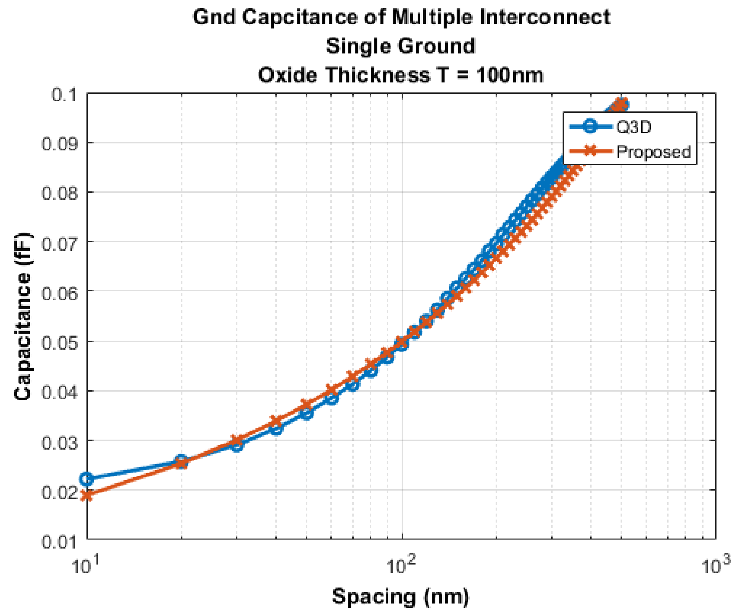


(a)

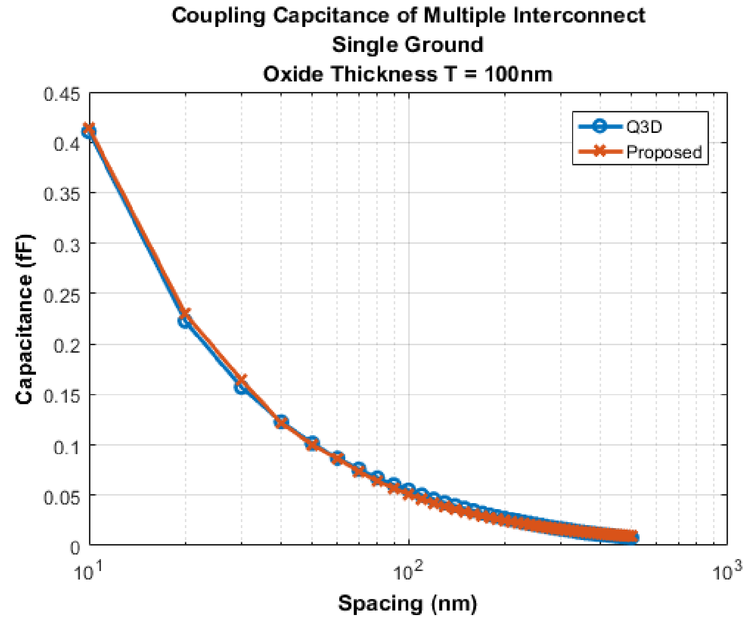


(b)

Figure 3.3.2: (a) Ground capacitance and (b) coupling capacitance of multiple interconnect line between two ground planes.



(a)



(b)

Figure 3.3.3: (a) Ground capacitance and (b) coupling capacitance of multiple interconnect line over a ground plane.

3.4 Summary

Novel analytical models for interconnect capacitance are developed by geometrically modeling electric flux lines between interconnect lines in a multilayer interconnect structure. The derived expressions are simple and show excellent agreement with the extracted capacitances by Ansys Q3D extractor field solver. While most existing capacitance models are constrained by a specific range of interconnect dimensions, the proposed models can be applied to any VLSI interconnect configurations and thus can be embedded as a quick tool in CAD circuit programs.

CHAPTER 4

ANALYSIS OF DIFFERENT MATERIALS AND STRUCTURES FOR THROUGH SILICON VIA AND THROUGH GLASS VIA IN 3D INTEGRATED CIRCUITS

4.1 Introduction

To incorporate more functionality into the traditional 2D chips different methods like transistor scaling and system-on-chip (SoC) implementation have been adopted. However, increasing density of devices leads to increasing lengths of interconnects to a great extent. Increasing interconnect resistance, capacitance, inductance, and other parasitic effects with the increasing lengths lead to higher power consumption, signal delay and noise. Signal speed in current digital systems depends mainly on the delay of interconnects [31]. To overcome these problems and keep up with the Moore's law, 3D integrated circuit (vertical integration of multiple dies) with through-silicon via (TSV) has been introduced to ensure much smaller interconnect lengths, and lower delay and power consumption compared to conventional 2D IC technology [32]. 3D TSV also offers higher system integration at lower cost [33]. But for high performance system signal integrity in these TSVs is one of the most critical issues. The number of TSV is continuously increasing with integration density [34]. Many TSVs placed close to each other result in higher crosstalk and other switching noises. In this paper, we plan to investigate the material combinations for TSV cores and interposers best suited to overcome the signal integrity problem in 3D TSVs. In recent research an alternative of TSV is being explored, where glass could be used as interposer instead of

silicon. The concept has become known as through-glass via (TGV). Here, we focus on both glass and silicon as interposer materials. For the via core we plan to explore copper (Cu), tungsten (W) and Cu-W bimetal. We have also investigated the performance of TSVs depending on their size and relative spacing, the effect of bumps and their dimensions, and the stacking of TSV layers in 3D IC.

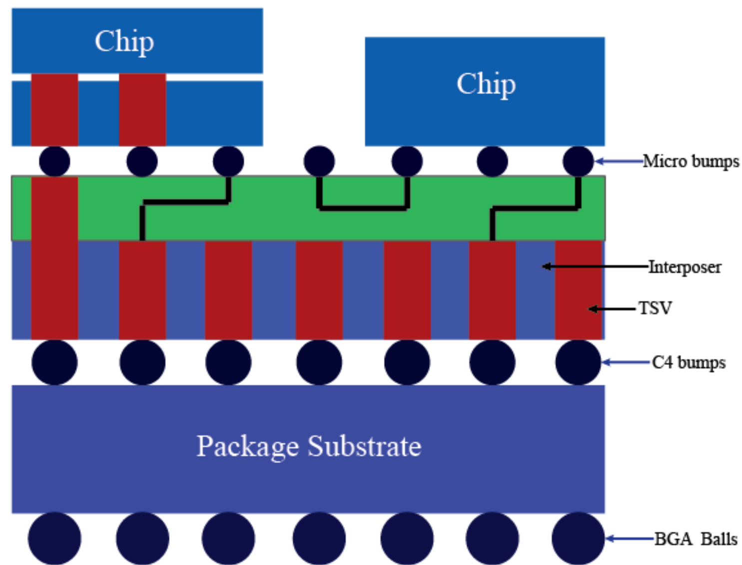


Figure 4.1.1: 3D IC with package substrate, TSVs and different bumps.

In 3D IC technology two or more layers of active elements are connected vertically to form a single IC environment as shown in Figure 4.1.1. The 3D ICs promises better performance over conventional 2D ICs because of their reduced interconnect length, heterogeneous integration capability, higher packing density and smaller footprint. Monolithic 3D IC and stacked 3D IC are two main categories of 3D IC technology. In

monolithic 3D IC, different active layers are fabricated sequentially whereas in stacked 3D IC the layers are fabricated separately and then connected vertically together using various bonding technology [35]. A typical 3D IC consists of BGA (ball grid array) to connect the IC with the power line, package substrate, C4 bumps, interposer to route the power and signal vias between C4 bumps and the micro bumps, and micro bumps (usually SnAg solder) that are used to make connection between two dies or between a die and a substrate [35]. In the interposer it is possible to integrate multiple dies. TSV based 3D integration technique is very promising because it offers high density of vertical interconnect [36].

The TSVs can be classified as 'via first', 'via middle' and 'via last' depending on when the vias are formed. In 'via first' method vias are fabricated first then transistors are fabricated; and in 'via middle' and 'via last' methods vias are formed after the transistor fabrication process. The chips in a 3D IC can be connected to each other by back-to-back or back to face or face-to-face configuration.

Figure 4.1.2 shows the simulation setup for measuring different performance matrices. The pitch (distance between two TSVs) used in the experiment is $10\mu m$. The diameter of the TSV conductor is $5\mu m$ when single material (Cu or W) is used as the core material and the SiO_2 layer has a diameter of $6\mu m$. The height of the TSVs is $32\mu m$ (as shown in Figure 4.1.3). The interposers (silicon or glass) have $100\mu m$ of length and width and $32\mu m$ of height. Air is used as the surrounding material (not shown in figure). When bimetal (Cu-W) TSV is used the diameter of the Cu via is $4\mu m$ and for W it is $5\mu m$. Other

sizes remain the same. Cu and W are the most common materials used for vias. The resistivity of Cu ($1.6\mu\Omega - cm$) is very low compared to W ($4.9\mu\Omega - cm$). But the biggest problem with the Cu-TSV is that the coefficient of thermal expansion (CTE) of Cu is $\sim 17 \times 10^{-6}/K$, which is nearly six times of the CTE of Si ($\sim 2.6 \times 10^{-6}/K$) [37]. This large difference in CTE value exerts a large negative thermo-mechanical stress (compressive) followed by a positive stress (tensile) in the active Si close to TSV at room temperature [38]. Cu-TSV also suffers back-metal contamination, which reduces the device performance [39]. The CTE of W ($\sim 4.5 \times 10^{-6}/K$) is close to the CTE of Si, so W-TSV can be used for signal lines [40]. W-TSV induces much less stress than Cu-TSV. To utilize both the advantages of Cu and W a bimetal Cu-W TSV can be used with W as outer layer and Cu as inner core. Ansoft HFSS 3D field solver software has been used to carry out the simulation.

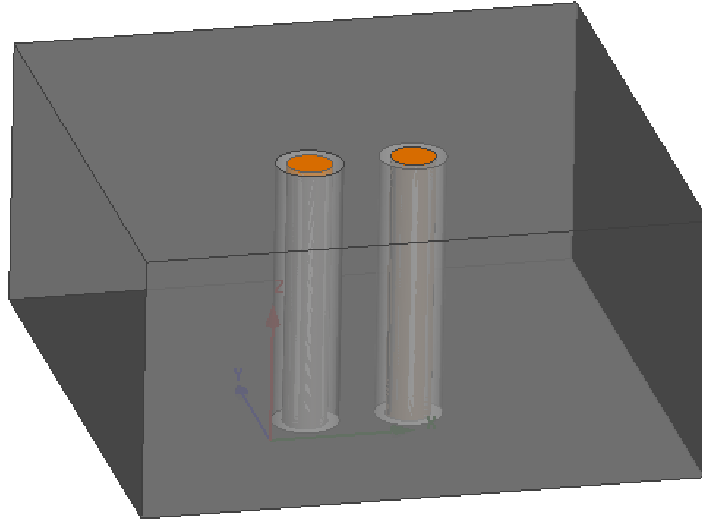


Figure 4.1.2: Simulation setup to measure return loss, transmission coefficient, near-end crosstalk (NEXT) and far-end crosstalk (FEXT). The distance between the signal TSV and the ground TSV is 10µm (pitch).

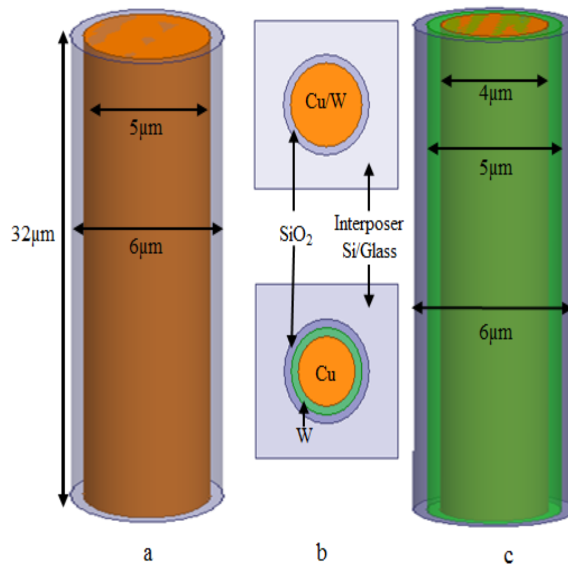


Figure 4.1.3: a. TSV of height 32µm and diameter 5µm with 6µm of SiO_2 layer (thickness 0.5µm) b. cross sectional view of Cu/W TSV (top) and bimetal (Cu-W) TSV (bottom) as the core surrounded by SiO_2 insulating layer and Si/Glass interposer c. TSV of height $32\mu m$, Cu core with diameter $4\mu m$ and W layer with thickness $0.5\mu m$.

4.2 Result and Analysis

4.2.1 Return Loss in TSV For Different Materials

Return loss is defined as the effectiveness of the power delivery from a transmission line [41]. Figure 4.2.1 shows the reflection coefficient (S_{11}) for TSVs in silicon interposer with different materials. The large negative number in decibel scale indicates the magnitude of the return signal is low (Pr/Pi ratio is low) so the return loss is low. It is observed that at lower frequencies (<1GHz) all TSVs showed almost same reflection coefficient ($S_{11} \approx -25dB$). At higher frequencies (>5GhHz) the S_{11} varies from -3dB to -2dB where W coated Cu TSV showed highest return loss (higher S_{11}) and Au TSV showed the lowest return loss (lower S_{11}). According to the simulation result W TSV had lower return loss than Cu TSV. Though the loss in Au is lower than conventional metals like Cu and W and it is not economically feasible to use Au as a core material for mass scale production Au may not be a practical choice for TSV core material.

In Figure 4.2.2 the reflection coefficient of Cu, W and Cu-W bimetal TSV buried in glass interposer is measured. Like silicon interposer here also the low frequency all three TSVs showed identical loss pattern but at higher frequencies W TSV showed better performance than Cu-W and Cu alone TSV. But the differences between the losses between them are minimal.

Discontinuities in the structure or impedance mismatch are the major reason for return loss to occur. As the impedance of core is function of frequency at higher frequency

the impedance of the core changes significantly and that creates mismatch with the core of the TSV and source resulting higher return loss in high frequency.

Table 2

TSV parameters and their values

Geometrical parameters	**Typical value**
Radius of TSV	2.5µm
Radius of SiO2 layer	3µm
SiO2 thickness	0.5µm
Height of the TSV	10µm
Pitch	10µm
Number of TSV used	2
Pitch	10µm
Relative permittivity (Cu)	1
Relative permittivity (W)	1
Relative permittivity (Si)	11.9
Relative permittivity (Glass)	5.5
Relative permittivity (SiO2)	4

Bulk Conductivity (Cu)	58×106S/m
Bulk Conductivity (W)	18.2×106S/m
Bulk Conductivity (Si)	0
Bulk Conductivity (Glass)	0
Bulk Conductivity (SiO2)	0

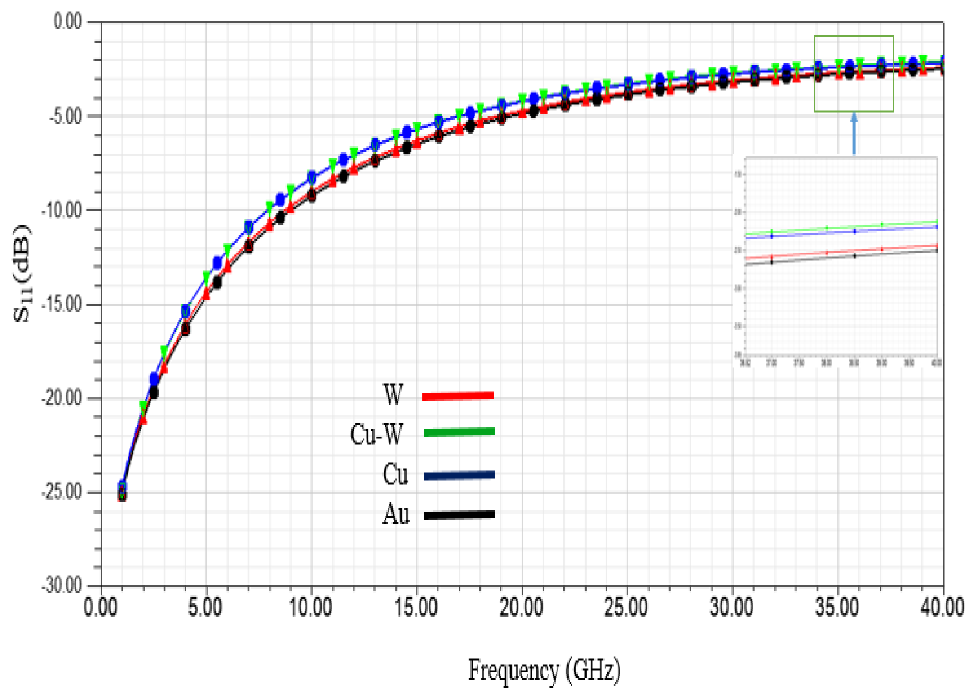


Figure 4.2.1: HFSS simulation for reflection coefficient (S_{11}). Blue curve shows S_{11} values for Cu TSV. Green curve is for Cu-W bimetal (overlapping in main figure with Cu TSV), Red is for W TSV. Silicon is used as an interposer material in the simulation.

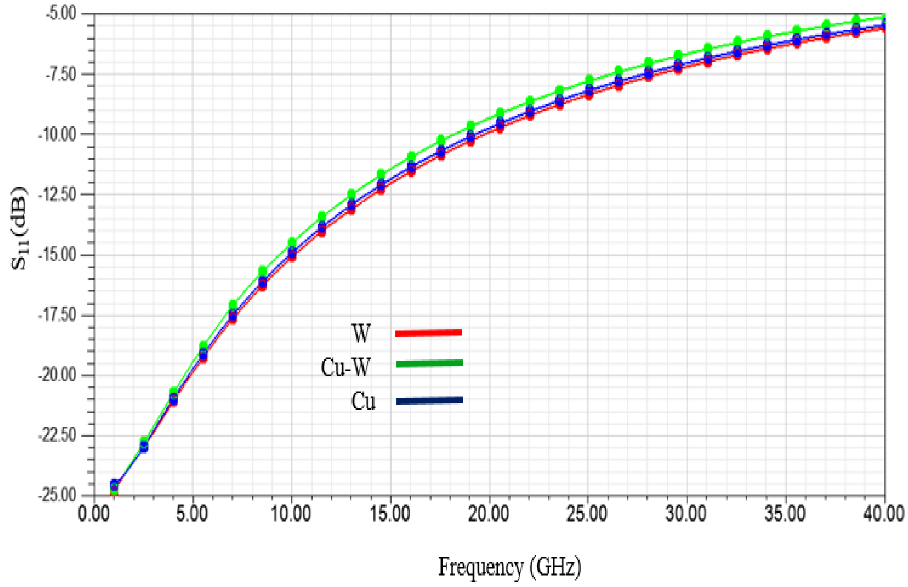


Figure 4.2.2: HFSS simulation for reflection coefficient (S_{11}) with Glass as an interposer (TGV). (Red curve is for W via, Green curve is for Cu-W via and Blue curve is for Cu via).

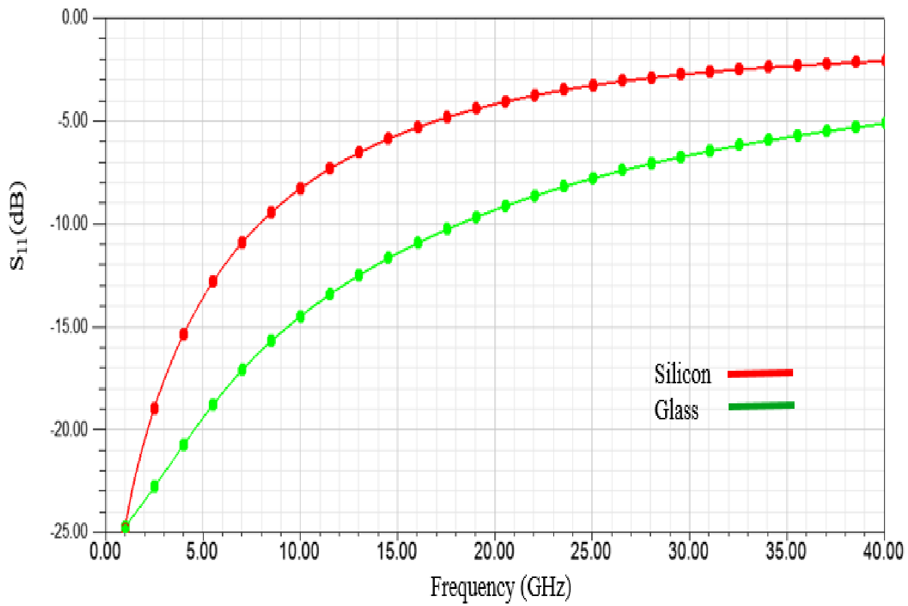


Figure 4.2.3: Comparison between the reflection coefficients (S11) of Cu-W bimetal vias when glass is used as an interposer (Green) and silicon is used as interposer (Red).

In Figure 4.2.3 we compare the return loss of a Cu-W TSV in both glass and silicon interposer. At 1GHz they showed exactly the same return loss but just after 1GHz two curves showed big deviation from one another. At 15GHz Cu-W TSV in glass interposer showed $S_{11} = -12dB$ whereas at the same frequency Cu-W TSV in silicon interposer showed $S_{11} = -5.5dB$. At 40GHz the difference between two losses minimizes compared to earlier frequencies but still the difference between them was significantly large ($\sim 3dB$). So S_{11} in glass interposer is lower than that of in silicon interposer in frequencies higher than 1GHz, so return loss of Cu-W via in silicon interposer is higher than glass interposer.

4.2.2 TSV Transmission Coefficient or Insertion Loss for Different Materials

Insertion loss measures how much the signal is attenuated between transmitter end and receiving end. In low frequency the insulator layer (SiO_2) leakage is the main reason for insertion loss whereas in high frequencies substrate leakage is more dominant. Insertion loss/Transmission coefficient (S_{21}) was measured for different combinations of interposer and via materials. Figure 4.2.4 depicts the transmission coefficients for Cu, W and Cu-W TSVs with silicon interposer. The Cu-W TSV had higher transmission coefficient ($S_{21} \approx -6.12dB$) at high frequency (40GHz), whereas W TSV had lower transmission coefficient ($S_{21} \approx -5.5dB$) at the same frequency. The Cu TSV had TC value in between them ($\sim -6dB$). So, the insertion loss is higher in Cu vias than in W vias. In Figure 4.2.5 the simulation result is shown when glass interposer was used instead of silicon to measure insertion loss for

W, Cu and Cu-W bimetal TSV and the simulation results indicate that like silicon interposer W TSV had lower insertion loss than Cu and Cu-W bimetal TSV.

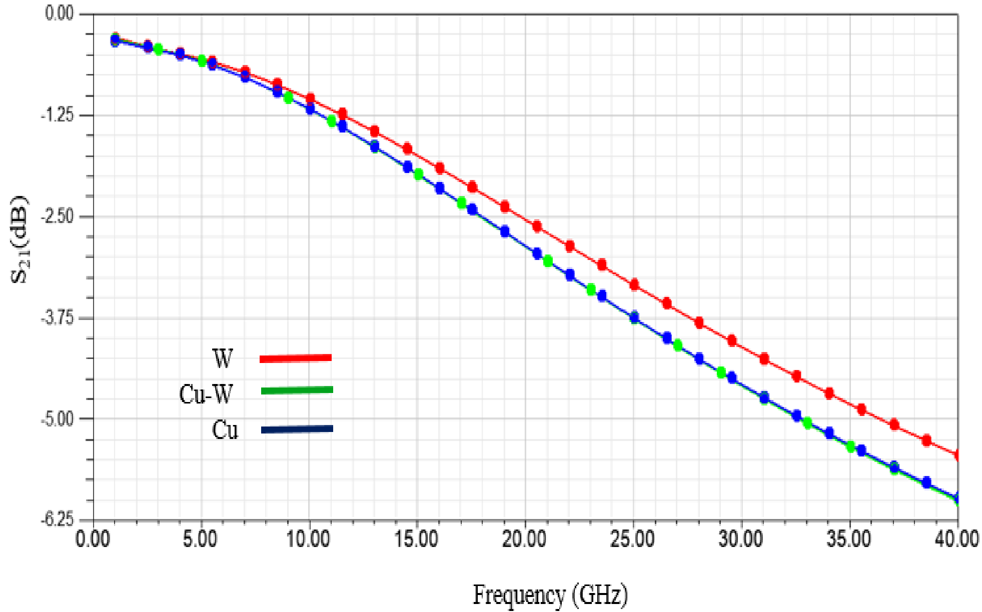


Figure 4.2.4: HFSS simulation for transmission coefficient (S21). Red curve shows S21 values for W TSV. Green is for Cu-W bimetal TSV and Blue is for Cu TSV. Silicon is used as an interposer material in the simulation.

Figure 4.2.6 shows the results for the transmission coefficient of Cu-W TSVs in both silicon and glass interposers. Before 5GHz frequency mark Cu-W TSV in glass has higher insertion loss (~-0.5dB at 1GHz) and Cu-W TSV in silicon interposer exhibits lower insertion loss (~-0.3dB at 1GHz). But after 5GHz frequency mark TC of Cu TSV in silicon increased more quickly than insertion loss of Cu TSV in glass. At 40GHz insertion loss of Cu TSV in silicon interposer reached as high as -6dB and in glass interposer the peak value is -2.4dB.

4.2.3 Near End and Far End Crosstalk

We measured near end crosstalk (NEXT) and far end crosstalk (FEXT) between two TSVs in various combinations. In Figure 4.2.7 and Figure 4.2.8 it was observed that the NEXT has the tendency to increase sharply with increasing frequency below 5GHz. But after 5GHz as the frequency increased the NEXT is decreased. Among all TSVs W TSV in silicon interposer has lowest and Cu TSV has highest crosstalk effect at low frequencies (<5GHz). But as frequency increases the cross talk in Cu TSV was lower than W TSV and Cu-W TSV has the lowest crosstalk. W TSV in glass interposer always has higher value of NEXT than Cu TSV (shown in Figure 4.2.8). Cu-W bimetal TSV shows promising results in the higher frequencies in glass interposer. It is observed from the simulation result that the near end cross talk effect is severe in silicon interposer than in glass interposer (Figure 4.2.9).

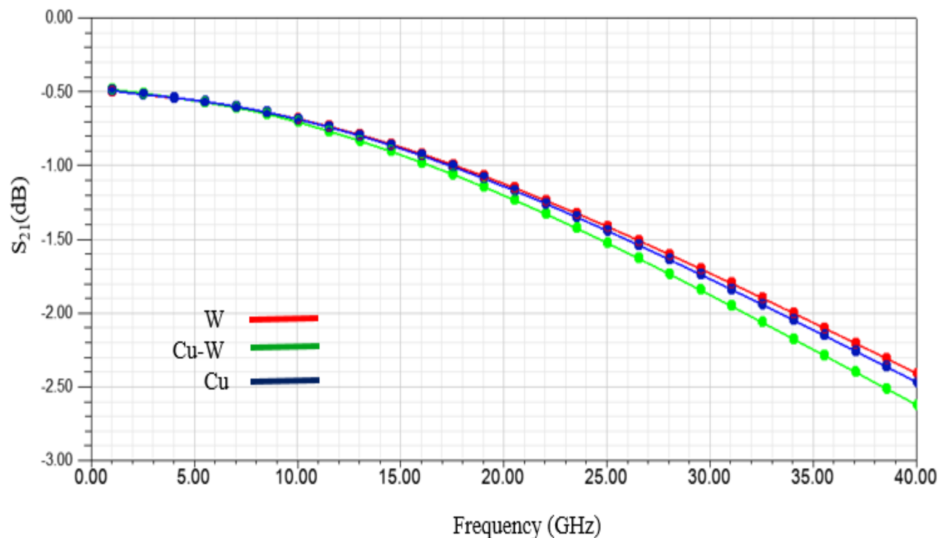


Figure 4.2.5: HFSS simulation for transmission coefficient (S21) with Glass as an interposer. (Red curve is for W TGV, Green curve is for Cu-W TGV and Blue curve is for W TGV).

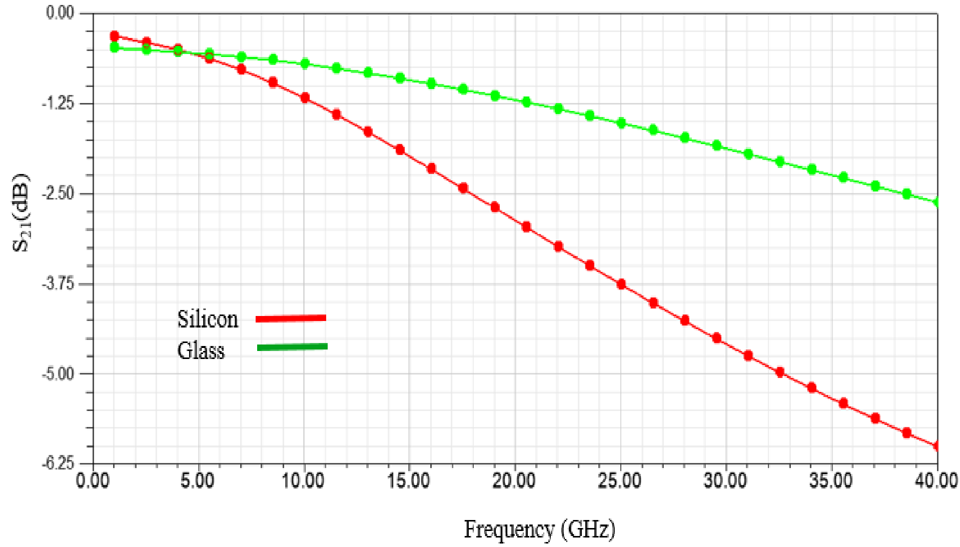


Figure 4.2.6: Comparison between the transmission coefficients (S21) of Cu-W vias when glass is used as an interposer (Green) and silicon is used as interposer (Red).

Cu TSV showed better performance in terms of far end cross talk in silicon interposer. It has slightly lower value in low frequency range (lower than W TSV and Cu-W TSV). In high frequencies it has much lower value than all other TSVs (see Figure 4.2.10). In glass interposer Cu TSV showed higher FEXT than W TSV but as the frequency increased the performance of the W TSV degraded compared to Cu TSV (Figure 4.2.11). The performance of Cu-W TSV in terms of far end crosstalk is lower than Cu and W TSVs. Figure 4.2.12 suggests that it is better to use glass interposer than silicon interposer to prevent far end cross talk as both high and low frequency values indicate improved performance for Cu TSV in glass interposer. Near 1GHz frequency FEXT in glass interposer is almost 4dB lower than silicon inter poser and at 40GHz it is almost 1.5dB.

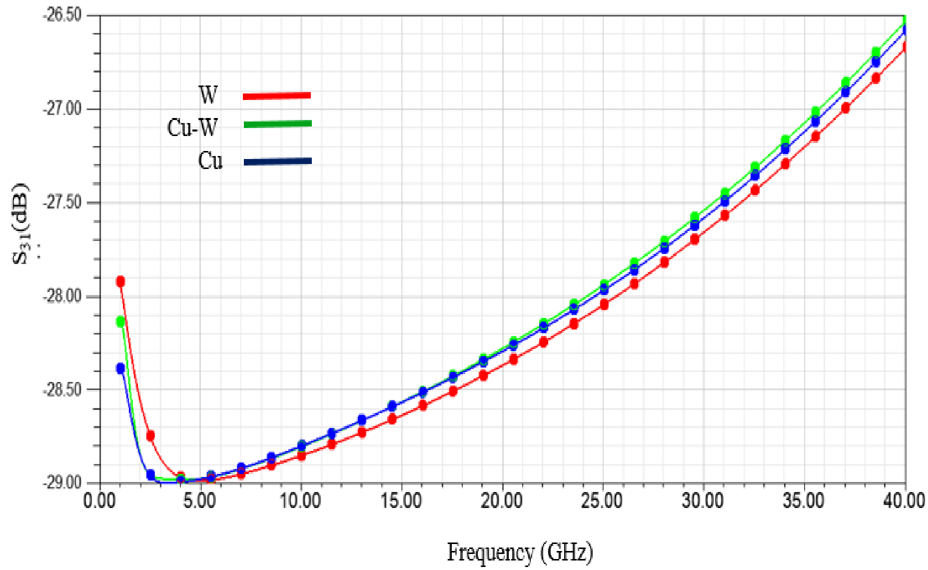


Figure 4.2.7: Near-end crosstalk (NEXT) simulation for different via cores in silicon interposer (TSVs). Red curve is for W TSV, Green curve is for Cu-W TSV and Blue curve is for Cu TSV.

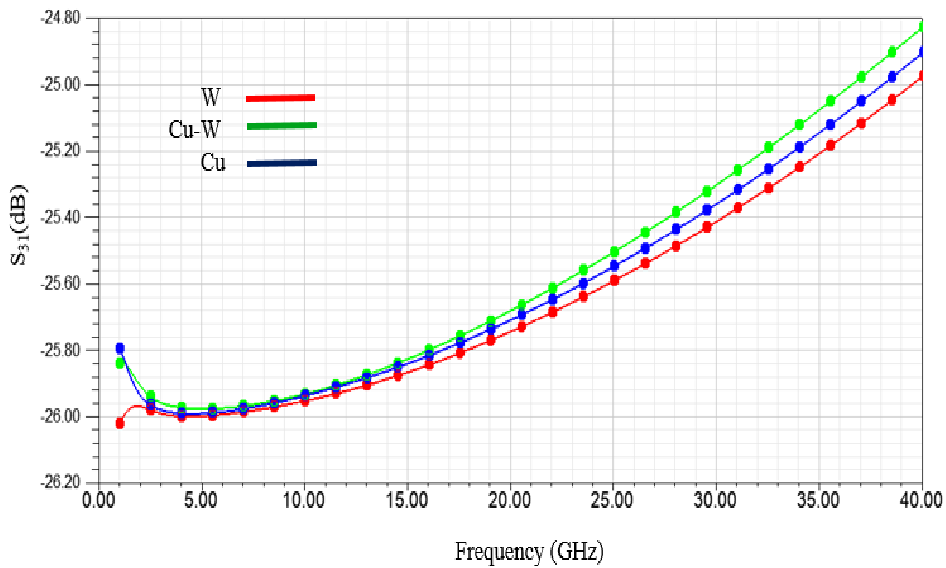


Figure 4.2.8: Near end crosstalk (NEXT) simulation for different vias in glass interposer (TGVs). Red curve is for W TGV, Green curve is for Cu-W TGV and Blue curve is for Cu TGV.

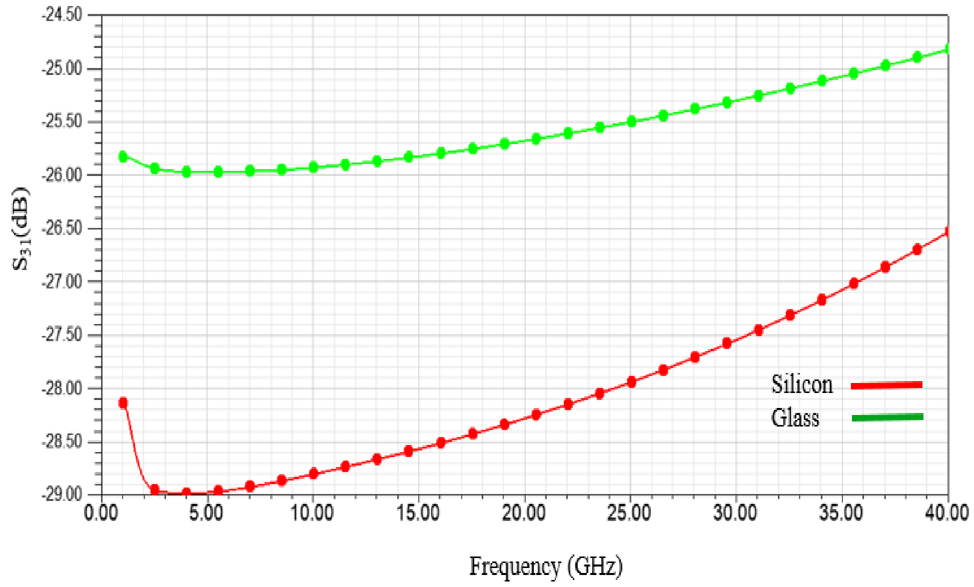


Figure 4.2.9: NEXT in Cu via with silicon (RED) and glass (GREEN) interposers.

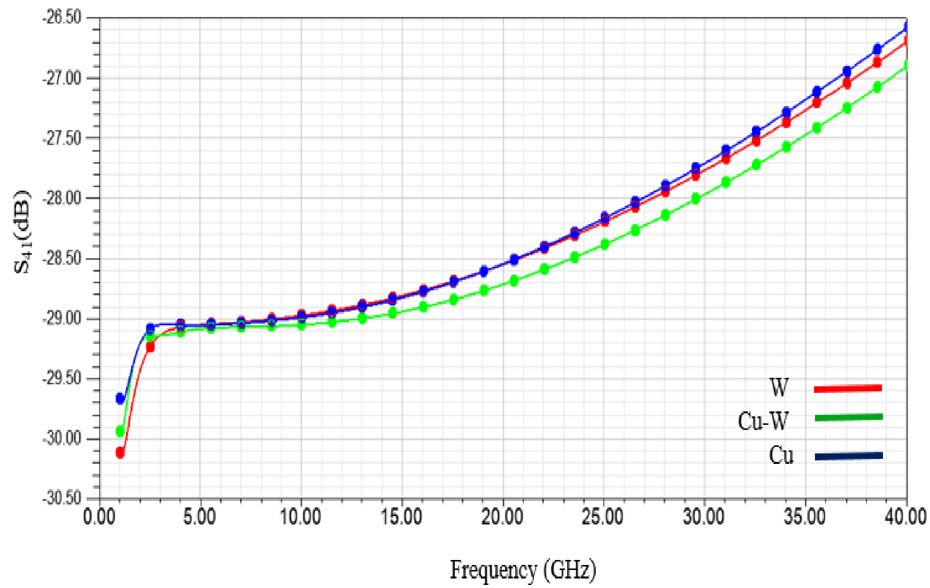


Figure 4.2.10: Far-end crosstalk (FEXT) simulation for different vias in silicon interposer. (Red curve is for W TSV, Green curve is for Cu-W TSV and Blue curve is for Cu TSV).

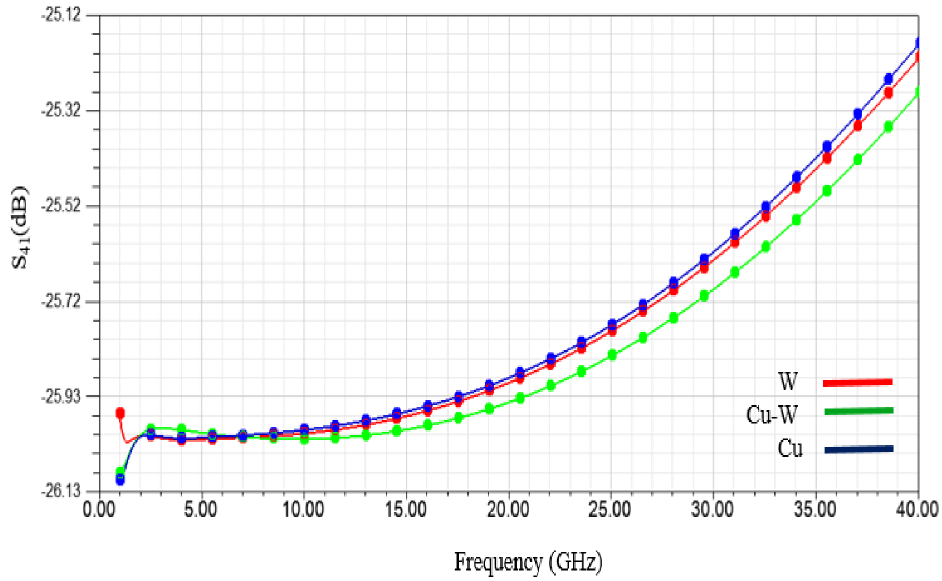


Figure 4.2.11: Far-end crosstalk (FEXT) simulation for different vias in glass interposer. (Red curve is for W TGV, Green curve is for Cu-W TGV and Blue curve is for Cu TGV).

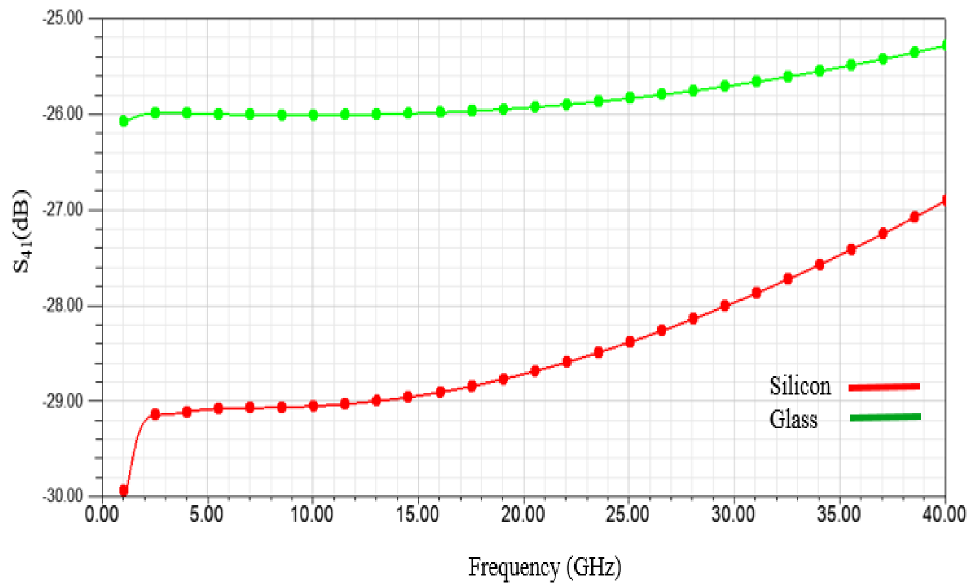


Figure 4.2.12: FEXT in Cu TSV with Silicon interposer (Red) and Glass interposer (Green).

4.2.4 Radius Variation

In this section we consider Cu TSV's performance for different dimensions of TSV. We change the diameter of TSV and add an additional bump to the structure. Figure 4.2.13 shows the model we used to measure the insertion loss and return loss of TSVs with different radius. Cu TSVs are used for both the Signal and GND TSVs.

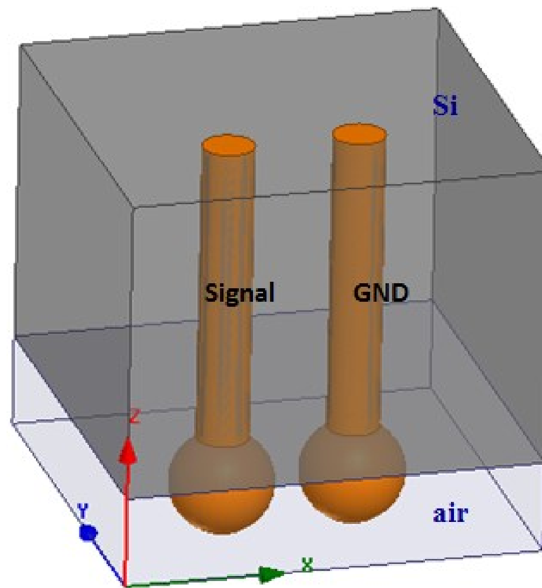


Figure 4.2.13: Basic HFSS model used to measure the performance of TSVs with different TSV diameter and relative spacing.

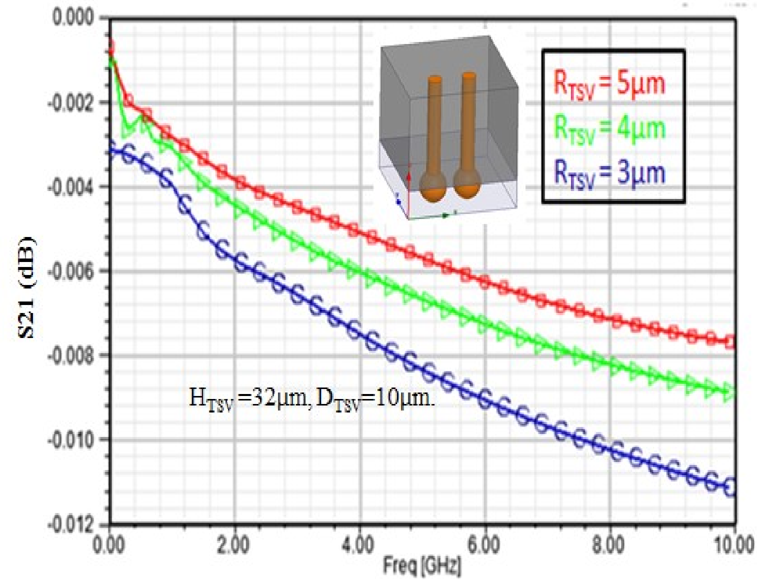


Figure 4.2.14: Transmission coefficient measurement of Cu TSV for three different radii.

The heights of the TSVs are kept constant at 32µm. The radius of the TSVs varies from 3µ to 5µm. It is found that the transmission coefficient drops faster if the TSV radius is decreased because the signal is getting less cross-sectional area in the TSVs as shown in Figure 4.2.14.

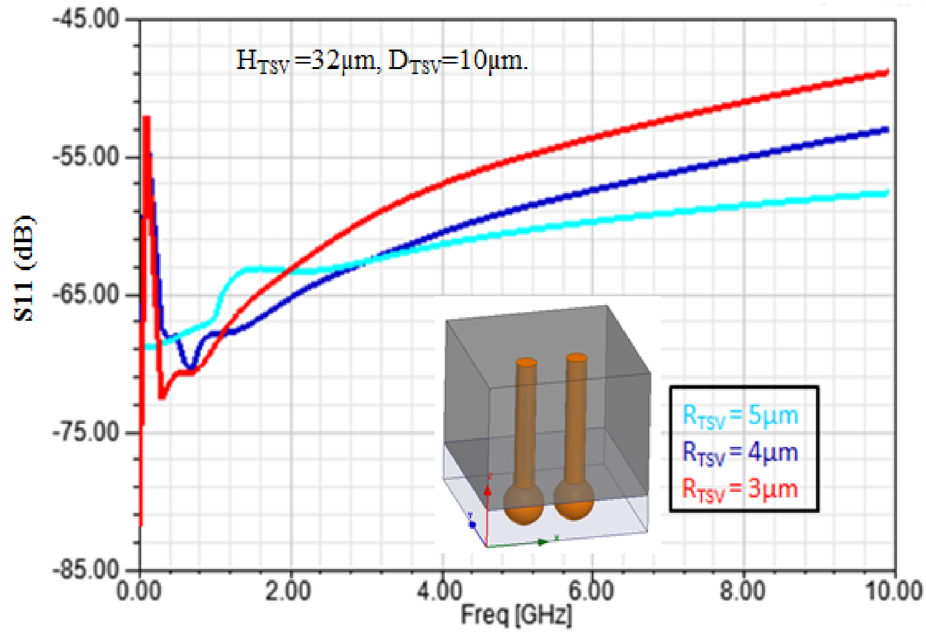


Figure 4.2.15: Return Loss measurement of Cu TSV for different radii.

At low frequency TSV with 5μm radius have higher return loss than TSVs with 4μm and 3μm radius but as the frequency increases, we have contrasting result with 5μm TSV has the lowest return loss and 3μm and 5μm TSVs has higher return loss.

4.2.5 Bump Dimension Variation

A bump is used to connect two TSVs or a TSV and pin. Bumps also help stabilize the 3D IC structure. Figure 4.2.16 shows the typical structure of a signal and ground bump.

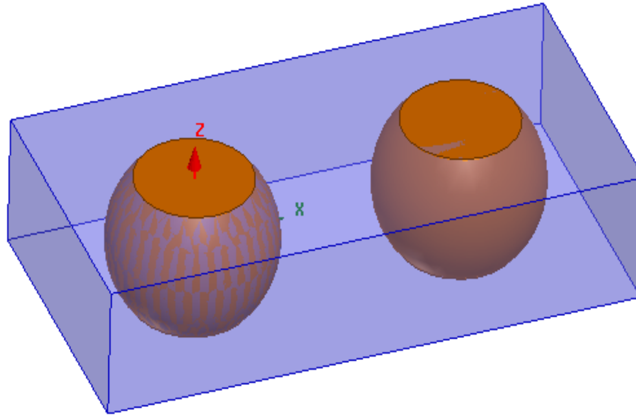


Figure 4.2.16: Typical signal and ground bump with Bump height of 18µm and radius of 12.5µm

It is observed from Figure 4.2.17 that the S_{21} decreases as the operating frequency increases. So, insertion loss increases with increasing frequency. The insertion loss increases faster when the bump diameter is lower (25µm) than when the bump diameter is larger (35µm and 30µm). This is because the larger cross-sectional area of the bumps results in higher current flow.

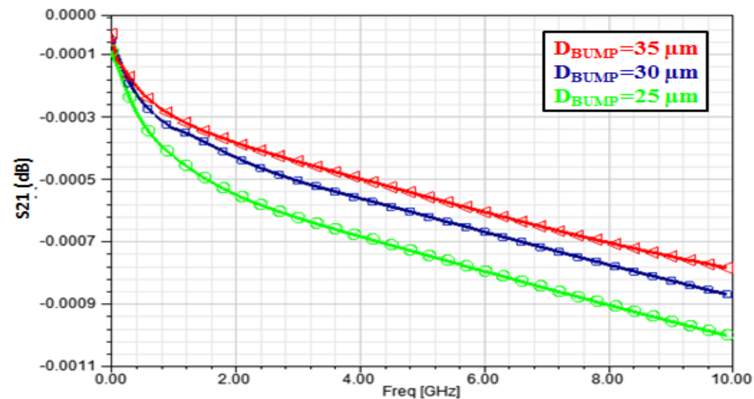


Figure 4.2.17: Transmission coefficient between bumps at different frequencies.

Figure 4.2.18 shows the comparison between the return losses of three bumps with different diameters. Return loss increases with increasing frequency. At lower frequency return loss in the cases of 25µm, 30µm and 35µm bump diameters shows the same increase rate but as frequency increases loss in 35µm bump more quickly than other two bumps. The 25µm and 30µm bumps show exactly the same results above 1GHz frequency.

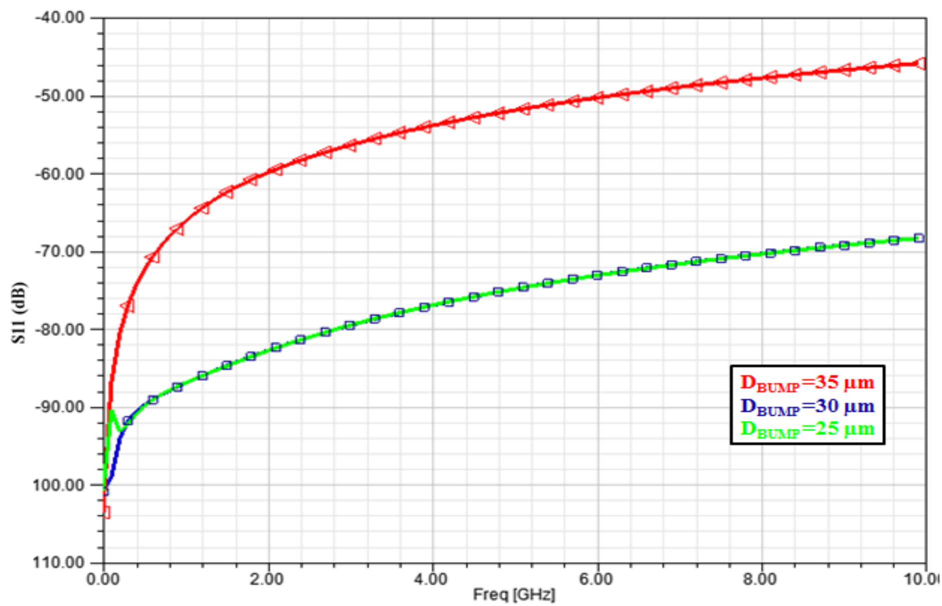


Figure 4.2.18: Return loss (S11) measured between two bumps for different bump diameters.

The transmission coefficient doesn't very too much with increasing or decreasing distance between two adjacent bumps. As shown in Figure 4.2.19 the distance between two bumps has increased 50% but the transmission coefficient is not increased significantly. But higher spacing between two bumps causes greater return loss (Figure 4.2.20)

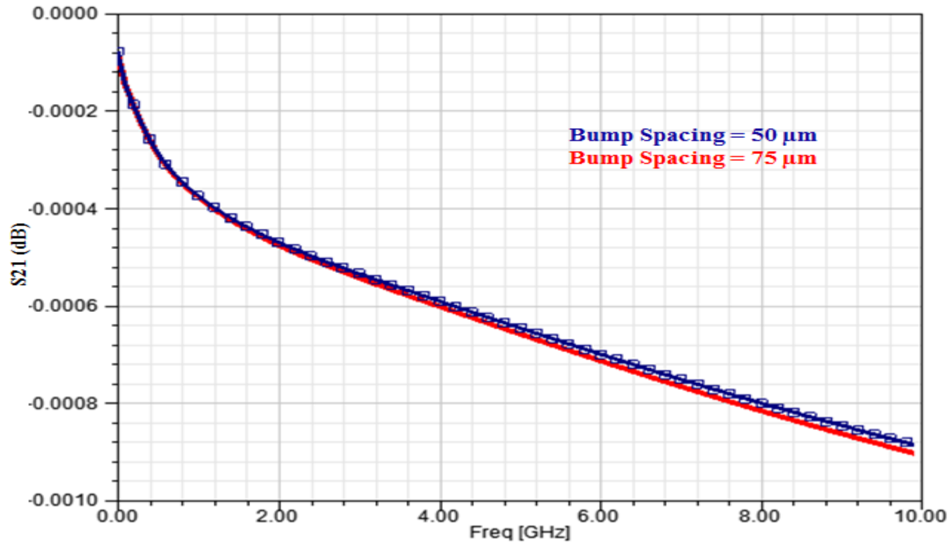


Figure 4.2.19: Transmission coefficient (S21) between two bumps when the relative spacing between them is 50µm (blue) and75 (red).

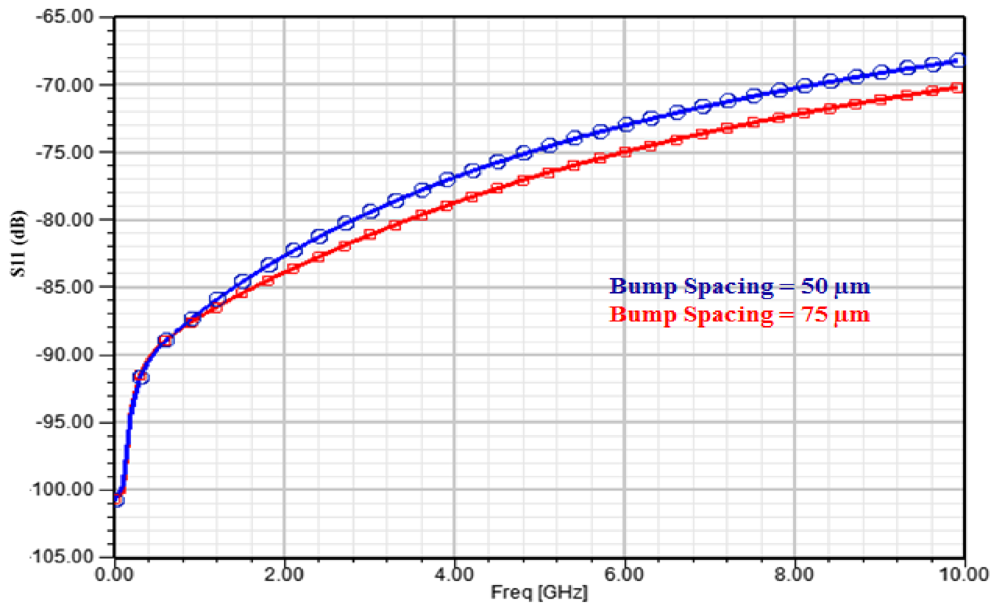


Figure 4.2.20: Return loss comparison between two bumps when they are placed 50µm and 75µm apart.

4.2.6 Effects of Multiple Layers of TSVs

The impact of stacking multiple layers of TSVs is shown in Figure 4.2.21 and Figure 4.2.22. We use Cu TSV with height of 60µm radius of 10µm and the distance between the signal TSV and ground TSV is 25µm for both single layer and multi layers of TSVs. The return loss decreases with increasing frequency, but the transmission coefficient is increased with increasing frequency.

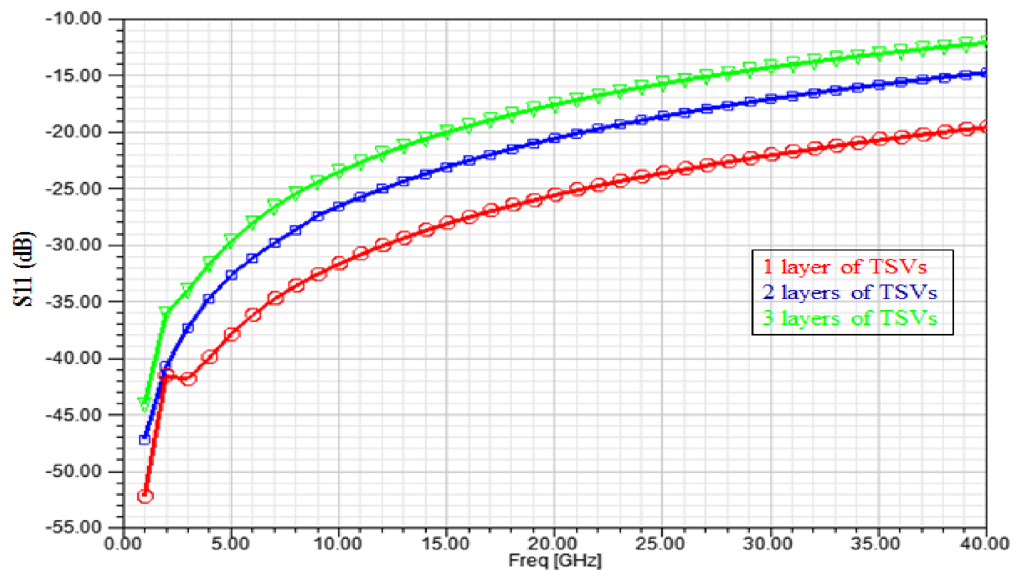


Figure 4.2.21: Return loss measurement for stacked TSV layers with diameter of the TSV is 20µm, height of the TSV is 60µm and pitch is 25µm.

The return loss in multi-layer TSV is higher than single layer TSVs in all frequency ranges. But the insertion loss remains almost same for single layer and multilayer TSVs for low frequency range but as the frequency is increasing insertion loss of multilayer TSVs increased rapidly compared to single layer TSV.

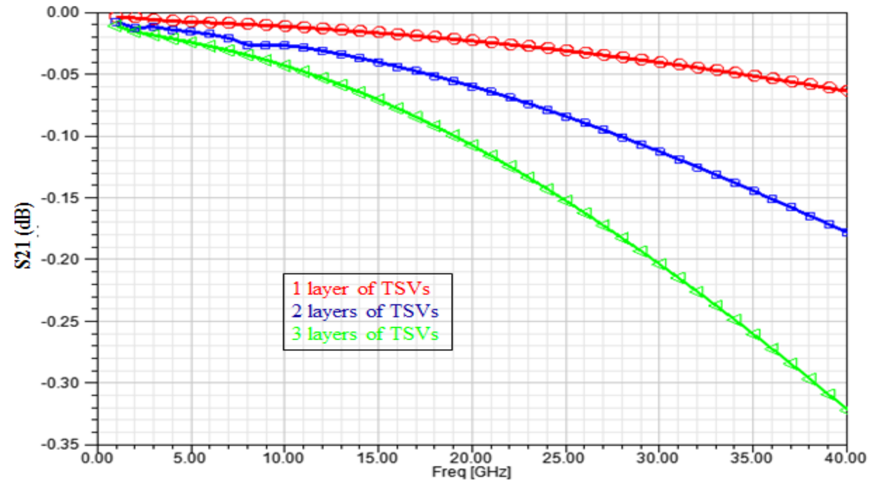


Figure 4.2.22: Comparison of transmission coefficient between TSVs with different layers.

4.3 **Summary**

Various performance parameters like return loss, transmission coefficient, NEXT and FEXT have been measured and compared for conventional TSV material like Cu and W, non-conventional material like Au and Cu-W bimetal. We have performed the same set of analysis for silicon and glass interposers. It is observed that TSVs in glass interposer demonstrate much better performance than in silicon interposer. Therefore, to reduce the crosstalk effect in 3D ICs it is better to use glass interposer. In high frequencies, TSV core made of W has shown better performance in case of insertion loss (transmission coefficient) and far end crosstalk (FEXT). The W based TSV also shows better performance in terms of near-end crosstalk (NEXT) when the operating frequency is low. In glass interposer the performance of Cu TSV is better. Therefore, W based TSV might be the better choice for signal TSV in moderately high frequency applications. The performance of Cu-W bimetal

TSV is not better than W via but it is very similar to Cu via. So, if Cu-W bimetal TSV is used it can handle both the thermal stress of Cu on silicon and the crosstalk effect. For better understanding of the Cu-W bimetal TSV an analytical model for the structure should be developed and the result obtained from the model should be compared to the simulation results for the validation of the model. It is also found from the analysis that the insertion loss depends on the TSV diameter and as the diameter increases the insertion loss decreases. The size of the bumps has its effect on the return loss and insertion loss. To reduce these losses bump size should be increased. Increasing the TSV layers caused higher return and insertion loss.

CHAPTER 5

IMPACTS OF DIFFERENT SHAPES OF THROUGH-SILICON-VIA CORE ON 3D IC PERFORMANCE

5.1 Introduction

As the demand for more functionality to be integrated into a single chip, different methodologies in 2D technology like transistor scaling and system-on-chip (SoC) are implemented. One of the main problems of SoC technology is placing digital, analog and RF circuits in the same die and in the same process node which is very difficult to achieve. An alternative approach is system in package (SiP) where different technology nodes can have different die mounted on a single substrate. But in all of these cases to connect the large number of transistors require long interconnect. This long interconnect length results in higher power consumption, signal delay and noise as parasitic components like resistance, capacitance and inductance is also increased with the increase of interconnect length. The delay introduced by the long interconnect is limiting factor of signal speed in current digital systems [31]. 3D integrated circuit (multiple dies connected vertically) with through-silicon via (TSV) is a potential solution to this long interconnect issue. 3D IC promises more functionality and better performance on a similar 2D chip area. It is a step towards 'more than Moore' era. The TSVs in a 3D IC are the vertical interconnects between the chips and they are responsible for power and signal delivery. As they are connected vertically and is much shorter in length compared to conventional 2D interconnect length. So, the signal delay

and the power consumption are much lower compared to existing 2D technology [32], [39]. The cost of integration is also less in 3D TSV technology [33]. Like 2D design, in 3D IC technology the integration density is increasing day by day so a large number of TSVs should be placed in compact fashion to meet the increased functionality requirement [34]. Many TSVs placed close to each other result in higher crosstalk and other switching noises. Here we investigate different shapes of TSV for example rectangular, octagonal and compare the result with more conventional circular TSV to find the best possible shape and dimension for lower loss. As the core material of the TSV we use Cu and as an interposer material we use Si. We also investigate the effect of an insulating layer outside the main TSV core material.

5.2 Simulation Setup

Figure 4.1.2 shows the primary simulation setup of TSVs for measuring different losses relative to TSV. The distance between the signal TSV and the ground TSV (pitch) is 10 µm. The diameter of the core of the TSV is 6 µm and the diameter of the SiO_2 insulating layer is 7 µm. The height of the TSVs used in simulation is 32 µm. Silicon is used as an interposer material and the length and width of the interposer is 200 µm. For simulation, the structure is surrounded by air. Figure 5.2.1 shows the different shapes of TSV used for measuring the losses.

Conventional circular TSV is used to benchmark the performance of other TSVs like rectangular, octagonal, hexadecagonal etc. We tried our best to maintain the dimensions of

the polygonal TSVs and circular TSV as similar as possible. For all the TSVs circular shaped SiO_2 insulating layer is used except one particular case where we simulate the performance of an octagonal TSV without the insulating layer. Table 3 summarized the different parameters of TSV and other materials used for simulation. Ansoft HFSS 3D field solver software has been used to carry out the simulation.

The height of the TSV is $32\mu m$ with diameter of $6\mu m$. The diameter of the insulating SiO2 layer is $7\mu m$ having thickness of $0.5\mu m$. The distance between the signal TSV and the ground TSV is $10\mu m$ (pitch).

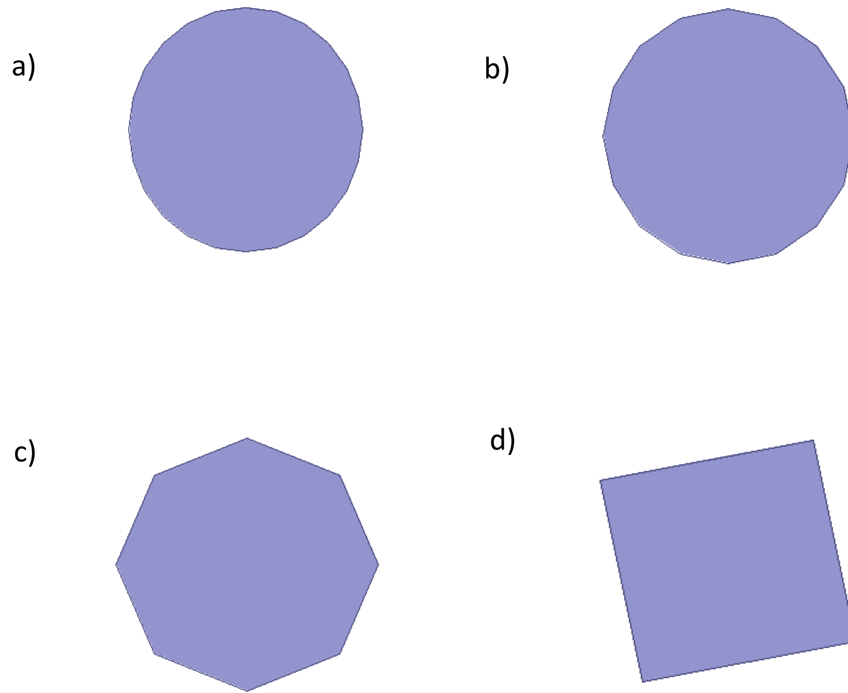


Figure 5.2.1: Different shapes of TSVs used for simulation. a. circular TSV b. Hexadecagonal TSV c. Octagonal TSV d. Rectangular TSV

Table 3

TSV parameters and their values

Geometrical parameters	**Typical value**
Radius of TSV (Circular)	3µm
Radius of SiO2 layer	3.5µm
SiO2 thickness	0.5µm

Height of the TSV	32μm
Pitch	10μm
Number of TSV used	2
Number of edges for non-circular TSV	4/8/16
Relative permittivity (Cu)	1
Relative permittivity (W)	1
Relative permittivity (Si)	11.9
Relative permittivity (SiO2)	4
Bulk Conductivity (Cu)	58×106S/m
Bulk Conductivity (Si)	0
Bulk Conductivity (SiO2)	0

5.3 Result and Analysis

5.3.1 Measurement of Return Loss for Different Shapes of TSVs

Return loss is the measurement of how effectively the power is delivered through a transmission line [41]. When the Pr/Pi ratio (Pi is the power of the incident signal and Pr is power of the reflected signal) decreases the return loss decreases which is reflected by the large negative number in the decibel scale. Figure. 5.3.1 shows the reflection coefficient or return loss (S_{11}) for different shapes of TSVs in silicon interposer. It is observed that at lower

frequencies (<1GHz) the rectangular TSV shows the best performance having -62dB (lower the better) return loss whereas octagonal TSV without an insulating layer has the highest loss of -55dB. This is because in the absence of an insulating layer signal may leak to the surrounding material. In low frequency the octagonal and hexadecagonal TSVs have almost the same loss. Return loss of circular TSV is higher than rectangular TSV but lower than other shapes of TSVs. At high frequency we observe the same trend, the rectangular TSV has the lowest return loss compared to other TSVs. The reason for lower loss in rectangular TSV is the cross-sectional area of the insulating layer for rectangular TSV is larger when compared to the other shapes of TSV.

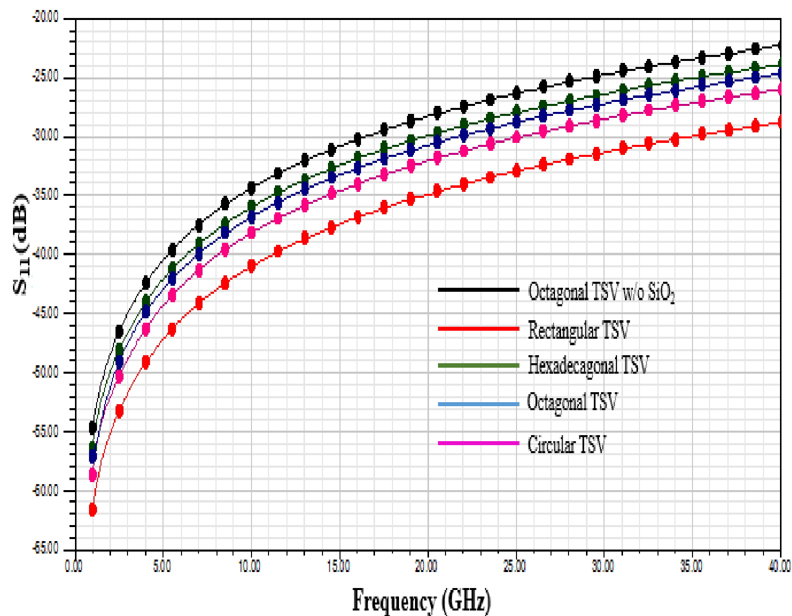


Figure. 5.3.1: HFSS simulation for reflection coefficient (S11). Pink curve shows S11 values for circular TSV. Green curve is for hexadecagonal TSV, Red is for rectangular TSV, Blue curve is for octagonal TSV and Black curve is for octagonal TSV without the insulating layer.

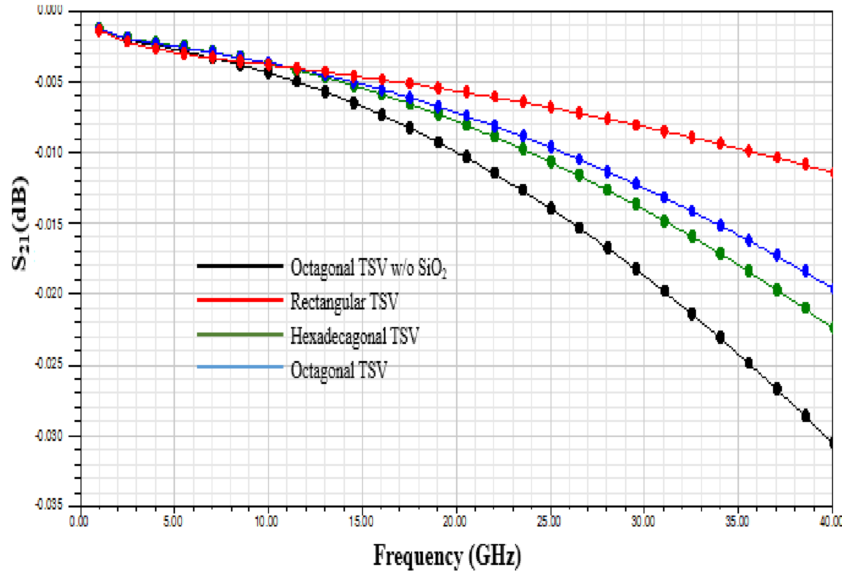


Figure 5.3.2: HFSS simulation for insertion loss (S_{21}) for different shapes of TSVs. Green curve shows S21 values for hexadecagonal TSV, Red is for rectangular TSV, Blue curve is for octagonal TSV and Black curve is for octagonal TSV without the insulating layer.

5.3.2 Measurement of Transmission Coefficient for Different Shapes of TSVs

Insertion loss is the measurement of how much the signal is attenuated from the transmitting end to the receiving end. Figure 5.3.2 shows the insertion loss or transmission coefficient (S_{21}) for different shapes of TSVs. At frequencies below 1GHz the insertion loss is almost same for all shapes of TSVs. But as the frequency increases insertion loss of the octagonal TSV without the insulating layer increases more rapidly compared to other TSVs having an insertion loss of $-0.031dB$ (higher the better). Here also rectangular TSV shows the best performance having insertion loss of $-0.012dB$. The insertion loss of hexadecagonal TSV is higher compared to octagonal TSV with the insulating layer. In Figure 5.3.3 we

compared the insertion loss of the circular TSV with other polygonal TSVs. The loss of circular TSV is excessively higher than other TSVs with minimum value of -0.50*dB* and maximum value of -2.50*dB* at 40GHz.

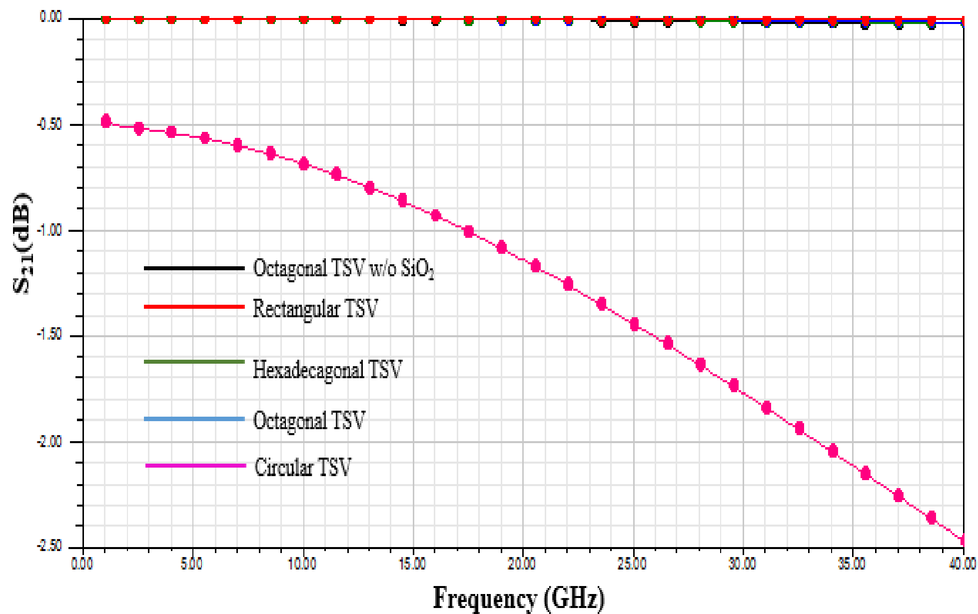
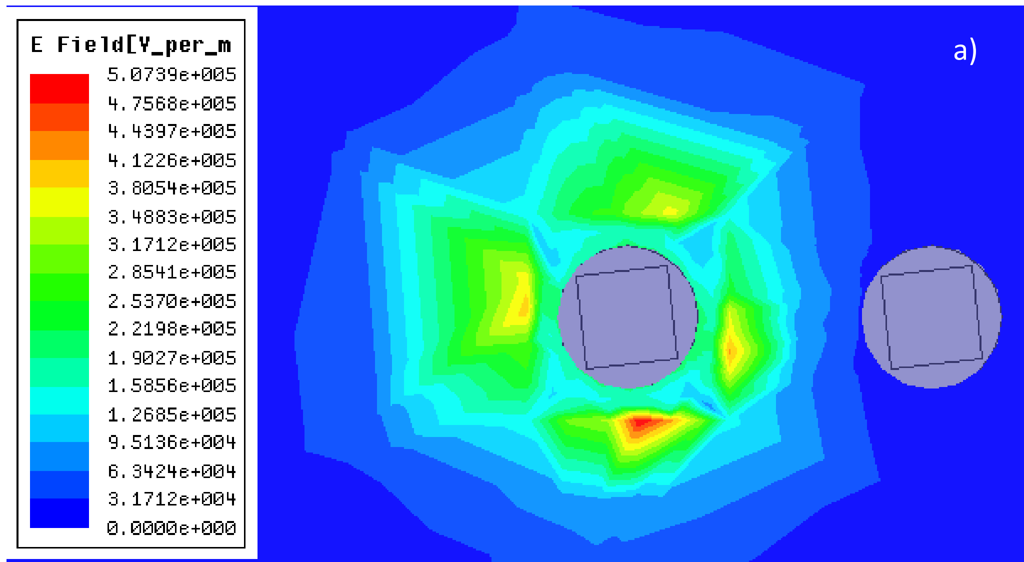


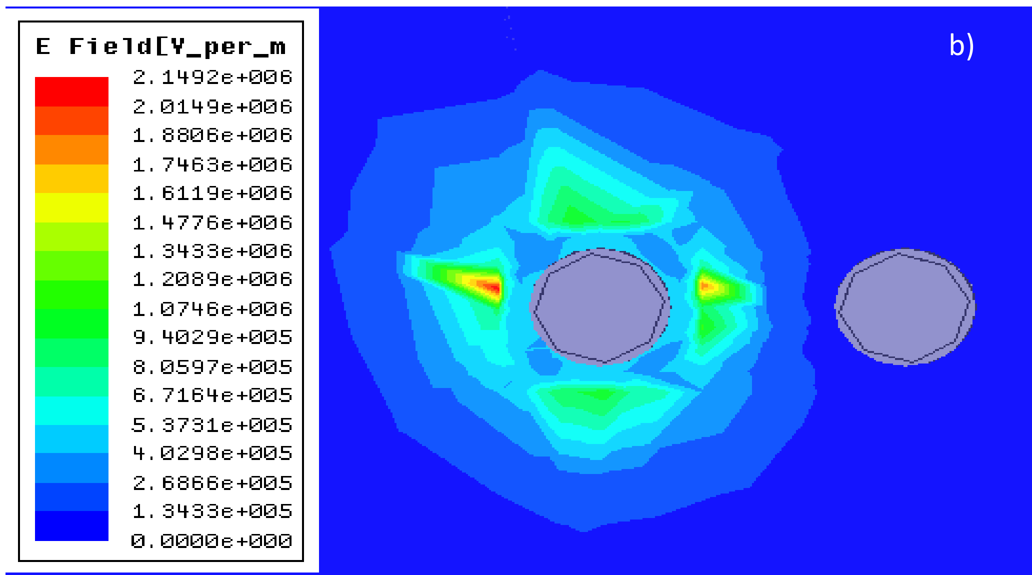
Figure 5.3.3: Comparison between the insertion loss (S21) of circular TSV (pink) with other polygonal TSVs (Overlapping)

5.3.3 E-Field and H-Field Distribution

Mutual capacitance and inductance between two closely placed via is the reason behind crosstalk. Mutual capacitance couple energy between two vias by means of electric field whereas mutual inductance couple energy via magnetic field. When the magnetic flux lines initiates from one via intersect another via a current induced into the victim via and hence create a voltage noise. In the same way when the electric field line intersect a via, that also produce a voltage noise [42]. And Figure 5.3.4 and Figure 5.3.5 shows the E-field and

H-field distribution of different TSVs. From the electric field distribution it is observed that the octagonal TSV is less affected. As mutual capacitance between two adjacent TSVs are responsible for the electric filed distribution so the octagonal shaped TSV helps reducing the mutual capacitance between TSVs.

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2.0149e+006
1.8806e+006
1.7463e+006
1.6119e+006
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1.3433e+006
1.2089e+006
1.0746e+006
9.4029e+005
8.0597e+005
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2.6866e+005
1.3433e+005
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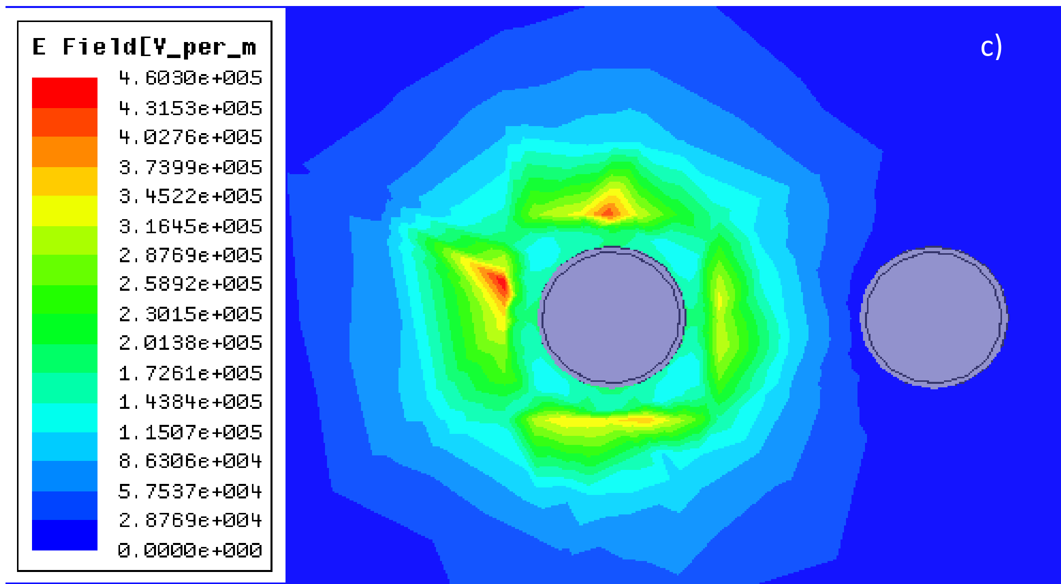
b)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2.3015e+005
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c)

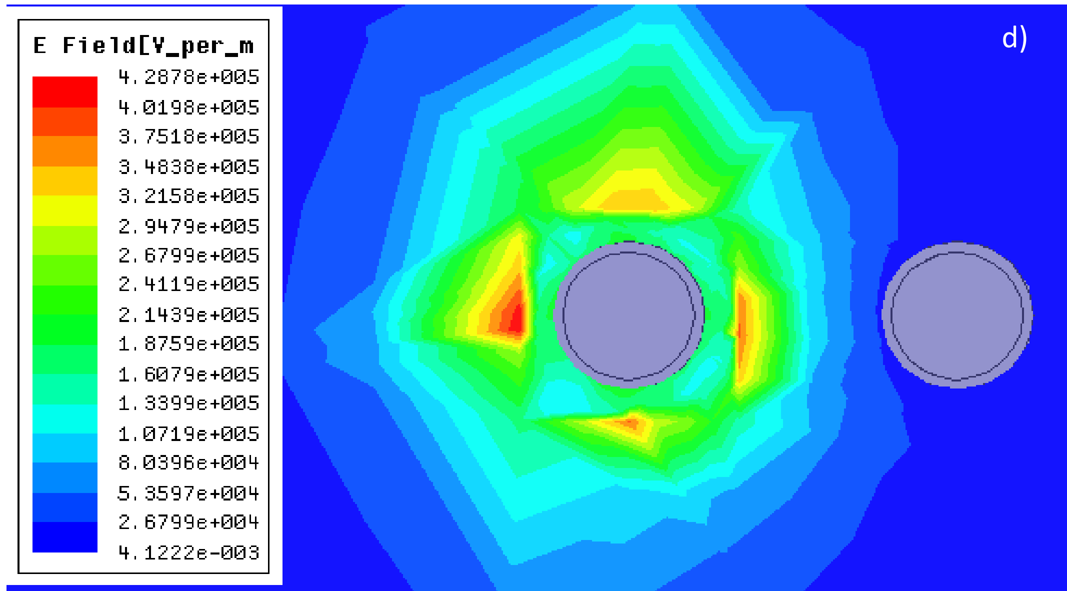
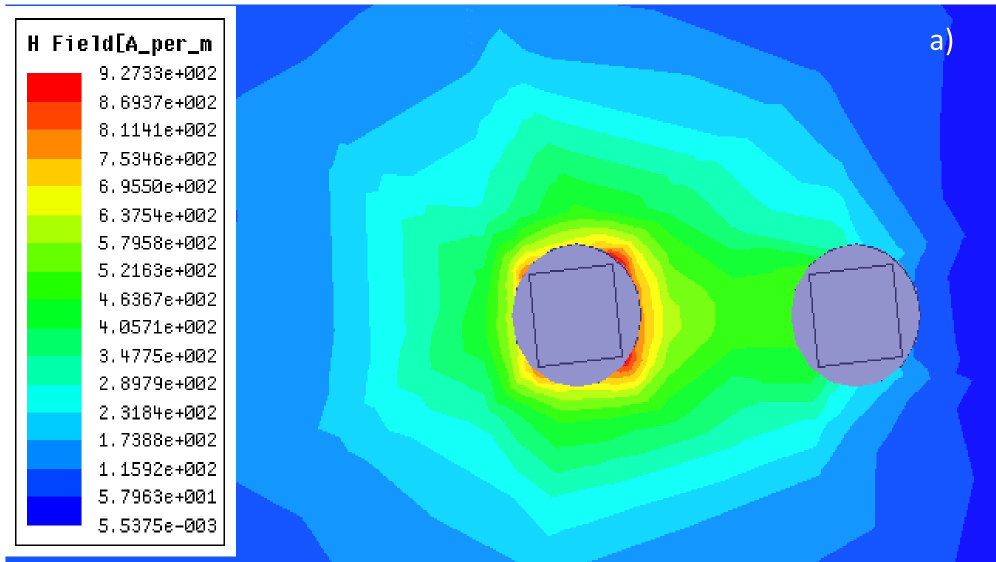


Figure 5.3.4: HFSS simulation of E-field distribution of a. rectangular, b. octagonal, c. hexadecagonal and d. circular TSVs

From the H-field distribution it is observed that the rectangular TSV is less affected. As the side of the polygon increases the coupling of magnetic field between two TSVs increases. The circular TSV shows the maximum H-field coupling. From the simulation result it is obvious that the mutual inductance between the TSVs is higher when the segments of polygon increases or even in circular TSV.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5.2163e+002
4.6367e+002
4.0571e+002
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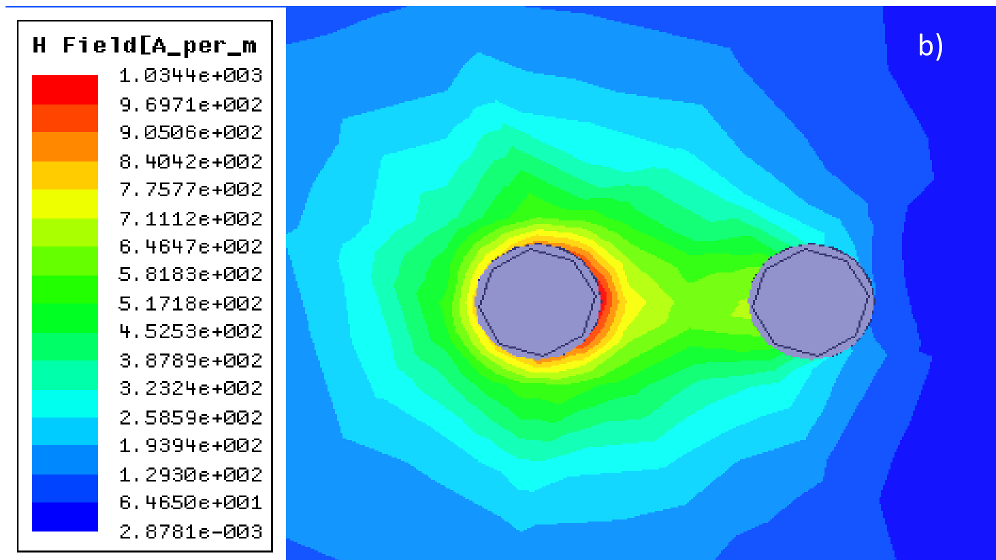
a)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5.1718e+002
4.5253e+002
3.8789e+002
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b)

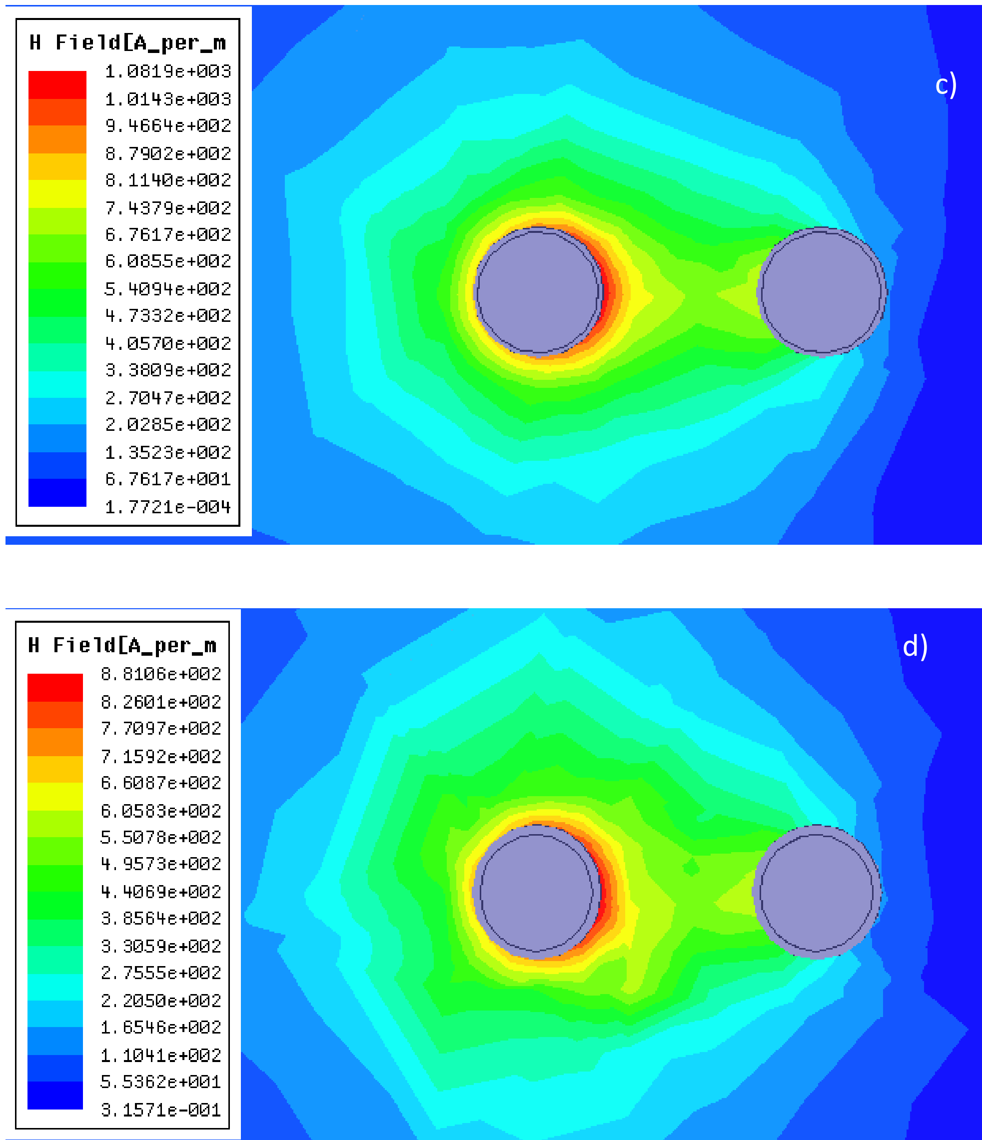


Figure 5.3.5: HFSS simulation of H-field distribution of a. rectangular, b. octagonal, c. hexadecagonal and d. circular TSVs.

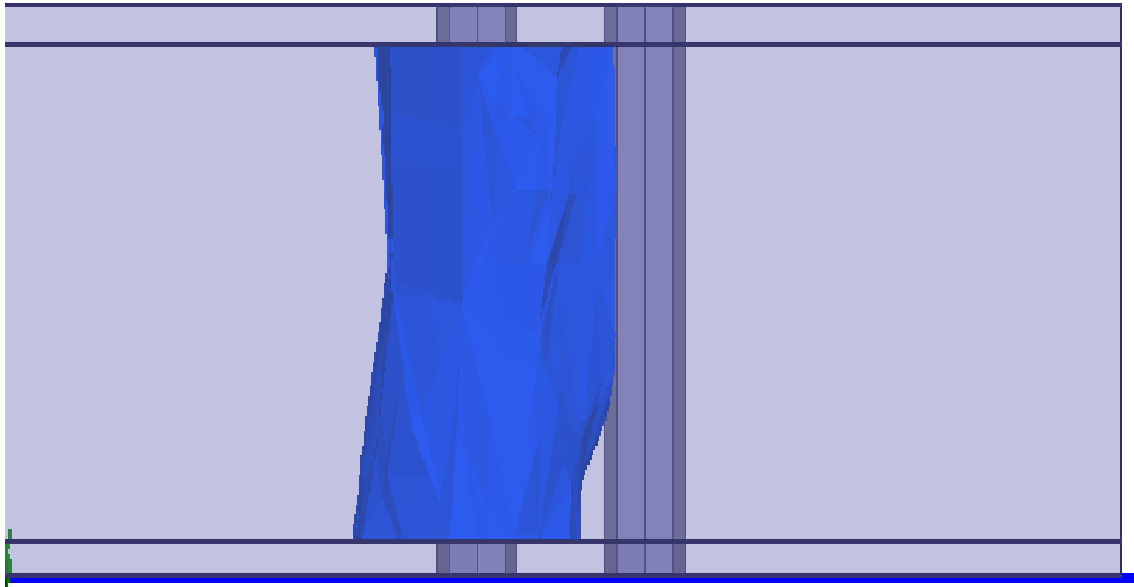


Figure 5.3.6: Side view of electric field distribution of an octagonal TSV when no insulating layer is used.

Figure 5.3.6 shows the effects of not having an insulating layer outside the TSV. Here it is observed that the electric field coupling between the signal TSV and ground TSV is more prominent than when a TSV has an insulating layer. The thickness of the insulating layer is also effects on the behavior of E-field and H-field. As the thickness of the insulating layer decreases the capacitance increases as a result the probability of coupling of electric field between two TSVs also increases.

5.4 Summary

Various performance parameters like return loss, transmission coefficient, mutual electric and magnetic field coupling have been measured and compared for conventional circular TSV and different polygonal TSVs. From the simulation results it is observed that the rectangular TSV has superior performance in terms of return loss, insertion loss and H-field coupling. Octagonal TSV shows good results when measuring the E-field coupling. As the segments of the polygon increases the performance degrades. For optimal performance rectangular TSV can be used if the fabrication process supports. Having an insulating layer surrounding the core also play an important role on the TSV performance. For better understanding of the effect of TSV and insulating layer shapes we need an accurate capacitive and inductive model.

CHAPTER 6

ACCURATE ELECTRICAL MODELING OF CU-FILLED THROUGH-SILICON VIA (TSV)

6.1 Introduction

The necessity of integrating more functionality within the same IC footprint as before in the state-of-the-art electronics pushes silicon scaling to its limit. Industries are embracing new design methodologies like system-on-chip (SoC) in which predesigned blocks obtained from the third parties or internal sources are combined in a single chip [43]. The challenge of the SoC technology is placing digital, analog and RF circuits in the same die and in the same process node, which is very difficult to achieve. A different design approach is a system in package (SiP), where different technology nodes have different die and all are mounted on a single package substrate. However, all of these design methodologies are 2D in nature, because the semiconductor devices are placed in a single-layer substrate. In 2D integrated circuits, connecting a large number of transistors require long interconnects, which result in higher power consumption, signal delay, and noise because of the parasitic components like resistance, capacitance, and inductance increase significantly with the increase of the interconnect length. The delay introduced by the long interconnect lines is the main limiting factor of the current digital systems [44]. The 3D integrated circuit (IC) with through-silicon-via (TSV) can resolve the problems that arise due to the long interconnect length. 3D integration is the stacking of multiple dies or chips on top of each other [45]. On the same

footprint of a 2D IC, 3D IC can deliver more functionality and better performance because of their reduced interconnect length, heterogeneous integration capability and higher packing density. Monolithic 3D IC and stacked 3D IC are two main categories of 3D IC technology. In monolithic 3D IC, different active layers are fabricated sequentially whereas in stacked 3D IC the layers are fabricated separately and then connected vertically together using various bonding technology. A typical 3D IC consists of BGA (ball grid array) to connect the IC with the power line, package substrate, C4 bumps, interposer to route the power and signal vias between C4 bumps and the micro bumps, and micro bumps (usually SnAg solder) that are used to make connection between two dies or between a die and a substrate. In the interposer, it is possible to integrate multiple dies. The TSVs in the 3D IC are the vertical interconnects between the chips and are responsible for power and signal delivery across the dies. TSVs consist of metal conductors (commonly copper) insulated from silicon commonly using a thin dielectric liner as shown in Figure 6.2.1. The 3D integration reduces the interconnect length compared to the 2D ICs. Shorter interconnect of the 3D IC leads to lower power consumption and signal delay [46]- [47]. As a result, 3D IC with TSV has a higher potential to deliver better performance. The cost of integration is also less in 3D TSV technology [48]. But the large sizes of the TSVs compared to the conventional on-chip interconnect lines lead to higher parasitic capacitance, resistance, and inductance. These parasitic components introduce new sources of coupling, which in turn causes coupling noises leading to severe signal integrity issues. Therefore, it is very important to estimate these parasitic components

quickly at the early stages of the design cycle to have some insight about the anticipated performance of the 3D IC. Also for an applicable and practical model of the TSV, the TSV channel that includes not only the TSVs, but also the bumps and the landing/bond pads has to be modeled and should be analyzed. The bump provides a joint between the stacked chips, and the landing pads provide a horizontal interconnection to the TSVs and the bumps. When designing the I/O channel with the TSVs in 3-D IC, the bumps are essential components that should be considered with the TSVs. Therefore, modeling and analysis of a TSV with the bump is important for advanced 3-D IC design. Here, we present an analytical modeling approach to estimate the capacitance, resistance, and inductance of the TSV in 3D IC.

6.2 Modeling of TSV Capacitance

Capacitances (C_{ox}) are formed between pairs of adjacent TSVs and bumps primarily in the 'liner' layer (dielectric layer) that surrounds the Cu-filled TSV and separates the TSV from the conductive silicon. In addition, there is another capacitance present in the conductive silicon substrate (C_x). Also a capacitance is present between two bumps separated by the substrate. As the TSVs are primarily cylindrical, we can use Gauss's law to formulate the capacitance equation. Using Gauss's law, for a cylindrical structure shown in Figure 6.2.2, the relation between charge and electric field can be stated as in (1).

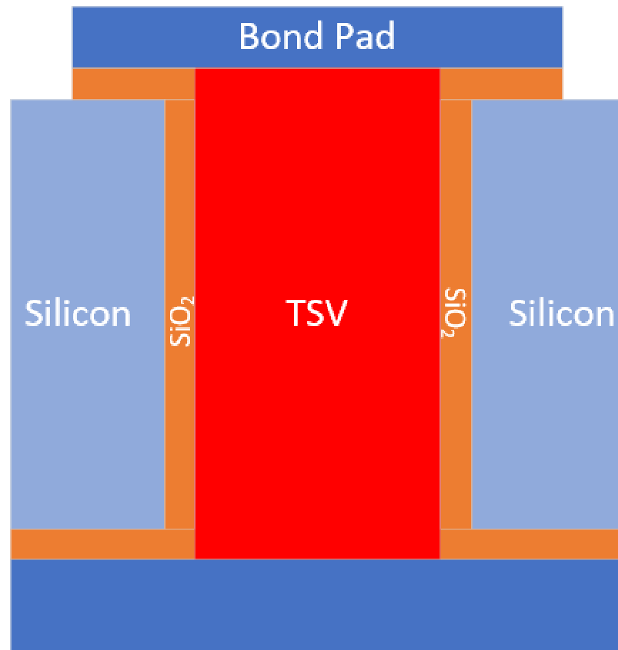


Figure 6.2.1: Through-Silicon Via (TSV) structure with the core (copper pathway), surrounding dielectric layer and landing pads.

$$\oint \vec{E}.d\vec{A} = EA = \frac{Q/_L}{\varepsilon_0} \tag{1}$$

$$E = \frac{Q/_L}{2\pi\varepsilon_0 r}, a < r < b \tag{2}$$

The potential difference is given by (3).

$$\Delta V = V_a - V_b = \int_a^b E_r dr = \frac{Q/_L}{2\pi\varepsilon_0}\int_a^b \frac{dr}{r} = \frac{Q/_L}{2\pi\varepsilon_0}\ln\left(\frac{b}{a}\right) \tag{3}$$

And the capacitance can be expressed as in Eq. (4).

$$C = \frac{Q}{\Delta V} = \frac{2\pi\varepsilon_0 L}{\ln\left(\frac{b}{a}\right)} \tag{4}$$

We use Eq. (4) as our basis to formulate the capacitance between two cylindrical line-segments as shown in Figure 6.2.3. The corresponding capacitance formulae are shown in Eq. (5) and Eq. (6), where x is the distance between the center of two cylinders, R_x is the radius of the cylinders, t_{ox} is the thickness of the insulation layer, T is the number of adjacent cylinders including the center cylinder [49].

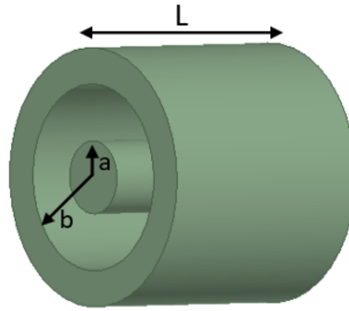


Figure 6.2.2: A cylindrical capacitor

$$C_{ox} = \frac{1}{T}\frac{2\pi\varepsilon_{ox}L_x}{ln\frac{R_x + t_{ox}}{R_x}} \tag{5}$$

$$C_x = \frac{\pi\varepsilon_x}{ln\left[\frac{x}{2R_x} + \sqrt{\left(\frac{x}{2R_x}\right)^2 - 1}\right]}L_x \tag{6}$$

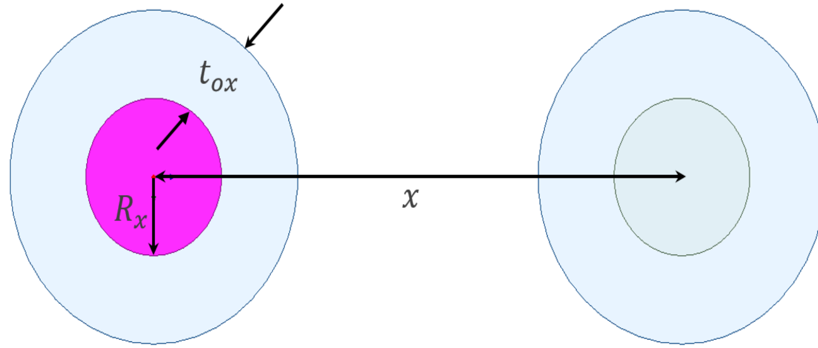


Figure 6.2.3: Two cylindrical segments at a distance x, with a radius of the cylinder R_x and thickness of the insulating layer t_{ox}. This diagram is used to derive cylindrical capacitive formulae.

6.2.1 The Capacitive Model of The Bumps

In 3D-IC technology, the bumps or the micro-bumps are not a full sphere but a spherical segment, where the top or the bottom or both the top and bottom portions are flattened. Also, as the spherical bumps are not fully cylindrical, the cylindrical capacitive formulas cannot predict the capacitance between two bumps accurately. So, we approximate a spherical segment as a group of small cylindrical segments as shown in Figure 6.2.4 so that we can use the capacitive formulas to each of the small cylindrical segments. From Figure 6.2.4 it is clear that with each subsequent cylinder on the top or bottom of the middle one, the radius is decreasing by the amount of Δr with a thickness Δl. If the value of Δr is small, the structure will replicate the shape of a sphere.

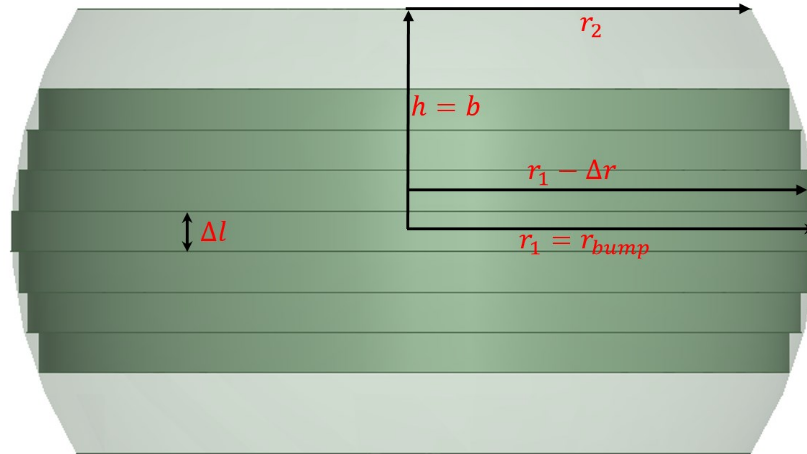


Figure 6.2.4: A spherical segment is divided into small cylindrical segments, where the radius of each segment is Δr higher or lower than the previous one.

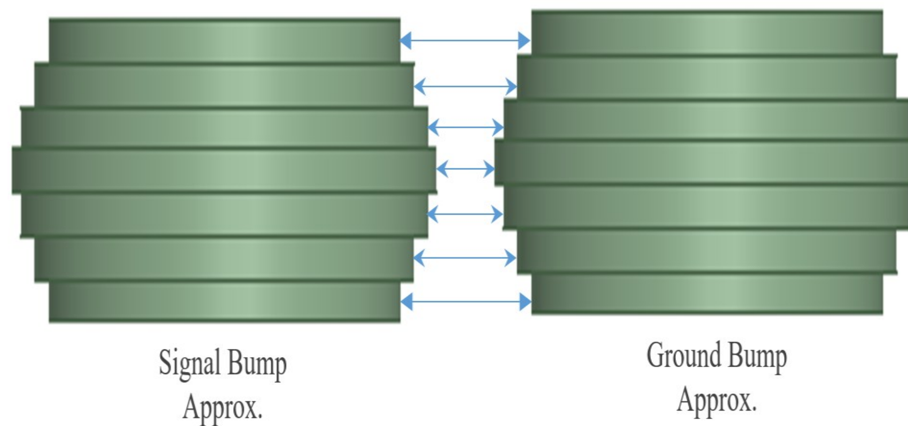


Figure 6.2.5: Electric filed lines between two segmented bumps.

Figure 6.2.5 shows the electric field lines between the signal bump and ground bump approximation. As there is no insulation layer present around the bumps only Eq. (6) is applicable here. So, the capacitance equation for the bump can be expressed as in (8).

$$C_{bump} = \frac{\pi\varepsilon_{si}}{ln\left[\frac{x}{2r_{bump}} + \sqrt{\left(\frac{x}{2r_{bump}}\right)^2 - 1}\right]}\Delta l + \frac{2\pi\varepsilon_{si}}{ln\left[\frac{x}{2(r_{bump}-\Delta r)} + \sqrt{\left(\frac{x}{2(r_{bump}-\Delta r)}\right)^2 - 1}\right]}\Delta l + \frac{2\pi\varepsilon_{si}}{ln\left[\frac{x}{2(r_{bump}-2\Delta r)} + \sqrt{\left(\frac{x}{2(r_{bump}-2\Delta r)}\right)^2 - 1}\right]}\Delta l + \cdots \ldots \ldots \tag{7}$$

$$C_{bump} = \frac{\pi\varepsilon_{si}}{ln\left[\frac{x}{2r_{bump}} + \sqrt{\left(\frac{x}{2r_{bump}}\right)^2 - 1}\right]}\Delta l + \sum_{n=1}^{(r_1-r_2)/\Delta r} \frac{2\pi\varepsilon_{si}}{ln\left[\frac{x}{2(r_{bump}-n\Delta r)} + \sqrt{\left(\frac{x}{2(r_{bump}-n\Delta r)}\right)^2 - 1}\right]}\Delta l \tag{8}$$

Here h is the distance between the top of the middle cylindrical segment to the end of the spherical segment. The relationship between r_1 and r_2 (refer to Figure 6.2.4), the height of the small cylindrical segment Δl, and the change of radius Δr, can be expressed as in Eq. (9) - Eq. (11).

$$r_1 - r_2 = n\Delta r \tag{9}$$

$$h = b - a \tag{10}$$

$$r_1 = \sqrt{r_{bump}^2 - (b-h)^2} \quad (11)$$

$$r_2 = \sqrt{r_{bump}^2 - (h-a)^2}$$

The radius of the original sphere r_{bump} and the radius of the middle most cylinder r_1 is equal. So $a \approx 0$ and $b = h.$ So h can be expressed as in Eq. (12) – Eq. (14).

$$h = \sqrt{(2r_1 - \Delta r) \times n\Delta r} \quad (12)$$

$$h \approx n\Delta l \quad (13)$$

$$\Delta l \approx \frac{\sqrt{(2r_1 - \Delta r) \times n\Delta r}}{n} \quad (14)$$

6.2.2 The Capacitive Model of the Landing Pads of the TSVs

The landing pads of the TSV would also contribute some capacitances in the TSV structure, but due to their lower dimension (width) compared to the bumps and the TSV cores the capacitance value is low. We can model the landing pad capacitance using the parallel plate and fringing capacitance models. Depending on the dimensions of the landing pad, bumps and TSVs, there will be fringing capacitance between the landing pad and the bumps, and the landing pad and the TSVs. But to make the model simple we are omitting these capacitances.

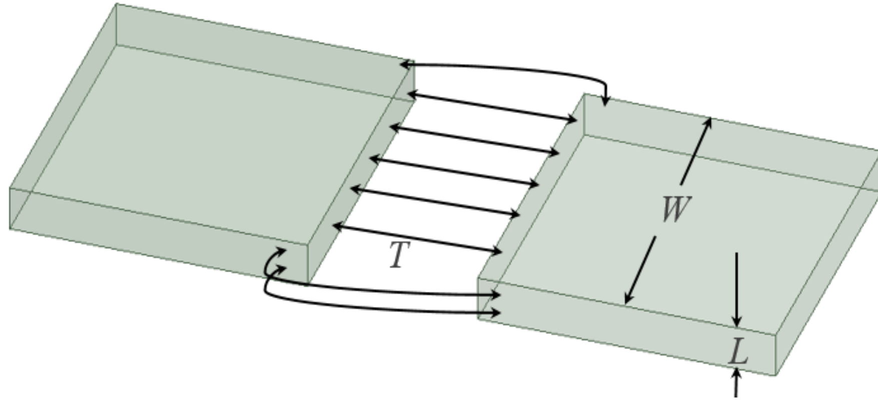


*Figure 6.2.6:*Parallel plate and fringe capacitances between two TSV landing pads. Here, L is the thickness, W is the height and width of the pad, and T is the distance between two pads.

The parallel plate and the fringe capacitances of the landing pad can be given by Eq. (15) and Eq. (16). We assume that the landing pad is a square box with a length of one side equal to W. We also assume the fringing capacitance is present on $\frac{1}{4}th$ of the length of W.

$$C_{PP} = \frac{\varepsilon_x WL}{T} \tag{15}$$

$$C_{fringe} = \frac{2\pi\varepsilon_x \frac{W}{4}}{ln\left(1 + \frac{2T}{\sqrt{L^2}}\right)} \tag{16}$$

6.2.3 The Capacitive Model of TSV Core

For two perfectly cylindrical TSV (as shown in Figure 6.2.7), Eq. (5) and Eq. (6) are adequate to calculate the capacitance between them. But unlike the vias in the silicon interposer, the vias in the glass have tapered shapes (see Figure 6.2.8) [50]- [51]. The taper

angle can vary from 75^0 to 88^0 depending on the via formation method [52]. Therefore, we divided the structure of a tapered via into small cylindrical segments as shown in Figure 6.2.9(an approach like what we have done for the bumps). The capacitance between two tapered TSV in the presence of silicon (or glass) substrate can be expressed as in (13).

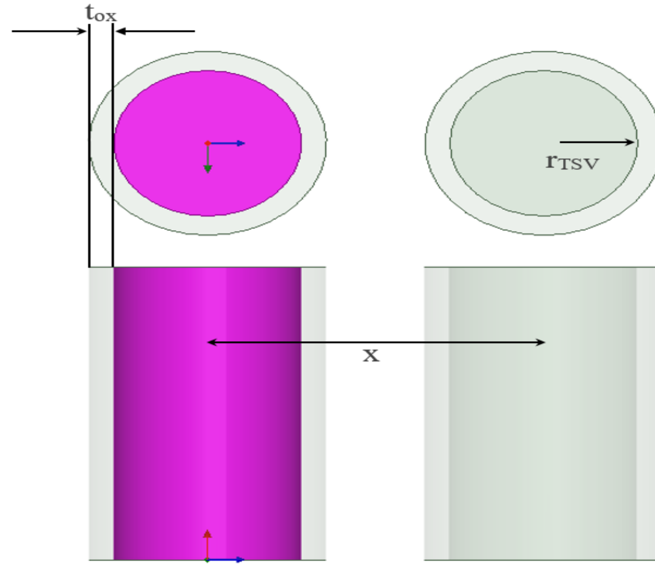


Figure 6.2.7: Cylindrical TSVs with a pitch of x, oxide layer thickness t_{ox} and Cu-filled layer radius r_{TSV}

Here $r_1$is the highest radius of the tapered TSV and r_2 is the lowest radius of the tapered TSV (as shown in Figure 6.2.8), Δl is the height of each cylindrical segment (as shown in Figure 6.2.9). Here, $r_1 > r_2$, and $\Delta r = \frac{r_1 - r_2}{n}$, where n is any positive integer. The thickness of the insulating layer (t_{ox}) is constant for both the tapered and cylindrical TSVs. Only the radius of the tapered TSV gradually decreases. Therefore, the capacitance due to insulating layer of the tapered TSV can be expressed as in Eq. (18) and Eq. (19).

$$C_{TSV,si} = \sum_{n=0}^{(r_1-r_2)/_{\Delta r}} \frac{\pi\varepsilon_{si}}{ln\left[\frac{x}{2(r_1-n\Delta r)} + \sqrt{\left(\frac{x}{2(r_1-n\Delta r)}\right)^2 - 1}\right]} \Delta l \tag{17}$$

$$C_{TSV,ox} = \frac{1}{T}\frac{2\pi\varepsilon_{ox}\Delta l}{ln\frac{r_1+t_{ox}}{r_1}} + \frac{1}{T}\frac{2\pi\varepsilon_{ox}\Delta l}{ln\frac{r_1-\Delta r+t_{ox}}{r_1-\Delta r}} + \frac{1}{T}\frac{2\pi\varepsilon_{ox}\Delta l}{ln\frac{r_1-2\Delta r+t_{ox}}{r_1-2\Delta r}} + \cdots \ldots. \tag{18}$$

$$C_{TSV,ox} = \sum_{n=0}^{(r_1-r_2)/_{\Delta r}} \frac{1}{T}\frac{2\pi\varepsilon_{ox}\Delta l}{ln\frac{r_1-n\Delta r+t_{ox}}{r_1-n\Delta r}} \tag{19}$$

When $r_1 = r_2$, the TSVs are perfect cylinders. The relation between r_1 and r_2, tapered angle α, and the height of the tapered TSV, h_{TSV} can be given by Eq. (21).

$$h_{TSV}\, tan\,\alpha = r_1 - r_2 \tag{20}$$

$$\Delta l = \frac{\Delta r}{tan\,\alpha} \tag{21}$$

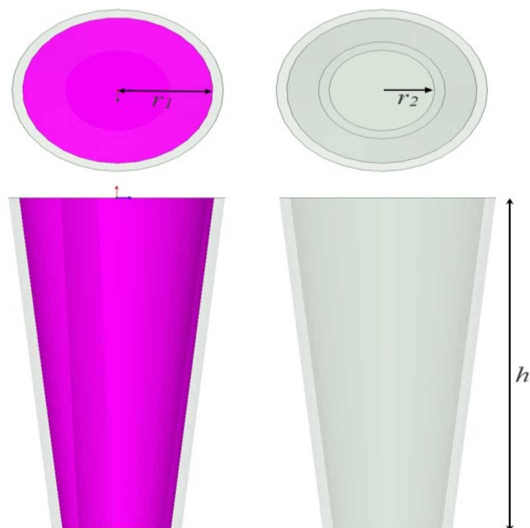


Figure 6.2.8: Tapered TSV with radius r_1 and r_2, where $r_1 > r_2$, and h is the height of the TSV.

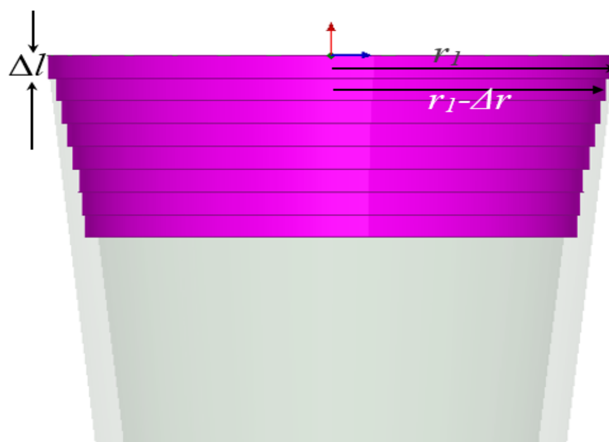


Figure 6.2.9: Tapered TSV divided into cylindrical segments with each step the radius of the cylindrical segments is decreased by an amount $\mathbf{\Delta r}$ and the height of each step is $\mathbf{\Delta l}$.

6.3 Modeling of TSV & Bump Resistance

The resistances of the TSV (R_{TSV}) and the bump (R_{bump}) are also modeled as functions of the structural parameters. High-frequency current flows close to the surface of the conductor due to the formation of the eddy current, which is called the “skin effect.” To model TSV and bump resistances with a nonuniform current distribution at high frequencies, the depth of penetration, which is the skin depth, must be determined. The skin depth depends on the material properties such as the permeability in H/m and the conductivity in S/m, and the frequency in Hz. So, the resistance of a TSV can be evaluated into two parts a. $R_{dc,TSV}$ in low frequency and b. $R_{ac,TSV}$ in high frequency when skin effect phenomena is dominant. DC resistance of a TSV is dependent on resistivity of the core material and the height and radius of the TSV and can be expressed as in Eq. (23) for TSV with height l and radius r.

Due to the skin effect with the increase of the frequency, the current tends to flow closer to the surface, reducing the effective radius of the TSV core. So the area of the TSV with radius r_{TSV} is reduced from πr_{TSV}^2 to $(2\pi \times r_{TSV} \times \delta_{skin\ depth,\ TSV} - \pi\delta_{skin\ depth,\ TSV}^2)$, therefore TSV resistance at high frequency can be expressed as in Eq. (24). Where the skin depth of the TSV due to the high frequency can be expressed as in Eq. (25), where μ_{TSV} is the relative permeability.

$$R_{TSV} = \sqrt{R_{dc,TSV}^2 + R_{ac,TSV}^2} \tag{22}$$

$$R_{dc,TSV} = \rho_{TSV} \times \frac{l_{TSV}}{\pi r_{TSV}^2} \quad (23)$$

$$R_{ac,TSV} = k_p \left(\frac{\rho_{TSV} \times l_{TSV}}{2\pi \times r_{TSV} \times \delta_{skin\,depth,\,TSV} - \pi \delta_{skin\,depth,\,TSV}^2} \right) \quad (24)$$

$$\delta_{skin\,depth,\,TSV} = \frac{1}{\sqrt{\pi f \mu_{TSV} \sigma_{TSV}}} \quad (25)$$

$$R_{dc,TSV} = \sum_{n=0}^{(r_1 - r_2)/\Delta r} \frac{\Delta l \, \rho_{TSV}}{\pi (r_1 - n\Delta r)^2} \quad (26)$$

$$R_{ac,TSV} = k_p \left(\sum_{n=0}^{(r_1 - r_2)/\Delta r} \frac{\rho_{TSV} \times \Delta l_{TSV}}{2\pi \times (r_1 - n\Delta r) \times \delta_{skin\,depth,\,TSV} - \pi \delta_{skin\,depth,\,TSV}^2} \right) \quad (27)$$

The resistances of a tapered TSV with radii $r_1$and r_2 and length l can be formulated as in Eq. (26) and Eq. (27). These two equations can also be used to formulate the resistance of bump.

6.4 **Modeling of TSV Inductance**

The inductance equation can be derived based on the physics associated with the wave propagation in a coaxial transmission line and a two-wire line. Assume the current flows in the wires in the opposite direction, so one becomes the return path for the other.

According to Ampere's law, magnetic field due to current flow I through a wire can be expressed as $B = \frac{\mu I}{\pi D}$. The magnetic flux between two wires is

$$\Phi_B = \int BdA = \frac{\mu I}{\pi} \int_{\frac{D}{2}}^{S} \frac{L}{\frac{D}{2}} d\left(\frac{D}{2}\right), dA = Ld\left(\frac{D}{2}\right) \tag{28}$$

$$\Phi_B = \frac{\mu I L}{\pi} \ln \frac{S}{\frac{D}{2}} \tag{29}$$

As inductance $L = \frac{\Phi_B}{I}$, Eq. (30) can be used to compute the loop inductance L_{TSV} based on Eq. (29) for the structure shown in Figure 6.2.8.

$$L_{TSV} = \left(\frac{\mu_0 \mu_{TSV}}{2\pi} \times h_{TSV} \times \ln\left(\frac{x}{r_{TSV}}\right)\right) \tag{30}$$

This equation does not capture the frequency dependence of inductance due to skin effect as for TSVs the frequency dependent variation of inductance is small and can be neglected. So, inductance equations for tapered TSV segmented into n parts with each of the segment having height Δl can be expressed as in Eq. (31).

$$L_{TSV} = \sum_{\mathrm{n}=0}^{(\mathrm{r}_1-\mathrm{r}_2)/\Delta\mathrm{r}} \left(\frac{\mu_0 \mu_{TSV}}{2\pi} \times \Delta l \times \ln\left(\frac{x}{r_1 - n\Delta r}\right)\right) \tag{31}$$

6.5 Equivalent Circuit and S-parameter for TSV Pair

Using the computed R, L, C parameters and equivalent circuit for a TSV pair can be constructed. The equivalent circuit is a lumped T-element circuit that is symmetric, where R, L are series elements, and C is the shunt element.

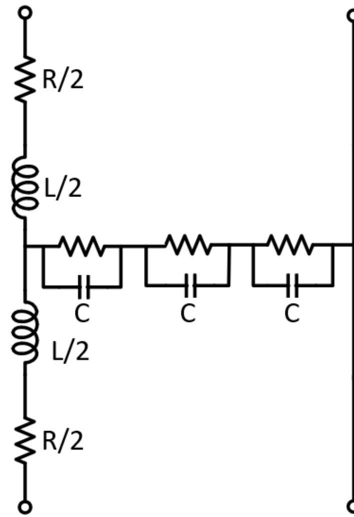


Figure 6.5.1: T-element equivalent circuit

6.6 Results and Analysis

An extensive comparative study is done to validate the accuracy of the derived mathematical expression. Furthermore, we compared our model with Q3D field solver [53]. Table 4 shows the TSV parameters used for model validation. We simulate tapered TSV and bump separately. Figure 6.6.1 shows the capacitance between two tapered TSVs when their

highest radius is changed from $16\mu m$ to $11\mu m$. We choose $\Delta r = 0.01\mu m$ so that when $r_1 = 16\mu m$, the TSV is composed of 1600 small cylindrical segments.

Table 4

TSV parameters and their values

Geometrical parameters	Typical value
Radius (r_1) of tapered TSV	16μm
Radius (r_2) of tapered TSV	10μm
SiO2 thickness	0.5μm
The height of the TSV	100μm
Pitch	110μm
Radius of Bump	50 μm
Number of TSV used	2
Relative permittivity (Cu)	1
Relative permittivity (Si)	11.9
Relative permittivity (SiO2)	4
Bulk Conductivity (Cu)	58×106S/m
Bulk Conductivity (Si)	0
Bulk Conductivity (SiO2)	0

We first simulate the capacitance between two cylindrical TSV in Q3D extractor. Then compare the simulation result with the capacitance resulting using Eq. (5) and Eq. (6) to generate an error term. Considering the error term our proposed model is closely matched with Q3D results showing error close to 10%.

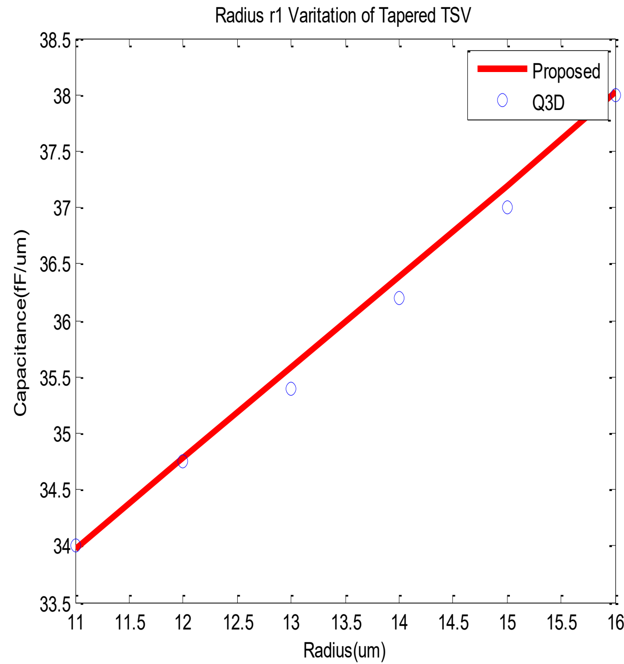


Figure 6.6.1: Comparison of Q3D field solver capacitance and the proposed model when the radius (r_1) is decreased from 16μm to 11μm.

Figure 6.6.2 shows the capacitance between the two sphere segment bumps. The radius of the bump $r_{bump} = r_1$ is varied from 45μm to 50μm and r_2 is varied from 35μm to 40μm to keep the height h [as in Figure 6.2.4] to be approximately equal to 30μm. We choose $\Delta r = 0.01$μm. The proposed model is within 5% of error margin.

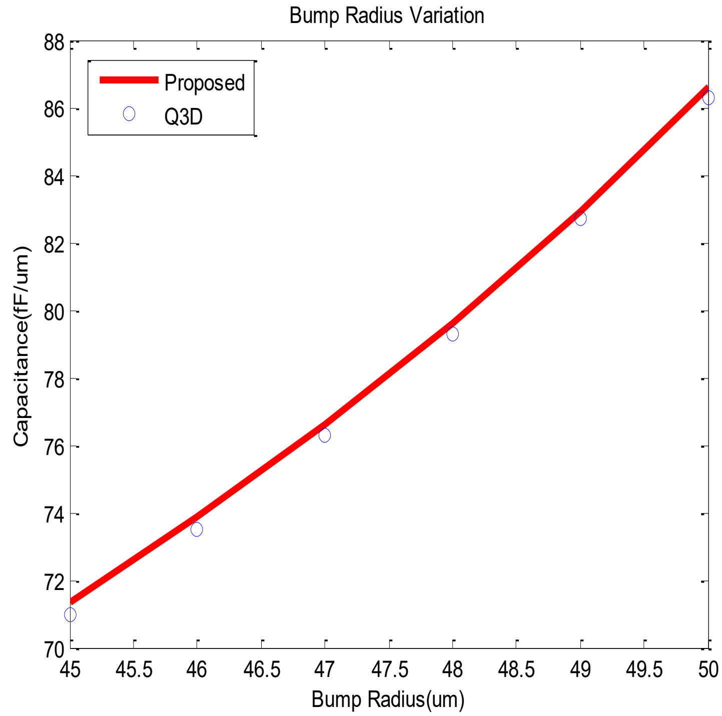


Figure 6.6.2: Comparison of Q3D field solver capacitance and the proposed model when the bump radius ($r_{bump} = r_1$) is varied from 45μm to 50μm.

The variation of resistance with frequency for a tapered TSV is shown in *Figure 6.6.3* where resistance is increased from 0.008Ω from 0.05Ω at 10GHz. It is evident from the figure that at a lower frequency only DC resistance is present and skin effect makes an impact after 100MHz.

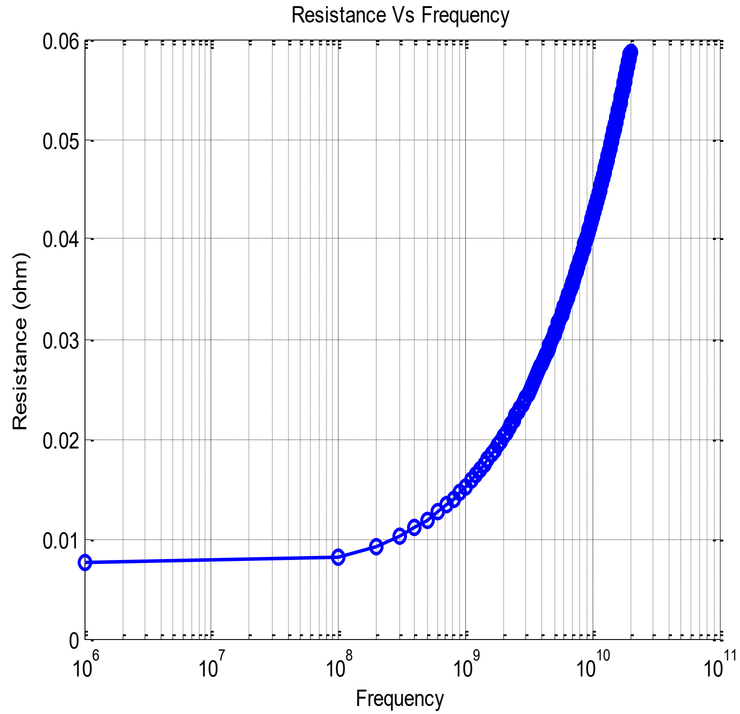


Figure 6.6.3: Change of TSV resistance with frequency due to the skin effect.

Using the T-element equivalent circuit the computed return loss (S_{11}) for differential TSV pair is shown in Figure 6.6.4. The correlation of the physics-based model to the electromagnetic simulation is quite good with a small deviation of about 5%.

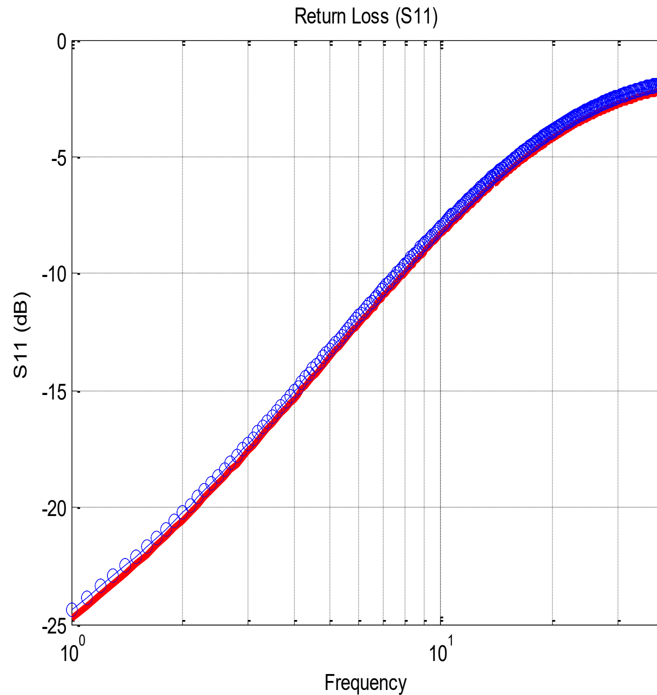


Figure 6.6.4: Return loss of differential TSV

6.7 **Summary**

A mathematical model to calculate TSV capacitance, resistance and inductance are developed in this paper by segmenting large TSV and bumps into small cylindrical segments. The derived expressions are simple and show excellent agreement with the parasitic extraction software Q3D. The model estimates the RLC values for both cylindrical and tapered TSV within less than 5% of error margin. The models also capture the effect of high frequency and the accurately predict the change of resistance of TSV at different frequencies. Performance of TSV at high frequency is modeled with an equivalent T-element circuit, and

the return loss is measured (up to 40GHz) and compared with the industry standard high-frequency tool HFSS. The proposed model is scalable and can be applied to the various dimension of TSVs and bumps and thus can be embedded as a quick tool in CAD circuit programs.

CHAPTER 7

DESIGN AND CHARACTERIZE TSV BASED INDUCTOR FOR HIGH FREQUENCY VOLTAGE-CONTROLLED OSCILLATOR DESIGN

7.1 Introduction

The necessity to integrate more functionality in the same IC footprint of the state-of-the-art electronics pushes silicon scaling to its limit. Industries tried to embrace new design methodologies like system-on-chip (SoC) in which predesigned blocks obtained from third parties or internal sources are combined in a single chip [54]. The main challenge of SoC technology is to place digital, analog, and RF circuits in the same die using the same process node, which is a challenging goal to achieve. A different design approach, system-in-package (SiP), where different technology nodes have different die and all are mounted on a single package substrate, was also explored. However, both 2D design methodologies (SoC and SiP) require connecting an exceedingly large number of transistors using long on-chip wires. The high volume of long wires results in very high-power consumption, signal delay, and noise due to the parasitic effects (resistance, capacitance, and inductance of the interconnecting lines). For example, the delay introduced by the long interconnects is the main limiting factor of signal speed in current digital systems [55]. As a remedy, a 3D integrated circuit based on Through-Silicon-Via (TSV) has emerged in the last two decades. TSVs have been proven to be the solutions for many of the problems related to long on-chip interconnects. 3D integration can be defined as the stacking multiple dies or chips on top of

each other [56]. On the same footprint of a 2D IC, 3D IC can deliver more functionality and better performance. The TSVs in a 3D IC are the vertical interconnects between the chips and are responsible for power and signal delivery among the chips. 3D integration reduces the interconnect length compared to the 2D ICs. Shorter interconnect of 3D IC leads to lower power consumption and signal delay [57]- [58]. As a result, 3D IC with TSV has a higher potential to deliver better performance.

Among the many challenges of 3D ICs, the large size of the TSVs (typically 5-10x larger than the standard cells in the 32nm process [59]) is a major one. The problem is that the diameters of the TSVs do not scale with the devices due to the imposed limitations of wafer handling and aspect ratios. Based on International Technology Roadmap for Semiconductors (ITRS) suggestion, the TSV diameters remained almost constant in the 2012-2015 period [60]. It is also important to acknowledge that a large number of TSVs are needed to deliver signal and power, to dissipate heat, and to provide redundancy. Moreover, to ensure a high yield rate, foundries typically impose a minimum TSV density rule. For example, *Tezzaron* [61] requires that at least one TSV must exist in every 250µm x 50µm area [62]. To comply with this rule, many dummy TSVs required be inserted, which further increases the area overhead. To lessen the problem with dummy TSVs, there have been efforts to utilize these dummy TSVs for other purposes [63].

One of the most difficult challenges in integrated circuit design and fabrication is the integration of on-chip inductors. Conventional implementation of on-chip inductors uses a

multi-turn planar spiral structure. This structure occupies a significant area and requires a special RF process for a higher quality factor. In 3D ICs, however, it is possible to utilize the TSVs to build vertical inductors [64] - [65]. An apparent advantage of such TSV based inductors is the minimal footprint on routing layers and, accordingly, high inductance density. However, since it is completely buried in the lossy substrate, its quality factor is inferior compared to that of the 2D spiral inductor. Here we investigate tradeoffs among several critical measures of on-chip inductor design to enable more efficient implementations and circuits.

7.2 Background

On-chip inductors traditionally use a planar multi-turn spiral structure that consumes significant global routing and requires additional shielding to prevent the coupling [66]. Due to its consumed area and cost, the use of a planer on-chip spiral inductor is limited to very few critical applications. Recently TSV based inductor has been proposed to overcome the issues mentioned above of a planner inductor, which utilize dummy/unused TSVs to form to an on-chip vertical inductor for 2.5/3D design [67]. Such structures enable a more compact design with smaller parasitic and can be used for applications with wide frequency ranges.

The properties of inductors are highly associated with the magnetic field it creates. The magnetic field intensity is represented by the magnetic flux density B as in Eq. (1), where μ is absolute magnetic permeability.

$$B = \mu . H \tag{1}$$

Similar to capacitors storing electric charge, an inductor stores magnetic energy within the core of its windings where the flux density is highest. The inductance, in general, a function of the inductor's geometric shape and can be determined by the ratio of flux leakages to the current that creates the magnetic flux as in Eq. (2) for a N-loop solenoid.

$$L = \frac{\lambda}{I} = \Phi_T . \frac{N}{I} = \frac{\mu N^2 \pi r^2}{h} \propto N^2 \tag{2}$$

For modeling the TSV based inductor, the key control factors are radius and length of the TSV, the distance between adjacent TSVs (pitch) and length, width and thickness of metal interconnects, and the number of turns as shown in Figure 7.2.1. In most cases, the radius and length of the TSVs and the thickness of the metal interconnects are limited by the foundry process, and due to mechanical stress, TSV pitch has certain minimum threshold limits. In general, the substrate is assumed to be bulk silicon, which is conductive, hence a separation layer of SiO_2 is maintained between the metal and silicon layers.

The inductance and quality factor of the inductor are calculated from the Y parameters, as shown in Eq. (3) and (4).

$$L = \frac{lmag\left[\frac{1}{Y_{11}}\right]}{2\pi f} \quad (3)$$

$$Q = \frac{lmag\left[\frac{1}{Y_{11}}\right]}{Real\left[\frac{1}{Y_{11}}\right]} \quad (4)$$

Figure 7.2.2 shows how the inductance and quality factor changes as the radius of the TSVs varies from $0.5\mu m$ to $4.0\mu m$. The inductance of a 3D inductor increases with a decreasing radius, so it is tempting to uses very narrow TSVs to make the inductors. But analyzing the quality factor Q, it is evident that the same is not true for Q, as Q tends to decrease with decreasing radius. So, to achieve high inductance value with a high quality factor, an optimum radius should be chosen.

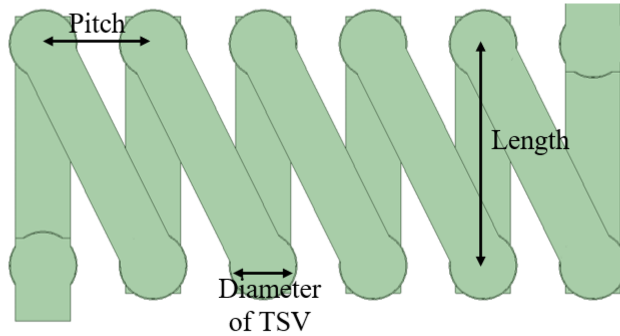
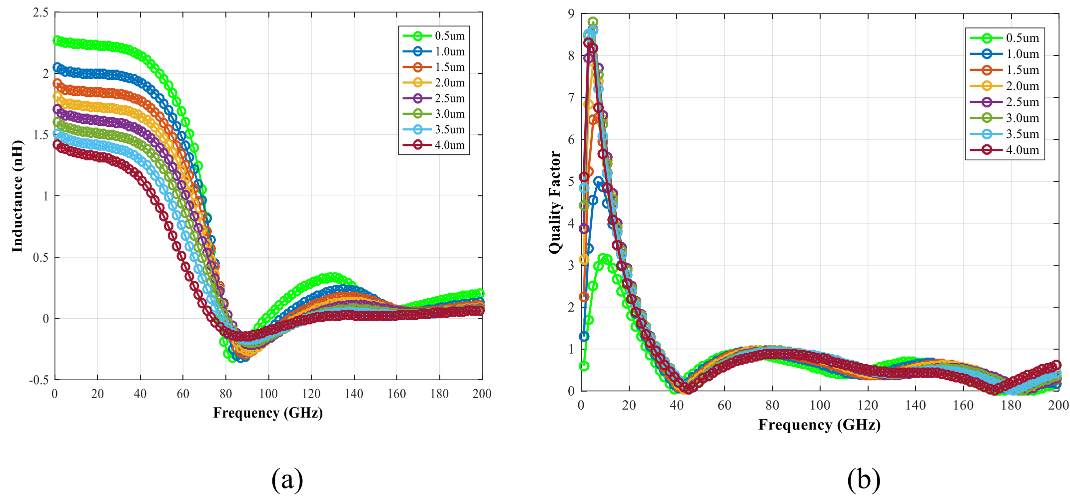


Figure 7.2.1: TSV based 3D inductor (top view)

Other than the inductance (L) and Quality factor (Q) the performance of the inductor also depends on series DC resistance (R_{dc}) which is the resistance of the inductor at DC and AC resistance (R_{ac}), which is the resistance of the inductor at the frequency of interest, as shown in Figure 7.2.3. In general, the series resistance of an inductor can be expressed as Eq. (5).

$$R_s = \frac{2\pi f L}{Q} \tag{5}$$



(a) (b)

Figure 7.2.2: (a) Inductance and (b) Quality Factor of 3D TSV inductor when the radius of the TSV changes from 0.5μm − 4.0μm.

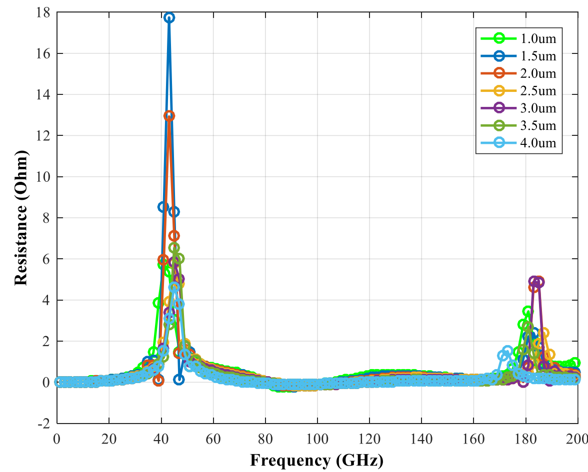


Figure 7.2.3: The series resistance of a 3D TSV inductor when the radius of the TSV changes from $1.0\mu m - 4.0\mu m$.

To reduce the series resistance of a 3D inductor, the maximum possible radius of the TSV that support by the foundry can be used, but that will reduce the overall inductance of the inductor. So, one should investigate the core material that is used for TSV. The common core material that is used for signal TSVs is Tungsten (W) for its superior signal integrity performance over other materials. But compared to Copper (Cu) the resistivity of W is way too high. So Cu is the suitable candidate for Core material. Also, the inductors are formed using the TSVs in the topmost metal layers to reduce its series resistance.

Two common structure to form a TSV based inductors are Coupled vertical TSV structure and Coupled toroidal TSV structure [66]. Though the coupled vertical TSV structure is compact and saves more area, toroidal based inductor shows the smallest R_{ac} and

higher Q compared to coupled vertical spiral TSV inductor due to its larger cross-sectional area.

7.3 Optimization of TSV Inductor Performance for VCO Design

The monolithic CMOS planar inductor architecture has been widely used due to the ability to integrate it using the existing CMOS processes. The usage of damascene processing and inter-layer vias enabled the integration of the inductor in the uppermost layers of the standard multi-metal processes. However, these inductors occupy a significant portion of the metal layers and impose very high area and power overheads. Serious efforts have been made to optimize inductor designs, and several alternatives to conventional architecture have been proposed. Patterned ground shields (PGS) were theoretically expected to diminish the substrate losses. However, experimental results have shown little improvement. Differential symmetric inductors have the potential to provide the best possible performance. Still, the designers usually do not use these mainly due to the irregular and complicated design and because of the proximity of the ports that result in stronger interconnect coupling. Integrated inductors have been reported in exotic technologies like Silicon-on-Insulator (SOI) platforms. However, these inductors require modification of many steps in the current 2D CMOS processes. The planar integrated inductors occupy excessively larger areas because the ferrite cores are not applicable. Other alternative designs like the stacked inductor have

been reported. Still, compared to the single-layer inductors, the stacked inductors exhibit higher capacitive losses and higher resistance because the lower metals are thinner.

To overcome the limitations of the existing inductor design and integration techniques, TSV based implementation of inductors in 3D ICs is gaining significant attention. In this project, the objective is to come up with an innovative design technique for the 3D TSV based inductor. The second objective is to optimize the design so that the inductor can be used in an LC Voltage Controlled Oscillator (VCO) that would oscillate between $5 - 6\ GHz$. Different approaches of inductor designs are investigated to find the combination that provides the maximum inductance and the highest quality factor, which is a crucial metric used to measure the efficiency of an inductor.

Figure 7.3.1 shows the 3D TSV based inductor structure. Here all the TSVs are located on the same plane. The number of turns is 10. The design parameters are summarized in Table 5. We used this structure and varied the core material of the TSVs, substrate material, oxide thickness, etc. to measure the inductance and quality factor.

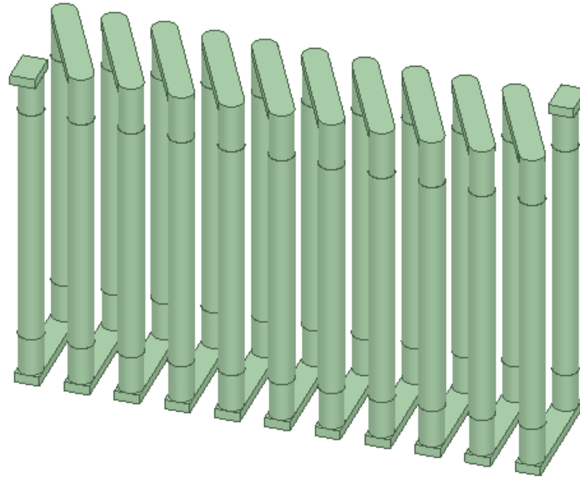


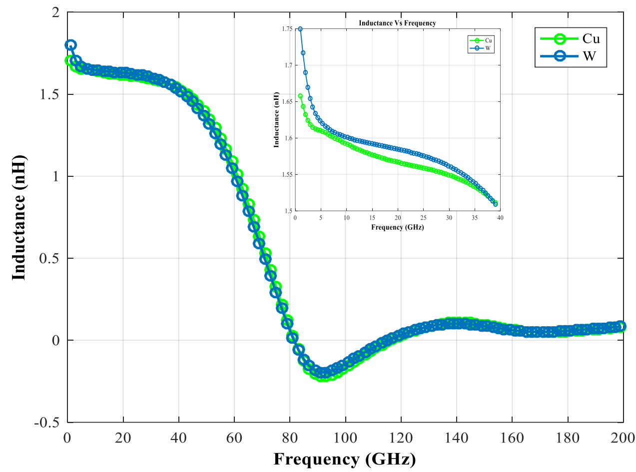
Figure 7.3.1: 3D TSV based inductor in a single layer with 10 turns.

We first investigate if the core material of the TSV has any effect on the inductance and quality factor. For this, we used Copper (Cu) and Tungsten (W) as the core material and silicon as the substrate material to simulate the behavior of the inductor. Figure 7.3.2 shows that at our frequency of interest (between $5 - 6\,GH$), TSVs with Tungsten (W) core has slightly higher inductance value ($1.63nH$) whereas Copper (Cu) core is showing $1.61nH$ of inductance. But there is a bigger difference in quality factor between these two. In this case, Cu based TSV shows a better result (Figure 7.3.2 (b)) with a quality factor of 8.6 compared to 5 in the case of W. Even though Cu based TSV inductor has higher quality factor value in Silicon substrate, the value is not optimal. This is because, in the 3D TSV structure, the TSVs are inside the silicon substrate, which tends to be very lossy at higher frequencies. As part of

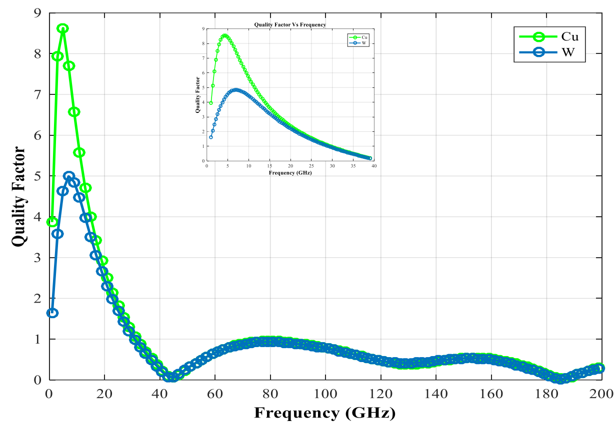
our investigation to find a better solution, we have also explored Glass substrate to compare its performance with the silicon substrate.

Table 5
TSV Design Parameters

Parameters	**Dimensions/Value**
Radius of TSV	2.5 μm
Thickness of Dielectric	0.5 μm
Length of TSV	50 μm
Number of turns	5-10
Tier	1-2
Pitch	10 μm



(a)

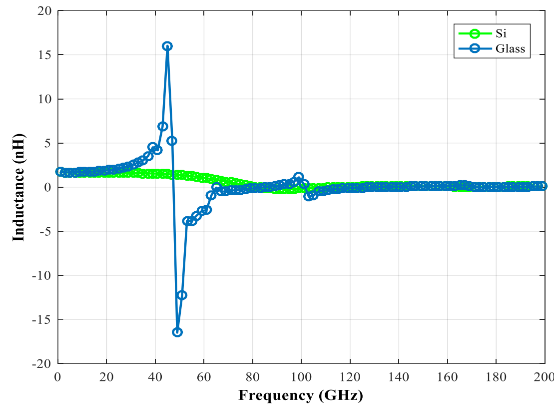


(b)

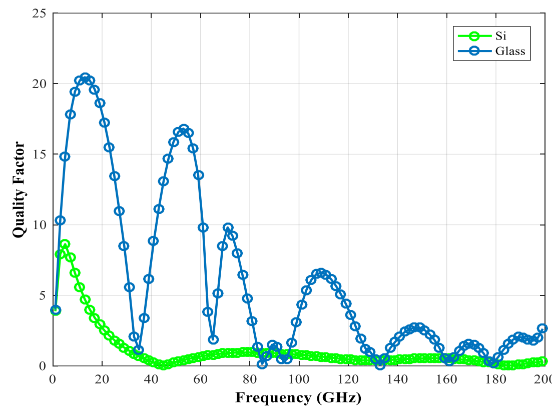
Figure 7.3.2: (a) Inductance and (b) Quality Factor of 3D TSV inductor when Cu (Green) and W (Blue) are used as the core material.

Figure 7.3.3 shows the simulation results comparing between Silicon and Glass substrate. In this simulation, Cu is used as the core material for TSVs. At the frequency of interest, both Silicon and Glass show the same value of inductance, but the more significant difference is in the quality factor. The quality factor is almost double in the case of Glass

compared to silicon, which indicates Glass tends to be less lossy at higher frequencies than Cu.



(a)

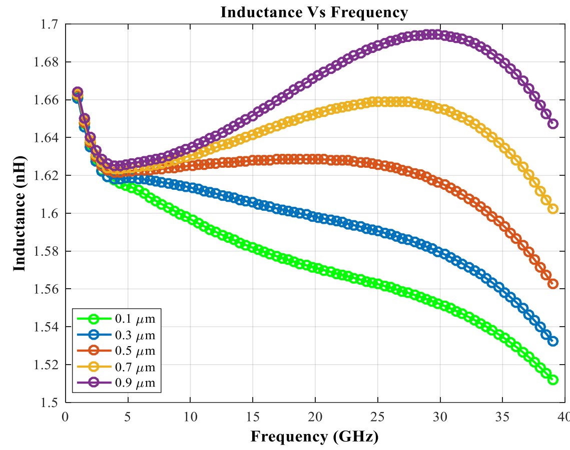


(b)

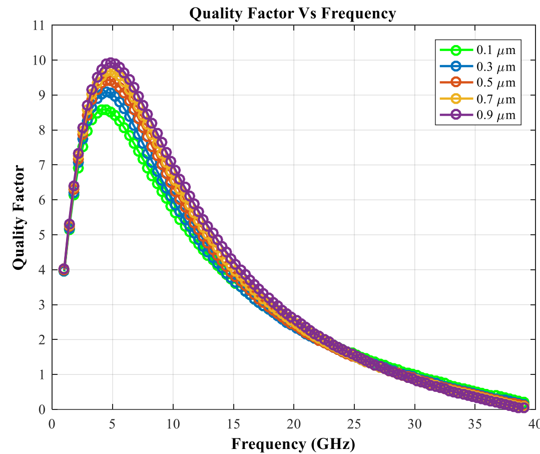
Figure 7.3.3: (a) Inductance and (b) Quality Factor of 3D TSV inductor when Si (Green) and Glass (Blue) are used as the substrate.

Another way to tackle the leakage to the substrate issue is to increase the width of oxide thickness that surrounds the TSVs. We simulate the effects of oxide thickness in case

of Silicon substrate with SiO_2 surrounding layer. We varied the thickness from $0.1 - 0.9\ \mu m$. As expected, the quality factor increases with increasing oxide thickness (Figure *7.3.4*(b)) as a thicker oxide layer reduces leakage to the substrate. Still, interestingly the inductance value also increases slightly, as shown in Figure *7.3.4*(a).



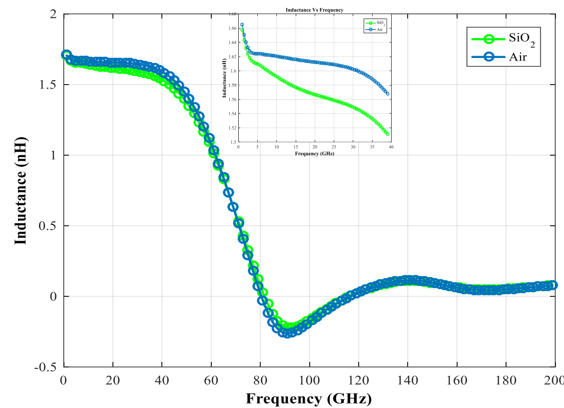
(a)



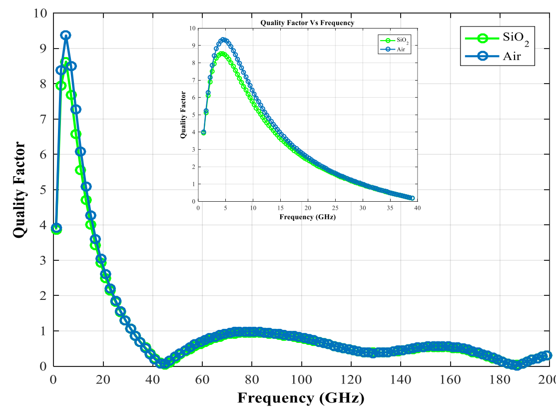
(b)

Figure 7.3.4: (a) Inductance and (b) Quality Factor of 3D TSV inductor for different 'Oxide thickness.

Using air gaps instead of $SiO_2$is another way to improve the electrical and thermal performance of TSVs [68]. We simulate to observe if using air gaps gives rise to any significant improvement in the quality factor of the inductance. Figure 7.3.5 show the simulation results where the simulation is performed with Cu core and Silicon substrate. The simulation results indicate that there is close to 15% improvement is can be achieved while using air gaps.



(a)



(b)

Figure 7.3.5: (a) Inductance and (b) Quality Factor of 3D TSV inductor for SiO_2/Air insulation layer.

Finally, the area constraint is the main factor we have to consider. For this reason, we investigate if reducing the number of turns hence reducing the lateral area, has any effect. Figure 7.3.6(a) shows one such structure where we reduced the number of turns from 10 (Figure 7.3.1) to 5, but in this case, instead of using a single layer the structure is in between two layers increasing the height of the TSV as so the total loop is same compared to single-layer TSV structure. Figure 7.3.7 shows the simulation results comparing single tier and 2-tier structure. The result indicates that lowering the turn but increasing the tier helps to increase the quality factor by almost 30%. Table 6 summarizes the performance of different 3D TSV based inductors.

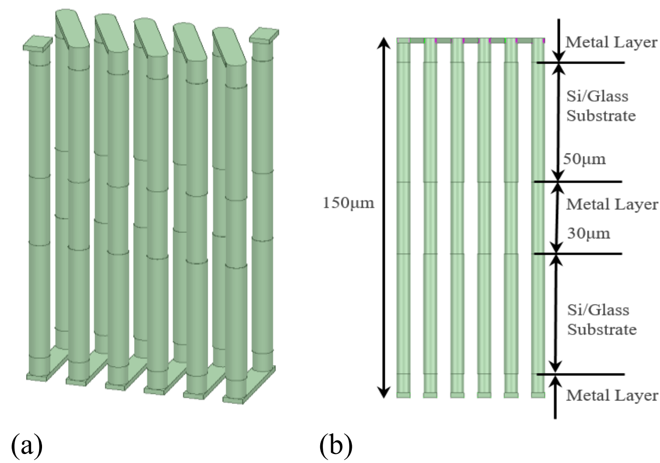
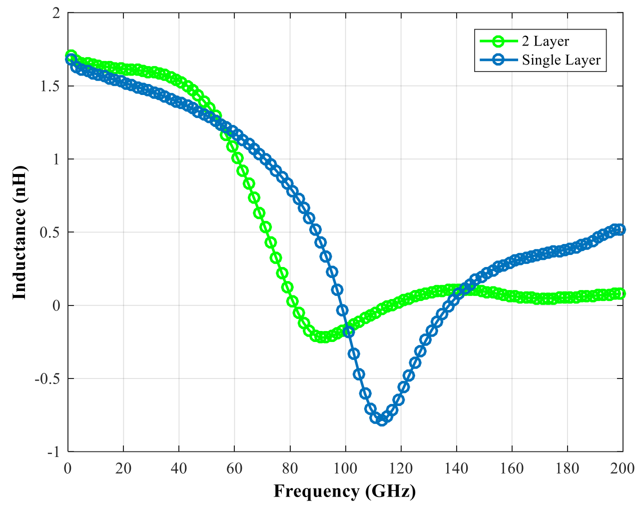
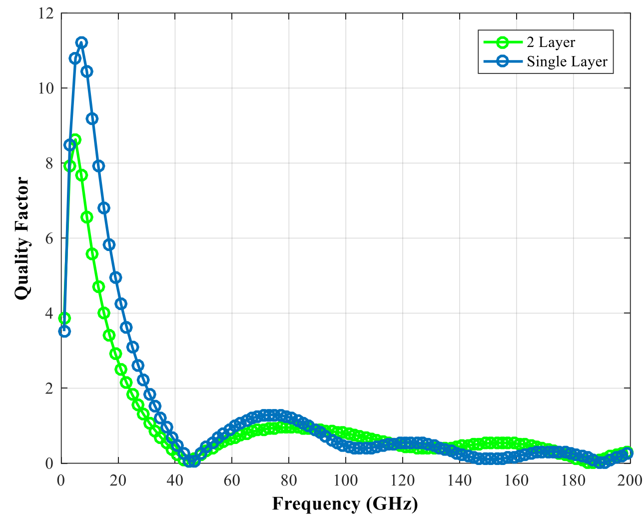


Figure 7.3.6: (a) 3D TSV based inductor (b) Cross-sectional view of 3D TSV inductor.



(a)



(b)

Figure 7.3.7: (a) Inductance and (b) Quality Factor of 3D TSV inductor for Single layer and two-layer approach.

Table 6
Inductor Performance Comparison

	Inductance (nH)	**% Improvement**	**Quality factor**	**% Improvement**
Si-Cu-1 Tier	1.61	-	8.5	-
Si–W-1Tier	1.63	1.25%	5	-41%
Glass-Cu-1Tier	1.61	0%	17	100%
Si-Cu-1Tier-Air	1.625	1.2%	9.5	11%
Si-Cu-2Tier	1.63	1.25%	11	29%

7.4 Voltage Controlled Oscillator Design Using TSV based inductor

A voltage-controlled oscillator is one of the main building blocks of Phased Locked Loop (PLL). Different types of oscillators are used for high-frequency applications, namely Ring Oscillator, Relaxation Oscillator, and LC Oscillator. The LC-based oscillator can provide better phase noise performance compared to a ring and relaxation oscillator. The resonance of an inductor and a capacitor is the basis of all LC oscillators. The negative resistance required to maintain the oscillation can be provided by cross-coupled transistors. Figure 7.4.1 shows LC VCO with cross-coupled PMOS and NMOS structure. As the inductor, we use the model TSV based inductance we simulate in the previous section. Table 7 summarizes the inductor parameters.

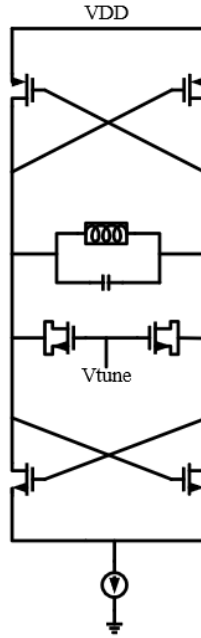


Figure 7.4.1: LC VCO with Cross coupled NMOS/PMOS with varactor Capacitor for voltage tuning.

Table 7
Inductor parameters for VCO Design

L	1.6 nH
Q @ Fmax	15
C_par_L	112.57 fF
Rp	110 ohms

The capacitance per unit inductance and equivalent resistance (R_p) can be calculated using the equations (6) and (7).

$$C_{par_L} = \frac{1}{(2\pi f_{res})^2 L} \tag{6}$$

$$R_p = L\omega Q = 2\pi f_{min} LQ \frac{f_{min}}{f_{max}} \quad (7)$$

To overcome the value of R_p we have to add the cross-coupled NMOS/PMOS, which will act as a negative resistance source. The transconductance of the MOS pairs should be equal to $g_{mcore} = \frac{2}{R_p}$. Table 4 shows all the other design parameters.

Table 8
Core parameters for VCO Design

Ibais	5 mA
W_nmos	50 μm
W_pmos	100 μm
L	0.18 μm
C (Varactor)	25 fF

7.5 Analysis

The designed VCO shows a tuning range of $1GHz$ (from $5 - 6GHz$). We extracted the S-parameter values of the inductor and used the S-parameter model in a Hspice simulator to simulate the VCO. Figure 7.5.1 and Figure 7.5.2 show the circuit oscillating at a frequency of $6GHz$ and $5.2GHz$ respectively. The proposed TSV inductor based VCO should take much less area compared to LC VCOs that used monolithic inductors. The power consumption is around 0.5mW, which is reasonable. Table 9 summarized the performance of the VCO.

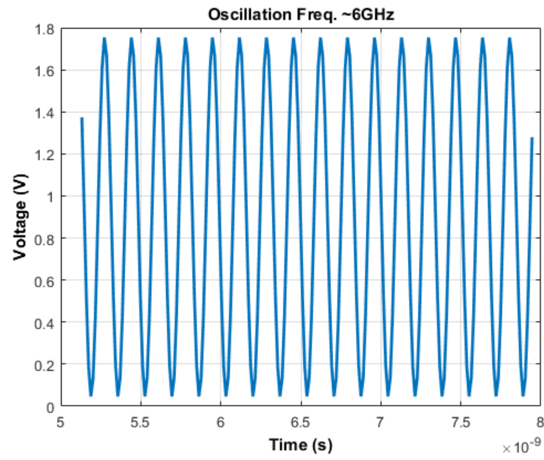


Figure 7.5.1: Frequency of oscillation 6GHz

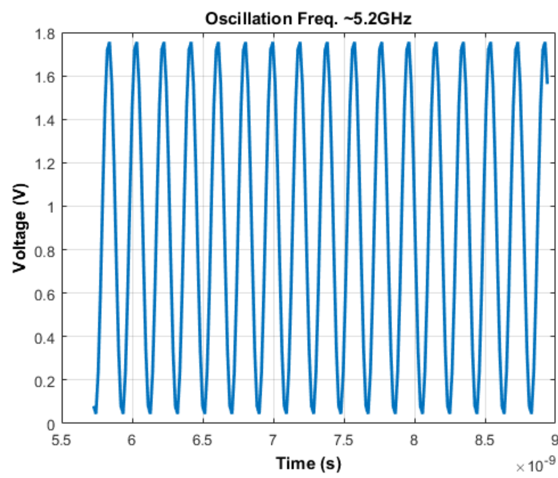


Figure 7.5.2: Frequency of oscillation 5.2GHz

Table 9
VCO Performance

CMOS Process	180 nm
Supply voltage	1.8 V
VCO type	LC
Output Phase	2
Phase Noise	-
Power	0.5 mW
VCO tuning range	5-6GHz

7.6 Summary

A LC-based voltage-controlled oscillator with the tuning frequency of 5-6GHz is implemented with the TSV based inductor. To achieve maximum performance from the TSV based inductor, we investigate different materials and structures. We conclude that a TSV with a Copper core inside a Glass substrate will give the highest achievable performance with an inductance value of 1.6nH and a quality factor of 17. When compared to Through-silicon via based inductor with similar size and design the TGV based inductor shows 1.25% improvement in inductance value and as high as 41% improvement in quality factor. The biggest advantages of having TSV/TGV based inductor in integrated circuit design is the area requirements. In our VCO design it requires 35% less area compared to having an on-chip inductor. TSV/TGV based inductors can also be used where on-chip inductors are used and

the requirements of inductance value is not so high such as low-drop out regulator and analog filters.

CONCLUSION AND FUTURE WORK

Novel analytical models for interconnect capacitance are developed by geometrically modeling electric flux lines between interconnect lines in a multilayer interconnect structure. First, we formulate the capacitance model of a single wire over a ground plane. When compared the model with capacitance extractor simulation software Ansys Q3D the result is within 10% of its simulation value. Based on the single interconnect model we then developed a capacitance model for multiple interconnect line between two ground plane and a special case where multiple interconnect line were placed over a single ground plane. Both models show good consistency when compared to Q3D results showing less than 8% error. While most existing capacitance models are constrained by a specific range of interconnect dimensions, the proposed models can be applied to any VLSI interconnect configurations and thus can be embedded as a quick tool in CAD circuit programs. The proposed model is useful when the interconnect dimension is not less than 5nm. For structures having dimension less than 5 nm, the model is not a very good fit. Further investigation will be done to model capacitance for interconnect having very narrow structure.

Conventional TSV material like Cu and W, non-conventional material like Au and Cu-W bimetal are investigated. Insertion loss and return loss are measured for those materials as well as silicon and glass interposers. It is observed that TSVs in glass interposer demonstrate much better performance than in silicon interposer. Therefore, to reduce the crosstalk effect in 3D ICs it is better to use glass interposer. In high frequencies, TSV core

made of W has shown better performance in case of insertion loss (transmission coefficient) and far end crosstalk (FEXT). The W based TSV also shows better performance in terms of near-end crosstalk (NEXT) when the operating frequency is low. In glass interposer the performance of Cu TSV is better. Therefore, W based TSV might be the better choice for signal TSV in moderately high frequency applications. The performance of Cu-W bimetal TSV is not better than W via but it is very similar to Cu via. So if Cu-W bimetal TSV is used it can handle both the thermal stress of Cu on silicon and the crosstalk effect. For better understanding of the Cu-W bimetal TSV an analytical model for the structure should be developed and the result obtained from the model should be compared to the simulation results for the validation of the model. It is also found from the analysis that the insertion loss depends on the TSV diameter and as the diameter increases the insertion loss decreases. The size of the bumps has its effect on the return loss and insertion loss. To reduce these losses bump size should be increased. Increasing the TSV layers caused higher return and insertion loss. In future novel material like carbon nanotube can be investigated as the core material of TSV.

Various performance parameters like return loss, transmission coefficient, mutual electric and magnetic field coupling have been measured and compared for conventional circular TSV and different polygonal TSVs. From the simulation results it is observed that the rectangular TSV has superior performance in terms of return loss, insertion loss and H-field coupling. Octagonal TSV shows good results when measuring the E-field coupling. As

the segments of the polygon increases the performance degrades. For optimal performance rectangular TSV can be used if the fabrication process supports. Having an insulating layer surrounding the core also play an important role on the TSV performance.

A mathematical model to calculate TSV capacitance, resistance and inductance are developed by segmenting large TSV and bumps into small cylindrical segments. The derived expressions are simple and show excellent agreement with the parasitic extraction software Q3D. The model estimates the RLC values for both cylindrical and tapered TSV within less than 5% of error margin. The models also capture the effect of high frequency and the accurately predict the change of resistance of TSV at different frequencies. Performance of TSV at high frequency is modeled with an equivalent T-element circuit, and the return loss is measured (up to 40GHz) and compared with the industry standard high-frequency tool HFSS. The proposed model is scalable and can be applied to the various dimension of TSVs and bumps and thus can be embedded as a quick tool in CAD circuit programs.

An LC-based voltage-controlled oscillator with the tuning frequency of 5-6GHz is implemented with the TSV based inductor. To achieve maximum performance from the TSV based inductor, we investigate different materials and structures. We conclude that a TSV with a Copper core inside a Glass substrate will give the highest achievable performance with an inductance value of 1.6nH and a quality factor of 17. When compared to Through-silicon via based inductor with similar size and design the TGV based inductor shows 1.25% improvement in inductance value and as high as 41% improvement in quality factor. The

biggest advantages of having TSV/TGV based inductor in integrated circuit design is the area requirements. In our VCO design it requires 35% less area compared to having an on-chip inductor. TSV/TGV based inductors can also be used where on-chip inductors are used and the requirements of inductance value is not so high such as low-drop out regulator and analog filters.

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VITA

Abdul Hamid Bin Yousuf received his B.Sc. and M.S. degree in Applied Physics and Electronics from University of Dhaka, Bangladesh, in 2010 and 2012, respectively. Then he joined Southeast University as a lecturer in the department of Electronics and Telecommunication Engineering and worked there up until summer 2013. From Fall 2013, he started Ph.D. under supervision of Dr. Masud Chowdhury in University of Missouri-Kansas City. His primary discipline for Ph.D. was electrical engineering with physics as co-discipline.

His research interests include high-speed interconnect design for next generation computing, through-silicon via modeling and implementation, phase-locked loop design and integration. In Fall 2019 he joined Ferric Inc. as Analog and mixed signal circuit design intern and worked on clock distribution network design. He also worked as Analog circuit design intern in Intel Inc. in Summer and Fall of 2020.