MULTIPLE-VALUED LOGIC: TECHNOLOGY AND CIRCUIT IMPLEMENTATION

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MULTIPLE-VALUED LOGIC: TECHNOLOGY AND CIRCUIT IMPLEMENTATION

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ABSTRACT

Computing technologies are currently based on the binary logic/number system, which is dependent on the simple on and off switching mechanism of the prevailing transistors. With the exponential increase of data processing and storage needs, there is a strong push to move to a higher radix logic/number system that can eradicate or lessen many limitations of the binary system. Anticipated saturation of Moore's law and the necessity to increase information density and processing speed in the future micro and nanoelectronic circuits and systems provide a strong background and motivation for the beyond-binary logic system. During this project, different technologies for Multiple-Valued-Logic (MVL) devices and the associated prospects and constraints are discussed. The feasibility of the MVL system in real-world applications rests on resolving two major challenges: (i) development of an efficient mathematical approach to implement the MVL logic using available technologies and (ii) availability of effective synthesis techniques.

The main part of this project can be divided into two categories: (i) proposing different novel and efficient design for various logic and arithmetic circuits such as inverter, NAND, NOR, adder, multiplexer etc. (ii) proposing different fast and efficient design for various sequential and memory circuits. For the operation of the device, two of the very promising emerging technologies are used: Graphene Nanoribbon Field Effect Transistor (GNRFET) and Carbon Nano Tube Field Effect Transistor (CNTFET). A comparative analysis of the proposed designs and several state-of-the-art designs are also given in all the cases in terms of delay, total power, and power-delay-product (PDP). The simulation and analysis are performed using the H-SPICE tool with a GNRFET model available on the Nanohub website and CNTFET model available from Standford University website.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled "Multiple-Valued Logic: Technology and Circuit Implementation," presented by Zarin Tasnim Sandhie, candidate for the Doctor of Philosophy degree, and hereby certify that in their opinion it is worthy of acceptance.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

With the exponential increase of the quantity and density of information, the demands for extremely high data processing speed and storage requirements are rapidly moving beyond what binary logic based digital systems can offer. Binary logic-based computing machines are expected to face an enormous challenge in the near future due to the severe thermal and reliability problems. To mitigate these inevitable limitations of the binary systems, researchers have already started exploring different multiple-valued logic and memory devices. Before the semiconductor device technology came into existence, the electrical switching system relied on electromagnetic relays and its derivatives. Though the simplest form of relays was binary, there were also some multi-position devices, which were used in the telephone system, railroad traffic control, and some industrial applications. The design of such systems was not firmly based upon any structured mathematical or synthesis technique. With the introduction of solid-state devices, the use of switching devices with two distinct states became prevalent and versatile. There were some initial efforts to develop multiple-state devices (e.g., Rutz commutating transistor), multiple-frequency oscillator concept of Edson, multiple-phase devices (e.g., the parametron), and multi-aperture square-loop ferrite devices, etc. A ternary computer named SETUN was built in 1958 [18]. During the 1960s, numerous other projects were

undertaken to manufacture ternary logic gates, arithmetic circuits, and memory cells. In 1973, a complete ternary machine named TERNAC and also a software emulator was designed [19]. With the arrival of BJT (Bipolar Junction Transistor) and later the MOS (Metal Oxide Semiconductor) transistors, these early developments in the field of multi-state devices faded away from academic research and industrial development arenas [20]. However, as the binary logic system is approaching the end-of-the-roadmap, there has been a renewed interest in exploring multiple-state devices for logic and memory applications. Compared to a binary logic system, the multiple-valued logic holds many advantages. It allows a single digit to contain more data than binary. Consequently, on- and off-chip wiring density would decrease, leading to smaller and simpler chips with lower pin-count. Table 1 shows the density of information that can be held by binary (2-valued), ternary (3-valued), and quaternary (4-valued) logic systems for different numbers of bit combinations.

Table 1: Table showing the density of information by 2, 3 and 4 valued logic

Highest Possible data that can be contained by:	Binary (R=2)	Ternary (R=3)	Quaternary (R=4)
1 bit	$2^1 = 2$	$3^1 = 3$	$4^1 = 4$
2 bit	$2^2 = 4$	$3^2 = 9$	$4^2 = 16$
3 bit	$2^3 = 8$	$3^3 = 27$	$4^3 = 64$
4 bit	$2^4 = 16$	$3^4 = 81$	$4^4 = 256$

For our general arithmetic and algebraic calculations, we use decimal or base ”10” number system, and for all digital applications, we now use binary or base ”2” system. Theoretically, the most appropriate base to work with is neither base ”2” nor ”10” [21]. For any numerical system, the number of digits required to express a specific value is

inversely proportional to the radix number. If *N* is the range of number, *R* is the radix, and *d* is the required number of digits, which is rounded to the subsequent integer value, then the relationship can be expressed by (1).

$$N = R^d \Rightarrow logN = d \times logR \Rightarrow d = \frac{logN}{logR} \tag{1.1}$$

The cost or the complexity of the system hardware *C* can be assumed to be proportional to the digit capacity *($R \times d$)*. Then from (1), it can be derived that,

$$C = k(R \times d) = k\left[R \times \frac{logN}{logR}\right] \Rightarrow C = k\left[R \times \frac{logN}{logR}\right] \tag{1.2}$$

Here *k* is the constant of proportionality. If the equation (2) is differentiated with respect to *R*, it can be shown that for the least value of cost *C*, radix number *R* is equal to *e = 2.72*. Considering the nearest integer to the value of *e*, it can be said that that *R = 3* or a ternary system would be more cost-effective than *R = 2* or a binary system. If under a different assumption, it is considered that *C* is independent of the system radix *R*, then (2) can be re-written as (3).

$$C = k \times d = k\left[\frac{logN}{logR}\right] \tag{1.3}$$

From (3), it is evident that the circuit cost or complexity *C* steadily decreases with the increase of radix *R*. Also, in this case, a ternary system is more cost-effective than a binary system [20]. At present, the MVL arithmetic circuits are not used in the industry directly. But the research in this field creates a path for an unforeseen opportunity. As most of the devices in the real-world are in binary nature, it might take some

time to be accustomed to the MVL system, but the concept of MVL is already introduced in several fields. In the sector of network routing [22] for IPv4 and IPv6, Ternary Content-Addressable Memories (TCAMs) have been used for decades [23]. Generally, the TCAMs are designed using conventional SRAM or DRAM with additional circuitry. Lately, large flash memories having multiple bits per cell have been realized [24]. The notion of communicating data using symbols that carry more than one bit of information has been used for a long time in wireless and in some wireline communication systems, which use large complex-valued signal constellations like QAM (Quadrature Amplitude Modulation) and QPSK (Quadrature Phase Shift Keying). Currently, this technique is being used to increase the speed of chip-to-chip and optical communications by using PAM (Pulse Amplitude Modulation) [24]. In the Ethernet protocol, M-ary PAM is already in use [11]. Another successful commercialization of MVL is the StrataFlash from Intel [25], [26].

1.2 Thesis Objective

A fair amount of work on Multiple-Valued Logic (MVL) has been done by different researchers because MVL technologies hold high potentials to significantly enhance the capabilities of the binary logic based circuits and systems. The scopes for MVL devices are profound and can be categorized into two primary approaches. The first approach uses multiple-valued logic as the background platform to solve binary problems more efficiently. The second approach is to design entirely new types of circuits and systems that would directly process and provide output signals with more than two unique

values. Researchers are exploring both prevailing and emerging device technologies for these two approaches. However, MVL technologies are expected to face some critical challenges. For example, with the continuous decrease of technology nodes that are operated at a lower voltage (around 1.2V as VDD and 0V as ground), it would be quite challenging to maintain three or more distinct voltage levels with sufficient intermediate voltage gaps to maintain multiple logic states under severe noise constraints. Considering the prevalence of MOSFET technology, it would be prudent to utilize it to implement higher radix systems while exploring completely new technologies for MVL systems. However, the interconnect-centric power, performance, and reliability limitations of MOSFET technology make it less appealing for MVL devices.

Carbon-based Field Effect Transistors (FETs) are drawing widespread attention due to their outstanding electrical properties and integration capabilities. Carbon-Nano-Tube-Field-Effect-Transistor (CNTFET) and Graphene-Nano-Ribbon-Field-Effect-Transistor (GNRFET) are the two forms of carbon-based transistor that have become trendy research topics. Different pieces of literature are found which work in CNTFET and GNRFET based ternary logic design [13], [27], [12], [28], [29] etc. which uses the threshold voltage control method for implementing different ternary logic circuits and arithmetic circuits. The circuit designs using CNTFET and GNRFET technology is similar to MOSFET based designs. Also, they offer faster simulation result, optimized power consumption and improved noise margin.

In our work, we have proposed different kinds of ternary logical, arithmetic and memory circuits using GNRFET and CNTFET. The scope of our thesis objective can be

categorized into:

1. Conducting an all-inclusive analysis and comparison of different prevailing and emerging technologies used in the field of developing MVL circuits

2. Proposing different basic logic gates like inverter, NAND, NOR gates using GNRFET

3. Proposing different arithmetic circuits like half-adder, decoder, multiplexer using GNRFET

4. Proposing different sequential circuits like latch and flip flop using GNRFET

5. Proposing a novel 3T Dynamic Random Access Memory or DRAM using CNTFET

6. Comparing the proposed design with different other state-of-the-art designs in terms of delay, power and transistor count

CHAPTER 2

FUNDAMENTALS AND SCOPE OF MULTIPLE VALUED LOGIC

2.1 Definition of of Multiple Valued Logic

The multiple-valued logic system is comprised of "R" distinct logic levels, where $R > 2$. The base 2 or binary numeric system has two distinct values known as "true and false" or"1 and 0" or "high and low". The MVL system may consist of a set of any number of logic levels that are represented by some signal variables, such as, current, voltage, or charge. These sets of values can be illustrated using any of the two conventions: unbalanced and balanced. An unbalanced system is the extension of the binary number system in a single direction, for instance, $0, 1, 2, 3, \cdots, (R-2), (R-1)$; and the balanced system needs an odd radix $R = 2K+1$, with the values $(-K), (1-K) \cdots -1, 0, 1 \cdot \cdot, (K-1), K$ [30].

According to the definition above, a ternary logic system would have three values to represent false, true, and undefined states [31]. Table 2 and Table 3 show the representation of basic unbalanced (0, 1, 2) and balanced (-1, 0, 1) ternary logic systems respectively.

Table 2: Logic levels for unbalanced ternary logic system

Logic level	Logic symbol
0	0
0.5*VDD	1
VDD	2

Table 3: Logic levels for balanced ternary logic system

Logic level	Logic symbol
- VDD	-1
0	0
VDD	1

Most of the recent research work, along with the designs proposed in our thesis paper works solely on unbalanced ternary system. Based on the operating principle, an unbalanced General Ternary Inverter (GTI) can be of three types: Negative, Positive, and Standard. A GTI is represented by (2.1)-(2.3), where x is the input and y_0, y_1, and y_2 are the outputs that represent a Negative Ternary Inverter (NTI), a Positive Ternary Inverter (PTI) and a Standard Ternary Inverter (STI), respectively [32]. The truth table that represents the functions, y_0, y_1, and y_2, is shown in Table 4.

$$y_0 = C_0(x) = \begin{cases} 2, & x = 0 \\ 0, & x \neq 0 \end{cases} \tag{2.1}$$

$$y_1 = C_1(x) = \begin{cases} 2, & x \neq 2 \\ 0, & x = 0 \end{cases} \tag{2.2}$$

$$y_2 = C_2(x) = \bar{x} = 2 - x \tag{2.3}$$

Table 4: Truth Table Representing NTI, PTI STI

Input	**STI**	**PTI**	**NTI**
0	2	2	2
1	1	2	0
2	0	0	0

A ternary function $f(X)$ containing n variables $\{X_1, X_2 \ . \ . \ . \ , X_n\}$ can be described as a logic function mapping from $\{0, 1, 2\}^n$ to {0, 1, 2}, where *X* = { X_1, X_2 . . . . , X_n}. The elementary algebraic operations of ternary logic can be described using (2.4)-(2.6), where, X_i, X_j = {*0, 1, 2*} [33].

$$X_i + X_j = max(X_i, X_j) \tag{2.4}$$

$$X_i \cdot X_j = min(X_i, X_j) \tag{2.5}$$

$$X_l = 2 - X_i \tag{2.6}$$

Here, + and . represents the OR and AND operations respectively and - represents the arithmetic subtraction. Table 5 shows basic ternary logic functions, such as NAND, AND, NOR, and OR.

Table 5: Truth Table Representing Ternary NAND, AND, NOR, and OR

Input 1	**Input 2**	**NAND**	**AND**	**NOR**	**OR**
0	0	2	0	2	0
0	1	2	0	1	1
0	2	2	0	0	2
1	0	2	0	1	1
1	1	1	1	1	1
1	2	1	1	0	2
2	0	2	0	0	2
2	1	1	1	0	2
2	2	0	2	0	2

2.2 Synthesis Techniques

For a multiple-valued logic system, the function minimization techniques become more complex with the increase of radix. In the case of ternary, the minimization is a little bit complicated than that of binary but the use of Karnaugh map (K-map) for binary can be extended to ternary with little modification. In [34], a method to minimize a ternary function with the help of a K-map is presented. From the half-adder truth table (Table 6), the K-map for the Sum and Carry of a ternary half adder can be derived as in Table 7 and

equations (2.7)-(2.8).

Table 6: Truth Table Representing a Ternary Half-Adder

Sum	**Carry**
0	0
1	0
2	0
1	0
2	0
0	1
2	0
0	1
1	1

Table 7: K-Map for Sum and Carry Signal of a Ternary Half-Adder

Sum			
X1\X2	0	1	2
0		1	2
1		2	
2	2		1

Carry			
X1\X2	0	1	2
0			
1			1
2		1	1

The equation for representing the sum and carry from the k-map is written as:

$$Sum = 2 \times (X_1^2 X_2^0 + X_1^1 X_2^1 + X_1^0 X_2^2) + 1 \times (X_1^1 X_2^0 + X_1^0 X_2^1 + X_1^2 X_2^2 \qquad (2.7)$$

$$Carry = 0 + 1 \times (X_1^2 X_2^1 + X_1^1 X_2^2 + X_1^2 X_2^2) \qquad (2.8)$$

Besides K-map, there are other synthesis techniques for MVL like Galois Field Polynomials, Arithmetic Polynomials, and Linear Cellular Arrays [35]. In Galois Field Polynomials, an arbitrary logic function with m-values and n-variables is characterized by

m^n different polynomial expressions or polarities, and an optimum representation is obtained. The coefficients of the polynomials can be attained with the help of direct and inverse Reed-Muller Transforms over Galois Field [35], [36], and [34]. Arithmetic Polynomial is similar to Galois Field Polynomials, where different polarities can also be obtained using direct and inverse arithmetic transform matrices. In Linear Cellular Arrays, the m-valued and n-variable logic function *f* is partitioned into a set of subvectors, then the multiple-valued variable is encoded into new binary variables called pseudo-variables and the function f is represented by an arithmetic expression based on those pseudo-variables [35], [34]. In [37], a mapping method is proposed in which the synthesis problem is formulated as a mapping from an input matrix to an output matrix. An approach for computing and analyzing MVL has been proposed in [35], which is applicable and adaptable to any multiple-valued function. The process can be divided into three different steps: domain selection, linear regression, and pattern matching for deriving selection criteria. In the domain selection stage, the domain for the input, and output and parametric constants are fixed. After the selection of domain, linear regression is carried out on the input combinations through which a linear equation is derived that fits the majority of function outputs. On the residual unmatched outputs, linear regression is done again so that a set of linear expressions is obtained. Once all the outputs of the functions are matched with a particular linear expression, this step continues. For the third stage, based on the sets of linear expressions obtained in Stage 2, individual selection conditions for individual expressions in the sets are derived. For a particular input combination, the hardware must

be able to select the correct linear expression from the sets, through the selection conditions derived, to obtain the correct output. It proposes a visual pattern-matching scheme for the derivation of the selection conditions. Besides all these above-mentioned methods, various other synthesis techniques are available [38], [39]. Several MVL synthesis tools and techniques have been proposed and tried out for years, for example, Multiple-Valued Sequential Interactive Synthesis or MVSIS [40] and ABC [41]. Another low-level language tool named BLIV-MV is also available which describes the MVL circuits in such a way that the logic synthesis tool can understand it [42].

CHAPTER 3

TECHNOLOGICAL ASPECT OF MULTIPLE VALUED LOGIC CIRCUIT

3.1 Different Technologies for Multiple Valued Logic (MVL)

The initial efforts to implement ternary and other MVL devices and circuits had been based on CMOS technology. Subsequently, many new initiatives have been started by the research community to explore MVL device and circuit implementations using Resonant Tunneling Diode (RTD), Single Electron Transistor (SET), Fin Field Effect Transistor (FinFET), Fully Depleted Silicon on Insulator (FDSOI), Quantum Dot Gate Field Effect Transistor (QDGFET), Carbon Nano Tube Field Effect Transistor (CNTFET), Graphen Nano Ribbon Field Effect Transistor (GNRFET), Memristor, Metal-Insulator Transition (MIT) material based memcapacitance technologies. In this section, a brief overview of various technologies and techniques for ternary logic design is provided.

3.1.1 Metal Oxide Silicon Field Effect Transistor or MOSFET

3.1.1.1 Operating Principle:

The main reason behind selecting MOSFET for ternary logic would be its simplicity and compatibility with the prevalent semiconductor process. Mouftah and Jordan (in 1974) and others (in later periods) demonstrated that binary CMOS circuits can be converted to ternary circuits with little effort and without requiring any new types of transistors [1,2,27,43,44]. The threshold voltages of MOSFET can be easily changed during

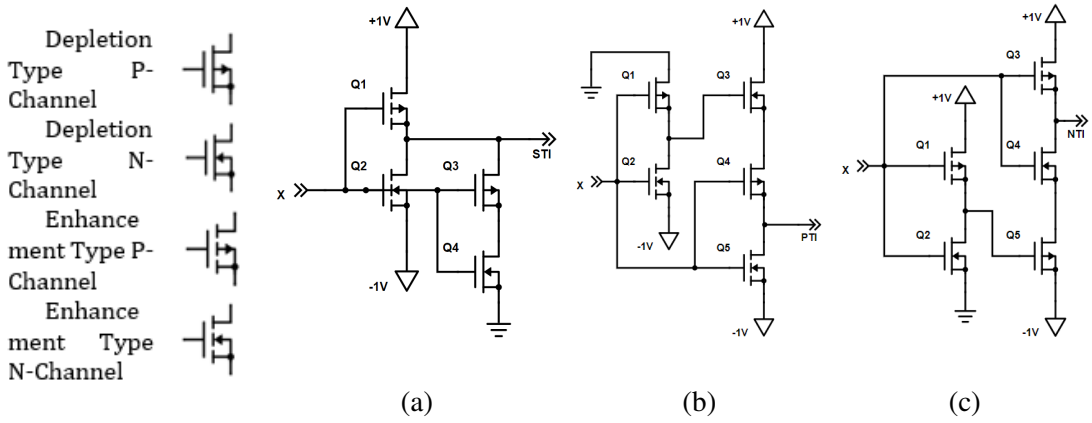


Figure 1: Schematic diagram of (a) STI, (b) PTI, and (c) NTI [1]

the fabrication process, which can be used as a means to create multiple voltages or current levels required in the MVL device. Two different techniques have been explored in this regard. The first one is to use a combination of enhancement and depletion type of MOSFETs in the same circuit [1], [27], [45] and the second one is to use only enhancement type MOSFETs along with some resistors to implement a voltage divider to obtain multiple voltage levels [2], [44].

Fig. 1 shows the circuit diagrams of the STI, NTI, and PTI, respectively implemented using the first technique [1]. For the STI, the output shows a balanced standard ternary inverter, i.e. for the input logic level of 1, 0, and -1, the output will have a value of -1, 0, and 1, respectively. When the input is of high value (logic 1), *Q1* will be off whereas *Q2* will be on; and *Q3* will be off though *Q4* will be on. This setup will keep the output node at a low value (-1V). For the low input voltage (logic -1), *Q1* and *Q3* remain on, whereas, *Q2* and *Q4* become off and the output becomes high. For an intermediate input value, *Q1* and *Q2* will remain off and *Q3* and *Q4* will be on, thus connecting the output to the ground (logic 0). The condition for the STI circuit to work is as shown in

(6), where $\pm V$ = value of the power supply, V_T = threshold voltage of the enhancement MOS transistors, and V_P = pinch-off voltage of the depletion devices.

$$V < V_T < 2 \tag{3.1}$$

$$0 < V_P < V \tag{3.2}$$

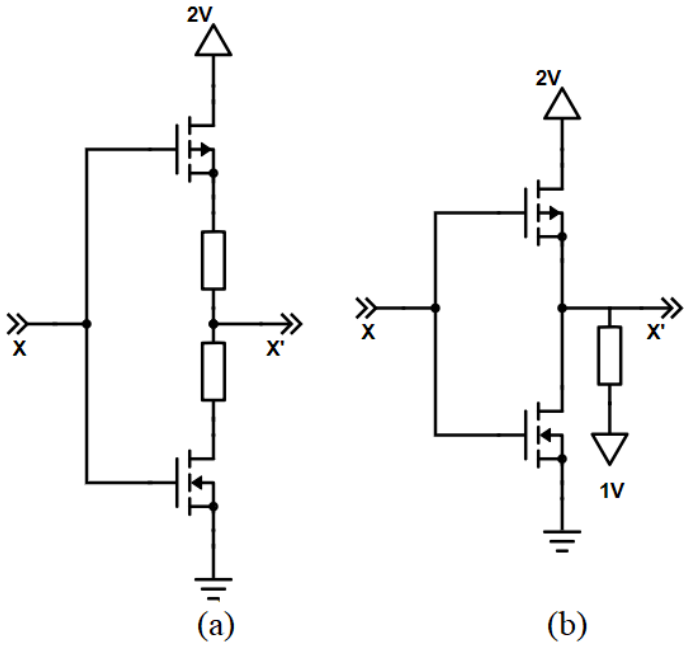


Figure 2: Standard Ternary Inverter using (a) two resistors (b) one resistor [2]

Fig. 2 shows the ternary circuits with only enhancement type MOSFETs and resistors. Here, resistors are inserted in between the transistors to get the required intermediate voltage level [2]. Fig. 3 shows the DC transfer characteristics of the circuit of Fig. 2. The same circuit can be constructed without using the resistors and controlling the threshold voltage [32]. All these techniques and circuits can be extended to implement ternary NAND, NOR, ALU, adder, multiplier, etc. complex circuits [1], [27], [32], and [46].

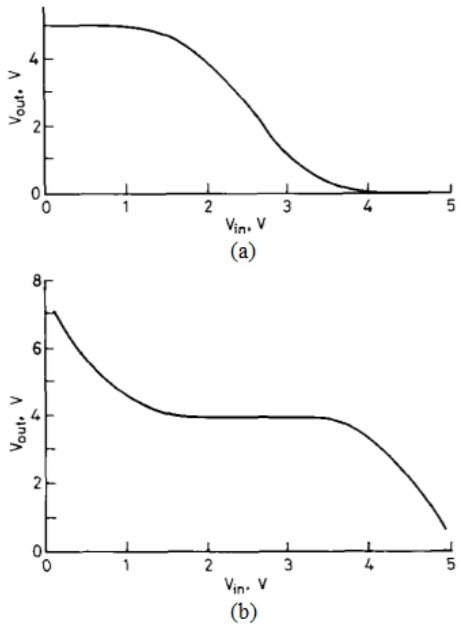


Figure 3: (a) Transfer characteristics with two resistors (b) Transfer characteristics with one resistor [2]

3.1.1.2 Analysis:

Among all the technologies, MOSFET is the oldest one to be explored for the MVL device, mainly because MOSFET based MVL devices would be compatible with the current process. The prevailing binary CMOS circuits can be modified into ternary circuits with a new type of transistor. As threshold values of MOSFET transistors are easily changed during the fabrication, multiple voltage or current levels can be created. In a current-mode circuit, logic levels are usually defined by different currents which are the integer multiples of the reference current. Currents are possibly being scaled, copied, and algebraically sign changed by the simple current mirror. Frequently used Linear-sum operation can be performed by wiring, which results in the reduced number of active devices in the circuit. Many prototype chips of the current-mode CMOS circuits have fabricated in the past showing better performance as compared to the corresponding binary-circuits [47–49]. It is to be believed that current-mode designs provide a much better noise margin than voltage-mode CMOS design. Some of the major benefits of binary CMOS logic are zero-static power dissipation for stable states and almost similar output impedance in either state. However, in the CMOS MVL circuits, these positive properties are not achievable. CMOS MVL circuits are generally categorized by rail-to-rail current flow in one or more than one static state and the higher output impedance in 1 state as compared to other states. There have been two solutions proposed to these problems recently. In the current-mode CMOS Multiple-Valued Logic circuits, dual-rail source-couple logic is introduced [48]. The use of complementary input pairs and the source-coupled logic allows high-speed circuits with lower power dissipation. Another alternative solution is,

where the low-power and low-voltage, current-mode MVL circuits are to be designed by using the neuron-MOS transistor. Another major problem with CMOS MVL circuits is unlike Binary CMOS circuits, they are not self-restored. The level restoration circuit has to be utilized for every block of a certain number of stages for recovering signals. To solve this problem the new self-restored architecture is presented, which uses both voltage-mode binary circuit and current-mode MVL circuit to implement MVL functions and to restore the output signal simultaneously [48]. Binary gates are to be used within design architecture so that the binary-MVL or MVL-binary conversion circuits are not necessary to interface with binary circuits. The average size of resulting circuits is around 50% smaller than previously proposed MVL circuits, whereas average power dissipation and time delays are comparable. The voltage-controlled CMOS MVL circuits are expected to share the three key advantages of the CMOS binary circuits - 0 static power dissipation in stable states, low output impedance in stable states, and the elimination of the passive elements (resistors). Any multiple-valued signal can be transmitted through a CMOS transmission gate. In contrast with the bipolar junction transistors, the ability to change the threshold voltage of the MOS transistors simplifies the task of responding to a multilevel input signal. The first CMOS ternary circuits were proposed in 1974. Since then, a lot of novel work has been done with a different perspective for the implementation of CMOS based ternary circuit design.

With the continuing scaling of CMOS technology, different short dimension effects are introduced such as Carrier velocity saturation and mobility degradation, Drain

Induced Barrier Lowering (DIBL), punch-through, hot carrier effects, etc [9]. If the channel length is small enough to compare with the source and drain depletion region, the magnitude of these short channel effects increases manifold. Due to these effects, the leakage current flows more easily through the channel and the turning off the transistor becomes difficult. That is why newer designs involving newer methods and emerging technologies are sought by researchers to alleviate the challenges.

3.1.2 Resonant Tunneling Diode (RTD) based Ternary Logic

3.1.2.1 Operating Principle:

A Resonant tunneling diode is a device in which there are different semiconductor materials, which are present in alternate layers. Tunneling of electrons through different resonant states at certain energy levels causes the flow of current inside the device. The current-voltage (I-V) curve of an RTD demonstrates the negative differential resistance (NDR) feature. The decreasing part of the current curve with respect to the voltage gives rise to the negative differential resistance. This characteristic is very crucial to the circuit implementation as it can offer different voltage-controllable logic levels corresponding to the peak and valley currents. It consists of two heavily doped contacts made of a semiconducting material with a narrow energy gap (e.g. GaAs). These two contacts constitute the emitter and collector region. In between them, there are two barriers made of a comparatively larger bandgap material (e.g. AlGaAs). These two barriers encompass a quantum well, which is made of a relatively smaller bandgap material as shown in Fig. 4 [3]. This type of structure is called a Double Barrier Quantum Well (DBQW) structure. Before

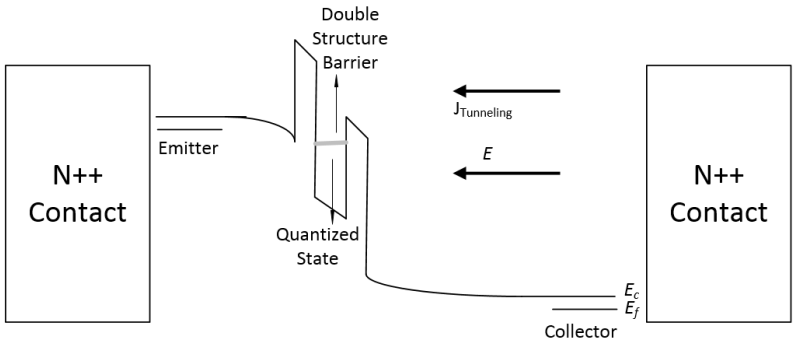


Figure 4: Resonant Tunneling Diode operation. The shaded region in the double-barrier structure represents the quasi-bound state in the quantum well [3]

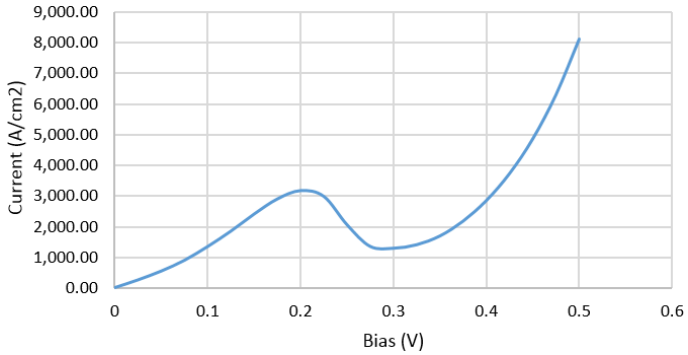


Figure 5: RTD I-V characteristics

applying any forward bias, the majority of the electrons and holes create an accumulation layer in the emitter and collector region, respectively. With the application of a forward voltage bias, an electric field is generated. This field forces the electrons to travel from the emitter region to the collector by the process of tunneling through the scattered states inside the quantum well. Due to the tunneling of electrons through these quasi-bound energy states, a current is created. As the number of electrons in the emitter with the same energy as the quasi-bound state increases, more electrons become able to tunnel

through the quantum well. This results in an increase of current corresponding to the applied voltage. At a particular point, the energy level of the emitter electrons matches the energy level of the quasi-bound state. At that point, the current reaches its' maximum value and resonant tunneling is said to happen. The occurrence of the resonant tunneling is observed at a certain resonant energy level, which depends on the corresponding doping level and the quantum well width. As the applied bias keeps on increasing, more electrons obtain too much energy than the energy of the quantum well and the amount of current starts decreasing. After reaching a specific applied voltage, the current rises again due to the substantial thermionic emission where the electrons can tunnel through the non-resonant energy levels as well. The current at the minimum valley is termed as leakage current. This phenomenon is demonstrated in Fig. 5 which was drawn using a simulation tool in nanoHUB [50]. Different ternary and quaternary logic gates and memory devices have been proposed using different circuitry [4, 51, 52]. Among all of these, a very famous technique is the use of different combinations of up and down literals to produce multiple-valued outputs. These literals can be obtained by using circuits called monostable-to-bistable transition logic elements (MOBILE) [4], [53]. Two RTD's connected in series combination creates a MOBILE, as shown in Fig. 6. Here, *X* has a gate that can module the peak current by controlling the voltage. The output voltage curve for the respective input voltage can be seen in Fig. 7b. V_1 is considered for low voltage and V_2 is for high voltage. When V_{CLOCK}=V_1, both the RTD's are ON and the circuit is in the monostable state. When V_{CLOCK}=V_2, the circuit transfers to a bistable state. V_2 is selected in such a way that either *A* or *X* switches to OFF state from ON state when V_{CLOCK}

is set to V_2. Depending on the ON and OFF states of *A* and *X*, high or low voltages can be seen in the output.

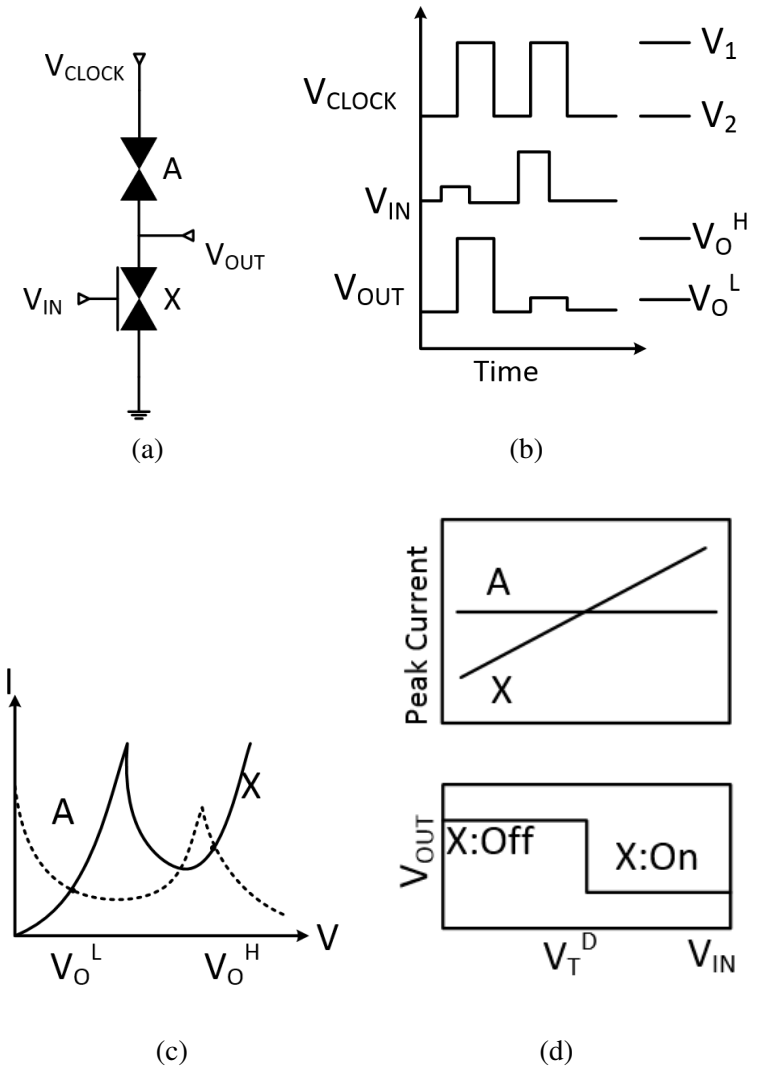
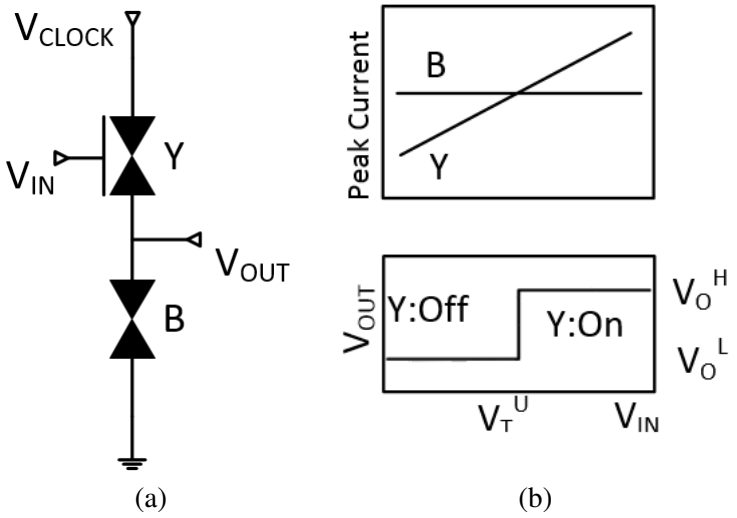


Figure 6: (a) Circuit diagram of a down literal MOBILE, (b) Voltage vs time graph of the operation, (c) current-voltage curve showing the bistable state and (d) peak currents as a function of the input voltage [4]

Here, the peak current of *X* increases with an increase in gate voltage V_{IN}. If $V_{IN} < V_{TD}$, the peak current of *X* is less than the peak current of *A*, which changes the

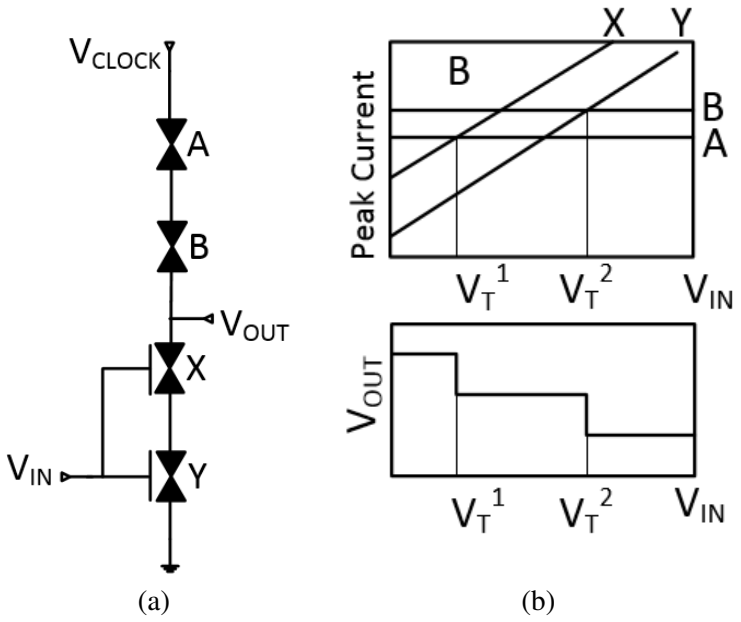
state of *X* from ON to OFF. Thus the output voltage is found to be V_{OH} (High). Again, when $V_{IN} > V_{TD}$, the peak current of *A* is smaller than that of *X*. For that, *A* switches to OFF state making the output V_{OL} (low). Similarly, an up literal can be obtained in a manner shown in Fig. 7.



(a) (b)

Figure 7: (a) Circuit configuration of an up literal MOBILE. (b) Peak currents as a function of input voltage and transfer characteristics of up literal [4]

By combining these up and down literals any transfer characteristics with multiple thresholds and multiple outputs can be presented. In [4], a ternary inverter was proposed using the combination of two down literals. In Fig. 8a, the circuit configuration of a ternary inverter using only down literals is given. Here, one down literal is comprised of *A* and *X* with a threshold voltage of V_{T1}, and another pair of is consisted of *B* and *Y* which has the threshold voltage V_{T2}. Peak current of *A* is smaller than the peak current of *B*. When V_{CLOCK}=V_2 (high), and V_{IN}¡V_{T1}, the output is at the highest value (2). When $V_{T1} < V_{IN} < V_{T2}$, *A*, and *Y* are switched off which results in an intermediate output voltage (1). For $V_{IN} > V_{T2}$, *A* and *B* are switched off and the output becomes low (0).



(a) (b)

Figure 8: (a) Circuit configuration of an up literal MOBILE. (b) Peak currents as a function of input voltage and transfer characteristics of up literal [4]

Table 8: Operating conditions of a ternary inverter

V_{IN}	Switched OFF RTDs	V_{OUT}
$V_{IN}<V_{T1}$	X, Y	2
$V_{T1}<V_{IN}<V_{T2}$	A, Y	1
$V_{IN}>V_{T2}$	A, B	0

The operating conditions and different states are summarized in Table 8.

Along with basic gates, complex ternary gates using RTD have been proposed in different literature, for example, adder [51], Analog-to-Digital converter [52], predecoder [54], Programmable Logic Array or PLA [55], etc. Few other ways combine the RTD with some other technologies like HEMT (High Electron Mobility Transistors), HBT (Heterojunction Bipolar Transistor), or MODFET (Modulation Doped field-Effect Transistor) to produce multiple-valued logic circuits [4], [56].

3.1.2.2 Analysis:

Due to the lack of suitable dedicated devices, Multiple-valued logic circuits have not been extensively established commercially by the industry. Most of the multiple-valued circuits are of the threshold type which uses conventional active devices such as bipolar transistors or field-effect transistors. Similar to analog circuits, these threshold type circuits also suffer from the same type of limitations in terms of noise margin and circuit complexity, which usually slows down the circuit operation. Whereas the resonant tunneling diodes (RTD) possesses some unique characteristics like folding I-V characteristics and high-speed operation owing to the tunneling effect. Due to these unique characteristics, RTD is considered to be a viable candidate for multiple-valued digital applications [51]. Though RTD holds a major possibility in the field of multi-valued logic, recent works on these are very rare. Most of the works regarding RTD based MVL are date in the '90s. The need for completely new circuitry and technology might be the reason for it. There are few instances of literature work in the field of RTD fabrication though it is not mature enough to reach the full potential. Very precise thickness control is required to ensure the uniformity through the whole wafer. The output power of RTD is also limited which requires an amplifier or other drivers [3].

3.1.3 Single Electron Transistor based Ternary Logic

3.1.3.1 Operating Principle:

Single Electron Transistor or SET is such a device, which is based on Coulomb Blockade Effect. A SET comprises of two electrodes that work as the drain and the

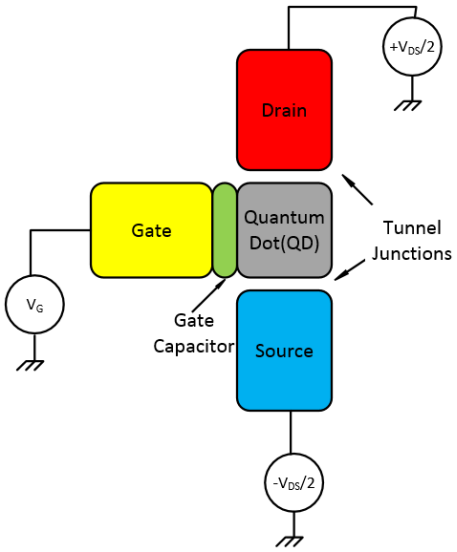


Figure 9: Single Electron Transistor [5]

source. These electrodes are connected through tunnel junctions to a Quantum Dot (QD), which is also called the island. A third electrode, known as the gate, which is capacitively coupled to the island can be used to control the electrical properties of the island. The structural diagram of a SET can be seen from Fig. 9 [57].

Fig. 10 shows the working principle of a SET in terms of energy levels. In the absence of an applied external bias (Fig. 10a), a blocking state prevails. Here, no available energy levels of the island are in the range of tunneling for the electrons in the source contact (in red). All the available or lower energy levels are occupied beforehand. Upon application of a positive voltage (Fig. 10b), the energy levels are lowered for the island electrode. At that point, the emitter electron (green 1) can tunnel through a previously vacant energy state of the island (green 2) to the drain electrode (green 3). Here it inelastically scatters and moves to the drain electrode Fermi level. The separation between the

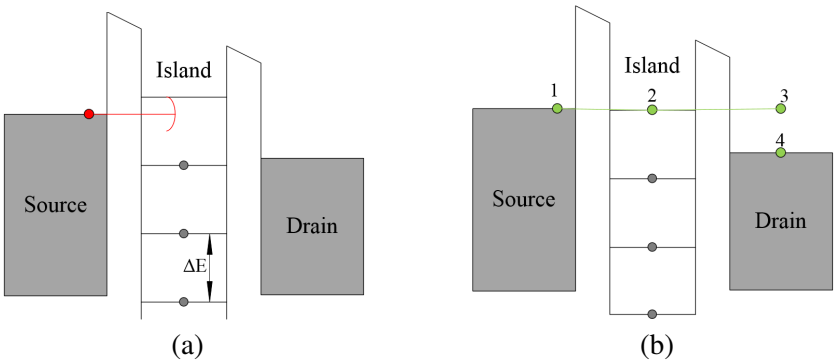


Figure 10: Left to right: energy levels of source, island and drain in a single-electron transistor for the (a) Blocking state and (b) Transmitting sate [5]

energy levels of the island electrode is ΔE which gives rise to a self-capacitance *C* of the island, which can be defined by (7).

$$C = \frac{e^2}{\Delta E} \tag{3.3}$$

One of the key characteristics of a SET device is the possibility to include multiple gates that provide options to have an adjustable threshold voltage. Fig. 11 demonstrates a dual gate SET, where C_{g1} and C_{g2} are the gate capacitances of gate 1 and gate 2, respectively, and C_D and C_S are the tunnel junction capacitors of the drain and source. One gate is used as the voltage input port and the other gate is defined as the threshold voltage adjusting port. The inputs for these two gates are V_{in} and V_{con}, respectively. The voltage on the island V_{island} controls the current flowing through two tunnel junctions and can be represented by (8).

$$V_{island} = \frac{1}{C_{\Sigma}}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne) \tag{3.4}$$

Here, $C_{\Sigma} = C_{g1} + C_{g2} + C_D + C_S$ and *n* is the number of electron on the island [58]. Considering the inherent threshold voltage of the island to be V_{th}, the condition for turning

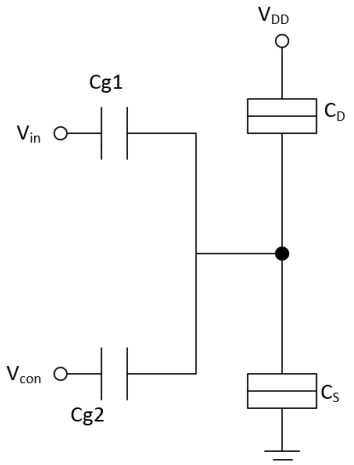


Figure 11: Dual gate SET [6]

the SET on is:

$$\mathrm{V}_{island} > V_{th}$$

$$\Rightarrow \frac{1}{C_{\sum}}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne) > V_{th}$$

$$\Rightarrow V_{in} > \frac{C_{\sum} V_{th} - C_{g2} V_{con} - C_D V_{DS}}{C_{g1}}$$

Hence, the gate threshold voltage can be defined by (10).

$$V_{in}^{'} > \frac{C_{\sum} V_{th} - C_{g2} V_{con} - C_D V_{DS}}{C_{g1}} \tag{3.6}$$

Using the concept of SET, a design is proposed in [6] to implement basic ternary gates. Here, two different SET with two different threshold voltages V_{th1} and V_{th2} are used. The input voltage level is set in such a way that the voltage less than V_{th1} is considered to be logic â0â, the voltage higher than V_{th2} is considered to be logic â2â. And the intermediate voltage between V_{th1} and V_{th2} is considered to be logic â1â. In [59], new designs of ternary logic gates and ternary adder are proposed by merging the SET and MOS transistors.

More arithmetic circuits like an adder, multiplier, etc. circuits using are proposed in [60], [61]. Some quaternary logic gates along with quaternary memory cells are proposed in [62].

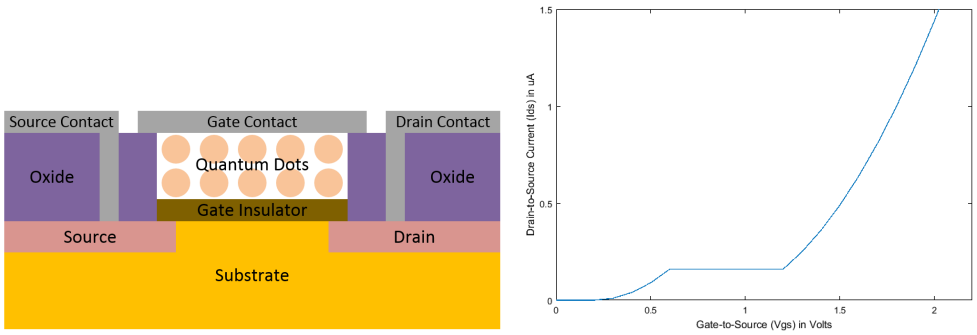
3.1.3.2 Analysis:

SET offers very low power consumption, compact size, high operating speed, simpler circuits and operation, and straight to the co-integration with the traditional CMOS circuit [53]. The use of multiple gates makes it possible to have a variable threshold voltage that can be used for the design of MVL. To operate the SETs at the room-temperature large quantities of the monodispersed nanoparticles (lesser than 10nm in the diameter) should be synthesized. However, as it is very difficult to fabricate the large quantities of SETs using traditional optical lithography and semiconductor processes. It is also very difficult to fabricate the SETs and link the SETs with the outside environment [63]. The major drawbacks are poor current drive capability as compared to CMOS devices and the need for low-temperature operation [64]. Also, the background charge problem is another major downside.

3.1.4 Quantum Dot Gate Field Effect Transistor based Ternary Logic

3.1.4.1 Operating Principle:

A quantum dot is a minuscule configuration of electrons enclosed in a three dimensional potential well and the size of the well is in the range of the size of de Broglie wavelength of electrons. Any quarantined atom or a multimolecular collection of atoms



(a) (b)

Figure 12: (a) Structural diagram of QDGFET [7], (b) IDS vs VGS in QDGFET

can also be called quantum dots. A quantum dot exhibits similar discrete, quantized energy levels like an atom and sometimes called an ”artificial atom”. By controlling the dimension of the quantum dots, the energy levels can be modified.

The structure of the Quantum Dot Gate Field Effect Transistor (QDGFET) is similar to the MOSFET and can be fabricated using the conventional CMOS fabrication process that makes this technology more practical and appealing [65]. In a QDGFET, on top of the gate oxide layer, there are two layers of quantum dots (QDs). Upon application of a gate voltage, the charge carriers from the inversion channel move through the gate insulator to the QD layers through resonant tunneling, thus creating a new intermediate state in between the two stable states. The device structure of a QDGFET is shown in Fig. 12a.

The QDs which are deposited in the gate area is comprised of nanocrystals of silicon (Si) or geranium (Ge) which are cladded by their oxide. Due to the presence of tunnel oxide enclosing the semiconductor nanocrystal, the charge leakage is reduced [66]. For a QDGFET, when gate voltage V_{GS} is increased, due to the effect of resonant

tunneling, the threshold voltage V_{th} also increases, keeping the overdrive voltage $V_{GS}-V_{th}$ constant. The threshold voltage of a QDGFET can be expressed with (11) [65].

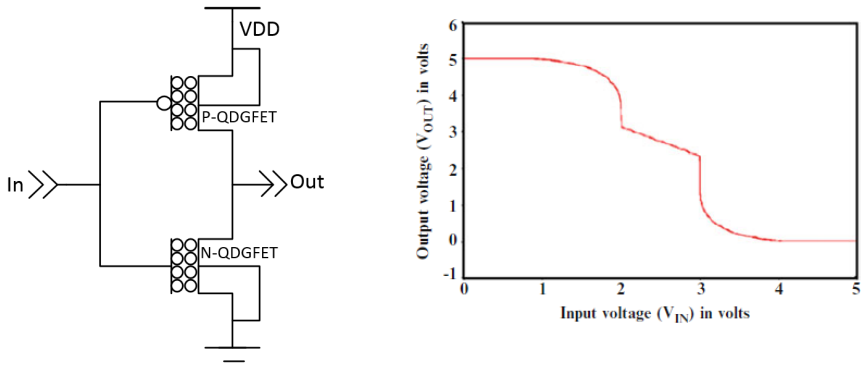
$$V_{Teff} = \begin{cases} V_T, & V_{GS} < V_{g1} \\ V_T + \alpha(V_{GS} - V_{g1}), & V_{g1} < V_{GS} < V_{g2} \\ V_T + \alpha(V_{g2} - V_{g1}), & V_{GS} > V_{g2} \end{cases} \tag{3.7}$$

Where V_{g1} and V_{g2} are respectively the lower and upper threshold voltage of the intermediate state and they are dependent on device structure. Within the range of V_{g1} and V_{g2}, the threshold voltage changes linearly with the gate voltage, and the rate of linearity depends on the value of α. When α=0, the device acts as a simple FET, and for α=1, the threshold voltage changes linearly with V_{GS}. The value of α can be controlled by changing the thickness of the insulator or by changing the size and number of dots [7]. And the drain current equation is [65]:

$$I_D = \begin{cases} 0, & V_{GS} < V_{Teff} \\ \frac{W}{L} C_o \mu (V_{GS} - V_{Teff} - \frac{V_{DS}}{2}) V_{DS}, & V_{DS} < V_{GS} - V_{Teff} \\ \frac{W}{L} C_o \mu \frac{(V_{GS} - V_{Teff})^2}{2}, & V_{DS} > V_{GS} - V_{Teff} \end{cases} \tag{3.8}$$

The graph derived from the drain current equation is shown in Fig. 12b. Fig. 13 shows a CMOS representation of a standard ternary inverter using QDGFET and its transfer characteristics.

Similarly, ternary NAND, NOR, etc. basic gates along with some combinational circuits have been designed using QDGFET in [65], [66]. Being similar in the circuit diagram and fabrication process, QDGFET based ternary circuits can be easily produced by prevailing binary logic gate architecture.



(a) (b)

Figure 13: (a) STI using QDGFET (b) Transfer characteristics of QDGFET based STI [8]

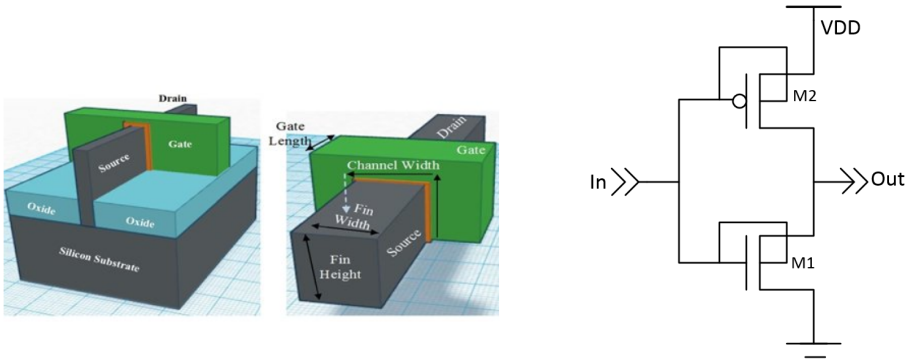
3.1.4.2 Analysis:

Quantum Dot Gate Field Effect Transistor (QDGFET) has a similar structure and operating principle to the SET. However, unlike SET, QDGFET does not suffer from the background charge problem. Moreover, it can be designed in the same way as the CMOS, reducing the design complexity to implement MVL logic. Despite all the advantages, more research is needed to be done in the field of QDGFET to come to a secure conclusion. A limited number of literature is found on the fabrication as well as the circuit development of QDGFET.

3.1.5 Fin Field Effect Transistor based Ternary logic

3.1.5.1 Operating Principle:

Whenever a lower node technology is introduced, it introduces different kinds of short dimension effects like carrier velocity saturation and mobility degradation, Drain Induced Barrier Lowering (DIBL), punch-through, hot carrier effects, etc. In a conventional CMOS system, the gate has lower control of the channel as it is situated far from



(a) (b)

Figure 14: (a) FinFET Structure [9] (b) FinFET based STI [10]

the channel. One way to alleviate this situation is to make the channel above the substrate making a fin-like structure. The gate is wrapped around the fin-shaped channel giving better control of the channel. This gives rise to a vertical channeled device called FinFET in contrast to the horizontal channel of planer MOSFET. For FinFET, the height of the fin plays a crucial role in determining the channel width. The channel width L for FinFET can be derived using (13) [9].

$$L = 2 \times Fin_{Height} + Fin_{Width} \tag{3.9}$$

FinFET can also be used to design ternary logic circuits. However, there are very few efforts to implement FinFET based ternary logic. In terms of the working principle, the FinFET is identical to the conventional MOSFET. Therefore, the ternary or other multiple-valued logic implemented using FinFET would have a similar operating principle. However, due to better gate control in FinFET, it is anticipated that FinFET based MVL would be more reliable compared to the conventional MOSFET based MVL. Some of the ternary logic and adder designs based on FinFET are illustrated in [10, 67, 68].

3.1.5.2 Analysis:

FinFET devices are introduced by the industry to address the challenges associated with lower-node planar MOSFET technology. FinFET is a very promising and the latest mass-produced Si-based transistor used in the production of microprocessor type VLSI circuits and systems. FinFETs have significantly better performance in terms of V_{th}, speed, and leakage because of the major geometrical change in the design of the channel. The increased control over the channel region through the wrapped up gate [69], the use of multiple-gate, body biasing, multiple supply voltages [70], etc. gives a better threshold voltage control in FinFET devices which can be utilized to implement MVL devices. FinFETs are 3-D structures that need high aspect ratio etching with the non-uniform pitches or locally varying pitches which is complex. Thus, FinFETs possess significant numbers of Restricted Design Rules (RDR). The body biasing techniques are commonly used in planar which are less effective in FinFETs due to fully-depleted channels. Accurate FinFET parasitic extraction is more complicated [71].

3.1.6 Fully Depleted Silicon on Insulator based ternary logic

3.1.6.1 Operating Principle:

Fully-Depleted-Silicon-On-Insulator, or FD-SOI, is a planar process technology which differs from a bulk-CMOS process in terms of an ultra-thin layer of insulator called the buried oxide which is insulated from the channel. In an FDSOI, this oxide layer is placed on top of the base silicon. And then a very thin silicon film creates the transistor channel. As the silicon layer is very thin, no doping is needed for the channel which makes

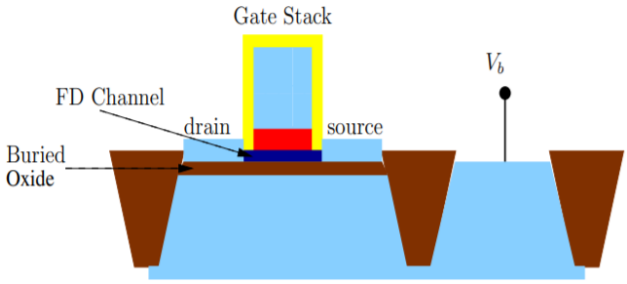


Figure 15: Structural Diagram of an FDSOI [11]

the transistor fully depleted [72]. The structural diagram of an FDSOI is given in Fig. 15. The advantages of a standard FDSOI are: Superior Junction capacitance, Higher Electrostatic control of the channel in comparison to bulk CMOS, better threshold voltage (V_{th}) variation as the channel is not doped [73]. The transistor can be controlled through two independent gates. By the process of Reverse Body Biasing (RBB), the threshold voltage can be controlled to a great extent, which is not possible for bulk CMOS [11].

The technique of threshold voltage control enables FDSOI to be tried in the field of multiple-valued logic. Few literatures is present on the sector of FDSOI based MVL design [73], [74], [25].

3.1.6.2 Analysis:

FDSOI devices are one of the possible solutions for the scaling effects of conventional MOS technology. In the conventional MOS device, as the channel length shrinks, the gate cannot fully control the channel. This results in an increased sub-threshold leakage between drain and source. The structure of an FDSOI ensures more control of the gate over the channel which results in lower leakage current [69]. One of the disadvantages

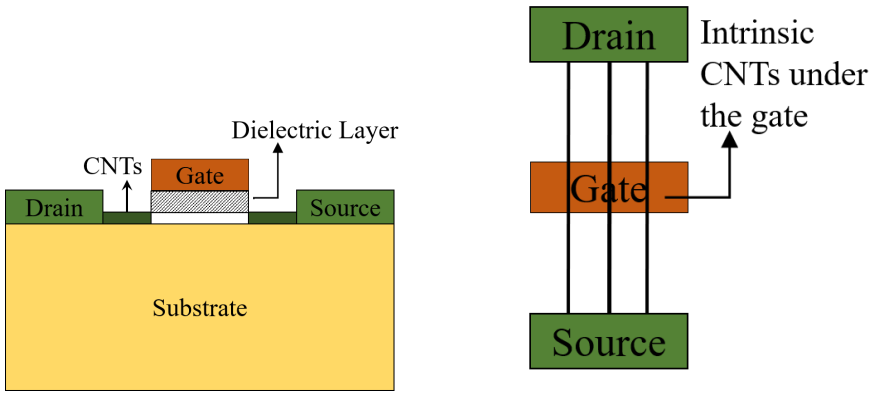


Figure 16: (a) Cross section view (b) Top view of a CNTFET structure

of the SOI device is self-heating. In FDSOI, the active thin body which is comprised of silicon oxide is a good thermal insulator. The power consumed by the active region during operation cannot dissipate easily. This effect increases the temperature of the thin body which in turn reduces the mobility of the device. Another disadvantage of FDSOI is the difficulty of fabricating the thin body wafers [9]. Similar to FinFET, FDSOI fabrication technology is very matured and started to appear at an industrial level. But in the case of FDSOI based MVL designs, most of the works done are very recent and at an initial stage.

3.1.7 Carbon Nano Tube Field Effect Transistor based ternary logic

3.1.7.1 Operating Principle:

Carbon Nano Tube (CNT) is made of a rolled-up graphene sheet. The rolling angle of the graphene sheet is known as chirality, which defines the behavior of the CNT's. Depending on the chirality vector (two variables, n, and m, are commonly used to represent the chirality), a CNT can act as a metal or semiconductor. If n=m or n-m=$3i$ (where

i is an integer value) the CNT provides metallic behavior and if *n-m¿3i* the CNT shows semiconducting behavior. For a single-walled CNT, the relationship between the chirality (*m,n*) and tube diameter (D_{cnt}) can be expressed as in (3.10).

$$D_{cnt} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \tag{3.10}$$

Here, *a=2.49 A*°, which is the interatomic distance between two neighboring atoms. The chiral angle can be defined as in (3.11) [75].

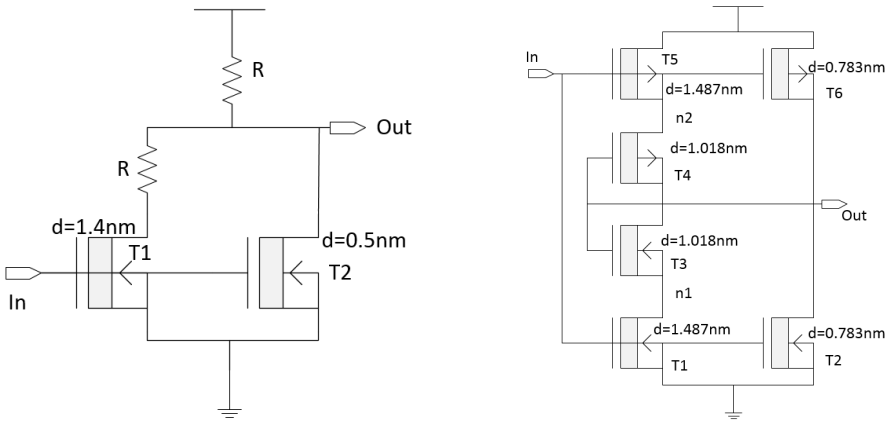
$$\theta = tan^{-1}\frac{\sqrt{3}n}{2m + n} \tag{3.11}$$

There exists quite a similarity between I-V characteristics of a CNTFET and a MOSFET. The threshold voltage of a device can be described in terms of the voltage required to turn the device ON. In the case of the CNTFET, the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half-bandgap that is an inverse function of the diameter [13].

$$V_{th} \approx \frac{Eg}{2e} = \frac{aV\pi}{3 * eD_{cnt}} \tag{3.12}$$

The parameter Vπ (3.033 eV) is the carbon π-π bond energy in the tight bonding model, *e* is the unit electron charge, and D_{cnt} is the diameter of a CNT. For a chirality vector of (19,0), the D_{cnt} is found to be 1.487 nm. Putting all the values in (16), V_{th} is found to be 0.293V. Considering *m* in the chirality vector to be 0, it can be derived from the (3.10) and (3.12), that the threshold voltage of the CNTFET is inversely proportional to the diameter of the CNT as well as the chirality vector*n* if the CNT.

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{cnt2}}{D_{cnt1}} = \frac{n_2}{n_1} \tag{3.13}$$



(a) (b)

Figure 17: Design of CNTFET based inverter (a) [12] (b) [13]

Fig. 16 gives a structural diagram of a CNTFET. Like a conventional CMOS, CNTFET also has four terminals. Here, the channel region is consisting of an undoped semiconducting carbon nanotubes or CNTs which is present under the gate region. And some heavily doped CNT segments are placed between gate and source/drain to permit for a low series resistance in the on-state.

The main advantage of using CNTFET in a logic circuit is the opportunity of using transistors with different threshold voltage in the same circuit. Using this concept, two different standard ternary inverters (STI) were proposed in [12] and [13], which has their own merits and demerits. The proposed design in [12] and [13] is shown in Fig. 17a and 17b respectively. In Fig. 17a, two CNTFETs with diameter d_1=1.4nm and d_2=0.5nm are used. As a result, the threshold voltages of the two CNTFETs are V_{th1}=300mV and V_{th2}=840mV respectively. Two resistors both with the value 100kΩ are used. When the input voltage is less than 300mV, both the transistors are in off-state and the output voltage is equal to V_{dd} (1.5V). For input voltage greater than 300mV, transistor *T1* becomes on

and the output voltage reaches the value near to V_{dd}/2. As input voltage becomes equal to V_{th2}, the second transistor is turned on and the output reaches an almost zero state. The proposed design in [13] uses 6 transistors which can be observed from Fig. 17b. The properties of the 6 transistors are given below:

- The chiralities of the CNTs used in *T1/T5*, *T2/T6* and *T3/T4* are (19, 0), (10, 0), and (13, 0), respectively.
- The diameters of *T1/T5*, *T2/T6* and *T3/T4* are 1.487, 0.783, and 1.018 nm, respectively.
- The threshold voltages of *T1*, *T2*, and *T3* are 0.289, 0.559 and 0.428 V, respectively.
- The threshold voltages of *T5*, *T6*, and *T4* are â0.289, â0.559, and â0.428 V, respectively.

As the input voltage is increased from low to high (low being 0V and high being 0.9V), primarily the input voltage is lower than 300 mV. This turns ON both the transistors *T5* and *T6*, and both *T1* and *T2* are turned OFF; the output voltage is 0.9 V, i.e., logic 2. When the input voltage rises to a value greater than 300 mV, *T6* is OFF and *T5* is still ON and *T1* is ON and *T2* is OFF. The diode connecting the CNTFETs *T4* and *T3* generates a voltage drop of 0.45V in-between node *n2* and output and in between output and node *n1* due to the threshold voltages of *T4* and *T3*. Therefore, the output voltage takes a value of half of the power supply voltage, i.e., 0.45 V. From Table 2, it is seen that half V_{dd} represents logic 1. Once the input voltage goes above 0.6 V, both *T5* and *T6* are OFF,

and *T2* is ON to pull the output voltage down to zero. The transition from high to low is similar to the low to high transition. Besides this, there is another 6 transistor-based design for the ternary inverter which has been used by much other literature [76]. Based on the above-mentioned techniques, different other logic gates such as NAD, NOR, XOR can be constructed. Besides these, several other complex arithmetic circuits like the adder, multipliers, etc. are also proposed in [33], [77–81].

3.1.7.2 Analysis:

Carbon-Nanotube Field Effect Transistor (CNTFET) has characteristics which are qualitatively like silicon MOSFETs, and therefore, most of the conventional MOSFET circuits can be converted to CNTFET based designs [82]. CNTFET's are a promising alternative for traditional bulk silicon-based MOSFET for the high-performance and low power designs because of its ballistic transport and low OFF-current properties. Also, in a CNTFET threshold voltage (V_{th}) is determined by CNT diameter; therefore, the multi-threshold design is accomplished by utilizing CNTs having different diameters (chirality) in a CNTFET [12]. Even though there are lots of merits to CNTFET based electronics, it also comes with several challenges [83]. Further scaling is one of the challenges. Another challenge is multi-level interconnects, for instance, various metal layers are still unavailable with CNT.

3.1.8 GNRFET based Ternary Logic

3.1.8.1 Operating Principle:

Graphene is an allotrope of carbon, which is a group 4 element like silicon and has four electrons in the valence band. Due to the presence of 4 electrons in the outermost band, carbon atoms form covalent bonds with the neighboring atoms and demonstrate mostly non-metallic behavior. In nature, carbon is found in many different non-metal forms. However, when carbon atoms are arranged in the crystalline structure of benzene-like rings of hexagonal shapes, several allotropes possessing extraordinary electrical properties are observed. Two of the most popular allotropes of carbon are carbon nanotube and graphene, which are widely explored as the replacement materials for silicon in the transistor channels [84]. Graphene is a two-dimensional, atomic-scale sheet of carbon atoms, which has a zero band-gap in normal state. If a narrow strip of graphene has a width of less than 50nm, it is called Graphene Nano-Ribbon (GNR). GNR can be of two types depending on the edge structure: zigzag and armchair. While zigzag edged GNR always shows metallic characteristics, the armchair edged GNR can be either semiconducting or metallic in nature, depending on the ribbon width [85]. For the implemented MVL design in this paper, semiconducting GNR would be used. Fig. 18a exhibits the structure of an armchair Graphene Nanoribbon with N number of Dimer lines. The number of dimer lines (N) in a GNR strongly controls the semiconducting property of the GNR. The GNR shows semiconducting property mostly when $N=3p$ or $3p+1$, p being an integer [86]. Based on N, the width of a GNR can be expressed as in (3.14), where a_{c-c}

signifies the lattice constant and the value is equal to 0.142nm [87].

$$W_{GNR} = (N-1)\frac{\sqrt{3}}{2}a_{c-c} \tag{3.14}$$

Graphene Nano Ribbon Field Effect Transistors (GNRFETs) with GNR channels show complete switched off transistor state and large on-off current rations [86]. GNRFET contains another property of controlling the threshold voltage with regard to the width of the GNR. Table 9 summarizes the dependence of the electrical properties of the transistor on the number of dimer lines [27]. Based on the advantages of GNRFET technology, it is utilized for designing the proposed low voltage ternary logic gates circuit topology. Fig. 18b represents a multiple (three) ribbon channel GNRFET. Different designs have been proposed using GNRFET for the implementation of ternary logic [88–92], and quaternary logic [93].

There are two types of GNRFETs: MOS-type and Schottky Barrier (SB) type. In the SB-GNRFET, the Schottky barrier is present at the interface of metal and graphene. Here, the charge transport is mainly due to the tunneling phenomenon through the barriers instead of the thermionic conduction as in the MOS-type FETs. Although the tunneling mechanism can overcome the fundamental thermionic limit of the MOS-type FETs (60mV/decade), the MOS-type GNRFET is preferred here for designing the ternary logic circuits because of lots of advantages like higher Ion-Ioff ratio due to absence of ambipolar transport, higher Ion, higher transconductance, better saturation behavior due to smaller output conductance, higher cutoff frequency, faster-switching speed, etc. [84]. In the MOS-type GNRFET structure, the Si channel is replaced by a parallel arrangement of multiple GNRs. Multiple parallel ribbons are provided to enhance the drive

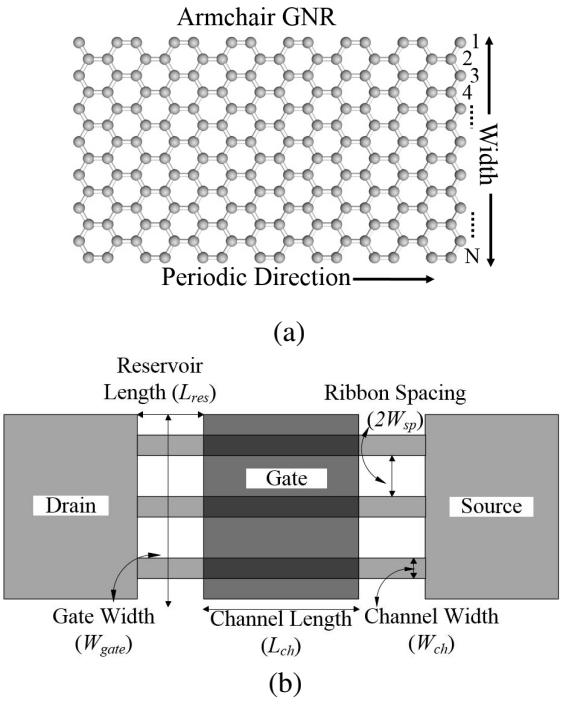
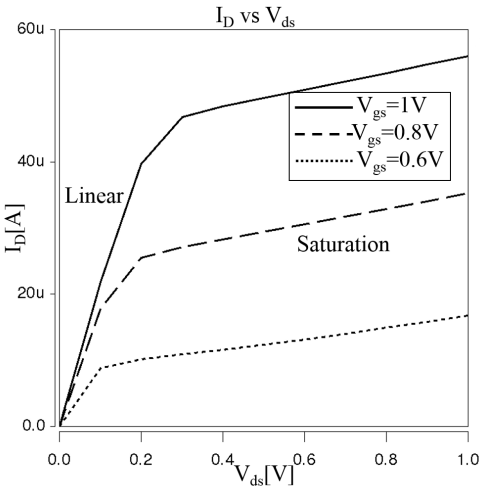


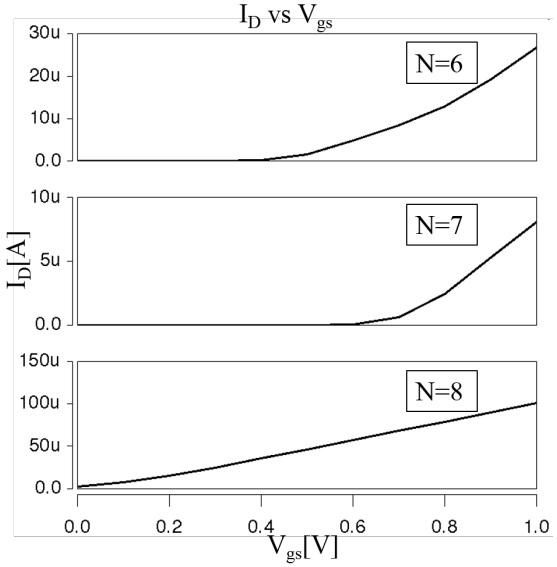
Figure 18: (a) Width of an Armchair GNR with respect to Dimer lines, (b) A multiple (three) ribbon Armchair GNRFET [14]

strength and create a wider contact. Fig. 18b demonstrates the structure of a 3-ribbon MOS-type GNRFET. The portion of the ribbons, which is under the gate, is intrinsic in nature and called the channel. And the portion of the ribbon connecting the gate and the contact part is called the reservoirs, and they are heavily doped with a doping fraction of fdop=0.001 [94]. In Fig. 18b, L_{ch} = channel length, L_{res} = reservoir length, $W_{ch}(WGNR)$ = ribbon width, W_{gate} = gate width, and $2W_{sp}$ = spacing between the ribbons.

Fig. 19a shows the I_D vs. V_{ds} curve with respect to a different level of V_{gs}. Initially, with the increase of V_{ds}, the drain current increases following a linear path, which represents the linear or triode region. After a certain V_{ds}, the current follows the almost



(a)



(b)

Figure 19: (a) I_D vs. V_{ds} curve of an N-type GNRFET with respect to different values of V_{gs}, (b) I_D vs. V_{gs} curve of an N-type GNRFET at V_{ds}=1V for $N = 3p$, $3p+1$ and $3p+2$ $(p = 2)$

Table 9: Dependence of GNRFET Behavior On Dimer Lines (N)

Dimer Lines, N	Band Gap	I_{on}/I_{off}	Order of I_{on}/I_{off}	I_{on}
8, 11, 14, 17	Small	Lowest	$\sim 10^1$	Highest
6, 9, 12, 15, 18	Moderate	High	$\sim 10^6$	High
7, 10, 13, 16	Highest	Highest	$\sim 10^6$	Low

constant value, which denotes the saturation region. Fig. 19b shows the I_D vs. V_{gs} curve for a drain to source voltage of 1.0 V. Like any other MOS-transistors, the I_D vs. V_{gs} curve gives a better understanding of the threshold voltage. For N-type GNRFET, increasing V_{gs} above a specific value turns the transistor ON. And as the gate voltage increases, the current also increases. In the figure, the $I_D$vs. V_{gs} curve is given for $N = 3p$, $3p + 1$, and $3p + 2$ (where, $p = 2$). It is seen that for $N = 3p$ and $3p + 1$, current switches from almost zero to a finite value, which results due to the semiconducting behavior of GNR. And for $N = 3p + 2$, the I_{off} current is never zero, which results due to the metallic state of GNR. Upon close observation of the graph, the threshold voltage of the transistor for different values of N can also be measured.

3.1.8.2 Analysis:

The operating principle of GNRFET circuits is quite similar to the CNTFET circuit. As a result, it possesses all the benefits of CNTFET circuits in the application of MVL. The main advantage of GNRFET above CNTFET is the planner structure and fabrication similarity to MOSFET. In terms of the ternary circuit, GNRFET has been proved to be better in terms of noise margins, power consumption, and fastness [90]. One of the main issues with working with GNR is the effect of Line Edge Roughness (LER), which

results from the unevenness in the edge of the ribbon during the fabrication process. LER affects the electrical properties of the ribbon as well as the transistor. The unevenness of the ribbon introduces unpredictability in the operating condition by changing the ribbon width. Studies show that the off currents of the transistor increases due to the gap states induced in the band-gap region that increases the leakage current at the OFF state. Simultaneously, the on-current of the device generally decreases due to the decreased quantum transport [95]. Different fabrication techniques have been tried for the fabrication of GNR like lithography, chemical synthetics, Extreme ultraviolet lithography, unzipping of carbon nanotubes [96], [97], [98], [99] etc.Lithography can produce GNRs up to the width of 20 nm and produces uneven edges [14]. A combination of lithography and etching is presented in [97], in which lithography is used to pattern the ribbon, and etching is used to narrow it. In this method, GNR having a width of ~ 4 nm has been produced. In [98], chemical synthesis has been used to produce GNRs up to ~ 2 nm of width. There is another bottom-up chemical synthesis approach that can produce atomically precise graphene nanoribbon in different chirality and patterns in $<$2nm of width [99]. The fabrication of ~ 2 nm wide precise GNRs is reported in [100] and [101]. The approach in [101] displays the possibility of fabricating such narrow GNRs with perfect edges.

3.1.9 Memristor based Ternary Logic

3.1.9.1 Operating Principle:

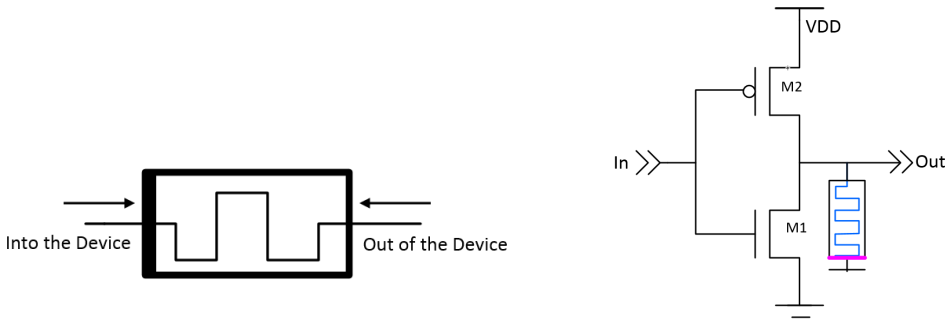
An alternative way to implement MVL circuits is to utilize resistors to achieve multiple voltage levels. However, the electrical properties of the resistor based MVL circuits are not desirable [2]. Memristors are a good alternative to resistors for ternary-circuit design because memristors are capable of handling more than two states with minimal hardware. Memristor is a nonvolatile passive memory element, which can retain its information even if there is no power supply, which is introduced by Chua Leon in 1971. The memristor is defined in terms of a non-linear functional relationship between magnetic flux $\phi_M(t)$ and the total amount of electric charge *q(t)*.

$$f(\phi_M(t), q(t)) = 0 \tag{3.15}$$

The correlation between $\phi_M(t)$ and *q(t)* , being the derivative of one with respect to other is depended on the value of either of them, hence the value of each memristor is characterized by its memristance function which describes the charge-dependent rate of change of flux with charge. The change in the memristance is based on the history of the device.

$$M = \frac{d\phi}{dq} \tag{3.16}$$

Fig. 20a represents the symbol for a memristor symbol. The thick black line on the left side of the device represents the polarity of the device. If the current flows into the device, the resistance of the device decreases which can be defined as R_{on}. If the current flows out of the device, the resistance increases and can be described as R_{off}. Formally,



(a) (b)

Figure 20: (a) Memristive device symbol [15] (b) Ternary inverter using MOSFET and Memristor [16]

a current-controlled time-invariant memristive system is represented by:

$$\frac{dx}{dt} = f(x, i) \tag{3.17}$$

$$v(t) = R(x, i) \times i(t) \tag{3.18}$$

Where *x* is an internal state variable, *i(t)* is the memristive device current, *v(t)* is the voltage of the memristive device, *R(x,i)* is the memristance, and *t* is time [15]. A memristor is a very suitable alternative to resistive load ternary designs. A design to implement basic ternary logic gates like inverter, NAND, and NOR gates using MOSFET and memristor are given in [16]. A diagram of a memristor-based ternary inverter is seen in Fig. 20b. Here, the memristor replaces the large resistors of a resistive-load MOSFET based ternary logic design (Fig. 2b). Besides these, memristor-based ternary logic circuits and adder is proposed in [16, 102, 103].

3.1.9.2 Analysis:

Though the concept of memristor had been proposed in 1971 [104], the use of memristor in ternary logic is quite new. A lot of scopes are present to implement MVL

with the help of memristor technology. Until now, a hybrid of memristors along with some other technology has been tried. For instance, [16] and [103] works on MOSFET-memristor hybrid whereas [105] and [14] works on a hybrid of CNTFET-memristor.

3.1.10 Ternary logic using Metal Insulator Transition Material based memcapacitive modelling

3.1.10.1 Operating Principle:

Memcapacitor are nonlinear capacitors with immediate response. Memcapacitor has the memory capacity and can exhibit different capacitance value upon applying any kind of external incentives like pressure, voltage, or current. Due to the presence of the memory holding capability, it can show different levels of capacitance with respect to time. Just like Memristor memcapacitor possess the capabilities to store data without the power source which proves it to be a useful alternative for the multi valued design. Using Metal-Insulator-Transition (MIT) material is one of the ways to attain memcapacitance in a device. MIT is the property of some material that makes it possible for the material to switch between metal to insulating state with the application of external incitements like pressure, voltage, or temperature. This MIT behavior is one of the ways to achieve memcapacitive. A device is proposed in [17] which utilizes MIT material to generate a memcapacitor based ternary device. In that paper, the percolation phenomenon was used to describe this MIT phenomenon. Fig. 21a shows the structural diagram. The structure is consists of two metal electrodes in between which there is a layer of a dielectric material and a single layer of MIT material. When the gate voltage is applied to the top electrode, a charge puddle is created in the MIT layer, which transforms the insulating layer to a

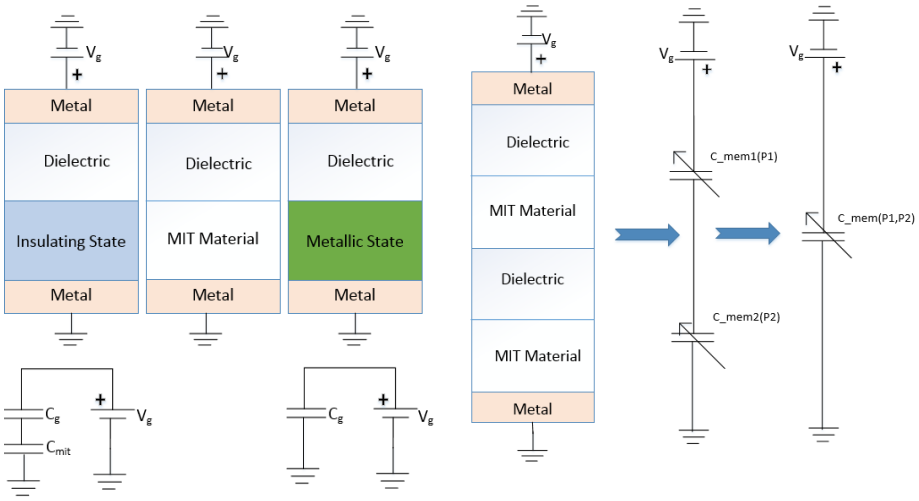


Figure 21: (a) Proposed device structure in [17], its virtual states and schematic for metallic and insulating state of MIT material (b) Vertically cascaded structure for three states with its equivalent schematics

metallic state and thereby creates a continuous conducting channel.

Here, C_g represents the capacitance value introduced between the gate and the dielectric due to the presence of the gate voltage. And C_{mit} is the capacitance value of the MIT layer. The percolation probability, p varies between the values 0 to 1 and has a critical value p_c=0.4. Within the range of $0 \leq p \leq p_c$ the MIT layer stays in the insulator region. And for the range of $p_c \leq p \leq 1$, the layer moves to the metallic region. The memcapacitance value can be expressed with respect to the percolation probability by (3.19).

$$C_{mem}(p) = C_{total} + (C_g - C_{total}) \times p(t) \tag{3.19}$$

A simple cascading of the structure of Fig. 21a can be used for generation of a ternary valued device which is shown in Fig. 21b. The memcapacitance values of the

upper and lower MIT layer can be expressed by (3.20) and (3.21).

$$C_{mem_1}(p) = C_{total_1} + (C_{g1} - C_{total_1}) \times p_1(t) \tag{3.20}$$

$$C_{mem_2}(p) = C_{total_2} + (C_{g2} - C_{total_2}) \times p_2(t) \tag{3.21}$$

Here, p_1 and p_2 are the percolative states of the upper and lower MoS_2 layers respectively. The total memcapacitance C_{mem} of cascaded structure is equivalent to the series combination of C_{mem_1} and C_{mem_2} which is shown in (3.22).

$$C_{mem}(p_1, p_2) = \frac{C_{mem_1} \times C_{mem_2}}{C_{mem_1} + C_{mem_2}} \tag{3.22}$$

Molybdenum disulphide (MoS_2) was used as MIT material in [17]. The same experimentation was done with Graphene-Nano-Ribbon (GNR) to produce the similar results [106].

3.1.10.2 Analysis:

The concept of a memcapacitor based ternary device is very novel.The advantage of the device is the simplicity to attain the ternary logic cell by simply cascading the binary logic cell and the ability to work in psec range. The major drawback of this technology is that it is still at a conceptual stage. A lot more research is needed to compare it with other technologies. And the structural difference with CMOS technology makes the fabrication process far more complicated.

3.2 Comparative Analysis of Different MVL Technologies

The theoretical understanding of multiple-valued-logic (MVL) has been around since the beginning of the 20th century. Research on many different technologies and

implementation approaches for MVL devices has been going on for the last four decades. A summary of the findings of Section 3 regarding the prevailing technologies in the MVL system is given in Table 10. The summary is given in terms of circuit development, techniques used to implement the MVL circuits, advantages, and drawbacks of the respective technologies.

3.3 Discussion

The exponential progress of the prevailing computing system is supposed to face some complications in terms of data density and physical challenges. If they cannot meet the newer demands, new computing paradigms will then be much needed. The present research works involving newer computing paradigms will be useful at that time. This paper shows the different techniques used in designing the multiple-valued logic besides explaining the basic concept of multiple-valued logic. Moreover, it also explains the detailed description of different techniques on a device level and circuit level to design ternary valued logic. The technologies explained in the paper can be divided into two major categories. One is the prevailing technologies like MOSFET, FinFET, FDSOI, SET, and RTD. And another one is emerging technologies like Memristor, CNTFET, QDGFET, GNRFET, etc. Among the prevailing technologies, MOSFET, SET, and RTD have been tried for a long time. Though SET and RTD hold huge promise in the field of MVL, using whole new technology which is completely different from the present CMOS technology would be a huge step. And it can lead to a different other fabrication complexity which was not seen with MOSFET technology. FinFET and FDSOI, on the other hand, improves

Table 10: A summary of different technologies for MVL designs

	Circuit Development	Implementation Technique	Advantages	Drawbacks
MOSFET	Basic logic gates as well as complex arithmetic circuits are available. Mostly on higher node technologies.	1. Combination of Depletion and Enhancement MOSFET. 2. Enhancement MOSFET along with resistors.	Currently prevailing technology which results in the best-matured fabrication process.	Saturation of Moore's' law in lower node forces to look for more advanced technology like FinFET, FDSOI, etc.
RTD	Basic logic gates and few arithmetic circuits are developed.	Using Up/Down Literals	RTD is prevailing for long time. Folding I-V characteristics makes it a promising candidate for the MVL system.	There are very few current works involving RTD based MVL.
SET	Basic logic gates and few arithmetic circuits are developed.	Using Multiple gates to obtain controllable threshold voltage	The threshold voltage is easily controllable through multiple gates.	The challenges of fabrication is a major issue. Few recent works are being done on SET-MOS hybrid technology.
QDGFET	Few designs have been proposed for QDGFET based logic gates and arithmetic circuits.	Threshold voltage control	The simulation results show a very promising outcome.	More work needs to be done to estimate all the pros and cons of QDGFET based MVL. Very few instances of fabrication of QDGFET is available.
FinFET	Though FinFET is a very promising technology for the MVL system, the circuit designs are not developed. Most of the available works are on simple logic gates like an inverter.	Threshold voltage control	The fabrication of FinFET found on the industrial level. In the case of lower node technology, FinFET is expected to alleviate the challenges associated with MOSFET.	Fewer research on FinFET based MVL design.
FDSOI	Very few complex arithmetic circuits designs are available. Few designs for MVL FPGA have been proposed.	Threshold voltage control through the back gate.	Matured fabrication technology, lower short channel effects, etc.	MVL circuit development is not matured. Heating problems and difficulty to fabricate thin bodies.
CNTFET	A significant number of designs are available for basic logic gates and complex arithmetic circuits.	Threshold voltage control through the control of the chirality values of the CNT.	In the developed fabrication process, an ample amount of study is available for CNTFET.	Fabrication complexity like gate alignment challenge and incompatibility to planner technology.
GNRFET	Basic logic gates and few arithmetic circuits are developed.	Threshold voltage control through the control of the width of the GNR.	Due to the planer structure, it has the potential to use in the existing MOSFET fabrication process.	Few fabrication challenges like line edge roughness are present. The fabrication process is currently developing.
Memristor	Few designs have been proposed for Memristor based logic gates and arithmetic circuits.	Replacement of Resistor in MOSFET-based designs.	Currently, Memristor is being extensively researched for its numerous potential applications.	The fabrication of hybrid of MOSFET-Memristor or CNTFET-Memristor is on a preliminary level.
MIT material based memcapacitive modeling	Circuit-level implementation is not developed.	Changing memcapacitance of the device using Metal to insulator transition method.	The use of a two-terminal device is an interesting concept which contributes to a very simple operating mechanism.	Most of the work is on a conceptual level.

the limitations that come with MOSFET without having to modify lots of fabrication techniques. In addition to this, they are already been used in place of MOSFET in different sectors. On the other hand, among the emerging and futuristic technologies, carbon-based transistors hold the most potential for implementing MVL. Though CNTFET has been the topic of interest for a longer time than GNRFET, GNRFET has the advantages of a planner structure which makes it a more suitable substitute for MOSFET. But in terms of fabrication, the maturity of CNTFET is very much well ahead of GNRFET and other emerging technologies. The major drawback of the MVL system is the abundant usage of the binary system on most of the computing system. It might not be possible for the MVL system to replace the binary system at once, but MVL is already started to make its way especially in terms of MVL memory. As the operating voltage of the memory system is still high compared to the arithmetic system, the problem associated with the low operating voltage for MVL is not a big issue here. Also in the case of arithmetic circuits, ternary and quaternary logic circuits have been proposed which was proven to give very good results with low operating voltage.

CHAPTER 4

TERNARY LOGIC GATES USING GRAPHENE NANO RIBBON FIELD EFFECT TRANSISTOR (GNRFET)

Previous chapter explains the operating principle of Graphene Nano Ribbon Field Effect Transistor or GNRFET. In this chapter, we explain the different proposed ternary logic gates design such as inverter, NAND, and NOR using GNRFET. For the implemented design and analysis, the GNRFET model files available on Nanohub [107] are used. In the MOS-GNRFET model developed in [108], [107], the architecture is designed in such a way that there are multiple metal layers on the top of the single graphene layer. The metal gates of the GNRFET and most of the interconnects are comprised of those metal layers. The channels, drains, and sources of transistors are located on the graphene layer, and metal gates are located on the first metal layer. The width of the local GNR interconnects between transistors is 20nm, which is much shorter than the mean free path of the graphene and, as a result, has negligible resistance. Due to this, the resistance of local interconnect within logic gates is neglected. The vias in the design is considered to be metal because the research on graphene vias is still on an underdeveloped level. Graphene-metal contact resistance is usually high [109]. For this reason, they are modeled with a 20-k resistor for a 50 nm wide via. In all the simulations in our paper, GNRFETs with three parallel armchair GNR as the channel is used (Fig. 20a). GNRFET with varied dimer length is used in the design to get appropriate threshold voltage. The channel length of each transistor is 16nm.

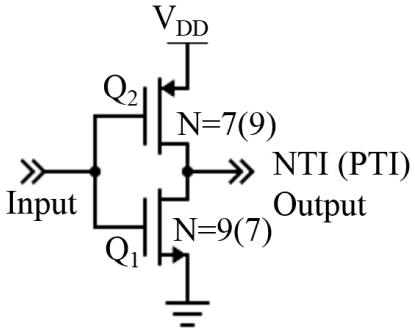


Figure 22: Schematic Diagram of Negative (Positive) Ternary Inverter using GNRFET

4.1 Ternary Inverter

Fig. 22 shows the design for the negative ternary inverter (NTI) and the positive ternary inverter (PTI). For NTI, the numbers of dimmer lines (N) are 7 and 9 for the p-type and n-type GNRFET, respectively. For PTI, the values of N are 9 and 7 for the p-type and n-type GNRFET, respectively. Fig. 23 shows the standard ternary inverter (STI) design. The circuit topology for the inverter used here is similar to the CNTFET based inverter topology demonstrated in [33]. However, the operating principle and techniques to achieve multiple voltage levels are different in the proposed GNRFET based ternary inverter. For example, in CNTFET based ternary inverter, the chirality of the CNTs are varied to achieve different threshold voltages. On the other hand, in GNRFET, the width of the GNRs are varied to change the threshold voltage. Here, $Q1$, $Q2$, and $Q3$ are n-type transistors, and $Q4$, $Q5$, and $Q6$ are p-type transistors. The threshold voltage of $Q1$, $Q2$, and $Q3$ are 0.24V, 0.6V, and 0.4V, respectively. The threshold voltage of $Q4$, $Q5$, and $Q6$ are -0.4V, -0.6V, and -0.24V, respectively. To obtain the specific threshold voltage, $Q1$

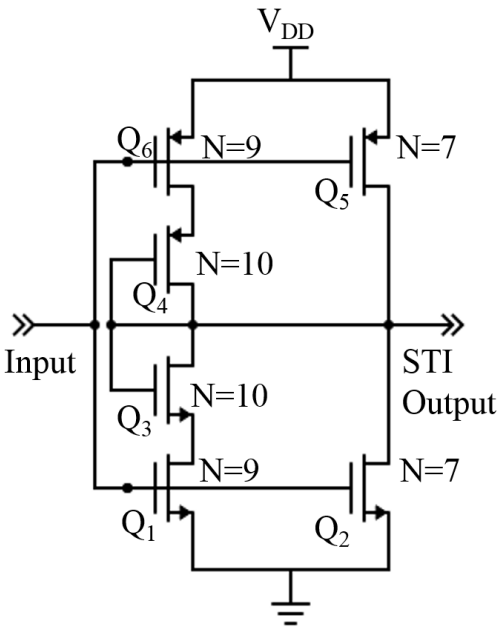


Figure 23: Schematic Diagram of Standard Ternary Inverter using GNRFET

and $Q6$ are set to have $N = 9$, $Q2$, and $Q5$ to $N = 7$ and $Q3$ and $Q4$ to $N = 10$. If the input voltage is increased from low to high, when it is less than 0.3V, $Q5$ and $Q6$ become ON, which makes the output voltage high. For an input voltage within the range 0.3V and 0.6V, $Q1$ and $Q6$ become on, and $Q3$ and $Q4$ perform as a diode-connected load. This maintains an intermediate voltage level at the output node. When the Input voltage reaches to a value higher than 0.6V, $Q2$ becomes ON, which brings the output voltage to a value equal to 0V.

Fig. 24 shows the transient response of three different types of ternary inverters. The voltage transfer curve for the STI is shown in Fig. 25, which displays that the device is capable of holding three discrete output voltage levels for a wide range of input voltage.

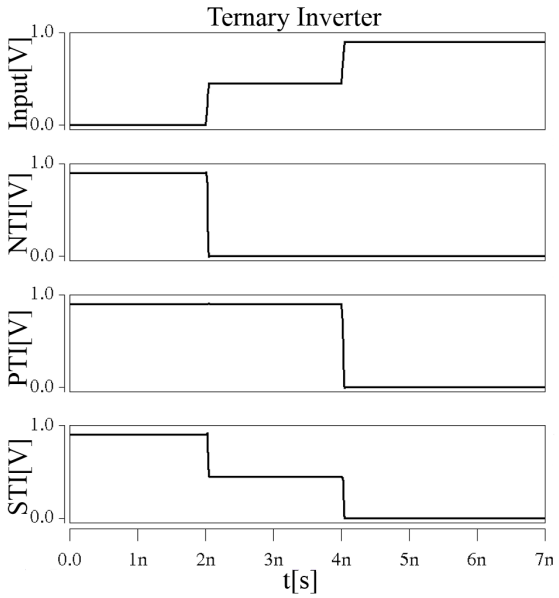


Figure 24: Transient response of NTI, PTI, and STI

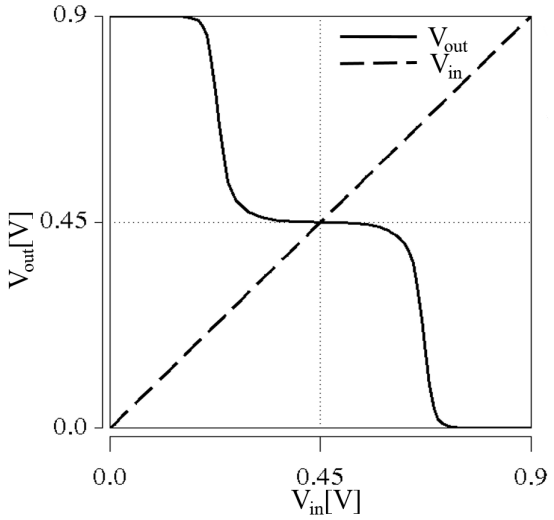


Figure 25: Transfer curve for GNTFET based STI

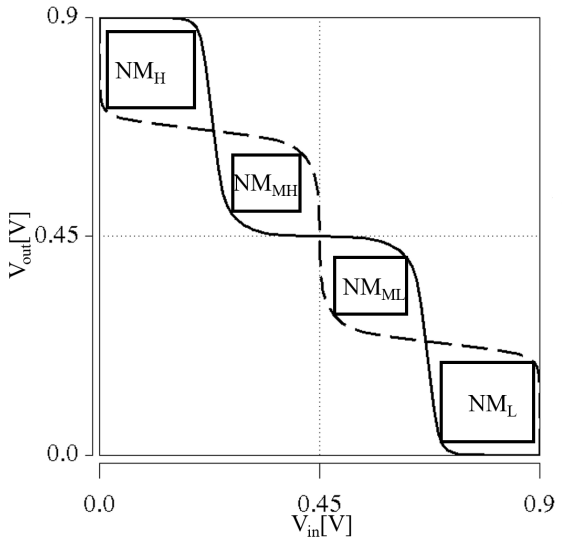
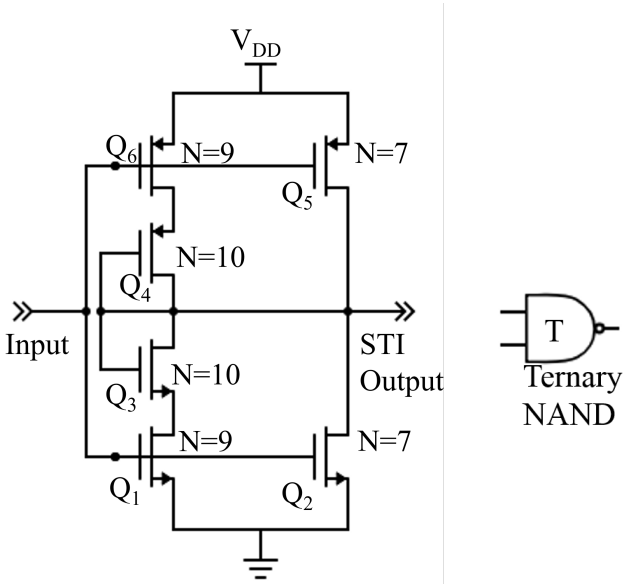


Figure 26: Butterfly curves for GNRFET based STI showing different Noise Margins (NM)

Four separate noise margins (NM) are relevant to the ternary logic circuit, and these are (i) noise margin low (NML), (ii) noise margin low-to-medium (NMML), (iii) noise margin medium-to-high (NMMH), and (iv) noise margin high (NMH) [110]. To estimate the robustness of the three discrete voltage levels (logic states) of the implemented STI, we performed the noise margin analysis using the butterfly curve method, as shown in Fig. 26. This curve demonstrates that the GNRFET based STI has reasonably high noise margins to offer stable output voltages.

4.2 Ternary NAND and NOR Gates

Using the same convention used for the STI, we have designed both ternary NAND and NOR gates. The designs for these gates are presented in previous literature using



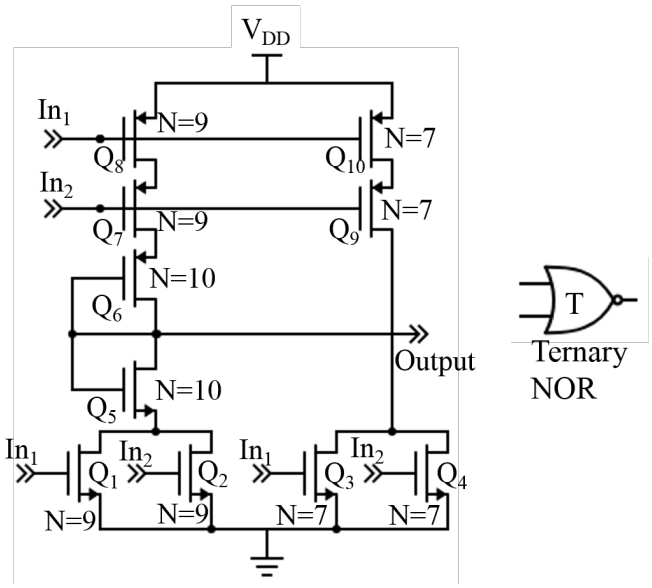
(a) (b)

Figure 27: (a) Schematic Diagram (b) Logic symbol of GNRFET based 2-input NAND gate

different technologies [33]. Here, we have implemented the designs using GNRFET. Fig. 27 shows the implemented design of a ternary NAND gate and its logic symbol. Fig. 28 shows the design of a ternary NOR gate and its logic symbol. The transient response for the ternary NAND and NOR gates are shown in Fig. 29.

4.3 Comparison

In the literature, many CNTFET based ternary logic gate designs can be found. It is widely perceived that GNR would be a better choice for the transistor channel than CNT. Therefore, this paper focuses on GNRFET based ternary logic and arithmetic circuit implementation. Here, a comparative analysis between some of the existing CNTFET,



(a) (b)

Figure 28: (a) Schematic Diagram (b) Logic symbol of GNRFET based 2-input NOR gate

GNRFET, CMOS, and the proposed GNRFET based basic ternary logic circuits are summarized in the latter portion of this section. All the simulations are done using an input slew of 50ps and an output load of 1pf. The doping fraction f_{dop} is selected to be 0.001 for all the transistors. he simulations are done in H-spice using model files from Stanford Nanoelectronics lab, which are derived in [111], [112]. The comparison between different basic gates in terms of delay, leakage power, total power, and power-delay-product (PDP) of CNTFET and GNRFET is presented in Table VII. From the Table, it can be observed that, in terms of delay, total power, and PDP, our proposed logic gates hold a lot of promise in the field of ternary devices.

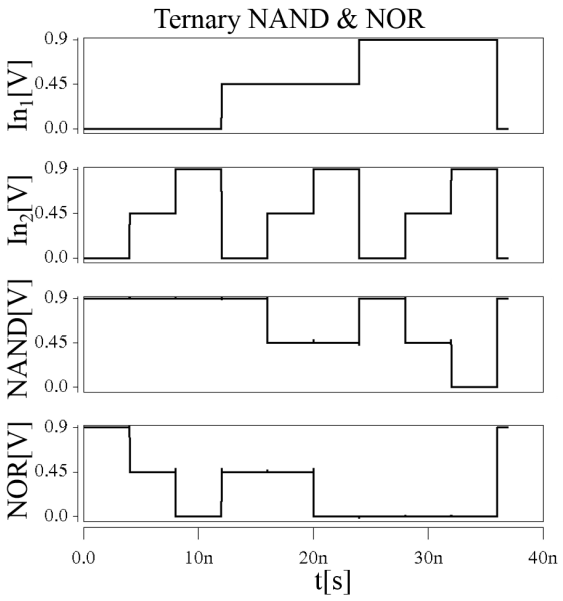


Figure 29: Transient response of a NAND and NOR gate.

Table 11: Comparative Analysis Between Existing CNTFET/GNRFET And the Proposed GNRFET Based Ternary Logic Gates.

Logic Gates		Transistor count	Delay (ps)	Total power (nW)	Power Delay Product, PDP (e-18)
STI	CNTFET [33]	6	11	88.6	0.98
	CNTFET [113]	-	18.8	1170	33.2
	CNTFET [79]	6	8.9	263	2.34
	GNRFET [88]	6	30	8100	24
	GNRFET [89]	3	1.57	22200	34.9
	Proposed Work	6	13	23.22	0.302
NAND	CNTFET [33]	10	3	100.8	0.3
	CNTFET [113]	-	27.6	704.8	19.46
	GNRFET [88]	10	58	1580	92
	Proposed Work	10	5.2	27.5	0.14
NOR	CNTFET [33]	10	2	100	0.2
	CNTFET [113]	-	27.3	1054	28.79
	GNRFET [88]	10	47	1635	77
	Proposed Work	10	3.33	27.42	0.1

CHAPTER 5

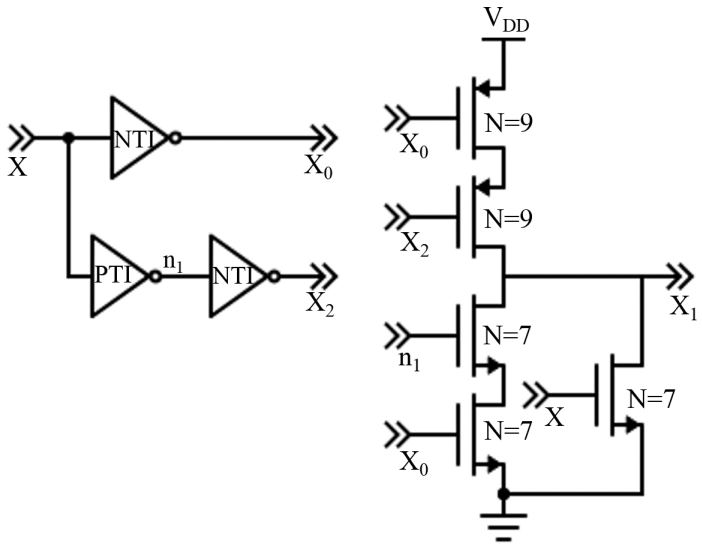
TERNARY ARITHMETIC CIRCUITS USING GRAPHENE NANO RIBBON FIELD EFFECT TRANSISTOR (GNRFET)

In the previous chapter, we explained our different basic logic gates design using Graphene Nano Ribbon Field Effect Transistor or GNRFET. In this chapter, we describe our proposed design for different ternary arithmetic circuits using those basic logic gates. Here, we introduced a novel design for ternary decoder, ternary buffer, ternary half-adder, and ternary 3:1 multiplexer. Similar to previous chapter, we have used 16nm GNRFET model files available on Nanohub [107] for the simulation purpose.

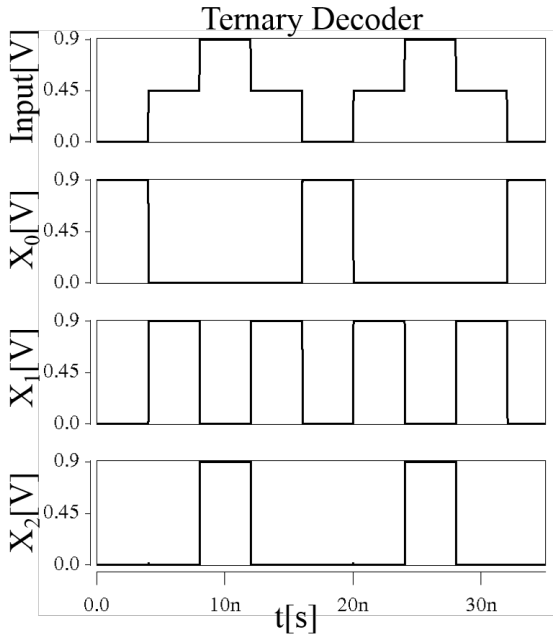
5.1 Ternary Decoder

Using the logic gates mentioned above, a ternary decoder can be designed. The decoder is an essential part of a ternary half adder. It has one input port (X) and three output ports (X_0, X_1, and X_2). A ternary input voltage operates the decoder, and depending on the input voltage level, one of the three output ports gives a high output voltage. For example, if the input voltage is 0V, the X_0 node will show a high voltage level (V_{DD}). The logical relation between the input and output ports of the decoder is represented by (5.1), and its schematic diagram and transient response are shown in Fig. 30.

$$X_k = \begin{cases} 2, & X = k \\ 0, & X \neq k \end{cases} \tag{5.1}$$



(a)



(b)

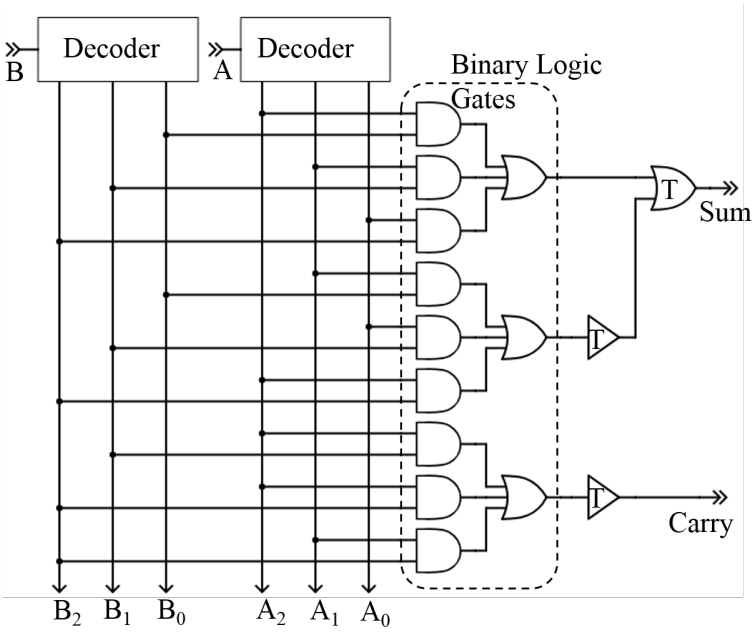
Figure 30: (a) Schematic Diagram (b) Transient Response of GNRFET based proposed ternary decoder

5.2 Ternary half-Adder

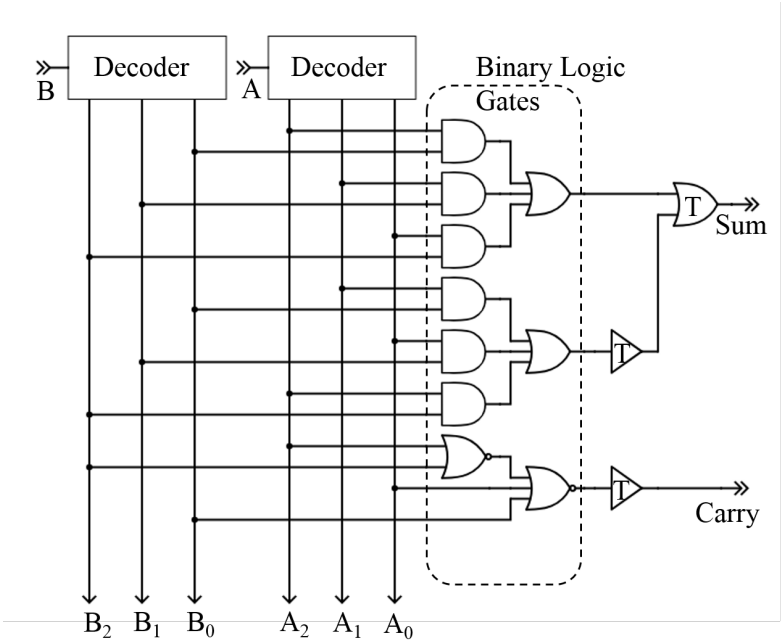
The ternary half adder takes two 1-trit input voltage and produces a 1-trit sum and a 1-trit carry as the outputs. The equations and truth table for describing a ternary half-adder is already mentioned in Chapter 2.

For the internal operation of the adder, different designs have been proposed in [1], [27], and [33]. Among them, the design in [31] uses the simplest and the most efficient topology using CNTFET. For the half adder, we have followed the topology of [33] and proposed a simpler carry circuitry which requires lesser transistor. Fig. 34b demonstrates the proposed diagram of the ternary half adder using our proposed decoder. Here, the decoder is ternary, and it takes ternary input and produces high voltage levels at the respective output port, depending on the input voltage level. For example, for the input $A = 2$ and $B = 1$, it will give full rail-to-rail voltage on A_2 and B_1. The second stage of the ternary half-adder is made of binary logic gates, which receive the input signals from the ternary decoder output nodes to generate the half-adder outputs as in (2.7)-(2.8). And the outputs of these binary logic gates remain in binary form. The third stage of the half-adder circuit is comprised of a ternary OR and a T-buffer gate, which converts the binary signals from the second stage to ternary signals. T-buffer is a simple circuit that acts as a level shifter. The logical operation of the T-buffer is as shown in (5.2), and the proposed circuit diagram of the T-buffer is shown in Fig. 32.

$$Out = \begin{cases} 1, & V_{in} = 1, 2 \\ 0, & V_{in} = 0 \end{cases} \tag{5.2}$$



(a)



(b)

Figure 31: (a) Schematic diagram of ternary half adder [31] (b) Proposed design of ternary half-adder

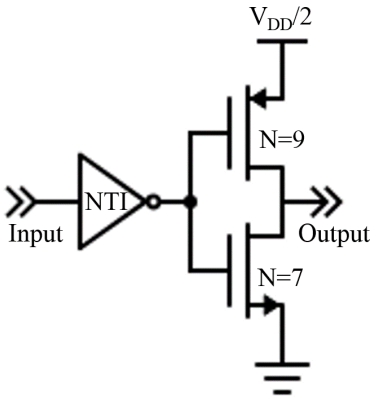


Figure 32: Proposed Schematic Diagram of T-buff

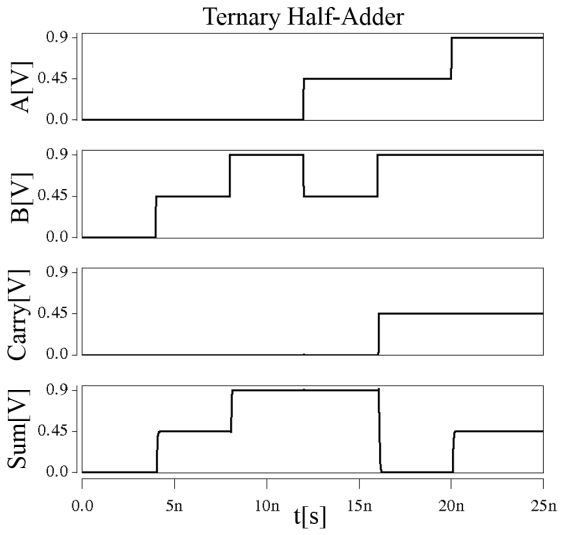


Figure 33: Transient Response of the ternary half-adder

The input-output voltage curves of the ternary half-adder of Fig. 34b is shown in Fig. 33. It is observed that the voltage curves match the truth table exactly.

5.3 Ternary Multiplexer

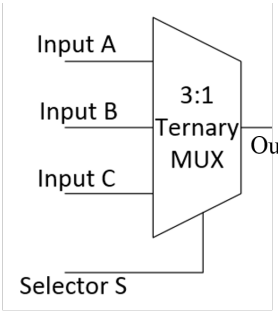
The basic multiplexer is a device, which depending on the signal value in a particular select pin, can transmit one of several inputs to the output port. For example, in case of a 2:1 binary multiplexer (MUX), if the value on the select pin is 0, input-1 will be transmitted to the output, and if the value on the select pin is 1, input-2 will be transmitted. Here, we propose the design of a 3:1 ternary multiplexer, which can transmit any one of the 3 inputs to the output port depending on the select pin value. And it can transmit both binary and ternary data. Table 12 shows the truth table, and (10) represents the logical expression (input-output relation) of the 3:1 ternary MUX.

$$Output = S_0A + S_1B + S_2C \tag{5.3}$$

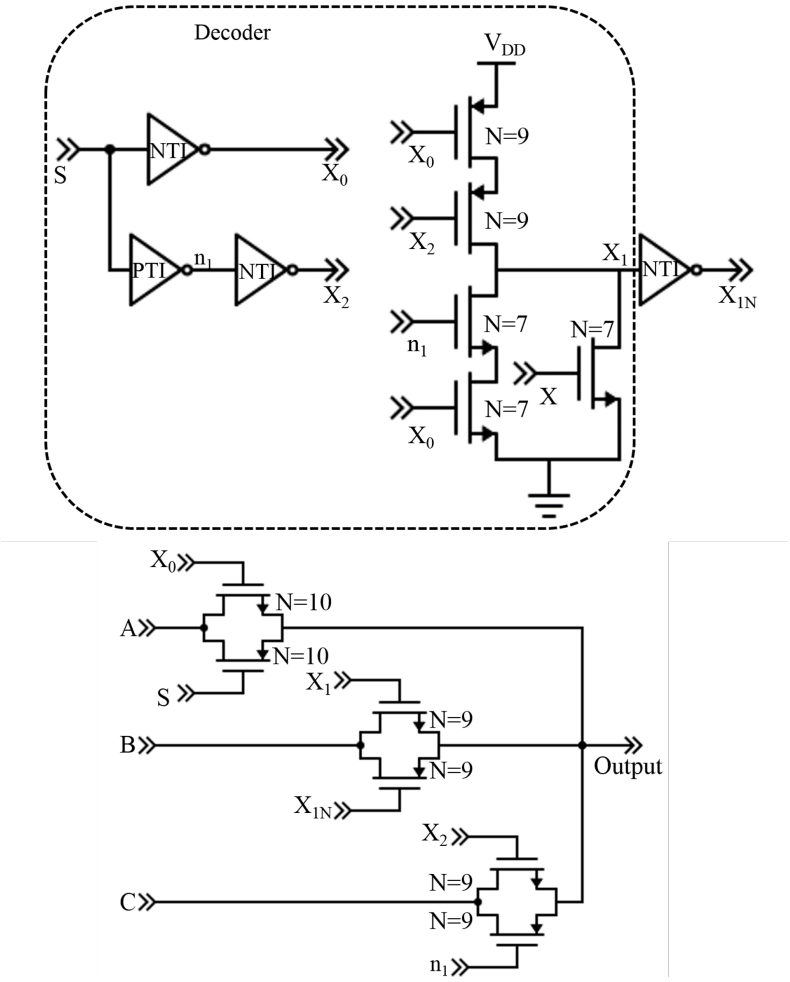
Here, the values of S_0, S_1, and S_2 obtained from a ternary decoder explained in the previous subsection. Depending on the input voltage value at the select (S) input terminal, it passes the corresponding input signals (A, B, or C) to the output port.

Table 12: Truth Table for 3:1 Ternary MUX

Selector	**Output**
0	A
1	B
2	C



(a)



(b)

Figure 34: (a) Logic Diagram and (b) Schematic Diagram of 3:1 Ternary MUX

The logic and schematic diagrams of the ternary MUX are shown in Fig. 34, where S denotes the select pin and A, B, and C are the three different inputs of the multiplexer. Fig. 35 shows the simulated output of the multiplexer. The voltage range in those inputs is varied in such a manner that it can be observed that the circuit can transmit inputs of all voltage range. Here, input A is a signal within the range 0 to 2, input B is in the range of 0 to 1, and input C is in the range of 1 to 2. In all of the cases, the signal is passed accordingly without any significant distortion.

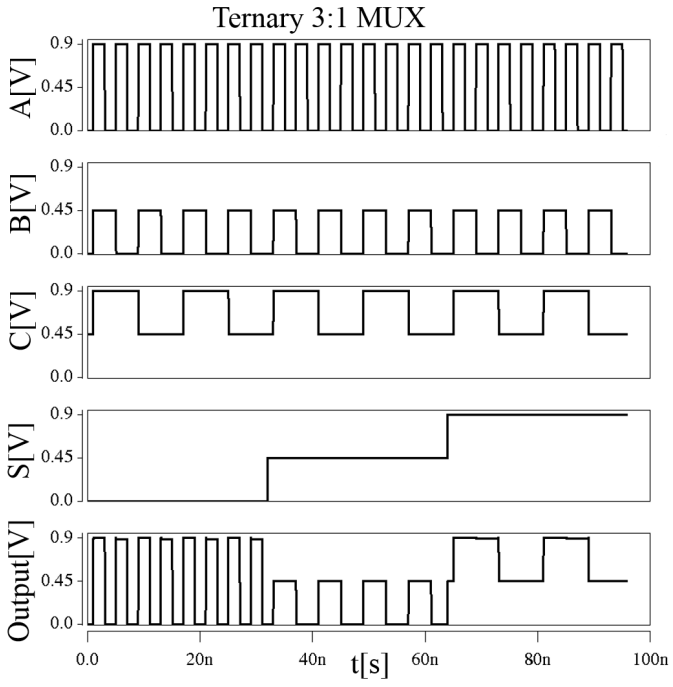


Figure 35: Transient Response of 3:1 Ternary MUX

5.4 Analysis and Comparison

The performance analysis of the proposed decoder and 3:1 ternary MUX is given in Table 13.

Table 13: Performance Analysis of the Proposed Decoder and 3:1 Multiplexer

Parameters	Decoder	Multiplexer
Transistor Count	11	19
Delay (ps)	14	1.5
Total Power (nW)	6.09	1.548
Power Delay Product, PDP (e-18)	0.09	0.002

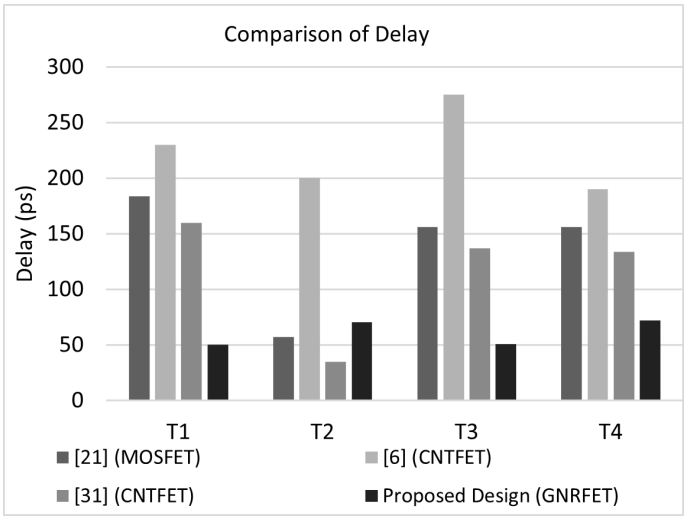


Figure 36: Comparative analysis of transient delay of half adder for different designs

Fig. 36 shows the delay comparison of three different types of ternary half-adder circuits presented in [12], [32], and [33] with the proposed GNRFET based half-adder. Here,

Table 14: Comparative Analysis of PDP (Power-Delay Product) of the Proposed GNRFET based Half-Adder Design with Different Existing Designs

Reference	**Technology**	**Transistor Count**	**Power Delay Product, PDP (e-15)**
[32]	MOSFET	-	0.542
[81]	CNTFET	64	0.025
[12]	MOSFET	-	6.7
[80]	CNTFET	65	0.117
[33]	CNTFET	136	0.411
[114]	CNTFET	112	0.05
Proposed Design	GNRFET	102	0.01

$T1$ = 0-1 rise time delay of Sum with respect to B

$T2$ = 1-2 rise time delay of Sum with respect to B

$T3$ = 0-1 rise time delay of $Carry$ with respect to B

$T4$ = 0-1 rise time delay of Sum with respect to A

It is observed that the delay in the proposed GNRFET based half-adder design is much lower than the other three designs. The comparison of the transistor count and power-delay-product (PDP) of the proposed GNRFET based ternary half-adder with one MOSFET based and five other CNTFET based half-adder circuits is shown in Table 14. It shows clearly that in terms of PDP, the proposed GNRFET based ternary half-adder offers a significant improvement over other designs.

CHAPTER 6

TERNARY SEQUENTIAL CIRCUITS USING GRAPHENE NANO RIBBON FIELD EFFECT TRANSISTOR (GNRFET)

Digital circuits can be categorized into (a) combinational nonregenerative circuits and (b) Sequential or regenerative circuits. In a combinational circuit, at any point in time, the output is some Boolean function of its current inputs. No intentional connection from outputs back to input is present. And in a sequential circuit, the output is not only a function of current inputs, but also of previous values of the inputs, This can be accomplished by connecting one or more outputs intentionally back to some inputs, by providing a memory to remember past events. A sequential circuit includes a combinational logic portion and module to store previous logic states.

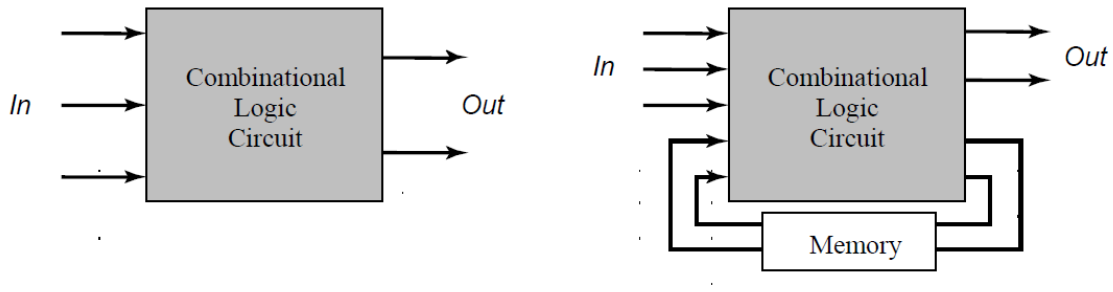


Figure 37: Combinational vs Sequential Circuit

6.1 Ternary D-Latch

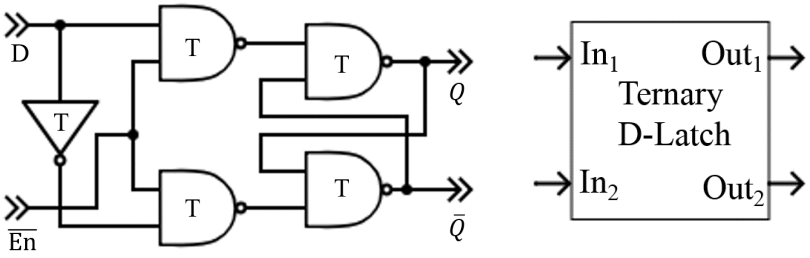
Latch and flip-flops are the fundamental elements for the storage of data. A single latch or flip-flop can hold a single bit of data. For the case of a latch, the output is continuously controlled by the input as long as the enable signal is asserted. They are level sensitive devices, i.e., the output will be affected by the input irrespective of the rising or falling edge of the Enable or clock signal. A latch either stays in a transparent mode or a hold mode. In transparent mode, the output follows the input, and in hold mode, the output is kept at the previous output value [115].

Table 15: Truth Table for representing Ternary D-latch

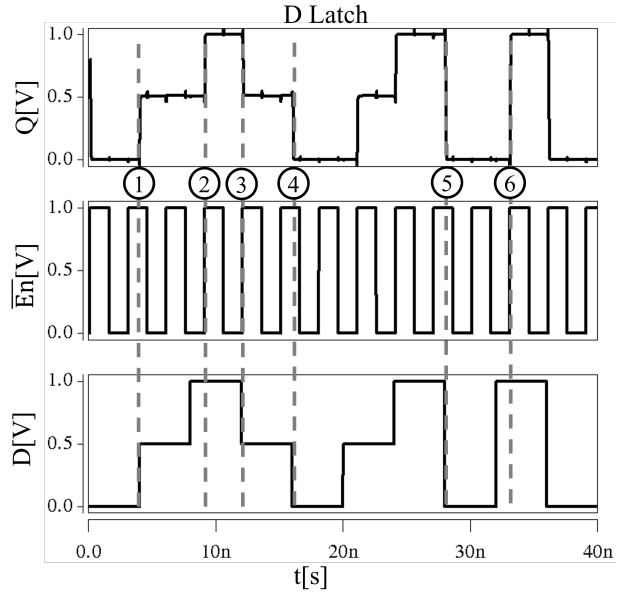
En	**D**	Q	$\bar{Q}$
0	0	0	2
0	1	1	1
0	2	2	0
2	X	Q_{prev}	$\bar{Q}_{prev}$

The truth table for a ternary D Latch using a binary clock is given in Table 15. For the low value of the clock/Enable signal, the output follows the input or maintains transparent nature. But for the high value of clock/Enable, the output retains the previous value.

In this paper, we follow a similar convention used in binary NAND-based D-latch. The design of the proposed GNRFET based D-latch and itsâ symbol are shown in Fig. 38 and Fig. 38b, respectively. The simulation results showing the input and output voltages are shown in Fig. 38c. Points 1 to 6 denote six possible transitions of voltages for the



(a) (b)



(c)

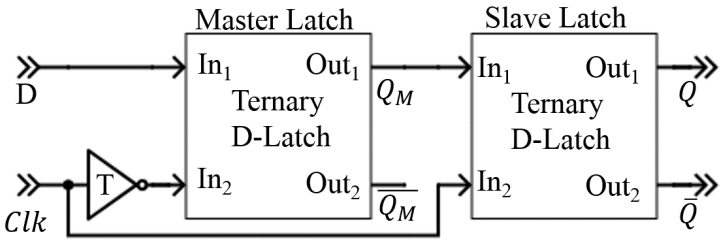
Figure 38: (a) Schematic Diagram (b) Symbol and (c) Transient Response of D-Latch

ternary output signal ($0 \rightarrow 1, 1 \rightarrow 2$, and so on). From Fig. 38c, it is evident that the output Q follows input D depending on the value of the Enable signal. If $En = 0$, only then the Q adheres to a transparent mode. Otherwise, it holds the previous value.

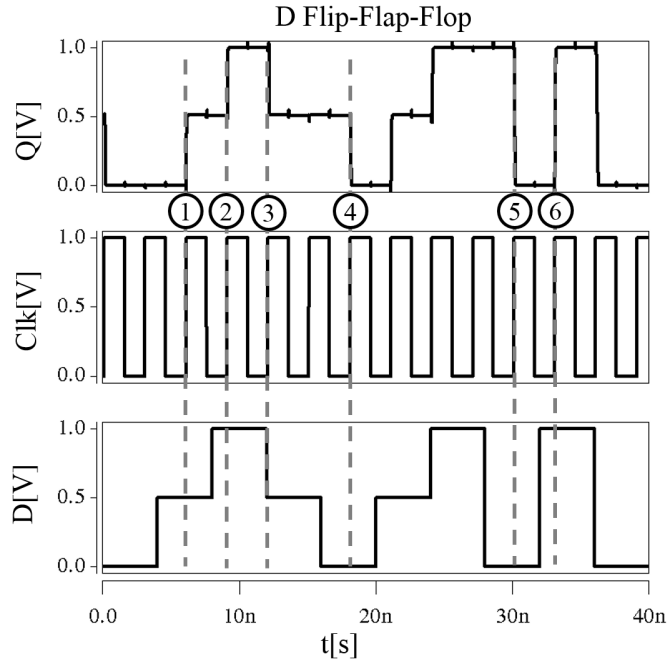
6.2 Positive Edge Triggered D Flip Flap Flop

In this work, we have designed a positive edge-triggered Master-Slave Ternary D Flip-Flop using two D-latch. For a positive edge-triggered D Flip-Flap-Flop or DFFF, the output follows a transparent mode only in the presence of a rising edge of the clock. A positive edge-triggered master-slave DFFF is made by connecting a two D latch back to back. The schematic diagram of the ternary D Flip-Flop or D Flip-Flap-Flop is given in Fig. 39a. Here, The first latch is master whereas the second latch is slave. When $clock = 0$, the master stage is transparent, and the input D is delivered to the output Q_M of the master latch. At the same time, the slave latch is kept in the hold mode to retain its earlier value by the feedback. At the rising edge of the clock, the master latch stops processing the input, and the slave starts transferring the output Q_M of the master, while the master latch goes to hold mode and conserves Q_M using its feedback method. Since Q_M is stable during the high stage of the clock, the output Q makes a single transition per cycle after the rising edge of the clock. Consequently, these two cascaded D flip-flops act as a positive edge-triggered storage element. Table 16 represents the truth table for the DFFF.

The transient response of the DFFF showing the input and output voltages is given in Fig. 39b. From the six points shown in Figure (points 1 through 6), it is apparent that



(a)



(b)

Figure 39: (a) Schematic Diagram and (b) Transient Response of D Flip-Flop

Table 16: Truth Table for representing Ternary D Flip Flop

Clock	**Mode**	D	Q	$\bar{Q}$
$0 \rightarrow 2$	Transparent	0	0	2
		1	1	2
		2	2	0
$2 \rightarrow 0$	Hold	X	Q_{prev}	$\bar{Q}_{prev}$

the output Q changes the value only at the positive edge of the clock signal. Otherwise, it holds the previous value.

6.3 Analysis and Comparison

The Power and Delay analysis of the proposed D-latch and D Flip-Flop-Flap is given in Table 17 and Table 18, respectively. We have also done a quantitative analysis of power and delay of DFFF with other prevailing designs in Table 18. Among the references, [116] and [117] are CMOS based designs, and [118] is the Carbon Nano Tube Field Effect Transistor (CNTFET) based design. The simulation results of [117] and [118] are taken from [116].

A close observation of Table 18 shows that, in terms of average delay, our proposed design is 1.1, 4.5, and 1.94 times better than the designs proposed in [116], [117] and [118] respectively. In terms of Static Power, storing â1â appears more crucial as it requires a very high power to store or transfer an intermediate voltage level (â1â). In this case, our proposed design is 1.81, 5.76, and 3.69 times efficient than the designs of [116], [117], and [118], respectively. Finally, in the case of Average Power, our design is 2.26, 4.8, and 2.85 times better than [116], [117], and [118], respectively. The average

Table 17: Power and Delay Analysis of Ternary D-latch

		Proposed Design (D-latch)
Delay (ps)	$0 \rightarrow 1$	45.3
	$0 \rightarrow 2$	53
	$1 \rightarrow 0$	100
	$1 \rightarrow 2$	51.9
	$2 \rightarrow 0$	105
	$2 \rightarrow 1$	93
	Average	70.1
Static Power (nW)	Holding 0	5.0237
	Holding 1	495.76
	Holding 2	4.98
Leakage Power (μW)		0.005
Average Power (μW)		0.230

power is calculated by multiplying average delay with average current flowing through the circuit. For the simulation of our design, we have used a 16-nm GNRFET model [107], and all the simulations are done in HSPICE.

Table 18: Power and Delay Analysis and Comparison of Ternary D Flip Flop

		[116]	[117]	[118]	Proposed Design
Delay (ps)	$0 \rightarrow 1$	69.196	90.504	99.416	24.8
	$0 \rightarrow 2$	116.66	326.88	284.92	61
	$1 \rightarrow 0$	61.687	463.01	116.62	111
	$1 \rightarrow 2$	83.393	305.79	232.14	79.9
	$2 \rightarrow 0$	95.044	489.30	24.641	93
	$2 \rightarrow 1$	38.405	220.88	60.475	51
	Average	77.398	316.06	136.369	70.1
Static Power (nW)	Holding 0	62.969	216.61	17.406	11.953
	Holding 1	2405.2	7667.9	4883.4	1331
	Holding 2	101.98	206.35	16.792	12.838
Leakage Power (μW)		-	-	-	0.331
Average Power (μW)		1.1835	2.5143	1.4918	0.523

CHAPTER 7

TERNARY MEMORY CIRCUITS USING CARBON NANO TUBE FIELD EFFECT TRANSISTOR (CNTFET)

In this paper, we have proposed a ternary 3T Dynamic Random-Access Memory or DRAM cell using a 16nm Stanford University model of CNTFET [82]. In the proposed design, we have used three CNTFETs along with a single word line for both read and write operation. Also, we have examined the delay and power consumption in the presence of various process variations using Monte Carlo simulations.

The proposed diagram of ternary 3T-DRAM is given in Fig. 40. Here, one word-line (WL) and two bit-lines (BL) has been used for the proper operation of the DRAM. The control signal is given by WL. Depending on the value of WL, the DRAM cell operates in a write or read mood. BLs are used for the reading or writing operation of data. BL_1 takes part in the write operation and BL_2 takes part in the read operation of the memory cell directly. The threshold voltage of the three transistors M_1, M_2, and M_3 are 0.24V, 0.6V, and 0.24V, respectively. Two capacitors C_S and C_{BL} are used for the data storage and discharge operation. The values of the capacitors are 0.1fF and 0.7fF, respectively.

7.1 Operating Principle

- Write Operation: The data that needs to be written in the memory cell is placed in BL_1. Upon the arrival of the positive edge of the word-line WL, the transistor

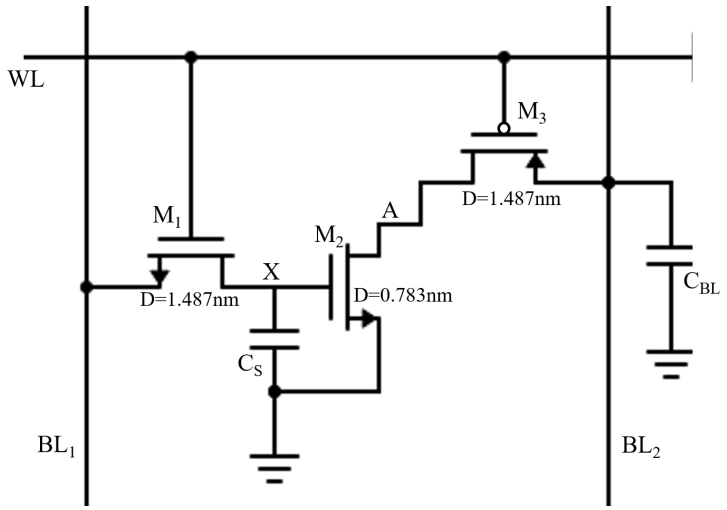
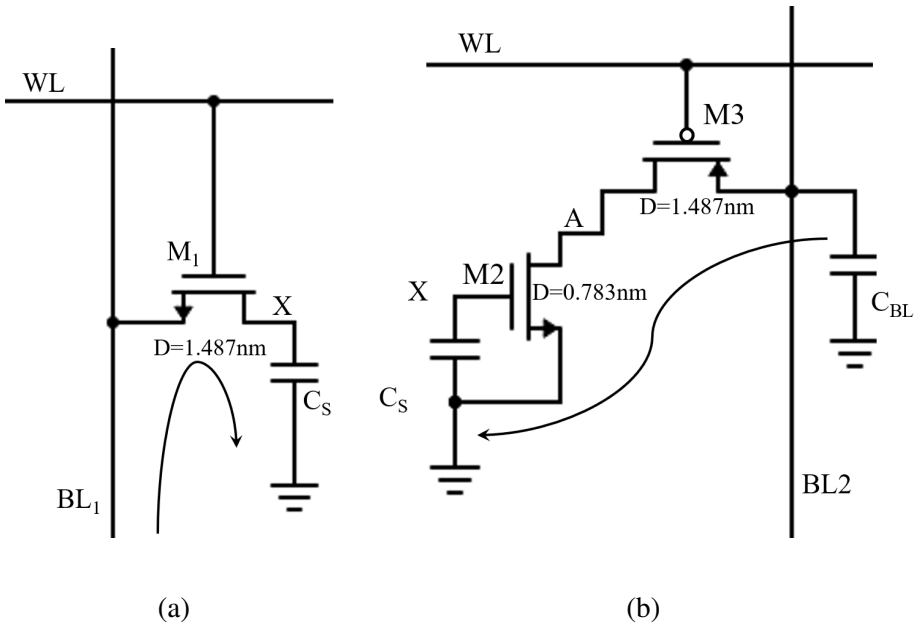


Figure 40: Schematic diagram of the proposed 3T DRAM

M_1 starts conducting. As a result, the data starts to store in the capacitor C_S. For storing the data 1 or $0.5V_{DD}$, the exact $0.5V_{DD}$ gets stored in the capacitor. For the storage of the data 2 or V_{DD}, a threshold voltage drop happens like the binary DRAM. Once the data is written in the node X, it stays there until the next positive edge of the word-line.

- Read Operation: When the value on the word-line becomes zero, the read operation begins. At that time, the transistor M_3 turns on. The bit-line BL_2 is pre-charged to the voltage V_{DD}. If the data stored in X is zero, then transistor M_2 remains off and the voltage at node A remains high. If the data stored in the cell is 1 or 2, then M_2 turns on, and BL_2 discharges through the following path. The rate of discharge is different for the read operation of 1 and 2, which is shown in Fig. 5. This is an inverting memory cell for which the inverted value of the data is obtained from the

BL_2.



(a) (b)

Figure 41: (a) Write, and (b) Read Operation of Proposed ternary 3T-DRAM

7.2 Simulation Results and Analysis

Different parameter values that have been used during the simulation are given in Table 19. Fig. 42 shows the transient response of the proposed DRAM cell for a single cycle. For three consecutive cycle of WL, three different data (0, 1 and 2) have been written and read. For the first cycle, 0 is stored in X and then in the falling edge of the WL, the bit-line holds itsâ pre-charged value. At the second rising edge of the word-line, write bit-line BL_1 is holding the value 1 which is read in the next falling edge of the WL by the BL_2. Similarly, at the third rising edge of the word-line, write bit-line BL_1 is holding the value 2 which is read in the next falling edge of the WL by the BL_2. The

difference between reading 1 and 2 can clearly be differentiating from the slope of the discharging curve.

Table 19: Different Process and Device Parameter Values

Temperature	25ÂºC
Supply voltage	1.2V
Channel length	16nm
Oxide Thickness	4nm
Propagation delay	50ps

Table 20: Simulation results for the ternary 3T DRAM for nominal conditions

Write time	31.776ps
Read sensing time	0.55675ns
Total Current	28.319nA
Total Power	32.2674nW

The simulated result such as write time, data sense time during read operation, and the total current are given in Table 20. These data are extracted considering the mentioned parameter values in Table 19. The write time or write delay is measured as the time required for the X node to reach to 50% value after the signal WL reaches 50% of its' value. And the read sensing time is dependent on the capacitor to be discharged to a certain value so that a sense circuit can sense the transition and decide. For that, we have calculated the read sensing time or read time as the time required by BL_2 to reach 20% of the data to be read. The total current is calculated as the current flowing from $BL_1 \rightarrow X$ and $BL_2 \rightarrow X$ for a total read/write cycle as shown in Fig. 42. Fig. 43 and Fig. 44

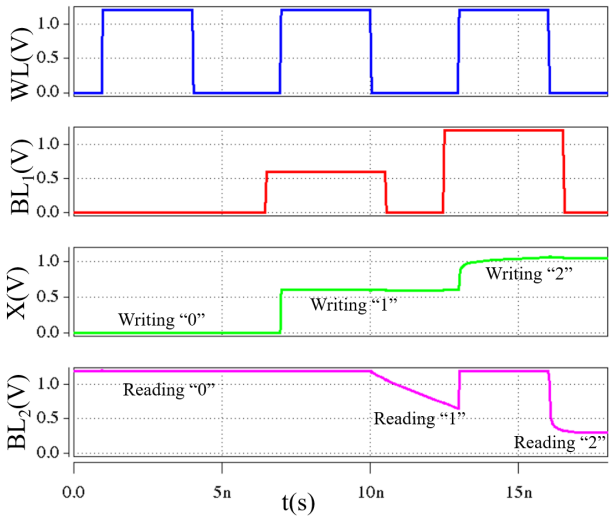


Figure 42: Transient response of proposed DRAM showing the read and write operation of 0, 1 and 2

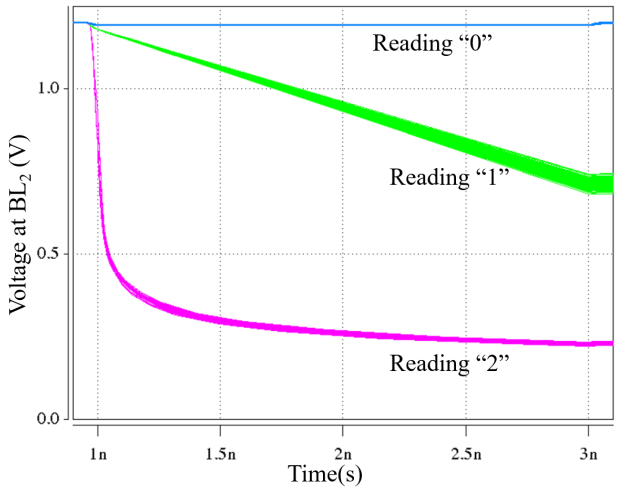


Figure 43: Read operation of the ternary DRAM for data 0, 1 and 2 following 100MC operation with different process variation

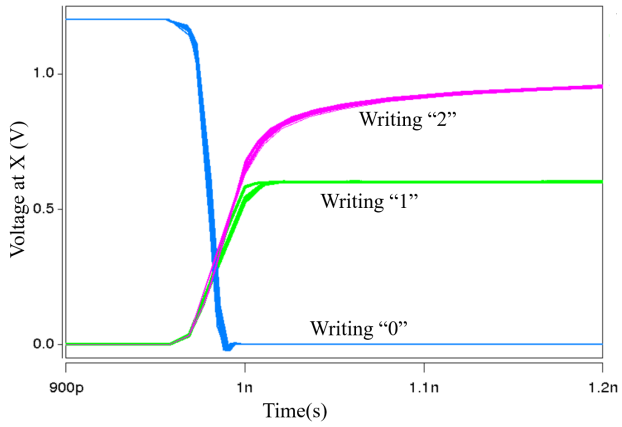


Figure 44: Write operation of the ternary DRAM for data 0, 1 and 2 following 100MC operation with different process variation

show the graphs of the reading and writing operation using 100 Monte Carlo simulations considering temperature, supply voltage, channel length, and oxide thickness variation. For the write operation, we have considered $2 \rightarrow 0$, $0 \rightarrow 1$, and $0 \rightarrow 2$ transitions. We can see from the graph that the transition between different states is most vulnerable in the state 1.

CHAPTER 8

CONCLUSIONS & FUTURE WORK

8.1 Summary

The exponential progress of the prevailing computing system is supposed to face some complications in terms of data density and physical challenges. If they cannot meet the newer demands, new computing paradigms will then be much needed. The present research works involving newer computing paradigms will be useful at that time. This paper shows the different techniques used in designing the multiple-valued logic besides explaining the basic concept of multiple-valued logic. Moreover, it also explains the detailed description of different techniques on a device level and circuit level to design ternary valued logic. The technologies explained in the paper can be divided into two major categories. One is the prevailing technologies like MOSFET, FinFET, FDSOI, SET, and RTD. And another one is emerging technologies like Memristor, CNTFET, QDGFET, GNRFET, etc. Among the prevailing technologies, MOSFET, SET, and RTD have been tried for a long time. Though SET and RTD hold huge promise in the field of MVL, using whole new technology which is completely different from the present CMOS technology would be a huge step. And it can lead to a different other fabrication complexity which was not seen with MOSFET technology. FinFET and FDSOI, on the other hand, improves the limitations that come with MOSFET without having to modify lots of fabrication techniques. In addition to this, they are already been used in place of MOSFET

in different sectors. On the other hand, among the emerging and futuristic technologies, carbon-based transistors hold the most potential for implementing MVL. Though CNTFET has been the topic of interest for a longer time than GNRFET, GNRFET has the advantages of a planner structure which makes it a more suitable substitute for MOSFET. But in terms of fabrication, the maturity of CNTFET is very much well ahead of GNRFET and other emerging technologies. The major drawback of the MVL system is the abundant usage of the binary system on most of the computing system. It might not be possible for the MVL system to replace the binary system at once, but MVL is already started to make its way especially in terms of MVL memory. As the operating voltage of the memory system is still high compared to the arithmetic system, the problem associated with the low operating voltage for MVL is not a big issue here. Also in the case of arithmetic circuits, ternary and quaternary logic circuits have been proposed which was proven to give very good results with low operating voltage. This paper presents the designs of a set of basic ternary logic gates (inverter, NAND, and NOR) and circuits (decoder, multiplexer, and half-adder) based on GNRFET. These particular set of basic gates and circuits are selected to establish the proposed design methodology. These basic gates and circuits can be utilized to implement any complex logic, arithmetic, and signal processing circuits. Here, the fundamental approach is to control the threshold voltage and other electrical properties of GNRFETs by changing the width of the GNRs to obtain different output levels. A comparative analysis between some of the proposed GNRFET based ternary logic gates and circuits and existing designs is performed in terms of delay, leakage power, total power, and power-delay-product (PDP). It is observed that

the proposed GNRFET based ternary gates and circuits offer significantly better results compared to similar gates and circuits based on CMOS and CNTFET technologies. The H-SPICE simulation and analysis are performed using a GNRFET model available on Nanohub, and the channel length for the device is selected to be 16nm. The proposed design approach can be extended to implement quaternary logic.

8.2 Future Work

However, it is essential to acknowledge that this paper is an attempt to establish the fundamental design concept of GNRFET based ternary logic gates and circuits. Some many issues and challenges need to be addressed before implementing more complex circuits like ternary full adders and complete ternary application systems. Implementing ternary memory with the proposed logic gates and circuits is another direction that can be pursued. As memory is the most critical part of any electronic system, increasing information and data storage capacity while decreasing delay and power consumption are the grand challenges for the memory designers. The ternary logic system is highly promising to resolve the grand challenges of the memory industry. It is also important to remember that the analysis techniques and design metrics for the MVL devices and circuits are still evolving. Our ongoing and future work is focused on addressing some of the issues and challenges mentioned above.

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