FUNCTION IMPLEMENTATION IN A MULTI-GATE JUNCTIONLESS FET STRUCTURE

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ABSTRACT

This dissertation explores designing and implementing a multi-gate junctionless field-effect transistor (JLFET) structure and its potential applications beyond conventional devices. The JLFET is a promising alternative to conventional transistors due to its simplified fabrication process and improved electrical characteristics. However, previous research has focused primarily on the device's performance at the individual transistor level, neglecting its potential for implementing complex functions. This dissertation fills this research gap by investigating the function implementation capabilities of the JLFET structure and proposing novel circuit designs based on this technology.

The first part of this dissertation presents a comprehensive review of the existing literature on JLFETs, including their fabrication techniques, operating principles, and performance metrics. It highlights the advantages of JLFETs over traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) and discusses the challenges associated with their implementation. Additionally, the review explores the limitations of conventional transistor technologies, emphasizing the need for exploring alternative device architectures.

Building upon the theoretical foundation, the dissertation presents a detailed analysis of the multi-gate JLFET structure and its potential for realizing advanced functions. The study explores the impact of different design parameters, such as channel length, gate oxide thickness, and doping profiles, on the device performance. It investigates the trade-offs between power consumption, speed, and noise immunity, and proposes design guidelines for optimizing the function implementation capabilities of the JLFET.

To demonstrate the practical applicability of the JLFET structure, this dissertation introduces several novel circuit designs based on this technology. These designs leverage the unique characteristics of the JLFET, such as its steep subthreshold slope and improved on/off current ratio, to implement complex functions efficiently. The proposed circuits include arithmetic units, memory cells, and digital logic gates. Detailed simulations and analyses are conducted to evaluate their performance, power consumption, and scalability.

Furthermore, this dissertation explores the potential of the JLFET structure for emerging technologies, such as neuromorphic computing and bioelectronics. It investigates how the JLFET can be employed to realize energy-efficient and biocompatible devices for applications in artificial intelligence and biomedical engineering. The study investigates the compatibility of the JLFET with various materials and substrates, as well as its integration with other functional components.

In conclusion, this dissertation contributes to the field of nanoelectronics by providing a comprehensive investigation into the function implementation capabilities of the multi-gate JLFET structure. It highlights the potential of this device beyond its individual transistor performance and proposes novel circuit designs based on this technology. The findings of this research pave the way for the development of advanced electronic systems that are more energy-efficient, faster, and compatible with emerging applications in diverse fields.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled "Function Implementation in a Multi-Gate Junctionless FET Structure," presented by Sehtab Hossain, candidate for the Doctor of Philosophy degree, and certify that in their opinion it is worthy of acceptance.

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ACRONYMS

JLFET	Junctionless Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MVL	Multi Valued Logic
IC	Integrated Circuit
GIDL	Gate Induced Drain Leakage
DIBL	Drain Induced Barrier Lowering
ALU	Arithmetic Logic Unit
TCAD	Technology Computer Aided Design
DOE	Design Of Experiment
NIR	Near Infrared Region
MTJ	Magnetic Tunneling Junction
STT	Spin Transfer Torque
IoNT	Internet of Nano-Things
SCE	Short Channel Effect
RDF	Random Dopant Fluctuation
WFV	Work Function Variance
DMG	Dual Metal Gate
XRD	X-ray Diffraction
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
ADC	Analog Digital Converter
SOI	Silicon On Insulator
MHK	Metal High K
DSL	Dual Stress Liner
HARP	High Aspect Ratio Process

ULK	Ultra Low K
RF	Radio Frequency
NBTI	Negative Bias Temperature Instability
BTI	Bias Temperature Instability
EOL	End Of Life
CP	Central Process
SC	System Control
BTBT	Band To Band Tunneling
HCD	Hot Carrier Degradation
TAT	Trap Assisting Tunneling
NSFET	Nano Sheet Field Effect Transistor
HNM	Hold Noise Margin
RNM	Read Noise Margin
WM	Write Margin
FEOL	Front End Of Line
BEOL	Back End Of Line
LFET	Lateral FET
VFET	Vertical FET
FDSOI	Fully Depleted Silicon On Insulator
QCL	Quantum Cascaded LASER
ALD	Atomic Layer Deposition
CVD	Chemical Vapor Deposition

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CHAPTER 1

INTRODUCTION

With the Integrated Circuit (IC) burgeoning, Moore's law has slowed down. Relentless scaling down of IC appears to be difficult to follow Moore's law. To address this problem, some solutions are provided. Some alternate solutions provide novel devices like Multi-Valued Logic (MVL), and Magnetic Transistors. But these devices have their limitations. Embedding logic devices is one of the solutions. We propose embedding logic standalone device. Instead of multiple devices to implement a Boolean logic, the embedding logic device has only one device to perform Boolean logic. However, a standalone device was capable of performing elementary Boolean functions like NAND/NOR. In this research, we extend our research to complex Boolean Logic which will be capable of performing multiple Boolean Logic operations.

1.1 Problem Statement

Integrated Circuit (IC) has changed the socio-economic perspective of the electronics industry. The advent of IC leads to the electronics device revolution and paved the path for advanced technologies. The advancement of IC leads to scaling down transistors to reduce power consumption and increase transistor counts. Transistor count plays a crucial role in processor speed and IC throughput. The transistor industry follows the rules of Moore's law as a standard for IC production and the advancement of IC. Progress was made gracefully until the advent of the 20 nm technology node. From 20 nm technology, scaling down the technology node becomes very complex with excessive

complex manufacturing processes along with circuit integration. In the case of manufacturing, oxide thickness becomes a problem. As advanced technology nodes have much thinner gate oxide, it was very difficult to grow a one or two nm Silicone dioxide (SiO_2) layer. To address this problem, the gate oxide is changed to Hafnium Oxide (HfO_2). Along with manufacturing problems, device physics problems also arise. The advanced node transistors suffer from short channel effects like Gate Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), punch through, etc. The short channel effects problems are resolved eventually but new problems appear. The problem of integration in the circuit appears to be greater in this regard. As transistors' gate pitch is getting smaller, integrating whole transistors as a circuit becomes a challenge. After integration, power consumption increases as the transistor number increases. Aggressive scaling down makes the gate size so short that it is very close to an atomic distance of Silicon. Increasing transistor number also raises the problem of excessive heat and heat transfer becomes an issue. As the scaling down process scales down all physical parameters, each technology node demands complete alternation of manufacturing processes.

1.1.1 End of Moore's Law

The major milestone in semiconductor electronics is the invention of CMOS in 1963. In 1971, Intel introduced the first commercial CPU (Intel 4004) and in 1976 RCA started the fabrication of CDP 1802, the first Si CMOS CPU. Since then, the transistor count doubled every two years – a trend known as Moore's law. In his 1975 IEDM paper, Gordon Moore discussed the three measures to be taken to continuously increase the number of transistors per chip, which are (i) shrinking the size of the individual transistors

(scaling), (ii) increasing the chip area, and (iii) improving device and circuit design. At this point, we are very close to the edge of scaling and it is feared that Moore's may no longer be applicable.

Fig. 1 shows the evolution of CPU transistor count and MOSFET gate length, indicating that Moore's Law and CMOS scaling are still alive.

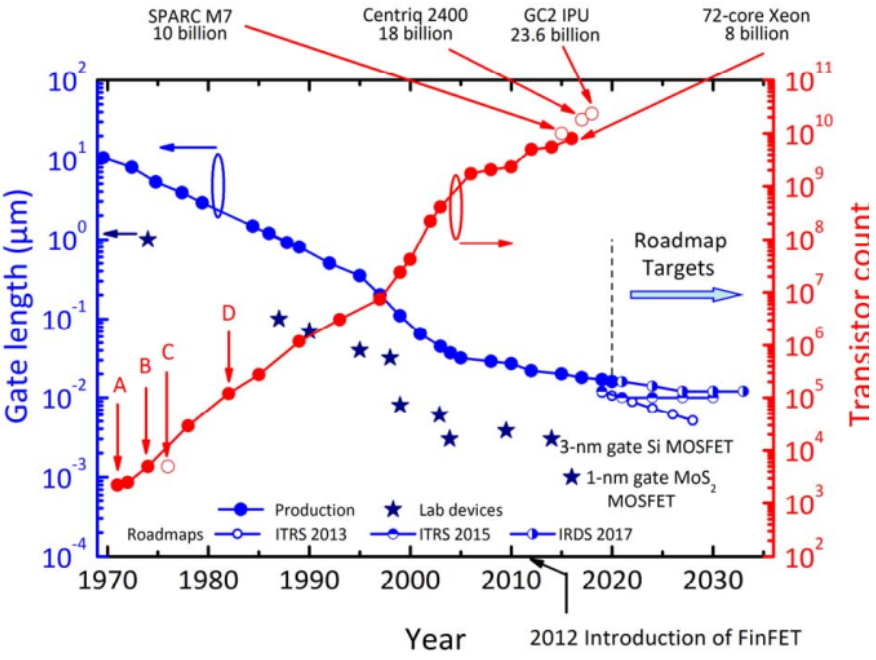


Fig 1. Evolution of CPU transistor count and gate length (production stage). Experimental CMOS cases are also shown [1]

Gate length scaling represents an achievement of engineering art. Conversely, it is a kind of "steamroller tactic" that sooner or later will become inappropriate. With the increasing demand for computation and processing density and transistor count increased relentlessly not only for CPU but also for GPU. As GPU has a different architecture than CPU, its architecture and circuit are different. Fig. 2 depicts the chip area for CPU and GPU. It is noticed that after 2010 CPU and GPU areas increased parallelly.

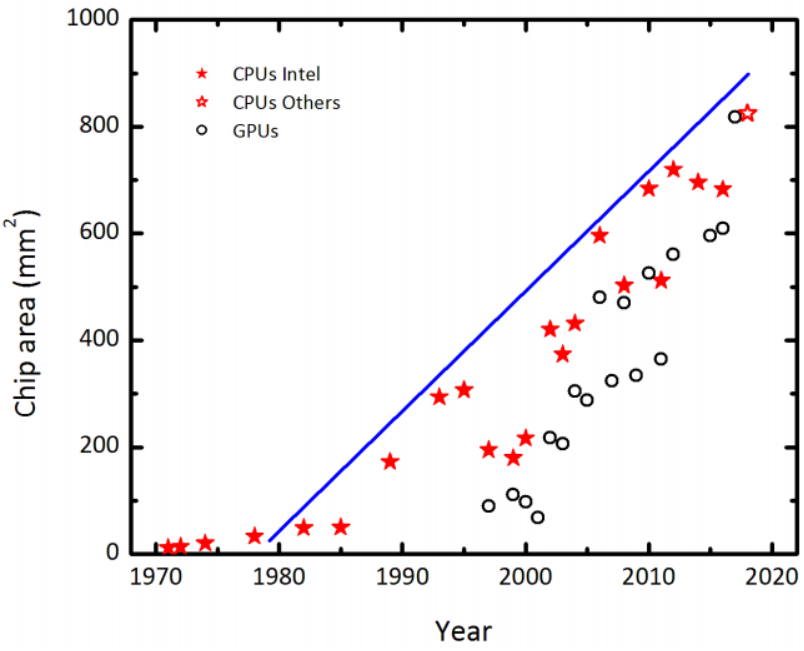


Fig 2. Evolution of CPU and GPU according to Chip area.[1]

The sole purpose of scaling is to increase performance and decrease cost. With the increment of transistor count, increase the performance. With the advent of FinFET, transistor count skyrocketed as well as performance. Fig. 3 exhibits the evolution of transistor count for CPU and GPU.

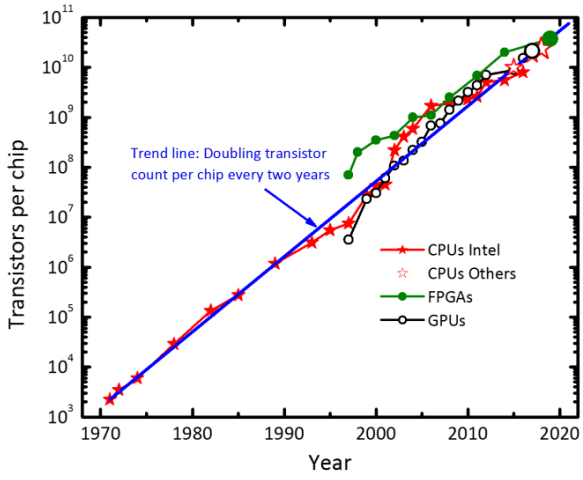


Fig 3. Evolution of Transistor count in CPU and GPU [1]

Amid this situation, the alternate solution is a hardware accelerator and alternate channel material.

Hardware accelerators are not general-purpose CPUs. GPU, TPU, and FPGA will be categorized as hardware accelerators. Because of special architecture, hardware accelerators are used for heavy computation. Specially TPU is used for heavy computation. TPU has a special architecture of tensor that is suitable for matrix multiplication to speed up the computation. Several alternate material were examined to replace silicon channel. One path of this research is directed to replacing the Si nMOS and pMOS channels with channel materials with light electron/hole effective masses leading to enhanced electron and hole mobilities. Options are (i) using Ge for pMOSFETs (Ge has the highest hole mobility of all semiconductors) and III-V semiconductors for nMOSFETs. (ii) using Ge channels for both nMOS and pMOS (iii) keeping Si as the channel material of choice for nMOSFETs and using Ge for the pMOS channels. Among alternate materials Graphene, MoS_2 WS_2, and WSe_2 are notable. Semiconducting 2D materials such as MoS_2, WS_2, or WSe_2 exhibit several features for ultra-short MOSFET channels: (i) They are ultimately thin, which leads to excellent electrostatics and superior suppression of short-channel effects. (ii) While the carrier mobility in most semiconducting 2D materials is lower compared to bulk Si, it is higher than in ultra-thin body Si. (iii) some 2D materials offer much heavier carrier effective masses m_{eff} than bulk Si, Ge, and III-V semiconductors.

Although an alternate approach to replace Si transistors is relentless it is still not suitable for industrial applications. Now semiconductor companies like TSMC and Samsung broke Moore's law and progressed to 2 nm technology node. Fig. 4 depicts the performance and power consumption improvement over the technology node [2].

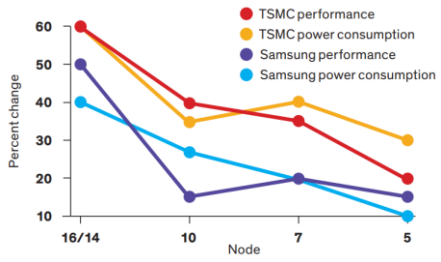


Fig 4. Performance and Power consumption improvement over Technology node [2]

1.1.2 Quantum Mechanical Problem

The major quantum mechanical effects are gate oxide tunneling, energy quantization in substrate and polygate, and source-drain tunneling.

A. Quantum mechanical tunneling from source to gate oxide: Due to the aggressive scaling down of transistor, gate oxide is ultra thin. For ultra thin oxide layer electric field is very high. Hence, the charge carriers in the channel will directly tunnel through the interface barrier to the gate oxide.

B. Energy Quantization in the Substrate: Ultra thin gate oxide results in very high electric fields in the silicon/silicon oxide interface and hence the potential at the interface becomes steep. As a result, formed a potential well between the oxide field and the silicon potentials. During the inversion condition, the electrons are confined in this potential well. Due to confinement, the electron energies are quantized and hence the electrons occupy only the discrete energy levels. This results in the electrons residing in some discrete energy levels which are above the classical energy level by some fixed value of energy as shown in Fig 5.

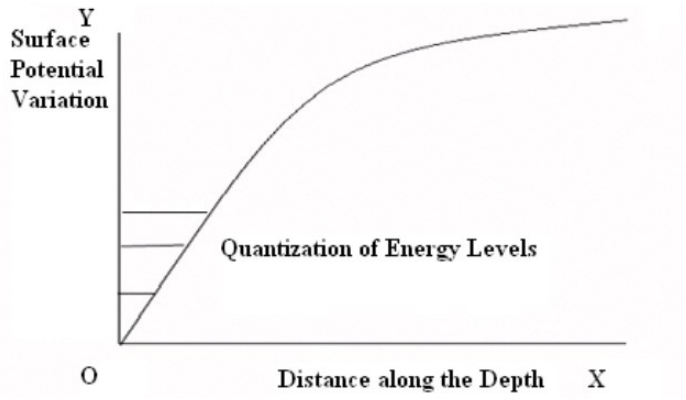


Fig 5. Energy Quantization in the substrate[11]

C. Displacement of inversion charge density into the bulk: Due to Energy Quantization, charge carrier density at the surface becomes less than the desired value from the classical analysis. The charge distribution in the case of classical charge distribution and Quantum Mechanical Charge distribution is shown in Fig. 6

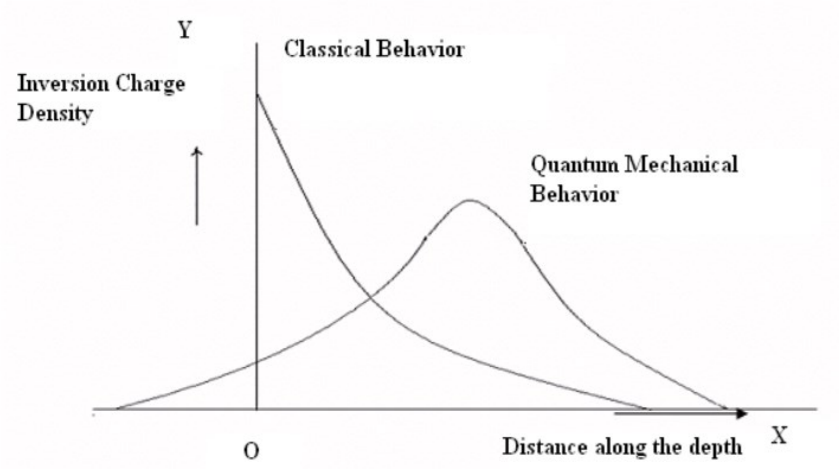


Fig 6. Electron Concentration Distribution in the Silicon Substrate in Classical and Quantum Mechanical Cases. [12]

D. The quantum mechanical tunneling from source to drain in the substrate: In sub 10nm channel length, the charge carriers are no longer obstructed in the source potential well and start tunneling quantum mechanically through the barrier between the source and drain. So, the gate voltage has no control over the MOSFET operation.

E. Threshold voltage and drain saturation voltage shift: The shift in the surface potential due to the quantum mechanical effects changes the threshold voltage as the effective oxide thickness increases. Operating the MOSFET at such a low dimension will cause energy quantization in the oxide/substrate interface. The confining of the charged carriers in the potential well will raise the energy of the electrons because of the quantization of energy and electrons will occupy much higher energy levels for which a different potential is required to turn on the transistor. The energy quantization process will decrease the drain current also. The drain to source saturation voltage will fall under such conditions.

1.2 Motivation and Scope

To enact Moore's in the advanced nodes, several forms of nanodevices have been introduced. But all alternate nanodevices have their drawbacks. Some beyond CMOS devices like Ferroelectronic transistors and Graphine spintronics are noted to be mentioned. An alternate approach like Beyond CMOS technology has its fair share of limitations [14]. Keeping up with Moore's law is crucial for the semiconductor industry for the production and development of IC chips. Our research is inspired by the downfall of Moore's Law. With the downfall of Moore's law, the semiconductor industry is facing a challenge in circuit integration and the scaling down of IC. To keep up with Moore's law, a different paradigm is required for circuit integration. Each technology node requires a different fabrication process (lithography) along with different circuit integration rules. Implying Moore's law needs a specific protocol and paradigm to be compatible with all technology nodes. This problem interested us to work on a special paradigm that will be compatible with a specific technology node and after development, it will be advent as a generic paradigm for all technologies. There is plenty of room left for working on this paradigm and protocol.

The paradigm requires extensive insight into the specific technology node. After selecting the technology node, the standard rule should be enforced for the devices. After envisioning the design for the device, at first elementary devices like NAND, and NOR will be put into the examination. Achieving successes from the elementary devices by examining AC and DC characteristics of the devices, the design of the experiment will be forwarded to the complex logic like carry circuit, Adder, etc. After achieving elementary and complex devices, the research will be moved to greater circuit integration like

Arithmetic Logic Unit (ALU). Examining greater circuit integration deals with extensive calibration of power and distribution of clock frequency. In the case of power, for each elementary and complex device, the maximum, minimum, and typical power must be determined. The same goes for the frequency. High, low and typical frequencies for each device need to be determined to get the process flow of the whole technology node. After achieving the process flow of a technology node, device integration in the whole circuit along with clock frequency distribution should be taken to account. While implementing clock frequency distribution, a lot of complexities arise. Circuit ringing, white noise generation, and crosstalk are a few to mention. This research initiates from device designing to characterization and implementation of the circuits.

1.3 Summary

In this research, elementary and complex logic devices are being designed and studied for AC and DC characteristics. At first, the paradigm is initiated and elementary logic devices are presented with their AC and DC characteristics to validate the research. Then the research moved on to the complex logic. After several rounds of tuning complex logic is achieved. After examining AC and DC characteristics the devices are integrated with circuits with TCAD. The devices are integrated with an inverter to form a circuit. The purpose of an inverter is to get a full swing of one and zero from the output. A full swing will produce a strong one and zero output which is very important for logic output. A noisy input will produce noisy output. That is why an inverter plays a very crucial role in the circuit. The whole circuit integration part is done in TCAD. Applying circuit integration

and generating netlists from TCAD is a very novel approach. After circuit integration, the whole design of the experiment (DOE) will be examined with pulse input to determine the gain and efficiency of the circuit. In this stage, several rounds of examination are done to fine-tune the gain and accuracy of the DOE. Ensuring gain and accuracy, the circuit will be targeted for greater integration of circuits like the Arithmetic Logic Unit (ALU). Several series of tuning for gain and accuracy will be performed over ALU. Then the ALU design will be sent to some Microchip company to fabricate chips. Receiving the batch of chips, will be examined to check the functionality.

1.4 Organization

In this dissertation, we propose a paradigm that is compatible with contemporary technology nodes and keeps Moore's law implemented. With this new paradigm, elementary and complex logic devices are designed and AC and DC characteristics are examined. The dissertation is organized like this: chapter one is Introduction with a Problem statement, motivation, and summary.

Chapter 2 describes an extensive elaboration of literature analysis. At first, starts with related work that is related to embedded devices. The device itself can work as a Boolean logic device. Standalone devices are extensively discussed in this section. Then Insight into gate material and gate oxide is discussed. Each gate material has its features and for standalone devices, high work function material is selected. For the gate oxide, a high dielectric material is always desired. Our device is based on a 14 nm technology node.

In this chapter, we discussed some advanced nodes like 7 nm, 5 nm, 3 nm, and 2 nm technology nodes.

Chapter 3 discussed the principle of crosstalk. As crosstalk is the main principle for this research, it is discussed very elaborately in this chapter. The mechanism and outcome of crosstalk are discussed in this chapter. Chapter 4 discusses the implementation of crosstalk in logic circuits with the outcome and circuit performance.

Chapter 5 is about device architecture. At first, device parameters and material descriptions are discussed. Device physics mechanisms along with some crucial principles like the Schrodinger equation, Poisson Equation, and continuity equations are elaborated. Device architecture for elementary logic devices and complex logic devices are discussed here. The devices also possess polymorphic properties. After changing the frequency of the device, the device behaves differently and shows a polymorphic property. It is found that each device shows different polymorphic properties.

Chapter 6 is about the environmental setup for simulation. The environment set up for elementary and complex logic circuits is discussed here. After discussing the environment, elementary and complex logic device parameters along with AC and DC characteristics are illustrated with I-V characteristics. Chapter 7 is Conclusion and Future Research. For future research, a roadmap of chip fabrication and chip batch process analysis is in process. This research has a roadmap for fabrication along with the mass production of chips. After getting a batch of chips, chips will be examined for performance and validity.

CHAPTER 2

LITERATURE REVIEW

In this chapter, we discussed literature discussion. In Chapter 1 it is stated that this research is on standalone device nanodevice. This chapter is divided into three parts. In this chapter, state of art-related works on standalone devices is discussed. Nanodevices are strongly dependent on the material property for performing a specific function and gate material and gate oxide are very crucial in this regard. In the second part of the chapter, these materials are discussed. The last part of this chapter is about advanced technology nodes and their pivotal specialization and parameters. In each section, we presented related works, how our research is related to that research, and how our research is novel.

2.1 Related Work

The early research of standalone devices is predominantly in the health sector [15-20]. Most of the standalone devices in the biology sector are to measure vital parameters like pH and others. A plasmonic nanodevice is fabricated whose input is all-optical and the purpose of the device is to measure pH. Embedding this pH meter inside a sample like a plant or animal cell to monitor the biological change[15]. Au nanoshell works as a whole as a standalone device to perform as a pH meter. In some literature [15-18], quantum dots, and nanowires are used for a standalone device. QD along with other materials is used for photoluminescence. The size and surface-to-volumes ratios of QD as a standalone device are used for displaying biologicals like protein, peptides, and DNA. Photocatalyst is also

regarded as a standalone device [18]. This photocatalyst work in Near Infrared Region (NIR). There is plenty of room left for improvement. Chemical variation will come up with completely different functions. The authors designed and integrated multiple functional components into a single nanostructure which offered a new avenue in the field of photocatalyst[17]. Pt/Si/Ag is used as the catalyst. Pt/Si/Ag catalyst with TiO_2 produces the most stable photocatalyst. This heterostructure with different ratios varies in efficiency. But TiO_2 based photocatalyst is only active in UV and near UV regions and thermodynamics uphills and downhills.

Magnetic Tunneling Junction (MTJ) is also used as a standalone device [18]. MTJ is used as Spin Transfer Torque Magnetic Random Access Memory (STT - MRAM) which is considered a pivotal breakthrough in embedded standalone memory. MTJ's basic cell is used in low-energy stochastic regimes and implements a stochastic function. This device is then used as a neuromorphic chip that retains memory and performs logic functions. From this device, an artificial synapse is built for higher functionality. The MTJ device was arranged in one transistor-one resistor architecture. Although this architecture has area benefits, it is suppressed by other difficulties like in need for complex read circuitry and break down of crossbar.

In this era of the Internet of Things (IoT) nanodevice is also used in this regime [19,20]. Nanodevice is realized in this IoT regime and addressed as the Internet of Nano-Things (IoNT). This idea utilizes the performance of nanosensors, nano processors, nanoantenna, nanobots, and nano memory and is implemented mostly in the healthcare field to revolutionalize the healthcare system. The nanodevice acts as a standalone device that will measure the vital signs of a patient and sends them to the servers for further

examination. This nanodevice is constrained by limited power, communication range, and processing. This standalone device, the IoNT is connected with the nanonetworks. These nanonetworks are responsible for communication and processing to overcome the limitation of a standalone device. Conventional TCP/IP protocol is not suitable for this nanonetwork as TCP/IP protocol is for general-purpose processing and nanonetworks have a limitation in this issue. So new networks with nanoantenna and nanodevices are deployed and IoNTs' are worked as a single node in this network. For nanonetworks, a layer-based model as network protocol is deployed. The purpose of this IoNT is drug delivery and disease detection. [20] discussed the deployment of IoNT networks. In their research, they addressed the scalability and complexity of the architecture. A layered approach of Software Defined Network (SDN), Internet of Things (IoT), and Fog network is realized to deploy IoNT. Secondly, they proposed a set of functions and used cases to realize the network. Lastly, they came out with several avenues of research in the field of IoNT and pointed out some problems and limitations in this IoNT field.

2.2 Review of Gate Material & Gate Oxide

Aggressive scaling down of the technology node depends on several pivotal parameters. Gate material and gate oxide are one of them. With the advent of the latest technology node, gate material and gate oxide are altered sometimes. In this section, the importance of gate material and gate oxide for a device is discussed. The advancement of technology nodes needs optimization of physical parameters like dielectric constant, and work function. As these parameters are intrinsic parameters of materials, materials need to be altered. Gate materials are chosen for the specific value of work function and gate oxide is chosen for the specific value dielectric constant. At first, the importance of gate material is discussed then gate oxide.

2.2.1 Importance of Gate Material

With the progression of technology nodes, device architecture is changed. From micron technology to nanotechnology, a transistor device is changed from CMOS to FinFET. In [21] 35 nm CMOS device is fabricated where Silicon On Insulator (SOI) is the platform for the bottom-up approach. The paper gave directions toward the advanced node by suggesting that changing gate oxide will increase the performance. In this paper, the gate oxide is in Armstrong range to control the gate. The gate length was 35 nm and Co-silicide is used as the gate material. The device appears to perform well with On current of 500 μA/μm and Off current of 600 nA/μm. Technology from 45 nm, polysilicon is used as gate material [22].

Different gate materials appear with different Short Channel Effects (SCE) [23]. In [23] authors compared several gate materials' performance. They studied from polysilicon to TiN and Ta/Mo. TiN has a problem with Random Dopant Fluctuation (RDF) and Work Function Variance (WFV). TiN and Dual Metal Gate (DMG) like Ta/Mo suffer severely from WFV [22]. The source of WFV is granularity difference. TiN has a small granularity difference but Ta/Mo has a granularity difference of 10 nm. As a result, Ta/Mo gate suffers from WFV more than TiN. Observing these findings, they fabricated a finFET with DMG of TA/Mo and examined the analog performance of the finFET. Parasitic resistance (R_p) is the main problem for this device. The reason for R_p is the fluctuation of fin thickness, T_{Fin}. The device suffered from other problems like Gate length fluctuation, granularity difference, RDF, and WFV.

In [24] authors reviewed different architecture and materials for FinFET. The authors discussed different gate materials and gate oxides. After rigorous reviews, they came out with their Multigate FinFET (MuGFET) of 22 nm technology. Their FinFET had a gate length of 22 nm and the source and drain were heavily doped but the Chanel was undoped. To ensure better On current, the gate is surrounded by spacers of Si_3N_4.

To tune gate metal work function, several procedures can be addressed [26]. In [26] the authors fabricated a P-type double gate FinFET. The FinFET had a gate length of 20 nm

and was made from Mo. The authors tuned the work function of gate material, Mo to tune the threshold voltage, V_t. Applying the device in a Nitrogen environment for special treatment and then etching the device with Hydrogen gave the authors got the freedom to tune Mo's work function. For regular Mo, the work function is 5 eV and after treating their device with N_2 and H_2, they got the work function dropped to 4.4 eV which is an ideal Work function for FinFET. With gate work function tuning, they tuned V_t. After treating V_t, On current improved by a large amount. In conclusion, the authors suggested that this fabrication process can be adapted to achieve N-type dual gate FinFET.

Sometimes aggressive scaling down of the gate length occurred [27]. Here the authors fabricated FinFet with a 10 nm gate length. This aggressive scaling down came out with the cost of a very steep subthreshold swing and Drain Induced Barrier Lowering (DIBL). Although On current and Off current value is within the limit but the device got some severe issues and will be a fabrication nightmare for the device physicists.

The researchers came out with new fabrication approaches [28]. Here the researchers appeared with a self-aligned double gate along the source drain with a gate length of 17 nm. In addition, they experimented with $Si_{0.4}Ge_{0.6}$ as gate material and SiO_2 as spacers. The fabrication segment is complex with Boron doped $Si_{0.4}Ge_{0.6}$, electron beam lithography several steps of SiO_2 hard mask to protect some parts of the device. The extremely meticulous procedure was followed in every step of fabrication. As a result, parasitic resistance decreased drastically. The device came out with better DIBL, GIDL, and subthreshold swing. After rigorous examination, the researchers suggested that a self-aligned double gate can suppress SCE effectively, $Si_{0.4}Ge_{0.6}$ can produce proper V_t even in the ultrathin Fin body and if a gate is aligned with the source-drain, R_p will be much lesser. With these findings, the authors envisioned the next generation of FinFET.

In summary, the gate material, and gate length play a crucial role in device operation. They influence V_t roll off and the gate length ratioed with Fin width can lessen parasitic resistance to a great extent. As a result, from planar CMOS architecture to FinFET design gate material is changed quite frequently. Table 1 is a list of gate materials along with their work function [29].

Table 1. List of Gate material along with work function

Gate Material	Work Function
Mg	3.66
Mg/Al_2O_3	3.6
Mg/SiO_2	3.45
Mg/ZrO_2	4.15
Al	4.28
Al/Al_2O_3	3.9
Al/SiO_2	4.14
Al/Si_3N_4	4.06
Al/ZrO_2	4.25
Ta	4.25
Ta/SiO_2	4.2
W	4.63
W/SiO_2	4.6-4.7
Mo	4.95
Mo/SiO_2	5.05
Mo/Si_3N_4	4.76
Mo/HfO_2	4.76
Pt	5.65
Pt/SiO_2	5.59
Pt/HfO_2	5.23
Pt/ZrO_2	5.05
Ni	5.04
Ni/Al_2O_3	4.5
Ni/ZrO_2	4.75
Au	5.31-5.47

Gate Material	Work Function
Au/Al_2O_3	5.1
Au/ZrO_2	5.05
Hf	3.95
Hf/SiO_2	4
Ti	4.33
TiC	5.0
TiN	4.4-4.6

2.2.2 Importance of Gate Oxide

Since the era of planar CMOS, gate oxides are used as a dielectric between the body/ Fin and the gates. With a polysilicon gate, SiO_2 is used as a gate oxide. With the advent of modern technology nodes, the gate oxide is also changed. The purpose of gate oxide is to build electrostatic. By controlling electrostatic, we control gates.

In [30] the author discussed the importance of gate oxide. Here the performance of SiO_2 and La_2O_3 is compared as the gate dielectric. According to the author's claim, La_2O_3 is better than SiO_2. As the research progresses, he claimed that La_2O_3 has a problem with getting hydroxide as the oxide is hydrophilic. This rare earth element with ternary oxide has another problem of changing chemical composition in varying temperatures. With varying the chemical composition, their permittivity also changes which also affects the dielectric constant. Examination with X-ray Diffraction (XRD) and Atomic Force Microscope (AFM), confirms the varying crystallization for lanthanum-based tertiary oxide. This report gave a deep insight into lanthanum-based oxide as a dielectric.

In [31] the authors discussed the effects of dielectric in a charge pump circuit. A charge pump circuit is a vital part of some memories like EEPROM. The gate oxide is responsible for junction breakdown voltage and operation of the charge pump circuit. The authors proposed a new charge pump circuit that will optimize supply voltage and efficiency. The authors went through several circuit architectures and compared the performance. With this research, they realized that their pump circuit is suitable for only low voltage. With a specific value of oxide thickness, they can reach maximum pump gain.

The ultra-thin oxide is used for the semi-empirical model and physics is analyzed [32]. The authors examined the effective mass of electrons in an ultra-thin gate oxide and came out with an electron model based on the device physics. The model can accurately describe electrons from the valence band (EVB), electrons from the Conduction band (ECB), and holes from the valence band. For this model a dual gate model with varying oxide thickness as well as gate polysilicon composition, $Si_{1-x}Ge_x$. The ultra-thin region's I-V and C-V profile is examined for continuous equation and Quantum correction is implied to get ballistic transport as well as quasi ballistic transport. The Quantum mechanical simulation is also addressed in this work to get a compact formula for the device. The prime reason for ultra-thin gate oxide is to increase the tunneling current. This research work emphasizes two main points:

1. The relative significance of different tunneling components
2. The sensitivity of tunneling current on oxide thickness

The device performed well with significant tunneling current increment but was not free from other short channeling effects.

Gate oxide defects can cause severe defects in the nanodevice [33]. The uneven thickness will cause an electron trap that is detrimental to any device. The Defected oxide layer like gate oxide short will cause stuck an error problem. As a result, the device needs to be discarded. The authors suggested several examinations to detect this defect. One is the measurement of I_{DD}. An increment of I_{DD} denotes gate oxide short. The authors suggested that IC designers should take this issue into account.

Table 2. Dielectric Constant of Some Gate Materials [34]

Material	Dielectric Constant, k
SiO_2	3.9
Si_3N_4	7
Al_2O_3	9
Ta_2O_5	22
TiO_2	80
$SrTiO_3$	2000
ZrO_2	25
HfO_2	25
$HfSiO_4$	11
La_2O_3	30
Y_2O_3	15
a-$LaAlO_3$	30

Table 2 contains a list of Gate materials and corresponding dielectric constant. From Table 2. We can select gate material to get a specific amount of electrostatic potential.

2.3 Advanced Technology Nodes

With the progress of technology, technology nodes moved from micron to nanotechnology. In micron technology, transistors are comparatively simpler in paradigm and gate length was regarded as technology node identity. Day by day the gate length decreases in microns as well as technology node is changing. The micron technology nodes are based on CMOS technology and the gate length is in microns. With the advent of

nanotechnology, the gate length plummets in nanometer. As the name suggests, the gates are in nanometers. But in the nanotechnology node, the transistors architecture gets complicated due to SCE. As a result, with the progress of technology node architecture is changed rapidly. From micron technology to nanotechnology CMOS was the dominant device up to 22 nm technology node. For analog applications, 45 nm is a very popular and well-matured technology. 45 nm technology analog devices like Analog to Digital Converter (ADC) and analog filters give high gain and steady performance. From 22 nm technology node, FinFET is dominant as nanodevices. 14 nm technology is very popular in commercial avenues, especially in the processor industry. At this moment 7 nm technology is already commercialized in all processors including desktop processors, cell phone processors, and other electronic devices. In this section, FinFET of some major and advanced technologies are discussed below.

Advanced MOSFET with several architectures related to gate engineering is analyzed in detail [35]. To decrease SCE, several architectures ranging from Double gate CMOS, Trigate CMOS, and Gate All Around are being studied along with their On state current, Off state current, and $I_{On} - I_{Off}$ ratio. Besides these analog and RF characteristics were examined. The authors also examined several insulator physics like Silicon On Insulator (SOI), Bulk CMOS, and Junctionless CMOS. The authors claimed that GAA architecture is most proficient in channel utilization and channel width can be utilized in this paradigm most graciously. Polysilicon and dual gate material $Si_{1-x}GE_x$ was used and it is noticed that different architecture are proficient in different parameters. Junctionless Double Gate had the lowest SS and the highest I_{On}-I_{Off} ratio. The lowest DIBL is obtained from graded channel dual gate material junctionless CMOS. The authors remarked that multi-material gate transistors had high potential as next-generation technology nodes.

SRAM with low power was built with 45 nm technology [36]. The authors pioneered a new technology of third optional gate-oxide for high-speed performance. The device operates in 1.1V and with low K gate oxide. The whole device is developed on (100) orientation of the substrate with a focus on process simplicity. Strain engineering was also implied to get reliability. With a meticulous manufacturing process, the device showed excellent performance in mixed-signal applications.

The authors studied with Silicon-Germanium source/drain for investigating layout dependencies. Stress engineering was extensively used through SiGE to examine the performance with the paradigm of the nested transistor. The authors claimed that increased recess depth and Ge concentration gave higher stress and there is an optimal recess for that optimal stress can be applied. Stress is very crucial for increasing the mobility of the carriers. The Mobility of carriers is dependent on channel stress. With these modifications, p-type transistor gained a higher saturation current [37].

32 nm technology node consisted of extreme level stress engineering and some other device physics engineering like Metal High K (MHK), Ultra Shallow Junction (USJ), Dual Stress Liner (DSL), High Aspect Ratio Process (HARP), Ultra Low K (ULK) integration, etc. For the case of MHK with different stacks, introduced some problems in the device like Vt roll-off, device reliability, mobility degradation, etc. [38]

The effect of alpha particles in 32 nm technology nodes is researched extensively [39]. By introducing radiation particles like alpha particles and neutrons, the upset time of an SRAM is addressed [39]. The upset time is responsible for the stability of SRAM. The appearance of noise particles affects the storage capacity of SRAM and produces logical errors in transient time which is considered a Single Upset Event (SEU). This research studied elaborately about this SEU. Masking like electrical masking, and logical masking block the propagation for SET. The upset time is more vital for combinational logic than sequential logic. The radiation is applied to four batches of chips, and it was observed that the sequential SER is independent of the clock speed, but combinational SER is dependent on clock speed. The neutron combinational SER is 2x time higher than the alpha particle SER [39].

The breakthrough happened in the 22 nm technology node. The transistor paradigm shifted from planar architecture to 3D architecture and FinFET architecture gave the cutting-edge technology in this regard [27]. Several variants of FinFET like Pi, Trigate, Gate All Around (GAA), etc. were studied in detail and it was noticed that vertical transistor offered 50% improvement in the area of density, reduced capacitance, and enablement of new materials. Due to new architecture and new fabrication processes in the area of lithography and annealing are introduced. With these improvements, some

problems arise like Random Dopant Fluctuation. 22 nm technology node also makes a bridge between analog and digital signals. This node can produce a better cut-off frequency to implement in the Radio Frequency (RF).

The change of architecture appears with several problems in the 22 nm technology node [28]. To follow Moore's law dimension is reduced. As a result, the drain comes close to the source and increases DIBL. Thinner gate oxide causes gate leakage current. As a solution, High K dielectric materials are proposed. Another problem is the Vt roll-off. For low Vt, Off current increases but for high Vt On current decreases. So The On-Off ratio is needed to be adjusted. These problems' solutions are provided by the authors. Adopting those solutions, SRAM with FinFET was developed and for drain leakage current, the Fin ratio was optimized. In these ways, robust FinFET was produced.

Stress engineering was implemented to increase the performance of 22 nm node [29]. The authors tried different materials rather than Silicon for their transistors and they examined III-V materials like GaAs. In this research [42], the authors implied stress through wafer bending. At first, a Silicon wafer was used as a substrate, and stress is introduced to it then GaAs layer is imprinted on the wafer. On top of the device layer, FinFET is introduced that had InGaAs channel. After that, the Density of State (DOS) was examined. It is observed that electron density is much higher in X and L valleys than in Γ valley. It was also noticed that under large uniaxial stresses, a saturation point appears, and after that DOS becomes degraded which is the opposite of biaxial composite stress. Hole mobility was also examined and found that both cases of electron and hole mobility are similar to Silicon ones. Applying this stress, PMOS performs better than NMOS.

With advanced nodes like 22nm and 14 nm, some new problems also come to the surface. Negative Bias Temperature Instability (NBTI) is one of them [30]. NBTI is responsible for Vt shift (ΔVt) and subthreshold slope shift (ΔSS). Various benchmark circuits are synthesized to analyze the effect. MOSFET aging like Bias Temperature Instability (BTI) is a pivotal reliability issue and NBTI is one of them. NBTI is predominantly governed by the generation of interface traps(ΔN_{IT}). The examination of NBTI is important for determining the device's end of life (EOL) and also measuring timing violations. To prevent this violation tiny time guard band is provided. As timing

violation happens for NBTI Vt increase with time and makes the transistor slower and the static power also degrades. With TCAD, authors examined NBTI and improved aging aware cell library, considering problems like ΔSS, ΔVt, transconductance, linear drain current (I_{DLIN}), saturation drain current (I_{DSAT}), and gate-drain capacitance (C_{GD}) [43].

IBM modified its z14 microprocessor with 14 nm technology node. With this advanced node, many improvements are implied on z14. Most of the improvements were arranged in Central Processor (CP) and System Control (SC). There were also improvements in the area of design methodology, hierarchy optimization, hierarchy management, and timing optimization. Using 14 nm technology, IBM managed to have a breakthrough in their z series microprocessor[44].

Defects in 14 nm technology nodes are elaborated [44]. NBTI is responsible for the defects like Off current leakage and GIDL. GIDL is mainly caused from the Band to band (BTBT) tunneling. For NBTI GIDL increases as NBTI causes Hot Carrier Degradation (HCD). It has been confirmed that by eliminating HCD, GIDL will be still present for Trap Assisting tunneling (TAT). The authors claimed that when V_{GD} is low, the energy bands will not have enough potential to bend. As a result, GIDL will happen and also claimed that t negative bias current Stress Induced Leakage Current (SILC) may be produced. SILC leads to gate leakage current. The authors examined their devices batch on different temperatures and every time GIDL happened. These are the findings from the authors' report [45].

The major updates happened in the 7 nm technology node. This node outdid all its predecessors in terms of RC control electrostatic discharge and made a path for its successors of the 5 nm technology node [46]. A compact model was built and analyzed with one dimension Poisson equation where the device is three-dimensional. The general model efficient extraction, high accuracy, strong scaling capability, and excellent transfer capability. And the performance of ESD improved dramatically. With the change of some crucial parameters like geometric parameters for all advanced technology nodes, it is very difficult to maintain a compact model. The authors offered a novel general compact model based on TCAD simulation. Fine-tuning the gate length and Fin width, the authors presented their BSIM-CMG model. They proved that the trade-off between L_g and W_{fin} of

FinFET greatly strengthen the performance of the power clamp while keeping the area compact and finally proved that their framework is effective for accurate circuit optimization under state-of-the-art technology and made a roadmap for the successors of advanced technology nodes.

Several attempts were made to make new approaches in 7 nm technology node. The authors experimented on this technology node by using Nano Sheet FET (NSFET) instead of FinFET. The band structure was calculated with the help of TCAD and the device was examined for DC characteristics and applied to the Ring Oscillator by taking into account electrostatics, parasitic components, and layout configurations. After examination, it is noticed that NSFET produces 5% more drive current compared to NW FET. The reason for the higher drive current is several nanosheets. The authors claimed that NSFET will compete with other FET architectures and NSFET circuits will be much more robust at heavy loads by stacking channels. By introducing EUV, the designers will get the freedom to tune the geometric parameters and have quantized channels [47].

With rounds of improvement in 7 nm, some authors applied this technology to build 6T SRAM. They achieved 56.7% reduction in leakage current, 7.9% improvement in hold noise margin (HNM), 8.6% improvement in read noise margin (RNM), and 10.8% improvement in write margin (WM) and cost them 19.3% increase in delay under design speculations. Quantization of Lg and Wfin leads to limited improvement of SRAM. A few improvements in the avenue of circuits were being done by the authors [48]. They tuned the gate pitch and Fin pitch to increase the accuracy. They researched with advanced TCAD modeling considering seven crucial parameters and in some cases, they made some trade-offs in parameters to examine the performance. After implying those updates, the authors got high-speed. Cost-effective SRAM cell that is optimized for architecture and peripheral circuits [48].

Sometimes new architecture like Hexagonal nanowire and NanoRing were imposed in 5 nm node for higher current drivabiity and lower parasitic capacitance compared to conventional NW. The multiple vertical stacks with 1-fin-per-device and 2-fin-per-device were evaluated. Parasitic capacitances are more serious in Back-End-Of_Line (BEOL) than Front-End-Of_Line (FEOL) for N5. And it is the major limitation, in terms of power and

performance at the cell level. The author studied comprehensively all the geometric and physical parameters [36]. According to the authors' clime, NR architecture with 3 stacks exhibited the highest performance in terms of drive current and parasitic capacitances.

Speed and power performance are evaluated for N5 Gate All Around FETs and Ultra thin FinFET architecture. Corresponding architectures are also applied to 6T SRAM to examine the area layout. GAAFET is capable of getting better control of SCE, hence better electrostatic control. The severe processing complexity was described in the reports and the author claimed that PFET performed better than NFET in FDSOI architecture [50].

Physics-based Quantum mechanical models were studied for P and NMOS with specific channel thickness and the research is also extended to 1) k.p model with Poisson solver for bandgap variations and confined charge distributions 2) Kubo-greenwood model for low field mobility with considering surface roughness and stress 3) multi sub-band Boltzmann transport equation based on a state-of-the-art phase space approach is employed to evaluate device IV characteristics 4) Vt variation with different channel variation. The authors' research indicated that {110} wafer Ge would be the most viable option [51]. A systematic assessment of the mobility of electrons and holes of NSFET considering the quantum mechanical effect was presented. The device characteristics were analyzed by the Boltzmann Transport equation and also with the semiclassical Drift-Diffusion approach. The authors demanded that their framework express the details of quantum confinement in Ge channel.

The performance of two GAA device configurations: Lateral FET (LFET) and vertical FET (VFET) is benchmarked and analyzed at analyzed using an ARM core processor. The tradeoffs among energy, frequency, leakage, and area are evaluated in the avenue of multi-Vth optimization flow. After tuning with several device parameters, the authors came to the conclusion that LFET had a higher frequency compared with VFET [52].

Multi-stacked NSFET showed a lot of potential as an advanced node as it draws much more driving current and much more controllability. The device was designed through TCAD and then BSIM-CMG library was created. Punch-through and subthreshold swings were studied extensively in this paper [53]. To stop punch-through leakage current,

a Punch-Through Stopper (PTS) was introduced [53]. TCAD calibration carried out two main directions: 1) the value calculated at the lower level of material properties and carrier transport is used as a calibration target, and 2) the measured value of the made device is used as a calibration target. In presence of bottom oxide, each N/PMOS was improved by 17.6% to 6.3% in SS, 59.9% to 31.3% in DIBL. In addition, circuit characteristics were analyzed by a five-stage ring oscillator and parasitic capacitance dropped significantly [53].

Ferroelectric metal FET was realized in 3 nm node. Although it showed some potential, it consumes very large amount of power. Multigate FeFET is being realized. After examining several stacks of nanosheet, the authors concluded that it had some potential to contribute to the advanced node [54].

N2 is the latest technology node in the semiconductor industry. It has replaced many fabrication technologies and introduced new technologies in the avenue of process, fabrication, and circuits. The authors compared four methods to compare for N2 fabrication. After fabrication, the device appeared to be a low-power device of 0.4 V. The analysis of RO behavior including MOL parasitic, all major variability sources suggested that there was a difference between FinFET and NSFET. The authors worked on a device that differs in processes. The 2fin-no-cut design exhibits ~3x better PPA products because of the high PMOS stress level. Single fin device suffers in PPA but consumes the lowest power [55].

The experiment on different channel materials played a vital role in N2 family. The authors came out with Ge channel and the device showed better electrical performance and reliability. Although, Ge has the higher electron and hole mobility it has a problem with interlayer oxide. Gate stack and vertically stacked strain are discussed in detail [56]. A combination of low Ge:P S/D and low C Si:P as a liner in the contact module further improves Ge nFinFET performance.

The scaling potential of Negative Capacitance FinFET and FDSOI are studied for the 2 nm technology node [65]. TCAD simulation justified the NC version of FinFET to a 2 nm node. NC version of FinFET and FDSOI have higher drive currents than their FinFET and FDSOI counterparts. NCFinFET with $HfZrO_2$ showed much higher electric field of 2

MV/cm that indicating a high potential of next-generation device. This device showed higher driving current with better SS and Vt roll-off.

Table 3 Different Technology Nodes

Node nm	Gate Length	Gate Dielectric	Gate Material	Gate Pitch nm	Interconnect Pitch nm	EOT	Fin Width	Fin Height	Fin Pitch
45	45	SiON, HfO_2	TiN	180	160	1.1-1.5			
32	30	HfO_2	TiN	112	160	1.1-1.5			
22	26	HfO_2	TiN	90	90	0.9	8	34	60
14	20	HfO_2	TiN	70	70	0.5-0.8	8	42	42
7	12-18	HfO_2	TiN	64	64	0.8	6	52	30
5	14	HfO_2	TiN	48	28	0.5	5	46	22-25
3	16	HfO_2	TiN	40	32	0.3			
2	12	HfO_2	TiN	30	20	0.9	4	50	44

Table 3 summarizes different technology nodes. As 45nm and 32 nm technology node is based on planar technology, there is no fin. From 22 nm technology, FinFET architecture was initiated. FinFET has a completely different architecture than planar CMOS technology. Even some technology node has several variants. For the case of the 45 nm node, the fast variant had a smaller gate length than the regular and slow variants. The same case happened to 7 nm technology, with different gate lengths for different variants. Nodes like 5 nm, 3 nm, and 2 nm are not matured yet. There is plenty of room for development for those nodes.

My proposed devices' architecture is influenced by 14 nm technology node with junctionless FET.

CHAPTER 3

CROSSTALK PRINCIPLE

In electronics, crosstalk is the occurrence of any noise phenomenon by which a signal transmitted on one circuit or channel creates an undesired effect/noise in another circuit or channel. Crosstalk is generally caused by undesired capacitive, inductive, or conductive coupling from one circuit or channel to another. The term Crosstalk comes from the early analog phone lines where one could hear voices from neighboring lines due to Electromagnetic coupling. Due to "Mutual Capacitance (C_M)" and "Mutual Inductance (L_M)" in the transmission line, the crosstalk phenomena occur.

Crosstalk is based on the principle of Superposition :

1) Multiple signals can exist on the same line same time without affecting each other.
2) A random signal can be coupled onto a line independent of what may already exist in the line

3.1 Crosstalk Terminology

In crosstalk, two main terminologies are aggressor and victim. The line which is carrying the signal is called the aggressor and the line which is receiving noise from the aggressor is addressed as the victim. Fig 7. depicts the crosstalk phenomena. In Fig 7. The victim and the aggressor are in close proximity. When a signal transfers through the aggressor and the victim is idle, the aggressor inducts the same magnitude of electrical signal in the victim line. As a result, crosstalk occurs as a form of noise. From the aggressor line, six electric field lines emit, and four of them are connected with the ground, and the rest two lines are connected with the victim and considered crosstalk noise.

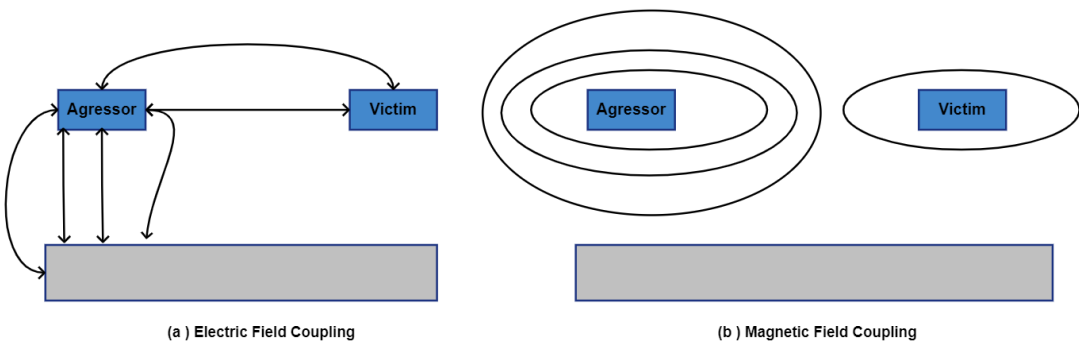


Fig 7. Crosstalk phenomena. (a) Crosstalk happened in electric lines where electric field couplings occur, and some electric lines are coupled with the victim for proximity and considered as crosstalk noise (b) In a magnetic circuit crosstalk occurred for proximity with the victim and aggressor

In Fig 7(b), crosstalk is happening in a magnetic circuit. As the aggressor and the victim are in proximity, magnetic field lines from the aggressor induce the same magnetic flux in the victim line.

3.2 Kinds of Crosstalk

Crosstalk may happen for several reasons. But all kinds of crosstalk can be categorized into two kinds - Signal X-talk and Switching Noise.

(a) Signal X-talk

This kind of crosstalk happens in transmission lines where C_M and L_M produce the same magnitude of noise in a close transmission path. This kind of crosstalk happens in PCB and on chips.

(b) Switching Noise

When the return path is highly inductive and inductive noise is dominant in the circuit, then this kind of crosstalk occurs. This is also known as Ground Bounce / Power Supply Droop", "Simultaneous Switching Noise (SSN)" or "Simultaneous Switching Output (SSO) Noise".

3.3 Crosstalk Location

Crosstalk happens in specific two locations: Near End, and Far End. Near end location can be realized as the location closest to the driving source resistor and the far end can be realized as the location closest to the termination resistor.

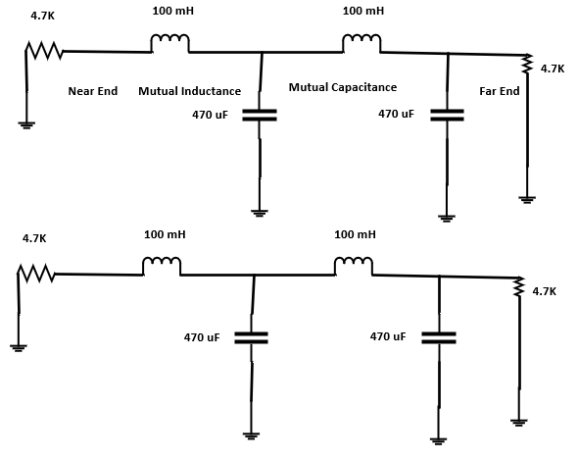


Fig 8. Far end and Near End location of Crosstalk

3.4 Capacitive Crosstalk

As the aggressor current propagates through the line, it will inject the current into the victim line according to

$$I_C = C_M \quad dV/dt \tag{1}$$

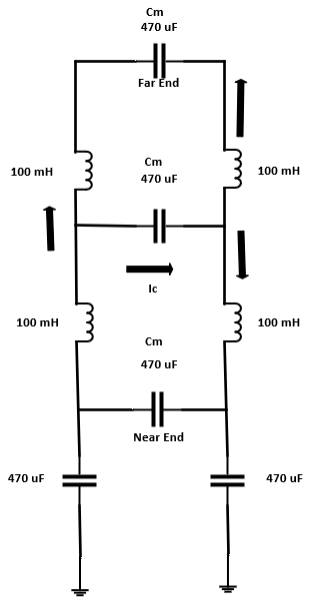


Fig 9. Crosstalk occurrence in the Far end and near end

As the current is injected into the victim line, it will see an equal impedance in the forward and backward directions and will flow in both directions. The current injected is related to the spatial extent of the rise time that can be described using the per unit length value for Mutual capacitance.

$$C_M = C_M' .\Delta x$$

$$C_M = C_M' \ (vel.t_{rise}) \tag{2}$$

Then the total current becomes:

$$I_C = C_M \quad dV/dt$$

$$= C_M' \, (vel.t_{rise}) \, V/t_{rise}$$

$$= C_M'. \, vel. \, V \qquad (3)$$

Half of the current injected into the victim as the incidence voltage step travels down the aggressor travels back to the Near End. In the Near end, only a fixed amount of current is present. The maximum amount of current injected is reduced by a factor of ½ to account for the injected energy dividing in both the forward and reverse directions. It is again spread out with a factor of ½ over the period of 2 T_D.

$$I_C = ½ \, ½ \, C_M'. \, vel. \, V$$

$$= ¼ \, C_M'. \, vel. \, V \qquad (4)$$

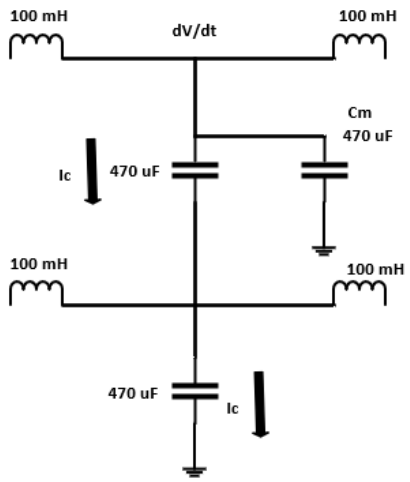


Fig 10. Capacitive crosstalk mechanism. Crosstalk current is flowing through parasitic capacitance

dv/dt occurs in the aggressor node that affects the victim line and is seen across Cl and Cm as shown in Fig 10. For the change of voltage, the Ic current will flow through both of them. Applying KCL it can be realized that the same magnitude of current will flow through both of them.

Applying KCL in the node:

$$Ic = Im$$

$$¼\ C_L'.\ vel.\ V_A = ¼\ C_M'.\ vel.\ V_B$$

$$V_B/V_A = C_M/C_L \qquad (5)$$

This is the total voltage created at the injection before the inductors start to conduct and allow the current to flow through both directions. Now applying Eq.5 in the near field crosstalk location, it becomes:

$$V_{NE}/V_A = ¼\ C_M/C_L \qquad (6)$$

The term ¼ term appears as the current propagates both in the forward and backward directions. For the case of Far end crosstalk

$$I_{CL} = C_L\ .\Delta x\ dV/dt$$

$$= C_L\ .(Vel.\ t_{rise})\ 0.8\ V_B/t_{rise}$$

Applying KCL in the node:

$$Im = Ic$$

$$C_L'.(length)\ 0.8.\ V_A / t_{rise} = C_M'.\ vel.\ t_{rise}\ 0.8.\ V_B/\ t_{rise}$$

$$V_B/V_A = C_M/C_L\ (length/vel.\ t_{rise}) \qquad (7)$$

3.5 Inductive Crosstalk

Current transfers through a wire will cause a magnetic field and a magnetic field can also create current flow. When the aggressor has a magnetic field and the victim is in proximity, then it will create a current in the victim. The direction of the B-field lines in the victim is opposite of the aggressor. The direction of the current creates a negative current in the far end and a positive voltage in the near end.

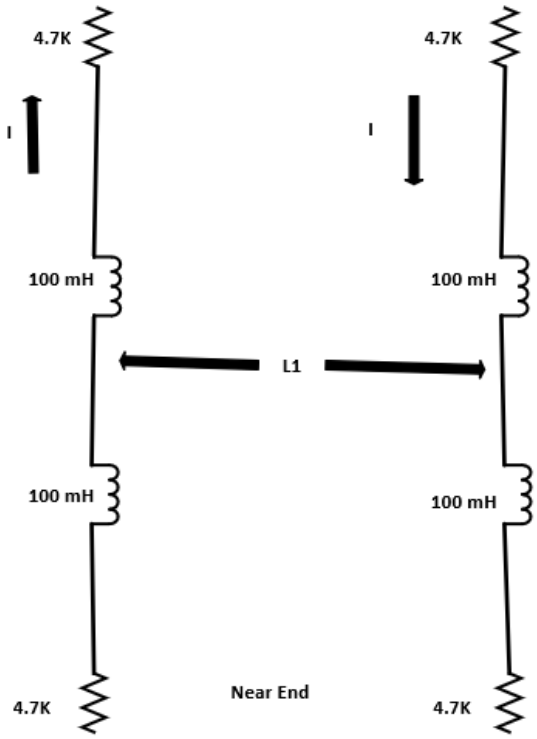


Fig 11. Near End Inductive Crosstalk

The current that flows through the self-inductance of the aggressor line causes a voltage on the victim line as follows:

$$V_M = L_M \ dI_A/dt \tag{8}$$

This voltage appears across the inductance of the victim which causes current to flow:

$$V_L = L_L \ dI_B/dt \tag{9}$$

Since the coupled voltage (V_M) is the same as the Victim line voltage (V_L) which creates the current, we can relate the currents of the Aggressor and Victim.

$$V_M = V_L$$

$$L_M \ dI_A/dt \ = L_L \ dI_B/dt$$

$$L_M \ I_A/t_{rise} \ = L_L \ I_B/ \ t_{rise}$$

$$L_M/L_L = V_B \ /V_A \tag{10}$$

Considering forward/ reverse travel by a factor of ½ and energy being split out over $2.T_D$ eq(10) becomes:

$$V_{NE}/V_A = ¼(L_M/L_L) \tag{11}$$

The difference between the near end and far end is just polarity. The polarity is the opposite.

$$V_{FE}/V_A = -1/2(\text{length}/\text{vel}.t_{rise})(L_M/L_L) \tag{12}$$

3.6 Switching Noise

When the return path is highly inductive and inductive noise dominates, switching noise happens in a switch. It is also known as Ground Bounce/ Power Supply Droop/ Simultaneous Switching Noise (SSN). When the signal travels through connectors or packages, the shape of the return path changes.

The return current that passes through the inductive interconnect causes a voltage to form:

$$V_N = L_{ret} \cdot dI_A/dt \tag{13}$$

This voltage changes the ground potential of the integrated circuit relative to the ground of the system which gives the name Ground Bounce. This becomes a more critical problem when signals in packages and connectors share a common return pin. It is cost-effective to reduce the pin count of packages/connectors by sharing ground pins. Moreover, ground bounce is proportional to the number of signals and eq. 12 becomes:

$$V_N = (L_{ret} \cdot dI_A/dt).(\#\ \text{of signals}) \tag{14}$$

There is a mutual inductance that couples between the signal inductance and the return path inductance. In this case, the inductor acts as a voltage source in the return path, which creates a voltage in the opposite polarity as the noise caused by the return current. This causes the result of decreasing the total inductive ground bounce noise and can be a good thing. But this is a secondary effect compared to the noise generated when multiple signals share a common return path.

3.7 Effects of Crosstalk

The effect of crosstalk is severe. In RF circuit, it creates an unnecessary magnetic field which hampers the circuit and causes excess power consumption. In RF circuit excess magnetic field causes noise in the transmission and receiver. In the case of capacitive crosstalk, any Rf circuit will experience noise on the receiving end of the input side. Crosstalk happens between two parallel transmission lines. When capacitive crosstalk happens the victim line experience a bump in the transmission line. In the case of PCB, crosstalk will create an excess magnetic field which hinders the regular signal flow and creates noise in the transmission line. In the case of semiconductor circuits, crosstalk creates a bump in the transmission line and the null carrying victim line will then carry logic1 as a signal.

3.8 Crosstalk Mitigation Techniques

There are several ways to mitigate this crosstalk noise. They are:

1. Minimum width among Transmission lines

   When defining the electrical circuit, it is possible to set some rules, such as the minimum distance between two traces and the minimum distance between each trace and the components present on the circuit. Setting different values for transmission line distance is also a solution. The width of the transmission line must be defined also. The general rule to take into due consideration is that the coupling, both inductive and capacitive, decreases with the increasing distance that separates the traces.

2. Keep traces on adjacent layers perpendicular

PCB layers should be configured in a way that the signals' directions are perpendicular to each other, avoiding that their traces are parallel. It is also used to say that if on one layer is in one direction and another layer should be in the opposite direction. This simple precaution allows for minimizing the effects of broadside coupling.

3. Use ground planes

Between two adjacent signal layers, it is safe to insert a ground plane (or, alternatively, a power plane). Doing so further reduces the likelihood of broadside couplings occurring. This solution has the two advantages of increasing the distance between the layers and providing a better return path to the ground required for the signal layers.

4. Exploit ground return path

Another technique for the reduction of crosstalk consists precisely in exploiting the parallelism existing between the traces, coupling the ground return path with the high-frequency signal. Since the ground return path has the same amplitude but opposite direction concerning the signal, the effects are eliminated with a consequent reduction in crosstalk.

5. Use differential signals

Another way to ensure signal integrity is by minimizing the effects produced by crosstalk, is to use differential signals, that is, two signal lines with the same amplitude but opposite polarity that form a single high-speed signal. Since in the receiver end, the signal is obtained as the difference between the voltages of the two signal lines, and since the electromagnetic noise equally affects both lines, the signal maintains a high integrity even in the presence of significant external noise. It is advised is to keep the greatest possible distance between the differential signal pairs and the other PCB traces. A rule of thumb is to choose a distance that is at least three times the width of the track.

6. Reduce the width of parallel traces

Keeping the width as short as possible will reduce the extent of coupling.

7. Isolate high-frequency signals from other traces

High-frequency signals, such as clocks, must travel as far as possible. Even in this case the rule of thumb can be applied, choosing a minimum distance equal to three times the trace width.

8. Isolate asynchronous signals

Asynchronous signals, such as reset or interrupts lines, shall be used with traces as far away as possible from high-frequency signals. These are the signals used only in certain phases of the circuit operation and not continuously.

For my research, capacitive crosstalk as well as near end crosstalk is implemented both in the avenue of circuits and devices. Crosstalk circuits are described in Chapter-4 and devices are discussed in Chapter-5 and 6.

CHAPTER 4

EXPERIMENT OF CROSSTALK

Crosstalk is an unwanted noise that needs to be eliminated. The source of crosstalk noise is the proximity of two signal-carrying wires. The existence of this noise causes severe problems in circuit systems and in PCB. In the RF circuits, crosstalk produces excessive noises both at the source end and the receiving end. The crosstalk noise is so dominant that it also affects modern days' highly noise-resistant MIMO networks [103]. There is an ample amount of research on crosstalk mitigation [103-118]. Moreover, crosstalk noise is not only dominant in circuits but also in semiconductor devices ranging from Quantum Cascaded LASER (QCL) and also in Quantum devices and circuits. Extensive work has been done to mitigate this crosstalk noise in all departments of electrical engineering. The most dominant noise of crosstalk is an aggressor-created glitch. All the research is related to the elimination of crosstalk noise. In 2016 we pioneered a new paradigm of circuits where crosstalk was used for logic generation [118]. We utilize the crosstalk capacitance by varying capacitance value with altering aggressor-victim distance and came up with several Boolean logic.

Our logic gathers three states: Input State (IS) when Inputs are fed through aggressor nets (Ag1 and Ag2); Logic State (LS) when logic is evaluated; and Discharge State (DS) when floating nodes in the circuit are periodically discharged to ground hence gaining control over the floating nodes. We have accompanished deterministic outputs in all CT (CrossTalk) circuit implementations which provide further improvement and development opportunities

At first, we experimented with AND gate. In between two aggressors, one victim wire is placed at nanometers distance. By the definition of crosstalk, coupling capacitance will develop between the victim and aggressor1 and also with aggressor2. The amount of capacitance will be in the range of femtofarad and if the capacitance is scaled properly then it will deliver a specific amount of discharge which will lead to the output voltage. This

scenario is depicted in Fig 12(b). when input signals a and b are logic 0 or either one of them is Logic 0 the circuit's output cannot exceed the threshold voltage. As a result, the output voltage is below the threshold and regarded as logic 0 output. The output is logic 1 only for the case of all inputs are logic 1. When both inputs are logic 1 coupling capacitance will charge up and discharge and the voltage at the output will be equal to the discharged charge from the coupling capacitor (Cc) and the charge will appear as the voltage at the output node. Hence, the circuit exhibits the virtue of an AND logic circuit.

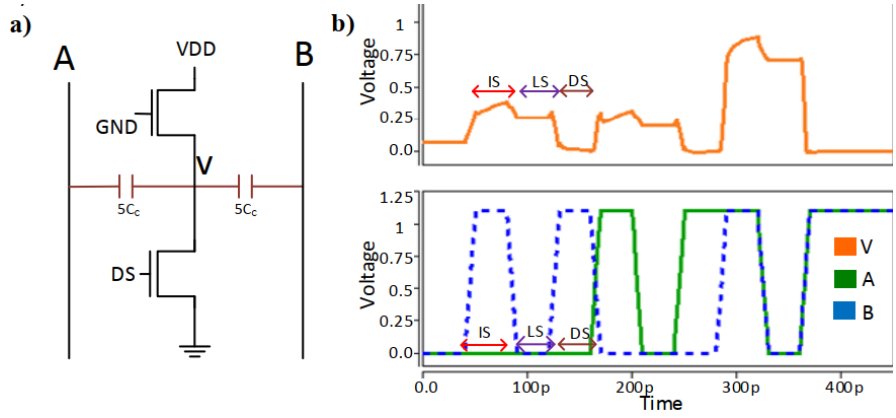


Fig 12. (a) Crosstalk AND circuit. Cc is the coupling capacitance. To get proper logic output threshold is fixed to 5Cc. (b) Wave output of simulation where V(a) and V(b) are input signals, V(dis)is the discharge signal and V(vi) is the output signal. When V(a) and V(b) are both one V(vi) is logic 1 and for other input combinations it is logic 0 output.

AND circuit with conventional CMOS technology is depicted in Fig 13(b). For A = 0 and B = 0 pmos on top both will be ON and pass logic 1 to the junction. For nmos, both will be OFF. As a result, logic 1 will pass from the junction to the inverter and the final output will be zero. For A= 1 and B = 1, pmos with signal A will be OFF and the other will be ON which will cancel each other and in nmos part A will be ON and B will be OFF. As a result, logic 0 will pass from the junction to the inverter and the final output will be logic 0. For A=0 and B=1 same output will be produced. When A and B both are one then both pmos will be OFF and logic 0 will pass to the junction and in nmos part, all will be ON and logic 1 will pass to the ground. Logic 0 which is in the junction will pass from the junction to the inverter and the final output will be logic 1. Compared to conventional CMOS transistors, crosstalk architecture has fewer transistors. AND gate CMOS transistor needs

eight transistors whereas crosstalk architecture AND circuit will take only two transistors. Hence, the device will consume less space and the layout footprint will be much smaller than the regular AND gate with CMOS technology. The same goes for layout and PCB circuit board design. Fig 13 (a, b) depicts the transistor count for both technologies.

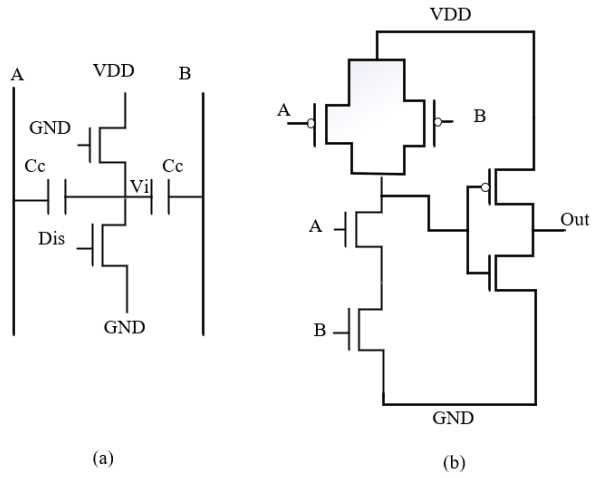


Fig 13. (a) AND gate with crosstalk architecture with two transistors (b) AND gate with Conventional CMOS architecture with eight transistors

OR logic circuit works in a different way. The circuit architecture is the same as AND crosstalk circuit, the only difference is the coupling capacitance. For OR circuit coupling capacitance is five times lower than AND's one. When input A and input B are logic 0, coupling capacitance will get less charge and during discharge time current will be discharged to the output node. But the charge is below the threshold which will be considered as output Logic 0. When either of the input is logic 1, the coupling capacitor will at first charge and the discharged charge will appear at the output node and the charge value is above the threshold value which will be considered as logic 1 output (Fig 14(a, b)). The same phenomenon happens when both the inputs are logic 1 the discharge is above the threshold and logic 1 appears in the output node. In Fig 14(b) simulation result depicts the whole event. When the discharge transistor is Off and signal pulse a is logic 1 and pulse b is logic 0, output vi is logic 1. Both a and b are logic 0 return logic 0 output regarding discharge transistor OFF. When discharge transistor is ON output will be disregarded.

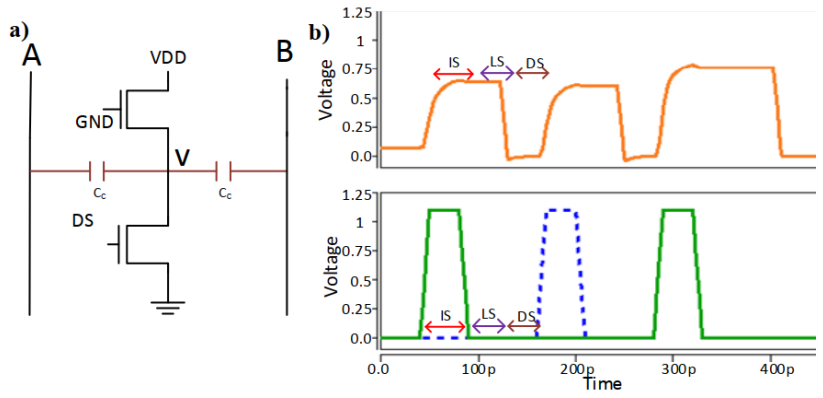


Fig 14. (a) Crosstalk OR circuit. (b) Wave output of simulation where V(a) and V(b) are input signals, V(dis)is the discharge signal and V(vi) is the output signal. When V(a) and V(b) are both one V(vi) is logic 1 and for other input combination it is logic 0 output.

The conventional OR circuit is shown in Fig 15(b). For A and B both are logic 0, pmos will be ON and logic 1 will pass to the junction and in the nmos part both will be logic 0. Logic 0 will pass from the junction to the inverter and the final output will be logic 0. When A =1 and B = 0, pmos with A signal will be OFF and the other will be ON. As a result, logic 0 will pass to the ground. In the nmos part, A will be ON and B will be OFF. Hence, logic 0 will pass to the inverter and the final output will be logic 1. When both are logic 1, both pmos will be OFF and logic 0 will be passed to the junction and in the nmos part all will be ON and logic 1 will be passed to the ground. Logic 0 will be passed to the inverter and the final output will be logic 1. The conventional CMOS OR circuit will take eight transistors to achieve the logic output but the crosstalk architecture will take only two transistors (Fig 15(a,b)). In the case of PCB and layout, the same issue is applicable. CMOS technology OR gate will take six times more area than the crosstalk logic OR gate in layout design. For PCB, the same phenomenon will happen.

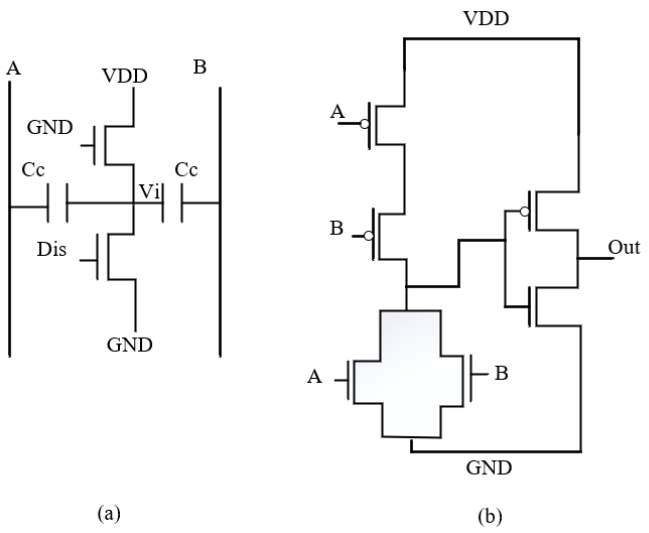


Fig 15. (a) OR gate with crosstalk architecture with two transistors (b) OR gate with Conventional CMOS architecture with eight transistors

The carry circuit, AB+BC+CA experiments with crosstalk architecture. The original AND circuit are modified to perform the carry operation. Instead of two fan-ins, the circuit is modified with three fan-ins A, B, and C. And circuit got an addition of a fan-in. In that case, coupling capacitance occurred in two places of the circuit. In addition to that coupling, capacitance is set up to half of the value of normal coupling capacitance. When all the inputs are logic 0, the circuit will deliver an output of logic 0. When either of the two inputs is logic 1, the circuit will deliver an output of logic 1. When input A and B are logic 1 (Fig 16 (a, b)) coupling capacitance will go up and the capacitor is charged after passing the RC time constant the capacitor will discharge the

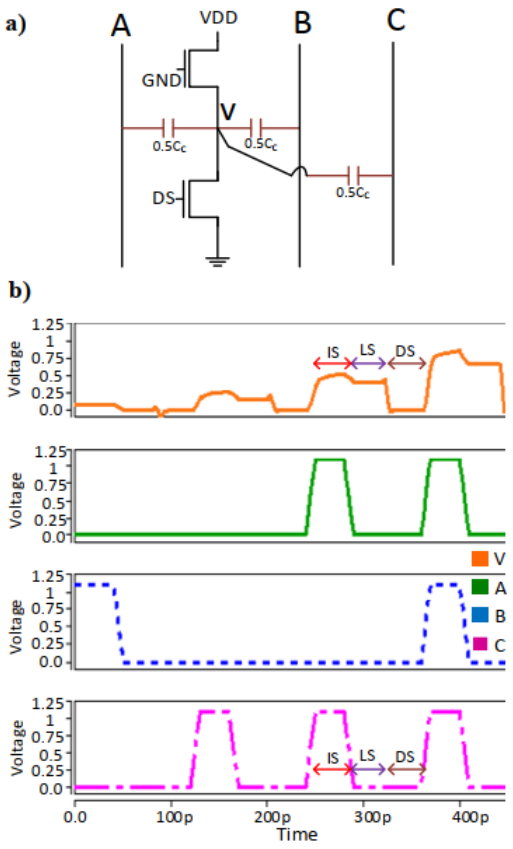


Fig 16. (a) Crosstalk Carry Circuit (b) Simulation of the carry circuit

Charge and this charge will pass to the next coupling capacitance and after RC time constant and in the output node this charge will appear as voltage as a logic 1. The same goes for the input combination of BC and AC. For the case of all inputs being logic 1, the output will be logic 1. In Fig 16(b) input A and C is high as a result output vi is high. The carry circuit is part of Full adder to measure the carry for the full adder. The carry circuit computes the carry output for the full adder. A full adder circuit has two inputs and one carry input. When carry input is one, carry will be added with the other two inputs in the ripple carry adder and this carry is propagated and finally added in the last segment for final computation. This crosstalk carry circuit can be used in a ripple carry adder, where A

and B are the regular input and C, is the carry input. When C is logic 1 and A and B are also logic 1, the internal carry of logic 1 will be generated and will be propagated in the next segment. When A and B are zero and C (carry-in) is logic 1, this logic one will propagate to the next segment and be added with the result of the addition in the next segment. When all are zero, this information will still pass to the next segment in the form of coupling capacitance and will be added to the next segment computation. In Fig 16(a) crosstalk carry circuit is depicted where A, B, and C are input signals and Vi is the output node. When A and B are high, the coupling capacitor will store the charge above the threshold level, and during the discharge, the charge will appear at Vi node as output voltage. The same phenomena will be observed in the case of the pair B-C and C-A. If A-B and B-C are high, the output will be high. When all three inputs are high, the output will be high also. When only A is high and the other two inputs are low the coupling capacitor on the side of A will store charge above the threshold but the coupling capacitor on B side and C side will store charge below the threshold level. Hence during the discharge time, charges from A and B will pass to Vi node and it will be below the threshold level, the same case from the side of input C which has a below threshold charge. The same phenomenon will happen when only B or C is high. The output node will deliver logic 0 output. When only one input is high, the output will be zero. All the charges will be aggregated at node Vi and this charge will be regarded as low voltage (logic 0 output). This is the virtue of the carry circuit for any architecture whether it is crosstalk or CMOS architecture. When one input is high and others are low it will deliver logic low output. When all inputs are low, the coupling capacitor will charge below the threshold level and discharge the low-level charge to the output node which will be addressed as logic 0 output. All the output will be addressed when the discharge transistor is Off or all the charges will lead to the ground.

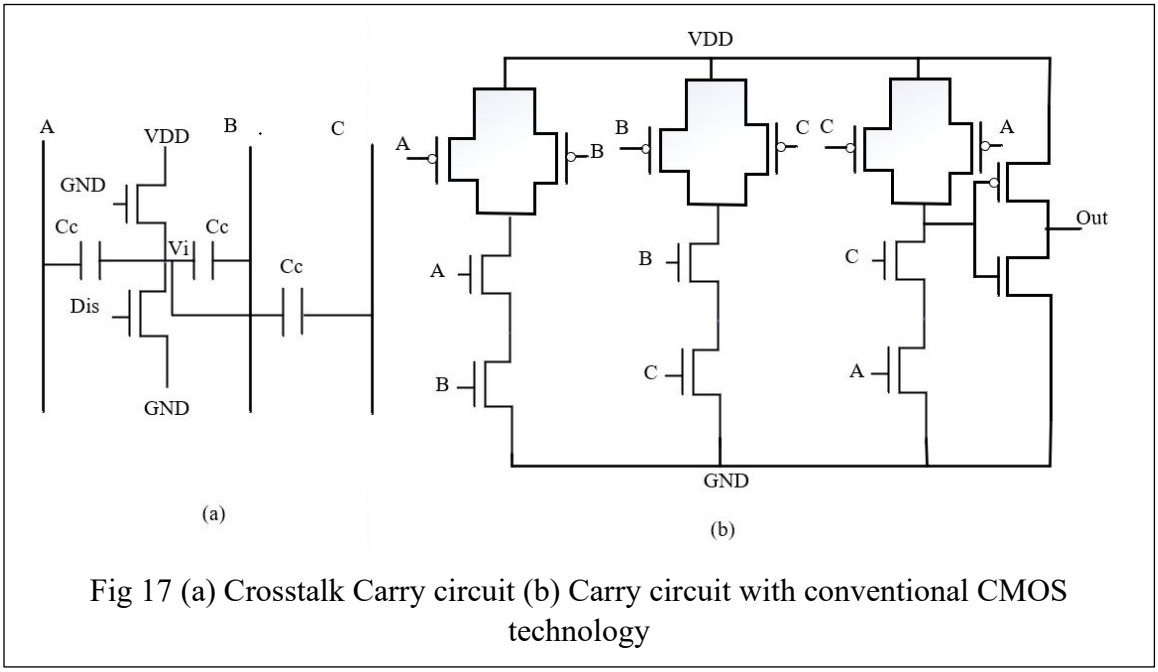


Fig 17 (a) Crosstalk Carry circuit (b) Carry circuit with conventional CMOS technology

Fig 17(a, b) depicts the carry circuit with crosstalk and CMOS architecture respectively. In CMOS architecture, the carry circuit consists of AND, OR circuits. In each branch AND, OR circuitry is available and performs the Boolean function. When each input pair is high the circuit will produce high output. When only one input is high and the others are low it will deliver logic low and for all low inputs, it will deliver logic low. The last part is the inverter which reciprocates and boosts the signal. In the case of transistor count, from Fig 17(a) it is noticed that the crosstalk logic circuit performs with only two transistors in comparison to CMOS technology, which takes fourteen transistors. For the case of device layout, crosstalk architecture will consume eight times less area than conventional CMOS technology. PCB layout will face the same event. The crosstalk architecture will consume less area for PCB than the conventional CMOS architecture. Because of fewer transistors, the crosstalk-carry circuit will consume less power with lesser propagation delay in comparison to conventional CMOS circuits.

XOR circuit has a different architecture with different logic. When both inputs are the same XOR circuit will deliver logic low at the output node. When both inputs are different, like one is low and another is high, the circuit will produce logic high at the output. In Fig 18(a) when both A and B signals are high, the coupling capacitors will store charge over the threshold and at discharge pass to the bottom coupling capacitors, and the bottom pair of capacitors at discharge will pass to the bottom transistor and finally to the ground. The exact same event will happen when both signals are logic-low. Either of them is logic-low, then after discharge from top capacitors, charges will be aggregated at node Vi and exceed the threshold limit and it will be considered as logic 1 output at node Vi. Fig 18(b) is the simulation result of the XOR-crosstalk circuit. a, and b are the inputs and dis is the discharge signal and vi is the output signal. When dis signal is zero, it is noticed that a, and b are zero and vi is also zero which gives evidence of XOR operation. When both are high and dis signal is high this signal is disregarded. The exact phenomenon for either of the signal is high and dis signal is high, the output is disregarded.

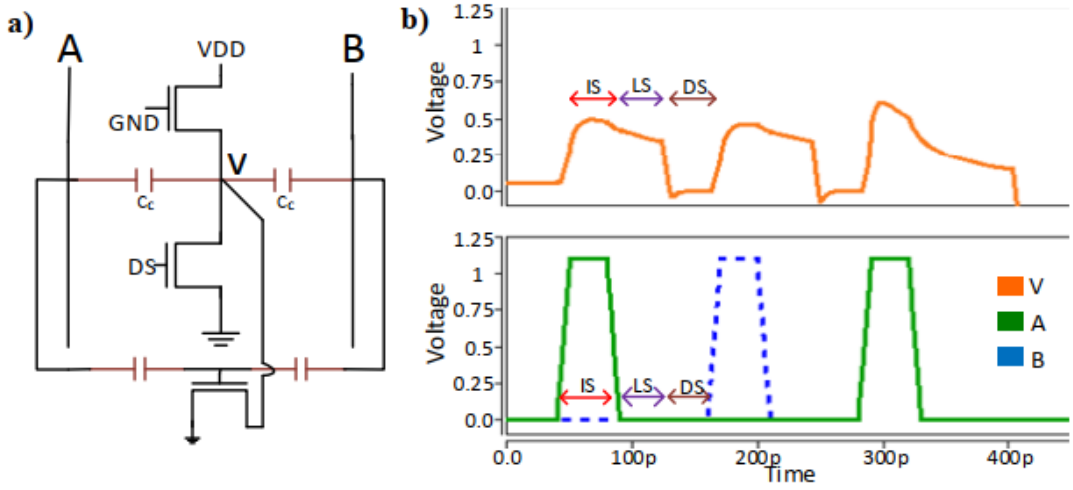


Fig 18 (a) Crosstalk XOR circuit (b) Simulation of the XOR circuit

In Fig 19(a, b) a comparison between the crosstalk XOR circuit and CMOS XOR circuit is exhibited. In Fig 19(b) CMOS XOR circuit is demonstrated. From the top of the circuit when B is high B' will cancel it and when A is high A' will cancel it out. For A = 1 and B = 1, B' pmos will switch ON and A pmos will switch OFF. As a result, from the left side, no signal will pass and that will be considered signal 0. On the right side, B pmos will be OFF and A' will be ON and B will be OFF. So logic 1 will pass to the junction but A pmos is passing zero and A' is passing 1 so both of them will cancel each other and the output junction will contain logic 0. At the bottom part

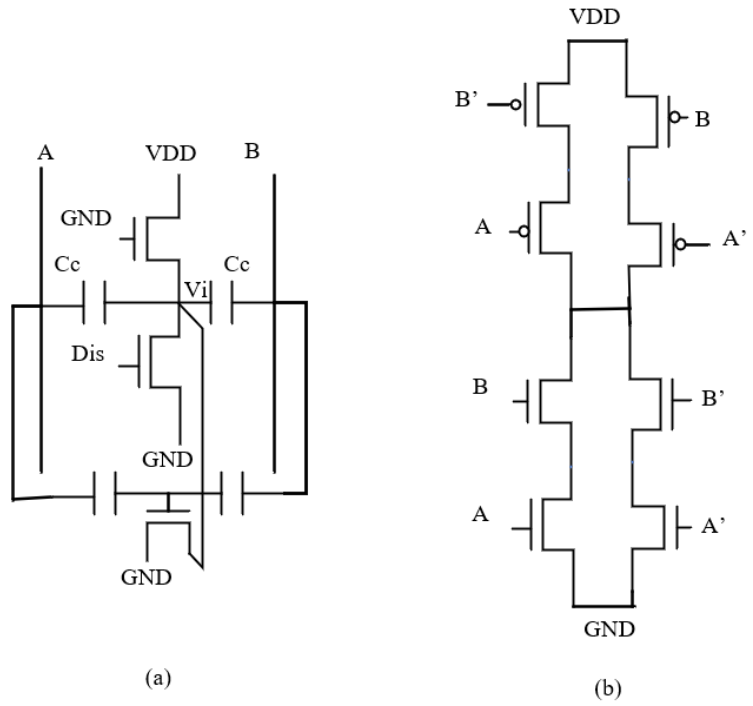


Fig 19 (a) Crosstalk XOR circuit (b) CMOS technology XOR circuit

A, B will be ON and B' and A' will be OFF and logic 1 will pass to the ground. As a result, the output will be logic 0. For A = 1 and B = 0, B' pmos will be ON A pmos will be OFF; on the right side, B pmos will be ON and A' pmos will be ON. As a result, a strong logic

1 signal will pass to the junction. On the bottom part of the circuit, B nmos will be OFF and A nmos will be ON and logic 1 will be passed to the ground. At the right side of the bottom, A' and B' nmos are OFF. As a result, the junction will retain logic 1 and it will appear at the output node.

At the avenue of transistor count, the crosstalk-XOR circuit takes only two transistors whereas the CMOS counterpart takes eight transistors for the Boolean operation. Hence, crosstalk architecture consumes four times less area than conventional CMOS technology. The layout will take lesser area and as well as PCB circuit area. The lesser transistor will consume lesser power and the same goes for the delay. Lesser transistors, lesser connection; hence lesser delay.

In this chapter, crosstalk circuits are compared with CMOS circuits only. CMOS circuit is a static circuit. There is more circuit architecture apart from static logic. Dynamic logic and domino logic are a few to mention. These circuits lag in signal integrity and have problems producing strong zero and strong one. The circuits are prone to noise and not robust. Domino logic circuits and dynamic logic circuits will take more area than crosstalk logic. The exact same issue for power consumption and delay. Domino logic and dynamic logic circuits will consume more power and produce more delay. In terms of reliability, signal integrity CMOS static logic is much better than these two architectures. For this reason, all crosstalk circuits are compared to their CMOS counterpart.

Crosstalk circuits have another quality of polymorphism. Polymorphic circuits have the virtue of changing the circuit behavior according to inputs or frequency. Changing the route of the circuit can alter its behavior of the circuit [119-135]. Crosstalk circuit routing is suitable to apply polymorphism. There are several methodologies for altering circuits. Some are decomposition, bi-decomposition, and poly-bi-decomposition. Each method has its own pros and cons. Poly-bi-decomposition method has a noise margin problem but it can utilize the full potential of built-in-multifunctional properties compared to Bi-decomposition techniques. Polymorphism in crosstalk can be approached both in the circuit domain and device physic domain. In the next chapter, polymorphism in the proposed device is discussed in detail.

Applying stick diagrams of the logic expression in 2D CMOS and CT logic style (Fig 20) , it can be noticed that CT logic needs 2 transistors while CMOS needs 12 transistors, and CT logic consumes less footprint of .044 µm2 while CMOS consumes .13 µm2 foot print. The simple CT and summation based implementation of the above logic expression shows the potential of CT logic with high fan in logic gates [118].

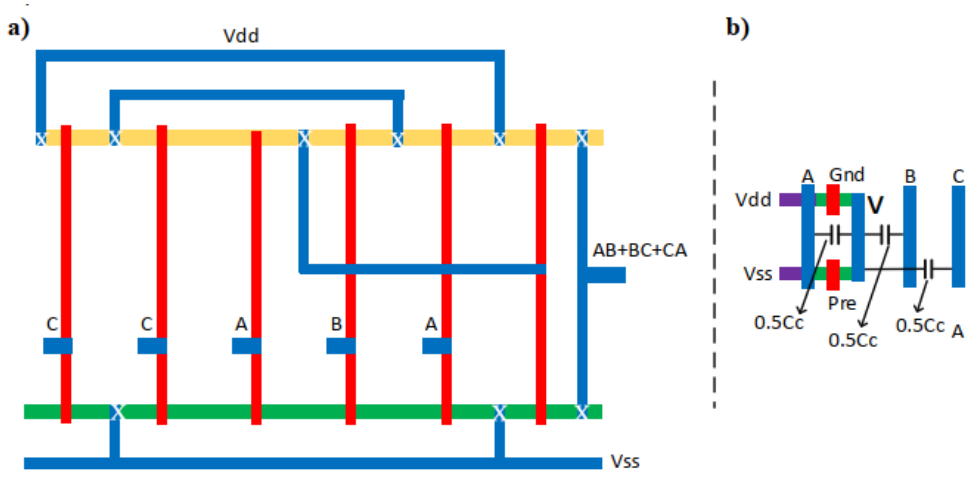


Fig 20. Stick diagrams of logic expression AB+BC+CA, a)2D CMOS b) Crosstalk logic [118]

The diagram in Fig. 21 illustrates the arrangement of a Full Adder. When it comes to implementing the full adder circuit using CMOS technology, a total of 40 transistors are needed, arranged in a cascaded topology (with 12 transistors for each XOR gate and 12 for the carry logic). However, utilizing Crosstalk implementation only requires 13 transistors, resulting in significantly reduced interconnection requirements. Fig. 21 clearly demonstrates that Crosstalk circuits occupy less active device area compared to CMOS.

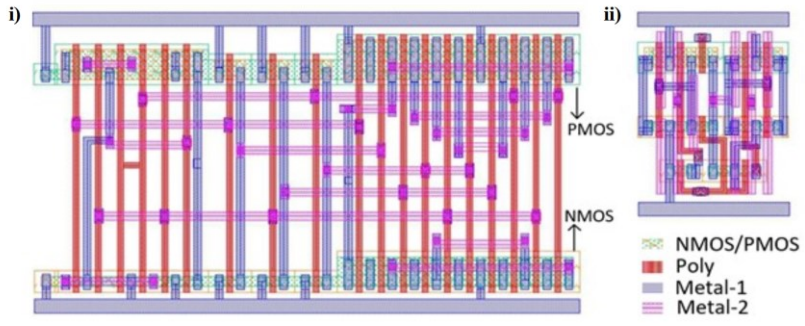


Fig 21. Layouts of Full Adder Circuit (Sum and Carry): i) CMOS Layout ii) Crosstalk Layout

CHAPTER 5

DEVICE ARCHITECTURE

The global socioeconomic progress owes much to the widespread adoption of Integrated Circuits (ICs). As Moore's law experiences a slowdown, finding solutions to sustain this progress becomes crucial. One of the most promising alternative paths, explored in existing literature, involves embedding logic within a single device through the manipulation of device parameters [140–142]. This approach seeks to collapse the ensemble of multiple devices for a Boolean logic unit into the compact footprint of a single device. However, current approaches are primarily limited to embedding only basic cells like NAND/NOR, resulting in only modest density benefits [143,144]. Some approaches incorporate exotic devices such as Complimentary Resistive Switch [140] and Bipolar Memristors [141], but these require costly non-conventional manufacturing processes [145].

I propose the implementation of Boolean complex logic using a standalone device, similar to the multi-gate junctionless FET, by leveraging a novel computing technique known as Crosstalk Computing [147]. In this approach, metallic nano-lines function as aggressors and are arranged compactly. When signal transitions occur in these lines, the cumulative crosstalk interference is induced through virtual coupling capacitance in another metal nano-line, termed the victim. The transitioning signals serve as inputs, and the resulting induced charge becomes the output, determining the computed logic. Our proposed multi-gate Junctionless device mirrors this aggressor-victim scenario, with independent gates acting as aggressors and the silicon fin of the device as the victim. By strategically placing the independent gates within the device, we can control the formation of accumulation or inversion in the device fin to achieve the desired saturation current at the output. The device's geometry, gate placement, and manipulation of device parameters are critical factors in accomplishing the targeted logic function.

5.1 Device Physics of 2D Architecture

My device modeling approach incorporates the innovative Crosstalk computing concept. In my simulations, we initially replicate the actual process flow to characterize the device using 3-D TCAD device simulations. The specific simulation parameters, such as implantation dosage and anneal temperature, are listed in Table 4 for reference. Figure 22.i presents the simulated device in our process, showcasing independent gates (Gate-1 and Gate-2) in a double-gated configuration. The selection of gate and contact materials in the figure is based on meeting the work-function requirements necessary for creating an aggressor-victim scenario. Additionally, the coupling capacitance, a vital aspect of Crosstalk technology [4], is thoroughly investigated. To achieve the desired interference for implementing the logic, we explore the material work function and gate oxide thickness of the device. The process simulation commences with wafer preparation, specifically choosing the (100) plane and creating a Silicon-On-Insulator (SOI) wafer with the (100) Miller Plane. We utilize advanced calibration techniques to achieve a fine mesh resolution of 1 nm. For the gate material, we have selected Titanium Nitride (TiN) with a work function of 4.7 eV, and Hafnium Oxide (HfO2) is chosen as the gate oxide.

Table 4 2D device Architecture

Parameters	Value
Gate Length(nm)	25
Fin Diameter (nm)	5
Gate Oxide Thickness (nm)	1
S / D Length (nm)	50
S/D Doping (cm^{-3})	5e18
Channel Doping (cm^{-3})	1e16
Channel Stop Doping (cm^{-3})	1e14

For the high-k/metal gate formation, we opt for a 1nm thick gate made of Hafnium Oxide (HfO_2). This choice allows us to achieve the desired high-k/metal gate structure. Following

this, Phosphorus implantation is conducted, resulting in a doping concentration of 5e18cm-3. For further details on the device's geometric parameters, please refer to Table 4.

To characterize the device's behavior, we utilize the process-simulated structure in TCAD device simulation. The simulation incorporates doping-dependent mobility to determine the ON current, while also considering high field saturation for velocity saturation. By employing channel doping and various other device parameters, we compare the drive current at a drain bias of 0.7V.

For the self-consistent solution of the Poisson and electron continuity equation, a fully coupled or 'Newton' method is employed in the device simulation. Figure 2.ii depicts the I-V characteristics of the device obtained from this simulation, showcasing the device's performance metrics. The device exhibits an Ion of 500e-6 A/µm, Ioff of 3.76e-13A/µm, Subthreshold Swing (SS) of 62mV/dec, and Drain Induced Barrier Lowering (DIBL) of 25mV/V. The threshold voltage of the device is 0.59V, with the gate metal being TiN, having a work function of 4.6 eV, and positioned in the mid-bandgap. Both the source and drain doping are set at $5e18cm^{-3}$.

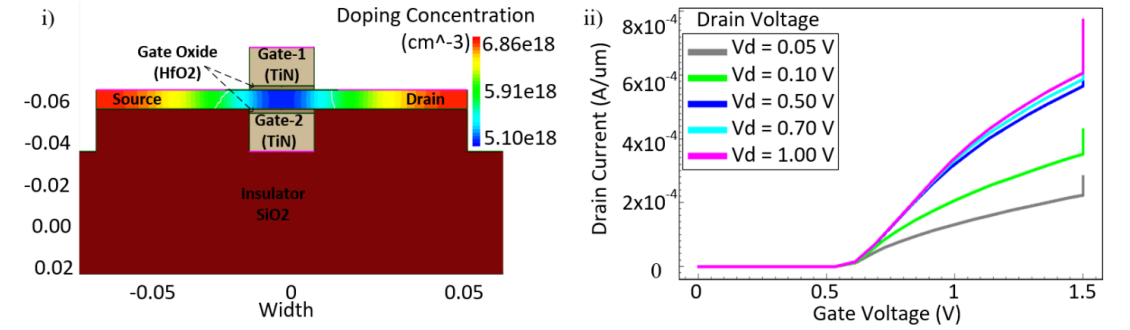


Fig 22. Device structure and characteristics of a Planar Double Gate FET. i) Process emulated device structure; the device has gate length of 25 nm, channel thickness of 5 nm, and HfO2 as gate oxide with thickness of 1 nm between both gates. n+ concentration is 6e18 cm^{-3}, ii) I-V characteristics ofthe Planar DG FET. The device has threshold voltage of 0.53 V, Ioff = 3.76e-13 A/µm and Ion = 500e-6 A/µm.

5.2 Device Physics Of 3D Architecture

In our implementation, we have successfully incorporated two fundamental logic gates (AND and OR) and two more complex Boolean functions (AB+BC+CA and B+AC). The results obtained from our study demonstrate and confirm the functionality of these logic gates. Additionally, our comparative analysis reveals noteworthy findings. For the primitive gates, we observed a remarkable 6x density gain and an average power reduction of 8x. As for the complex functions, the average density benefit achieved is 13x, along with an average power reduction of 10x. Moreover, the delay timings are in good agreement with their CMOS counterparts.

We adopted a bottom-up modeling approach, with a multi-gate Junctionless FET serving as the core functional unit. The logic operation in this single proposed device relies on controlling independent gates, utilizing inversion/depletion mode, and customizing device parameters. Initially, the device is implemented in the Sentaurus TCAD process and then characterized using TCAD device simulation within our bottom-up modeling approach.

To achieve Boolean functionality, we consider the Crosstalk Computing concept, known for its high-density benefits [8]. In this approach, the independent gates of the device act as aggressors, while the fin plays the role of a virtual victim. Based on the voltage level applied to the gate, the device will operate in either the inversion or depletion region. When the voltage remains below the threshold value, the device stays in the depletion region, resulting in a partial ON state and producing a logic 0 as output. On the other hand, when the voltage surpasses the threshold limit, the device enters the inversion region, leading to an entirely ON state and producing a logic 1 as output. Following this principle, we implement both elementary and complex logic in the device.

In this study, inputs A, B, and C are mapped to gate-1, gate-2, and gate-3, respectively. The choice of gate material and gate dielectric is based on extensive references [11–24]. We opt for TiN as the gate material due to its specific work function of 4.4 eV. Considering

granularity, the mid-bandgap metal TiN has its work function varied from 4.4 to 4.6 eV, enabling tuning of the work function and facilitating proper potential barriers for gate control. HfO2 is selected as the gate dielectric due to its high dielectric constant, essential for tuning the gate potential and facilitating gate control.

To implement the device while addressing these considerations, we utilize Sprocess and Sdevice platforms.

5.2 Elementary Logic Device Architecture

The elementary logic gates (OR & AND) are implemented using two independent gates based on the Junctionless FET. Input voltages are applied to the independent gates by voltage sweeping, specifically at Gate-1 (Input A) and Gate-2 (Input B) as shown in Figures 23(i & ii). During the subthreshold voltage application, charge depletion occurs in the silicon fin. As a certain part of the Silicon fin (Figure 23(i)(a)) becomes neutral, signifying the end of depletion, the threshold voltage is reached, and bulk current starts to flow through the neutral silicon [6].As the gate voltage increases and depletion decreases, the neutral channel's diameter also expands. At this point, the device enters the inversion state (Figures 22(i)(b-d)). Upon reaching the flat band voltage, the entire channel region becomes neutral (Figure 22(i)(d)). Further voltage increment leads to full inversion. In this scenario, the two gates act as aggressors, while the silicon fin acts as the victim, forming a setup that resembles Crosstalk configuration.

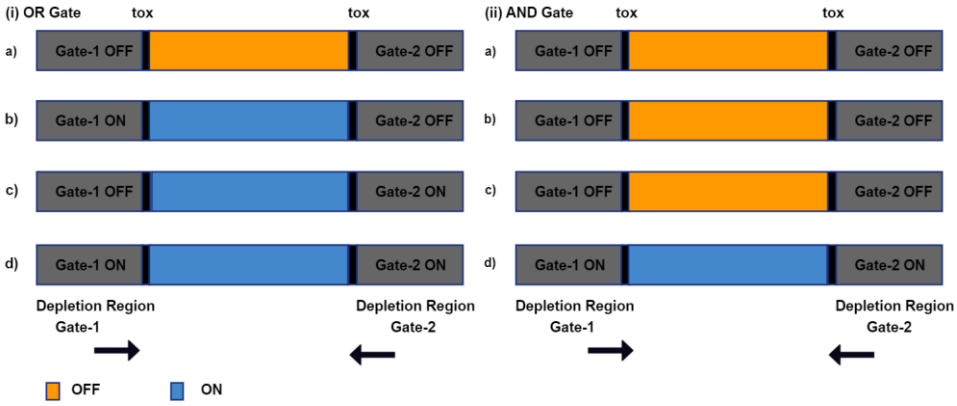


Fig 23. Switching Mechanism of elementary gates for several switching conditions i) OR gate ii) AND gate. In both cases, depletion, partial inversion, and inversion occur for switching conditions.

In a two-input OR logic scenario, when both gates are in the 'OFF' state, the depletion regions beneath them overlap (Fig. 23(i)(a)). As a result, no current flows, and the output remains logic 0. However, when one gate is 'ON' and the other is 'OFF,' the depletion region vanishes, leading to partial inversion and the creation of a conduction path (channel) between the source and drain (Figs. 20(i)(b-c)). The device enters the 'ON' state, producing a logic 1 output. When both gates are 'ON,' and the drain voltage is constant, the depletion region completely disappears, causing full inversion and widening the channel path to achieve a fully 'ON' state, resulting in a logic 1 output (Fig. 22(i)(d)).

Similarly, in the AND operation, when both gates are in the 'OFF' state, the depletion regions overlap, as shown in Fig. 20(ii)(a). If one gate is 'ON,' the depletion region diminishes from that particular 'ON' gate area due to voltage increments and leads to inversion. However, the depletion region remains at the 'OFF' state, keeping the transistor in the 'OFF' state (Fig. 22(ii)(b-c)). Only when a specific voltage above the threshold voltage is applied to both gates, all depletion regions vanish, and the transistor enters the 'ON' state (Fig. 23(ii)(d)).

Based on these principles, we propose a double-gate Junctionless device as depicted in Fig. 23, featuring 2-input AND and OR gates. Figures 23(a) and (b) illustrate the OR device and its log plot of I-V characteristics, respectively. According to Table 5, the device has a gate length of 14 nm, TiN as the gate material, a silicon fin width of 20 nm, and a height of 20 nm. The device exhibits an ON current of 10 μA, an OFF current of 0.32 pA, and a threshold voltage of 0.3 V (Fig. 23(b)).

The main differences between the AND and OR devices, as seen in Figs. 23(a) and (c), lie in the orientation of the two independent gates. For OR logic implementation, the gate lengths are placed across each other to have equal control of the channel. Such arrangements allow any individual gate or both gates together to create a partial inversion region within the channel (logic 1 at the output) whenever an input voltage is applied to the gates. In contrast, the placement of the gates in the AND device is diagonal to each other, ensuring proper AND operation.

Table 5. Device Dimensions for implementing the different logic function

Proposed Device	Fin Width (nm)	Fin Height (nm)	Gate-1,3 Oxide Thicknes s (nm)	Gate-2 Oxide Thicknes s (nm)	Gate Length (nm)
AND	20	20	2 (Gate-1)	2 (Gate-2)	**14**
OR	20	20	2 (Gate-1)	2 (Gate-2)	**14**
AB+BC+CA	22	20	9	3	**14**
B+AC	**42**	**20**	**9**	**3**	**14**

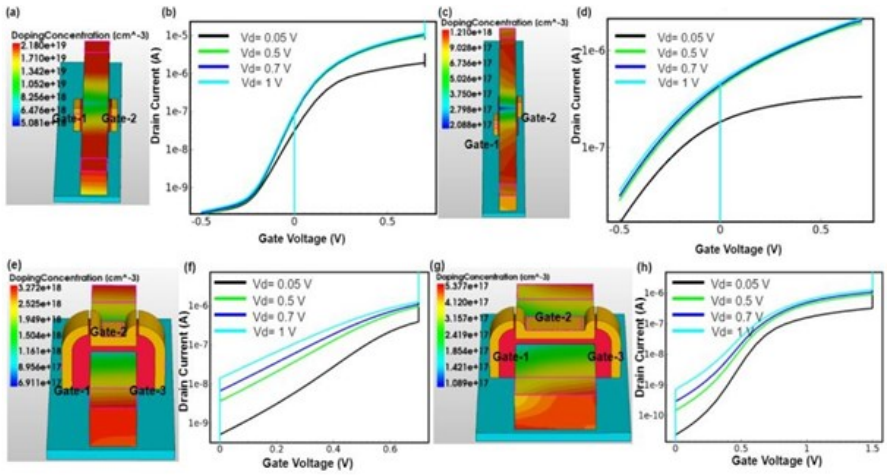


Fig 24. The device structure of proposed Junctionless FET where elementary logic and complex logic are implemented a) OR logic device structure b) Log plot of I-V characteristics of OR logic gate c) Device structure of Junctionless FET where AND logic is implemented d) Log plot of I-V characteristics of AND logic device. e) Device structure of AB+BC+CA logic implemented device f) Log plot of I-V characteristics of AB+BC+CA g) Device structure of B+AC implemented device h) Log plot of I-V characteristics of B+AC device.

In Fig. 24(c), we observe the AND gate implemented in a device with a gate length of 14 nm, a silicon fin height of 20 nm, and a silicon width of 20 nm. The corresponding I-V characteristic of the AND gate device is depicted in Fig. 24(d). From the log plot of the I-V characteristics (Fig. 24(d)), we determine that the device exhibits an ON current of 1 μA and an OFF current of 1 pA, with a threshold voltage of 0.25 V. The detailed dimensions of the device are provided in Table 4.

For implementing the AND logic, the gates are positioned on opposite sides, far away from each other. As a consequence, if any single gate receives a logic 1 input, it will not exert enough control over the fin to create partial inversion and, consequently, will generate a logic 0 at the output. However, when both gates receive logic 1 inputs, the device transitions from the depletion region to the partial inversion region, resulting in a logic 1 output.Using the geometric parameters from Table 5, we model the AND and OR devices. Table 6 presents the total current for all input combinations for both the 2-input AND and OR logic gates. For the 00-input combination, the AND gate produces 1 pA, and the OR gate produces 20 pA, remaining in the OFF state. For the 01 and 10 input combinations, the AND device has a total current of 25 nA, which is lower than the ON current obtained from the device's I-V characteristic due to gate orientation. However, for the OR device, the total current is 10 μA, which is greater than the AND device's ON current, leading to an ON state (logic 1) at the output. When both gates receive a logic 1 input, the AND device has a total current of 1 μA, reaching the ON state, while the OR device draws 20 μA and remains in the ON state.

Table 6. Elementary Logic Total Output Current

Gate-1 Logic Input	**Gate-2 Logic Input**	**OR Gate Total Current (A)**	**AND Gate Total Current (A)**
0	0	2e-11	**1e-12**
0	1	1e-5	**2.5e-8**
1	0	1e-5	**2.5e-8**
1	**1**	**2e-5**	**1e-6**

5.3 Complex Logic Device Architecture

Figures 24(e) and (g) demonstrate the implementation of two distinct complex Boolean functions, AB+BC+CA and B+AC, respectively. Both devices consist of three independent gates, corresponding to the number of inputs required for the logic functions. Leveraging Crosstalk Computing technology, these three independent gate-based Junctionless devices efficiently execute various complex multi-level logic functions, such as AB+BC+CA and B+AC.

The logic function AB+BC+CA represents the expression for a full adder carry function, enabling the production of a full adder using this device. The device can be customized based on the input configuration of the logic function, with customization involving varying the gate location and gate oxide thickness [143].

The implementation of the Boolean Function AB+BC+CA is depicted in Figs. 21(e) and (g), with the device dimensions specified in Table 4. For this function, the output becomes logic 1 when at least two inputs transition from low to high. To achieve this functionality, we customized the device with three equal independent gates, all of equal length contributing to the fin to attain partial inversion. However, to limit excess current flow during switching activities, we opted for different gate oxide thicknesses. Previous work [8] has shown that, while keeping other parameters constant, limiting current flow can be achieved by increasing doping concentration and gate oxide thickness. In this case, the gate oxide thickness for Gate-1 (Input A) and Gate-3 (Input C) is set at 9 nm, while for Gate-2 (Input B), it is 2 nm. HfO2 serves as the gate oxide material. The Junctionless FET features a gate length of 14 nm, a fin width of 22 nm, and a height of 20 nm. Figure 2f provides the log plot of the device's I-V characteristic, indicating an ION of 2.2 μA, IOFF of 1e-10 A/μm, and a threshold voltage of 0.53 V.

Fig. 24(g) illustrates the device structure designed to implement the B+AC logic function. This particular device features a fin width of 42 nm, a fin height of 20 nm, and a gate length of 14 nm made of TiN. Similar to the previous device, HfO2 is used as the gate

oxide material. Specifically, Gate-1 (Input A) and Gate-3 (Input C) have a gate oxide thickness of 9 nm, while Gate-2 (Input B) has a gate oxide thickness of 2 nm. The log plot of the I-V characteristics for this device can be seen in Fig. 2g, showcasing an ON current of 1.2 μA and an OFF current of 6.5e-10 A, along with a threshold voltage of 0.53 V.

To meet the B+AC logic condition, we increase the width of the fin. By doing so, Gate-2 (Input B) will have a broader area to exert control over inversion/partial depletion [145]. Consequently, Gate-2 will produce more current compared to Gate-1 (Input A) and Gate-3 (Input C). To achieve this, we intentionally make Gate-2 wider and set its oxide thickness to 2 nm, enabling it to function as the dominant gate/input to generate more current. As a result, Gate-2 achieves inversion faster than the other two gates and fulfills the B+AC logic.

In this device, Gate-1, Gate-2, and Gate-3 have varying gate areas, with Gate-2 being intentionally wider, and current flow is also limited with the 9 nm oxide thickness in Gates 1 and 3. This gate arrangement is specifically designed to meet the B+AC logic condition. The same Crosstalk setup, as discussed earlier, is applied here, where three gates act as aggressors, and the silicon fin acts as the victim.

5.4 Polymorphic Behavior of the Devices

The concept of polymorphism in devices occurs when different inputs or frequencies are applied, leading to changes in the device's behavior. Our proposed devices exhibit promising characteristics in terms of polymorphism. While elementary devices may not fully display polymorphism due to limited electron routes, complex logic devices show some potential in this aspect. The carry device, represented by AB+BC+CA, demonstrates certain traits of polymorphism. This device consists of three fan-ins: A, B, and C.

When A = 0, gate-1 remains below the threshold due to the logic 0 input voltage. However, gate-2 (input B) and gate-3 (input C) have logic 1 inputs that exceed the threshold voltage. The drain voltage is set at the supply voltage, VDD. In this scenario, when gate-2 and gate-3 are ON, the current flows from the drain to the source, resulting in a logic 1 at the output node of the source. As a result, the AB operation, combined with the AND

operation, does not occur, and the same is true for CA. Since two AND operations do not take place, the AB+BC+CA operation simplifies to BC, which is essentially an AND operation. Therefore, the device AB+BC+CA showcases polymorphism in this specific switching instance, morphing into AB, performing an AND operation.

Similarly, for the device B+AC, gate-2 (input B) is substantially wider than the other two gates. When B = 0, the voltage at gate-2 does not exceed the threshold voltage, rendering gate-2 OFF. Conversely, with gate-1 and gate-3 receiving logic 1 inputs, their voltages surpass the threshold level, leading to their activation (ON state). As the drain is connected to the source voltage VDD, current passes from the drain to gate-1 and gate-3, and subsequently to the source, producing the final output of AC, which represents an AND operation. Thus, the device B+AC polymorphs to AC, functioning as an AND operation.

Similarly, when A = 0, gate-1 becomes OFF, while gate-2 and gate-3 remain ON. However, since gate-1 and gate-3 are paired with an AND operation and gate-1 is OFF, the AND operation does not occur, resulting in the final function being B. This illustrates how our proposed device can achieve polymorphism by changing the input.

The AB+BC+CA device essentially serves as a carry device, acting as a carry circuit. When combined with an XOR device, the whole setup operates as a full adder. Integrating our proposed device with other devices enhances its functionality, and new functions can be achieved through these combinations.

CHAPTER 6

SIMULATION & RESULTS

6.1 Simulation Environment

In this study, the roadmap begins with the initial design and tuning of the proposed circuit using various materials to achieve optimal results. After the device design, a iterative loop is carried out to modify the device multiple times. Throughout this process, the device is examined using different materials for various components. Once the device design is finalized, simulations are performed to characterize its behavior.

The device characterization includes a range of assessments, such as I-V characteristics with both DC and AC characterization, among other criteria. The characterization process is not limited to these aspects and may encompass additional analyses. To facilitate this methodology, a suitable simulation environment is essential. This environment can be established within a single platform, or each step may require the use of different platforms to carry out the simulations effectively.

6.1.1 Device Architecture Simulation

For this research, the device architectures are simulated using Sentaurus SProcess [144]. To achieve the desired architecture, the process begins by defining the wafer coordinates along with the materials used, in this case, Silicon on Insulator (SOI). With the 3D coordinates established, the SOI stack is defined, and both surface coordinates and wafer coordinates are declared. To create the silicon fin, specific masks are defined and applied during the etching process. Once the device layer is etched, the silicon fin is obtained and then subjected to chemical and mechanical polishing (CMP).

Since the device is a junctionless transistor, uniform doping is crucial, and this is achieved through ion implantation. The entire fin body is uniformly implanted with phosphorus to ensure consistent doping. During ion implantation, the tilt rotation is fixed

at 0˚, while the angle remains constant at 7˚. Fig 25 illustrates the relationship between wafer coordinates, simulation coordinates, and the beam direction.

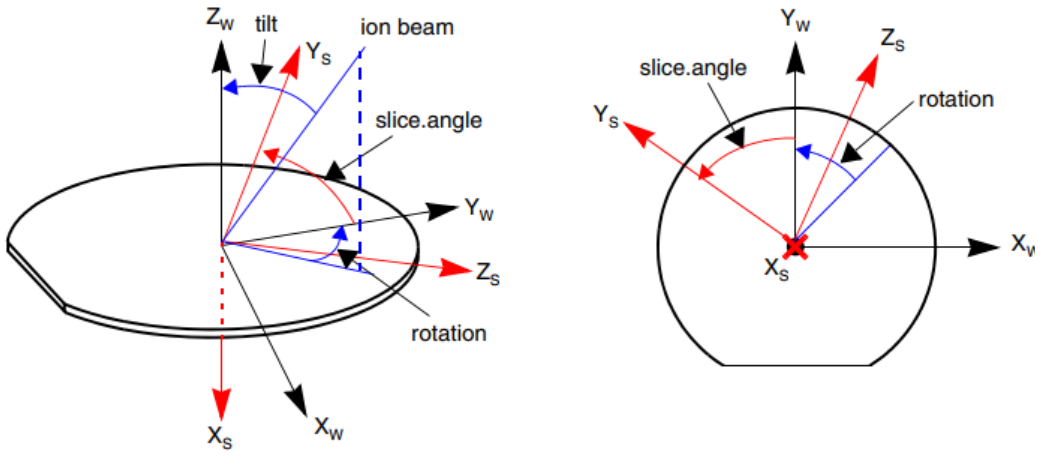


Fig 25. Tilt and rotation angle for implantation. Here, tilt= 20˚ and rotation = 45˚

Following ion implantation, the annealing simulation is conducted with a diffusion process at 500˚C for one hour. This diffusion process is essential to cleanse the fin surface from impurities and debris. To achieve the best results in polishing and obtaining an efficient working surface, the temperature can be adjusted to find the optimum value.

Moving on to gate construction, the initial step involves the deposition of gate oxide. For this research, Hafnium Oxide (HfO2) is chosen as the gate oxide material. It is deposited with a thickness of 1 nm using Atomic Layer Deposition (ALD). To facilitate gate oxide deposition, a necessary mask is created. Once the gate oxide is in place, the gate material, Titanium Nitride (TiN), is deposited using the same mask, employing Chemical Vapor Deposition (CVD).

Upon completion of the gate, mesh refinement is performed. A denser mesh is defined for the gate area and channel, while a regular mesh is defined for other parts of the device. Subsequently, remeshing is applied using the Delaunay-Voronoi refinement algorithm, which generates a three-dimensional tetrahedral mesh. This algorithm follows a divide and conquer approach, where Delaunay triangulation is initially carried out. Delaunay triangulation is an effective method for creating triangles from discrete points, and it serves as the foundation for the Voronoi diagram.

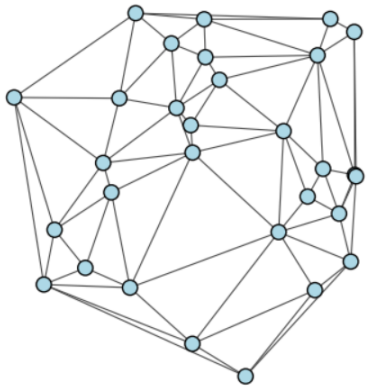


Fig 26. Delaunay Triangulation [161]

In mathematics, a Voronoi diagram is a way of dividing space into a number of regions. A set of points is specified beforehand and for each seed there will be a corresponding region consisting of all points closer to that seed than to any other. The regions are called Voronoi cells. It is dual to the Delaunay triangulation. It is named after Georgy Voronoy, and is also called a Voronoi tessellation, a Voronoi decomposition, or a Dirichlet tessellation. Voronoi diagrams can be found in a large number of fields in science and technology, even in art, and they have found numerous practical and theoretical applications [162].

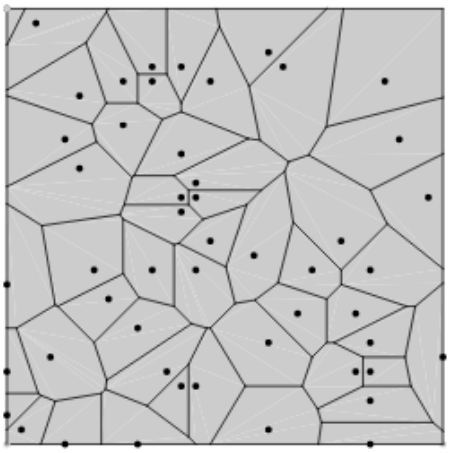


Fig 27. Voronoi Diagram

Delaunay triangles and Voronoi diagram are combined to get a refined mesh of the device [163]

After the refinement of the mesh, the whole structure is reflected on the right side to get the whole device and avoid the computational cost. Source, drain, and gate terminal is defined with Aluminum metal contact to get a complete device for front-end and back-end analysis.

6.1.2 Device Characterization Simulation

The device characterization for this research is performed by Sentaurus TCAD SDevice. This module is optimized for achieving physical parameters like Id-Vg characteristics, Subthreshold Swing, On current, Off Current, and transconductance. To achieve the characterization of a device, an environment with the necessary prerequisite is compulsory. Proper file selection and inclusion of perquisites will lead to a successful environment for device characterization. For this reason, the proper tool flow is obvious. In Sdevice, commands and scriptings will be stored with a file of .cmd extension. If the device requires a special material library a .par file extension is required to include the special material library. As discussed earlier, SDevice is for device characterization. For proper simulation environment, mesh and grid data are also required. These data will transfer from SProcess/ Structure Editor. .cmd and .tdr files are for command and boundary respectively and will create the final gid_mesh.tdr file that will contain mesh and grid data with boundary and will be an input for SDevice along with Sdevice .cmd and .par file extension. The final output files are .plt for graph plotting and .tdr file for plot description. Fig 28. exhibits the tool flow for SDevice.

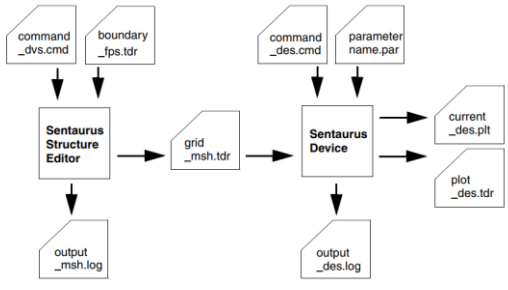


Fig 28. Typical Tool flow of Sentaurus SDevice. [145]

In the first part of environment invocation, in .cmd file input file in the form of .tdr format as well as for plot .plt file and output .tdr must be mentioned. .plt file contains the electrical output data. In the electrode section, electrodes with proper electrode material will be defined. Along with electrodes, offset voltage or boundary voltage can be mentioned. 'Barrier' can be mentioned as a potential barrier or work function.

In the Physics section, the device physics is mentioned. Generally, this section is limited to Mobility and bandgap. In the mobility doping dependence, High field saturation can be mentioned for some specific devices. For bandgap, EffectiveIntrinsicDensity is mentioned that computes intrinsic carrier concentration with Bandgapnarrowing and oldslotboom.

The plot section specifies all the variables that will be stored in the output plot files.

Math section usually solves device equations – partial differential equations, self-consistently, on the discrete mesh, in an iterative fashion. In each iteration, the device tries to converge on a solution that has a very small error. Extrapolate and RelErrControl are required in this section. In extrapolate, the initial guess for a given step is achieved from the previous two equations. RelErrControl switches error control during iterations using internal error parameters.

Solve section provides a sequence of solutions from the solver. In this section, offset voltage and initial bias. To simulate Id-Vg characteristics, it is necessary to ramp the gate bias from 0V to any specific voltage and obtain solutions at a number of points in-between. As the simulation proceeds, output data (current, voltage, charges) are generated and stored in the .plt file. Poisson and continuity equations are generally used as equation solvers.

6.1.2.1 Poisson Equation

The Poisson equation relates electrostatic potential with a given charge distribution. It can be derived from Maxwell eq.:

$$\nabla . D = \rho \tag{15}$$

Where D is the displacement vector and ρ is the charge distribution.

Using the relation between electric displacement vector and electric field vector, we get:

$$D = \varepsilon . E \tag{16}$$

Where ε is the permittivity tensor. This relation is valid for materials with time-independent permittivity. As materials used in semiconductor devices normally do not show significant anisotropy of the permittivity, ε can be considered as a scalar quantity ε in device simulation. The total permittivity is obtained from the relative ε_r and the vacuum permittivity, ε_o as $\varepsilon = \varepsilon_r \varepsilon_o$

∇ x E = 0 when it is stationary, E can be expressed as a scalar potential field.

$$E = -\nabla \Phi \tag{17}$$

Substituting eq 15, 16 in eq 14:

$$\nabla . \varepsilon . \nabla \Phi = - \rho$$

(18)

Regarding permittivity as scalar as it's constant on homogenous material, Poisson Eq becomes:

$$\nabla . \nabla \Phi = - \rho / \varepsilon \tag{19}$$

The space charge density ρ consists of

$$P = q (p - n + C) \tag{20}$$

Where q is the elementary charge, p and n are hole and electron concentration respectively and C consists of the concentration of fixed charge.

$$C = N_D - N_A + p_p - p_n \quad (21)$$

Where ND and NA are donor and acceptor concentrations respectively and p_p and p_n are trapped hole and electron respectively. These are important to trace out device degradation.

Combining Eq 18, 19, and 20:

$$\nabla.\nabla\Phi = -\rho/\varepsilon\,(N_D - N_A + p_p - p_n) \quad (22)$$

6.1.2.2 Transport Equation

There are two major effects of current transport in silicon. Drift current for the influence of electric field and diffusion current by charge gradient.

6.1.2.2.1 Carrier Drift

Charged carriers that are subjected to an electric field are accelerated and acquire a certain drift velocity. The orientation depends on the charge state and electric field. Hole accelerates toward the electric field and electron accelerates away from the electric field. For the low electric field, drift current can be compared with the Ohm's law:

$$J_n^{drift} = \sigma_n E \quad (23)$$

$$J_e^{drift} = \sigma_e E \quad (24)$$

σ denotes the conductivity of the medium and can be expressed as the carrier mobility of electrons and holes.

$$\sigma_n = qn\mu_n \quad (25)$$

$$\sigma_p = qn\mu_p \quad (26)$$

6.1.2.2.2 Carrier Diffusion

A concentrated gradient of carriers leads to carrier diffusion. The reason is the thermal motion of carriers in lower concentrations. This can be depicted as:

$$J_n^{drift} = qD_n\nabla n \quad (27)$$

$$J_p^{drift} = qD_p\nabla n \quad (28)$$

Here D_n and D_p are the diffusion coefficient of electron and hole respectively. In equilibrium for non-degenerate semiconductor can be expressed by Einstein's eq.:

$$D_n = \frac{K_B T}{q}\mu_n \quad (29)$$

$$D_p = \frac{K_B T}{q}\mu_p \quad (30)$$

6.1.2.2.3 Drift Diffusion Current Relation

Combining eq 22 – 29 we get:

$$J_n = qD_n\nabla n \quad + \frac{K_B T}{q}\mu_n \tag{31}$$

$$J_p = qD_p\nabla p \quad + \frac{K_B T}{q}\mu_p \tag{32}$$

6.1.2.3 Continuity Equation

The continuity eq can be derived from Maxwell's eq. :

$$\nabla \text{ x } H = J + \frac{\delta D}{\delta t} \tag{33}$$

By applying Divergence operator ∇ and considering the divergence of a curl of any vector field is zero:

$$\nabla.\nabla \text{ x } H = \nabla.J + \nabla.\frac{\delta D}{\delta t} \quad = 0 \tag{34}$$

Separating current density, J as electron and hole current density, $J = J_p + J_n$:

$$\nabla.J_n + \nabla.J_p + q\left(\frac{\delta p}{\delta t} + \frac{\delta n}{\delta t} + \frac{\delta ND}{\delta t} - \frac{\delta NA}{\delta t} + \frac{\delta \rho p}{\delta t} - \frac{\delta \rho n}{\delta t}\right) = 0 \tag{35}$$

Considering impurities as time-invariant and introducing a new quantity R and separating the eq. into electron and hole:

$$\nabla.J_n - q\frac{\delta n}{\delta t} - \text{ q}\frac{\delta \rho n}{\delta t} = qR \tag{36}$$

$$\nabla.J_p + q\frac{\delta p}{\delta t} + \text{ q}\frac{\delta \rho p}{\delta t} = -qR \tag{37}$$

The quantity R gives the net recombination rate for electrons and holes. A positive value means recombination, a negative value means the generation of carriers.

In quasistationary statement, steady state equilibrium solution will be obtained.

6.2 Methodology

To achieve a functioning device, it is essential to examine the electrical characteristics. The device is designed with Sentaurus Process, which imitates the physical process steps. Obtaining the device by Synopsys Sentaurus Process [144], characteristic analysis is done with the Sentaurus Device [145]. The Sdevice model solves Poisson and carrier continuity equation to determine current behavior characterization. The silicon band structure and the effect of bandgap narrowing are calculated by the Oldslotboom method. From I-V characteristics, ON current, and OFF current is extracted and by examining the value of ON current, logic 0 and logic 1 are determined. the AC and DC behavior of a device cumulate the overall performance of a device (Table 6). For examining DC and AC characteristics of a device, average power, leakage power, and delay are crucial parameters. Average power and leakage power were extracted from the I-V characteristics using the basic formula for power. Propagation delay is calculated using the equation given in [178]:

$$\text{Delay}, \tau = Cg * Vdd / Ion \tag{38}$$

Cg is gate capacitance, Vdd is drain voltage, and Ion is ON current. Considering the condition of ON, the current of 1uA is regarded as logic 1. CMOS counterpart 14nm PTM I_{ON} and I_{OFF} are extracted from HSPICE simulations. Average power and leakage power are also extracted from the HSPICE simulation. To get the proper propagation delay of the PTM devices, the critical path of the circuit is considered and calculated from HSPICE. The Proposed devices and 14 nm PTM CMOS counterpart power and delay are summarized in Tables 7 and 8 .

6.3 Result & Discussion

6.3.1 2 D Devices Result & Discussion

I have successfully implemented a 2-input AND gate using Crosstalk technology in the aforementioned single device. Furthermore, we have demonstrated that crucial device parameters, such as work function and oxide thickness, can be adjusted to achieve the desired logic behavior.

In Crosstalk technology, coupling capacitance plays a pivotal role in attaining the desired logic behavior. The coupling capacitance is inversely proportional to the separation of metal lines and directly proportional to the permittivity of the dielectric and the lateral area of the metal lines. In this case, we have investigated the influence of gate oxide thickness and work function on the gate current. Fig 28i illustrates the impact of the work function on the I-V characteristics of the device. Both linear and logarithmic plots are shown, clearly indicating that the device reaches saturation. The work function strongly correlates with the flat band voltage, threshold voltage, and affects the ON-current and OFF-current. From Figure 29i, we observe that the maximum ON current is achieved when the work function is 3.1eV. For other work function values, the ON current decreases due to the increase in potential barrier and threshold voltage. We have also examined the variation of oxide thickness and its impact on the I-V characteristics. When the oxide layer is very thin, the ON current starts to decrease as the gate loses electrostatic control, and the short channel effect becomes more prominent. However, for other thickness values, the ON-current exhibits a linear relationship with different logic states. Fig 29.ii illustrates that both 0.5nm and 1nm oxide thicknesses result in the maximum ON current. For any other case, the ON current should remain below the threshold value.

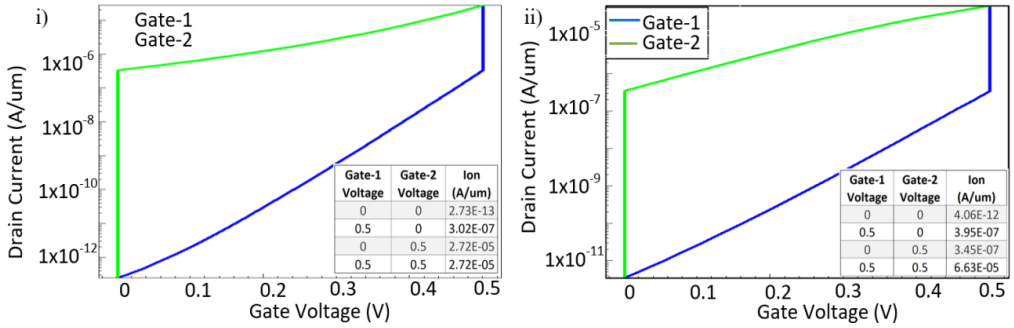


Fig 29 Crosstalk behavior in the proposed device. i) Same gate oxide thickness at Gate-1 and Gate-2; When both gates are at 0.5 V, they will obtain Ion and exhibits AND behavior, ii) Different gate oxide thickness at Gate-1 and Gate-2; Gate-2 gate oxide thickness is 30 A˚ as such exhibits dominant behavior as shown in the table.

It is noticed that work function variation causes variation in device performance. The variation is depicted in Fig 30. Best performance is obtained 4.6 eV and increment in work function decrease the device performance.

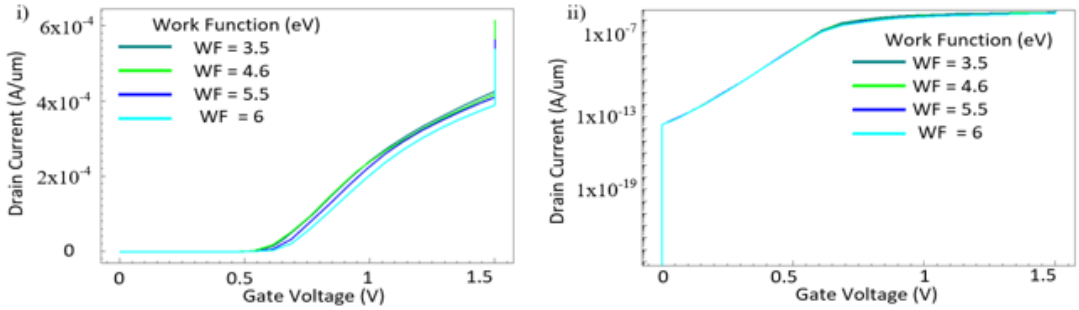


Fig 30. Work Function variation in the proposed device. i) AND device linear plot ii) AND device log plot

Oxide thickness variation also govern the performance of the devices. Increasing thickness decrease the current flow (Fig 31).

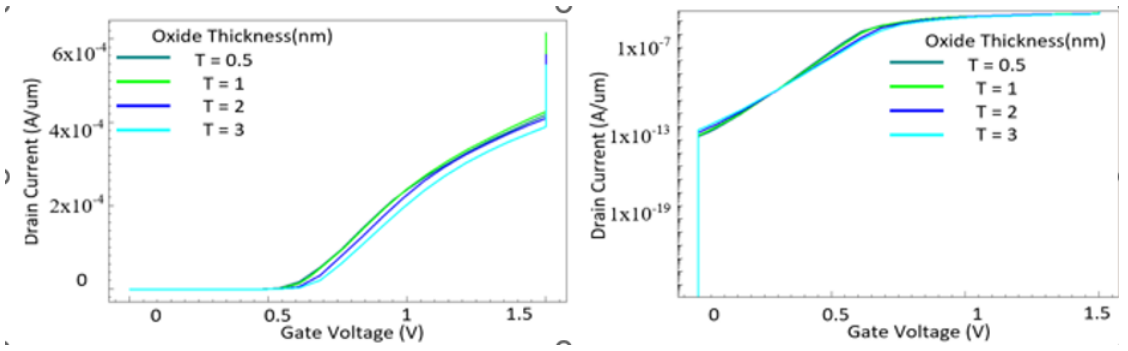
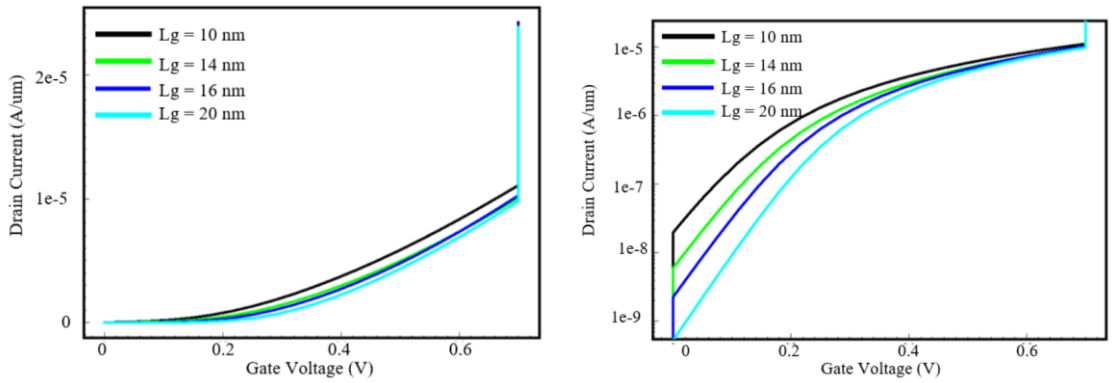


Fig 31. Oxide Thickness variation in the proposed device. i) AND device linear plot ii) AND device log plot

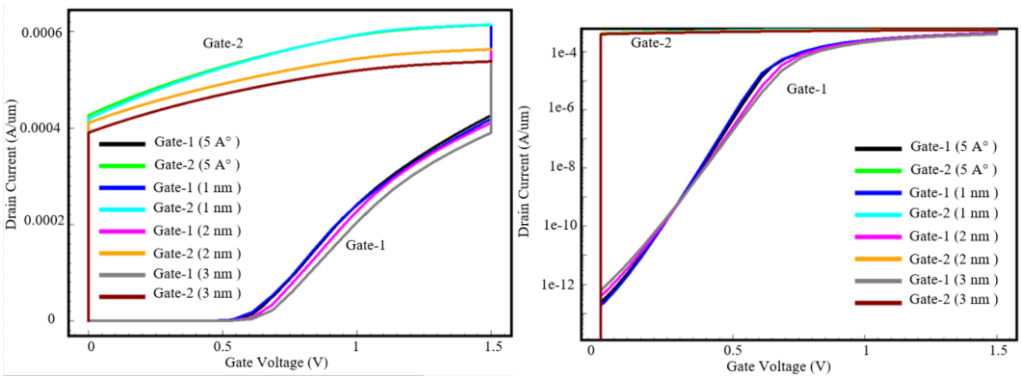
Gate length variation is also a crucial point for the proposed device. Small gate length causes Off current degradation but increase On current (Fig. 32)



(i) (ii)

Fig 32. Gate Length variation in the proposed device. i) AND device linear plot ii) AND device log plot

Gate voltage variation discovers an important aspect of the device characteristics. Gate -2 draws more current than Gate-1. Hence, Gate-2 is the dominant gate in the device (Fig 33).



(i) (ii)

Fig 33. Gate Voltage variation in the proposed device. i) AND device linear plot ii) AND device log plot

6.3.2 3 D Devices Result & Discussion

The current study validates the functional implementation of the standalone device (Fig. 23(a & c), Fig. 21(e & g)) and demonstrates the devices' effectiveness in multi-gate functionality. These findings collectively confirm the legitimacy of our proposed complex logic devices, AB+BC+CA and B+AC.

Fig. 34i showcases selected cases of input combinations (000, 010, 100, 101, 110, and 111) for the AB+BC+CA logic, while Table 3 presents all possible input combinations along with the corresponding gate currents and total current. For a logic 1 output, a threshold current of 1e-7 A was considered to achieve the AB+BC+CA logic. When all gates receive a logic 0 input, the inversion regions overlap, resulting in the device being in a weak inversion state and producing an output current of 1e-10 A, thus remaining in the 'OFF' state. Similarly, when only one gate receives a logic 1 input, the device produces a 5.2e-8 A output current and stays in the 'OFF' state.

In the cases of 011, 110, and 101 input combinations (logic 1 input in two gates), the inversion regions diminish, and a conducting channel forms between the source and drain, leading to an output current of 8.5e-7 A. As a result, the device transitions to the

'ON' state. The same phenomenon occurs when all three gates receive a logic 1 input, resulting in an output current of 2 µA and generating a logic 1 output.

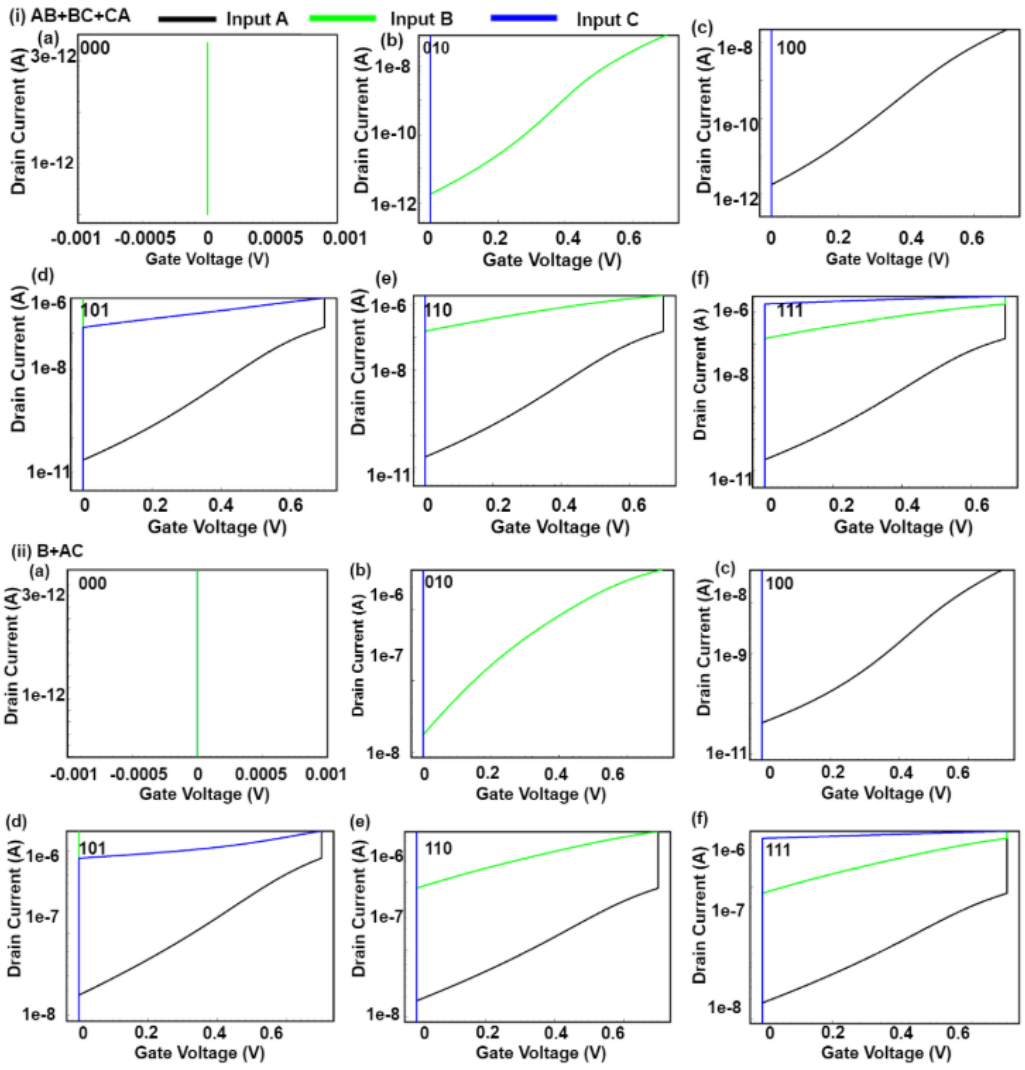


Fig 34. Log plot of I-V characteristics of several switching cases of complex logics i) AB+BC+CA logic Here I-V plot corresponding to a) 000 input b) 010 input c) 011 input d)101 input e) 110 input and f) 111 input ii) Log plot of I-V characteristics of B+AC logic Here I-V plot corresponding to a) 000 input b) 010 input c) 011 input d) 101 input e) 110 input f) 111 input. Here gate-1, 2, and 3 correspond to Input A, B, and C respectively.

Fig. 34ii illustrates selected input cases for the B+AC logic, while Table 6 presents the corresponding current outputs for gates and the total current. From Table 3, it is evident

that when all three gates receive a logic 0 input, they lack sufficient control to achieve inversion, and consequently, the device remains in the depletion region, drawing a current of 1e-10 A, resulting in a logic 0 output. The same scenario occurs for logic 1 inputs in combinations 001 and 100, where the device remains in the depletion region and generates a 5.7e-8 A output current, representing the 'OFF' state.

In the case of the 010 input, the device exhibits a 5.5e-7 A output current, resulting in a logic 1 output. Here, Gate-2 dominates the device's behavior. During the high transition of the input signal, the device enters the partial inversion region, indicating the 'ON' state (i.e., logic 1 output). For input combinations 011, 101, and 110, where multiple inputs are high, the device also enters the partial inversion region, leading to a logic 1 output. For all cases with input 011 and 101, the device produces a 1.6 μA output current. The same pattern is observed for input 111, where the device achieves a logic 1 output through partial inversion and generates a total output current of 2.5 μA from all three gates.

From Table 7, it is evident that all switching cases are similar except for the 010 input, where a logic 1 output is obtained. In the second device, the wider Gate-2 functions as the dominant gate and effectively controls the channel, guiding it towards the partial inversion state. Both figures demonstrate that in situations with multiple high inputs like 011, 101, 110, and 111, one gate emerges as the dominant gate, aggregating all the currents from the other gates and producing the total current.

Table 7 Complex Logic Total Output Current

Device	Gate-1 Logic Input (A)	Gate-2 Logic Input (B)	Gate-3 Logic Input (C)	Current (G-1)	Current (G-2)	Current (G-3)	Total Current
AB+BC+CA	0	0	0	1e-10	1e-10	1e-10	1e-10
	0	0	1	1e-10	1e-10	5.2e-8	5.2e-8
	0	1	0	1e-10	6.3e-8	1e-10	6.3e-8
	0	1	1	1e-10	7e-8	8.5e-7	8.5e-7
	1	0	0	5.2e-8	1e-10	1e-10	5.2e-8
	1	0	1	5.2e-8	1e-10	4e-7	4e-7
	1	1	0	5.2e-8	8.5e-7	1e-10	8.5e-7
	1	1	1	5.2e-8	8.4e-7	2e-6	2e-6
B+AC	0	0	0	1e-10	1e-10	1e-10	1e-10
	0	0	1	1e-10	1e-10	5.7e-8	5.7e-8
	0	1	0	1e-10	5.5e-7	1e-10	5.5e-7
	0	1	1	1e-10	5.2e-7	1.2e-6	1.2e-6
	1	0	0	2.5e-8	1e-10	1e-10	2.5e-8
	1	0	1	2.5e-8	1e-10	1.5e-7	1.5e-7
	1	1	0	2.3e-8	1.4e-6	1e-10	1.4e-6
	1	1	1	2.3e-8	1.4e-6	2.5e-6	2.5e-6

Average power, leakage power, delay, and Power Delay Product (PDP) are also evaluated for the proposed devices of AND, OR, AB+BC+CA, and B+AC, and their comparison with CMOS 14 nm devices is presented in Tables 8 and 9. The average power consumption for the AND logic circuit and the OR device is found to be 0.3 μW and 0.115 μW, respectively, while the 14 nm PTM AND and OR devices consume significantly higher power at 3.74 μW and 6.19 μW, respectively. This substantial difference can be attributed to the reduction in transistor count in the proposed single-device functionality compared to the CMOS counterpart, which involves multiple transistors with more resistive paths. Consequently, the CMOS devices consume significantly more power during multiple switching events.

Both the AND device and the OR device exhibit very low leakage power of 0.064 nW and 0.016 nW, respectively, due to their minimal OFF currents of 0.92 nA and 0.023 nA. In comparison, the 14 nm PTM counterparts have higher leakage power, again influenced by the larger transistor count and resistive paths.

For the proposed AB+BC+CA and B+AC devices, the leakage power is recorded as 0.098 nW and 0.412 nW, respectively, while their 14nm PTM counterparts exhibit higher leakage power at 0.574 nW and 0.373 nW. The minimal leakage power in the proposed devices is attributed to their tiny OFF currents.

The delay for the AB+BC+CA device and the B+AC device is measured at 11.84 ps and 25.51 ps, respectively. The larger width of the B+AC device contributes to its longer delay compared to the AB+BC+CA device. In contrast, the 14 nm PTM counterparts have delays of 59.48 ps and 61.1 ps for AB+BC+CA and B+AC, respectively. The delay is calculated considering the critical path netlist.

The proposed AND and OR devices exhibit delays of 4.45 ps and 3.93 ps, respectively. The smaller gate length in the proposed AND device results in a longer time to achieve partial depletion, leading to its longer delay compared to the proposed OR device. The 14nm PTM AND and OR devices have delays of 37.19 ps and 29.49 ps, respectively. Despite the differences, the proposed devices' delays are in good agreement with their CMOS counterparts.

In summary, the proposed devices demonstrate lower power consumption, minimal leakage, and comparable delays when compared to their 14nm PTM CMOS counterparts. These findings validate the efficiency and promise of our proposed devices in complex logic applications.

Table 8 Power, Delay, and Density Comparison of Elementary Logics

	AND (14nm PTM)	AND (Proposed Device)	OR (14nm PTM)	OR (Proposed Device)
Average Power (μW)	3.74	0.3	6.19	0.115
Leakage Power (nW)	0.346	0.064	0.2	0.016
Delay (ps)	37.194	4.45	29.49	3.93
Transistor Count	6	1	6	1
Area (μm^2)	0.047	0.037	0.047	0.037
PDP (J)	1.39e-4	1.34e-6	4.52e-7	1.83e-4

Table 9 Power, Delay, and Density Comparison of Complex Logics

	AB+BC+CA (14nm PTM)	AB+BC+CA (Proposed Device)	B+AC (14nm PTM)	B+AC (Proposed Device)
Average Power (μW)	9.1	0.6	6.8	1.45
Leakage Power (nW)	0.574	0.098	0.373	0.412
Delay (ps)	59.48	11.84	61.109	25.51
Transistor Count	20	1	8	1
Area (μm²)	0.13	0.062	0.062	0.062
PDP (J)	5.41e-4	7.1e-6	4.16e-6	3.7e-5

Power Delay Product (PDP) indicates the average energy consumed per switching. Regarding our proposed device, AND, OR devices have PDP of 1.34e-6 J and 1.83e-6 J, and CMOS counterparts have much higher PDP because of transistor number. The same case goes for complex logic. Our proposed devices have less PDP than CMOS devices.

Achieving such Crosstalk logic behaviours in a single device indicates a denser circuit design. From the proposed methodology, it is evident that the device consists of lesser transistors with significant benefits. The AB+BC+CA logic circuit will require only one transistor, whereas CMOS technology will involve twenty transistors in the proposed device. For the case of B+AC Logic, the proposed research requires one transistor, where CMOS technology involves eight transistors. In the proposed research, the AB+BC+CA logic circuit space occupation is 10 times smaller compared to the CMOS counterpart regardless of the technology node. For B+AC logic, it is 3 times smaller than the CMOS counterpart. Regarding power, it consumes 8x times less average power than existing CMOS architecture, and the time delay is in picoseconds for both of our proposed devices which can be considered high-speed devices.

6.4 Random Dopant Fluctuation (RDF) Analysis

Random dopant fluctuation (RDF) is analyzed for junctionless devices with TCAD [179]. RDF is a kind of process variation that occurs from implanted impurity concentration. RDF causes threshold voltage fluctuation, degradation of ON current, and

increment of OFF current. RDF effect is simulated on elementary logic devices and complex logic devices.

Considering elementary logic, AND device is selected. Regular AND devices with RDF are compared with On current and Off current. The discrete random dopants are varied from 100 to 500, and performances are compared in Table 6. From this table, the regular AND device and RDF devices have the same current range with fluctuation. For 00 switching conditions, the device with 400 discrete particles has the highest current but is acceptable. For 01 switching condition, the device with 200 discrete dopants has the highest current limit.

In every case, some devices get a little bit extra current. The reason is that all the devices with RDF and the regular devices have the same doping concentration. For threshold voltage, the same reason is applicable.

AB+BC+CA device is analysed with RDF as a complex logic device in Table 10. The device was analyzed with varying discrete dopants from 100 to 500 particles. Compared with the regular device, the devices with RDF are working in the proper current range with a slight fluctuation. The threshold voltage remains the same for the regular device and all cases of RDF. Both ON current and OFF current are in the proper range. For the 011 switching case, the device with 100 discrete particles has the maximum current in the acceptable range. For the 111 switching case, the device with 200 discrete dopants has the highest current in the range. As all the devices are junctionless devices with the same doping concentration all over, that plays a significant role in retaining an acceptable range of current, and very small scale of current fluctuations occur for random dopant effect [221].

Table 10 Comparison of regular AND device and RDF-affected device

Switching Case	Regular	100 Particles	200 Particles	300 Particles	400 Particles	500 Particles
00	1e-12	1e-12	1e-12	1.5e-12	4e-12	1e-12
01	1.4e-8	7.2e-8	8e-8	2.4e-8	6.8e-8	1e-8
10	7.7e-8	6.4e-8	7.5e-8	7.7e-8	8e-8	9.3e-8
11	1.5e-6	1.3e-6	1.3e-6	1.2e-6	1.2e-6	1.2e-6
On Current (A)	1.5e-6	1.3e-6	1.3e-6	1.1e-6	1.1e-6	1.2e-6
Off Current (A)	7e-15	7.7e-15	6e-15	2e-15	2e-14	2e-15
Vt (V)	0.45	0.45	0.45	0.45	0.45	0.45

Table 11 Comparison of regular AB+BC+CA device and RDF-affected device

Switching Case	Regular	100 Particles	200 Particles	300 Particles	400 Particles	500 Particles
000	1e-12	6e-12	2e-12	1e-12	1e-12	6e-12
001	8e-8	8.8e-8	9e-8	9e-8	7e-8	8e-8
010	8e-8	8e-8	6e-8	8e-8	9e-8	9e-8
011	1.5e-6	3.3e-6	1.8e-6	1.2e-6	1.5e-6	1.5e-6
100	7e-8	4.7e-8	3e-8	4e-8	7e-8	4e-8
101	1e-6	1.2e-6	1e-6	1e-6	1e-6	1.3e-6
110	1.5e-6	1.5e-6	1.5e-6	1.5e-6	1.3e-6	1e-6
111	2e-6	1.5e-6	3e-6	1.8e-6	2.5e-6	2.6e-6
On Current (A)	2.8e-6	2.5e-6	3.4e-6	1.6e-6	2.8e-6	2.2e-6
Off Current (A)	1.8e-11	1.1e-11	2.7e-11	4e-12	1.8e-11	6e-12
Vt (V)	0.69	0.69	0.69	0.69	0.69	0.69

Although the RDF problem can be solved, there will be some difficulties with our proposed device. The devices will be hard to fabricate as their gate length is minimal, and the gate location must be precise to get logic output. Hence, there is some fabrication complexity with these proposed devices. Adjacent devices will affect the performance of each other if they are located too close. As a result, a particular distance between devices should be maintained to get noise-free output. Scaling down of devices may affect the noise margin of the devices. These complexities remain in our proposed devices.

6.5 Polymorphism Analysis

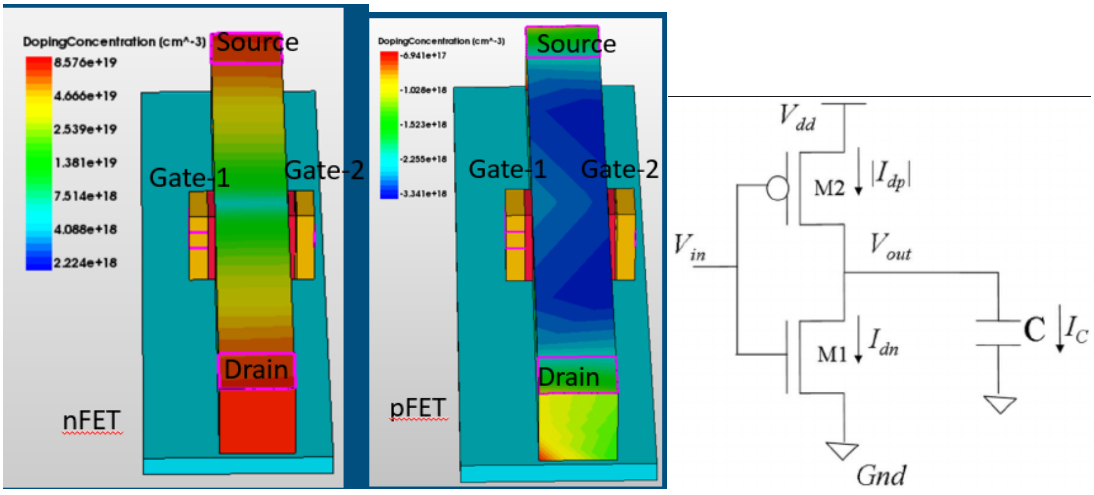
The complex devices show polymorphism. Polymorphism is defined as the change of function by changing inputs. After observing complex device - AB+BC+CA, these phenomena get clearer. When A = 0 and B = 0 then the product AB will be logic 0. As a result, the device's OR function will not work, only AND function will work. For 001 switching condition, output will be logic 0 for OR function. 011 will produce logic 1 output for OR function not for AND function. As for 011 switching condition from Table 11, it is noticed that AB will be logic 0, CA will be logic 0. As AB = CA = 0 then OR function will not work, only AND function will work. Finally, the device will perform only AND function for 011 input. Same case for 101 and 011 input. The device will act as an AND device. By tuning the inputs, we can change the functionality of the device. Hence, AB+BC+CA device has the virtue of polymorphism.

Examining B+AC device, it is noticed that when B = 0, then OR function is not working only AND function will work. Then the final product is AC. The switching condition 101 will show this phenomenon. From Table 6 it is noticed that for 101 switching case, output current is 1.5e-7 A which is logic 1 output. Hence, the device behaves as an AND device and shows polymorphism.

Polymorphism not only depends on inputs but also on input frequency. Our proposed devices are not sensitive to frequency. Hence, after varying frequency the device will not morph it's functionality. This is true for both devices.

6.6 System-Level Integration

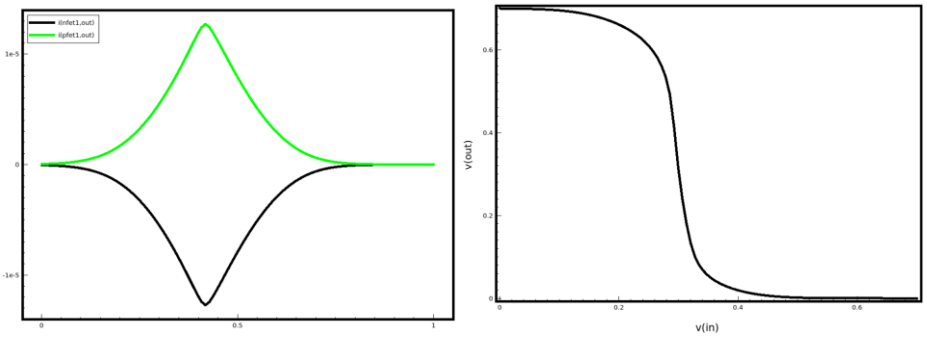
System-level integration is also explored for this proposed research. The proposed devices are implemented in a circuit and the netlist is generated from SDevice. With the proposed devices, an inverter circuit is implemented in SDevice (Fig. 35)



(a) (b) (c)

Fig 35 (a) nFET (b) pFET (c) netlist implementation of the circuit

After the implementation of netlist, transient analysis is performed, and I-V and transfer characteristics of the circuit is extracted from the simulation (Fig. 36). But the netlist is required to be further calibrated to get optimum results.



(a) (b)

Fig 36 (a) I-V characteristic (b) Transfer Characteristics

6.7 Crosstalk Circuits Comparison

Extensive comparison was conducted between CMOS and Crosstalk [118], wherein three MCNC benchmark circuits were implemented and their density, power, and performance results were compared to CMOS at 7nm. Fig 37. illustrates that the mux circuit experienced the highest reduction in transistor count at 62%. The cm85a and pcle circuits showed reductions of 59% and 23% in transistor count, respectively. On average, Crosstalk circuits exhibited 58% power benefits over their CMOS counterparts, primarily due to the reduction in transistor count. However, despite the significant transistor count reduction in the mux circuit, the decrease in average power was not substantial. This can be attributed to the extensive use of pass-gate circuit styles, which result in increased switching activities. Conversely, the pcle circuit demonstrated greater power reduction as it requires fewer buffer and pass-gate circuit styles, leading to reduced switching activity. Supplementary details regarding all implementations are provided in the supplementary section. Additionally, for the cm85a and pcle circuits, Crosstalk circuits exhibited performance improvements of 10% and 53%, respectively.

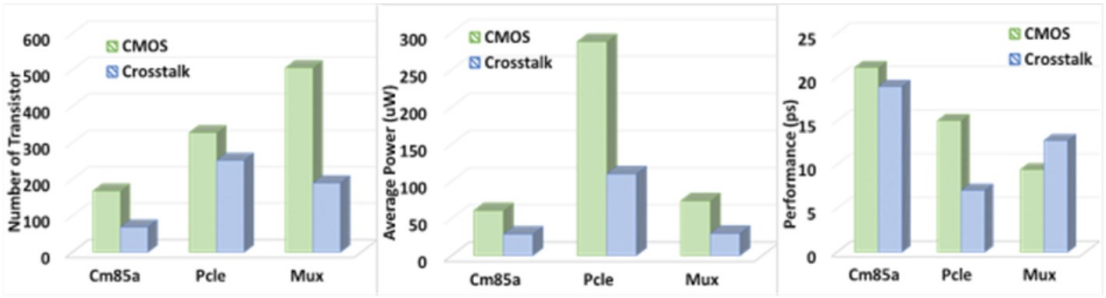


Fig 37 Difference in different large-scale MCNC Benchmark Circuits. i) Density Comparison, ii) Average Power and Performance

To further validate our work, we conducted a scalability analysis on Crosstalk basic gates. Fig 38 presents the scalability study of the Crosstalk NAND gate compared to CMOS at different technology nodes, namely 180nm, 65nm, 32nm, and 7nm, considering process variations. In Fig 30.i, it is evident that both CMOS and Crosstalk NAND gates exhibit a

reduction in power. However, Crosstalk gates demonstrate approximately 42.5% more power reduction than CMOS gates across all technology nodes. This improvement in power can be attributed to the lower number of active devices and the decreased effective load resulting from the series connection of coupling capacitance to the inverter. Fig 32.ii displays the performance results of Crosstalk gates compared to CMOS for various process corners. For the typical process corner, Crosstalk gates exhibit an average performance improvement of 34% compared to CMOS across all technologies. As illustrated in Fig 32(i&ii), the slow process corner yields the worst performance due to the sluggish PMOS and NMOS devices, while the FF corner offers the best performance owing to the fast active devices. The performance enhancement observed in Crosstalk circuits stems from lower effective load capacitances, reduced interconnect parasitics, and shorter VDD/GND to output rail connections.

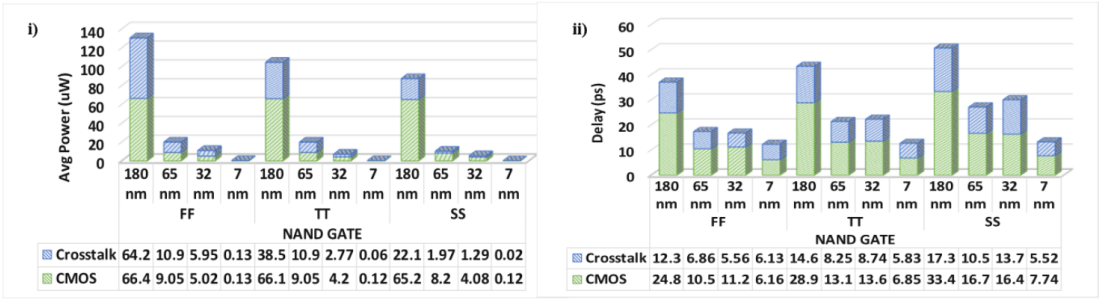


Fig 38. Technology scaling impact on the performance for Crosstalk and CMOS NAND gate with process variation. i) Average power for & ii) Performance of NAND Gate at 180nm, 65nm 32nm, and 7nm with process variations

CHAPTER 7

CONCLUSION

The implementation of advanced devices for nanoelectronics has been the subject of intense research for several decades. Among the new technologies, the junctionless field-effect transistor (JLFET) has drawn significant attention due to its unique characteristics. The JLFET has shown great potential for use in the design of digital circuits and memory elements, mainly due to its superior electrostatic control and reduced short-channel effects.

This dissertation has explored the various aspects of the JLFET, including the device structure, fabrication process, and electrical properties. The work has focused on the multi-gate junctionless FET (MGJLFET) structure, which is a more advanced version of the conventional JLFET with multiple gates.

The work has started with a review of the state-of-the-art technologies in the field of nanoelectronics and the need for new devices to overcome the limitations of conventional MOSFETs. The JLFET has been introduced as a promising candidate for future nanoelectronics due to its unique structure and properties.

The fabrication process of the MGJLFET has been discussed in detail, starting from the design and simulation of the device using advanced software tools. The device has been fabricated using state-of-the-art lithography and deposition techniques, followed by electrical characterization using different measurement techniques.

The electrical properties of the MGJLFET have been extensively investigated, including the current-voltage characteristics, transconductance, gate capacitance, and subthreshold swing. The results have shown that the MGJLFET has superior electrical properties compared to the conventional JLFET, mainly due to the multiple gates that provide better electrostatic control and reduced short-channel effects.

The functionality of the MGJLFET as a digital circuit element has also been investigated, and the results have shown that the device has the potential to be used in the design of high-performance digital circuits. The device has been used to design and

simulate different logic gates, including the NAND and NOR gates, and the results have shown excellent performance in terms of speed and power consumption.

Overall, this dissertation has shown that the MGJLFET is a promising device for future nanoelectronics due to its unique structure and superior electrical properties. The device has the potential to be used in the design of high-performance digital circuits and memory elements, and further research is required to explore its full potential in different applications.

Our proposed devices have some constraints which should be addressed. The devices' delay may mismatch with the 14 nm technology node. As the proposed devices are in still the development phase, some crucial parameters like delay may lag contemporary technology nodes. Our proposed devices have delay more than contemporary 14 nm devices. As a result, switching will lag for our devices as well as propagation delay will increase. For the improvement of the proposed devices, AC analyses will be performed in the near future.

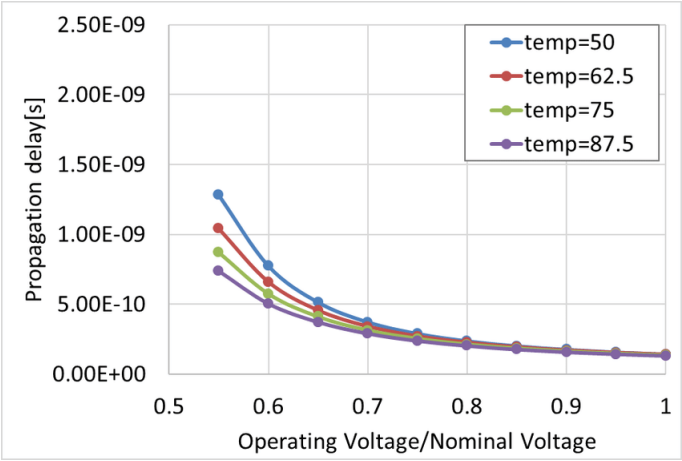


Fig 39: Propagation delays of contemporary technology node [222]

Our proposed devices have the problem of higher leakage power than contemporary 14 nm technology node devices [223]. As we are utilizing higher technology node devices,

the leakage power is also getting higher. Reducing the higher leakage power will be a future research plan.

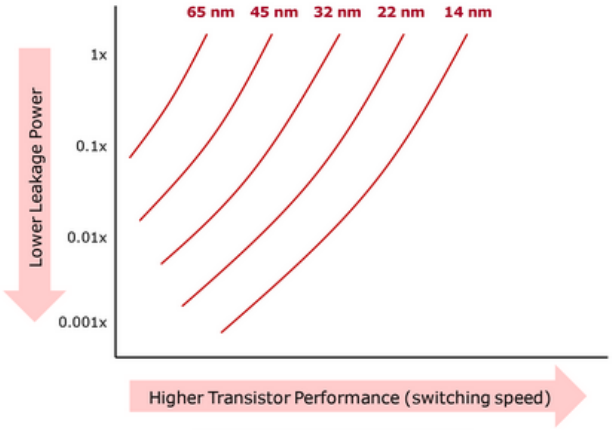


Fig 40. Leakage Power Vs performance of several technology nodes [223]

Circuit integration is another issue for this research. If the circuit contains various technology nodes then, it will be a challenge to integrate all nodes. Misconnection will cause excess power leakage and noise generation. Hence, integration will be a challenge to deploy the proposed research.

In the realm of Very Large Scale Integration (VLSI) circuits, noise margin plays a pivotal role in ensuring the reliable operation of digital systems (Fig. 41). However, when a circuit exhibits a bad noise margin, it becomes susceptible to various sources of noise, leading to erroneous logic levels and potentially catastrophic consequences. From Table 6 it is noticed that in some switching cases. Bad noise margin causes data corruption, reduced robustness, noise immunity, increased sensitivity to Environmental factors, and most alarmingly performance trade-off. To address this problem, future work will include the following steps:

1. Noise Filtering and Shielding: Implementing noise filtering mechanisms, such as decoupling capacitors and inductors, can help suppress noise sources and reduce their impact on the circuit. Additionally, proper shielding and isolation techniques can minimize the coupling of noise between different parts of the circuit.

2. Process Optimization and Variation Compensation: Optimizing the manufacturing process and employing techniques like process corner analysis and variation-aware design can help mitigate the impact of process variations on noise margin. This approach ensures that the circuit is less susceptible to noise-induced errors across different process corners.

3. Signal Integrity Analysis: Performing thorough signal integrity analysis during the design phase can identify potential noise-related issues early on. Simulation tools and techniques can help identify critical paths, evaluate noise margins, and determine potential areas of vulnerability. By addressing these issues proactively, the effects of a bad noise margin can be minimized.

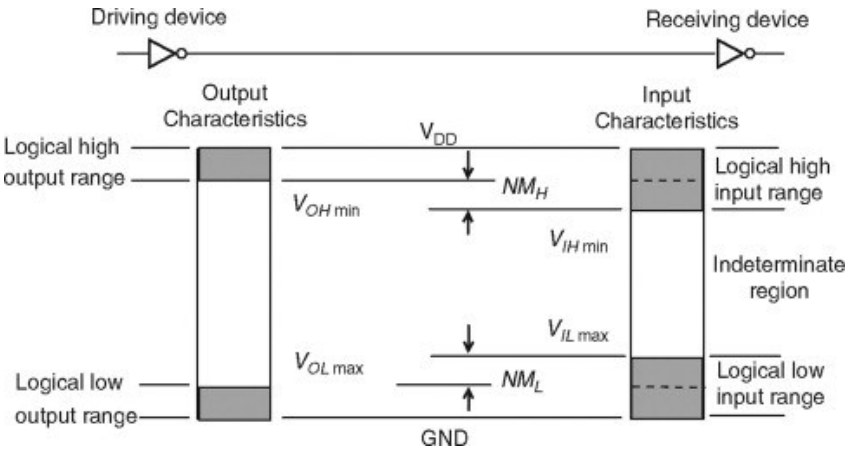


Fig 41. Noise margin [224]

Our future work also includes nanofabrication. First, before fabricating the devices, it is always good practice to fabricate patterns on the wafers (Fig 43). To fabricate a pattern, Silicon On Insulator (SOI) wafer is prepared with several steps. First, the wafer is cleaned with piranha solution for five minutes and washed with Acetone (sonication for ten minutes) then washed with Isopropanol and DI water respectively (Fig 43(a)). With a spin coater seventy-nanometer PMMA is coated over the wafer and the wafer is baked for one minute. Then the wafer is exposed to Electron Beam with a specific mask and the wafer is

dipped in MIBK developer for five minutes (Fig 43(b)). Ten-nanometer chromium is deposited on top of all layers and washed with acetone and get our desired pattern.

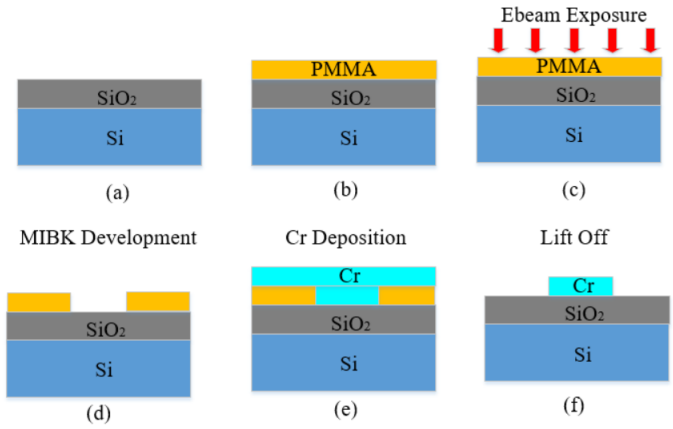


Fig 42. Lithography process steps of fabricating patterns.

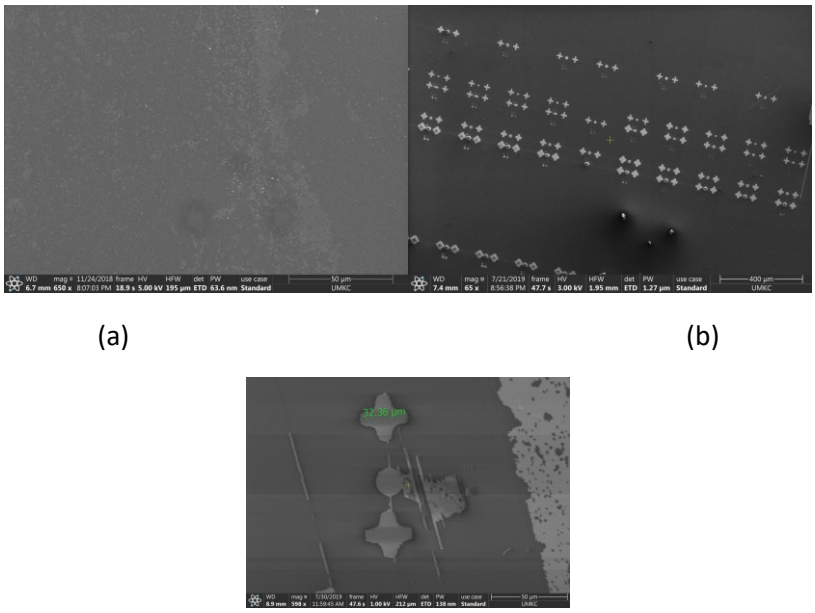


Fig 43. SEM microscopy of (a) Clean wafer (b) Mask pattern after MIBK developer (c) Lift Off

Up to this point, the pattern is already generated. In the near future, nanodevices will be fabricated with the experience of pattern generation. At first, the fin will be fabricated same process as pattern generation. For that at first, a hard mask of Si_3N_4 will be deposited and with lithography fin pattern will be fabricated with the hard mask on top of the fin. On both sides of the fin, SiO_2 will be deposited as another mask and etched to ten nm thickness. Then one nm thickness of HfO_2 is deposited on a specific area as a gate oxide with Atomic Layer Deposition (ALD). On top of that TiN will be deposited as gate material. At both sides of the gate, on the fin,1e20 / cm^3 dose of Boron will be deposited for Source and Drain region. The whole fabrication process is depicted in Fig 44.

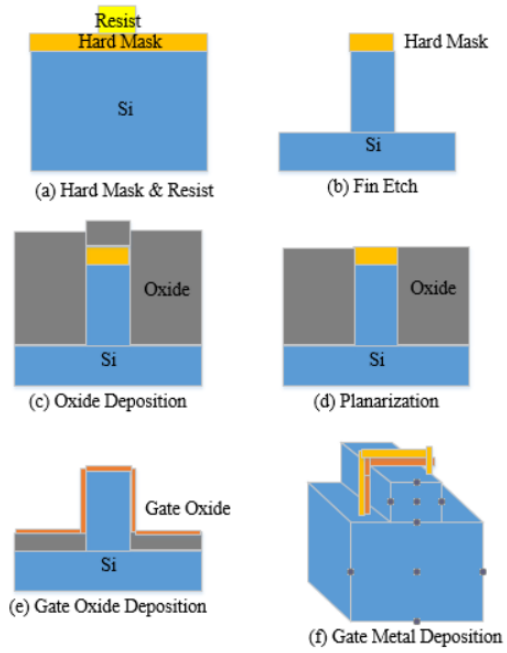


Fig 44. The fabrication process of the proposed device

In conclusion, this work has contributed to the field of nanoelectronics by providing a detailed investigation of the MGJLFET structure and its properties. The results have shown that the device has great potential for use in advanced digital circuits and memory elements, and further research is needed to explore its full potential in different applications. The work has also highlighted the importance of advanced simulation and fabrication techniques for the development of new devices in nanoelectronics.

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VITA

Sehtab Hossain was born on January 29, 1986, in Dhaka, Bangladesh. He received his B.Sc. degree in Electrical and Electronics Engineering from the Islamic University of Technology (IUT), Bangladesh in 2008. Mr. Hossain achieved his M.S. degree in Electrical Engineering from the University of North Dakota (UND) in 2015. Currently, he is a Ph.D. candidate in the Department of Electrical and Computer Engineering at UMKC.

Mr. Hossain has around five years of teaching experience at the undergraduate level. At UMKC, he taught ECE 227, ECE-277, ECE-303, and ECE-331. The classes consist of lectures and practicum. During his studies at UMKC, Mr. Hossain took part in several outreach programs, in collaboration with other departments.

His research interest falls in nanoelectronics and device physics – developing nanodevices that are capable of performing specific Boolean functions. Currently, he is working on improving the signal and noise margin of the proposed devices with Dr. Mostafizur Rahman. He also worked on a research project to analyze the thermal efficiency of IR imaging. In the future, Mr. Hossain is also interested in doing research on device physics, nanodevice fabrication, and AI chips.