LOW DIELECTRIC CONSTANT-BASED ORGANIC FIELD-EFFECT TRANSISTORS AND METAL-INSULATOR-SEMICONDUCTOR CAPACITORS

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In Partial Fulfillment
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Doctor of Philosophy

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by
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The undersigned, appointed by the Dean of Graduate School, have examined

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LOW DIELECTRIC CONSTANT-BASED ORGANIC FIELD-EFFECT TRANSISTORS AND METAL-INSULATOR-SEMICONDUCTOR CAPACITORS

Presented by Ndubuisi Benjamin Ukah

A candidate for the degree of Doctor of Philosophy

And hereby certify that in their opinion it is worthy of acceptance.

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DEDICATION

I cannot exhaust my many thanks to my loving wife, pillar of support, and co-strategist – Ahunna, who having traveled this extraordinary road before me, stood by me every step of the way. I also express my indebtedness and gratitude to my loving parents, sister, and brothers for their support, encouragement, sacrifice, and prayers throughout my graduate degree journey. I pray for the blessings of Almighty God on them, friends and well-wishers.

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ABSTRACT

This thesis describes a study of PFB and pentacene-based organic field-effect transistors (OFET) and metal-insulator-semiconductor (MIS) capacitors with low dielectric constant (*k*) poly(methyl methacrylate) (PMMA), poly(4-vinyl phenol) (PVP) and cross-linked PVP (c-PVP) gate dielectrics. A physical method – matrix assisted pulsed laser evaporation (MAPLE) – of fabricating all-polymer field-effect transistors and MIS capacitors that circumvents inherent polymer dissolution and solvent-selectivity problems, is demonstrated. Pentacene-based OFETs incorporating PMMA and PVP gate dielectrics usually have high operating voltages related to the thickness of the dielectric layer. Reduced PMMA layer thickness (≤ 70 nm) was obtained by dissolving the PMMA in propylene carbonate (PC). The resulting pentacene-based transistors exhibited very low operating voltage (below -3 V), minimal hysteresis in their transfer characteristics, and decent electrical performance. Also low voltage (within -2 V) operation using thin (≤ 80 nm) low-k and hydrophilic PVP and c-PVP dielectric layers obtained via dissolution in high dipole moment and high-*k* solvents – PC and dimethyl sulfoxide (DMSO), is demonstrated to be a robust means of achieving improved electrical characteristics and high operational stability in OFETs incorporating PVP and c-PVP dielectrics.

CHAPTER 1

INTRODUCTION

Until recently, semiconductor optoelectronics research has been restricted to the conventional inorganic semiconducting materials. Owing to the discovery in 1977 of the first highly conductive polymer – polyacetylene, by A. J. Heeger, H. Shirakawa, and Alan G. MacDiamid (Nobel Prize in Chemistry in 2000), intense research efforts have been directed at organic semiconductors and devices resulting in the birth of organic electronics [1]. Organic electronics is basically electronic devices made using organic materials (organic dielectrics, conjugated and small molecule semiconductors). The existence of π-orbitals in organic materials is responsible for carrier transport and semiconducting properties in these materials. Typical organic electronics include organic field-effect transistors (OFETs), organic light-emitting diodes (OLEDs) and organic photovoltaics.

The interest and increased research activities in solution-processable organic devices are due to their promise in large-area electronics fabricated on flexible substrates using low-cost and unconventional means such as spincoating, low/room temperature printing, and roll-to-roll processing [2]. Interestingly, some of the best

OFETs have shown performances that compare favorably well with amorphous silicon thin film transistors [3]. However, considerable challenges still need to be addressed in order to reap the full benefits of organic electronics. Such challenges include the inherent problems of polymer dissolution and solvent-selectivity particularly encountered in the fabrication of all-polymer devices as well as the difficultly in fabricating stable and low-operating voltage OFETs owing to the low dielectric constants of conventional polymer dielectric materials. Contained in this work are facile strategies for overcoming these above-mentioned organic electronics problems.

This report begins with a discussion of the working principles of metal-insulator-semiconductor (MIS) structures (field-effect transistors and capacitors) in chapter 2. Chapter 2 also contains brief descriptions of the organic materials employed in this work. Chapter 3 contains an overview of thin film deposition techniques for organic devices, organic devices fabrication procedure, device structures as well as some concise descriptions of employed device characterization techniques. Chapter 4 begins the results chapters. It discusses the morphology and electrical characteristics of poly (methyl methacrylate) (PMMA) films and electrical characterization results of our all-polymer OFETs and MIS capacitors with matrix-assisted pulsed-laser evaporated polymer semiconducting layers. Chapter 5 contains discussions about the morphology of pentacene films and electrical characterizations of pentacene OFETs and diodes incorporating PMMA dielectric layers. It also demonstrates the feasibility of low-operating voltage pentacene OFETs based on single-layer PMMA polymer dielectric. Chapter 6 also discusses electrical characterizations and operational as well as

environmental stability of high-mobility and low-operating voltage pentacene OFETs based on single-layers of pristine poly (4-vinyl phenol) (PVP) and cross-linked PVP (c-PVP). Here, the use of thin PVP and c-PVP layers with consequent low-voltage operation is demonstrated to be a robust means of achieving stability in pentacene-based OFETs incorporating PVP and c-PVP dielectrics. The report ends with some concluding remarks and suggestions for future work in Chapter 7.

CHAPTER 2

WORKING PRINCIPLES OF MIS DIODES

2.1 MIS Capacitance

An understanding of the working of the two-terminal MIS capacitor is critical for a proper understanding of the operations of the three-terminal MIS field-effect transistor (MISFET). Here, we will begin by defining some of the relevant terms. ϕ_m is the modified work function for the metal-insulator interface and it is the energy measured from the metal Fermi level to the conduction band of the insulator. ϕ_s is the modified work function at the semiconductor-insulator interface. In an idealized case, ϕ_m and ϕ_s are assumed to be equal, which means that there is no difference in the two work functions. ϕ_F is a measure of the position of the Fermi level below the intrinsic level of the semiconductor, E_i.

When the voltage across the ideal MIS structure is zero, flat-band conditions are at hand as shown in Fig. 2.1a. Assuming a p-type semiconductor, for a negative potential on the metal as shown in Fig. 2.1b, an effective negative charge is deposited on the metal and in response, an equal positive charge accumulates at the surface of the semiconductor giving rise to an accumulation of holes at the semiconductor-insulator

interface. The applied negative voltage results in the raising of the electron energies in the metal relative to the semiconductor; as a result, the Fermi level of the metal, E_{Fm} now lies above its equilibrium position by qV where V is the applied voltage.

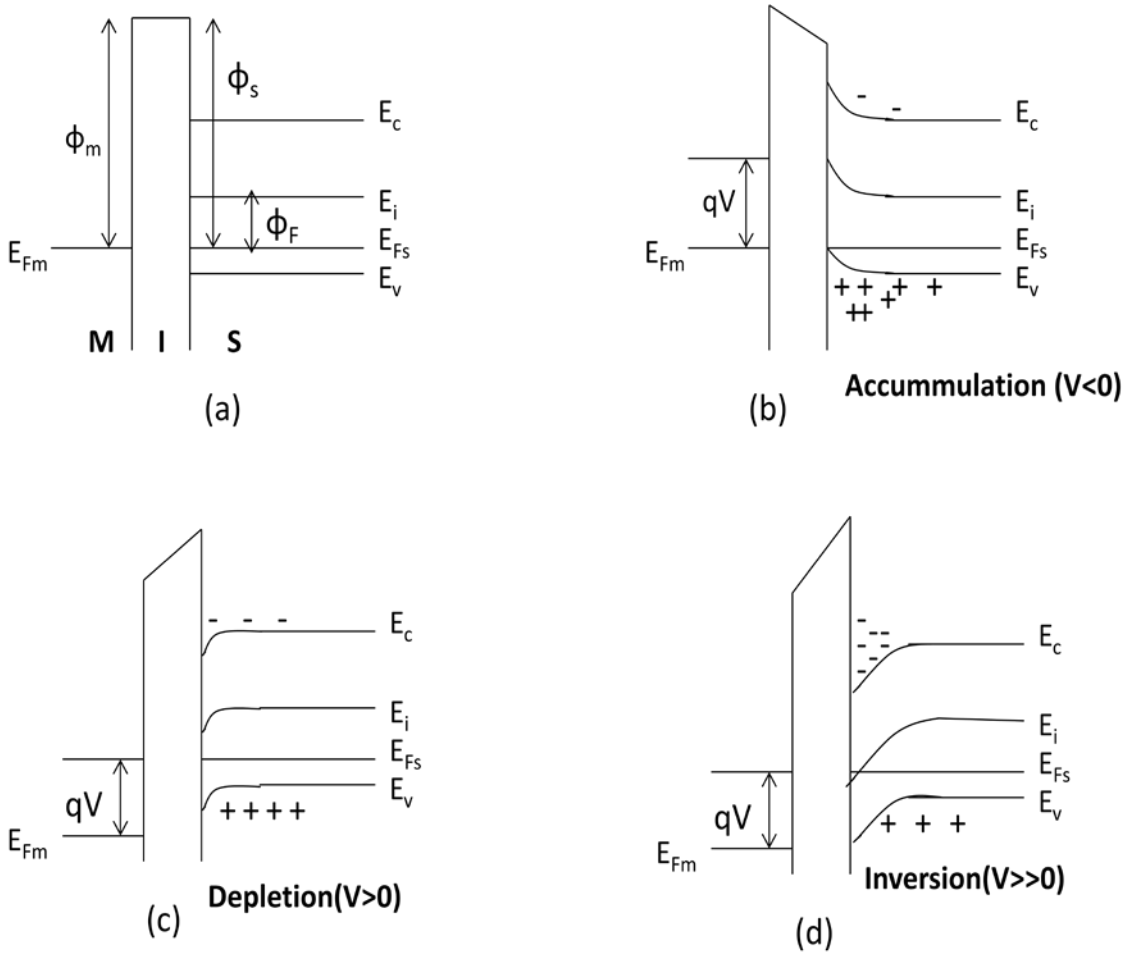

Figure 2.1: Energy band diagrams for an ideal p-type MIS device under (a) flat band, (b) accumulation, (c) depletion and (d) inversion conditions.

The energy bands of the semiconductor are seen to bend near the interface in order to accommodate the accumulation of holes, causing E_i to move up in energy near the surface due to a non-variation of the Fermi level in the semiconductor.

An application of a positive voltage causes the deposition of positive charges on the metal which results in corresponding negative charges at the surface of the semiconductor. The negative charges are due to a depletion of holes from a region near the surface which leave behind uncompensated ionized acceptors. As can be seen from Fig. 2.1c, the bands bend down near the semiconductor surface due to the decrease in the hole concentration and consequent shift of E_i closer to E_F. An increase in the positive voltage results in further downward bending of the bands at the semiconductor surface and at large enough positive voltage, E_i bends below E_F. At this point, the region near the semiconductor surface has conduction properties much like that of an n-type material, which is formed not by doping but by inversion of the originally p-type semiconductor caused by the applied voltage. This inverted layer is highly critical to inorganic MIS capacitor and transistor operations.

Three distinct capacitance components are distinguishable in a MIS structure (Fig. 2.3). Since charge storage results in capacitance, a charge exchange that take place between the semiconductor-insulator interface states and the energy bands in the semiconductor contributes a capacitance, C_i which is in parallel with the depletion capacitance of the semiconductor, C_s. This combination is in series with the insulator layer/bulk capacitance, C_b resulting in a total capacitance, C given by,

$$C = \frac{dQ_G}{dV_G} = \frac{C_b(C_i + C_s)}{C_b + (C_i + C_s)} \qquad 2.1$$

From Equation 2.1, it is obvious that *C* is voltage-dependent which could be helpful in acquiring information about charges and electron states in the insulator and at the

semiconductor-insulator interface. The MIS structure could be represented by an equivalent circuit as shown in Fig. 2.2.

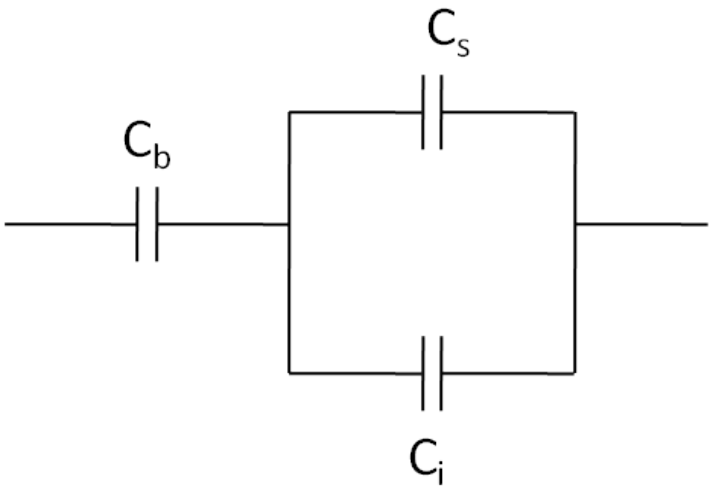

Fig. 2.2: Equivalent circuit of a MIS structure.

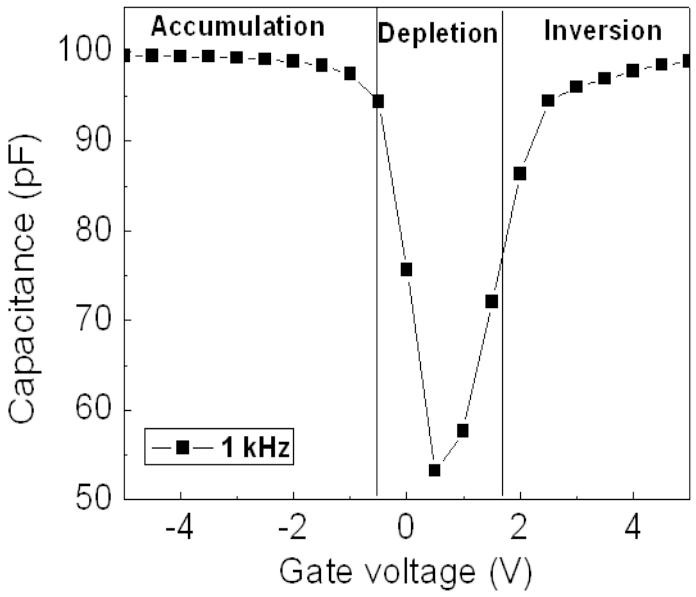

Fig. 2.3: Capacitance-voltage characteristics for a typical Si-based MIS capacitor indicating the accumulation, depletion, and inversion regions.

2.2 Charges and Potentials

The MIS structure is essentially a capacitor in which one of the plates is a semiconductor. There are four types of charge sources in a MIS structure: interface states, fixed interface charges, mobile ions, and impurity centers (Fig. 2.4) [4].

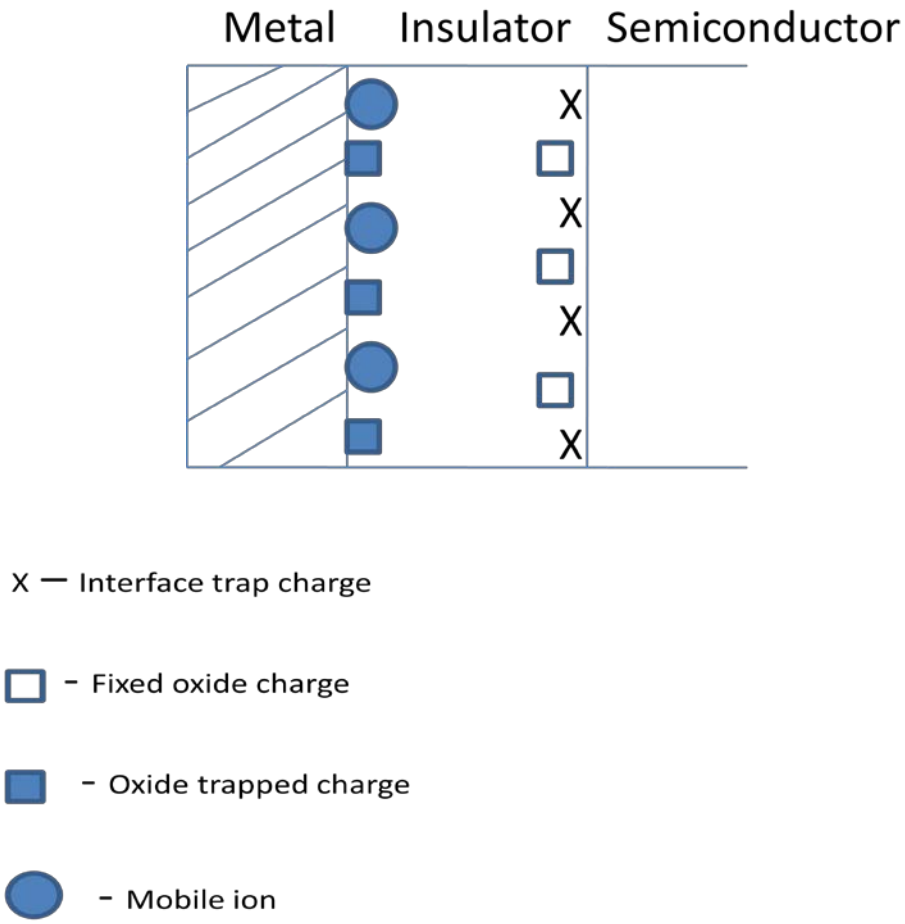

Fig. 2.4: Different types of charges occurring in a typical Si-based MIS structure.

The interface states are electron states at the interface between the insulator and semiconductor. Charge carriers can be captured and emitted at these states and they can also communicate with the energy bands of the semiconductor. The fixed interface charges cannot be filled or emptied from the semiconductor and have energy levels that

are often positioned outside the semiconductor band gap. The mobile ions move by diffusion or electric field drift in the insulator. The ionized impurity centers constitute deep-lying energy levels in the band gap of the insulator. As seen in Fig. 2.5, [4] there is a plane charge, Q_G at the metal-insulator interface. Fixed interface charges,

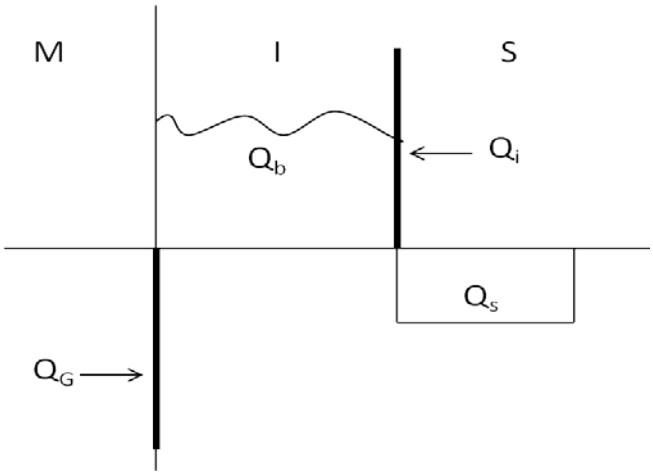

Fig. 2.5: Charge distribution in a MIS structure.

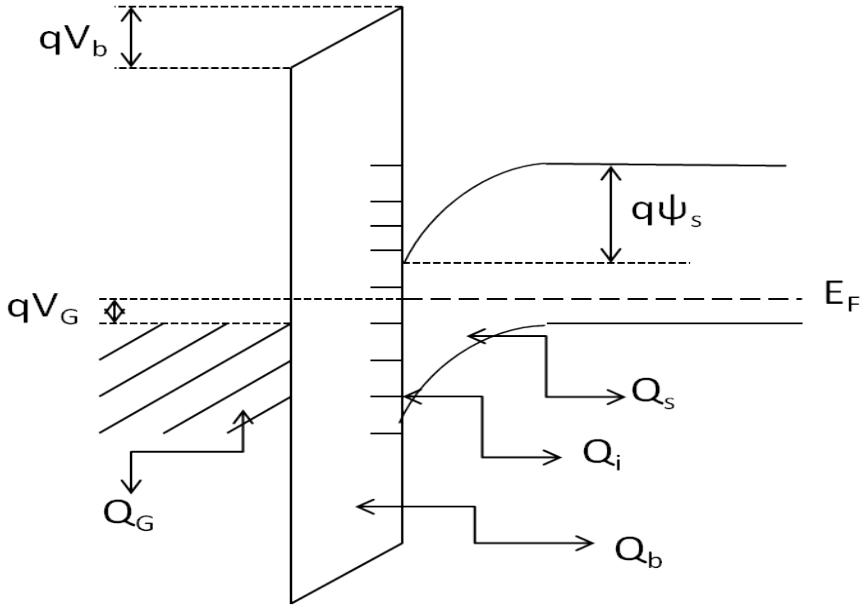

Fig. 2.6: Energy band diagram of the MIS structure.

mobile ions and ionized impurity centers form a volume charge, Q_b. At the insulator-semiconductor interface, a surface charge, Q_i is manifested by the interface states and in the space-charge region of the semiconductor, there exists a total charge, Q_s. Considering a p-type semiconductor, the band diagram of a MIS structure is as shown in Fig. 2.6 [4]. When the metal and the semiconductor are connected to external conductors involving a voltage source, a charge Q_G appears in the metal and it is related to the above-mentioned charges by,

$$Q_G + Q_b + Q_i + Q_S = 0 \qquad 2.2$$

These charges will give rise to a voltage drop V_1 across the insulator with a distribution of charges depicted in Fig. 2.6.

$$V_1 = -\frac{Q_b}{C_i} \quad , \qquad 2.3$$

where C_i is the insulator capacitance per unit area. A second potential, V_2 from the interface charge, Q_i and the charge in the semiconductor, Q_s is given by,

$$V_2 = -\frac{Q_s + Q_i}{C_i} \qquad 2.4$$

The total insulator potential, V_i is given by,

$$V_i = V_1 + V_2 = -\frac{Q_s + Q_i + Q_b}{C_i} \qquad 2.5$$

For different values of ϕ_m and ϕ_s, a potential ϕ_{ms} (ϕ_m - ϕ_s) exists even before the metal and semiconductor are brought into contact. Finally, the total potential drop, V_G across the MIS structure is given by,

$$V_G = \phi_{ms} + V_i + \psi_s \qquad 2.6$$

where ψ_s is the surface potential occurring in the semiconductor due to the depletion region. Using the expression for V_i in equation 2.5, V_G becomes,

$$V_G = \phi_{ms} - \frac{Q_s + Q_i + Q_b}{C_i} + \psi_s \qquad 2.7$$

A reference point for practical application is the gate voltage which needs to be applied on the gate in order to eliminate the depletion region or "flatten" the energy bands of the semiconductor. This voltage is referred to as the flat band voltage, V_{FB}.

$$V_{FB} = V_G(\psi_s = 0; Q_s = 0) \qquad 2.8$$

Substituting equation 2.7 into 2.8, V_{FB} becomes,

$$V_{FB} = \phi_{ms} - \frac{Q_i + Q_b}{C_i} \qquad 2.9$$

It is observable that V_{FB} is a measure of the charge present at the interface and in the dielectric. For real MIS structures, V_{FB} is not zero. As a result, the capacitance-voltage (C-V) curves are usually parallel-shifted along the voltage axis by a magnitude, ΔV_{FB}, corresponding to the additional voltage from the interface charges. For an ideal MIS structure, V_{FB} is zero.

2.3 Interface Trap States

The presence of trapped charges in the bulk of the insulator or at the semiconductor-insulator interface results in a stretching of the C-V curve along the voltage axis and a parallel shift to either the right or left of the ideal curve. The shift in

flat band voltage, ΔV_{FB} could be used to estimate the total trapped charge in the insulator, Q_{tot} [5].

$$Q_{tot} = C_{insulator} \Delta V_{FB} \qquad 2.10$$

Negative charge trapping in film results in positive $\Delta V_{FB,}$ while positive charge trapping yields negative ΔV_{FB}. The interface states are able to keep pace with low frequency variations of the gate bias (~ 1 – 1000Hz), but do not at very high frequencies (~ 1 MHz). As such, the interface traps contribute to the low frequency capacitance (C_{lf}), but not to the high frequency capacitance (C_{hf}). It is possible to calculate the density of interface (D_{it}) from the difference in capacitance between C_{lf} and C_{hf} at a particular gate bias [6] using the relation,

$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{lf}}{C_i - C_{lf}} - \frac{C_i C_{hf}}{C_i - C_{hf}} \right) \qquad 2.11$$

where q is the electronic charge. D_{it} ($cm^{-2}eV^{-1}$) can be measured for different gate biases in the depletion region. The draw-back in using the above capacitance method in estimating D_{it} lies in the difficulty in extracting the interface trap capacitance from the measured capacitance that comprises the insulator capacitance, the depletion-layer capacitance and the interface trap capacitance. It turns out that higher inaccuracies exist in the extraction of interface states information from the measured capacitance since the difference between two capacitances must be used. But, this is not the case in capacitance and conductance as functions of voltage and frequency measurements since both measurements contain similar information about the interface. As such, the conductance method is the preferred method of calculating D_{it} since the above difficulty

does not apply as the measured conductance is directly related to interface traps [7]. The conductance method proposed by Nichollian et al. [7] was employed in the calculation of interface state density (D_{it}) in this work.

Here, the interface traps change occupancy over a few *KT/q* wide centered about the Fermi level by interacting with the semiconductor bands via the emission and capture of carriers. A small ac signal applied to the gate of an MIS diode results in an alternate movement of the band edges toward or away from the Fermi level. Using the conductance technique, interface trap states are detected through the loss resulting from changes in their occupancy due to small variations in dc gate bias. Usually, a conductance peak is observed as a result of the ac (energy) loss due to capture and emission of carriers by these interface states.

An equivalent conductance, G_p can be used to represent the energy loss due to capture and emission of carriers in a MIS structure. At fixed bias, an increase in energy loss is usually observed with a gradual increase in frequency in the low frequency range, which is attributed to a response of interface states to the low frequency with time lag. However, the energy loss decreases with further increase in frequency since fewer traps are now able to respond. A maximum energy loss is observed when most of the interface traps respond; as such, a measure of G_p over a range of frequencies and gate biases in the depletion region results in a measure of D_{it} (Fig. 2.7).

Shown in Fig. 2.8 are schematics of the equivalent, simplified and measured circuits of a MIS structure with interface traps. In Fig. 2.8a, E_{it} is the energy loss due to interface traps, C_{it} is the capacitance due to the trapped charges, C_D is the depletion

capacitance which is in parallel with the series connection of C_{it} and E_{it}, while the insulator capacitance, C_i is in series with C_D, C_{it}, and E_{it}. Fig. 2.8b, which was derived from

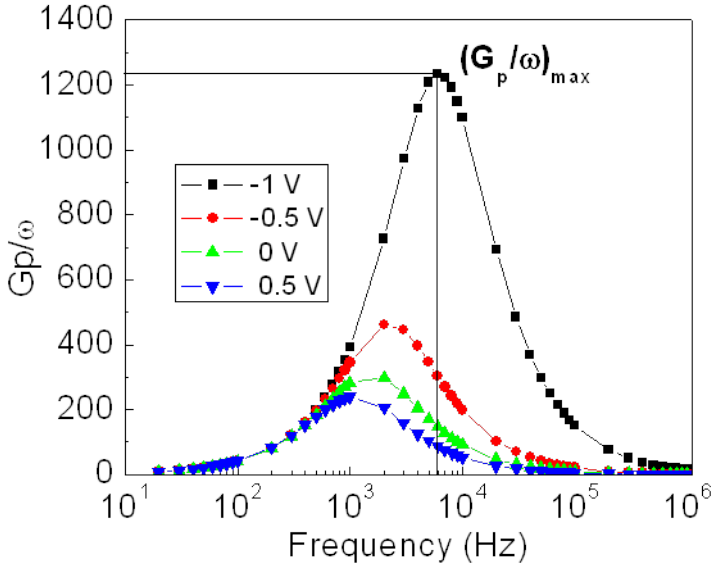

Fig. 2.7: Plot of G_p/ω as a function of log (f) for various gate biases in the depletion region.

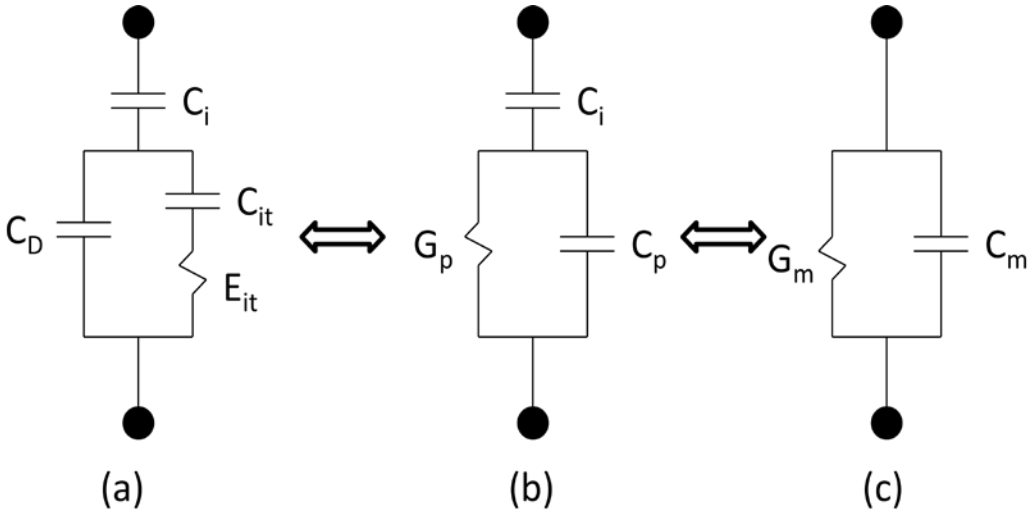

Fig. 2.8: Schematics of (a) equivalent (b) simplified and (c) measured circuits for MIS structures with interface traps.

2.8a is a parallel combination of the equivalent conductance, G_p and the equivalent capacitance, C_p. Fig. 2.8c contains the measured parallel conductance, G_m and capacitance, C_m obtainable via direct measurements on a MIS structure using an LCR meter. G_p is obtainable from the measured data using the relation,

$$\frac{G_p}{\omega} = \frac{\omega G_m C_i^2}{G_m^2 + \omega^2 (C_i - C_m)^2} \qquad 2.12$$

where ω=2πf is the radian frequency. G_p is estimated in the depletion region as a function of both gate bias and frequency.

Depending on the assumed energy distribution of the interface traps, either the single time constant (STC) or continuum of states model of the conductance method could be used to estimate D_{it}. For the STC model, the traps are assumed to behave as a single trap with a single energy level. Here, the admittance of the traps, Y_{it} is given by

$$Y_{it} = \frac{\omega^2 \tau C_{it}}{1 + \omega^2 \tau^2} + j \frac{\omega C_{it}}{1 + \omega^2 C^2} \qquad 2.13$$

where j is complex. In general,

$$Y_{it} = G_p + j\omega C_p \qquad 2.14$$

According to this model, G_p of a single level interface state is given by,

$$\frac{G_p}{\omega} = \frac{qD_{it}\omega\tau}{1 + \omega^2 \tau^2} \qquad 2.15$$

where $qD_{it} = C_{it}$ is the interface states capacitance, τ is the time constant of the interface state and G_p/ω has a maximum at $\omega\tau$=1. For the continuum of states model which was used in the calculation of D_{it} in this work, the interface traps are assumed to have

energy levels that are so closely spaced across the band gap and as such, could be treated as a continuum of states. The admittance of the continuum of states model is

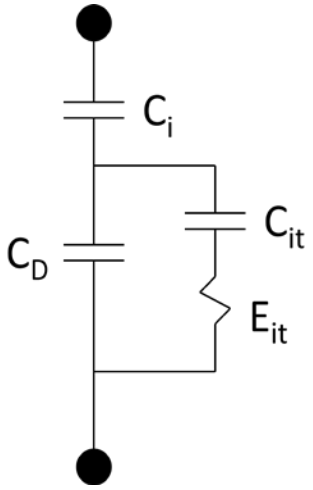

Fig. 2.9: Schematic of equivalent circuit for an STC model.

given by,

$$Y_{it} = \frac{C_{it}}{2\tau}\ln(1+\omega^2\tau^2) + j\frac{C_{it}}{\tau}\tan^{-1}(\omega\tau) \qquad 2.16$$

According to this model, G_p of a single level interface state is given by,

$$\frac{G_p}{\omega} = \frac{qD_{it}\ln(1+\omega^2\tau^2)}{2\omega\tau} \qquad 2.17$$

G_p/ω has a maximum at $\omega\tau$=1.98. From here, D_{it} can be calculated from the highest peak of G_p/ω versus log (f) plot as shown in Fig. 2.7 (obtained from Eq. 2.9), using the relation,

$$D_{it} = \frac{2.5}{qA}\left(\frac{G_p}{\omega}\right)_{\max} (cm^{-2}eV^{-1}) \qquad 2.18$$

where *A* is the area of the MIS capacitor.

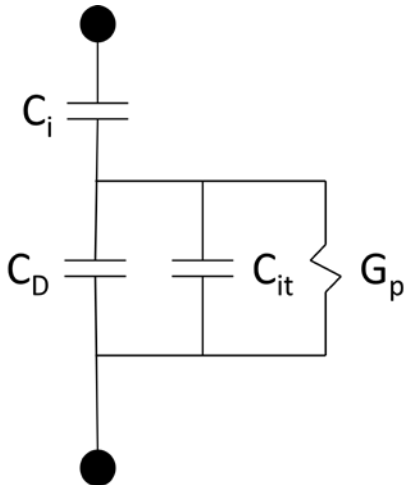

Fig. 2.10: Schematic of equivalent circuit for the continuum of states model.

2.4 OFET Electrical Characteristics

The OFET, unlike a regular inorganic FET works in the accumulation mode. Looking at a hole-transporting (p-type) OFET which was used in this work, application of a negative gate voltage induces positive charges at the grounded source electrode, which are consequently injected into the organic semiconductor. For an effective hole injection, these electrodes (source and drain) materials must have Fermi levels that match or are close enough to the highest occupied molecular orbital (HOMO) of the organic semiconductor. This means that the hole injection barrier (Δ) between the Fermi level of the metal and HOMO level of the organic semiconductor must be as low as possible (Fig. 2.11). These accumulated positive charges form a conducting channel at the organic semiconductor-insulator interface and can be made to move along the channel and collect at the drain by an application of a negative voltage at the drain electrode. No current can flow from source to drain if the gate-source voltage (V_{GS}) is lower than the threshold voltage (V_T) ($V_{GS} < V_T$), since there is no mobile charge at the

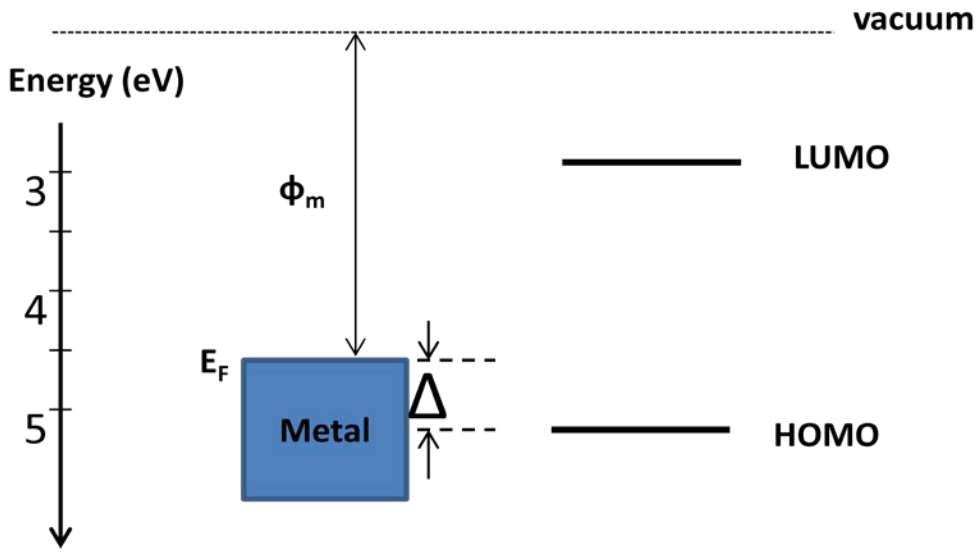

Fig. 2.11: Energy band diagram alignment at a metal-organic semiconductor interface.

surface of the semiconductor. In the linear regime of the transistor (Fig. 2.12b) in which the current flowing through the channel is directly proportional to the drain-source voltage (V_{DS}), for low V_{DS} ($V_{DS} << V_{GS}$), the drain-source current (I_{DS}) is related to V_{DS} by

$$I_{DS(lin)} = \frac{WC_i}{L}\mu\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS} \qquad 2.19$$

where V_T is the threshold voltage, C_i is the dielectric capacitance per unit area and μ is the field-effect mobility. The threshold voltage refers to the value of V_{GS} required to induce the inversion layer in an inorganic transistor or accumulation layer in an organic transistor (onset of transistor conduction).

For high V_{GS} ($V_{GS} > V_T$), conduction is established if there is a potential (V_{DS}) between the drain and the source. As V_{Ds} increases from source to drain, a

point P, ($V_{DS} = V_{GS} - V_T$) is reached at which the channel is "pinched-off" as

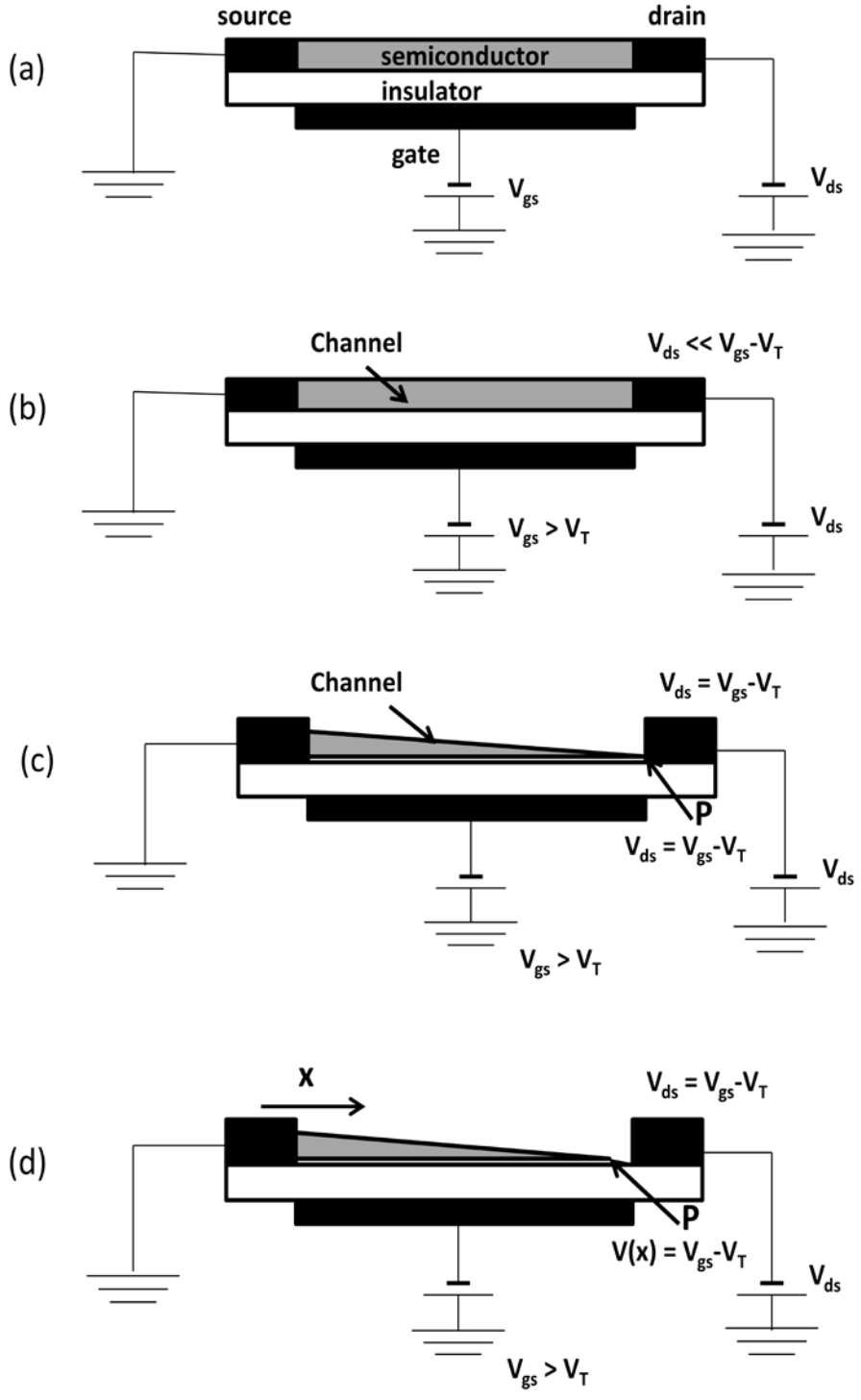

Fig. 2.12: (a) Schematic of an organic field-effect transistor. Illustrations of (b) linear (c) start of saturation and (d) saturation regimes of organic field-effect transistors.

shown in Fig. 2.12c. Due to the difference between the local potential V(x) and V_{GS} which is now below V_T, a depletion region develops next to the drain. Carriers pulled into the drain by the strong electric field that exists within the narrow depletion region between the drain and the pinch-off point, give rise to a space-charge-limited saturation current, $I_{DS(sat)}$. Further increase in V_{DS} will not result in an increase in current beyond the value it reached before the onset of the ''pinch-off''; rather, it gives rise to an expansion of the depletion region and a reduction of the channel (Fig. 2.12d). This is the referred to as the saturation regime of the transistor. It is observable that the saturation current must be proportional to $(V_{GS} – V_T)^2$ considering that the "pinch-off" potential ($V_{DS} = V_{GS} – V_T$) is the potential difference that drives the current through the conducting part of the channel, and the conductance of the channel itself is directly proportional to the density of mobile charge at the source-end of the channel. Therefore,

$$I_{DS(sat)} = \frac{WC_i}{2L}\mu\left(V_{GS} - V_T\right)^2 \qquad 2.20$$

The OFET transfer characteristic plots the output drain current as a function of the input gate bias for a fixed drain bias. For the transfer characteristics in the saturation region, the square root of I_{DS} is plotted as a function of V_{GS}, with the threshold voltage as the intercept. Similarly, the slope of the transfer characteristics can be used to determine value of the saturation field-effect mobility, $\mu_{(sat)}$ in the saturation regime using the relation,

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad 2.21$$

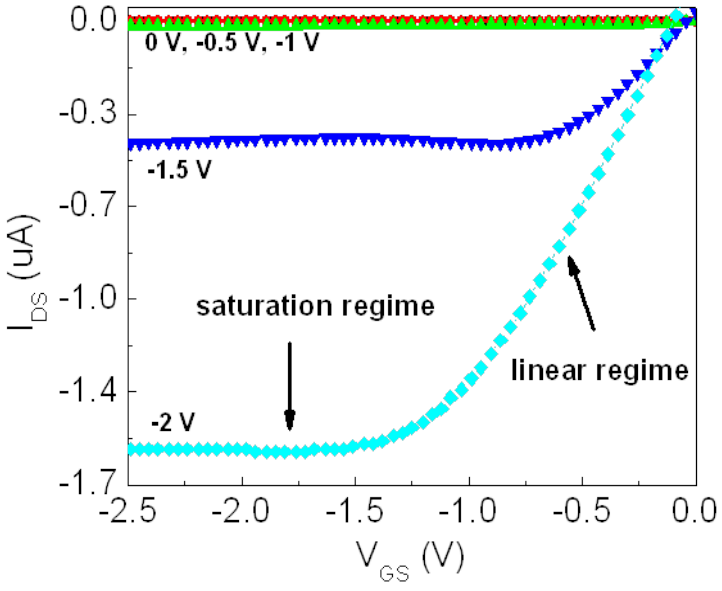

Figure 2.13: Output characteristics for a typical OFET indicating the linear and saturation regimes.

The on/off current ratio and subthreshold slope (SS) are extractable from a plot of $I_{D(sat)}$ on a logarithmic scale as a function of V_{GS} as shown in Fig. 2.14. Eq. 2.20 suggests that the current abruptly becomes zero as soon at the as V_{GS} equals V_T. In practice, this is not the case as there is still some drain conduction below threshold (Fig. 2.14) referred to as subthreshold conduction. This subthreshold current may be due to weak accumulation in the channel between flat band and threshold which may result in a diffusion current between source and drain. Usually, a plot of log (I_{DS}) as a function of V_{GS} exhibits a linear behavior in the subthreshold regime (marked SS in Fig. 2.14) and the reciprocal of the slope of this line is known as the subthreshold slope (SS). For state-of-the art MOSFETs, SS has a typical value of ~ 70 mV/decade at room temperature [6]. A smaller

value of SS implies that a small change in input bias considerably modulates the output current.

$$SS = \frac{dV_{GS}}{d(\log I_{DS})} = 2.3\frac{KT}{q}\left[1+\frac{C_D + C_{it}}{C_i}\right] \qquad 2.22$$

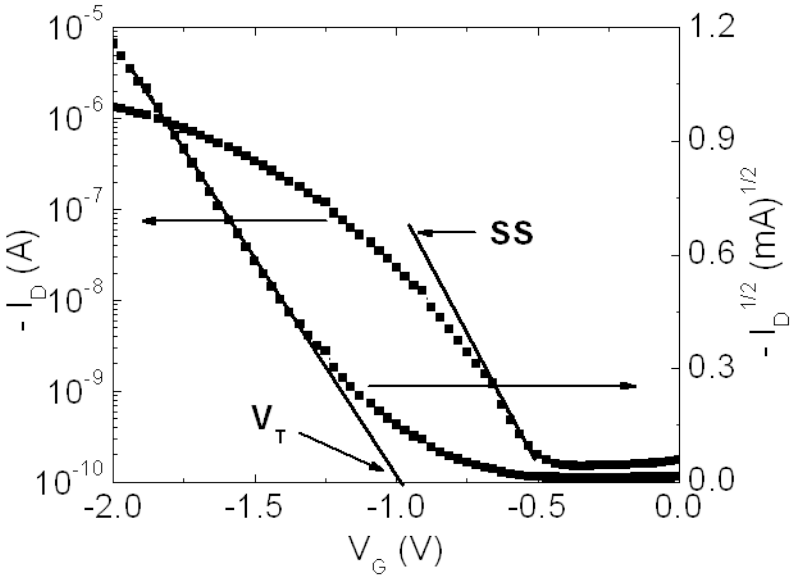

Figure 2.14: Transfer characteristics for a typical OFET indicating V_T and SS.

2.5 Organic Materials

2.5.1 Polymer Dielectrics

Poly(methyl methacrylate) (PMMA) is an example of a polymer dielectric and was used in this study. Because it is a polymer dielectric, it is solution-processable. PMMA is a hard, rigid, hydrophobic, less-polar, and brittle polymer dielectric. It is one of the most common polymer dielectric materials. PMMA is a linear amorphous polymeric thermoplastic with high transparency and surface gloss [8]. It is highly resistive to oxidation and photodegradation [9], and stable to sunlight [10]. PMMA is also easily

Table 2.1: Various solvents used in this work and their properties.

Solvent	Dipole moment	Dielectric constant	Solubility parameter $(MPa)^{1/2}$
Butyl acetate	1.84	5.01	17.4
Toluene	0.375	2.38	18.2
Anisole	0.994	4.33	19.5
Propylene carbonate	4.90	64.90	27.2
Dimethyl suloxide	3.96	47.20	26.6

preparable and available. Its monomer, methyl methacrylate (MMA) is synthesized by heating acetone cyanohydrins with sulfuric acid to form methacrylamide sulfate, which is then reacted with water and methanol to yield methyl methacrylate [9]. PMMA has a

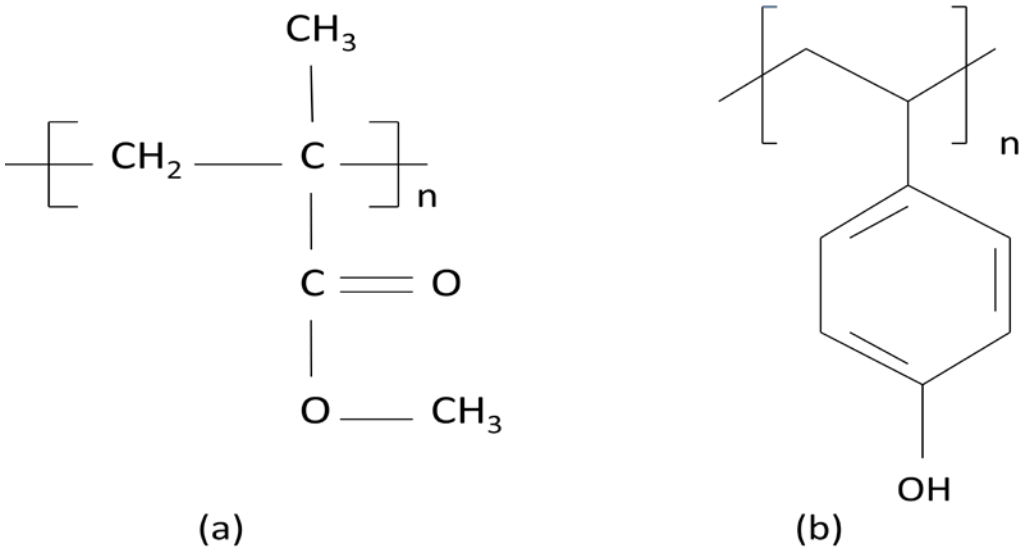

Fig. 2.15: Molecular structures of (a) PMMA and (b) PVP.

dielectric constant that ranges from about 3.5 (at 5 kHz) to 2.6 (at 1 MHz). In this work, PMMA (Mw = 996,000 g/mol.) obtained from Sigma-Aldrich was used as the gate dielectric layer in our OFETs and diodes. Another polymer dielectric that was used in this work is poly (4-vinyl-phenol) (PVP). Unlike PMMA, PVP is a hydrophilic polymer dielectric with a dielectric constant that ranges between 4.0 and 5.2. Table 2.1 contains the various solvents used in this work and their respective properties.

2.5.2 Organic semiconductors

Pentacene is an aromatic hydrocarbon and one of the most promising and extensively studied organic small molecule semiconductors with quite high carrier mobility. Small molecule semiconductors are usually evaporated. Pentacene is a planar molecule with five linearly-fused benzene rings with herringbone packing of two molecules per unit cell resulting in a triclinic crystal structure. It could be thermally evaporated under both high and low vacuum pressures. During evaporation, pentacene film formation begins with an adsorption and subsequent diffusion of the sublimated pentacene molecules on a substrate, which proceeds to a two-dimensional (2D) island at some critical film quantity. The growth finally changes to three-dimensional (3D) growth with the deposition of about one or some monolayer of films. In this work, pentacene (obtained from Tokyo Chemical Industrial Co. Ltd) was used as the

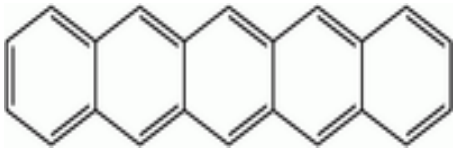

Fig. 2.16: Molecular structure of pentacene.

semiconductor in some of our OFETs and MIS diodes.

9,9-dioctylfluorene-co-bis-N-N-(4-butylphenyl)-bis-N,N-phenyl 1,4-phenylenediamine (PFB) is a polymer semiconductor and was used in this work. It belongs to the family of polyfluorenes (PFs). PFB, just like all polymer semiconductors is solution-processable. PFs are polymers that emit light via electroluminescence; as such, are promising materials for optoelectronic device applications, especially light-emitting diodes (LEDs) considering their electroactive, photoactive, and excellent electro-optical characteristics. PFs have the fluorene unit as their building blocks. Polyfluorenes have high thermal stability and can emit light across the entire visible spectrum [11]. In this study, PFB (obtained from American Dye Source) was used as the semiconductor in some of our OFETs and diodes. Our choice of PFB here was mainly due to the very close matching of its HOMO level with the Fermi level of the gold source and drain contacts.

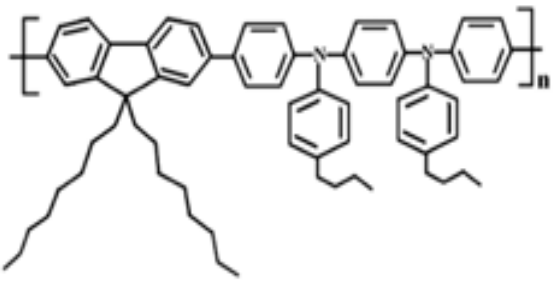

Fig. 2.17: Molecular structure of PFB.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 Film Deposition

3.1.1 Spincoating

Spincoating is a technique that is typically employed in the deposition of polymeric thin films onto substrates (flexible and non-flexible). The procedure could be summarized thus: (a) an amount of a solution (material to be deposited) is dispensed on the substrate either before substrate rotation or while the substrate is slowly rotating (b) the substrate is rotated at a pre-set speed which is usually a few thousand rotations per minute (rpm), and (c) the solution spreads outwards with a resultant thin film formation. The process completes with baking/curing in an oven – a process aimed at evaporating the solvent out of the film. The spincoating process could be modeled thus [12]:

$$d = \left(\frac{\eta}{4\pi \ell \omega^2} \right)^{1/2} \left(\frac{1}{t} \right)^{1/2} \qquad 3.1$$

where d is the thickness of the spincoated film, η is the coefficient of viscosity of the solution, ℓ is the density of the solution, ω is the angular frequency of the spin, and t is spin time.

3.1.2 Matrix-assisted pulsed-laser evaporation (MAPLE)

MAPLE is a derivative of pulsed laser deposition (PLD), which is a deposition technique whereby a pulsed laser beam focused down by a lens hits a target of the desired material and creates a plume of the material perpendicular to the target surface. Typical lasers employed include ArF, KrF excimer lasers, and Nd:YAG laser. The main difference between MAPLE and PLD is in the original forms of the targets. While the PLD target is always solid, the MAPLE target is originally a liquid solution but turned into a solid via freezing. The MAPLE set-up used in our work has a KrF excimer laser source (Lambda Physik COMPex) and a vacuum system that can attain pressures up to 10^{-5} mbar with the aid of roughing and turbo pumps. The vacuum deposition system (Fig. 3.1) comprises a deposition chamber, target carousel with target holders, a variable temperature substrate holder, and many standard ports such as pumping ports, gas inlet, pressure gauge, and view ports. Different parts are indicated in Fig. 3.2: the laser port, L; the target port flange-to-beam focal plane distance, Z; the target to substrate distance, S, and the substrate-to-flange distance, T. The target-to-substrate distance is usually about 5–15 cm. MAPLE involves a complex physical process of the interaction of high-power pulsed irradiation on a frozen target with the laser beam, the formation of plasma plume, and the transfer of the ablated material through the plasma plume onto

the substrate surface. Hence, MAPLE deposition of polymer thin films could be broken down into four different steps:

(a) Interaction of the laser radiation with the target

(b) Ablation materials dynamics

(c) Deposition of the ablated materials onto the substrate

(d) Thin film growth and nucleation on the substrate surface

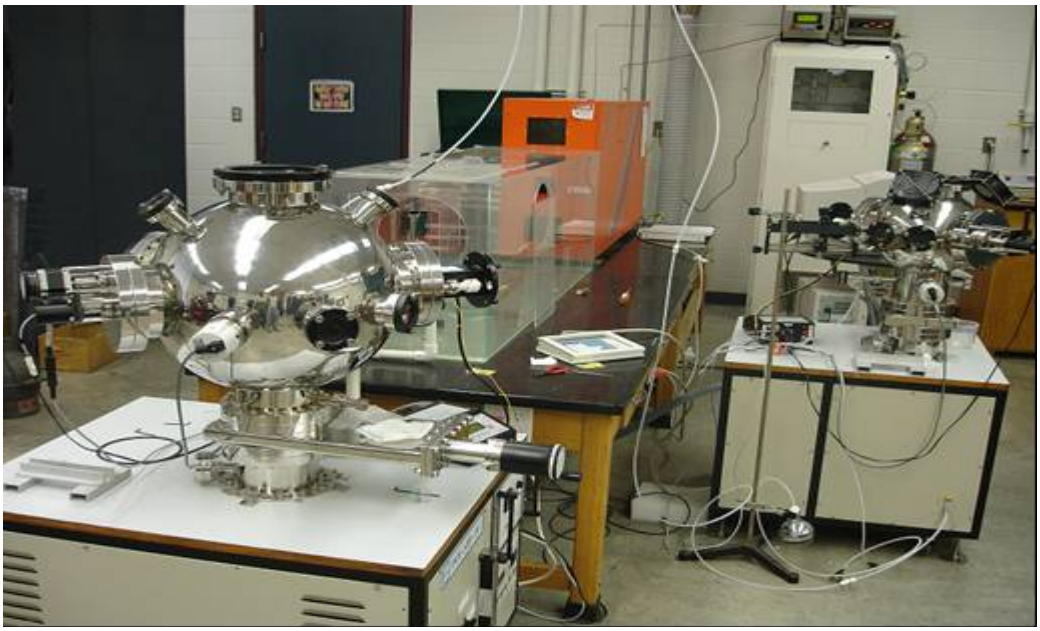

Fig. 3.1: The MAPLE system at Missouri State University in Springfield, Missouri.

The first step involves a focusing of the laser beam onto the surface of the target, and subsequent stoichiometric dissociation and ablation of the target material from the target surface. Various complex physical phenomena such as collisions, heating, electronic excitation etc, accompany the ablation process.

The second step involves a movement of the dissociated materials from the target towards the substrate as governed by the laws of gas-dynamics. Here, the

majority of the laser intensity is initially absorbed by the solvent molecules (toluene) which cause them to vaporize. Then the kinetic energy of the solvent molecules is transferred to the solute through collective collisions, causing the polymer to evaporate and deposit on the substrate. All polymer films were deposited at room temperature. The films were deposited for ~ 30 min with the growth rate of ~ 0.6 nm/min. During the deposition, the target was kept frozen by passing liquid nitrogen externally through a tube which goes into the target holder. The uniformity of the deposited film on the substrate is affected by the spot size of the laser and the plasma temperature. Also the angular spread of the ablated materials depends on the target-to-substrate distance.

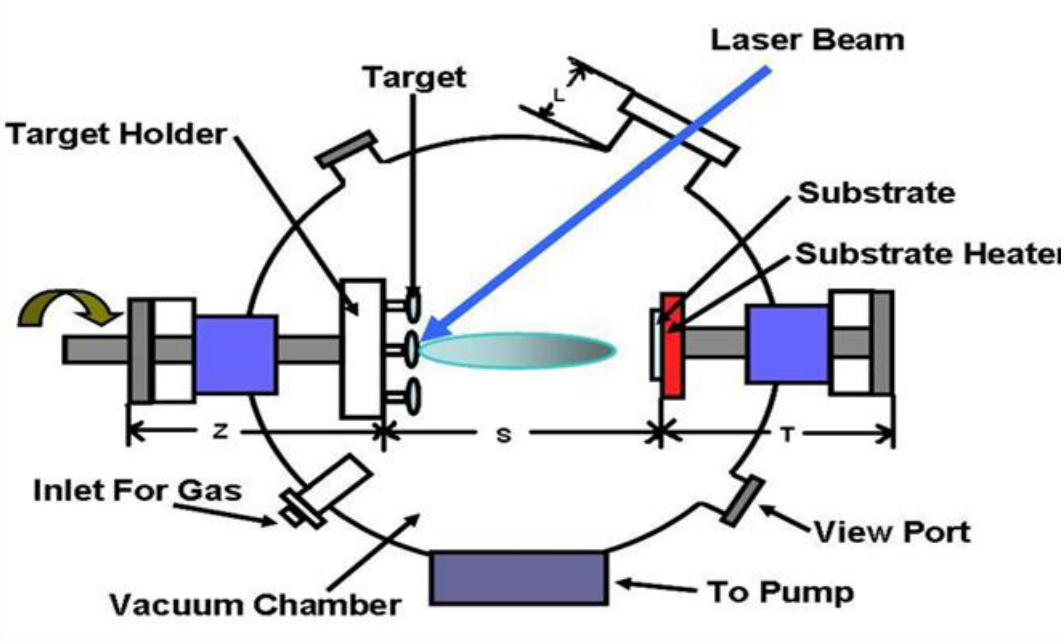

Figure 3.2: Schematic diagram of the MAPLE system.

In the third step, the emitted high-energy species impinge on the substrate surface. This step is critical in determining the quality of the film. Here, some of the surface atoms are sputtered by the energetic species, and this leads to the formation of

a collision region between the incident flow and sputtered atoms; films grow only on the formation of a thermalized region.

The growth and nucleation step is a critical step which depends on such factors as the energy of the laser, density, and ionization degree, as well as physical and chemical properties of the substrate. The growth of the film is dependent on the surface mobility of the adatom, which diffuses through several atomic distances before settling at a stable position within the film. The nucleation process depends on the interfacial energies between the substrate, condensing material, and vapor.

3.1.3 Thermal evaporation

At high enough temperatures, a solid can vaporize whereby the molecules of the solid are detached from the solid. This process is harnessed for deposition of thin films on substrates. The process could be summarized thus: (a) heating of solid causes an escape of molecules from the solid (b) the removed molecules travel over some distance in the vacuum from the source to the substrate (c) the molecules deposit on the susbtrate resulting in thin film growth. According to kinetic theory [13], the mean free path of gas atoms (λ) is given by

$$\lambda = \frac{k_B T}{P \pi d^2 \sqrt{2}} \quad , \qquad 3.2$$

where d is the diameter of the molecules, T is temperature, P is pressure, and k_B is Boltzmann's constant. From the above relation, it becomes necessary to evaporate at low pressures in order to ensure that the depositing species travel from source to substrate with minimal impurity collisions. It is desirable to ensure that λ exceeds the

source-to-substrate distance. Also from the Langmuir relation [13], the rate of evaporation, *Γ* from a surface is given by

$$\Gamma = P\left(\frac{M}{2\pi RT}\right)^{1/2}, \qquad 3.3$$

where *P* is the vapor pressure of the material at temperature *T*, *R* is the gas constant,

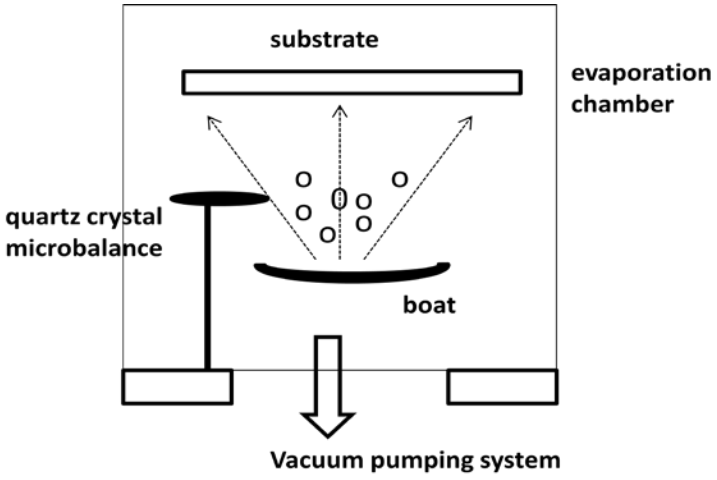

Fig. 3.3: Schematic of thermal evaporating system.

and *M* is the molecular weight. There are usually collisions between the traveling molecules and impurity gases in the evaporation chamber. Critical considerations for thin film growth using thermal evaporation include the deposition rate as well as the substrate temperature during deposition. A typical thermal evaporation system comprises evaporation chamber, a vacuum pumping system, a crucible boat (that holds the Joule heated source material), and a quartz crystal balance (for measurement of film thickness).

3.2 Experimental details

3.2.1 Device structures and fabrication

The device fabrication process begins with the ultrasonic cleaning of our 1" x 1" cut glass substrates with distilled water, acetone and alcohol, respectively. This is immediately followed by air drying of the glass substrates. Shown in Fig. 3.4 (a) and (b) are the configurations for our OFETs and MIS diodes, respectively. The structures are of bottom-gate configuration. And as the name implies, the aluminum gate electrode was first

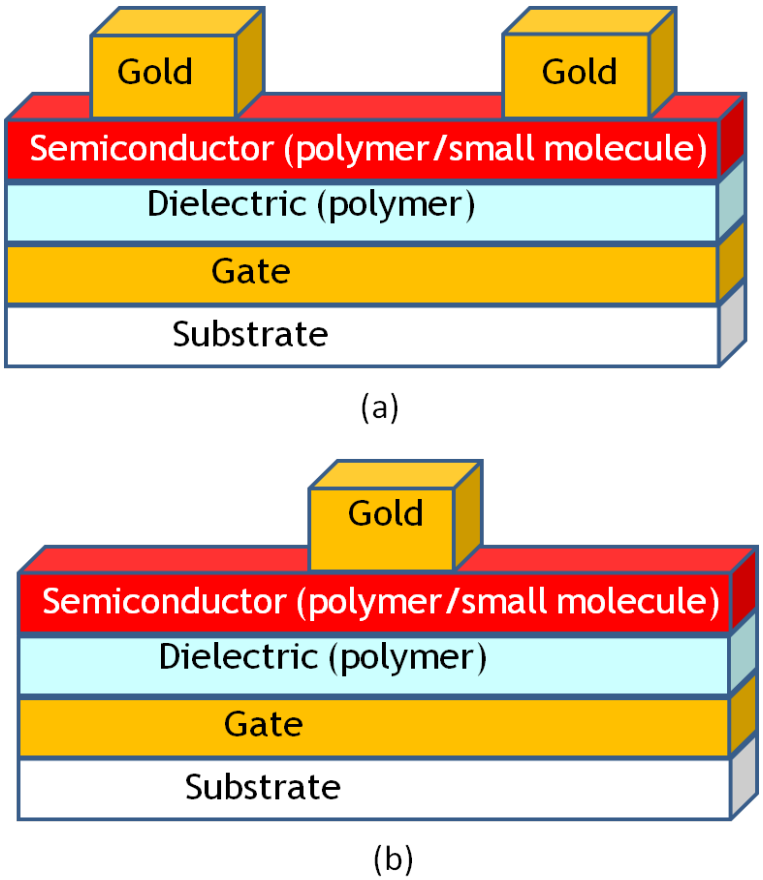

Fig. 3.4: Schematic representations of our (a) OFET and (b) MIS diode structures.

deposited on the glass substrate, which is followed by the deposition of the dielectric and semiconductor layers, respectively. The structures were then completed with the

deposition of the source and drain contacts (for the OFET) and top metal contact (for the MIS diode) onto the semiconductor layer. For the OFETs, the source and drain contacts must be in direct contact with the semiconductor so as to achieve good carrier injection, while the gate is separated from the semiconductor by the dielectric layer.

In this work, aluminum gate was deposited on cleaned and dried glass substrates by evaporation at room temperature using an MBraun thermal evaporation system located in a glove box. The pressure inside the evaporation chamber was initially pumped down to about 10^{-2} mbar using a roughing pump, and afterwards to pressures of 10^{-5} to 10^{-6} mbar with the aid of the turbo pump. This automated thermal evaporation system is controlled by an SQC-222 co deposition controller. The evaporation source materials were Al pellets (99.9 % purity) held in a tungsten boat, while the glass substrates were screwed down on a custom-built metallic plate fitted in the substrate holder. The Al gate layer with a thickness of about 60 nm was evaporated at a rate of ~ 3 Å/s. The film thickness and deposition rate were monitored via the SQC-222 co deposition controller which is connected to a quartz crystal microbalance.

The aluminum gate deposition process was followed by spincoating of polymer dielectrics. PMMA and PVP dielectrics were used. The thickness of a spincoated film is mostly dependent on the concentration of the solution and spin speed. Here, we used an 8” desk-top precision spincoating system (Model P-6708D), located in a glove box (right box of Fig. 3.4). The solution was dropped on the Al-coated substrate before spinning at an initial low spin speed of about 500 r.p.m. The spin speed was increased afterwards to about 2000 – 5000 r.p.m in order to achieve the desired film thicknesses.

For the MAPLE project, 8 wt% of PMMA (996,000 g/mol) purchased from Sigma-Aldrich and dissolved in three different solvents: butylacetate, toluene, and anisole, were spincoated onto cleaned Al-coated glass substrates at 2000 r.p.m for 60 s, resulting in film thicknesses of between 500 and 550 nm as measured using a reflectometer. Thereafter, the samples were baked at 100 °C for 1 h in order to achieve solvents evaporation.

Fig. 3.5: MBraun glove box system with thermal evaporator in box 1 (left).

For the PMMA-pentacene project, again, 8 wt% of PMMA (996,000 g/mol) purchased from Sigma-Aldrich and dissolved in two different solvents: propylene carbonate (PC) and butylacetate (BTAc), were spincoated onto cleaned Al-coated glass substrates at 5000 r.p.m for 60 s, resulting in film thicknesses of ~ 70 nm and ~ 350 nm for PMMA-PC and PMMA-BTAc films, respectively. The films were then baked at 100 °C for 1 h in order to achieve solvents evaporation. For the PVP-pentacene project, 8 wt%

of pristine PVP (25,000 g/mol) and PVP cross-linked with poly (melamine-co-formaldehyde) methylated, purchased from Sigma-Aldrich and dissolved in propylene carbonate were spincoated onto cleaned Al-coated glass substrates at 5000 r.p.m for 60 s. The resulting film thicknesses were ~ 80 nm and ~ 30 nm, respectively. The films were then baked at 100 °C for 1 h in order to achieve solvents evaporation.

Next was the deposition of the semiconducting layers. For the MAPLE project, the polymer semiconductor – PFB was deposited on the PMMA dielectric layers using earlier discussed MAPLE technique. While for the PMMA and PVP-pentacene projects, an organic small molecule semiconductor – pentacene was thermally evaporated on the polymer dielectric layers at room temperature using an MBraun thermal evaporation system located in a glove box. The evaporation source material was pentacene purchased from Tokyo Chemical Industrial Co. Ltd., which was held in a quartz crucible, while the PMMA and PVP-covered substrates were screwed down on a custom-built metallic plate fitted in the substrate holder. The pentacene film layer with a thickness of about 60 nm was evaporated at a rate of ~ 0.3 Å/s. The film thickness and deposition rate were monitored via the SQC-222 co deposition controller which is connected to a quartz crystal microbalance.

Our device structures were completed with the room temperature evaporation of the source and drain gold contacts for the OFETs and top gold contact for the MIS capacitors onto the semiconductor layers. This was done using the MBraun thermal evaporation system located in a glove box. The evaporation source materials were gold wires purchased from Kurt J. Lesker (99.9 % pure), which were held in a tungsten boat,

while the semiconductor-covered substrates were screwed down on a custom-built metallic plate fitted in the substrate holder. The gold contacts with thicknesses of about 40 nm were evaporated at a rate of ~ 3 Å/s. The film thicknesses and deposition rate were monitored via the SQC-222 co deposition controller which is connected to a quartz crystal microbalance. The gold source and drain electrodes, which define a channel length (*L*) of 0.05–0.10 mm and channel width (*W*) 0.50–1.00 mm for the FETs, and top gold contacts for MIS diodes, were deposited though metallic shadow masks. The device area for MIS structures, determined by a scanning electron microscope, varied between $2–8 \times 10^{-3}$ cm^2.

Finally, for the MAPLE project, each of our devices contains both FET and MIS diode with Al/PMMA/PFB/Au structure and is named according to the solvent used to dissolve PMMA: butylacetate (Sample A), toluene (Sample B), and anisole (Sample C).

For the PMMA-pentacene project, each of our devices contains both FET and MIS diode with Al/PMMA/Pentacene/Au structure and is named according to the solvent used to dissolve PMMA: devices fabricated with PMMA using butyl acetate (BTAc) as the solvent are denoted as PMMA-BTAc while OFETs/MIS structures cast from PC are simply denoted as PMMA-PC. Also for the PVP-pentacene project, each of our devices contains both FET and MIS diode.

3.3 Device characterizations

3.3.1 Atomic force microscopy

Atomic force microscopy (AFM) is a highly sensitive method which mechanically gives information about surface morphology with atomic scale resolution. The basic idea

is to let a sharp tip scan the surface of the sample. A small force applied to the tip moves the tip across the surface resulting in a variation in force between the tip and the surface atoms. The tip is mounted on a cantilever and the force causes it to deflect. The deflection is usually measured by a laser beam which is reflected in different angles depending on the degree of deflection. The actual force can then be calculated using Hooke's law, F = - kz; where F is the force, k is the cantilever spring constant and z is the displacement of the cantilever [14]. A piezoelectric system is used to move the tip

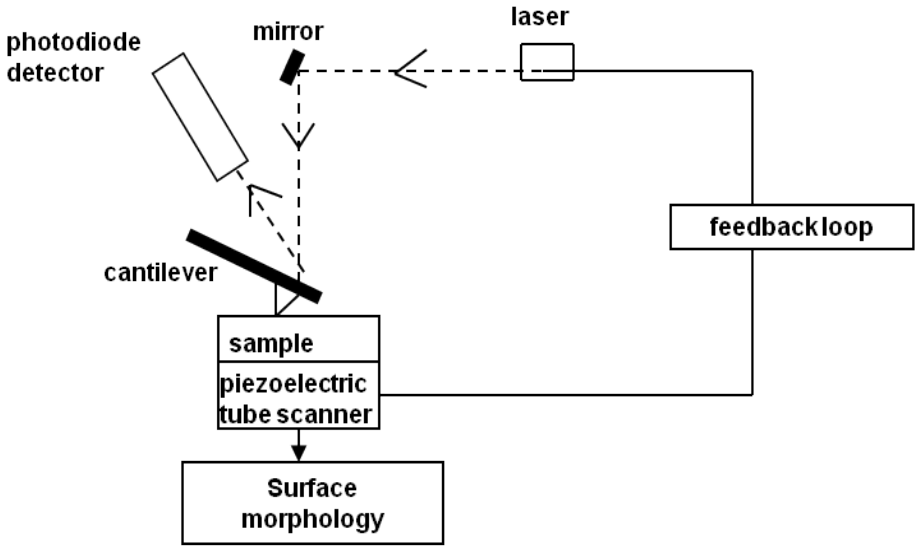

Fig. 3.6: Schematic representation of the working principle of the atomic force microscope.

across the surface with high precision. The AFM has three different modes of operation: contact mode, non-contact mode and tapping mode [14]. Cypher scanning probe AFM used in the tapping mode was employed in this work. As the name implies, the tip taps the surface. The tip is set in motion, oscillates at or close to the resonance frequency and moves with an amplitude typically > 20 nm. Starting away from the surface, the tip

is slowly brought in contact with the surface, tapping the surface atoms. An energy loss to the surface atoms and a decrease in amplitude occur due to the tapping. A feedback loop keeps the amplitude and force, constant by adjusting the separation during movement.

3.3.2 MIS capacitance-voltage measurement

The charges inside the dielectric and at the interfaces of a MIS structure can be measured by measuring the capacitance as a function of voltage (C-V). During the measurement, an ac signal with small amplitude of usually between 10 – 15 mV is superimposed on a dc voltage that is swept from the negative to the positive. While the ac signal is required to measure the capacitance, the dc voltage determines the bias condition. An inductance-capacitance-resistance (LCR) HP 4284A meter was utilized for the C-V measurements. It provides a dc voltage of ± 40 V and an ac frequency of 20 Hz to 1 MHz. Most of our measurements were performed at low frequencies (1 kHz – 10 kHz) with a 100 mV ac signal at a scan rate of 0.05 V/s. A sketch of a C-V measurement set-up is shown in Fig. 3.8.

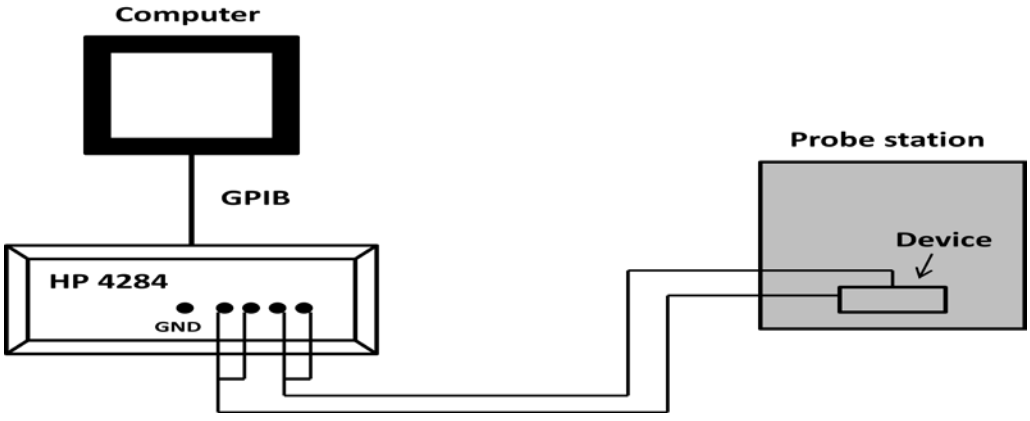

Fig. 3.7: A sketch of a C-V measurement set-up.

3.3.3 OFET current-voltage measurement

The current-voltage (I-V) characteristics of our OFETs were carried out under ambient conditions using the Keithley 2400 and 236 source/measure units. This is usually a three-probe measurement. For a measurement of the OFET output characteristics, a set dc voltage was applied to the gate via the 2400 source meter, while the 236 source/measure unit was used to simultaneously sweep the drain-source voltage (V_{DS}) and measure the drain current (I_D). The measurement was repeated with several gate voltages. For measurement of the transfer characteristics, a sweeping dc voltage was applied to the gate via the 2400 source meter, while the 236 source/measure unit was used to supply set V_{DS} and measure I_D as well. A two-probe measurement set-up making use of only the 236 source/measure unit was used for measuring the gate leakage current of the dielectric layer. A sketch of I-V measurement set-up for an OFET is shown in Fig. 3.9.

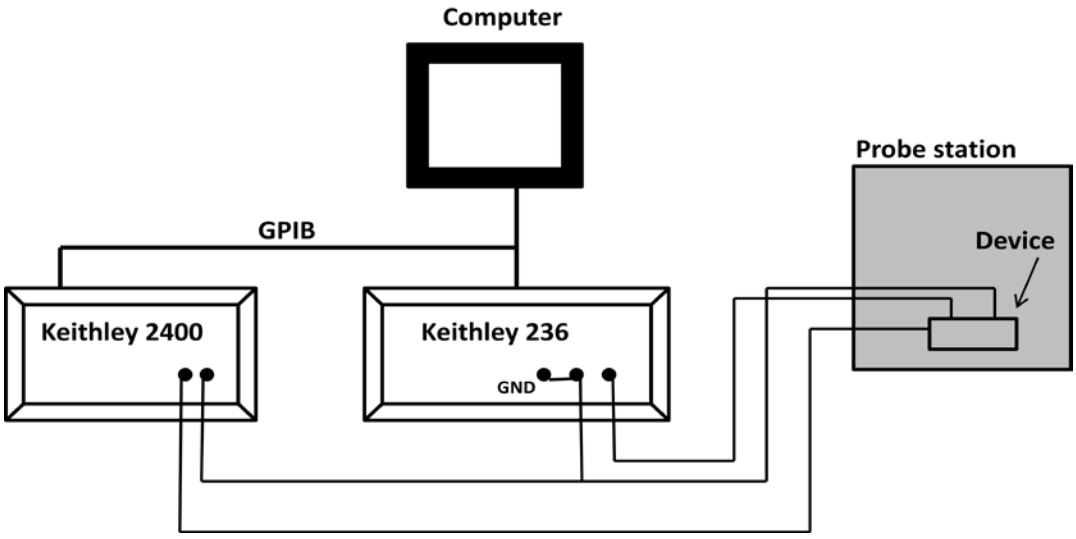

Fig. 3.8: A sketch of OFET I-V measurement set-up.

CHAPTER 4

MAPLE PFB FILMS FOR ORGANIC FIELD-EFFECT-TRANSISTORS AND METAL-INSULATOR-SEMICONDUCTOR CAPACITORS WITH POLY (METHYL METHACRYLATE) GATE DIELECTRIC

4.1 Introduction

Lately, considerable research efforts have been directed at organic semiconductors and dielectrics and their applications in organic field-effect transistors and diodes owing largely to their low cost solution processable fabrication. Organic devices can be fabricated by spincoating and other cost effective procedures such as inkjet printing. Active matrix displays based on organic thin film transistors and integrated circuits realized via inkjet printing have been reported [15- 19]. There exist ample reports where polymer dielectrics with varying dielectric constant have been used with small molecule semiconductors such as pentacene and rubrene [20,21] and high/low-k inorganic insulators such as SiO_2 and Al_2O_3 have also been used with solution processable conjugated polymers [21,22]. Among polymer semiconductors, poly (3-hexylthiophene) (P3HT), when used with SiO_2 as the dielectric has been shown to yield carrier mobility as high as 0.2 $cm^2 V^{-1} s^{-1}$ [23]. Nevertheless polymeric dielectric materials are preferred to their inorganic counterparts due to their numerous advantages: easily

processable, low cost, flexible, and hydrophobic. Unfortunately, the fabrication of polymer thin film transistors and diodes in which both the semiconductor and the dielectric layer are solution processable polymers has been limited. This limitation is due to the inherent fabrication problem whereby an underlying dielectric layer can be damaged by spincoating the overlying semiconducting layer, in the case of bottom-gate architecture or where an underlying semiconducting layer can be damaged by spincoating the overlying dielectric layer, in the case of top-gate device architecture.

Sun *et al.* [24] have reported baking their PMMA dielectric film at a high temperature of 220 °C for 30 min in nitrogen gas environment in order to make the film resistant to swelling and dissolution by trichlorobenzene (TCB) used to dissolve the overlying semiconducting layer. They observed that for PMMA films baked at lower temperatures, spincoating with TCB resulted in changes in film color and increase in surface roughness. Also the difficulty in finding an orthogonal and stable solvent that does not dissolve the underlying semiconducting film when spincoated has been identified as one of the obstacles in applying crosslinkable polymer thin gate dielectrics in top-gate transistor architectures [25]. The use of solution processable semiconductor with divinyl-tetramethylsiloxane-bis(bisbenzocyclobutene) derivative (BCB), as a solution processable dielectric has been reported [26,27], but it turns out that BCB requires a very high curing temperature (250 °C), which is difficult to handle at times.

This work introduces matrix-assisted pulsed-laser evaporation (MAPLE), a derivative of pulsed laser deposition (PLD), as an alternative fabrication technique that circumvents the inherent solvent selectivity problem encountered in the fabrication of

organic field-effect transistors (OFET) and metal-insulator-semiconductor (MIS) diodes via spincoating. Besides offering the advantage of good layer-by-layer film control, remarkable features of this technique are its solvent non-selectivity and its ability to not cause the swelling and dissolution of polymer dielectrics and semiconductors, common inherent problems associated with spincoating. Here, an organic semiconducting material, 9,9-dioctylfluorene-co-bis-N-N-(4-butylphenyl)-bis-N,N-phenyl 1,4-phenylenediamine (PFB) was dissolved in a toluene solvent and frozen at liquid nitrogen temperatures. Then the frozen target is irradiated by a pulsed laser beam (e.g. KrF excimer laser), whose energy is absorbed by the toluene and is pumped away, thereby leaving the PFB molecules to be gently evaporated and deposited without causing any swelling or dissolution of the PMMA film on the substrate. Our prior studies of MAPLE deposited polyfluorene films show that the optical and structural properties of the films remain unchanged comparable to spincoated films [28].

4.2 Results and Discussion

4.2.1 Dielectric Film: Morphology and Electrical Characteristics

The surface morphology of the films resulting from dissolving PMMA in butylacetate, toluene, and anisole, obtained by means of AFM (Cypher scanning probe microscope) in tapping mode are shown in Fig. 4.1. The films exhibited very smooth surfaces with root-mean-square values of 2.18 Å, 2.35 Å, and 2.55 Å for butylacetate, toluene, and anisole, respectively. Parallel plate capacitor structures (Al/PMMA/Al) were fabricated to investigate the dielectric properties of PMMA. The leakage current density of the films is in the low 10^{-8} A cm^{-2} for applied fields of up to 1.4 MV cm^{-1} (Fig.

4.2) and measurements of the dielectric constant of PMMA dissolved in the different solvents revealed a decrease of the observed dielectric constant from approximately 3.50 at 5 kHz to 2.81 at 1 MHz. This range of values is in good agreement with other published reports [29,30].

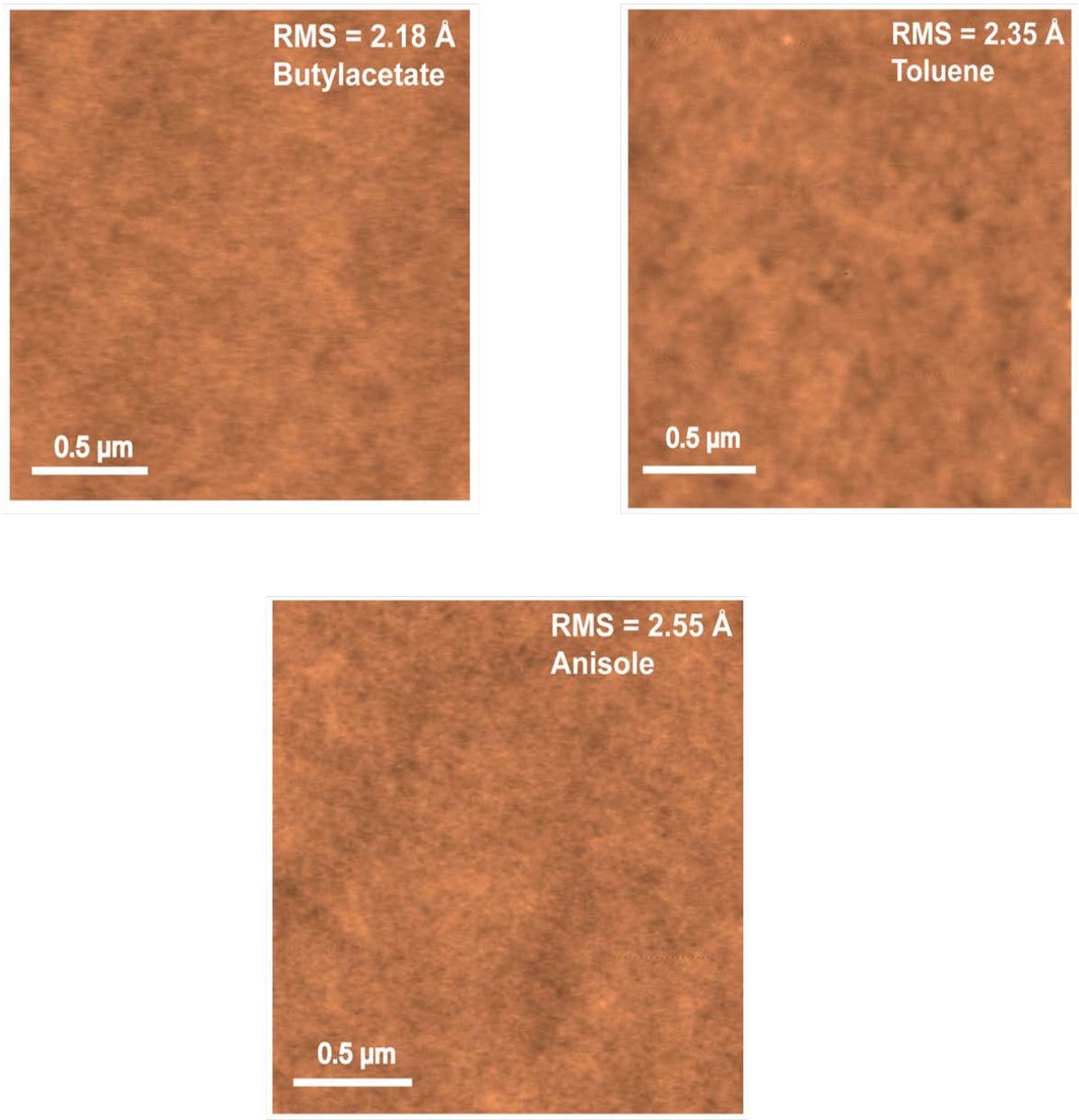

Fig. 4.1: Atomic force micrographs of PMMA films prepared in different solvents.

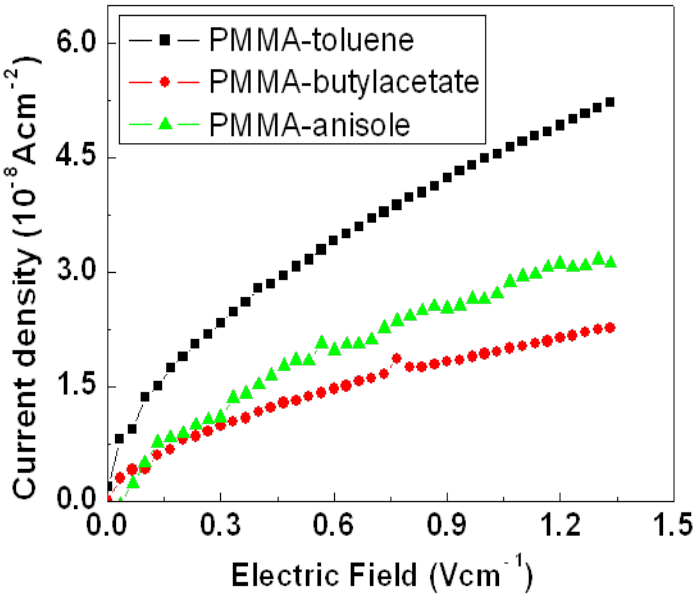

Fig. 4.2: Current density – electric density characterization for PMMA dielectric film dissolved in butylacetate, toluene, and anisole.

4.2.2 MIS Diode Characteristics

Figure 4.3 shows capacitance-voltage (C-V) characteristics of PFB MIS diodes with PMMA dielectric dissolved in butylacetate, toluene, and anisole measured at four different frequencies in the low kHz range. Observable is the existence of frequency dispersions in the accumulation and depletion regions. The C-V curves are typical of p-type organic MIS behavior characterized by an accumulation of holes at the dielectric/semiconductor interface at large negative bias, a depletion of holes from the dielectric/semiconductor interface at less negative bias, and a deep depletion of holes from the dielectric/semiconductor interfacial region at positive bias, corresponding to the accumulation, depletion, and deep depletion regimes. No inversion is observed, which is typical of organic MIS diodes. The amount of frequency dispersion in

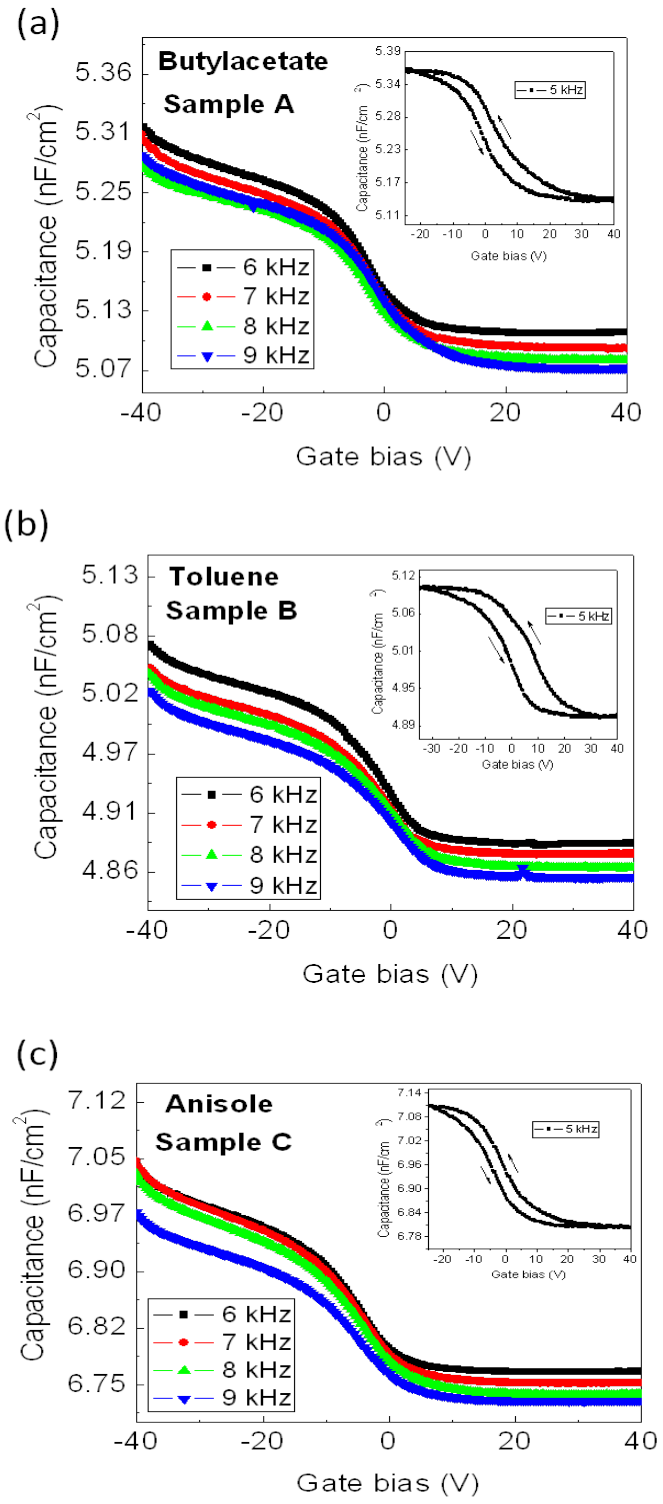

Fig. 4.3: C-V characteristics between 6 – 9 kHz for Al/PMMA/PFB/Au structure and C-V characteristics of Al/PMMA/PFB/Au MIS diodes at 5 kHz (insets) for (a) butylacetate (Sample A), (b) toluene (Sample B), and anisole (Sample C).

accumulation capacitance, ΔC_{OX} is approximately 0.5 %, 0.8 %, and 0.9 % for Samples A, B, and C, respectively. These values are smaller than similar observations involving inorganic devices [31]. The dispersion in the accumulation region may arise from a difference in the response of trapped and mobile charges in the interface and the bulk.

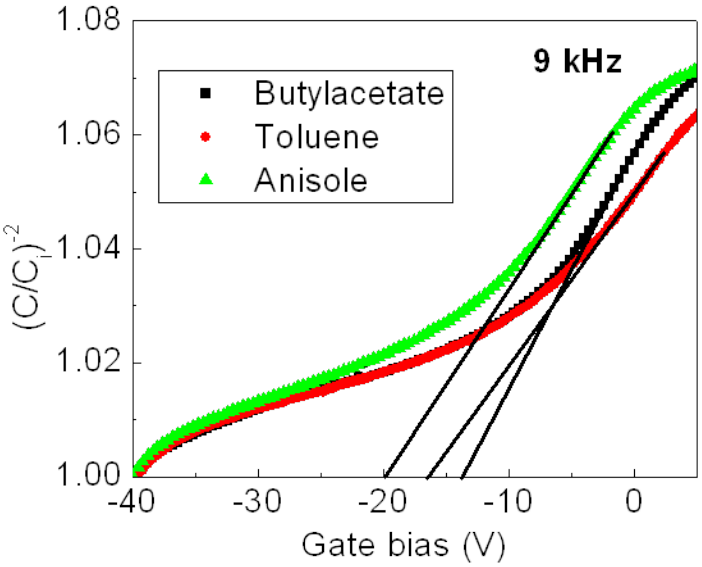

Fig. 4.4: Plot of $(C/C_i)^{-2}$ vs. gate bias (V) for Samples A, B, and C.

The insets of Fig. 4.3 show the hysteresis effects observed by measurement of the devices at 5 kHz by sweeping the gate bias (V) continuously in a staircase shape with a 0.4 V step, starting from – 40 V, passing through 40 V, and finally back to – 40 V. The magnitude of the hysteresis, Δ is approximately 3.47 V, 8.62 V, and 3.97 V for Samples A, B, and C, respectively. The magnitude of hysteresis observed here with PMMA as the insulator is well less than we had observed with the use of SiO_2 [32]. The hysteresis direction reveals the nature of charge injection. The counterclockwise loop of the hysteresis in the C-V curve indicates a positive carrier injection into the PFB layer with subsequent trapping [33]. The difference in the accumulation capacitance is due to

the variations in PMMA thickness for the three MIS diodes. According to the standard Schottky-Mott analysis, the unintentional doping density can be extracted using the relation [33]

$$\frac{\partial\left(1/C^2\right)}{\partial V_g} = \frac{2}{q\varepsilon_{semi}\varepsilon_0 N_A A^2} \qquad 4.1$$

where C is the capacitance in the depletion region, V_g is the gate bias, ε_{semi} is the relative permeability of the semiconductor, ε_0 is the permittivity of vacuum, A is the area of the device, and N_A is the doping density. The acceptor doping density N_A was estimated to be 2.6 × 10^{17} cm^{-3}, 2.9 × 10^{17} cm^{-3}, and 4.9 ×10^{17} cm^{-3} for Samples A, B, and C, respectively.

From the plot of $(C/C_i)^{-2}$ versus gate bias (V) taken at a frequency of 9 kHz (Fig. 4.4), flat band voltages (V_{FB}) of -14 V, -16.6 V, and -21 V were deduced for Samples A, B, and C, respectively, by extrapolating to the *x*-intercept at $(C/C_i)^{-2}$ = 1. Here, C_i is the capacitance of the PMMA layer. Noticeable from this plot is the negative occurrence and the obvious shifts in V_{FB} of the three devices. While the difference in the metal and semiconductor work functions (ϕ_{ms}) and the existence of positive interface traps (Q_i) at the semiconductor-insulator interface are known to account for negative V_{FB} in non-ideal MIS capacitors as given by the relation [34],

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i} \qquad 4.2$$

our observed shifts in V_{FB} are not due to ϕ_{ms} since it is presumably similar for the three devices. Therefore, considering our calculated values for density of interface states (D_{it}) at flat band for the various devices (Sample A = 2.8 ×10^{12} $eV^{-1}cm^{-2}$, Sample B = 3.9 ×10^{12} $eV^{-1}cm^{-2}$, Sample C = 5.0 ×10^{12} $eV^{-1}cm^{-2}$), the details of which are found below, and making use of Equation 4.2, we can conclude that the shifts in V_{FB} are due to the differences in the density of holes trapped at the semiconductor-insulator interfaces of these devices. The lower the D_{it} at flat band, the less negative is the shift in flat band voltage.

Figure 4.5 shows conductance – voltage (G-V) characteristics of the Al/PMMA/PFB/Au MIS diodes. The devices undergo a gate bias independent loss which results from the bias independence of electron and hole densities at the point where the Fermi level crosses bulk trap levels located near the mid gap [35]. This bias independent loss evidenced by the absence of conductance peaks suggests that loss in the devices is mainly dominated by generation and recombination through bulk states. Interface states usually give rise to confined energy levels at the semiconductor-insulator interface. The use of the conductance technique, as suggested by Nicollian and Goetzberger [35] in the depletion region enables the extraction of interface states density, capture probability and time constant dispersion of the majority carriers (holes in this case) from the real component of the admittance.

The interface trap states change occupancy over a few *KT/q* wide centered about the Fermi level by interacting with the semiconductor bands via the emission and

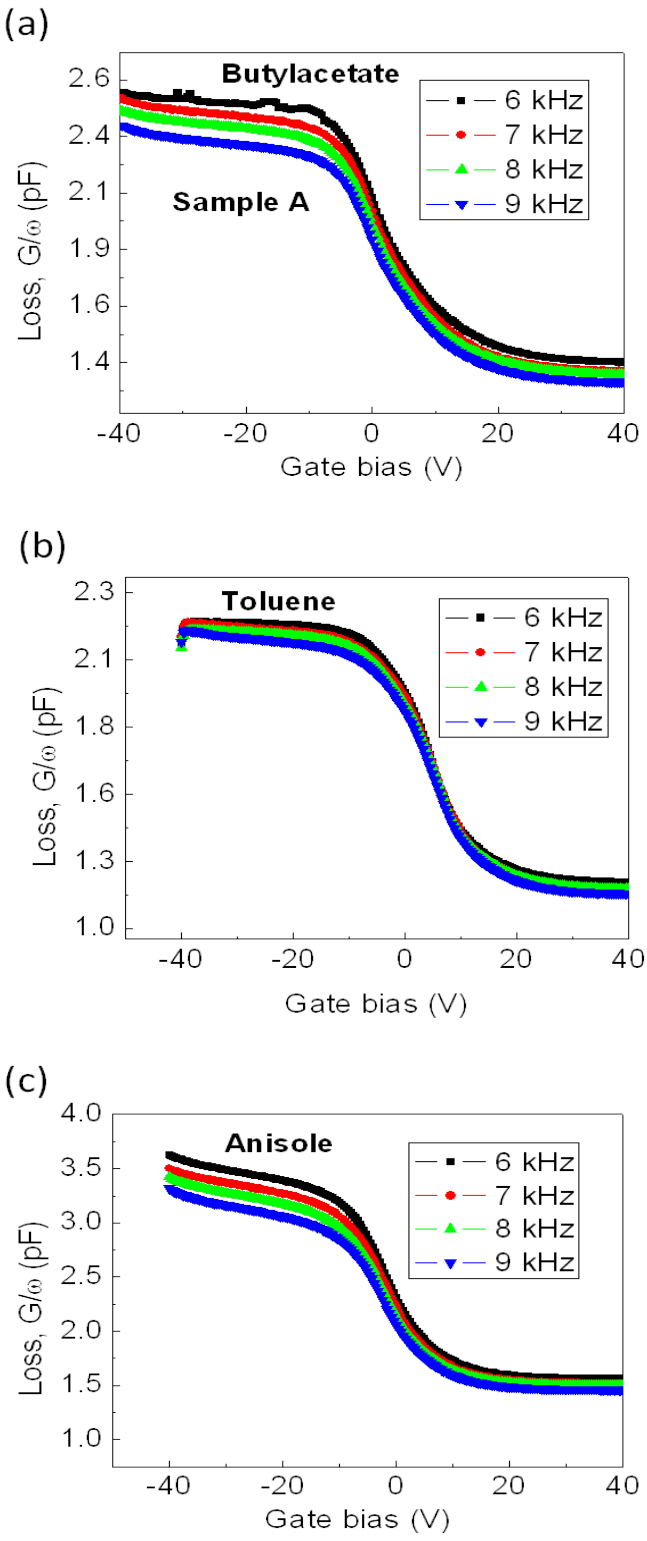

Fig. 4.5: Frequency dependence of loss (conductance/angular frequency) vs. gate bias for MIS diodes: (a) Sample A, (b) Sample B, and (c) Sample C.

capture of carriers. A small ac signal applied to the gate of an MIS diode results in an alternate movement of the band edges toward or away from the Fermi level. Using the conductance technique, interface trap states are detected through the loss resulting from changes in their occupancy due to small variations in dc gate bias. Usually, a conductance peak is observed as a result of the ac loss due to capture and emission of carriers by these interface states. A determination of the interface trap energy states (E_{it}) can be easily carried out by calculating the degree of band bending induced by the applied bias, by solving the Poisson equation in the depletion approximation:

$$E_{it} - E_{Fb} = \frac{qN_A \varepsilon \varepsilon_0 A^2}{2C_d{}^2} \qquad 4.3$$

where q is the electronic charge, N_A is the acceptor doping density, ε is the semiconductor dielectric constant, ε_0 is the permittivity of free space, and C_d is estimated at the relevant voltage. Figure 4.6 shows plots of interface state density (D_{it}) versus energy for Samples A, B, and C. The results of the analyses show a non-linear decrease of the interface trap density as one moves away from the bulk Fermi level. For sample A, D_{it} was found to decrease from approximately 2.8×10^{12} to 1.2×10^{12} eV^{-1} cm^2 over an energy range of 0.075 eV to 0.385 eV with a flat band value of 2.8×10^{12} eV^{-1} cm^2. D_{it} decreased from approximately 3.9×10^{12} to 1.1×10^{12} over an energy range of 0.035 eV to 0.395 eV in Sample B, with a calculated flat band value of 3.9×10^{12} eV^{-1} cm^{-2}. The D_{it} at flat band for Sample C was calculated to be 5.0×10^{12} eV^{-1} cm^{-2} and it decreased to approximately 1.5×10^{12} eV^{-1} cm^2 over an energy range of 0.035 cm^{-2} to

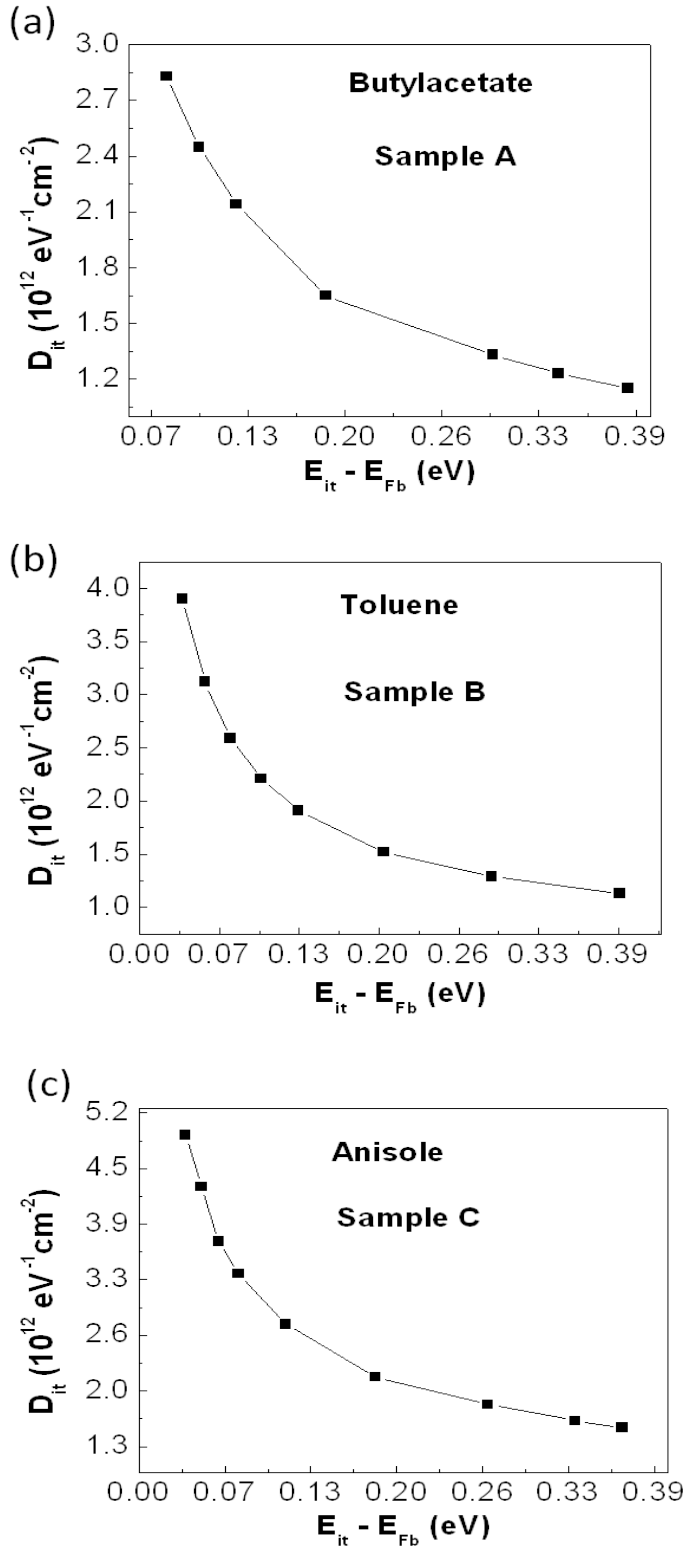

Fig. 4.6: Plot of D_{it} as a function of energy above bulk Fermi level, $E_{it} – E_{Fb}$ for Sample A, Sample B, and Sample C.

0.366 eV above the bulk Fermi level. A comparison of D_{it} versus energy plots for the three samples shows that D_{it} at flat band is least in sample A. The above D_{it} values were extracted from the depletion regions of the MIS diodes: between -13 and 5 V (Sample A), between -17 and 4 V (Sample B), and between -21 and 3 V (Sample C).

4.2.3 OFET Characteristics

Figure 4.7 shows the output characteristics of the PFB-based FET prepared using butylacetate, which is typical of transistor devices. This device exhibits leakage current of the order of about 0.1 nA. Also shown in Fig. 4.8 are the FET transfer characteristics from all three Samples (A-C) in the saturation region (V_D = - 40 V). The square root of the drain current is also plotted for all three. According to theoretical prediction [33], above the threshold voltage, these transfer plots should yield a straight line whose slope is proportional to the carrier mobility (μ), as well as a threshold voltage (V_T) which is equal to the intercept. By fitting the linear region between -15 and -30 V of V_G, the field-effect mobility in the saturation regime could be obtained by applying the standard saturation regime current-voltage FET characteristics shown in equation 2.18. The highest average field-effect mobility of 0.2 × 10^{-4} cm^2 V^{-1} s^{-1} and the lowest threshold voltage of -0.2 V were obtained for Sample A. For Sample B, the average field-effect mobility was calculated to be 0.4 × 10^{-5} cm^2 V^{-1} s^{-1} and a threshold voltage of -3.3 V was obtained. Sample C yielded average field-effect mobility and a threshold voltage of 0.2 × 10^{-5} cm^2 V^{-1} s^{-1} and -7.2 V, respectively. The FET mobilities here are higher than MAPLE deposited PFB on as-is SiO_2 as the dielectric layer [32].

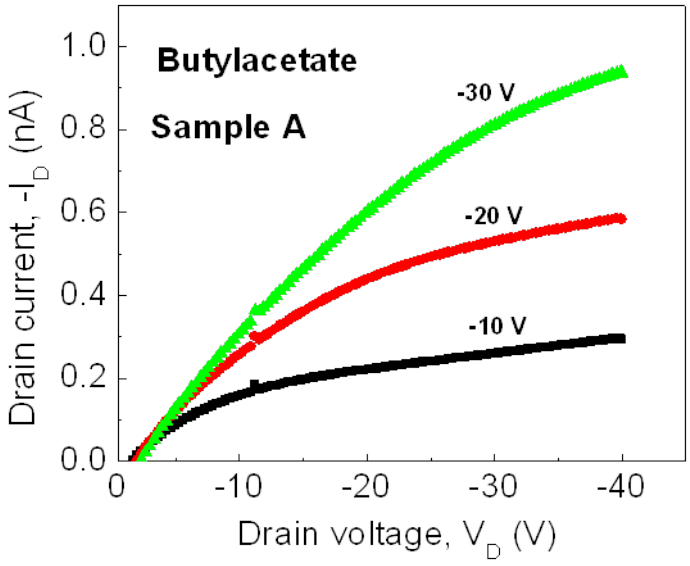

Fig. 4.7: Representative electrical output characteristics of the FETs from various solvents.

The threshold voltage is (V_T) negative for all the devices, which is typical of p-channel devices and is given by the relation [34]

$$V_T = V_{FB} + \frac{Q_d}{C_i} - 2\phi_F \qquad 4.4$$

where Q_d / C_i accommodates the charge in the depletion region, and ϕ_F defined as $(E_i - E_F)/q$ in the neutral substrate, is the bulk potential. From the above relation, it is understandable that an applied negative voltage higher than V_T is needed in order to achieve flat band condition. The depletion charge is proportional to the acceptor concentration (N_A), and as such, should be least for Sample A and highest for Sample C. Also looking at the extracted values for N_A, it is immediately obvious that ϕ_F is least in Sample A and highest in Sample C. Therefore, considering our aforementioned values for V_{FB} (in the MIS diodes) and using Eq. 4.4, the increase in threshold voltage of the

OFETs become easily explainable. Therefore, we can conclude that the behavior of V_T in FETs is predictable from knowledge of the doping concentration and the behavior of V_{FB} in MIS capacitors, in accordance with theory.

Considering that FETs based on polymer dielectrics typically show some hysteresis (shifts in threshold voltage depending on the sweep direction of the gate voltage) in I_D, remarkably, our FETs exhibited no hysteresis for Sample A and little hysteresis in only the off regime for Samples B and C. Hysteresis in organic thin film transistors has been linked with dielectric bulk trapping of electrons and holes injected from the gate [36,37]. It could be deduced that the absence of hysteresis in Sample A and little hysteresis in Samples B, and C are very likely due to suppressed gate injection of carriers and subsequent trapping in the PMMA bulk. The device characteristics for our FETs and MIS diodes are summarized in Table 4.1. As is evident from Table 4.1, the type of solvent used in dissolving the dielectric has quite noticeable effects on the performance of the devices. The morphology of the dielectric layer onto which the semiconducting layer is formed has been observed to play an important role in the performance of polymer devices [38]. Similarly, surface roughness of polymer dielectric films, which is very closely related to the solubility parameter, could be dependent on the type of solvent used [39]. It is well known that the less the difference between the solubility parameters of a polymer and its solvent, the more soluble the polymer is in the solvent and vice versa. Table 1 contains the solubility parameters of the various solvents used, while the solubility parameter for PMMA is 22.5 $(MPa)^{1/2}$ [40].

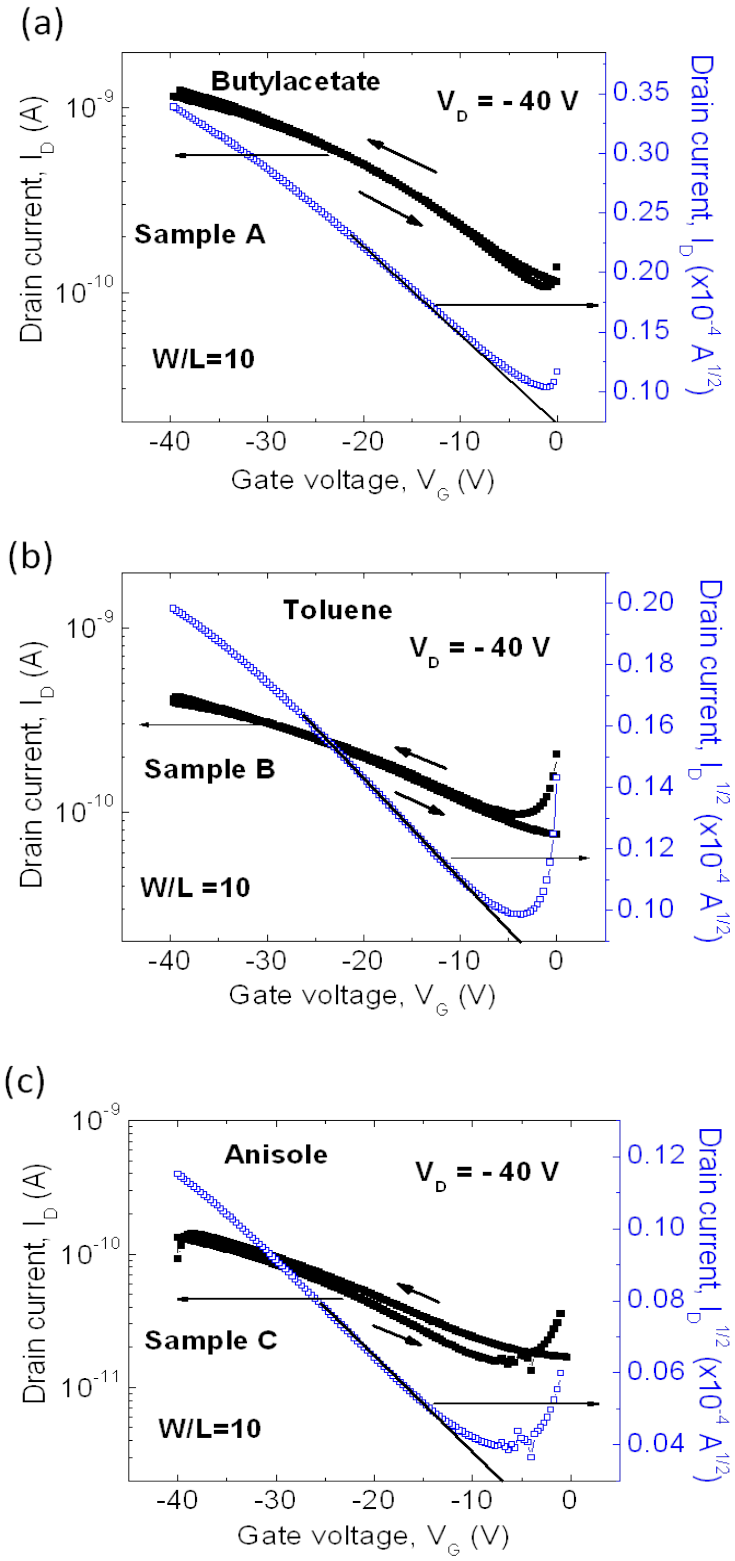

Fig. 4.8: Electrical transfer characteristics of OFETs from various solvents: (a) butylacetate (Sample A), (b) toluene (Sample B), and (c) Sample C.

TABLE 4.1: Field-effect mobilities in saturation regime, threshold voltages, root mean square values, density of interface state at flat band (D_{it}), and solubility parameters for various solvents.

	Mobility (cm^2/Vs)	Threshold voltage (V)	PMMA film rms (Å)	D_{it} @ flatband ($eV^{-1}\ cm^{-2}$)	PMMA/solvent solubility parameter difference $(MPa)^{1/2}$
Butylacetate (Sample A)	0.2×10^{-4}	-0.2	2.18	2.8×10^{12}	5.1
Toluene (Sample B)	0.4×10^{-5}	-3.8	2.35	3.9×10^{12}	4.4
Anisole (Sample C)	0.2×10^{-5}	-7.2	2.55	5.0×10^{12}	3.0

As could be seen from Table 4.1, while the FET mobility decreased with increasing PMMA film roughness, D_{it} at flatband of the MIS diodes followed the same trend as the PMMA film roughness. Earlier reports have shown that a rougher surface leads to increase in voids and defects giving rise to increase in interface trap states at the semiconductor-dielectric interface and consequent adverse effects on field-effect mobility and molecular ordering [41-43]. Our results point in the direction that there is a trade-off between solubility and swelling of the dielectric layer in the actual device performance. Although PMMA is most soluble in anisole, the device performance is worse compared to the other two solvents. It has been observed that the degree of swelling in a polymer increases with the decrease in the difference between the solubility parameters of the polymer and the solvent [38,39]; anisole is thus most likely

to leave behind the roughest PMMA film surface on evaporation, and as such, the lowest average field-effect mobility, followed by toluene, then butylacetate.

4.3 Conclusions

In summary, we have demonstrated the success of the MAPLE technique in overcoming the solvent selectivity and inherent swelling and dissolution problems associated with fabricating device-quality polymer FETs and MIS diodes via traditional spincoating technique especially when non-orthogonal solvents are used. It is observed that the higher the difference between the solubility parameters of the solvent and PMMA, the less rough the PMMA surface, and consequently, the better the device performance. Negative shifts of the threshold voltage in the OFETs were correlated with differences in acceptor doping density and similar shifts in flat band voltage of the MIS diodes, which was found to be due to difference in the density of interface states at flat band. Our PFB-based OFET exhibited a hysteresis-free operation, a low threshold voltage of -0.2 V, and field-effect mobility of 0.2×10^{-4} cm^2 V^{-1} s^{-1}. The density of interface trap states in the MIS diodes was found to decrease non-linearly and are distributed over an energy range of 0.075 to 0.385 eV above the bulk Fermi level and energy loss was found to be dominated by the emission and capture of carriers though bulk states.

CHAPTER 5

PENTACENE FIELD-EFFECT TRANSISTORS AND METAL-INSULATOR-SEMICONDUCTOR CAPACITORS WITH POLY (METHYL METHACRYLATE) GATE DIELECTRIC

5.1 Introduction

Having observed a dependence of the properties of the PMMA dielectric layer and consequently, the overall properties of our MAPLE-grown PFB-based devices on the solvent used to dissolve PMMA, we set out to investigate the effects of PMMA solvents in the properties of evaporated pentacene-based devices, especially in achieving low gate voltage OFET operation. Motivated by the need for low-cost, low-power, and large-area flexible electronics, the search for low-operating voltage and stable OFETs has been of utmost attraction. In order to achieve stable and low-operating voltage OFETs, the dielectric surface has to be hydrophobic and must provide a relatively high capacitance typically achievable via the use of high dielectric constant materials and/or ultra-thin layers.

Poly (methyl methacrylate) (PMMA) is a great candidate for operationally stable and reproducible OFETs owing to its high hydrophobicity, but has limitations in realizing low-operating voltage transistors due to its low dielectric constant ($k \leq 3.5$). Recently,

low-operating voltage OFETs have been achieved through the use of high-*k* inorganic dielectric materials such as Al_2O_3 [44], $Ti_{1-x}Si_xO_2$ [45], and low-*k* organic/high-*k* inorganic dielectric hybrid bilayers such as PMMA/ZrO_2 [46] and PMMA/Ta_2O_5 [47]. Despite the successful application of high-*k* inorganic dielectrics in achieving low-operating voltage OFETs, polymer dielectrics are still preferable since they give rise to a high-quality interface [47]. Low-operating voltage OFETs making use of high-*k* cross-linked polymer dielectrics such as poly (vinyl alcohol) [48,49] and cyanoethylated pullulan [50] have also been reported. Pentacene-based OFETs incorporating PMMA gate dielectric usually have high operating voltages (> -20 V) and PMMA films have been reported to have a high density of pin-holes for thicknesses below 150 nm [51] and almost unusable at 100 nm without cross-linking [25]. The lowest reported operating voltage (-8 V) for a PMMA-based OFET was achieved by using a 30 nm-thick cross-linked PMMA layer [25].

Here, we demonstrate the electrical characteristics and operational stability of low-operating voltage pentacene OFETs with thin pristine PMMA gate dielectric dissolved in a solvent (propylene carbonate) with a large dipole moment. These results are compared with devices from pristine PMMA gate dielectric dissolved in butylacetate (BTAc) which has a low dipole moment. The dipole moments of the solvents are shown in Table 2.1. Thin low-*k* dielectric films via dissolution in high dipole moment solvent could potentially be used to obtain low-operating voltages in solution processable polymeric semiconductor- based OFETs. OFETs/MIS structures fabricated from PMMA dissolved in PC are denoted as PMMA-PC while those from BTAc are denoted as PMMA-BTAc.

5.2 Results and Discussion

5.2.1 Morphology and Structure of the Dielectric Films

The surface morphologies of PMMA-PC, PMMA-BTAc and pentacene films on PMMA-PC and PMMA-BTAc are shown in Figs. 5.1(a-d). The surface root-mean-square (rms) roughness of the PMMA-PC and PMMA-BTAc films were found to be 1.0 nm and 1.2 nm, respectively over a 5 µm × 5 µm area. The pentacene films exhibited typical dendritic structures with layer-by-layer formation and large grain sizes (~ 1 µm)

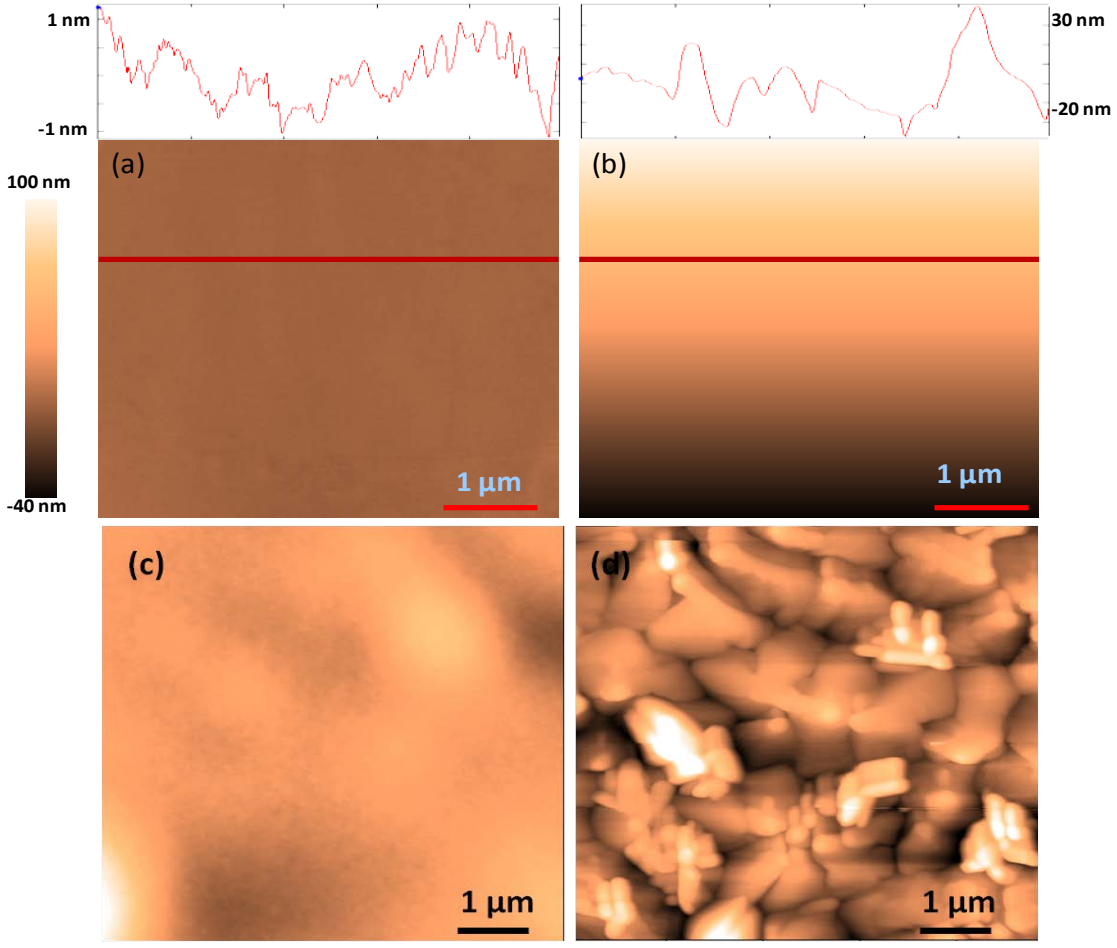

Fig. 5.1: Atomic force microscopy images of (a) PMMA-PC (b) pentacene on PMMA-PC (c) PMMA-BTAc and (d) pentacene on PMMA-BTAc.

comparable to other works [49], despite the relatively large PMMA film roughness. Improved crystallinity of the pentacene films may be due to a highly diminished number of polar groups on the PMMA surface. Polar groups are known to be responsible for surface energy fluctuations on polymer dielectric surfaces, which inhibit surface diffusion and enhance nucleation density [52]. Figure 5.2 shows the representative Raman spectra of PMMA-BTAc and PMMA-PC dielectric films. The 1450 cm^{-1} band belonging to the C-H vibration is the most prominent in the two spectra. Also visible is the 1240 cm^{-1} band. More importantly, the similarity of the Raman bands in both spectra is an indication of the solvent-independent nature of the PMMA structure.

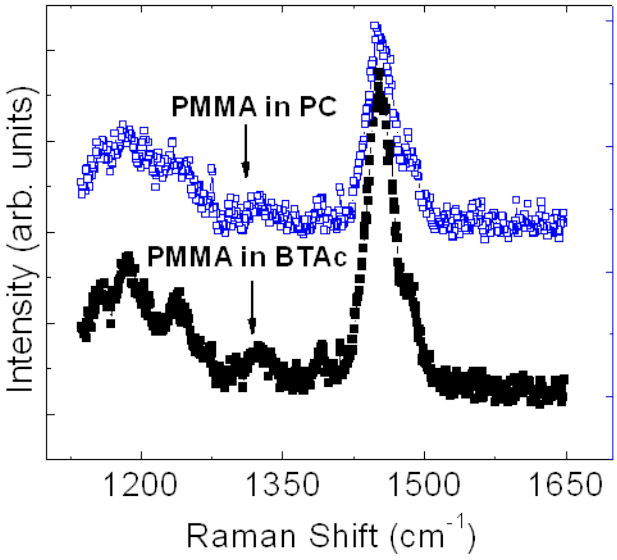

Fig. 5.2: Raman spectra of PMMA-BTAc and PMMA-PC dielectric films.

5.2.2 MIS Diode Characteristics

Capacitance-voltage (C-V) measurements from MIS devices (Fig. 5.3) show typical *p*-type behavior, which is characterized by an accumulation region at negative

bias, a depletion region at less negative bias, and a deep depletion region at positive bias. The PMMA-PC device exhibits almost no hysteresis (no flat band voltage, V_{FB}, shift)

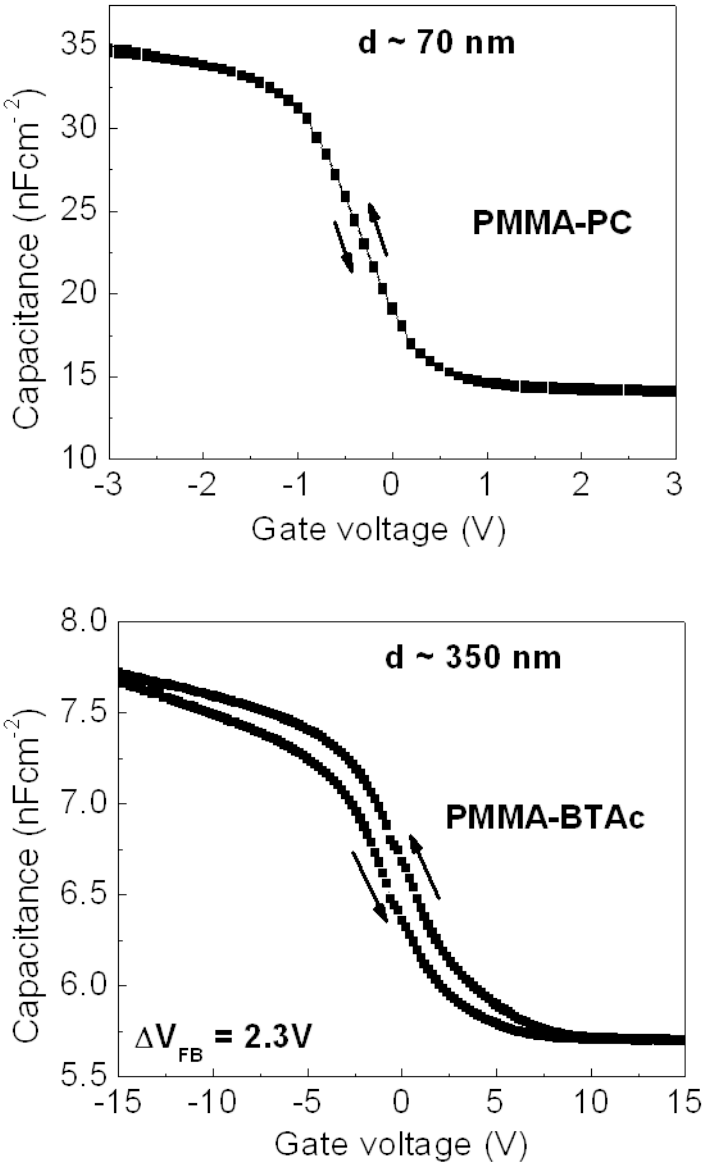

Fig. 5.3: C-V curves of Al/PMMA-PC/Pentacene/Au and Al/PMMA-PC/Pentacene/Au MIS diodes at a frequency of 5 kHz.

when the gate bias is continuously swept from -3 V, passing through 3 V and back to -3 V at a step voltage of 0.05 V, while the PMMA-BTAc device exhibits a flat band voltage

shift (ΔV_{FB}) of 2.3 V when the gate bias is continuously swept from -15 V, passing through 15 V and back. The absence of hysteresis and near-zero occurrence of V_{FB} in the PMMA-PC device are attributed to an improved and thinner PMMA dielectric layer with

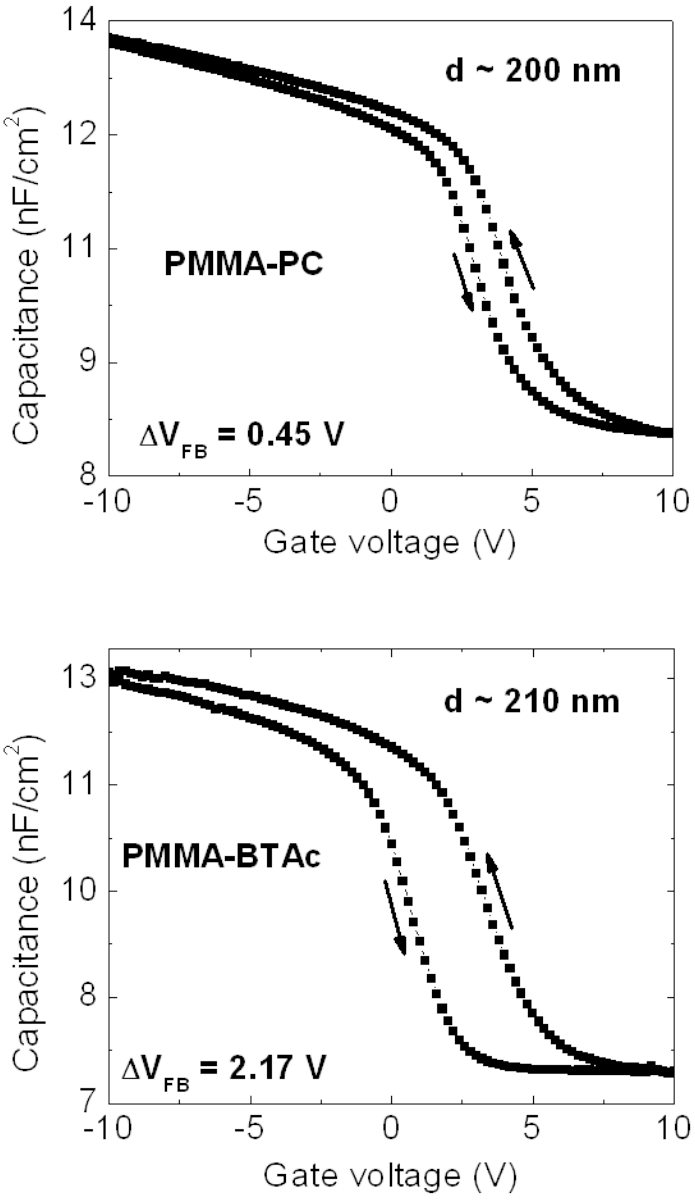

Fig. 5.4: C-V curves of Al/PMMA-PC/Pentacene/Au and Al/PMMA-PC/Pentacene/Au MIS diodes at a frequency of 5 kHz.

a highly diminished amount of trap states arising from polar groups, which usually give rise to slow polarization in PMMA bulk or at the semiconductor-PMMA interface. MIS device fabricated from PMMA-PC with comparable PMMA-BTAc film thickness exhibits ΔV_{FB} of nearly an order of magnitude lower than observed in PMMA-BTAc device (Fig. 5.4).

The improvements in dielectric properties observed with PC may be related to the mean square end-to-end distance, which has been shown to increase with an increase in dipole moment. This is mainly due to the increase in the interaction forces between polymer and solvent cluster [53]. As a result, the polymer chains remain more extended in solution. This may also improve the degree of orientation of the PMMA functional groups during deposition and baking; although, other mechanisms accounting for the excellent dielectric properties of our thin PMMA film spincast from PC are currently under investigation.

5.2.3 OFET Characteristics

Relevant extracted electrical parameters for both PMMA-PC (70 nm) and PMMA-BTAc OFETs (350 nm) are summarized in Table 5.1 below. There is an obvious enhancement in every FET electrical characteristic, including the operating gate voltage, with the use of PC over BTAc. Figures 5.5 and 5.6 show the output and transfer current-voltage (I-V) characteristics of OFETs measured under ambient conditions. These are typical characteristics of ~10 measured devices. Our OFETs exhibit good linear and saturation behaviors in the output characteristics and the PMMA-PC device could be operated below -3 V, aided by its relatively high dielectric capacitance (20 $nFcm^{-2}$ at 100 kHz).

Table 5.1: Summary of electrical characteristics of PMMA (with PC) and PMMA-BTAc OFETs.

	μ (cm2/Vs)	V_T (V)	ΔV_T (V) (hysteresis)	SS (V/dec)	ΔV_T (V) (bias stress)	V_{on} (V)	V_G (V)
PMMA-PC	0.1	-1	0.11	0.4	0.08	-0.3	< -3
PMMA-BTAc	0.04	-2.7	0.43	1.5	0.18	-0.9	< -8

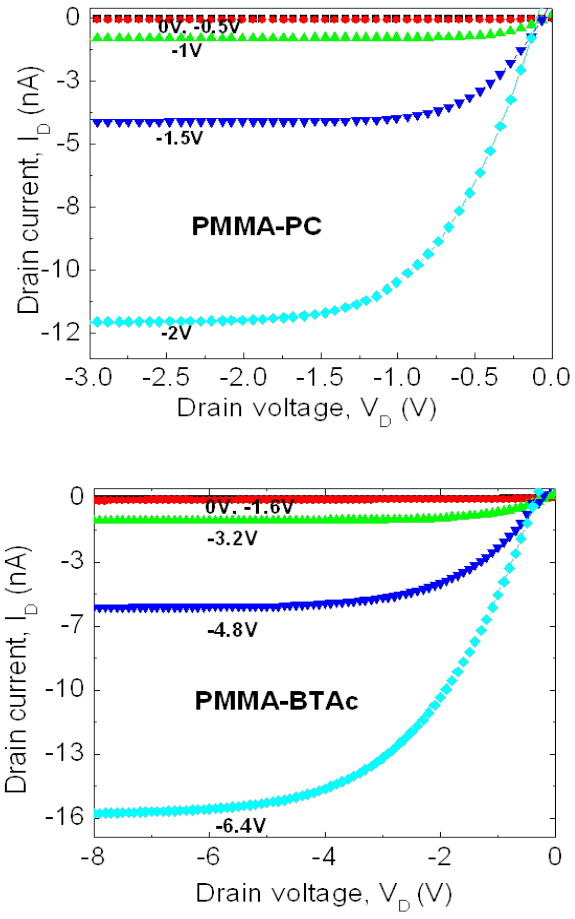

Fig. 5.5: Output characteristics for out OFETs.

The electrical parameters of our OFETs were obtained from the saturation regime by using Eq. 2.21.

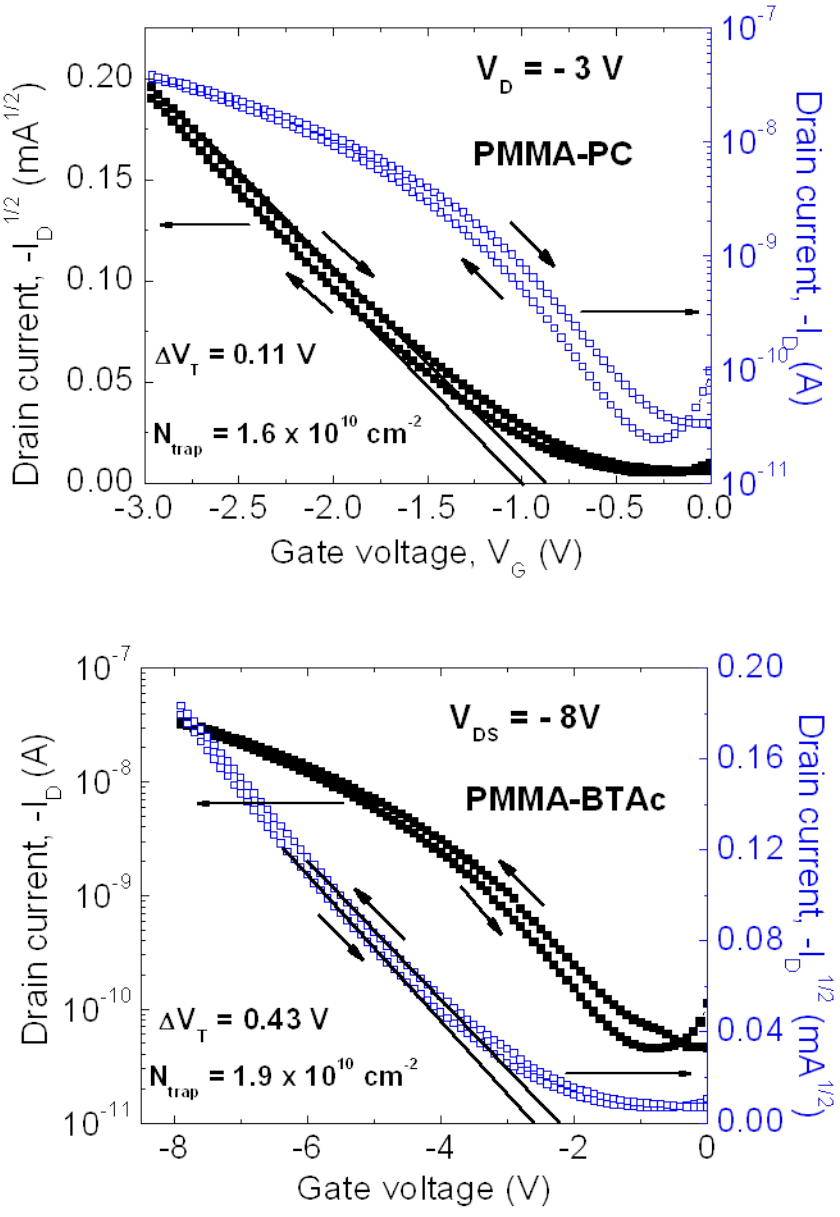

Fig. 5.6: Transfer characteristics for out OFETs.

the channel length, V_G is the gate voltage, I_D is the drain current, and μ is the field-effect mobility. The subthreshold slope (SS), controls the voltage swing required for the

off-to-on switching of the transistor and ought to be as low as possible [48]. The lower value of SS for our PMMA-PC OFET could be responsible for our estimated near-zero OFET turn-on voltage (V_{on}) of -0.3 V. Based on the SS value obtained from the OFET and using the relation, $N_{trap}^{\max} \approx \left[\frac{qSS\log(e)}{KT} - 1\right]\frac{C_i}{q}$ [50], we estimate a maximum trapped charge density of 7.1 x 10^{11} cm^{-2} and 4.4 x 10^{10} cm^{-2} for our PMMA-PC and PMMA-BTAc OFETs, respectively.

In order to verify the reproducibility and operational stability of our OFETs, hysteresis, duty-cycle, and gate bias stress measurements were carried out on our devices. We investigated the hysteresis by fixing the drain voltage at -3 V and sweeping the gate voltage from 0 to -3 V (forward direction) and then back. As seen from Fig. 5.6, the PMMA-PC OFET exhibits little off-regime hysteresis and a negligible positive shift of the threshold voltage (V_T) from -1 to -0.89 V (ΔV_T = 0.11 V), consistent with the absence of hysteresis in the C-V characteristics of the corresponding MIS diode, while the PMMA-BTAc OFET exhibits a higher ΔV_T of 0.43 V. With the above values, we estimate interfacial trap densities (N_{trap}) of 1.6 x 10^{10} cm^{-2} and 1.9 x 10^{10} cm^{-2} for our PMMA-PC OFET and PMMA-BTAc OFET, respectively using the relation, $N_{trap} \approx C_i\Delta V_T/q$ [48]. Our estimated value for N_{trap} in our PMMA-PC OFET is about an order of magnitude less than those reported for pentacene-based devices [50]. Polar molecules (such as polar functional groups and adsorbed water) at the organic semiconductor-dielectric interface have been reported to be responsible for positive V_T shifts in organic devices [54]. The low values for the trapped charge density as well as observed negligible ΔV_T in our

OFETs are credited to the hydrophobicity and reduced polarity of the PMMA surface, which strongly inhibit the adsorption of water molecules and resultant charge trapping activities.

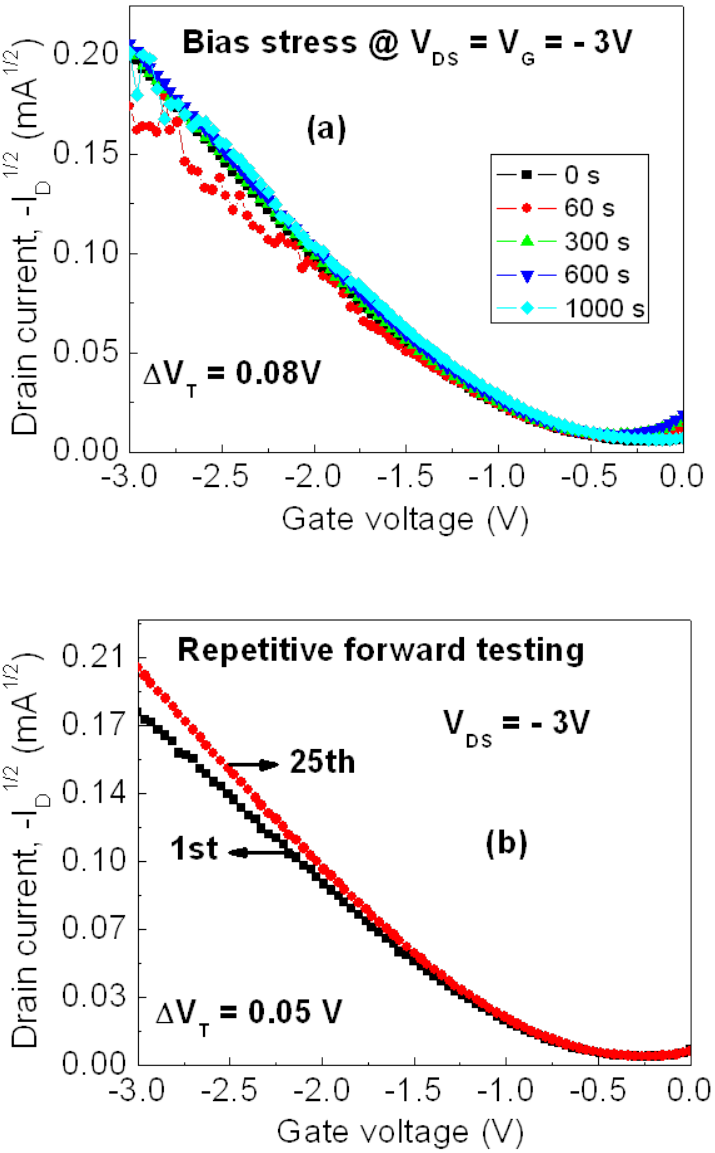

Fig. 5.7: Operational stability of OFET transfer characteristics (a) after bias stress at V_G = V_D = -3 V at varying stress times. (b) Repetitive forward testing at V_D = -3 V.

To investigate the bias-stress effect on the OFET (PMMA-PC), which could be manifested in OFET hysteresis and/or V_T shifts, I-V transfer characteristic was first

measured without applying any bias stress. Subsequently, bias stress ($V_G = V_D = -3$ V) was applied for set times and the I-V transfer characteristic was measured after each set time (Fig. 5.7a). In all, the OFET was subjected to 1,960 s of dc bias stress. We observe only very little shifts in transfer characteristics, with V_T shifting by a negligible 0.08 V – a confirmation of our low trap density estimates and a testament to the stability and reproducibility of our device. Bias stress investigations with similar time scales on SiO_2-based OFETs have shown V_T shifts higher than 13 V [55]. Considering the critical relationship between MIS V_{FB} and FET V_T [56], bias stress measurements carried out on the MIS diode showed no shifts in V_{FB} after 1,960 s at a gate bias of – 3 V, consistent with the OFET observations. Next, we stressed our OFET by repeatedly measuring transfer characteristics in the forward direction at a drain voltage of -3 V. This was carried out 25 times with a 4 s measurement interval. Shown in Fig. 5.7b are representative plots for the 1^{st} and 25^{th} cycles. Here again, no obvious change in the shape of the transfer curves or any device degradation was seen; only V_T shifted by 0.05 V. Importantly, negligible shifts of V_T indicate that our OFET devices have "clean interfaces" and are operationally stable and reproducible.

5.3 Conclusion

In summary, this study demonstrates that with a proper choice of solvent, thin, non-crosslinked and single PMMA dielectric layers could be used to achieve stable and very low-operating voltage OFETs (below -3 V); hence, opening up the prospects of a possible utilization of less-polar and low–*k* dielectric polymers in realizing device-quality,

stable, and low-voltage transistors that could be employed in the design of practical electronic circuits.

CHAPTER 6

LOW-OPERATING VOLTAGE AND STABLE PENTACENE FIELD-EFFECT TRANSISTORS WITH LOW-K POLY (4-VINYL PHENOL) POLYMER GATE DIELECTRICS

6.1 Introduction

As a further proof of the robustness and efficiency of our technique of achieving high yield, stable, and low-operating voltage devices incorporating low-*k* polymeric dielectrics dissolved in high dipole moment and high-*k* solvents, we fabricated OFETs and MIS diodes using pristine and cross-linked low-*k* PVP dissolved in PC and dimethyl sulfoxide (DMSO), as gate dielectrics and studied their electrical characteristics and operational as well as environmental stability. Again, from the drain current in the saturation region of an OFET as given by Eq. 2.20, it becomes obvious that the dielectric capacitance has to be high in order to obtain a high drain current at low gate voltage. The dielectric capacitance is defined by $C = k\varepsilon_0 A/d$, where *k* is the dielectric constant, ε_0 is the permittivity of free space, A is the area of the capacitor, and d is the dielectric thickness. Compared to most polymer dielectrics, poly(4-vinyl phenol) (PVP) turns out to be the most frequently employed in the fabrication of OFETs due to its higher performance [57,58]; however, its usage in OFETs for practical electronic circuits

(requiring low-operating voltage and threshold voltage stability) may still be limited by its low dielectric constant (like in most conventional polymer dielectrics) and presence of hysteresis during OFET operation [59] arising from its hydrophilicity. Therefore, in order to achieve low-voltage and stable OFETs, there has been the incorporation of high-*k* inorganic dielectrics or high-*k* inorganic/hydrophobic low-*k* organic dielectric bilayers [60,61,62,63]. Pentacene field-effect transistors incorporating single layer PVP dielectric usually operate at high voltages (> -30 V) due to its low dielectric constant [58,64,65]. Although, low-operating voltage OFETs using single-layer cross-linked PVP have been reported [66,57], there are hardly any studies of their operational and/or environmental stability.

In Chapter 5, we demonstrated highly stable and record low-voltage operation in OFETs incorporating thin pristine and single layer low-*k* poly(methyl methacrylate) (PMMA) gate dielectric dissolved in a high dipole moment solvent (propylene carbonate) [67]. The report suggested that thin layers of low-*k* polymer gate dielectrics are achievable via an appropriate choice of solvent and that the enhancement in the quality of the thin non-crosslinked PMMA gate dielectric and consequently in the OFET performance, could have been aided by the use of propylene carbonate as solvent. Here, we report on the study of the electrical characteristics, operational stability as well as environmental stability of low-operating voltage OFETs incorporating single pristine and cross-linked low-*k* PVP dielectric layers. This study suggests that the use of thin and single layer PVP films in OFETs ensures not only low-operating voltages, but high operational and environmental stability comparable to devices with hydrophobic

polymer dielectrics as well. Also reported are results of the electrical characterizations of accompanying metal-insulator-semiconductor diodes.

6.2 Experimental details

PVP (Mw = 25,000 g/mol) and PVP cross-linked with methylated poly(melamine-co-formaldehyde) (PMMF) were dissolved in propylene carbonate (PC) and subsequently spincoated on cleaned thermally-evaporated aluminum-coated (60 nm) glass substrates in a nitrogen-filled glove box. The resulting film thicknesses were ~ 80 nm and ~ 30 nm for the pristine PVP (referred to as PVP) and cross-linked PVP (referred to as c-PVP-30) films, respectively. The cross-linker reduces the porosity of the dielectric. In addition, another set of thin and thick cross-linked PVP films with thicknesses of ~ 35 nm (referred to as c-PVP-35) and ~ 115 nm (referred to as c-PVP-115) respectively, were also prepared for the purpose of investigating the dominant source of instability in PVP-based devices. All the above materials were purchased from Sigma-Aldrich and used without any purification. The PVP dielectric films were baked for 1 h at 120 °C. Subsequently, a 60 nm thick pentacene (purchased from Tokyo Chemical Industrial Co. Ltd and used without any purification) layer was thermally evaporated onto the dielectric surfaces at a rate of 0.2 Å/s at room temperature. Top contact source/drain (40 nm) gold electrodes which define a channel length (L) and width (W) of 50 µm and 1000 µm, respectively were thermally evaporated onto the pentacene films of PVP and c-PVP-30 devices via a shadow mask. The c-PVP-35 and c-PVP-115 devices have channel length (L) and width (W) of 100 µm and 1000 µm, respectively.

Figure 6.1 is a schematic of the cross-sectional view of our OFET showing the various sources/mechanisms of hysteresis or instability in OFETs and MIS diodes. Mechanism (a) is usually attributed to electrons that are trapped to hydroxyl (OH) groups at the semiconductor-insulator interface, (b) is associated with dipole groups such as OH groups inside the polymer dielectric which can be slowly re-oriented by an applied electric field, and (c) is attributed to injected electrons from the gate electrode that are trapped inside a defect-filled dielectric [68]. The dielectric film thicknesses were measured with a reflectometer (Mprobe) and re-confirmed using ellipsometry (J. A. Woollam variable angle spectroscopic ellipsometer). The electrical characterization of the OFETs and metal-insulator-semiconductor (MIS) diodes were carried out under ambient conditions using Keithley 2400 and 236 source/measure units and the HP 4284A LCR meter, respectively.

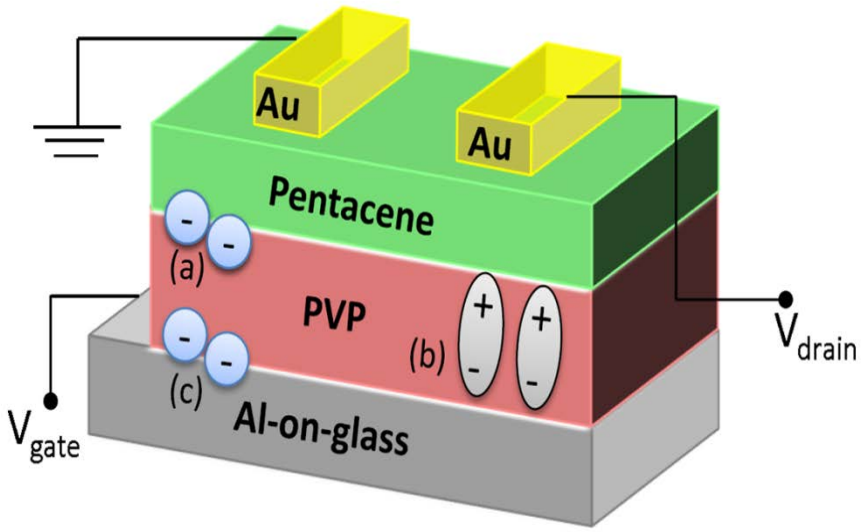

Fig. 6.1: Schematic cross-sectional view of OFET showing the various sources of instability arising from (a) semiconductor-insulator interface charges (b) slowly-polarizing dipole charges (c) gate-injected charges.

6.3 Results and discussion

6.3.1 Morphology of the dielectric films

The surface morphologies of PVP, c-PVP, and pentacene films on PVP and c-PVP are shown in Figs. 6.2(a-d). The surface of the PVP and c-PVP films were found to be

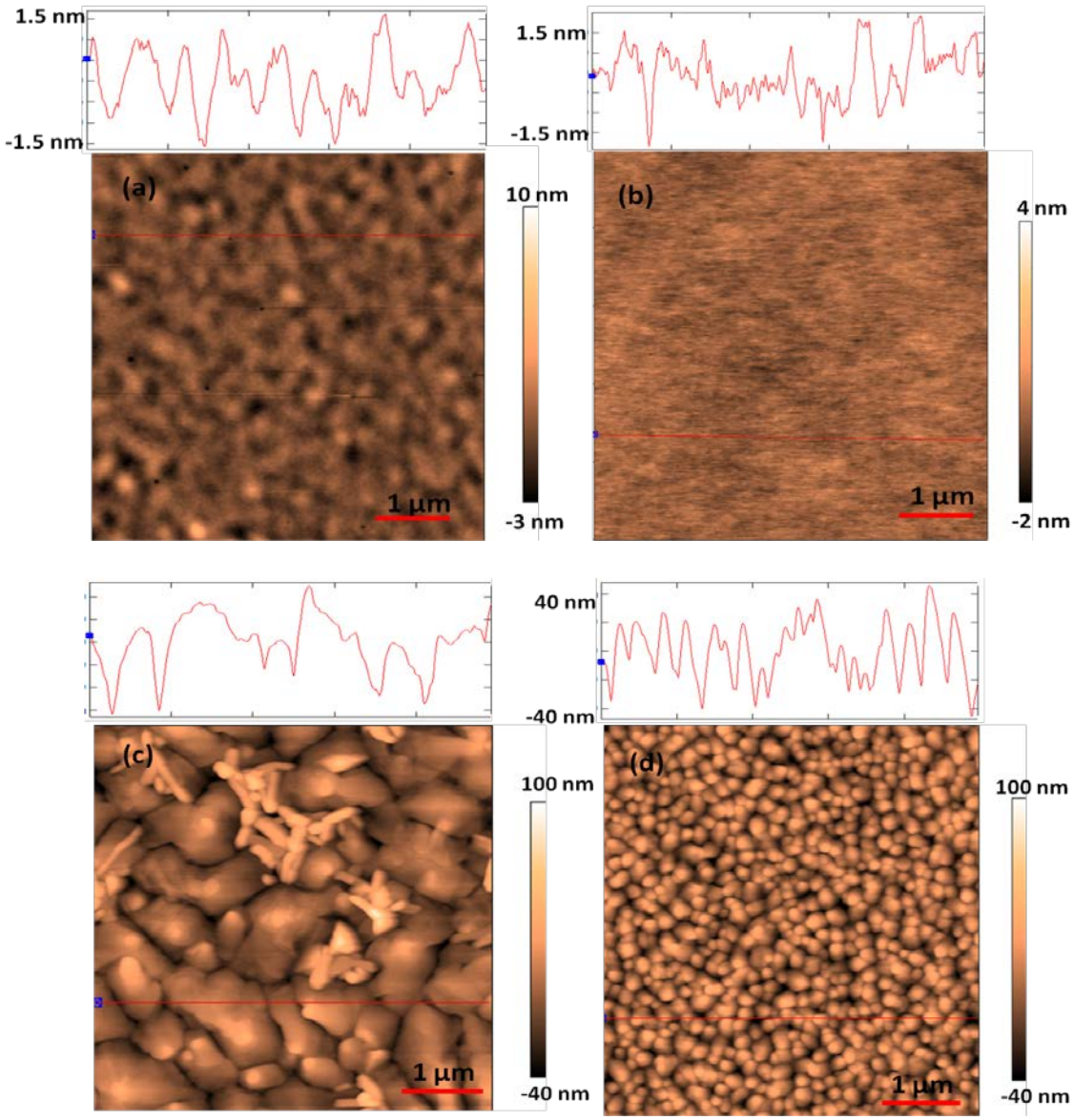

Fig. 6.2: Atomic force microscopy images of (a) PVP (b) c-PVP (c) pentacene on PVP and (d) pentacene on c-PVP dielectric films.

quite smooth with root-mean-square (rms) roughness values of 0.67± 0.02 nm and 0.26 ± 0.03 nm, respectively over a 5 µm × 5 µm area. The pentacene on PVP films exhibited typical dendritic structures with layer-by-layer formation and large grain sizes (~ 1 µm) unlike the pentacene on c-PVP exhibited island growth and smaller grain sizes even with a highly smooth c-PVP surface.

6.3.2 Surface energy and contact angles of the dielectric films

In order to properly understand the dominant source(s) of hysteresis in our devices, surface properties of our thin (30 nm ≤ thickness ≤ 80 nm) and thick (> 100 nm) dielectrics were characterized by determining the surface energies and water contact angles. Surface energy was determined from the contact angle measurement using distilled water, formamide, and diiodomethane as probe liquids. Representative thin dielectric (c-PVP-35) showed a water contact angle of ~ 59.4° and surface energy of ~ 54.6 mJ/m^2 compared to the thick c-PVP-115 dielectric which exhibited a higher water contact angle of ~ 69.7° and a lower surface energy of ~ 41.7 mJ/m^2. The above results suggest that the surfaces of the thin dielectrics were more hydrophilic than the thick dielectric possibly due to the presence of a higher density of polar OH groups [50].

6.3.3 MIS diode characteristics

Figure 6.3 shows the capacitance-voltage (C-V) scans from accumulation (negative gate bias) to deep depletion (positive gate bias) carried out on c-PVP-30, PVP, c-PVP-115 MIS diodes. From the C-V curves, flat band voltages (V_{FB}) of -0.6 ± 0.05, -0.1 ± 0.03, and 3.5 ± 0.09 V were extracted for the c-PVP-30, PVP, and c-PVP-115 MIS diodes, respectively. The difference in the metal and semiconductor work functions (ϕ_{ms}) and

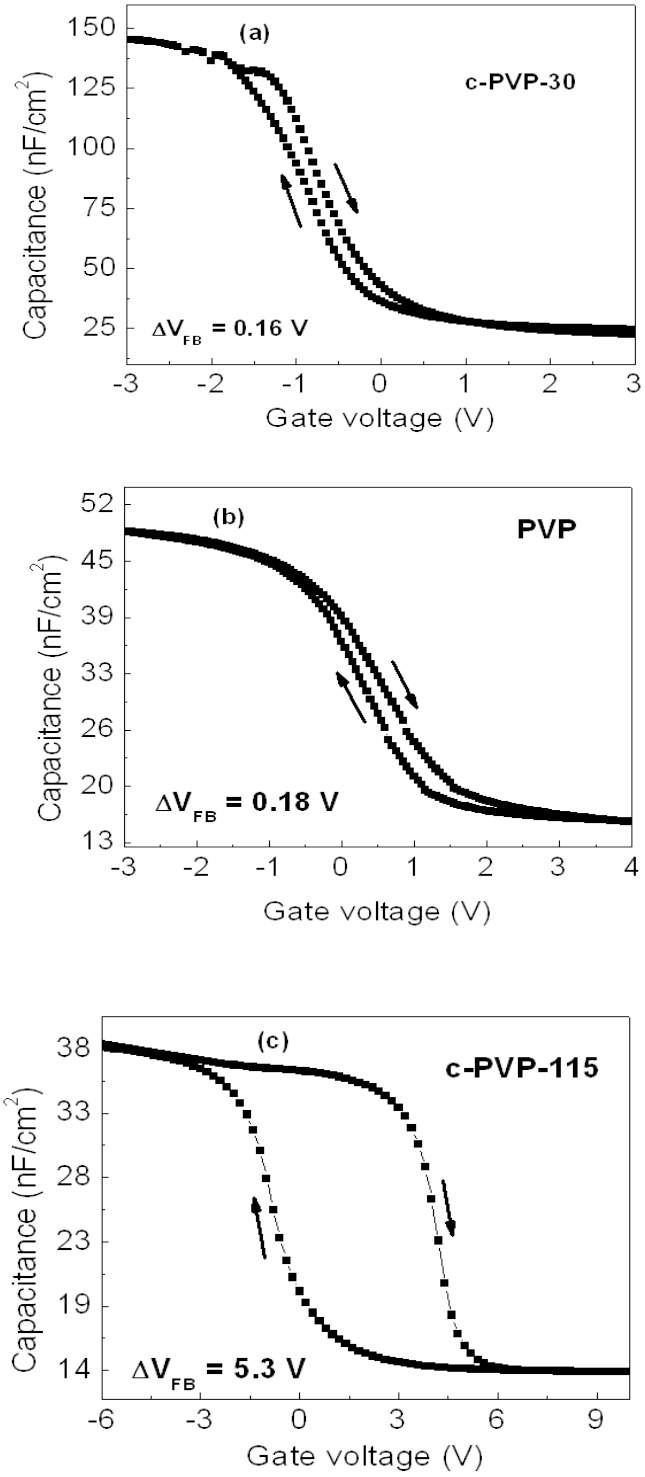

Fig. 6.3: Capacitance-voltage characteristics of (a) c-PVP-30 (b) PVP and (c) c-PVP-115 MIS diodes at 5 kHz.

the existence of positive interface charges (Q_i) at the semiconductor-insulator interface are known to be responsible for negative V_{FB} in MIS diodes as given by Eq. 4.2. The positive occurrence of V_{FB} in the thick c-PVP-115 MIS diode may be due to the existence of negative interface charges at its semiconductor-insulator interface. The C-V measurements were carried out by sweeping the gate bias continuously from negative bias to positive bias and back in order to estimate the extent of hysteresis originating from the bulk and/or interface trapped charges. Hysteresis characterized by a shift in flat band voltage (ΔV_{FB}) was estimated to be 0.16, 0.18, and 5.3 V for the c-PVP-30, PVP, and c-PVP-115 MIS diodes, respectively. Our thin MIS diodes show ΔV_{FB} values that are about two orders of magnitude less than observed values in other pentacene MIS diodes with pristine and cross-linked PVP dielectrics [69,59].

Hysteresis/instability in OFETs and MIS diodes incorporating polymeric gate dielectrics are believed to be due to (1) the existence of negative charge trappings by hydroxyl (OH) groups at the semiconductor-insulator interface, (2) slow polarization of dipole groups or molecules like OH groups inside the polymer dielectric by an applied electric field, and (3) charge injection from the gate into the dielectric and subsequent trapping [70,71]. An equivalent parallel conductance (G_p) extracted at different biases from the measured capacitance and conductance data within the depletion region is employed to estimate the density of interface traps, D_{it} (Fig. 6.4) using the continuum of states model (Eq. 2.17). From Fig. 6.4c, the thick c-PVP-115 MIS diode exhibited the

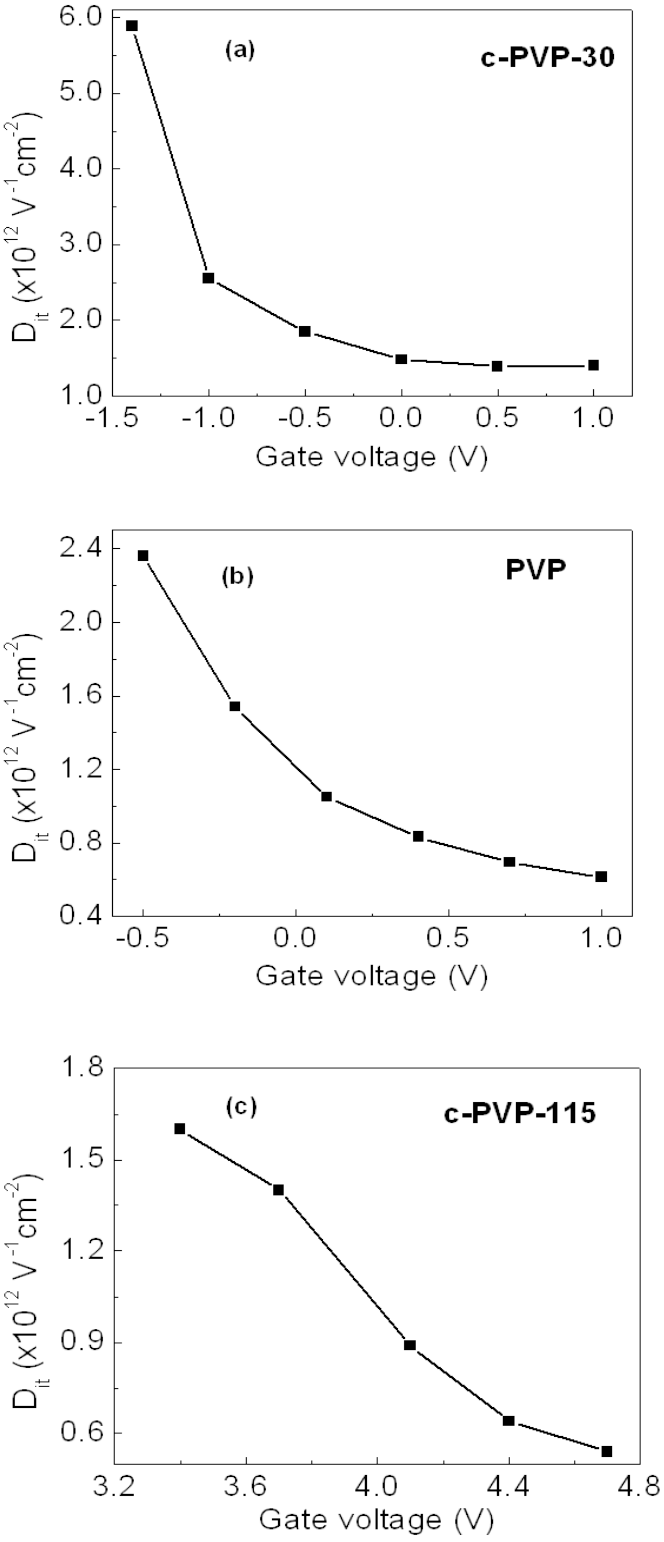

Fig. 6.4: Capacitance-voltage characteristics of (a) c-PVP-30 (b) PVP and (c) c-PVP-115 MIS diodes at 5 kHz.

least D_{it}, consistent with the results of the surface energy and water contact angle measurements which showed its surface to be the least polar; however, it still exhibited the largest hysteresis with a shift in V_{FB} (ΔV_{FB}) of 5.3 V. This observation indicates that charge trapping at the semiconductor-insulator interface is not the dominant cause of hysteresis in these devices; rather, it is dominated by slow polarization of dipole OH groups (increases with polymer dielectric thickness) inside the PVP dielectric and charge injection from the gate electrode (increases with gate voltage) into the PVP dielectric [70,71], schematically shown in Fig. 6.1.

6.3.4 FET characteristics

Figure 6.5 shows the output characteristics of c-PVP-30 and PVP OFETs. The devices exhibit excellent linear and saturation behaviors and could be operated within -2 V. Also shown in Fig. 6.6 are the corresponding transfer characteristics. Noticeable from the inset of Fig. 6.6a is the presence of hysteresis in the c-PVP-30 OFET; though with a small threshold voltage shift (ΔV_T) of 0.35 V. We estimate a carrier mobility (μ) of 1 cm^2/Vs, a threshold voltage (V_T) of -1 ± 0.02 V, an on/off current ratio ($I_{on/off}$) of 10^4, and based on the measured subthreshold slope (S) of 192 mV/decade, a maximum trap density ($N_{\max}^{trap}$) of 9.4 x 10^{11} cm^{-2} [72] for the c-PVP-30 OFET. The PVP OFET (inset of Fig. 6.6b) shows no obvious hysteresis as evidenced by a negligible ΔV_T of 0.07 V; we estimate a μ of 0.03 cm^2/Vs, a V_T of -0.8 ± 0.02 V, and an $I_{on/off}$ of 4.7 x 10^2 and from the measured S of 561 mV/decade, an $N_{\max}^{trap}$ of 3.1 x 10^{11} cm^{-2}. Our estimated values for $N_{\max}^{trap}$ are comparable to other reported values obtained for OFETs incorporating hydrophobic CYTOP dielectric

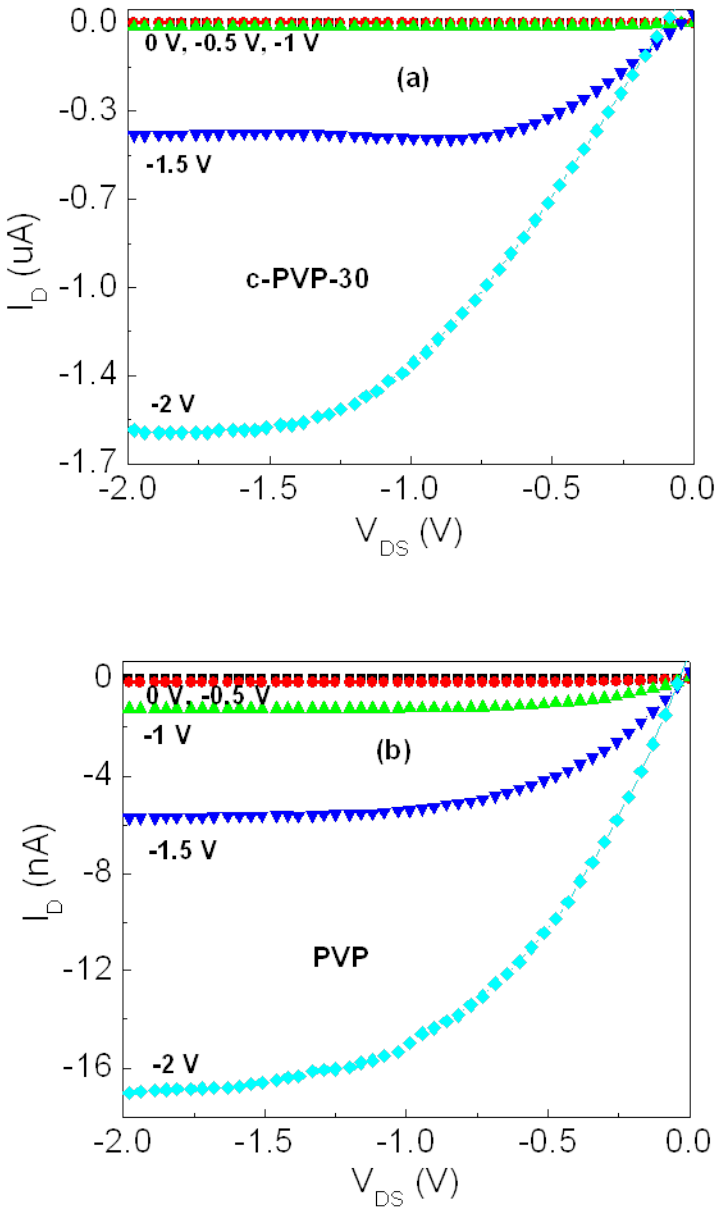

Fig. 6.5: Output characteristics of (a) c-PVP-30 and (b) PVP OFETs.

layers [73].

The improvement in performance in the c-PVP-30 OFET compared to the PVP OFET may be due to a reduction in the porosity of the c-PVP dielectric caused by the presence of the cross-linker. The estimated ΔV_T values for our OFETs are negligible

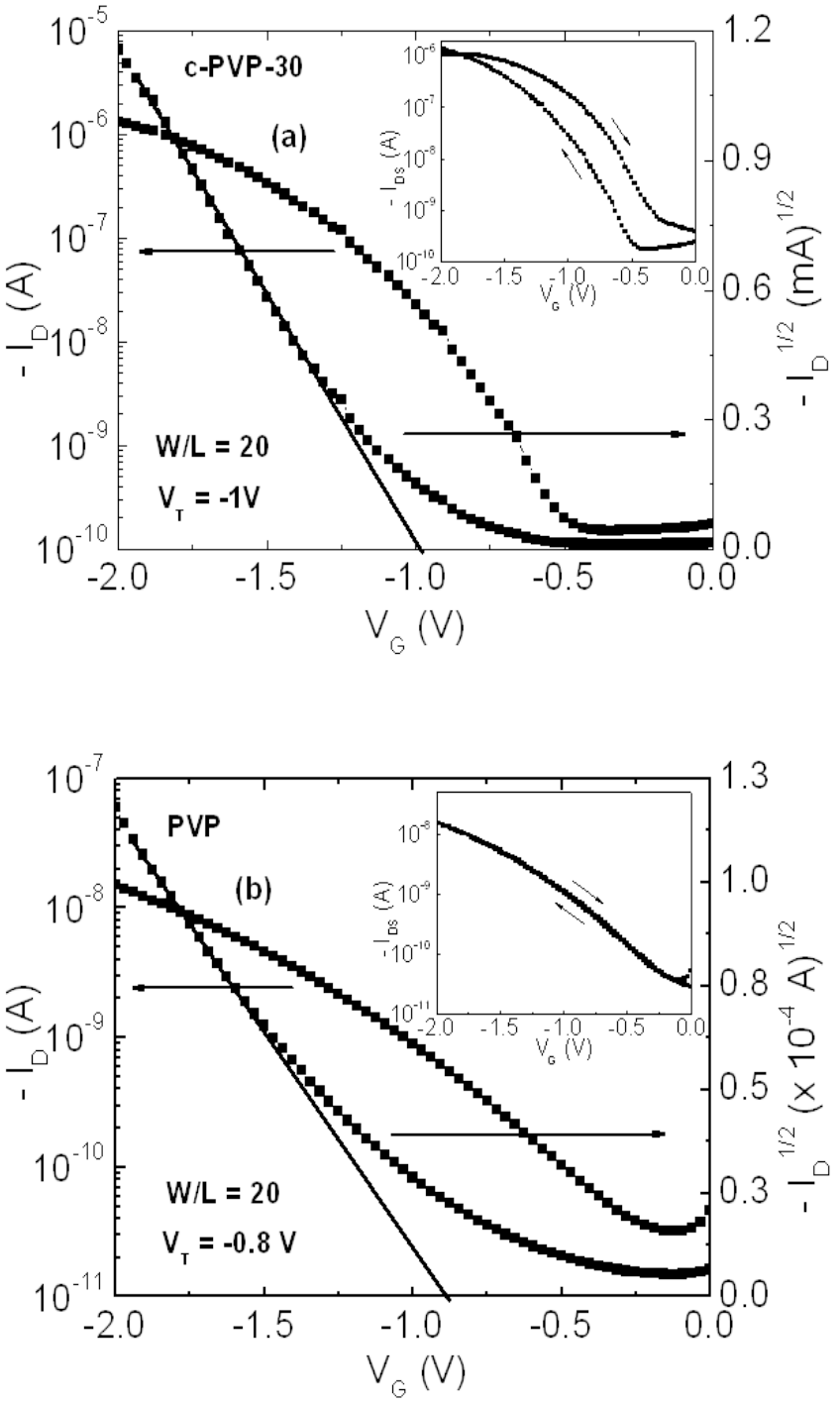

Fig. 6.6: Transfer characteristics of (a) c-PVP-30 and (b) PVP OFETs. Insets: Forward and backward sweeps of transfer characteristics.

compared to other reported values for pentacene OFETs incorporating pristine and cross-linked PVP [74,59]. The condensation reaction that occurs during curing between the hydroxyl groups of PVP and hydrogen or methyl group of PMMF on cross-linking, has been reported to result in the removal of OH and reduction in hysteresis in OFETs incorporating thick PVP dielectric [59,74]. In this work, both the pristine and cross-linked low-operating voltage OFETs exhibit reduced hysteresis with the pristine device even showing better stability – an indication that the use of thin PVP dielectric layer with consequent low voltage operation may be a more robust means of reducing OFET hysteresis. Hence, we conclude that observed stability in our devices is likely an indication of (1) a diminished density of slowly polarizing dipole OH groups in the OFETs made possible by the use of thin PVP dielectric films, and (2) a reduced charge injection into the dielectric from the gate electrode due to the low-voltage operation.

To further test the operational stability of our OFETs critical for practical electronic circuit design, bias-stress measurements – a situation where excess charges induced by the gate electric field fall into trap states with increase in stress time, were carried out on our OFETs. Bias stress effect is usually manifested in OFET hysteresis and/or a shift in threshold voltage [75]. To do this, we applied a constant direct current (dc) bias stress for 2 h (V_G = V_{DS} = -2 V) to our OFETs after which we immediately measured the current-voltage (I-V) transfer characteristics. Figure 6.7(a-b) shows the transfer characteristics of the c-PVP-30 and PVP OFETs before and after 2 h of bias stress.

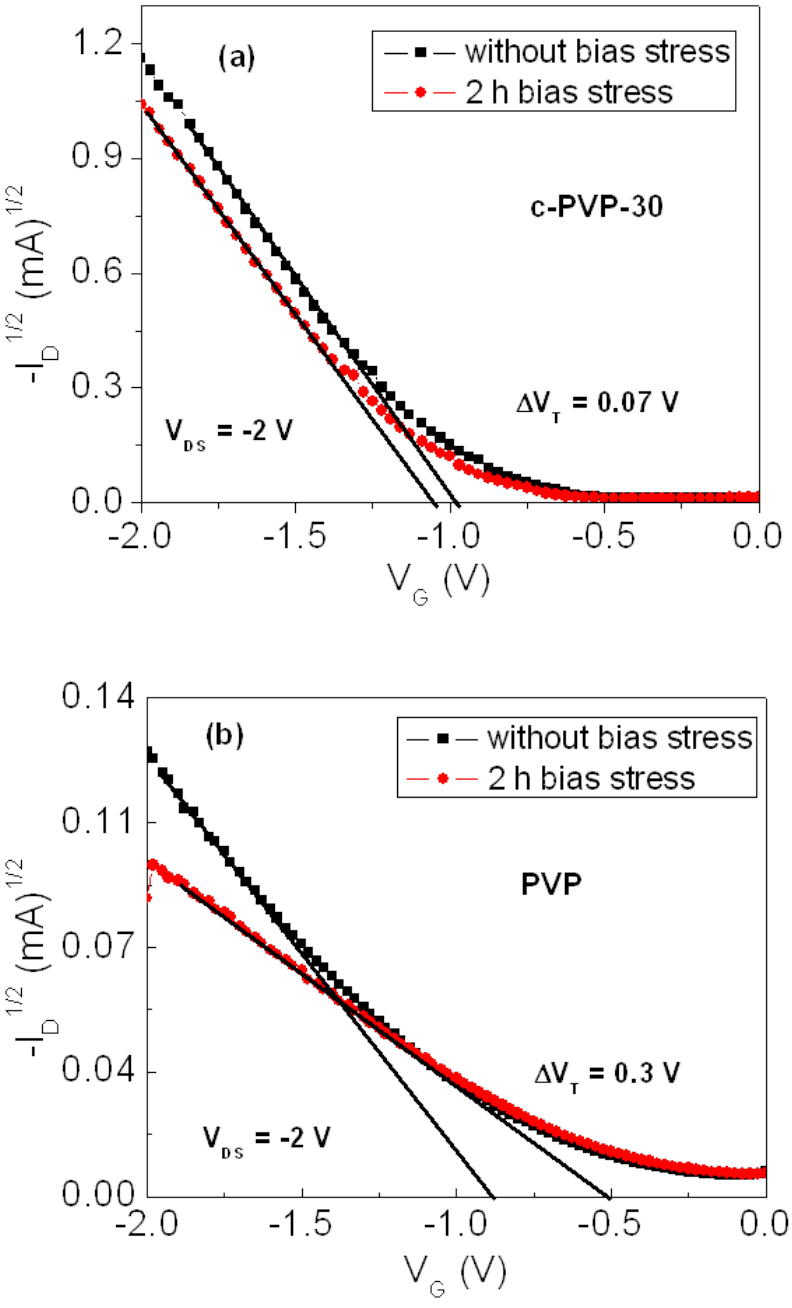

Fig. 6.7: Transfer characteristics of OFETs before and after bias stress (a) and (b). Bias stressing and measurements were carried out under ambient conditions.

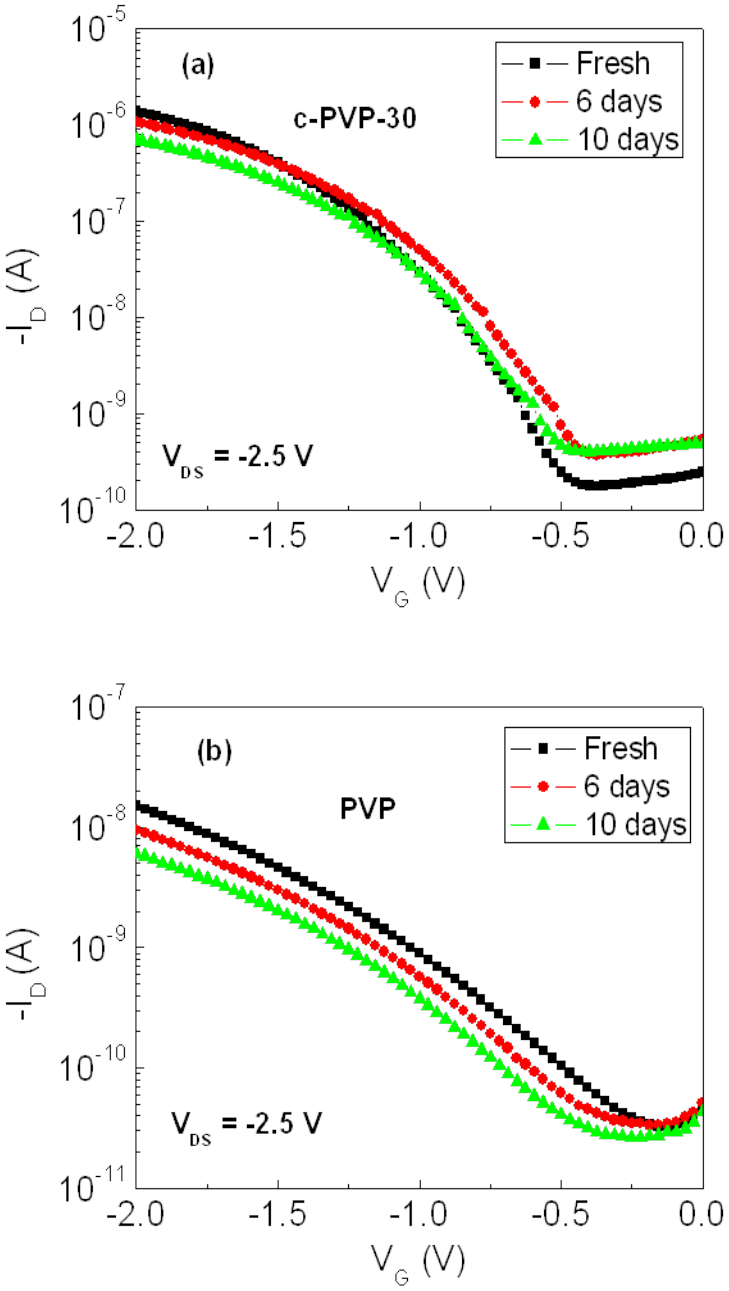

Fig. 6.8: Transfer characteristics of OFETs over a 10-day period of air exposure (c) and (d).

As is observable from Fig. 6.7a, the c-PVP-30 OFET exhibits a remarkable V_T stability with a negligible ΔV_T of 0.07 V and a slight decrease of μ from 1 cm^2/Vs to 0.9 cm^2/Vs. For the

PVP OFET (Fig. 6.7b), V_T shifted by only 0.3 V and μ slightly decreased from 0.03 cm^2/Vs to 0.01 cm^2/Vs after 2 h.

In order to study the environmental stability, the OFETs were exposed to normal ambient conditions for 10 days with changes in V_T, S, μ, and $I_{on/off}$ monitored. The results of the changes in the various parameters of the devices are summarized in Table 1. In the c-PVP-30 OFET, V_T positively shifted negligibly from -1 ± 0.02 V to -0.8 ± 0.06 V, μ decreased from 1.0 to 0.54 cm^2/Vs, S increased from 192 to 398 mV/decade, and $I_{on/off}$

Table 6.1: Summary of performance parameters of OFETs after 10 days of air exposure.

Sample	Time (days)	Capacitance (C_i) ($nFcm^{-2}$)	Threshold voltage (V_T) (V)	ΔV_T (V)	Mobility (μ) (cm^2/Vs)	Threshold slope (S) (V/decade)	Current On/off ($I_{on/off}$)
c-PVP	0	150	-0.98	0.35	1	0.19	10^4
	10	94	-0.84	0.30	0.54	0.39	$2.4x10^3$
PVP	0	52	-0.88	0.07	0.03	0.56	$4.7x10^2$
	10	49	-0.82	0.02	0.01	0.53	$4.9x10^2$

decreased from 10^4 to 2.4 x 10^3 after 10 days of air exposure. The increase in S may be related to the reduction in C_i from 150 nF/cm^2 to 94 nF/cm^2. The decrease in $I_{on/off}$ is due to the decrease in the on current from 1.34 μA to 0.7 μA and an increase in the off current from 0.18 nA to 0.62 nA (Fig. 6.8a), possibly caused by the diffusion of oxygen into the semiconductor. In the PVP OFET, V_T varied negligibly from -0.8 ± 0.02 V to -0.9 ± 0.03 V, μ decreased from 0.03 to 0.01 cm^2/Vs, S decreased from 561 to 534 mV/decade,

and $I_{on/off}$ hardly changed after 10 days of air exposure. We note that for this device the capacitance hardly changes. The negligible change in $I_{on/off}$ is traceable to the decrease

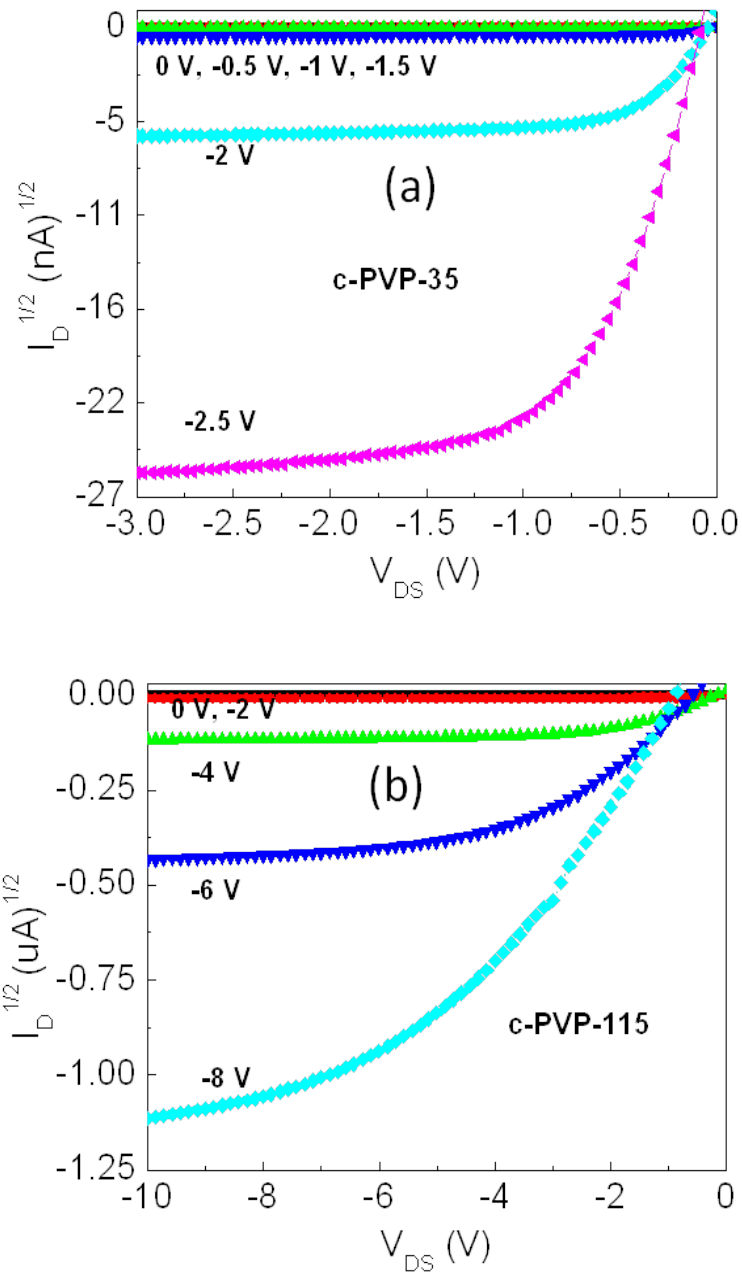

Fig. 6.9: Output characteristics of (a) c-PVP-35 and (b) c-PVP-115 OFETs.

in the on-current from 15 nA to 6.0 nA and a negligible decrease in the off-current from 47 pA to 44 pA as seen in Fig. 6.8b. As seen from Table 6.1, our low-operating voltage OFETS exhibit good air stability attributable to a diminished density of hydroxyl groups

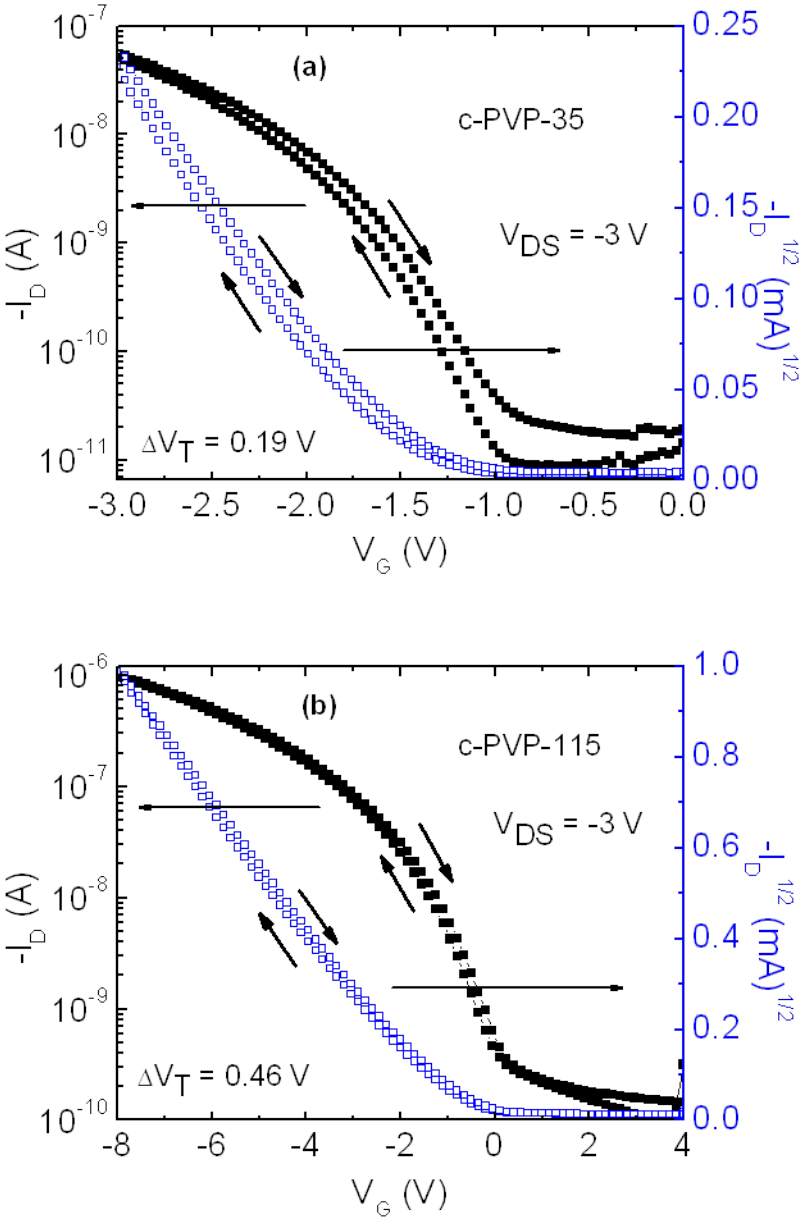

Fig. 6.10: Transfer characteristics of (a) c-PVP-35 and (b) c-PVP-115 OFETs.

inside the thin PVP dielectrics and reduced charge carrier injection from the gate. ΔV_T in our OFETs are about two orders of magnitude less than reported values for OFETs incorporating hydrophobic CYTOP dielectric layers with comparable period of air exposure [73].

To further investigate the influence of PVP dielectric thickness and low-operating voltage in OFET hysteresis/stability, we fabricated and characterized another set of OFETs using thin (c-PVP-35) and thick (c-PVP-115) PVP dielectric films. Although the c-PVP-35 OFET exhibited a lower drain saturation current when compared with the c-PVP-30 OFET, its operating voltage is quite as low (< -3 V) with distinct linear and saturation regions (Fig. 6.9a). This is unlike the c-PVP-115 device which hardly saturates even with a higher gate voltage (Fig. 6.9b). The c-PVP-35 OFET also exhibits a higher V_T stability with a negligible V_T shift of 0.19 V (Fig. 6.10a) and a low leakage current of 14.3 pA compared with a V_T shift of 0.46 V and high leakage current of 283 pA for the c-PVP-115 OFET (Fig. 6.10b). Considering that the surface of the c-PVP-115 dielectric was less hydrophilic than that of the c-PVP-115 OFET, with a possible lower density of surface hydroxyl groups, the increase in ΔV_T and gate leakage current in the thick c-PVP-115 OFET are not due to charge trappings by surface hydroxyl groups at the semiconductor-insulator interface; rather, they are believed to be due to increased PVP thickness resulting in increase in the density of slowly polarizing hydroxyl groups inside the bulk polymer dielectric, which also causes a deterioration of the polymer dielectric. The high gate voltage operation could have also given rise to an increased injection of charge carriers from the gate with subsequent trapping in the bulk dielectric.

Again, in order to investigate the reproducibility and operational stability of the OFETs, bias stress measurements were carried out. Here, I-V transfer characteristics

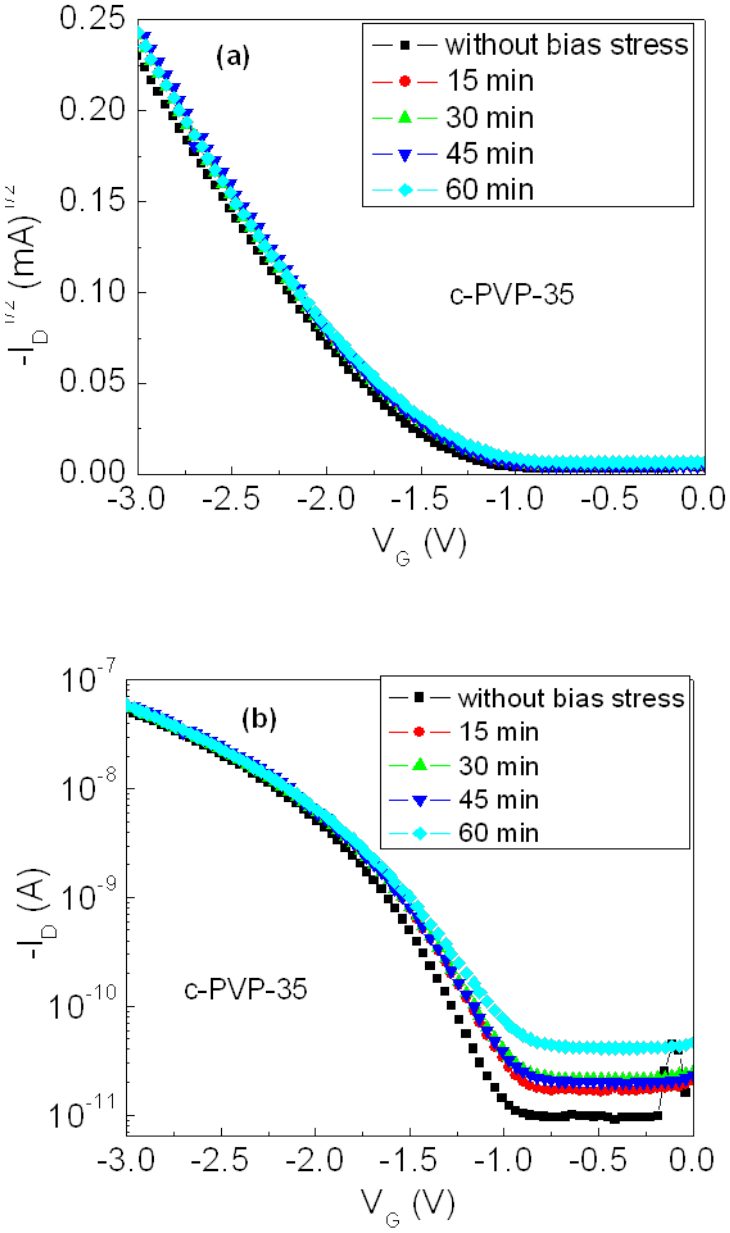

Fig. 6.11: Operational stability of transfer characteristics of (a) c-PVP-35 OFET and (b) c-PVP-115 OFET after bias stress at $V_G = V_{DS} = -3$ V at varying stress times.

were first measured without applying any bias stress. Subsequently, bias stress ($V_G = V_{DS}$ = -3 V) and ($V_G = V_{DS}$ = -8 V) were applied to the c-PVP-35 (Fig. 6.11) and c-PVP-115 OFETs (Fig. 6.12), respectively for set times and the I-V transfer characteristics were

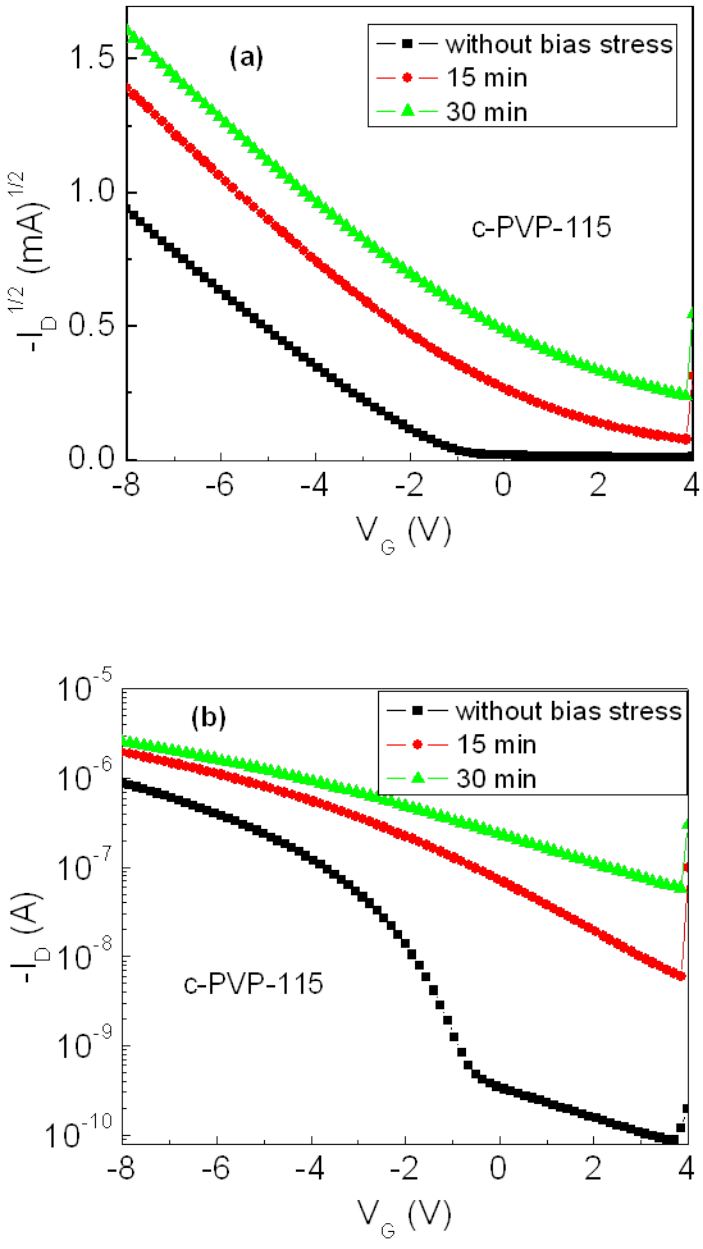

Fig. 6.12: Operational instability of transfer characteristics of (a) c-PVP-35 OFET and (b) c-PVP-115 OFET after bias stress at $V_G = V_{DS}$ = -8 V, respectively at varying stress times.

measured after each set time. In all, the c-PVP-35 and c-PVP-115 OFET were subjected to 9000 s and 2700 s of dc bias stress, respectively. While the c-PVP-115 OFET suffered pronounced operational instability and broke down after just 2700 s of bias stress, the c-PVP-35 OFET remained stable with no change in the I-V curves, zero shift in V_T, and a small increase in leakage current from 22 pA to 46 pA after 9000 s of bias stress (Fig. 6.11b) - a pointer to bulk-related rather than interface-related nature of the hysteresis/instability considering again, the results of the contact angle and surface energy measurements. As such, we conclude that the most obvious sources of operational stability in our c-PVP-35 OFET just like in our c-PVP-30 and PVP OFETs, are the reductions in both dipole OH groups inside the PVP dielectric and gate operating voltage with consequent reduction in charge injection and trapping - all of which are traceable to the use of thin PVP dielectric layers.

6.4 OFETs and MIS Diodes with DMSO-dissolved PVP layer

As a validation of the universality of this technique of achieving high yield, stable, and low-operating voltage devices incorporating low-*k* polymeric dielectrics dissolved in high dipole moment and high-*k* solvents, we fabricated OFETs and MIS diodes using pristine PVP dissolved in dimethyl sulfoxide (DMSO) (~ 50 nm) as the gate dielectric. As could be seen in Table 2.1, DMSO was used here considering that it has dipole moment and dielectric constant values comparable to PC and as such, is a good candidate for achieving low-operating voltage devices just like PC. The fabrication and experimental procedures are same as earlier described for the PC-dissolved PVP devices and the results are shown in Fig. 6.13. Capacitance-voltage measurements from an MIS device

(Fig. 6.13a) show a typical p-type behavior and the device exhibits almost no hysteresis (no flat band voltage, V_{FB}, shift) when the gate bias is continuously swept from -4 V to 3 V at a step voltage of 0.05 V. Fig. 6.13b shows the conductance-voltage (G-V) characteristics of the MIS diode. The device undergoes a bias-dependent loss as evidenced by the presence of conductance peaks. The obvious conductance peaks also suggest that the loss is dominated by interface trap states.

The OFETs exhibit clear current modulation with distinct linear and saturation regimes (Fig. 6.13c) and could be operated below -3 V. From the transfer characteristics (Fig. 6.13d) obtained from the saturation regime, we estimate a high carrier mobility (μ)

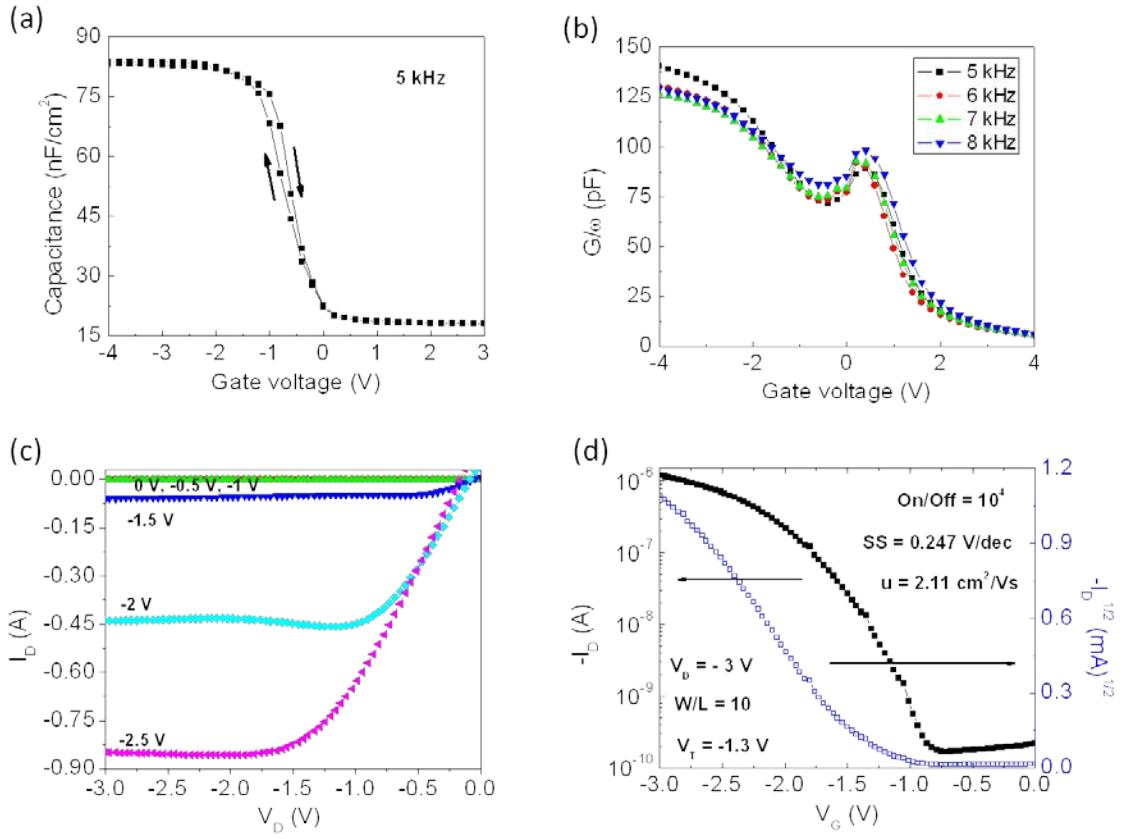

Fig. 6.13: (a) C-V characteristics of MIS diode at 5 kHz (b) G-V curves of MIS diode (c) Output and (d) Transfer characteristics of OFET.

of 2.11 cm^2/Vs, a threshold voltage (V_T) of -1.3 V, an on/off current ratio ($I_{on/off}$) of 10^4, and a small subthreshold slope of 0.247 V/decade. From the results above, dissolution of PVP polymer dielectric in DMSO results in high-quality and low-thickness gate dielectric layers necessary for high mobility and low-operating voltage OFETs and MIS diodes similar to PC-dissolve PVP observations. Considering the very high field-effect mobility of OFETs incorporating PVP dissolved in DMSO compared to PC, it could be argued that dissolving PVP in DMSO results in a more improved pentacene-PVP interface.

6.5 Hybrid Bilayer Devices

Building on the successes of PC-dissolved crosslinked PVP in achieving low operating voltage and stable devices, we fabricated PVP/SiO_2 hybrid OFETs and MIS

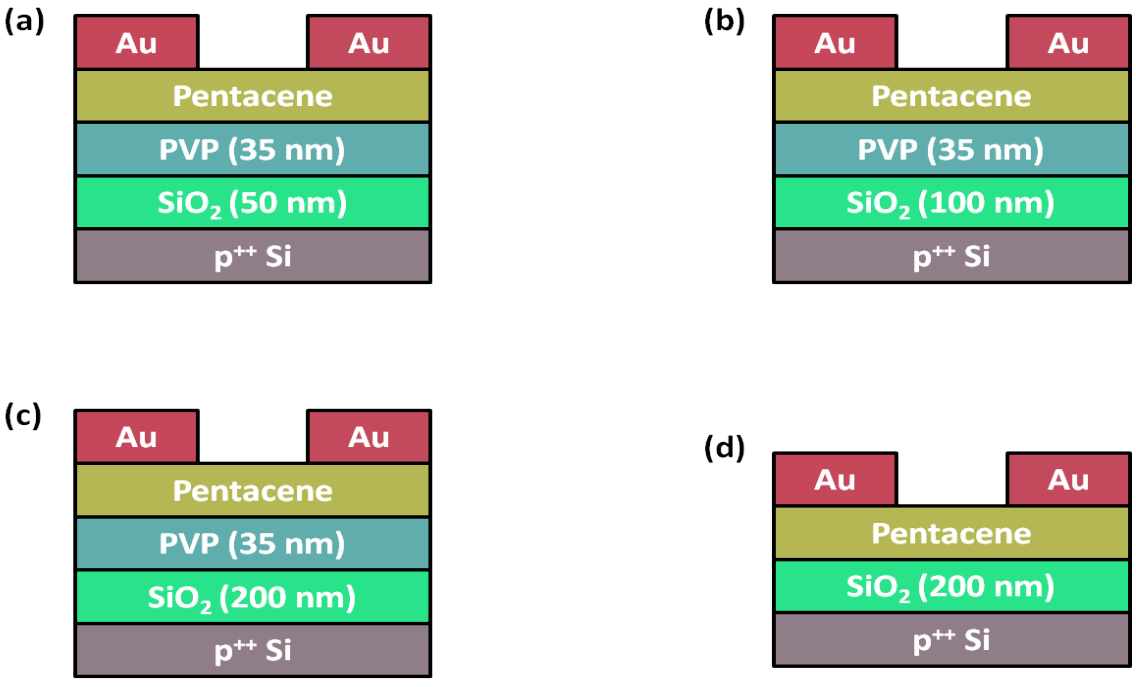

Fig. 6.14: Schematic cross-sectional view of OFETs.

diodes and investigated the effect of low-*k* cross-linked PVP buffer layer on the operating voltage and stability of these SiO_2-based OFETs and MIS diodes. Fig. 6.14 shows schematic cross-sectional views of the OFETs used for this investigation. OFETs and MIS diodes with top-contact and bottom-gate architectures were made on heavily p-doped silicon wafers with 50 nm, 100 nm, and 200 nm-thick SiO_2, respectively . For reference, OFETs were made on 200 nm-thick SiO_2 without any PVP layer. A PVP polymer dielectric film with a thickness of ~ 35 nm was deposited by spincoating on the

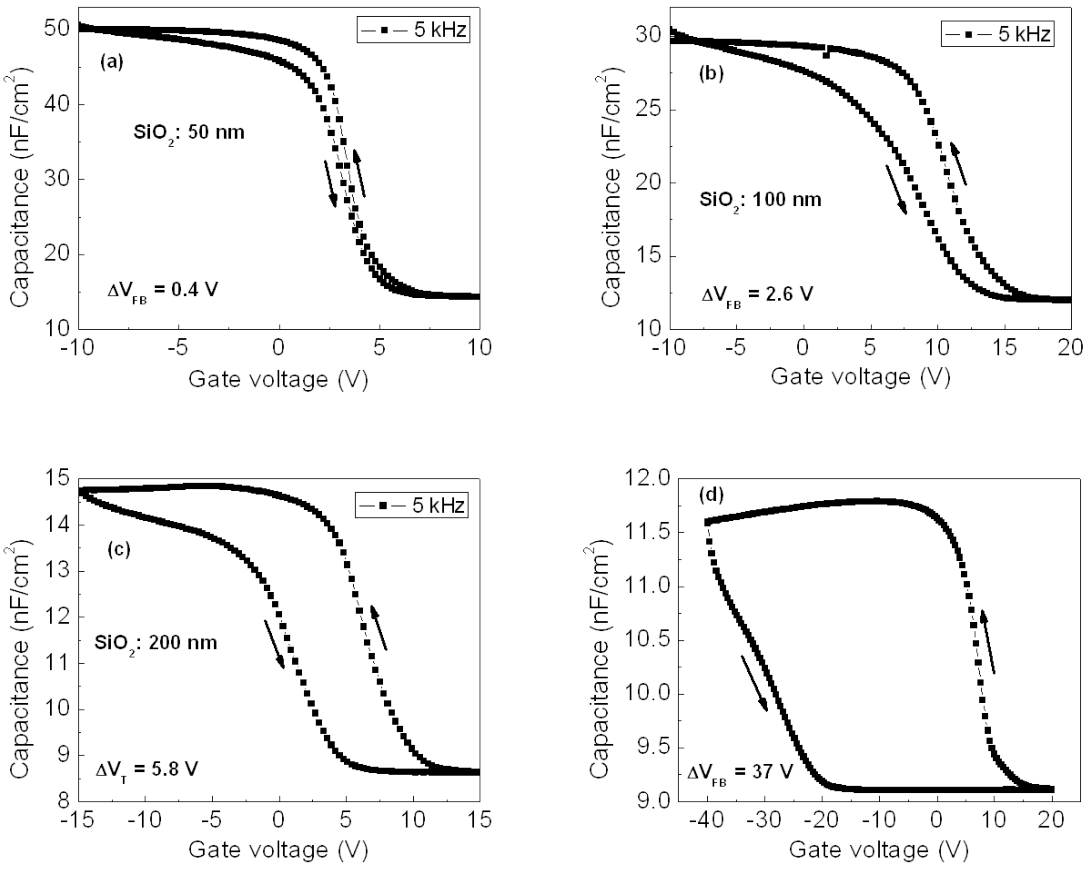

Fig. 6.15: Capacitance-voltage characteristics of (a) PVP/SiO_2 (50 nm) (b) PVP/SiO_2 (100 nm) (c) PVP/SiO_2 (200 nm) and (d) SiO_2 (200 nm) MIS diodes at 5 kHz.

SiO_2 substrates and then cured for 1 h at 100 °C. A 60 nm-thick semiconducting pentacene layer was then evaporated onto the substrates. The fabrication of the transistors were completed by depositing 40 nm-thick gold source/drain electrodes through a shadow mask to define the channel (width/length = 500 μm/50 μm). Electrical characterizations of the OFETs and MIS diodes were carried out under ambient conditions.

Figure 6.15 shows the capacitance-voltage (C-V) scans from PVP/SiO_2 (50 nm), PVP/SiO_2 (100 nm), PVP/SiO_2 (200 nm), and SiO_2 (200 nm) MIS diodes. The C-V measurements were carried out by sweeping the gate bias continuously from negative bias to positive bias and back in order to estimate the extent of hysteresis originating from the bulk and/or interface trapped charges. Hysteresis characterized by a shift in flat band voltage (ΔV_{FB}) was estimated to be 0.4, 2.6, 5.8, and 37 V for the PVP/SiO_2 (50 nm), PVP/SiO_2 (100 nm), PVP/SiO_2 (200 nm), and SiO_2 (200 nm) MIS diodes, respectively. While hysteresis is low in the hybrid devices and observed to increase with an increase in SiO_2 thickness, it is an order of magnitude higher in the bare SiO_2 MIS diode. Clearly, the hysteresis is related to charge trappings in the bulk SiO_2. Interestingly, our hybrid and SiO_2-based MIS diodes exhibit counter-clockwise hysteresis loop direction in contrast to the clockwise direction earlier observed in cross-linked PVP MIS diodes. As such, the reduction in hysteresis in the hybrid devices could be the result of a net compensating effect of the two contrasting hysteresis directions from the polymer dielectric buffer and SiO_2 dielectrics.

A summary of the electrical characteristics of the OFETs is shown in Table 6.2. From the output characteristics, the hybrid OFETs are observed to exhibit better

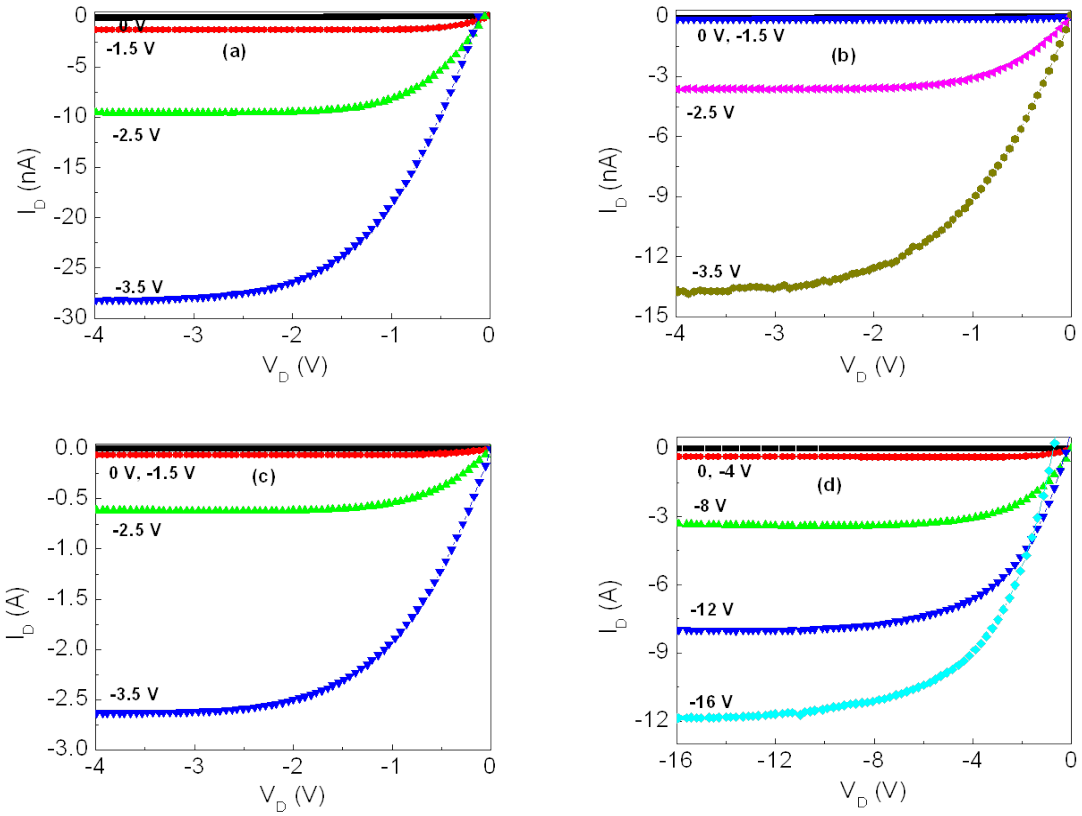

Fig. 6.16: Output characteristics of (a) PVP/SiO_2 (50 nm) (b) PVP/SiO_2 (100 nm) (c) PVP/SiO_2 (200 nm) and (d) SiO_2 (200 nm) OFETs.

current modulation and low voltage operation compared to bare SiO_2 OFET. Figure 6.16a-d show that OFETs with PVP layers operate below -4 V, while the OFET on bare SiO_2 operates at a higher voltage of -16 V. The reduction in operating voltage in the hybrid OFETs may not be attributed entirely to their high insulator capacitance density (C_i) considering that PVP/SiO_2 (200 nm) and SiO_2 (200 nm) OFETs have close C_i values of 14.5 and 11.5 nF/cm^2 (Fig. 6.15c-d), respectively. Leakage current was found to increase with a decrease in SiO_2 thickness with observed on/off current ratios of 1 x 10^2, 2.9 x

10^2, 3 x 10^3, and 6.6 x 10^3 for PVP/SiO_2 (50 nm), PVP/SiO_2 (100 nm), PVP/SiO_2 (200 nm), and SiO_2 (200 nm), respectively. The hybrid OFETs exhibited no obvious

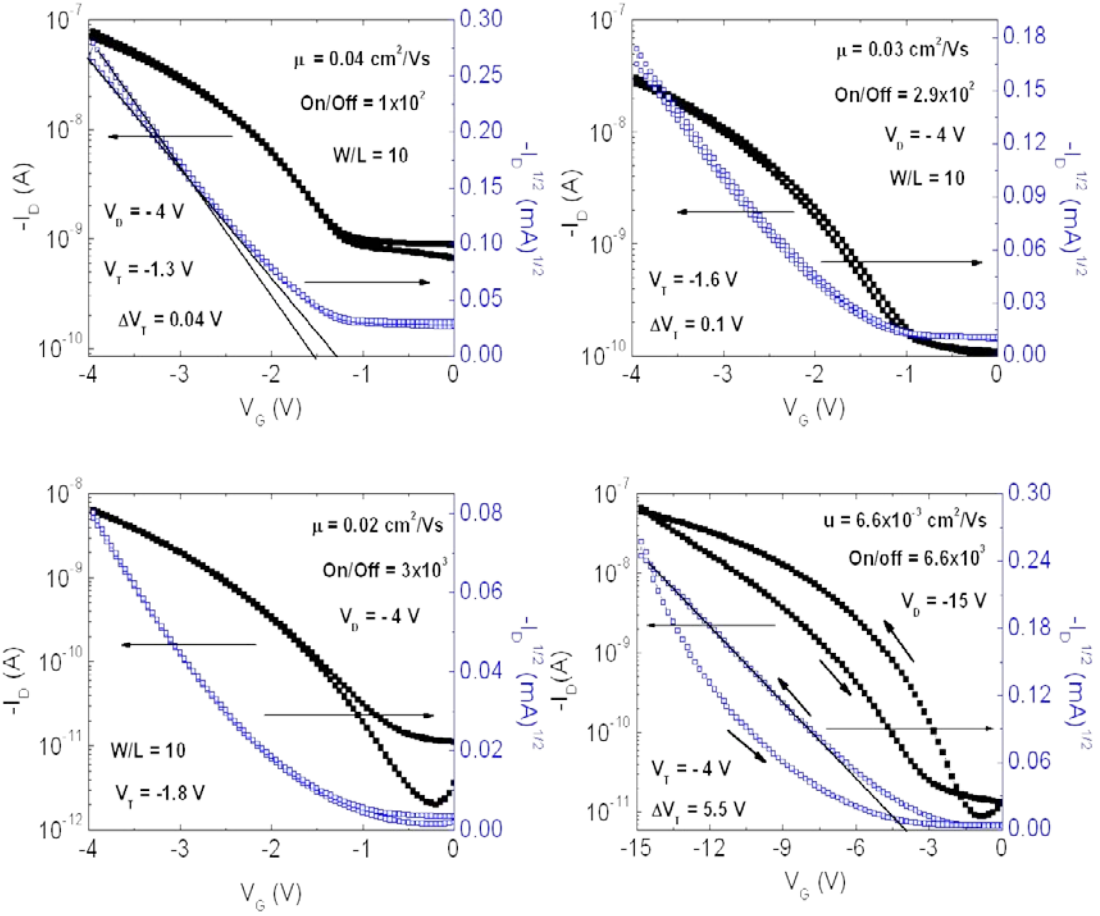

Fig. 6.17: Transfer characteristics of (a) PVP/SiO_2 (50 nm) (b) PVP/SiO_2 (100 nm) (c) PVP/SiO_2 (200 nm) and (d) SiO_2 (200 nm) OFETs.

hysteresis/threshold voltage shifts and a field-effect mobility of 0.03 ± 0.01 cm^2/Vs (Fig. 6.17a-c), in contrast to the bare SiO_2 OFET which exhibited a noticeable hysteresis/threshold voltage shift of 5.5 V and a lower mobility of 0.006 cm^2/Vs. Again, as was observed in the MIS diodes, hysteresis in cross-linked PVP gate dielectric OFETs (earlier results) exhibited hysteresis loops that are in opposite direction to the hysteresis in these hybrid and bare SiO_2 OFETs. This indicates that the reduced hysteresis in the

hybrid OFETs may be a net compensating effect from the PVP and SiO_2 dielectrics. A similar observation has been made in Cytop/Al_2O_3 hybrid OFETs and was attributed to

Table 6.2: Summary of performance parameters of (a) PVP/SiO_2 (50 nm) (b) PVP/SiO_2 (100 nm) (c) PVP/SiO_2 (200 nm) and (d) SiO_2 (200 nm) OFETs.

Sample	Threshold voltage (V_T) (V)	ΔV_T (V)	Mobility (μ) (cm^2/Vs)	Current On/off ($I_{on/off}$) (A)	Gate voltage (V_G) (V)
PVP/SiO_2 (50 nm)	-1.3	0.04	0.04	1×10^2	< -4
PVP/SiO_2 (100 nm)	-1.6	0.1	0.03	2.9×10^2	< -4
PVP/SiO_2 (200 nm)	-1.8	~ 0	0.02	3×10^3	< -4
SiO_2 (200 nm)	-4	5.5	0.007	6.6×10^3	< -15

the compensating effects arising from filling of deep traps and simultaneous dipolar orientation at the Cytop/Al_2O_3 interface and/or charge injection from the gate electrode [73]. The low gate voltage operation of the hybrid OFETs and the consequent reduction in charge injection from the gate into the SiO_2 dielectric could also have contributed to their excellent operational stability.

6.6 Conclusion

In summary, we have fabricated low-operating voltage (within -2 V) organic field-effect transistors employing thin pristine and cross-linked PVP dielectric layers with remarkable threshold voltage stability under gate bias stress and in air. We also fabricated another OFET employing thick cross-linked PVP layer which exhibited obvious electrical instability and gate leakage current, thereby confirming the dominance of dielectric bulk-related instabilities in polymer field-effect transistors. The use of thin (≤ 80 nm) polymer gate dielectric layers with consequent low gate voltage operation was shown to be a more robust means of achieving stability in OFETs incorporating either pristine or cross-linked PVP gate dielectrics. We also demonstrated the superiority of hybrid bilayer PVP/SiO_2 OFETs with regards to their low voltage operation and operational stability over OFETs with bare SiO_2. Once again, dissolution of low-*k* polymer gate dielectrics in high dipole moment and high-*k* solvents is shown to be a reliable and effective means of achieving low-voltage operation in pentacene OFETs incorporating single layer low-k polymer gate dielectrics. Overall, this study demonstrates the feasibility of thin and single PVP dielectric layer in achieving low-operating voltage and highly stable OFETs that compare favorably well with OFETs employing hydrophobic high-*k* inorganic or high-*k* inorganic/low-*k* organic hybrid dielectric bilayers; thus, strengthening the prospects of employing hydrophilic low-*k* polymer dielectrics in the design of practical electronic circuits.

CHAPTER 7

CONCLUDING REMARKS AND FUTURE DIRECTION

In this thesis, we investigated and addressed some of the obvious problems of organic electronics, precisely, (a) the inherent solvent-selectivity and polymer dissolution problems limiting the fabrication of all-polymer devices and (b) the difficulty in achieving stability and low-voltage operation using low-*k* polymeric dielectrics in organic field-effect transistors. Our belief is that our work will contribute immensely to an accelerated advancement of the fledgling field of organic electronics.

We demonstrated the success of the MAPLE technique in overcoming the solvent-selectivity and inherent swelling and dissolution problems associated with fabricating all-polymer FETs and MIS capacitors via traditional solution-processable techniques, especially when non-orthogonal solvents are involved. Our results showed that the higher the difference between the solubility parameters of the solvent and PMMA, the less rough the PMMA surface and consequently, the better the device performance. Negative shifts of the threshold voltage in the FETs were correlated with differences in acceptor doping density and similar shifts in flat band voltage of the MIS

diodes, which was found to be due to the difference in the density of states at the semiconductor-insulator interface.

However, it is worth noting that in this work, the MAPLE technique has been employed in depositing just one polymer semiconductor (PFB). As such, in order to prove its versatility in the fabrication of all-polymer FETs, it needs to be employed in the deposition of other solution-processable semiconducting and dielectric materials especially those with inherently better electrical characteristics such as P3HT. Also, by fabricating devices incorporating other solution-processable materials using MAPLE, the consistency of the above observed FET and MIS capacitor behaviors could be established.

Pentacene, which was also employed as the active layer in our work, is one of the most promising small molecule organic semiconductors due to its crystallinity and high field-effect mobility. Again, PMMA which was used as the gate dielectric is known to give rise to operationally stable organic devices due to its hydrophobic methyl methacryl group. However, its low dielectric constant and the presence of pinholes especially for low thickness PMMA films, limit the achievement of low-voltage OFETs. Our investigations revealed that device-quality, low-thickness (~ 70 nm) and pinhole-free PMMA layers are achievable via its dissolution in high dielectric constant and high dipole moment propylene carbonate (PC) solvent. Similar thin PMMA layers were not realized with PMMA when dissolved in low dielectric constant and low dipole moment solvents such as butyl acetate (BTAc). Using PC-dissolved PMMA gate dielectric, we demonstrated record low-operating voltage (below -3 V) and highly stable OFETs, which

opens up the prospects of a possible utilization of less-polar and low-k polymer gate dielectrics in the realization of device-quality, stable, and low-voltage transistors that could be employed in the design of practical electronic circuits.

However, there still exist some unresolved issues in our observations. The most interesting is the absence of a proper understanding of the basic reactions between PC and PMMA that give rise to low-thickness and pinhole-free PMMA films which enable very low-voltage operation and improvement in OFET performance. While we attribute the excellent quality of our dielectric layers and consequently, the excellent performance of our devices to the high dipole moment and high dielectric constant properties of PC, we believe that more experimental investigations and theoretical modeling may also be insightful. One of such experiments could be to fabricate and characterize top-gate OFETs incorporating just PC solvent and any other low dipole moment solvent as the gate dielectric. By eliminating the use of an actual polymeric dielectric such as PMMA from the devices, it may be easier to discern the exact contributions/effects of the solvent.

As a further demonstration of the universality of this technique of achieving high yield, stable, and low-operating voltage devices incorporating low-*k* polymeric dielectrics dissolved in high dipole moment and high-*k* solvents, we fabricated OFETs and MIS diodes using pristine and cross-linked low-*k* PVP dissolved in PC and DMSO, as gate dielectrics and studied their electrical characteristics and operational as well as environmental stability. Remarkably, OFETs fabricated with thin pristine and cross-linked PVP dielectrics were operated at very low gate voltages (within -3 V) and

exhibited high stability under bias stress and in air while OFETs with thick cross-linked PVP dielectric were operated at high gate voltages and exhibited considerable operational instability and gate leakage current attributable to an increased density of dipole groups inside the bulk polymer dielectric. Hence, the use of thin (≤ 80 nm) polymer gate dielectric layers with consequent low gate voltage operation was shown to be a more robust means of achieving stability in OFETs incorporating either pristine or cross-linked PVP gate dielectrics. We also demonstrated the superiority of hybrid bilayer PVP/SiO_2 OFETs with regards to their low voltage operation and operational stability over OFETs with bare SiO_2.

Again, while we attribute the excellent properties of our PVP-based devices to the high dipole moment and high dielectric constants of the solvents (PC and DMSO), we believe that more experiments and theoretical simulations aimed at a better understanding of the atomic/molecular-level chemistry of the interactions between PVP and this class of solvents are highly critical for a complete explanation of these exciting observations. Although, we gave an estimate of the thickness range necessary for achieving low-voltage operation in PVP-based OFETs, it will also be interesting to carry out more detailed device fabrications and characterizations around this range so as to be able to determine a precise cut-off thickness for low voltage OFET operation. Last, in order to properly investigate the behavior (filling and unfilling) of trap states at the semiconductor-insulator interfaces of MIS diodes and OFETs, application of pulsed voltages in the capacitance-voltage and current-voltage characterizations of MIS diodes and OFETs may be necessary.

While we recognize that organic electronics is still a fledging field with a host of challenges, we strongly believe that our work has helped in providing a critical roadmap and perhaps, erased two of the most daunting challenges of organic electronics namely: (a) the inherent solvent-selectivity and dissolution problems limiting the fabrication of all-polymer devices and (b) operational instability and difficulty in achieving low-operating voltage devices using conventional low-*k* polymer dielectrics.

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VITA

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PUBLICATIONS

- **N. B. Ukah**, J. Granstrom, R. R. Sanganna Gari, G. M. King, S. Guha, "*Low-operating voltage and stable organic field-effect transistors with poly (methyl methacrylate) gate dielectric deposited from a high dipole moment solvent*" Applied Physics Letters 99, 243302 **(2011)**

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- **N. B. Ukah,** D. Adil, J. Granstrom, R. K. Gupta, K. Ghosh, and S. Guha, "*Matrix-assisted pulsed-laser evaporated polymer films in all-organic field-effect transistors and metal-insulator-semiconductor diodes*" Organic Electronics 12, 1580 (**2011**)

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