CURRENT-MODE CMOS HYBRID IMAGE SENSOR

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ABSTRACT

Digital imaging is growing rapidly making Complimentary Metal-Oxide-Semi conductor (CMOS) image sensor-based cameras indispensable in many modern life devices like cell phones, surveillance devices, personal computers, and tablets. For various purposes wireless portable image systems are widely deployed in many indoor and outdoor places such as hospitals, urban areas, streets, highways, forests, mountains, and towers. However, the increased demand on high-resolution image sensors and improved processing features is expected to increase the power consumption of the CMOS sensor-based camera systems. Increased power consumption translates into a reduced battery life-time. The increased power consumption might not be a problem if there is access to a nearby charging station. On the other hand, the problem arises if the image sensor is located in widely spread areas, unfavorable to human intervention, and difficult to reach. Given the limitation of energy sources available for wireless CMOS image sensor, an energy harvesting technique presents a viable solution to extend the sensor life-time. Energy

can be harvested from the sun light or the artificial light surrounding the sensor itself.

In this thesis, we propose a current-mode CMOS hybrid image sensor capable of energy harvesting and image capture. The proposed sensor is based on a hybrid pixel that can be programmed to perform the task of an image sensor and the task of a solar cell to harvest energy. The basic idea is to design a pixel that can be configured to exploit its internal photodiode to perform two functions: image sensing and energy harvesting. As a proof of concept a 40 x 40 array of hybrid pixels has been designed and fabricated in a standard $0.5\ \mu m$ CMOS process. Measurement results show that up to $39\ \mu W$ of power can be harvested from the array under 130 Klux condition with an energy efficiency of 220 nJ /pixel /frame. The proposed image sensor is a current-mode image sensor which has several advantages over the voltage-mode. The most important advantages of using current-mode technique are: reduced power consumption of the chip, ease of arithmetic operations implementation, simplification of the circuit design and hence reduced layout complexity.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Computing and Engineering, have examined a thesis titled "CURRENT-MODE CMOS HYBRID IMAGE SENSOR," presented by MOHAMMAD KASSIM BENYHESAN, candidate for the Master of Science degree, and hereby certify that in their opinion it is worthy of acceptance.

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CHAPTER 1

INTRODUCTION

1.1 Introduction and Thesis Motivation

The complementary metal-oxide-semiconductor (CMOS) Image Sensor becomes indispensable in many of the everyday appliances such as cellular phones, surveillance devices, personal computers, tablets, etc. In addition, the development of wireless communications leads to a tremendous growth in wireless image sensor networks where communication among sensors located in different sites being possible. The new features of such appliances along with their low cost have motivated people to increase the usage of such appliances in different fields and for different purposes including but not limited to environment surveillance, hospitals where the intervention of the human is not preferred in some locations, and is being used to monitor the life of the animals in the wild [1]- [2]- [3]- [4]. However, the challenge is to find a balance between the need for high-energy to accomplish the continued improvement features such as high-resolution, readout speed and sending data remotely and the indispensable need for low-power operation to extend the system lifetime. High-efficiency batteries have been playing a main role to provide the required power for their operations, and thus, another challenge has appeared due to the fact that these batteries need to be charged and maintained regularly which will be a very critical and costly operation, especially with the increasing usage in far and possibly inaccessible areas.

After a careful scrutiny of the nature of the challenge, the challenge can be simplified into the following question: how to provide an alternative energy sources to the CMOS wireless image sensor in order to solve the limitation of the on-board energy sources problem?. An energy harvesting technique provides a viable answer to the question. The concept is to harvest the energy from the environment surrounding the CMOS wireless image sensor itself [5]. The harvested energy can be used then to charge the battery or it can be used to power some of the CMOS wireless image sensor components. There are several significant energy sources available in the sensor's surrounding environment such as light, heat, vibration, and so on. However, light is the most attractive energy source among the others because of the object under the lens is the image sensor which is mainly used to sense the light and convert it into electrical signals, and hence, it is easier to use the same sensor elements, if possible, to harvest the energy from the light and convert it into an electrical signals. Further these signals can be used to charge the system battery, and hence, extend the battery life-time. Moreover, to harvest the energy from the other energy sources, an additional mechanical part that are difficult to integrate on chip is needed [5].

As a starting point and in order to get the required knowledge about the image sensors subject, careful examination has been carried out on published research and books. A great information on the background and the various structures of the CMOS image sensors has been found in [6] and [7], where a variety of CMOS image sensor structures have been studied. Although, voltage-mode Active Pixel Sensor (APS) is more attractive and

has gained much attention from researchers due to its valuable characteristics, current-mode current-mode Passive Pixel Sensor (PPS) has provided a new avenue of research for the focal plane image processing architecture due to the great features of the current-mode image processing over the voltage-mode image processing [8]- [9]- [10]- [11]- [12]. In [13], a detailed information on the p-n junction photodiode basic characteristics has been a key point to understand the concept of the p-n junction characteristics, the author stated that, we should note that without reverse bias, the illuminated photodiode functions as a solar cell. Usually fabricated from low-cost silicon, a solar cell converts light to electrical energy, which is providing a hint to the possibility of using the photodiode which is the core of the CMOS image sensor as a solar cell. Moreover, [4] has a great study on the CMOS photodetector types with in-depth explanation on the p-n junction drift currents and the photo sensor structure types as well. Section 3.5 (Junctions and Diodes) of [14] has a valuable information of using p-n junction solar cell.

To summarize the outcome from the extensive study of the materials mentioned above, it has been found that the core of the CMOS image sensor is the photodector, basically a reverse biased p-n junction photodiode. The core of the solar cell is unbiased p-n junction photodiode. The basic function of the p-n junction photodiode is to sense the light and convert it into electrical signal. In the image sensor, the electrical signal in form of current or voltage is processed to be image data. In the solar cell the electrical signal is called the energy harvested and then its processed further to be used by the system. The p-n junction photodiode can be implemented in CMOS process with different forms.

After gathering the above information, another study has been carried out on several publications that are proposing CMOS image sensors with energy harvesting capability. In [15], a proposed self-powered active pixel sensor was presented, the idea was based on using an off-pixel p-n junction photodiode to harvest the energy from the light and provided to the pixel to perform image sensing function. The number of the external p-n junction photodiodes are equal to the number of the pixels in the image sensor array, and hence, the external p-n junction is taking up silicon resources given that the in-pixel p-n junction photodiode is inactive during the sleeping mode or between capturing images but it still occupying silicon area. However, the approach successfully proved the ability of the CMOS p-n junction photodiode to harvest the energy and power the sensor. Another study was presented in [16] to prove the ability of stacked CMOS p-n junction photodiodes to harvest and produce high-voltage generation. In [17], authors take a different approach by using the in-pixel p-n junction photodiode to harvest energy and capture images. The proposed image sensor is low-power with high-dynamic range. Another approaches were presented in [18], [19], and [20].

In this thesis, a passive pixel sensors are modified to create hybrid pixels which have the ability to sense and harvest light energy. The proposed hybrid pixel can be programmed to perform dual functions: image sensing and energy harvesting. The in-pixel p-n junction photodiode itself is used to perform the dual functions. An hybrid pixels sensor has been designed and tested.

1.2 Thesis Purpose

Based on the foregoing discussion, it is clear the need to design a CMOS image sensor that has the ability to configure its in-pixel photodiode to perform dual functions: image sensing and energy harvesting. The sensor's pixels will be called hybrid pixels due to their ability to harvest energy when there is no need to use them as photo sensor. The purpose of this thesis is to design and implement the proposed current-mode hybrid pixel with a memory cell included in the pixel to differentiate the two functions on a pixel-by-pixel basis and to prove the concept of such technique. A 40 x 40 hybrid pixel array has been designed. Each pixel contain 10 Metal-Oxide Semiconductor (MOS) transistors and a p-n junction photodiode as a photosensitive element of the pixel. An integrator, and readout shift registers have been fabricated using On Semiconductor $0.5\ \mu m$ technology along with the pixel array. The usage of shift registers for rows and columns , unlike the traditional readout technique of using a decoder for row selection purposes, makes the configuration of the array in various pattern possible such as configuring the array by selecting pixels arbitrarily or by selecting one or multiple pixels to do specific function while the other pixels doing another. The use of this technique along with the fact that all the currents provided by the pixels pour into single line make the design suitable for addition and subtraction operations. A customized double-layer board has been designed and fabricated to host the proposed image sensor in the experiment setup.

1.3 Summary of Contributions

The main contributions of this work are as follows:

- The design of a new structure of CMOS image sensor pixel which involves the use of memory latch circuit to control the photodetector functionality.
- The design and fabrication of a chip consists of 40 x 40 hybrid pixel array, shift registers together with integrator using On Semiconductor $0.5\ \mu m$ CMOS process.
- A printed board has been designed to test the proposed pixel and/or the proposed image sensor.
- Soldering the board components required to operate the chip.
- A VHDL codes with variety of timing and controlling patterns have been designed.
- A Matlab codes have been written to analyze the experiments results.

1.4 Thesis Outline

In Chapter 2 a brief reviews on a typical passive pixel image sensor, a solar cell basic, and the forms of p-n junction photodiodes in CMOS technology are given. in Chapter 3, a proposed hybrid pixel operation principle is presented first. Followed by the proposed current-mode CMOS hybrid image sensor design and implementation. In Chapter 4, the measurements and the results are carried out. In Chapter 5, the summary and conclusion.

CHAPTER 2

BACKGROUND AND OVERVIEW

2.1 Typical CMOS Image Sensor Structural Elements

A typical CMOS image sensor consists of an array of pixels that are commonly enabled on row-by-row basis by a peripheral shift register or encoder. Once a row is selected, the pixels in the row are read out to a vertical column bus that connects the pixel to an analog signal processing circuit. The analog signal processing circuit is used to perform various tasks such as charge integration, analog to digital conversion among other functions. Each pixel in the array act as an electrical signal transducer and the processing circuit is the receiver. The generated signal from the pixel represents the natural response of the essential photosensitive element in the pixel circuit to an reflected light from a scene. Traditionally, photodiodes are used as the photosensitive element in the pixel circuit. The photodiode, working as a reverse biased p-n junction, is used to collect a charges from the incident light's photon flux and convert the charges to an electrical signal that can be read out as a voltage or a current by the analog signal processing circuits. In CMOS sensing, a photodiode is made by forming n-type region on a p-type semiconductor substrate or forming p-type region on n-type region and then on p substrate.

Three pixel circuit designs is presented in [6] by Fossum. However, a passive pixel circuit approach is selected, as a guide to reach the target aim of this thesis. The selection is made due to the simplicity of the passive pixel circuit architecture. As depicted in

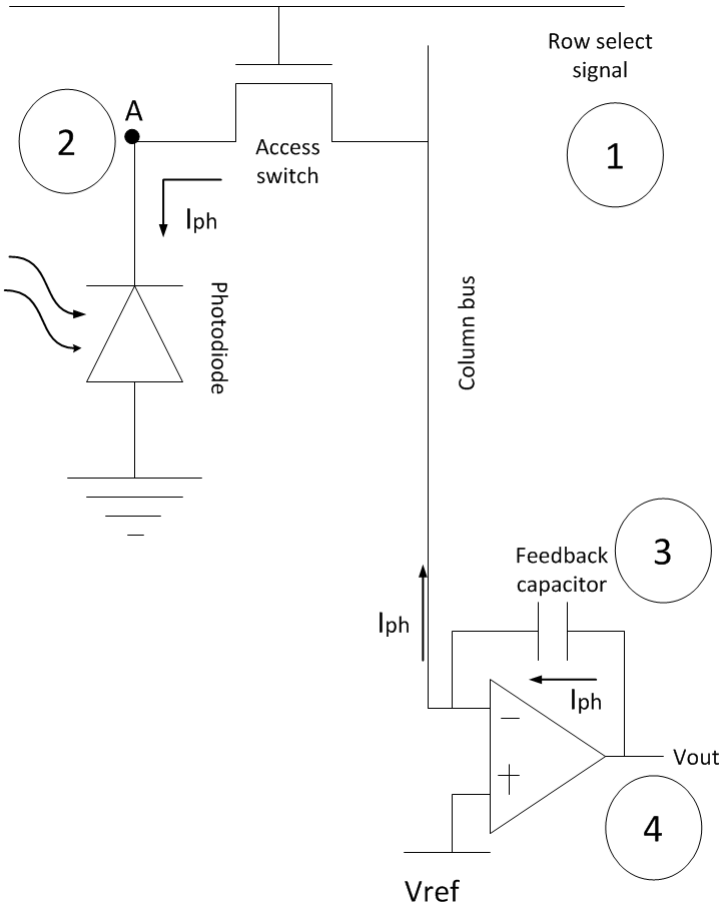

Figure 1: A Typical Passive Pixel Sensor

Fig. 1, the passive pixel circuit consist of a photodiode and an access switch, offering the highest fill factor among the other pixel circuit approaches. Once a row is selected (point 1 in Fig. 1), the photodiode is connected to a column bus. The voltage on the bus is kept constant by an integrator at the end of the column bus. The photodiode's cathode is kept at a constant voltage (point 2 in Fig. 1) with respect to the photodiode's anode which is kept at ground potential, and hence, the photodiode is reverse biased. Once the photodiode is illuminated, the photo generated current, proportional to the illumination

light, flow through the integrator feedback capacitor (point 3 in Fig. 1) causing a charge accumulation in the feedback capacitor. After a specific period of accumulation time, the integrator converts the charge accumulated in the feedback capacitor into an output voltage (point 4 in Fig. 1).

Fig. 2 is showing the operation region of the p-n junction photodiode. If the photodiode is illuminated with light, the photodiode I-V characteristic is shifted down and more reverse bias current (Iph) is produced proportional to the incident light. Region (A) in the figure is the operation region of the photodiode required to perform the task of photo sensing.

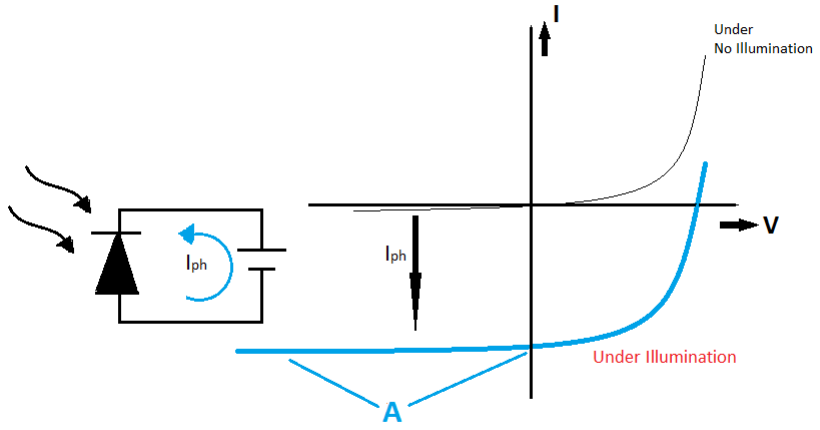

Figure 2: I-V curve: A is the operation region of the photodiode required to perform the task of photo sensing

2.2 Solar Cell Basics

Solar cell intrinsically can be viewed as an unbiased p-n junction photodiode. A solar cell is used to harvest energy from the sun rays or from the artificial light that is available in the environment surrounding the solar cell itself . A solar panel (or array) is constructed by connecting many of solar cells in parallel and/or in series. This connections are essentially made to achieve the biggest possible area of semiconductor material that can be illuminated by the incident light. The solar panel consist of a buffer to collect the harvested energy, a power management circuit, and a processing circuit. Most importantly, a p-n junction based solar cell is made by using the same forms mentioned in previous section and the essential function of the unbiased p-n junction photodiode is still the same as in the CMOS image sensor that is collecting charges from the incident light and convert it to an electrical signal. However, the p-n junction photodiode in the image sensor is required to work under a reverse bias condition. In contrast, the solar cell's photodiode is working under no biasing condition. The I-V characteristic in Fig. 3 describes the operation region of the phtotodiode in the solar cell. As can be seen in Fig. 3, B represent the p-n junction operation region. Clearly, as depicted in Fig. 3, the passive sign convention is not valid, from the circuit point of view, where the voltage is positive and the current is negative in region B, and thus, the p-n junction photodiode is a power/energy supplier in region B. If the anode and the cathode of a photodiode, under illumination condition, are shorted together, a current Isc (short circuit current) circulates contentiously in the loop from the anode (p-type region) towards the cathode (n-type region). If a photodiode's contacts are left unconnected, under illumination condition, a

potential difference (Voc = open circuit voltage) will be established between the photodiode's contacts. Isc and Voc, as shown in Fig. 3, are the interception points with I and V, respectively. However, the maximum power/energy that can be harvested is represented by the shadowed box. The maximum harvested power is equal to the product of ((Vmax) x (Imax)) as can be seen in Fig. 3.

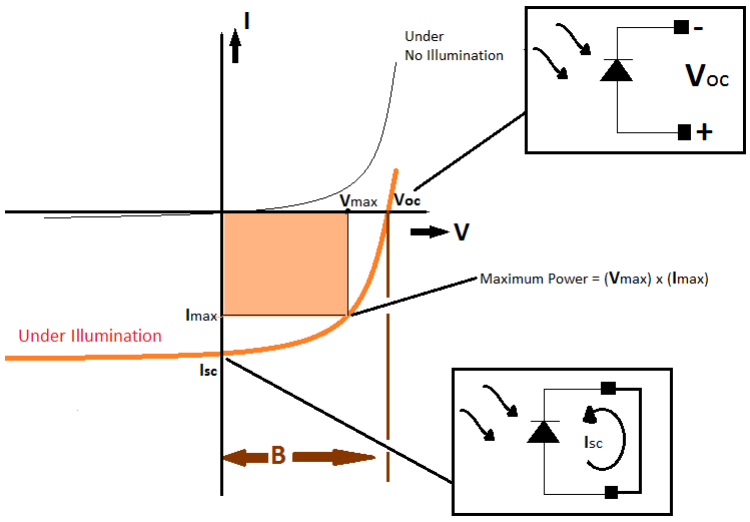

Figure 3: I-V curve: B is the operation region of the photodiode required to perform the task of energy harvesting (solar cell)

2.3 A Photodiode Forms In Standard CMOS Process

In a standard complimentary metal-oxide-semiconductor (CMOS) process, the p-n junction can be made by forming one of the following:

- Nwell/P-sub : the p-n junction is formed by an n-well implant on a p-type semiconductor substrate.

- N+/P-sub : the p-n junction is formed by an n-type implant region on a p-type semiconductor substrate.

- P+/Nwell: the p-n junction is formed by an n-well implant region on a p-type semiconductor substrate, and then a p-type implant material region on the n-well region.

The p-n junction photodiode is naturally formed between the n-type material and the p-type substrate in the first 2 types. The fact that the substrate must be connected to the most negative voltage in the circuit, makes the anode contact of the formed photodiode inaccessible. Fig. 4 shows the structural overview of the first 2 types. The cathode contact only can be accessible with these types of photodiodes. However, since biasing the photodiode is still possible by applying a positive voltage on its anode contact, the first 2 types is suitable to perform the tasks of photo sensing.

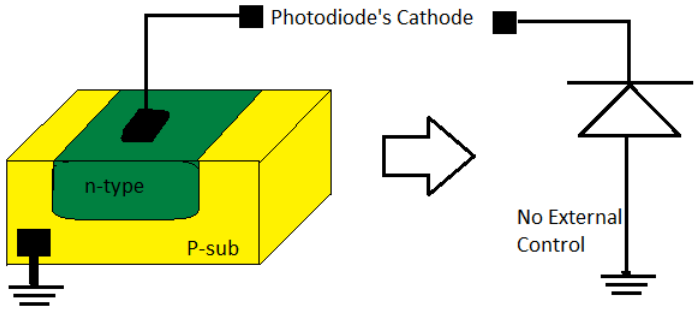

Figure 4: A structural overview of the Nwell/P-sub and N+/Psub p-n junction photodiode, the anode is always tied to the ground

In contrast, the P+/Nwell type is offering a full access to the photodiode's anode and cathode contacts. Fig. 5 shows a structural overview for the P+/Nwell type. The photodiode's anode and cathode are freed from the substrate and both contacts are accessible

externally. The advantage of P+/Nwell type over the first two photodiode's types is the possibility of studying the behavior of the photodiode alone, and since both photodiode's contacts are accessible, it is easy to control the photodiode's operation, and hence, this type is suitable to operate under reverse biased condition as a photosensor or under un-biased condition as a solar cell. However, a parasitic diode is formed naturally between the n-well and the p-substrate. The parasitic p-n junction is in deeper region comparing to the photodiode p-n junction from a layout point of view, and thus, its most likely that the incident light's photons are absorbed in the upper p-n junction depletion region rather than the p-n parasitic depletion region. Moreover, a layout techniques are very useful to lower the probability of reaching the parasitic p-n junction depletion region by a light photon flux.

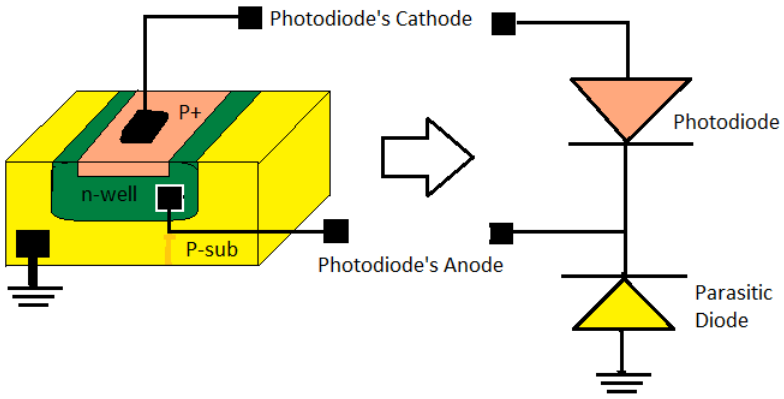

Figure 5: A structural overview of an P+/Nwell type photodiode; full access to the photodiode's contacts

2.4 Summary

In this chapter we gave a brief overview on typical CMOS image sensors structural elements and the solar cell basics. We showed that, the photosensitive element is the essential element to construct the image sensor array and the solar panel. The photosensitive element is basically a p-n junction photodiode. The photodiode's connection and the biasing condition govern the photodiode functionality: image sensor or solar cell (energy harvester). The rest of this thesis will be based on the information gathered in this chapter.

CHAPTER 3

A CURRENT-MODE CMOS HYBRID IMAGE SENSOR

3.1 Introduction

In Chapter 2 we have explored the principles and the components of the image sensors and the solar. The pixel in the image sensor and the solar cell in the solar panel both contain a photosensitive element, specifically a p-n junction photodiode, in their circuit. The main function of the photodiode in both systems mentioned above is to absorb the energy from the incident light and convert it to an electrical signal, and then this signal will be transferred to an appropriate processing circuit according to the system functionality. While both systems share the basic function of the p-n junction photodiode, the two systems deviate from each other by their techniques in reading out and processing the signal generated by the photodiode. This, in turn, motivate us to design a configurable pixel that can be programmed to connect the cathode and the anode of its in-pixel photodiode to a two separate biasing and processing destination circuits, and thus, the photodiode's generated signal due to the incident light on the photodiode's semiconductor materials is read out and processed separately. The same photodiode in the pixel circuit is used to perform the dual functions: the normal function of the image sensor (i.e. image sensing) and the normal function of the solar cell (i.e. energy harvesting), one function at a time. The dual functionality is the concept of the proposed pixel. The term 'hybrid pixel' is

referring to a pixel with dual functionality feature. The advantage of configuring the in-pixel photodiode to perform dual functions is to exploit the in-pixel photodiode's silicon area to harvest solar energy when the photodiode is not acquiring images.

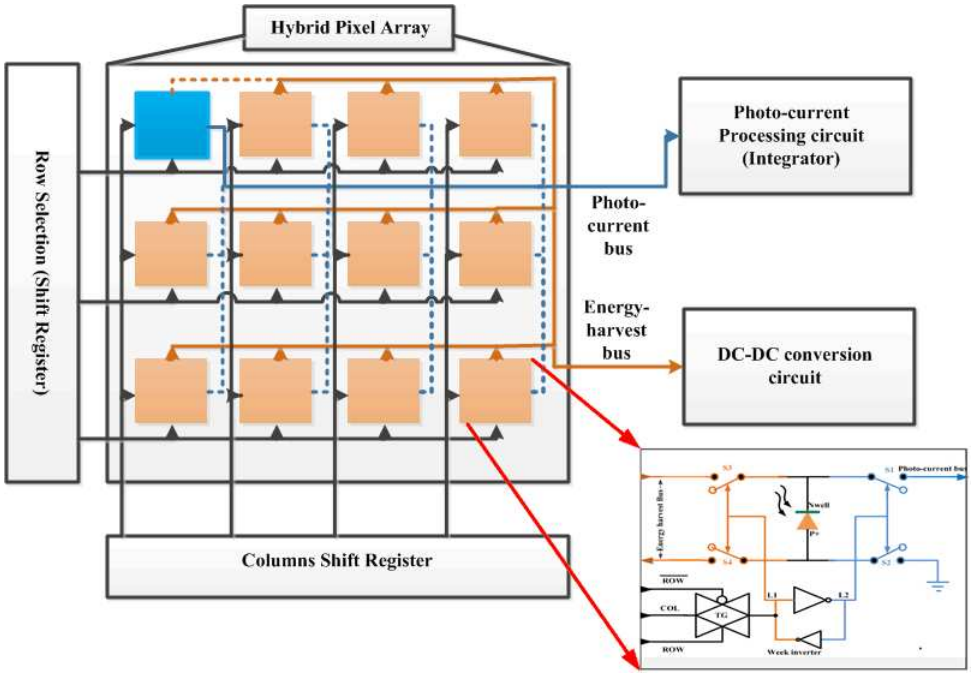

Figure 6: A basic overview of the proposed current-mode CMOS hybrid image sensor.

This chapter proposes a current-mode CMOS hybrid image sensor. Fig. 6 gives a basic idea about the concept of the proposed current-mode CMOS hybrid image sensor's structure and functionality. As depicted in Fig. 6, the proposed current-mode CMOS hybrid image sensor consist of an array of hybrid pixels, row and column shift registers and an integrator. Each pixel is able to perform dual functions by programming its internal circuitry. The dual functions are: image sensing and energy harvesting. If the hybrid pixel is set to perform the image sensing function, which is the normal function for the pixel in

a typical CMOS image sensor, then we say that the hybrid pixel is working in the image sensing mode. In this mode, the phtotodiode is working in the reverse bias region, and the photo generated signal, in form of current, is read out from the photo-current bus. Otherwise, we say that the pixel is in the energy harvesting mode and the current generated by the pixel photodiode flows in the energy harvested bus. The photo-current bus is common for all the pixels in the entire array, if a pixel wants to access this bus then the pixel must be working in the image sensing mode. A single integrator at the end of the photo-current bus is used to integrate (accumulate) the charges generated by illuminating the in-pixel reverse biased photodiode for a specific time and convert the accumulated charges to be read out as an output voltage. Similarly, the harvested-energy bus is common for all the pixels in the array, if a pixel is working in the energy harvesting mode then the in-pixel photodiode's contacts must be connected to the energy-harvested bus, and the energy-harvested bus will convey the charges generated, proportional to the intensity of incident light, in form of a current, from the pixel(s) to an off-chip energy harvesting conversion circuit. Further, the accumulated charges in the conversion circuit can be processed to charge the battery or to supply other components. A peripheral row and column shift registers are used to program the internal circuitry of an individual hybrid pixel or a group of pixels. Moreover, the signals flow in the proposed image sensor electronic circuit is in form of current and the proposed image sensor is a current-mode type image sensor. The current-mode signal processing has many advantages over the conventional voltage-mode signal processing [21] . The potential advantages of designing the current-mode image sensor

are: lower supply voltage, and hence, reduced power consumption of the chip. Moreover, current-mode is much faster than the voltage-mode due to the fact that the parasitic capacitance associated with the circuits would not degrade the operating speed, and the current-mode technique can simplify the circuit design and get a better use of the silicon die's area due to the fact that the output signals from the pixels of the image sensor array are inherently currents. Moreover, operations such as addition, subtraction, and product of sum can be more easily implemented in current-mode citebermak2004low- [22].

As depicted in Fig. 6, the blue pixel is programmed to work in the image sensing mode and the photo-current bus conveys its current to the integrator (the solid blue line in Fig. 6), and the other orange pixels is programmed to work in the energy harvesting mode and their currents (energy) flows through the energy-harvested bus to a DC-DC conversion circuit. The dashed blue and orange lines in the figure means that the pixel is internally disconnected from the bus and the photo-diode generated current is not contributing in the currents that flows in that bus. More importantly, the array in the proposed CMOS image sensor is exploited to harvest energy as well as sensing image and the photo-diode in each pixel work as image sensor and then can be switched back to work as energy harvester and deliver the harvested energy to an external DC-DC conversion circuit.

In section 3.2 the proposed hybrid pixel is presented in details. In section 3.3, we proposed a current-mode CMOS hybrid image sensor along with the design and implementation details are presented. As a proof of concept a chip contains the proposed image sensor is fabricated and presented in section 3.3 as well. Followed by a conclusion section (section 3.4).

3.2 CMOS Hybrid Pixel

CMOS hybrid pixel is a CMOS image sensor pixel able to perform dual functions: image sensing and energy harvesting. The idea of the hybrid pixel comes from the fact that the image sensor pixel circuit and the solar cell circuit have a common photosensing element, that is the p-n junction photodiode. For a photodiode to work as a photo sensor, a p-n junction photodiode is reverse biased; that is a positive potential applied on its cathode with respect to its anode. A p-n junction photodiode without biasing, no external potential applied to the p-n contacts, forms a solar cell that can be used to harvest ambient energy from the light. Thus, the connections and biasing conditions of the diode's anode and cathode define the diode's functionality: image sensor or solar cell (harvester). This concept is the cornerstone in designing the pixel that contains one p-n junction photodiode and four assert-high switches to control the photodiode's contacts connections such that the pixel is able to achieve both functions (i.e. image sensing or energy harvesting). The photodiodes occupy a significant area of a typical CMOS image sensor, and they are active to perform image sensing task at only a certain time to capture an image. After that, the photodiodes are usually inactive, but still take up area resources, until another request of capturing an image is initiated. The proposed hybrid pixel harness the inactive photodiodes's area resources to harvest solar energy, and hence, the image sensor's array is exploited to harvest solar energy. The proposed hybrid pixel during the image sensing mode inherits most of the passive pixel sensor's characteristic which is described in Chapter 2.

3.2.1 **Pixel Architecture and Operating Principle**

The proposed hybrid pixel architecture is shown in Fig. 7. The hybrid pixel consists of a p-n junction photodiode (P+/Nwell type photodiode) and a 10 transistors. Switches S1, S2, S3 and S4 are 1 transistor each, a latch composed of 4 transistors, and a transmission gate composed of 2 transistors.

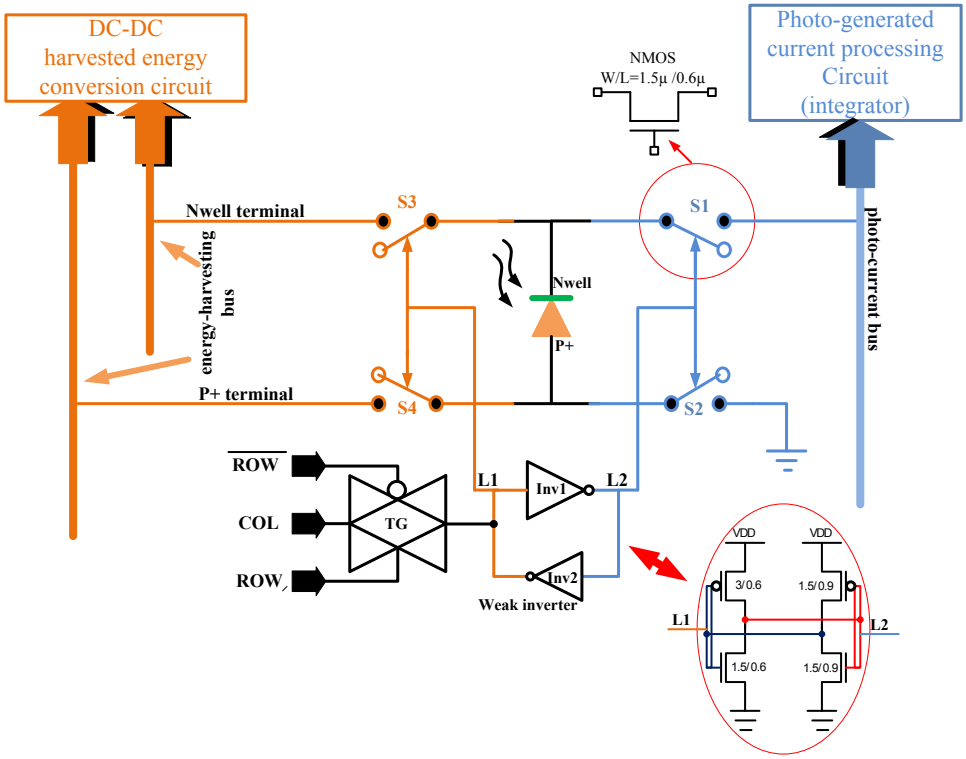

Figure 7: Hybrid pixel structure.

Switches S1 and S2 are used to connect the p-n junction photodiode's contacts to a photo-current bus and to the ground respectively, the other switches S3 and S4 are used to connect the the p-n junction photodiode's contacts to a two-wire bus for harvesting

energy purposes (Nwell Terminal and P+ Terminal wires), the two wires form an energy-harvesting bus. In addition to the switches there are two inverters connected back-to-back to form a *latch*, basically 1-bit memory cell, with two ends L1 and L2 as depicted in Fig. 7. The stored bit in both sides of the latch are in complementary form (i.e. when L1 = 0 then L2 = 1 and vice versa), thus, each side of the latch is used to produce a control signal for pair of switches. The logic bit stored in the L2 side generates the control signal to S1 and S2 switches and L1, the input side, will controls S3 and S4 switches. Basically, at any given time only one pair of switches is closed. That is, the control signal of one switch pair is logic 1, while the other set is in the opposite state. The data on COL passes to the latch through transmission gate, TG, controlled by ROW and $\overline{ROW}$ signals. The COL and the complementary pair ROW and $\overline{ROW}$ control signals are provided by a peripheral column and row shift registers respectively. If ROW goes high ($\overline{ROW}$=0) then the value of COL, logic 1 or 0, passes to L1 and then the complementary of the value at L1 shows up at L2. Table 3 summarizes the possible operation of the pixel circuit.

Table 1: Hybrid pixel circuit functionality table

ROW	COL	L1	L2	S1, S2	S3, S4	Bus
1 (TG enabled)	0	0	1	$closed$	$open$	photo-current
1 (TG enabled)	1	1	0	$open$	$closed$	energy-harvesting
0 (TG disabled)	ANY	0	1	$closed$	$open$	photo-current
0 (TG disabled)	ANY	1	0	$open$	$closed$	energy-harvesting

The transitions in Table 3 shows that the input data on COL plays the major role in defining the connection of the p-n junction diode such that by writing a 0 to the latch,

the diode's anode and cathode terminals will be connected to the ground and to the photo-current bus respectively and writing a 1 the diode's anode and cathode terminals will be connected to P+ terminal and Nwell terminal wires respectively.

3.2.2 **Operating Modes**

The proposed hybrid pixel is able to work in image sensing mode and energy harvesting mode. To get a better understanding of the hybrid pixel sensor, the complete read out paths are illustrated in Fig. 8 and Fig. 9. In Fig. 8 and Fig. 9, the hybrid pixel is assumed to be a part of an M x N array to show the ability of configuring an individual pixel. The COL and the complementary pair ROW and $\overline{ROW}$ control signals are provided by a peripheral column and row shift registers respectively. For an array of M x N, there are M pairs of ROW and $\overline{ROW}$, one pair for each row, and there are N single COL, one for each column. The photo-current bus and the 2 wires of the energy-harvesting bus are shared by all the pixels in the entire array. A single integrator is showing at the end of the photo-current bus. The integrator perform a charge integration (accumulation) function and a current to voltage conversion function.

Fig. 8 illustrates the hybrid pixel circuit in energy harvesting mode. To perform the energy harvesting function, the hybrid pixel is selected by a ROW = 1 and $\overline{ROW}$ = 0, and then a 1 is written to the latch by making the value on COL = 1. When ROW goes low, the latch retain its value (i.e. 1) and the COL value is not able to write the latch value until ROW goes back high again. Since the latched value is 1, the switches control signals L1 is high and L2 is low, and thus, switches S3 and S4 are in close position. Therefore, the

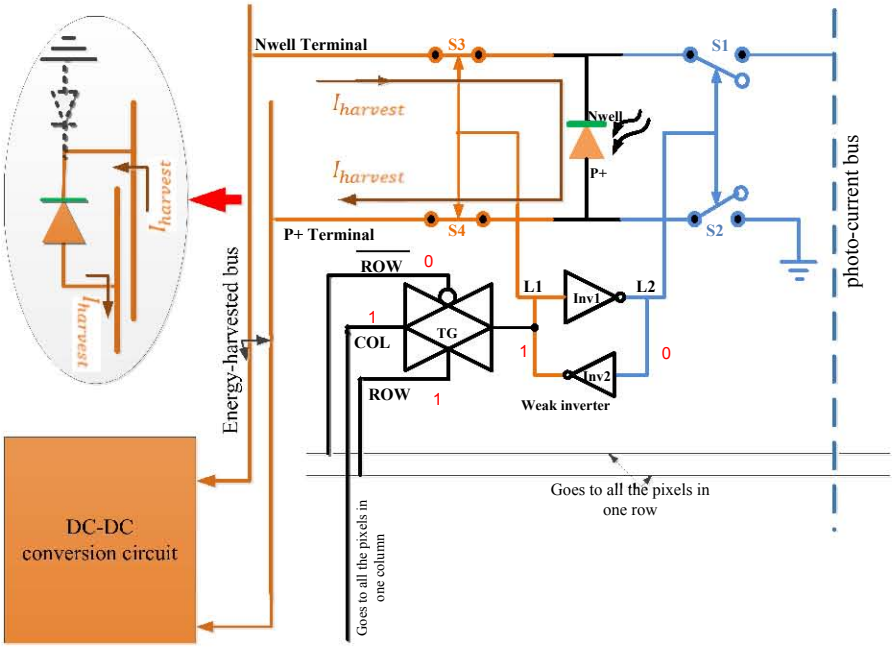

Figure 8: The hybrid pixel in energy harvesting mode. The equivalent circuit is shown inside the elipse.

pixel circuit can be simplified to an equivalent circuit as depicted by the circuit inside the ellipse shape in Fig. 8. It can be seen that the photodiode operates in its photovoltaic mode with its anode and cathode contacts are connected to an off-pixel energy-harvesting bus. In addition, Fig. 8 shows the parasitic p-n junction diode (the dashed black diode) formed naturally between the Nwell layer and the p-substrate, the p-type substrate is grounded always causing this diode to sink a small amount of current from the generated current from the original photodiode. The rest of the generated current is $I_{harvest}$. The effect of parasitic diode is reduced by freeing the anode and the cathode of the original photodiode, this in turn provide an easy path for the charges to flow in, instead of going through the

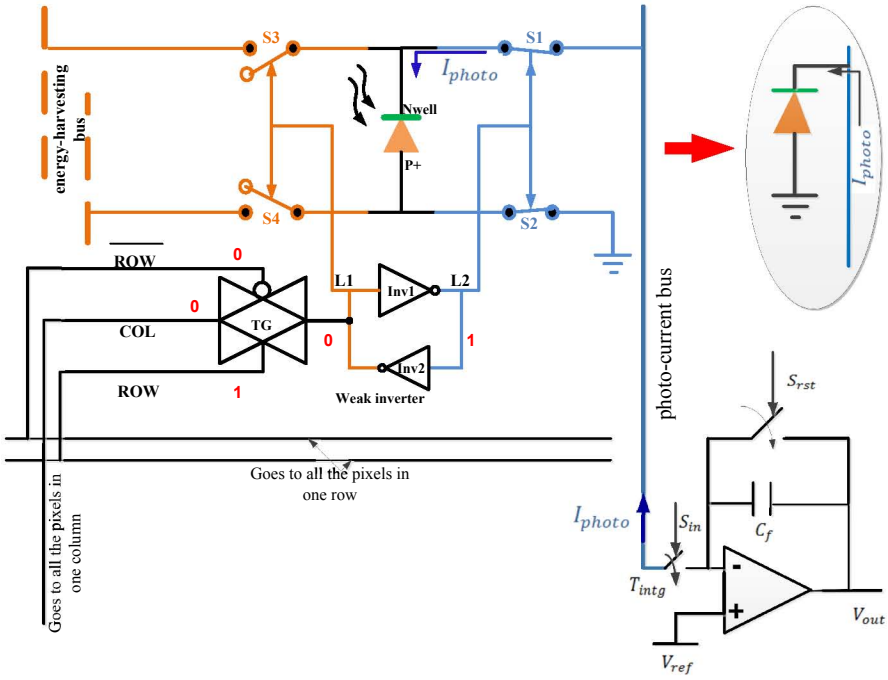

Figure 9: The hybrid pixel in image sensing mode. The equivalent circuit is shown inside the elipse.

reverse biased parasitic p-n junction diode. And therefore, more charges are expected to flow into the energy-harvesting bus in form of current $I_{harvest}$, and thus, more energy will be harvested. It's worth to mention that if all the pixels in an M x N array are configured to work in the energy harvesting mode, then the product of M rows by N columns represents the amount of the photodiodes in the array that are connected in- parallel, unanimously forming a large light sensing area. With a reasonable photodiode size, a certain amount of energy can be harvested by the M x N pixels array.

When a request to capture an image is initiated, the hybrid pixel switches to work in image sensing mode. To work in the image sensing mode, the hybrid pixel is selected

by a ROW = 1 and $\overline{ROW}$ = 0 first, and a 0 is written to the latch by making the value on COL = 0. When ROW goes low, the latch retain its value (i.e. 0) and the COL value is not able to write the latch value until ROW goes back high again, this can be seen in Fig. 9. Since the latched value is 0, the switches control signals L1 goes low and L2 goes high, and thus, switches S1 and S2 are in closed position. In contrast, S3 and S4 sre opened. Therefore, the pixel circuit can be simplified to an equivalent circuit as depicted by the circuit inside the ellipse shape in Fig. 9. Once the photodiode contacts are connected to the photo-current bus and to the ground respectively, the input switch of the integrator is closed by $Sin = 1$ keeping the photo-current bus voltage constant by the virtual V_{ref}, and hence, the photodiode's cathode is kept at V_{ref} volt with respect to the photodiode's anode contact (ground). The reverse bias current, proportional to the incident light, flows from the pixel all the way down to the integrator. The current, I_{photo}, is accumulated (integrated) for a well-defined interval (the integration time, T_{intg}). The integrator produces a voltages proportional to the photo generated current, I_{photo}, and to the integration time, T_{intg}. The output voltage can be described by the following equations:

$$V_{out} = V_{ref} + \frac{1}{C_f}\int_0^{T_{intg}} I_{photo} dt$$

which can be simplified to:

$$V_{out} = V_{ref} + \frac{T_{intg}}{C_f} I_{photo}$$

The second equation shows the linear relationship between the output voltage,

$Vout$, of the integrator and the photo generated current, I_{photo}, such that, if V_{ref}, T_{intg}, and C_f are kept constant then the output voltage, V_{out}, increases linearly when the photo generated current, proportional to the light illumination, increases. This is, in fact, one of the advantages of using the current-mode approach in designing the image sensor.

Once the output voltage is produced, an off-chip analog-to-digital converter can be used to digitize the output voltage for the particular pixel. After the digital value is obtained, S_{in} goes low to isolate the integrator circuit from the bus and a reset pulse, S_{rst}, is initiated to discharge the feedback capacitor, C_f, and keep V_{out} at constant level, V_{ref}. The integrator circuit is ready to repeat the process with the next pixel in the row. The next pixel in the row will switch to work in the image sensing mode, while the previous one switch back to energy harvesting mode.

3.2.3 **Design and Layout of The Proposed Hybrid Pixel**

The schematic and the layout of the proposed hybrid pixel has been implemented using Cadence 6.1 Virtuoso tools with ON Semiconductor design kit CMOS $0.5\ \mu m$ process. A schematic snapshot is shown in Fig. 10.

Initially, several goals have been targeted in the implementation of the pixel such us:

- Employ as small as possible amount of electronics inside the pixel. The goal is to achieve a high fill factor, that is, a high photosensitive area with respect to the pixel size. The bigger the sensitive area, the higher the photo generated current is.

- Get the highest use of the chip area. In other words, target a pixel's size that fulfill

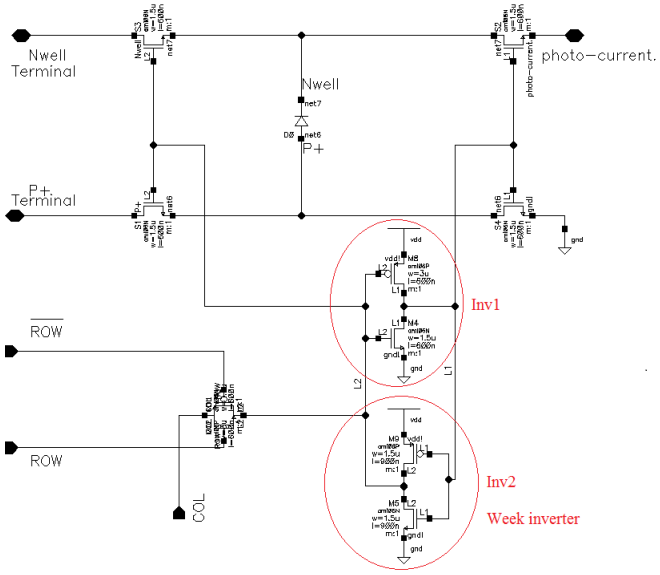

Figure 10: Schematic snopshot for the proposed hybrid pixel.

the required operations and is suitable to design the biggest possible array within a targeted chip of $4\ mm^2$.

- The power consumed by the pixel's circuit and/or by the peripheral circuits has to be as low as possible.

As depicted in Fig. 10, the switches S1, S2, S3, and S4 has been implemented by using n-type MOSFETs with minimum size allowed by CMOS $0.5\ \mu m$ technology process. Table 2 summarizes the sizes of every components that have been used to implement the pixel circuit.

The fact that the photo generated current is in range of $pico - amps$ to $nano - amps$ played the major role in choosing the switches sizes to be the minimum allowed size because the minimum size transistor is capable of handling such range of currents.

Table 2: Hybrid Pixel Component's Characteristics

Component	Width(W) μm	Length(L) μm
S_1	1.5	0.6
S_2	1.5	0.6
S_3	1.5	0.6
S_4	1.5	0.6
TG(PMOS)	1.5	0.6
TG(NMOS)	1.5	0.6
Inv1(PMOS)	3	0.6
Inv1(NMOS)	1.5	0.6
Inv2(PMOS)	1.5	0.9
Inv2(NMOS)	1.5	0.9

The number of MOSFETs inside the pixel is ten, including a basic memory cell (latch) composed of two inverters. However, certain facts have to be consider when designing such bi-stable circuits to assure stability and low-power operation. As depicted in Fig. 7 and Fig. 10, inverter Inv2 provides positive feedback and is sized with small W/L ratio so that Inv1 does not need to supply a large amount of DC current to force the latch to change states.

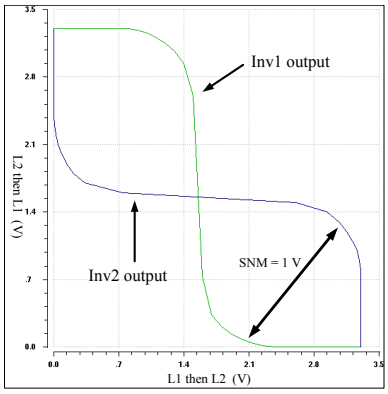

Figure 11: Butterfly plot resulted by simulating the latch circuit.

Fig. 11 shows the post-layout butterfly plot of the latch's inverters, the static noise margin is $1\ V$ which provides information about the immunity level of the latch in responding to noise cliches. At the same time, the figure shows that inverter, Inv1, has higher gain than Inv2 to achieve a low-power overriding operation.

After getting good results from simulation, the switches S1, S2, S3 , and S4 were laid out along with the latch and a p+/Nwell type p-n junction photodiode in one cell to finalize one hybrid pixel as shown in Fig. 12.

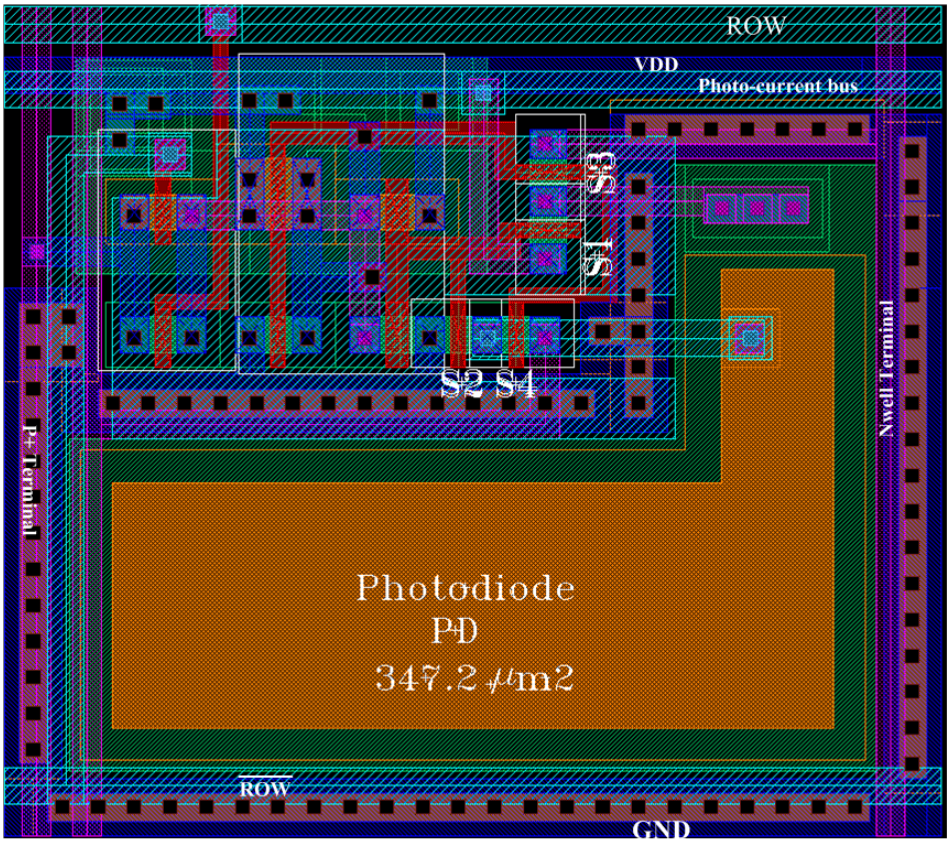

Figure 12: Layout view of the proposed hybrid pixel in ON Semiconductor $0.5\ \mu m$ CMOS technology. The pexil ocupies an area of 35x39 μm^2.

The pixel's layout have an area of approximately $39\ \mu m$ x $35\ \mu m$ with a p-n junction photodiode's area of $347.2\ \mu m^2$. The fill factor will be:

$$\frac{pn\ junction's\ area}{total\ pixel's\ area} \text{ x } 100\% = \frac{347.2}{1365} \text{ x } \ 100\% = 25\%$$

In addition to the fill factor, the p-n junction photodiode itself has been surrounded with a guard ring connecting the p-substrate to the ground in order to overcome the effect of the cross talk between the pixel itself and the neighbor's pixel in the array, and to prevent the electron-hole pairs that are generated outside the photodiode from affecting the current that is read from the photodiode. The transistors inside each pixel are shielded with metal-3 as well to overcome the electronics from generating electron-hole pairs.

Unfortunately, the NCSU design kit for the target process does not have a model for photodiode, therefore a photodiode was modeled by a current source and depletion capacitance to simulate the photodiode's functionality. To test the diode in simulation, the diode's current source is swept from 0 to 100 nA to simulate the effect of light. The capacitor is fixed to a constant value of 50 fF. The current is measured at every terminal that connects the pixel to a bus, the simulation results are shown in Fig. 13 and Fig. 14.

Fig. 13 and Fig. 14 show the dual-functions of the pixel. In both figures, the linear relationship between the simulation current source and the currents in the buses is clearly depicted. The linearity of the current is very important feature when designing image sensors.

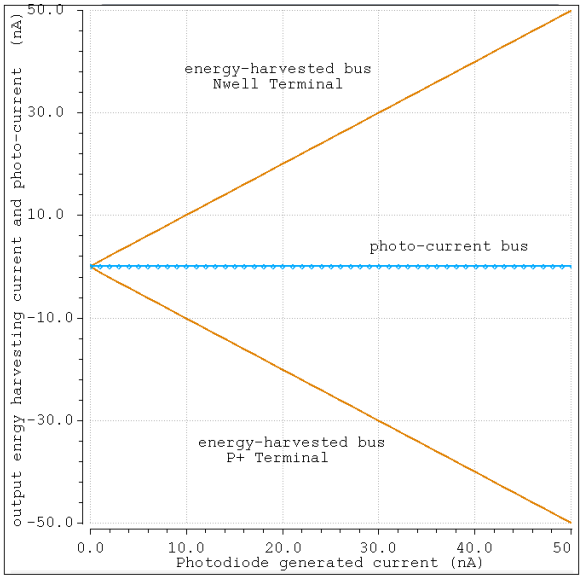

Figure 13: Post-layout simulation of the pixel: S3 and S4 are closed by programming '1' to the latch (energy harvesting mode).

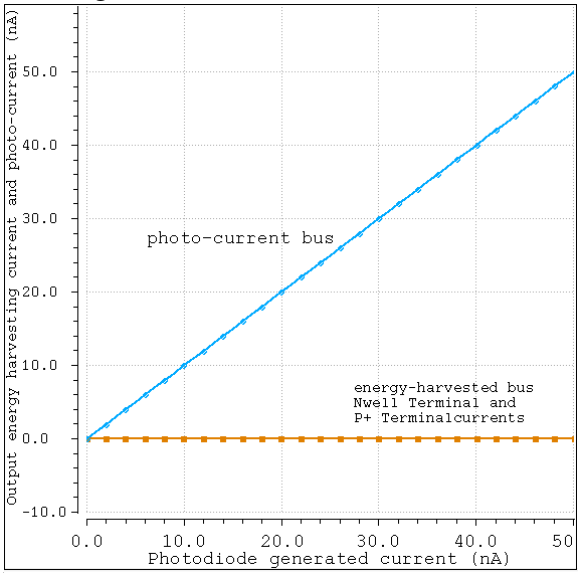

Figure 14: Post-layout simulation of the pixel: S1 and S2 are closed by programming '0' to the latch (image sensing mode).

3.3 Proposed Current-Mode CMOS Hybrid Image Sensor (Design and Implementation)

3.3.1 Hybrid Image Sensor Overview

As a proof of concept a 40 x 40 array of hybrid pixels has been designed and fabricated in a standard $0.5\ \mu m$ CMOS fabrication process. The block diagram of the proposed current-mode CMOS hybrid image sensor is illustrated in Fig. 15. The chip contains an array of a 40 rows by 40 columns of hybrid pixels, row and column shift registers, and three signal buses to convey the currents generated in the pixels to off-chip. At the intersection of a row line and a column line of the array is a hybrid pixel, and all the pixels are identical. Each one of these pixels has six terminals, three of them are produce input signals generated by a photodiode inside the pixel and the other three are used to control the in-pixel latch, a two complementary enabling signals, ROW and $\overline{ROW}$, and a data signal COL.

The contents of the latch for a certain pixel governs the functionality of that pixel, and directs the signal generated by the photodiode to an off-pixel signal bus depending on the pixel functionality. Outside the array there are row and column shift registers. Each register has a 40 parallel outputs and each output produces a control signal to all the pixels in the corresponding row or all the pixels in corresponding column. The output of the first stage of the row shift register is separated into a complementary pair by the line driver. The complementary pairs are connected to all the 40 pixels in the first row of the array via ROW and $\overline{ROW}$. The output of the first stage of the column shift register is connected directly to all the pixels in the first column of the array via COL terminals in the pixels

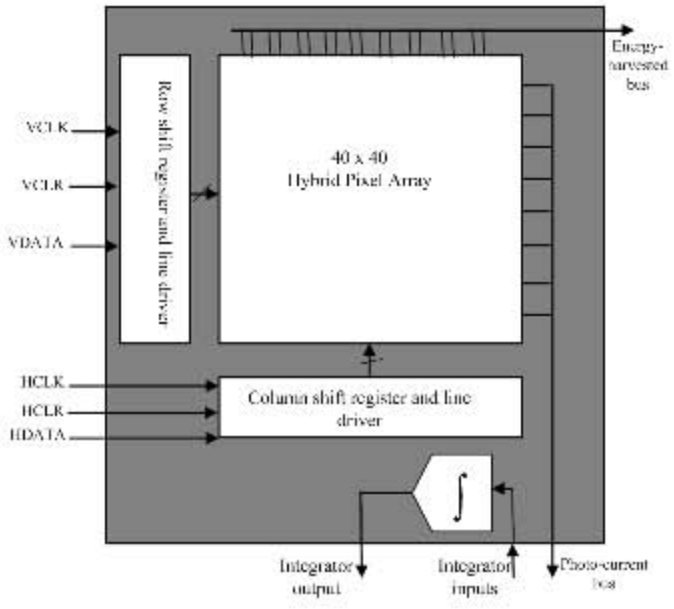

Figure 15: The block diagram of the proposed current-mode CMOS hybrid image sensor; the shaded area is the chip.

and the same procedure has been followed for the rest of the outputs accordingly. The value of the outputs of the row shift register enables or disables the entire row such that if the output of the row shift register is high, every pixel in the corresponding row will be allowed to overwrite the content of the in-pixel latch. The in-pixel latch bit can be written by using the pixel's input COL. The new bit value is provided by the column shift register. If the output is low then the data will be ignored and the latch will retain the previous saved value. While the output value of the row shift register enables or disables the rows in the array, the output values of the column shift register sets the contents of the latches which in turn sets the functionality of each pixel. If the in-pixel latch value is low then the pixel works as a photosensor and it is suitable for image sensing. In the sensing mode, the two contacts of the photodiode are connected to the photo-current bus and to

ground. If the in-pixel latch value is high, then the pixel works in the energy harvesting mode. In the energy-harvesting mode, the two contacts of the photodiode are connected to the energy-harvesting bus and disconnected from the photo-current bus. The energy-harvested bus and the photo-current bus are brought off-chip. The main idea is that each pixel can achieve dual-functions, one at a time, image sensing and energy harvesting such that some pixels are used to sense an image and the rest of the array's pixels can harvest energy from the incident light. The row and column shift registers allow a variety of selections to be made within the array such that one can select half of the pixel array to harvest energy and the other half to sense image and viceversa. The row and column shift register are controlled by external signals, 3 signals for each shift register. The required control signal for the row shift register are clock, VCLK, clear, VCLR, and serial input data, VDATA. The required control signal for the column shift register are clock, HCLK, clear, HCLR, and serial input data, HDATA. Providing the row and column shift register's control signals externally gives a flexibility in the test process. Moreover, an integrator is designed on-chip as shown in Fig. 15. The inputs and outputs terminals of the integrator are available off-chip. This, in turn, allow for multiple patterns of configuration during the test process. In addition, the digital components in the chip are connected to a digital Vdd bus and the analog circuits is connected to an analog $Vdda$ to keep the noise of the digital circuitry away from the sensitive signals of the analog circuitry.

The chip has been designed and implemented using Cadence 6.1 tools as shown in Fig. 16, the area occupied by the array is $1560\ \mu m$ x $1400\ \mu m$. The chip was fabricated using ON Semiconductor $0.5\ \mu m$ CMOS technology process through the MOSIS service.

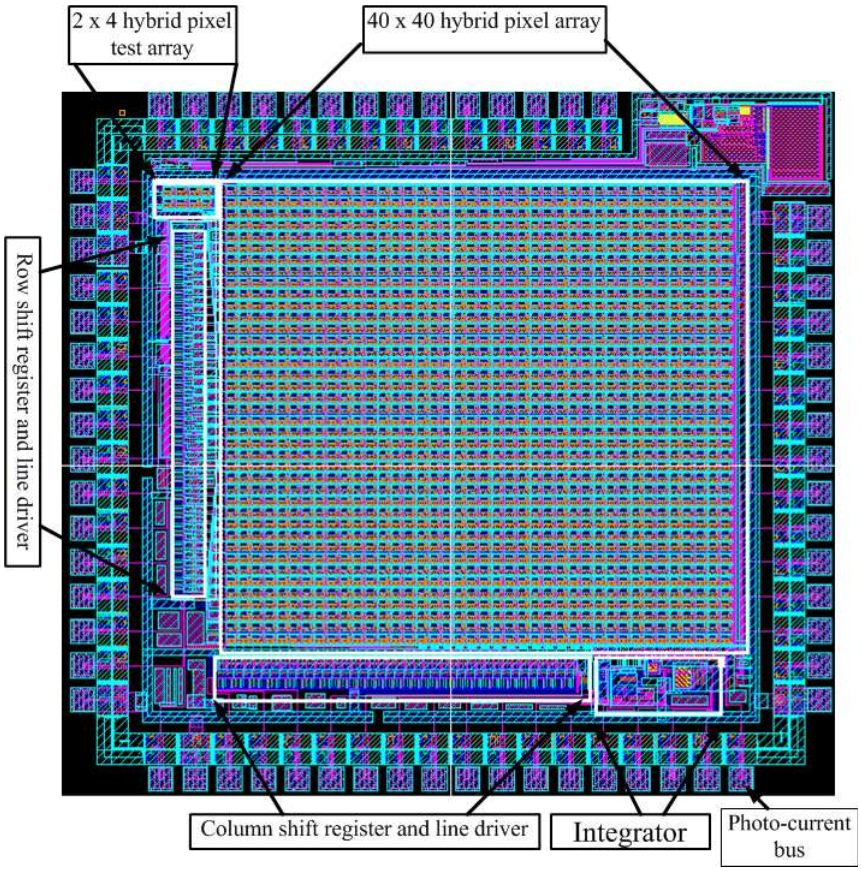

Figure 16: The layout view of the proposed current-mode CMOS image sensor.

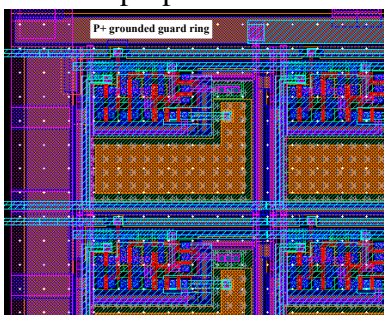

Figure 17: The top left corner of the array; array p+ type guard ring for interference reduction and noise minimization.

3.3.2 **40 (Horizontal) x 40 (Vertical) Hybrid Pixel Array**

A 40 x 40 hybrid pixel array was implemented on the proposes image sensor. A bottom-top approach was followed by instantiate the hybrid pixel's cell in Fig. 14 repeatedly. The area occupied by the array is $1560\ \mu m$ x $1400\ \mu m$. A noise minimization techniques in [23] are applied in the pixel level and in the array level. These techniques include:

- A grounded p+ type guard ring is constructed around each pixel and around the array as well. The guard ring help to minimize the noise generated by the shift registers and the integrator. The guard ring is shown in Fig. 17, where the array is surrounded by grounded p+ type guard ring.

- The peripheral circuitry is kept as far as possible from the array. Especially the row and the column shift registers because they are in the neighborhood of some rows and columns of the pixel array.

- The sensitive analog signal's buses like the photo-current bus and the energy-harvested bus are shielded and routed carefully so that there are no intersection with the digital circuitry signals.

- There are digital and analog power routes separated from each other so that the glitches associated with the digital circuitry would not impact the analog signals generated by the pixels in the array.

3.3.3 The Row and The Column Shift Registers

The row and the column shift register are identical and they are composed of 40 positive-edge master-slave D flip-flop connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. All the flip-flops share a common clock bus and clear bus so that all the flip-flop reset simultaneously. The first flip-flop in the chain receives the external data input serially and then shifts the data to the next stage with each clock pulse. Fig. 18 shows the block diagram of the shift register.

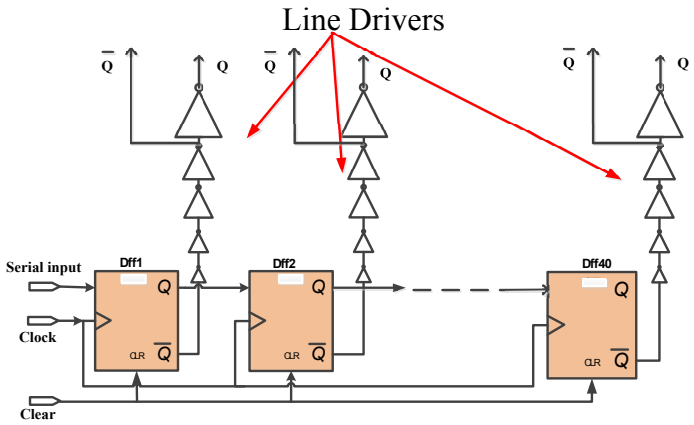

Figure 18: The block diagram of column and row shift register and line driver; the shift register is serial-input-parallel-output. For the row shift register, Q and Q' are used to derive each row in the array. For the column shift register, Q is used to derive each column in the array.

The output of each flip-flop is connected to a bus driver (a buffer) so that the output will be strong and sharp when its applied to the entire pixel array. The two output terminals from the bus driver are used to drive the complementary enable signals, ROW and $\overline{ROW}$, required for the operation of the transmission gate of the in-pixel latch. For the shift register used to drive the columns, only a single terminal (Q) is used to provide

the data to the in-pixel latch. Fig. 19 shows the layout of three stages of the shift register including the input stage. The power consumption and the compact design considered as priority in the design of the shift register.

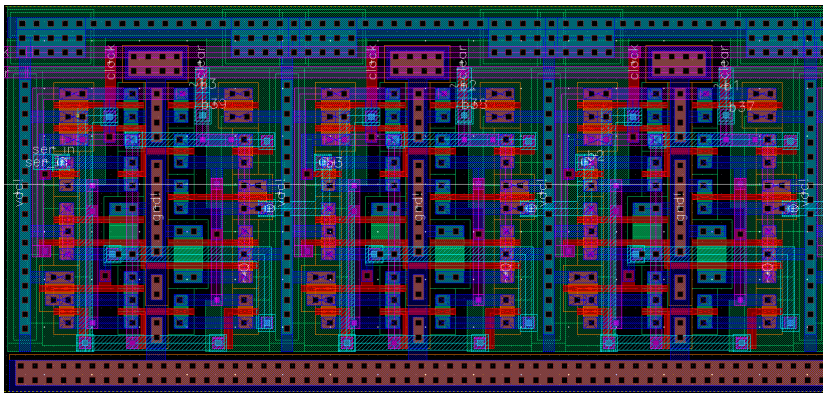

Figure 19: Layout view of a 3 shift register's stages.

The bus driver is composed of a chain of inverters. The size of each inverter is three times bigger than the size of the preceding inverter. The buffer has been laid out considering specific techniques to prevent latch up and to prevent the buffer from consuming a lot of power. These techniques includes surrounding the n-well and the p-well of the driver's inverters by a n+ type and p+ type guard rings separately. The n+ guard ring is biased at digital power supply and the P+ guard ring is grounded. Both rings are kept as close as possible from each other to prevent latch up. The other technique is to connect the gates of the inverters of the driver with metal, instead of using poly, to achieve the low power consumption.

3.3.4 **The Integrator**

Once the photo-generated current (I_{photo}) flows in the photo-current bus, its output is then suitable for any current-mode image processing techniques. To ensure the uniformity measurements, the output of the photo-current bus is connected to the integrator.

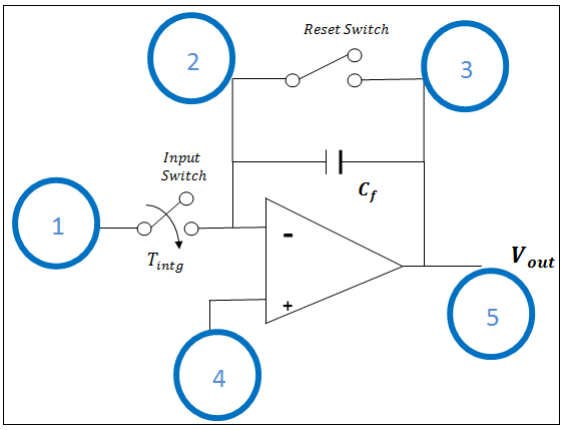

Figure 20: The integrator. Points 1, 2, 3, 4, and 5 are available off-chip.

As depicted in Fig. 20, the integrator consist of an operational amplifier with feed back capacitor (C_f), an input switch, and a reset switch. The operational amplifier is a two stage type op-amp. The input switch and the reset switch are implemented in form of transmission-gate. Point 1, 2, 3, 4, and 5 (V_{out}) as shown in Fig. 20 are all available off-chip. This, in turn, allow to configure the integrator circuit in many forms such as: to form a single-slope analog-to-digital converter, an external ramp signal can be applied to the positive node of the op-amp (node 4), given that a comparator circuit is available on-chip but not shown in Fig. 15. However, the essential purpose of the integrator in the proposed image sensor is to convert the photo-generated current into a proportional voltage. The

reason behind this conversion is that, the available lab equipments are reliable and easy to use in measuring the voltages rather than the currents. Alternatively, for a continuous-time mode operations, a tranresistance amplifier can be used off-chip to perform current-voltage conversion. C_f with value of $500\ fF$ are implemented on-chip. Since points 2 and 3 in Fig. 20 are available off-chip, therefore, C_f can be increased or decreased by either adding external capacitor in-parallel or in-series, respectively.

The integrator is designed and implemented using Cadence 6.1 tools, the post-layout simulation result is shown in Fig. 21.

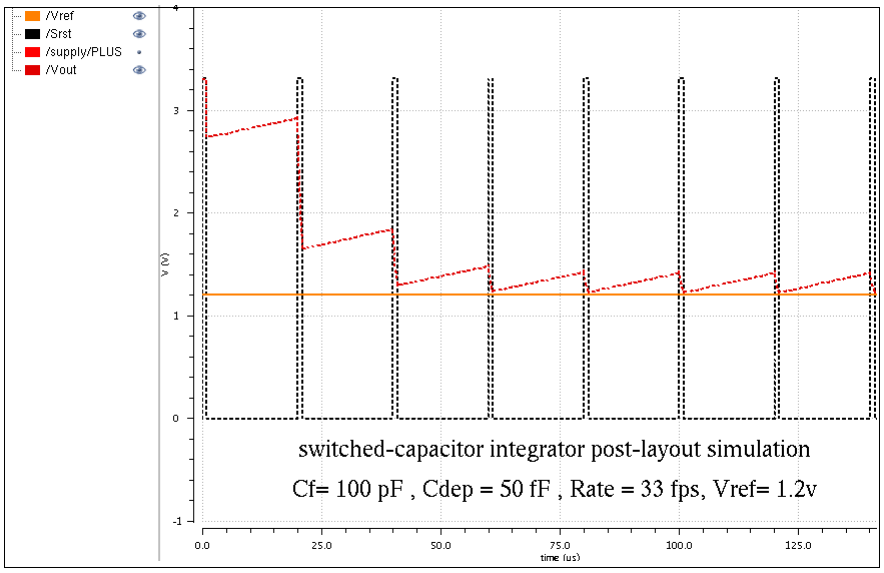

Figure 21: The post-layout simulation result of the integrator. The photodiode model is connected to the inverting input of the operational amplifier through the input switch.

The same photodiode model that is used in simulating the hybrid pixel circuit in section 3.2.3 is used again to simulate the integrator. The photodiode model is connected to the input switch of the integrator. The feedback capacitor C_f is selected to be $100\ pF$,

V_{ref} is kept constant (1.2 V), and S_rst is selected to discharge the C_f every $20\ \mu sec$.

As shown in Fig. 21, V_{out} increases linearly proportional to the simulated photodiode current source. When S_rst goes high, the dashed black waveform in the figure, the reset switch is closed. This, in turn, discharge C_f, therefor V_{out} return to V_{ref} level (1.2 V) as depicted in Fig. 21.

3.3.5 The Chip Implementation

The current-mode CMOS image sensor chip has been fabricated using ON Semiconductor CMOS $0.5\ \mu m$ technology process. The chip is packaged with Kyocera 65-pin ceramic PGA package. In addition to the array and the peripheral read out circuitry, there are 2 x 4 hybrid pixel array and some other electronics were designed on the chip for future experiments and tests. Moreover, all the electronics except the photodiodes are shielded with a top layer metal. Fig. 22 shows the chip. The chip was fabricated through the MOSIS service.

3.4 Summary

In this chapter, a current-mode CMOS hybrid image sensor is proposed. The operating modes, the hardware design and implementation of the proposed hybrid pixel and the proposed image sensor are discussed in detail. The proposed sensor has been fabricated and presented in the end of the chapter. Simulations have been carried out to utilize the dual functions of the proposed hybrid pixel. The simulation results showed the ability of programming the hybrid pixel individually to perform two functions: image sensing and energy harvesting.

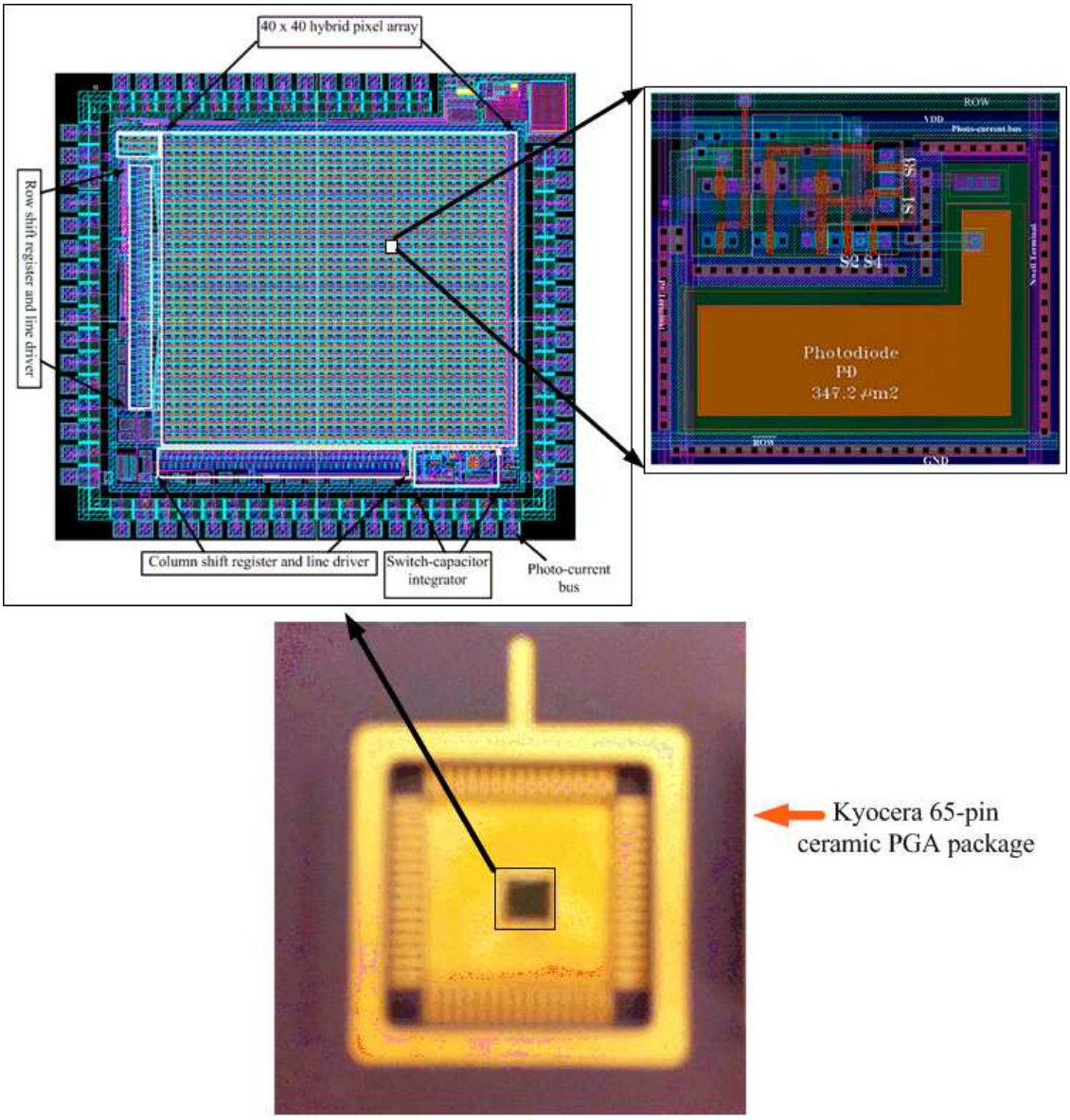

Figure 22: The chip with Kyocera 65-pin ceramic PGA package.

CHAPTER 4

MEASUREMENTS AND RESULTS

4.1 Introduction

As mentioned in Chapter 3, as a proof of concept, a test chip containing a 40 x 40 array of hybrid pixels, address shift registers and an integrator was designed and fabricated in a CMOS $0.5\ \mu m$ technology process. A printed circuit board (PCB) was designed and fabricated to host the test chip and the supporting circuitry. The chip was outfitted with a lens and mounted on the PCB.

Two experiments were carried out. We will call them the energy harvesting experiment setup and the image sensing experiment setup, respectively. In the energy harvesting experiment setup, the I-V curve of 2 x 4 test array and the main 40 x 40 hybrid pixel array were obtained under various conditions. The I-V curve is the best way to measure the photodiods response when they are under various levels of illumination. In the image sensing experiment setup, the pixel array functionality to acquire images is targeted.

In section 4.1 we illustrate the printed circuit board (PCB) components. Then in section 4.2, the energy harvesting experiment setup, measurements, and results are presented. The image sensing experiment setup, measurements, and results are presented in section 4.3. In section 4.4, the chip components power consumption are calculated. Followed by section 4.5 which summarizes the chapter.

4.2 The Printed Circuit Board Components

A photo of the printed circuit board (PCB) used to host the test chip is shown in Fig. 23.

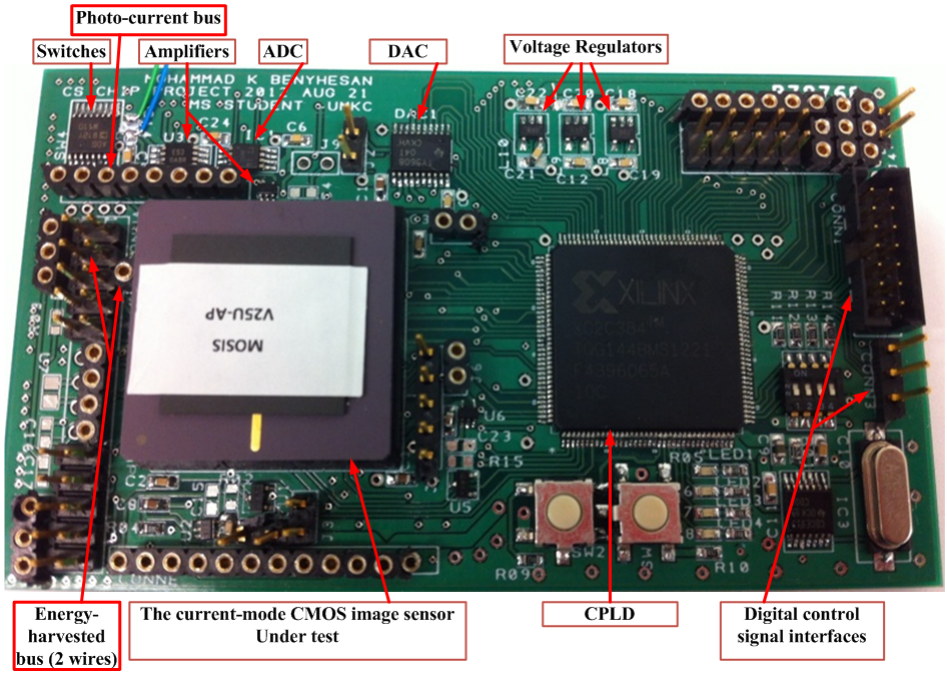

Figure 23: The printed circuit board used to host the test chip

The major components on the board include the test chip, two instrumentation amplifiers, a 12-bit analog-to-digital converter (ADC), voltage regulators, and a digital-to-analog converter (DAC). The voltage regulators provides 3.3V for analog chips and +3.3V, +1.8V for digital chips. Lens and lens mount assemble on top of the image sensor (test chip). There are 4 analog outputs coming out of the hybrid image sensor test chip. Three outputs correspond to each one of the chip current buses and one output correspond

the integrator output voltage. The output from the integrator is buffered by an ultra-low-power, low noise, rail-to-rail instrumentation amplifier (model: OPA369 from Texas Instruments). The output of this buffering stage is single-ended. The final analog signal is then digitized by a 12-bit, 200KSPS, low power serial analog-to-digital converter (model: TLV2542IDGK from Texas Instrument). The digital control signals are generated by a CPLD (complex programmable logic device, model: XC2C384 CoolRunner-II from Xilinx). The programming code is written in VHDL and loaded into the CPLD through a JTAG interface. The in-system programming ability of the CPLD provides high flexibility for generating the timing pattern of the control signals. Special timing patterns, such as the ones for varying the integration time or addressing a specific row or column, can be programmed into different files and easily download into the CPLD within seconds through the JTAG interface. A high-speed, single-supply, rail-to-rail Op Amps (model: OPA2353 from Texas Instruments) and a quad SPST switches (model:ADG812 frm Analog Devices) are used to form an external integrator to integrate the photo-generated current from the photo-current bus and convert the current into readily voltage. The external Op Amp and the switches can be configured to form a transimpedance or transconductance amplifier. The energy-harvested bus is accessible through two pins in the PCB as shown in Fig. 23. The communication between the PCB and the PC is accomplished by JTAG interface cable and FTDI cable through the digital control signal interface. A crystal and clock synthesizer are required by the CPLD to operate. The crystal and the clock synthesizer along with an input switches and a LEDS occupy the bottom right corner of the PCB. Finally, all the required biasing voltages are provided by a DAC (model:

TLV5608 from Texas Instrument).

4.3 Energy Harvesting Experiment Setup

The energy harvesting experiment setup is shown in Fig. 24. The major parts of the experiment setup are the PCB, a source-meter instrument (model: 2400 Broad Purpose SourceMeter from Keithley Company), a PC with special software to manage the source-meter device, and a variable light source.

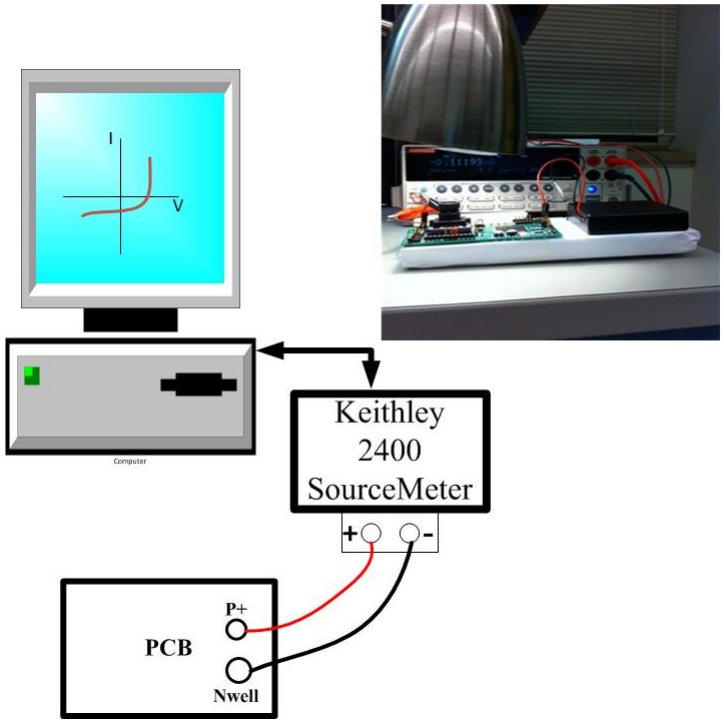

Figure 24: Energy harvesting experiment setup: the energy-harvested bus (Nwell Terminal and P+ Terminal wires) pins in the PCB are connected to the Source-Meter device's probes

The source-meter probes are connected to the energy-harvested bus. The energy-harvesting bus (Nwell Terminal and P+ Terminal wires) is brought from inside the chip to outside through the chip pads and pins. The pins are connected to a 2 header pins on the PCB. The Nwell Terminal pin is connected to the negative probe of the source-meter device and the P+ terminal is connected to the positive probe. The source-meter applies a range of voltages in incremental steps, usually the range from -0.5 to +0.5, and it reads the current flow in the loop with each voltage value. The source-meter presents the collected measurements in form of I-V plot.

The hybrid pixel in the chip's array are programmed to work in the energy harvesting mode. A VHDL code was written to program the CPLD to initiate the required control signals for the chip row and the column shift registers, for example the CPLD pushes 40 bits of logic 1 into the row shift register serially first and then another 40 bits of logic 1 into the column shift register in order to program all the hybrid pixels in the entire array to perform energy harvesting function. This example describes a method to harness the entire array to harvest energy.

4.3.1 Measurement and Test Results

4.3.1.1 2 x 4 hybrid pixel test array

The setup is carried out on a 2 x 4 hybrid pixel test array without lens. The 2 x 4 hybrid pixel test array has been implemented on-chip outside the 40 x 40 main array. The test array control signals ($COL1, COL2, COL3, COL4,\ ROW1, ROW2$), the photo-current bus and the energy-harvest bus, to convey the corresponding currents

from the small array to off-chip, are all available off-chip. The test array of hybrid pixels are programmed in 4 patterns such that: 1 pixel is in harvesting mode, 2 pixels are in harvesting mode, 4 pixels are in harvesting mode, and 8 pixels are in the harvesting mode. In all of these patterns, the rest of the hybrid pixels in the 2 x 4 array are in the image sensing mode. The patterns are generated by programming the CPLD with a VHDL code written for this purpose.

By using the source-meter device mentioned previously, the I-V characteristic is obtained for the full pattern under a fixed illumination condition $\sim$ 5 $Klux$. Fig. 25 shows,on the left hand side, the I-V characteristic obtained with different patterns. The I-V curve is flipped around the horizontal (voltage) axis so that the current is positive and the maximum current is the highest positive value. On the right hand side of Fig. 25, the power generated from the photodiode in the 4 test patterns. The power curves are resulted by multiplying the voltage by the current at every point of the I-V curve.

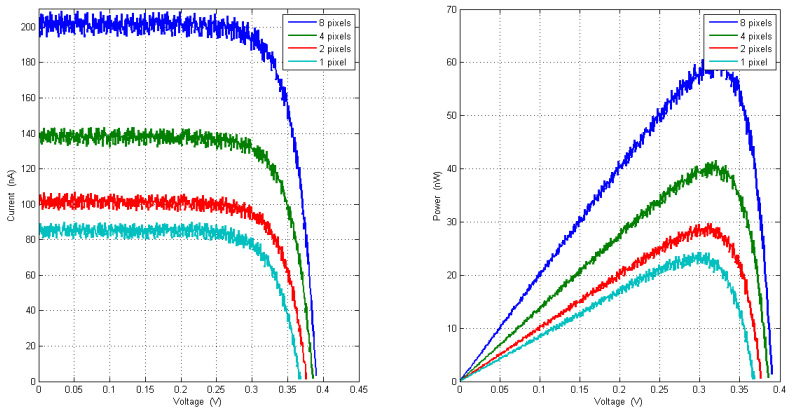

Figure 25: The left hand side plot is the I-V curve of 1, 2, 4, and 8 hybrid pixels working in the energy harvesting mode. The right hand side plot is the power- generated accordingly.

As depicted in Fig. 25, when the number of the hybrid pixels that performing energy harvesting task increases, the power generated increases accordingly. A minimum power is observed when a 1 hybrid pixel is deployed to harvest the light energy and the maximum is observed when 8 hybrid pixels are deployed to harvest the light energy. The minimum power-generated is 24 nW and the maximum is 61.3 nW. A good dynamic range is observed in between the minimum and the maximum power values. Moreover, since the results are varied proportional to the pattern used in the test, then the hybrid pixel success in responding to the pattern code. The in-pixel latch and switches are successfully performing their operation by differentiating the operation mode of each individual hybrid pixel according to the programming pattern code.

4.3.1.2 40 x 40 Hybrid Pixel Array (Dark-Current Measurements)

The dark-current of the 40 x 40 hybrid pixels array was targeted here. The dark-current is the value of the current in the reverse bias region of the I-V characteristic with absence of illumination. A Low dark-current is an important feature of the CMOS image sensors.

The average dark-current for the 40 x 40 hybrid pixel array is obtained via two steps: firstly, the I-V curve of the 40 x 40 array with the absence of the light (i.e. the chip is covered) obtained through the source-meter, and secondly, the obtained I-V data inserted into Matlab to calculate the average current in the reverse-bias region only. The I-V curve is shown in Fig. 26. The dark-current for the 40 x 40 hybrid pixel array with all pixels in energy harvesting mode is equal to $67.2\ pA$. This value is very low and it is

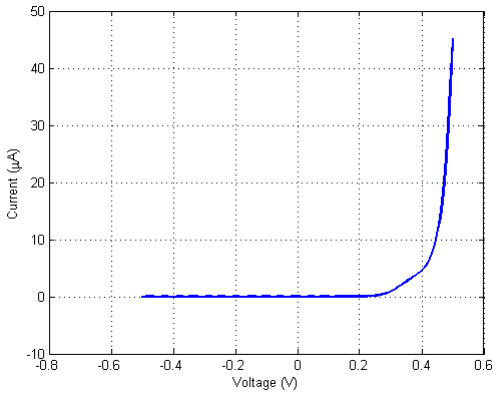

Figure 26: The I-V characteristic of the 40 x 40 hybrid pixel array under no illumination. The dark-current is obtained and it is equal to $67.2\ pA$.

represents the whole 1600 hybrid pixels.

4.3.1.3 40 x 40 Hybrid Pixel Array (energy harvesting measurements)

In this test, a VHDL code is written for the CPLD in order to initiate the control and the timing signals required to program all the hybrid pixels in the entire main 40 x 40 array to work in the energy harvesting mode. A variable light source are then used to illuminate the chip and the lens was removed to allow for accurate measurements. The illumination intensity is varied by varying the light source in a certain steps. A device (light-meter) is used to measure the light intensity at the chip surface. With each illumination intensity level, the source-meter is used to plot the I-V curve of the hybrid pixel array. Fig. 27 is showing the results of this test. In this figure, only the energy harvesting region of the I-V curves is shown and the curves are flipped around the horizontal (Voltage) axis so that the current values are positive in order to ease the calculation of the

power-generated by multiplying each voltage value by its corresponding current value. The collected curves and measurements are then entered to a Matlab code. The Matlab code was used to sort and analyze the measurements to calculate the maximum power-generated from the array.

As depicted in Fig. 27. The I-V curve is shifted up when the in-pixel photodiodes are illuminated. The I-V curve is shifted up proportional to the illumination intensity level. The illumination intensity is varied from 500 lux upto 130 Klux and the short circuit photo-generated current values (on the vertical axis) range is from a few nano-Amps upto 162 μA. Therefore, a high-dynamic range for the power-generated is observed. Fig. 28 shows the power-generated curves obtained from the I-V characteristic in Fig. 27.

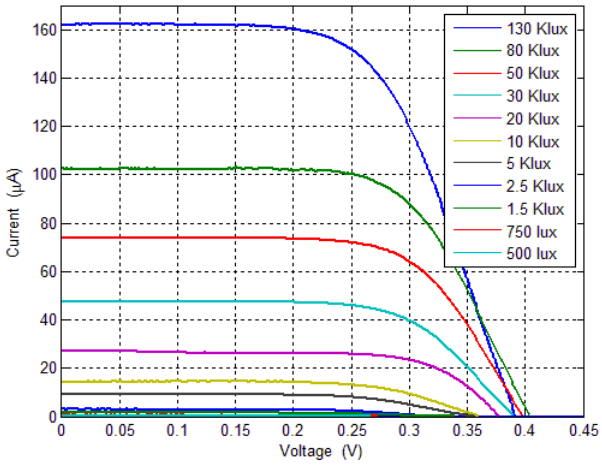

Figure 27: The I-V curves of the 40 x 40 hybrid pixel array under various illumination intensity levels.

As depicted in Fig. 28, a high power dynamic range is observed. The power-generated range is from few micro-Watts for a 500 lux illumination level to 39 μW for

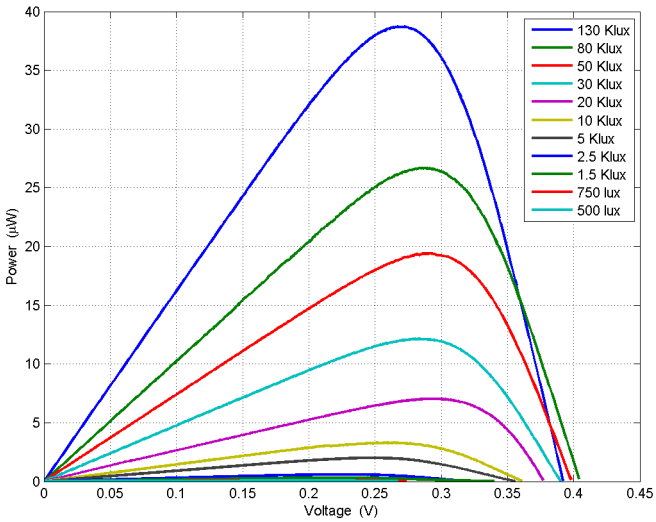

Figure 28: The power-generated from the 40 x 40 hybrid pixel array under various illumination intensity levels. A high power dynamic range is observed.

130 Klux. A power of $\sim 3\ \mu W$ is obtained under 5 Klux (office condition).

The results obtained in this test show the ability of the proposed image sensor array to harvest the light energy. Given that, either all the hybrid pixels in the entire array are working in the energy harvesting mode when there is no image acquiring or all the hybrid pixels in the entire array except one pixel are working in the energy harvesting mode during image acquiring. During image capture, only one hybrid pixel in the entire array is working in the image sensing mode and the rest of the hybrid pixels are in the energy harvesting mode. In conclusion, there is significant amount of harvested energy proportional to the illumination intensity at all the time, while the array acquiring image or not.

4.3.1.4 40 x 40 Hybrid Pixel Array Characteristic With Various Lenses (all the pixels are working in energy harvesting mode)

The target of this test is to utilize the effect of the lens on the amount of the power-generated by the hybrid pixel array. Three different types with different characteristics lenses are used : lens-1 (model: DSL210D from Sunex), lens-2 (model: DSL311 from Sunex), and lens-3 (model: DSL212 from Sunex, as shown in Fig. 29. Each lens was mounted in the chip one-by-one, and then the I-V characteristic of the entire 40 x 40 hybrid pixel array and the generated power measurements with various illumination intensity levels are obtained, Fig. 29 shows the obtained results.

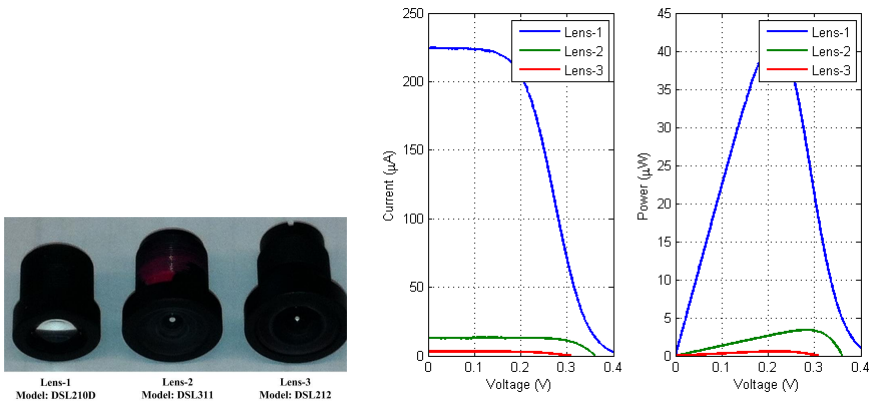

Figure 29: Utilizing the lens effectiveness on the amount of the power-generated from the 40 x 40 hybrid pixel array. The measurements are obtained under 20 Klux illumination intensity.

The peak of the power-generated: with lens-1 is the highest and is equal to $41.577\ \mu W$, with lens-2 is equal to $3.38\ \mu W$, and with lens-3 is the lowest $0.5834\ \mu W$.

A trade off between the amount of the harvested energy and the image quality should consider. For a certain lens type and specification, the lens could focus more light

on the chip surface and causing more energy generation, but that might cause a degradation in the image acquired resolution in the same time since strong exposure could result in higher electron-hole pairs generation in the substrate and/or the electronics in the chip and then these pairs could participate in the photo-current generated by the photodiode itself.

4.4 Image Sensing Experiment Setup

The image sensing experiment setup is shown in Fig. 30. The experiment setup consists of the PCB with lens mounted on the chip, a PC with Matlab software, and a scene.

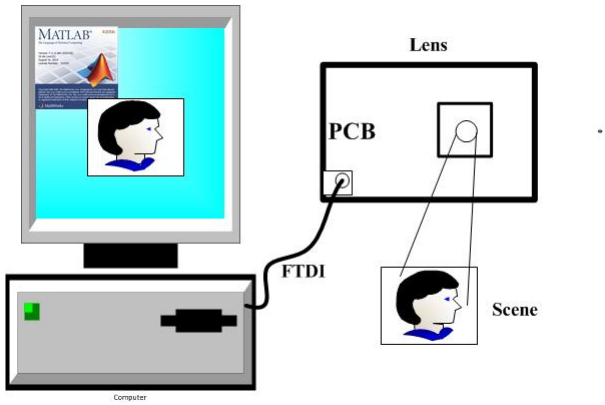

Figure 30: Image sensing experiment setup.

The suggested image capturing procedure can be summarized by means of the control signals generated by the CPLD as follow:

1- CPLD sends a reset signal to the components inside the test chip.

2- CPLD inserts a 40 logic 1 to the column shift register (40 clock cycle), the content of the column shift register is 0xFFFFFFFFFF.

3- CPLD inserts logic 1 to the row shift register (1 clock cycle), the row shift register contains 0x8000000000 .

4- CPLD inserts 0 to the column shift register (1 clock cycle). The column shift register contents becomes 0x7FFFFFFFFF. The pixel associated with this selection is in the image sensing mode now (pixel(1 , 1)).

5- CPLD sends signal to the switches of the integrator, the photo-generated current is flowing in the feedback capacitor. The output voltage of the integrator changes accordingly. After certain time (integration time) the CPLD initiate the required signal for the ADC to digitize the output voltage.

6- The CPLD receives the digitized value from the ADC, and then initiate a process to send this value serially through the FTDI cable to the computer. Matlab grabs this value and saves it.

7- CPLD shifts the contents of the column shift register by 1, and fills the empty by logic 1, the contents of the column shift register is 0xBFFFFFFFFF. This causes pixel(1, 1) to switch to energy harvesting mode and pixel(1 , 2) to image sensing mode.

8- Step 6 and 7 are repeated until the last pixel in the row is read out.

9- Once all the pixels in the row are read out, the CPLD shifts the contents of the row shift register by 1 and inserts a 0 to clear the previous flip-flop. The contents of the row shift register becomes 0x4000000000.

10- Steps 5, 6, 7, 8, and 9 are repeated until all the pixels in the array are readout.

11- By using the saved data in Matlab, the image corresponding to the scene can be seen on the computer by using Matlab tools.

A VHDL code was implemented using Xilinx ISE software and the test has been carried out on steps as follows:

- A VHDL code to program the DAC, the ADC, and the internal and external integrator was written. The code was implemented on the CPLD and the test success. The biasing voltages coming out from the DAC to the chip and the PCB components were measured accurately. Different waveforms were applied on the inputs of the ADC and then the output is obtained correctly on the PC side (Matlab). The internal and the external integrator operational amplifier were tested by forming a source follower via off-chip pins individually. A constant and a ramp wave forms were then applied on the non-inverting inputs of the integrator operational amplifier and the output is measured and observed through the oscilloscope screen successfully.

- The VHDL finite-state-machine code was completed to implement the 11 steps mentioned above. By using Xilinx ISE software, a simulation was carried out first

on the code. Once the transitions of the timing and the control signals observed and they were accurate, the code is implemented on the CPLD. A dip-switch on the PCB was used to variate the integration time in a wide range. The timing and the control signals were checked out of the CPLD pins via the oscilloscope and they were matching the ISE simulation results.

- Once the control signals were observed, the external amplifier was configured in transresistor form with a 10 MΩ feedback resistor. The photo-current bus was connected to the inverting input of the integrator operational amplifier and a 1.2 V (V_{ref}) was applied on the non-inverting input to create a virtual 1.2 V on the photo-current bus which, in turn, used to reverse bias the in-pixel photodiode.

- A request to acquire image was made by pushing a start button on the PCB. The transresistor output signal was observed on the oscilloscope screen. The analog output of the transresistor represents the responsiveness of the array to the light variation during image acquiring time. The images in Fig. 31 are showing the following: starting from the left image, the output analog voltage of the transresistor amplifier that resulted from converting the photo-generated current of the hybrid pixels through the feed back resistor into voltage. The image shows the range of the output voltages, proportional to the light, from 0.4 V above the bias voltage (1.2 V) all the way to 3.3 V. The PCB was elevated from one side gradually towards the ceiling florescent light.

  The image to the right in Fig. 31 shows the response when a piece of paper was used

to prevent the high-intensity florescent light from reaching the lens which causing the output voltage to drop to 1.64 V. This experiment was carried out while the sensor was performing image acquiring task, and hence, the array able to sense a variety of light intensity levels reflected from a scene.

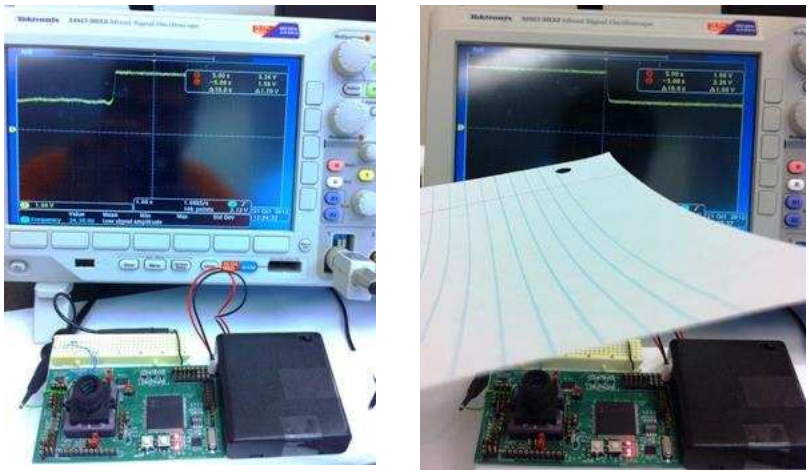

Figure 31: The analog output voltage proportional to the photo-generated current: the output voltage varies with light intensity levels.

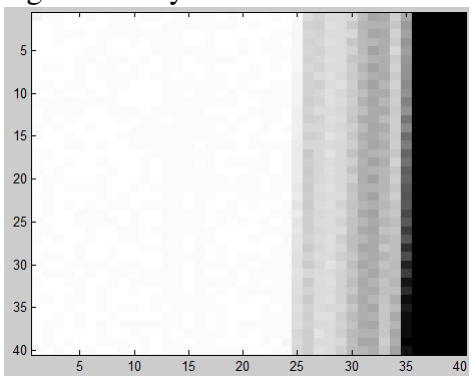

Figure 32: The digital output (image) obtained from Matlab.

The digital output (image) obtained from Matlab is shown in Fig. 32. The image obtained by applying high-intensity light level (the wight area in the image) then by

gradually decreasing the light intensity level (the gray pixels) upto closing the lens totally (the black pixels in Fig. 32).

- The test then was carried out by enabling the internal integrator. An external feedback capacitor is connected in-parallel to the internal 500 fF feed back capacitor. The total feedback capacitor is around 100 pF. The analog output of the integrator is observed via the oscilloscope screen while the hybrid image sensor performing image sensing function. A samples of the analog output are shown in Fig. 33.

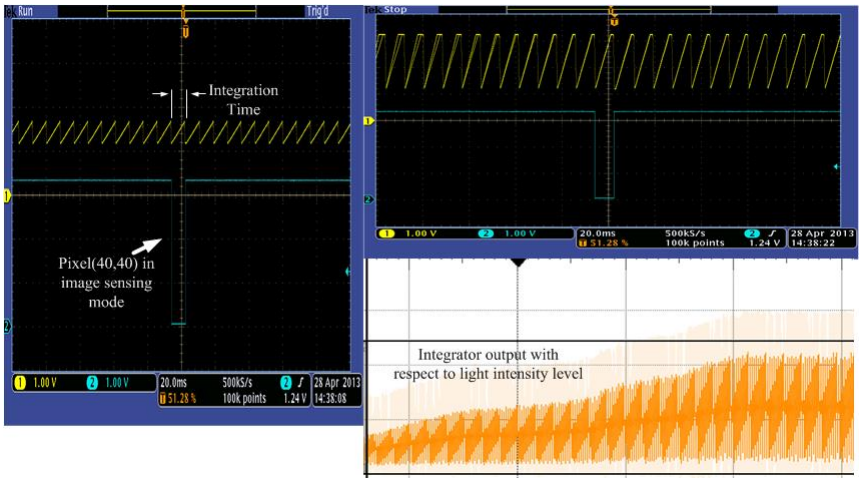

Figure 33: The analog output of the internal integrator.

As depicted in Fig. 33, the output voltage of the integrator is matched the simulation results which obtained in Chapter 3 and it follows the equation:

$$V_{out} = V_{ref} + \frac{T_{intg}}{C_f} I_{photo}$$

as discussed in the Chapter 3. The test on the internal integrator was successfully carried out and the results are matched with the post-layout simulation results.

4.5 Power Consumption and Array Energy Efficiency

The power consumption of the CMOS image sensor is an important performance measure, and hence, the power consumption measurements was carried out through simulating each components of the proposed image sensor individually. The power consumption of the proposed current-mode CMOS hybrid image sensor is comprised of the following:

a- Power consumption of the 40 x 40 hybrid pixel array: when all the hybrid pixels in the entire array are working in the energy harvesting mode, only leakage current is drawn from the on-board power supply. During image sensing, only one hybrid pixel per the array is activated to configure the in-pixel switches in order to perform image sensing task within specific time. Thus, the power consumption of the entire array can be normalized with respect to the frame rate and the number of pixels in the array as follows:

Let F_r represent the frame rate with a unit of fps (frame per second)

$T_r = \frac{1}{F_r}$, where T_r is the duration of capturing one image

$T_{pix} = \frac{T_r}{N}$, where N is the number of the hybrid pixels in the entire array and T_{pix} is the pixel activity time.

For each hybrid pixel during image sensing, T_{pix} sec is the time required for the hybrid pixel to switch from energy harvesting mode to image sensing mode and then switch back to energy harvesting mode. Therefor:

$$P_{pix} = I_{pix} \text{ x } Vdd$$

where P_{pix} is the power consumption of each hybrid pixel, I_{pix} is the average current drown from the power supply within T_{pix} sec, and Vdd is the voltage of the power supply, and therefore, the energy consumed per each hybrid pixel per array (E_{pix}) can be calculated as:

$$E_{pix} = P_{pix} \text{ x } T_{pix} \text{ (joules/pixel/frame)}$$

b- Power consumption of the column shift register and bus driver: during image sensing the column shift register is active only when the pixel is active. Each flip-flop change its value from 1 to 0 to program the in-pixel latch such that the operation mode of the pixel changes from harvesting to image sensing, and then the flip-flop return to 1 after a specific time. Therefore, the same equations that are used in (a) can be used to calculate the normalized energy for the shift register.

c- Power consumption of the row shift register and the bus drivers: the same conclusion in (b) is applicable for the row shift register.

d- Power consumption of the integrator: the integrator is integrating the photo-generated current by the pixel when the pixel in the image sensing mode. Thus, the power consumption follows the activity of the pixel itself. The reset switch is goes high only when the pixel is changing its mode from image sensing to harvesting, and hence, the same equations in (a) can be used to calculate the power consumption of the on-chip integrator.

To calculate the total normalized energy, F_r is selected to be $33\ fps$, and the simulation data entered into Matlab code. The results are shown in Table 2.

Table 3: Energy Efficiency of The Chip, $F_r = 33\ fps$

chip component	Energy
Array	004.10 nJ /pixel/frame
Column shift register	110.76 nJ /pixel/frame
Row shift register	107.10 nJ /pixel/frame
Integrator	006.07 nJ /pixel/frame
Total	228.03 nJ /pixel/frame

The total power consumption is 228 nJ/pixel/frame, where nJ is stand for nano-joules.

4.6 Summary

In this chapter, a test on the proposed hybrid pixel and the current-mode CMOS hybrid image sensor were carried out successfully. The hybrid pixel success in performing the energy harvesting task and the image sensing task. Various tests and scenarios were presented and the results approve the possibility of harness the hybrid image array to harvest the energy from the light.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Summary and Conclusion

The energy harvesting concept presents a viable solution to the on-board power limitation for the portable image sensing devices. The solar cell is the most suitable energy harvesting technique among the available CMOS energy harvesting techniques for the portable wireless image sensors. The essential elements in the image sensor and the solar cell is the photodetector element that convert the incident light to electricity. The connections of the p-n junction photodiode's contacts and the bias condition govern the functionality of the photodetector: image sensor or energy harvester. The p-n junction photodiode in the CMOS image sensor occupies silicon area, but it is not active most of the time (i.e. between frames or during sleeping mode). To get a better use for the p-n junction photodetector, a passive pixel was modified to create a pixel with dual functions: image sensing or energy harvesting. The new pixel is called a hybrid pixel. The hybrid pixel is programmable such that the in-pixel photodiode can be part of the image sensing processing circuit or the energy harvesting collecting and conversion circuit.

In this thesis, the hybrid pixel was designed and presented. The concept of the hybrid pixel were proved by designing and fabricating a current-mode CMOS hybrid image sensor. The chip contains a 40 x 40 hybrid pixel array. The test and the measurements were carried out on the test chip. The concept of the hybrid pixel (i.e. dual functions) were

proved successfully. Moreover, the default function of the hybrid pixels in the array is the energy harvesting function. During image sensing, the pixels in one row are switched to image sensing function on pixel-by-pixel basis and then each pixel switches back to perform the energy harvesting function and the process continues on row-by-row basis. This methodology was used to harness the largest number of hybrid pixels to harvest energy. The test results shows that, the generated power from the array varied with the intensity level of the incident light and the number of pixels that performing the energy harvesting function. The range of the generated power obtained from the test that performed on the proposed current-mode CMOS hybrid image sensor was between few nano-Watts up to 39 μW. The dark-current of the entire array was very low and it is equal to $67.2\ pA$. The benefits of using the current-mode technique to implement the hybrid image sensor were observed such that the output analog voltage were in linear relationship with the photo-generated current and the total power consumed by the image sensor working at rate of 33 fps were fairly low and it is equal to 228 nJ/pixel/frame.

5.2 Future Work

We focused in this work on the concept of exploiting the in-pixel p-n junction photodiode to harvest energy from the light. Future work may include the following:

1) We acquire images by using the proposed current-mode CMOS image sensor. However, the images were acquired with artifact like lines. These artifact are likely due to the fact that we use 3.3 V instead of using 5 V logic levels. This could be improved by designing board that work with 5 V instead of 3.3 V.

2) To boost the power generated by the array, a DC-DC conversion circuit were designed on-board. This circuit contains 7 on-chip switches. The input/output terminals of the switches are all available off-chip. For further work, a test could be done on this circuit to utilize the amount of the energy that could be obtained.

3) The hybrid pixel array can be programmed in random patterns such that some pixels can be selected randomly to perform image sensing at the same time ,and thus, the output photo-generated current represents the sum of product. This feature makes the implementation of compressive image sensing possible.

APPENDIX A

THE CURRENT-MODE CMOS HYBRID IMAGE SENSOR CHIP COMPONENTS AND PINOUT

A.1 The Current-Mode CMOS Hybrid Image Sensor chip components

The block diagram of the chip is shown in Fig. 34.

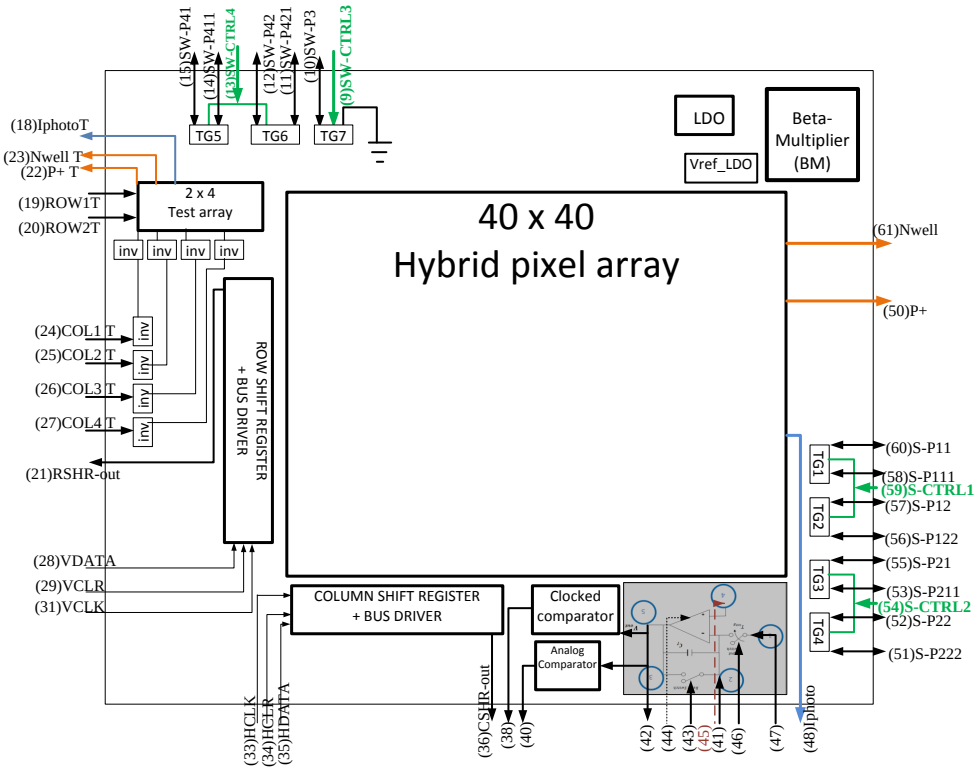

Figure 34: Chip components.

A.2 The Current-Mode CMOS Hybrid Image Sensor Chip Pinout Details

The chip pinout is shown in Fig. 35. The details of each pin is shown in Fig. 36, Fig. 37, and Fig. 38. The chip package number is V25U-AP.

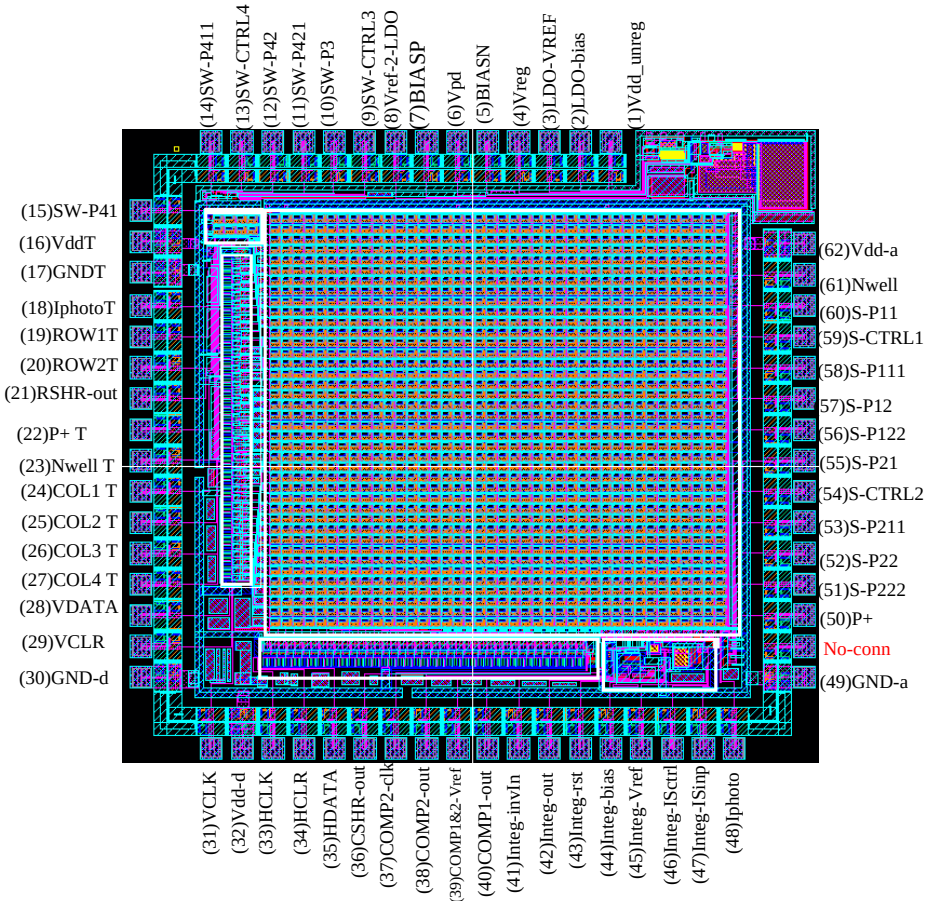

Figure 35: Chip pinout.

LDO

Pin Number	Input/output	Digital/Analog	Comments
(1) Vdd_unreg	Input	Analog	Unregulated Vdd
(2) LDO-bias	Input	Analog	0.7 V
(3) LDO-Vref	Input	Analog	2V to get 3.3V regulated at Vreg Or 1.2V to get 1.8V at Vreg
(4) Vreg	Output	Analog	Regulated LDO output

Beta-multiplier reference

Pin Number	Input/output	Digital/Analog	Comments
(1) Vdd_unreg	Input	Analog	Unregulated Vdd
(5) BiasN	Output	Analog	Page-624 in [23] Approx. 0.7V
(6) Vpd	Input	Analog	Connect to gnda ground to start the startup circuit then connected to Vdda
(7) BiasP	Output	Analog	Page-624 in [23] Approx. 2.2V
(8) Vref-2-LDO	Input	Analog	Connect to BiasP or to ext. 3 V

7 Transmission-gates

(6 (3pairs) with floating in/out and each pair have common control (ctrl1, ctrl2, and ctrl4), and 1 with single floating end and ground end (ctrl3))

Pin Number	Input/output	Digital/Analog	Comments
(9) SW-CTRL3	Input	Digital	Control signal
(10) SW-P3	Input	Analog	TG3's single i/p
(11) SW- P421	Input/output	Analog	TG6
(12) SW-P42	Input/output	Analog	TG6
(13) SW- CTRL4	Input	Digital	Control TG5 & TG6
(14) SW-P411	Input/output	Analog	TG5
(15) SW-P41	Input/output	Analog	TG5
(51)S-P222	Input/output	Analog	TG4
(52)S-P22	Input/output	Analog	TG4
(53)S-P211	Input/output	Analog	TG3
(54)S-CTRL2	Input	Digital	Control TG3 & TG4
(55)S-P21	Input/output	Analog	TG3
(56)S-P122	Input/output	Analog	TG2
(57)S-P12	Input/output	Analog	TG2
(58)S-P111	Input/output	Analog	TG1
(59)S-CTRL1	Input	Digital	Control TG1 & TG2
(60)S-P11	Input/output	Analog	TG1

Figure 36: Chip pinout details table-1.

2 x 4 hybrid pixel test array

Pin Number	Input/output	Digital/Analog	Comments
(16) VddT	Input	Analog	3.3 V
(17) gndT	Input	Analog	Ground
(18) Iphoto T	Output	Analog	Common photo-generated bus
(19) ROW1 T	Input	Digital	Row1 control (In-pixel TG)
(20) ROW2 T	Input	Digital	Row2 control
(22) P+ T	Output	Analog	Common P+ terminal (harvesting)
(23) Nwell T	Output	Analog	Common Nwell terminal (harvesting)
(24) COL1 T	Input	Digital	Data input to in-pixel TG
(25) COL2 T	Input	Digital	Data input to in-pixel TG
(26) COL3 T	Input	Digital	Data input to in-pixel TG
(27) COL4 T	Input	Digital	Data input to in-pixel TG

Vertical (row) shift register

Pin Number	Input/output	Digital/Analog	Comments
(32) Vdd-d	Input	Digital	Digital Vdd (3.3V)
(30) GND-d	Input	Digital	Digital Ground
(31) VCLK	Input	Digital	Clock
(29) VCLR	Input	Digital	To clear the register
(28)VDATA	Input	Digital	Serial input data
(21) RSHR-out	Output	Digital	MSB for test

Horizontal (column) shift register

Pin Number	Input/output	Digital/Analog	Comments
(32) Vdd-d	Input	Digital	Digital Vdd (3.3V)
(30) GND-d	Input	Digital	Digital Ground
(33) HCLK	Input	Digital	Clock
(34) HCLR	Input	Digital	To clear the register
(35) HDATA	Input	Digital	Serial input data
(36) CSHR-out	Output	Digital	MSB for test

Figure 37: Chip pinout details table-2.

Integrator

(on-chip two stage op-amp with 500 fF feedback capacitor, input switch, and reset switch)

Note: Two comparator are designed on-chip for test purposes only

Pin Number	Input/output	Digital/Analog	Comments
(62) Vdd-a	Input	Analog	3.3 V
(49) GND-a	Input	Analog	Ground
(47) Integ-ISinp (integrator-inputswitch-input end)	Input	Analog	The input switch usually connect to the (48) Iphoto pin
(46) Integ-ISctrl(integrator-input switch-control)	Input	Digital	The input switch control signal
(45) Integ-Vref	Input	Anaolg	Integrator reference voltage (non-inverting op-amp terminal). 1to 1.6V.
(44) Integ-bias	Input	Analog	Op-amp bias voltage 0.7 to 0.9 V
(43) Integ-rst (integrator reset switch-control)	Input	Digital	To discharge the feedback capacitor
(42) Integ-out (Integrator output)	Output	Analog	Usually connect to ext. ADC
(41) Integ-invIn (Integrator inverting input)	Input	Analog	To increase the feedback capacitor externally
(40) Comp1-out (Analog Comparator output)	Output	Digital	Two-stage op-amp comparator. The input is already connected to (42)
(39) Comp1&2-Vref (comparator s 1 and 2-reference voltage)	Input	Analog	Usually set to Vdd/2
(38) Comp2-out (clocked comparator- output)	Output	Digital	Details in [25] (this circuit for test only)
(37) Comp2-clk (clocked comparator clock)	Input	Digital	Details in [25]

40 x 40 hybrid pixel array

Pin Number	Input/output	Digital/Analog	Comments
(62) Vdd-d	Input	Analog	Vdd (3.3V)
(49) GND-a	Input	Analog	Ground
(48) Iphoto	Output	Analog	Photo-generated current bus end
(50) P+	Output	Analog	Energy-harvest P+ terminal wire
(61) Nwell	Output	Analog	Energy-harvest Nwell terminal wire

Figure 38: Chip pinout details table-3.

A.3 Transmission Gates Schematic and DC-DC converter details

There are 7 transmission-gates on-chip. The input/output pins of the switches are available off-chip. The PCB allow to design a DC-DC converter consists of the 7 transmission-gates, the energy-harvesting bus (2 pins available on-board) , and an external capacitors. The schematic of the on-chip transmission-gates are shown in Fig. 39.

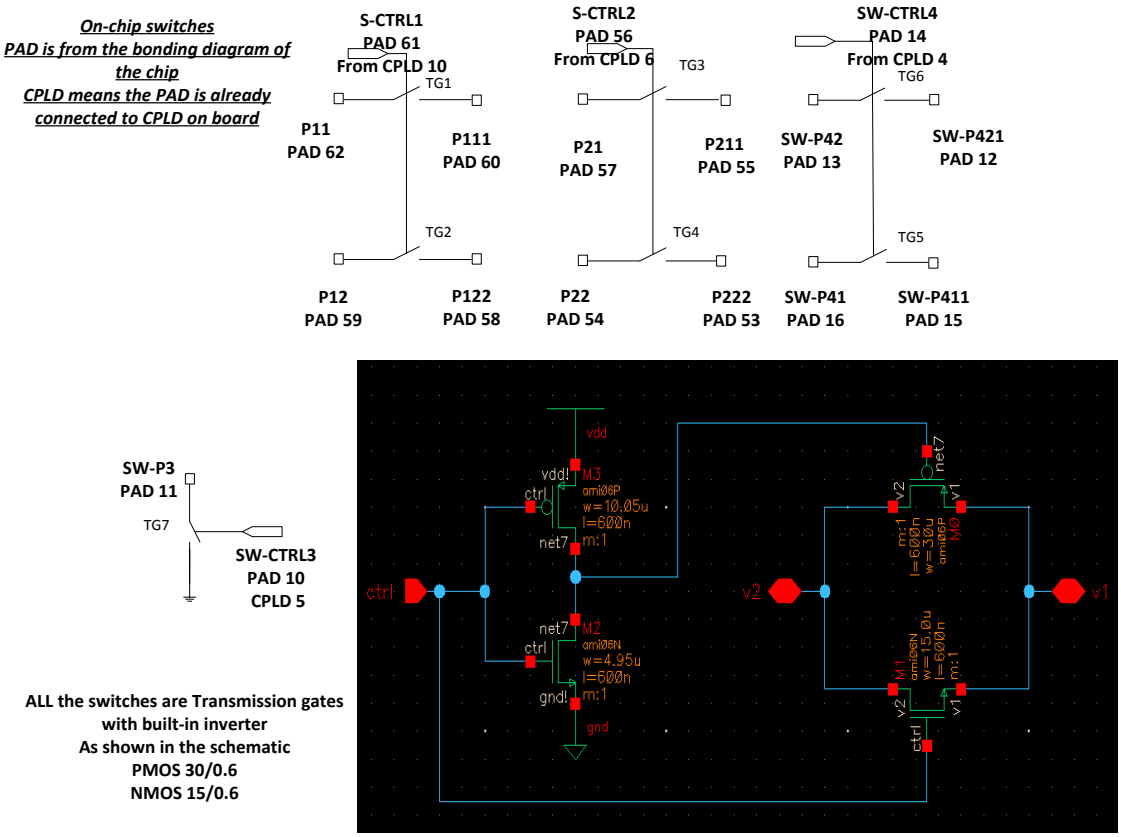

Figure 39: The on-chip transmission-gates schematic.

The DC-DC on-board circuit details can be seen on Fig. 40

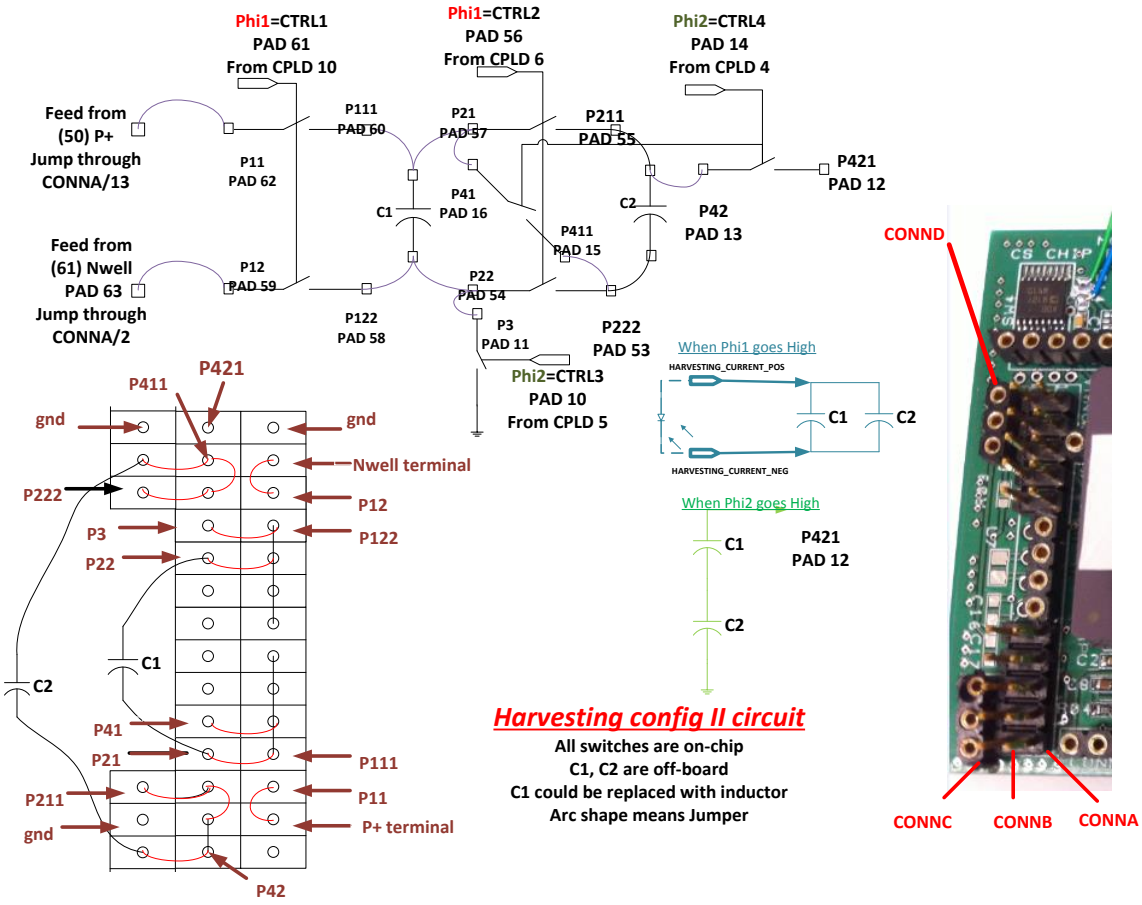

Figure 40: The on-board DC-DC conversion circuit.

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