

SILICON ON FERROELECTRIC INSULATOR FIELD EFFECT
TRANSISTOR (SOF-FET) A NEW DEVICE FOR THE NEXT
GENERATION ULTRA LOW POWER CIRCUITS

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By

Azzedin D. Es-Sakhi

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Missouri-Kansas City, USA 2011

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Azzedin D. Es-Sakhi, Candidate for the Master of Science Degree

University of Missouri - Kansas City, 2013

ABSTRACT

Field effect transistors (FETs) are the foundation for all electronic circuits and processors. These devices have progressed massively to touch its final steps in sub-nanometer level. Left and right proposals are coming to rescue this progress. Emerging nano-electronic devices (resonant tunneling devices, single-atom transistors, spin devices, Heterojunction Transistors rapid flux quantum devices, carbon nanotubes, and nanowire devices) took a vast share of current scientific research. Non-Si electronic materials like III-V heterostructure, ferroelectric, carbon nanotubes (CNTs), and other nanowire based designs are in developing stage to become the core technology of non-classical CMOS structures. FinFET present the current feasible commercial nanotechnology. The scalability and low power dissipation of this device allowed for an extension of silicon based devices. High short channel effect (SCE) immunity presents its major advantage. Multi-gate structure comes to light to improve the gate electrostatic over the channel. The new structure shows a higher performance that made it the first candidate to substitute the conventional MOSFET. The device also shows a future scalability to continue Moor's Law. Furthermore, the device is compatible with silicon fabrication process.

Moreover, the ultra-low-power (ULP) design required a subthreshold slope lower than the thermionic-emission limit of 60mV/decade (KT/q). This value was unbreakable by the new structure (SOI-FinFET). On the other hand most of the previous proposals show the ability to go beyond this limit. However, those pre-mentioned schemes have publicized a very complicated physics, design difficulties, and process non-compatibility. The objective of this research is to discuss various emerging nano-devices proposed for ultra-low-power designs and their possibilities to replace the silicon devices as the core technology in the future integrated circuit. This thesis proposes a novel design that exploits the concept of negative capacitance. The new field effect transistor (FET) based on ferroelectric insulator named *Silicon-On-Ferroelectric Insulator Field Effect Transistor (SOF-FET)*. This proposal is a promising methodology for future ultra-low-power applications, because it demonstrates the ability to replace the silicon-bulk based MOSFET, and offers subthreshold swing significantly lower than 60mV/decade and reduced threshold voltage to form a conducting channel. The *SOF-FET* can also solve the issue of junction leakage (due to the presence of unipolar junction between the top plate of the negative capacitance and the diffused areas that form the transistor source and drain). In this device the charge hungry ferroelectric film already limits the leakage.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Computing and Engineering have examined a thesis titled “Silicon on Ferroelectric Insulator Field Effect Transistor (SOF-FET) a New Device for the Next Generation Ultra Low Power Circuits” presented by Azzedin Es-Sakhi, candidate for the master of science degree, and certify that in their opinion it is worthy of acceptance.

Supervisory Committee

Masud H Chowdhury Ph.D., Committee Chair

Associate Professor, School of Computing and Engineering

Ghulam M. Chaudhry Ph.D

Chair for Department of Computer & Electrical Engineering

Dr. Yang (Cindy) Yi Ph.D

Associate Professor, School of Computing and Engineering

Dr. Deb Chatterjee Ph.D

Associate Professor, School of Computing and Engineering

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Azzedin D. Es-Sakhi
Wednesday, November 20' 2013, Kansas City, MO

DEDICATION

I would like to dedicate my thesis to all my family especially my beloved grandmother

CHAPTER 1

INTRODUCTION

This thesis report deals with the emerging field of ultra-low-power devices. An investigation of various materials and architecture is presented in this thesis. Toward the end of this research a new field concept of effect transistor terminology is introduced and principle of operation is explained.

1.1 Organization

This thesis consists of eight chapters beginning with this chapter. Chapter 1: gives the objectives and scope of the project, background of emerging nanotechnology, as well as the layout of thesis. Chapter 2: presents an introduction to carbon nanotube field effect transistors. This chapter include a short introduction into carbon nanotube, that include the major properties that made the carbon nanotube based field effect transistor the future building block of nano-electronic circuits. Chapter 3: is an introduction to FinFET, the design geometry and a short discussion about the advantage and disadvantage, and the reason behind switching to multi-gate devices. Chapter 4: present the definition of subthreshold swing and discussion of the major factor that control this parameter. A briefly discussion over tunneling Field Effect Transistor that involve various structures and different materials is presented in chapter 5. Chapter 6 presents an explanation and brief summary of I-MOS and Nanowire schemes. Chapter 7 passes the application of

ferroelectric material in Field effect transistor. In chapter 8 an analytical model to approximate the subthreshold swing of SOI- FinFET is presented. In Chapter 9, a new proposal to lower subthreshold swing, and threshold voltage proposed. Chapter 10 addresses the current-Voltage (I-V) characteristics of the *SOF-FET*. Finally, chapter 11 lists the advantages of this proposal, present some manufacturing process, introduce future works and conclude this thesis.

1.2 Thesis Objectives

The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the building block of all computing systems. MOSFETs handled an excessive development in the last decade. However, the advantage of this device starts vanishing in nanometer scale. Researchers are investigating numerous unconventional designs to solve the issue of density and power consumption (especially at standby or sleep mode) of the conventional MOSFET. Nanotechnology proposals to overcome the issues of downscaling and extend Moor's Law wide-ranging from materials substitution point of view going through new architectures and others proposed new physics and/or operating principals.

This thesis present a study of the prospects of emerging FinFET and Carbon Nanotubes (CNTs) based FET device technologies for ultra-low-power subthreshold design, also investigate a new field effect transistor (FET) design based on ferroelectric material to utilize negative capacitance effect in subthreshold design. The nano-electronics is an

emerging field whose goal is not limited to surpass the existing technology but also to present a design with lower power consumption.

The main objectives of this thesis are as follows:

- Understand the emerging technology devices characteristic, fundamental equation and mathematical analysis of subthreshold design.
- Comparing FinFET and CNTFET subthreshold regimes operations.
- An analytical model to approximate the subthreshold swing for SOI-FinFET
- Introducing a new design to lower subthreshold.

1.3 Nanotechnology Challenges

One of the challenges facing the conventional MOSFET is scaling the gate oxide to improve the transistor performance. Scaling-down the oxide thinness will increase the oxide capacitance therefore increasing the drain current, lowering the threshold voltage and improving other parameters as well. Because of thin gate oxide bond-to-bond tunneling occurs through the gate dielectric. Scaling-down of the MOSFET causes the depletion areas of source and drain to be exceedingly close to each other and they can merge. This issue will cause a high current leakage, this phenomenon called Drain Induced Barrier Lowering DIBL. Another reason that makes scaling reaching its limit is the subthreshold leakage. The off-state current (I_{OFF}) has been exponentially increased by multiple times in every generation. To obtain a high performance MOSFET a high mobility is required. To achieve higher subthreshold swing and lower threshold voltage a high-k materials needed instead of SiO_2 . This integration has to consider mobility

degradation or poor interference between the silicon substrate and any new material. Although supply voltage is decreased significantly, the number of transistor per chip increases is doubled every 18 to 24 months causing the overall power consumption to increase dramatically. As we reaching the end of MOSFET era, multiple proposals are considered and wide research to keep Moor's law alive. For that reason integrated circuit (IC) technologists are looking for a new material or a new technology with completely different concepts to start a new generation of development. FinFET and CNTFET are two promising substitution to the conventional MOSFET.

1.4 Recent and Emerging Device Technologies

1.4.1 Emerging Field of Ultra Low Power Devices

ICs power management has become a major concern in last decade due to the increase of number of transistor in single die (following Moor's Law). Furthermore, down scaling give privilege of faster devices under low supply. However, short channel effect increases significantly to increase off-state current. Additionally, the Supply Voltage scaling increases delay and decrease noise margin therefore. The supply voltage scaling slowed down considerably in the last decade. Table 1.1, shows the scaling trend at every technology node where Moor's Law is described in Figure 1.1. Table 1.2 pronounces the projected chip sizes and the number of transistors per chip of the next technology generations.

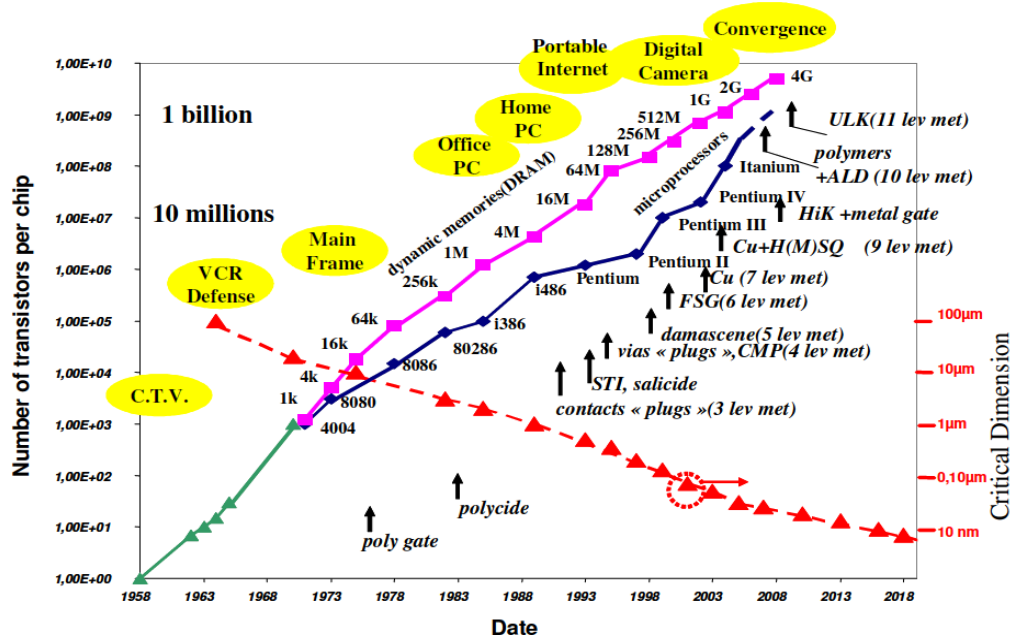


Figure 1.1: The progress of technology shows the increase of number of transistors at every process generation [11].

Table 1.1: Supply voltage scaling trend at every technology node reported by ITRS in [12].

| 2012 ITRS | 2011 | 2014 | 2017 | 2020 | 2023 | 2026 |
|-----------|--------|--------|--------|--------|--------|--------|
| feature | 35 nm | 25 nm | 18 nm | 13 nm | 9 nm | 6 nm |
| Vdd | 0.72 V | 0.65 V | 0.59 V | 0.53 V | 0.48 V | 0.43 V |
| power | 3.0 W | 3.0 W | 3.0 W | 3.0 W | 3.0 W | 3.0 W |

Two figure of merit that strongly considered at design level of every technology node. On-state current (I_{on}) and off-state current (I_{off}) both determine the power consumption and the performance of the device. I_{on} is proportional to $(V_{GS} - V_T)^\alpha$ (α :

alpha power law) and I_{off} is exponentially proportional to $q \times (V_{GS} - V_T)/nKT$. Low V_T is needed for better turned on device where High V_T is needed for low I_{off} . To keep standard functionality the factor $(V_{GS} - V_T)$ has to be scaled by the same level. Therefore, high $I_{\text{ON}}/I_{\text{OFF}}$ ratio is required while lowering the supply voltage. Note that there is a trade off between the power scaling and performance.

Table 1.2: Number of MOS per chip and chip size projection of upcoming technology node [12]

| 2012 ITRS | 2011 | 2014 | 2017 | 2020 | 2023 | 2026 |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| feature | 35 nm | 25 nm | 18 nm | 13 nm | 9 nm | 6 nm |
| chip size | 5.2 cm ² | 4.1 cm ² | 4.1 cm ² | 4.1 cm ² | 4.1 cm ² | 4.1 cm ² |
| total MOS | 8.8 G | 17.7 G | 35.4 G | 70.8 G | 141.5 G | 283.1 G |
| MOS/cm ² | 1.7 G | 4.3 G | 8.6 G | 17.2 G | 35.3 G | 69 G |
| Nb pads | 4800 | 5400 | 6000 | 6200 | 6840 | 6840 |

Field effect transistors in general have made marvelous progress in the last few decades by down scaling device dimensions and power supply level leading to extremely high numbers of devices in a single ship. High-density integrated circuits are now facing major challenges related to power management and heat dissipation due to excessive leakage, mainly due to subthreshold conduction. Subthreshold swing ' S ' represents the behavior of the device at voltage lower than threshold voltage. It is a figure of merit for the ultra-low-power designs. Figure 1.2 illustrates the increase of the subthreshold swing as the scaling move toward sub nano-technology. It is seen that S improves from 250nm to 130nm technology nodes due to the aggressive scaling of oxide thickness. But,

excessive increase in gate leakage current slows down the gate oxide scaling, and S deteriorates beyond 130nm that adversely affects the subthreshold operation by lowering I_{on}/I_{off} ratio.

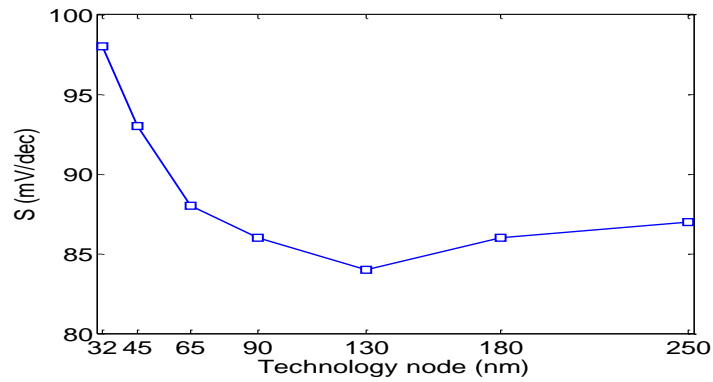


Figure 1.2: Subthreshold swing at different technology nodes [1].

Most scientists believe that the fundamental thermodynamic limits on the minimum operational voltage and switching energy of conventional transistors is given by this limit of $S = 60\text{mV/decade}$, which is known as the ‘Boltzmann tyranny’. Even with the excellent electrostatic and enhanced transport properties in all of the CMOS-based transistors (bulk, FinFET, and fully depleted silicon-on-insulator: FDSOI), S will be over 60mV/decade at room temperature. Some novel transistor structures like nanowire FETs (NWFET), the carbon nanotube based tunnel FETs (T-CNFET), the impact ionization MOS-based transistors (IMOS), and Tunnel-FET (TFET) have been shown to exhibit lower value of S . Figure 1.3 shows ‘ S ’ of various technology including the new scheme that contained in this report.

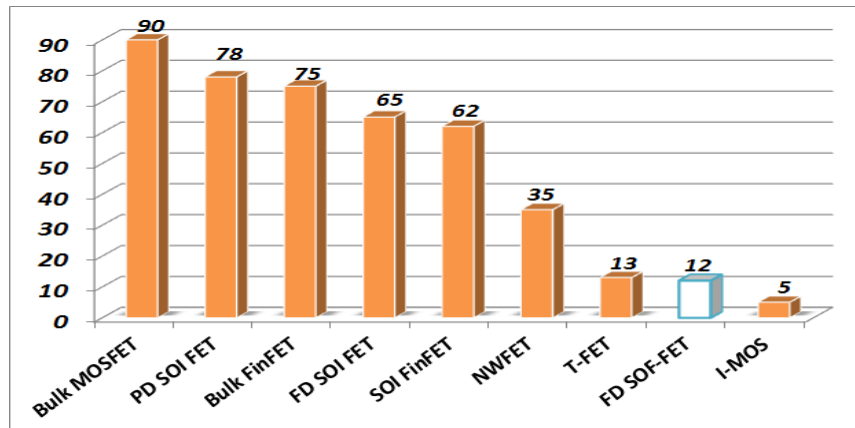


Figure 1.3 Subthreshold swings (S) reported for various CMOS and emerging Technologies

Recently DARPA initiated a program (STEEP: Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power) with a target of $S \leq 20\text{mV/decade}$ (see Figure 1.4 [5]). Researchers are actively looking into novel technologies based on tunneling mechanism of electrons. Carbon Nanotube Tunnel FET, Si/SiGe Vertical Tunnel FET, and Si Lateral Tunnel FET are leading potential candidates to replace conventional MOSFETs in the next generation ultra-low-power electronics that require very low value of S . People are also looking into new materials like ferromagnetic insulator.

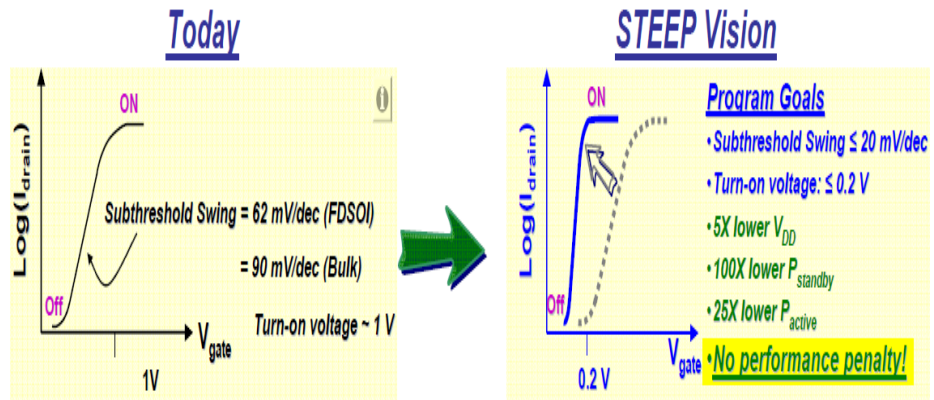


Figure 1.4: Subthreshold swing in some conventional devices and the DARPA goal of $\leq 20\text{mV/decade}$ [5].

A brief discussion of the current researches and different schemes are offered in the next section where more details are presented in the upcoming chapters.

1.4.2 Silicon-On-Insulator (SOI) Devices

The idea behind SOI MOSFET is to separate or isolate the active regions of the device from the reliant on influence of the underlying silicon substrate. SOI — silicon-on-insulator, refers to placing a thin layer of silicon on top of an insulator such as SiO_2 . The devices will be built on top of the thin layer of silicon. One of the major source of parasitic capacitance is from the source and drain to substrate junctions. SOI can reduced the capacitance at the source and drain junctions significantly by excluding the depletion regions extending into the substrate. SOI substrate leads to a dielectric isolation of the devices to lower the influence of the parasitic effects experienced in bulk devices. SOI has many promising features over the bulk technology. The demand for a high-speed high-performing, low power devices leads to aggressively reducing the fabrication

process to go beyond ultra-deep sub-micron (UDSM) technologies such 32-nm, and 22-nm.

Shrinking the planar MOSFET device has led to a higher off-state current (I_{OFF}). As a result the subthreshold swing increases significantly. Silicon-on-insulator (SOI) was presented to limit the influence of the underlying silicon substrate and leads to a progress over short channel effects. Merging his idea with scaling the gate length of MOSFETs has enhanced the speed of the device in addition to improving the short channel effect. Majumdar et al. show that a fully depleted SOI (FDSOI) transistors is the expected idea to bring down the technology under 22-nm. They have also indicate that using back-gated extremely thin silicon-on-insulator (ETSOI) device with thin buried oxide (BOX) will also lower the threshold voltage and allows lower voltage operation [3].

1.4.3 Carbon Nanotube Field Effect Transistor (CNTFET)

The demand for fast computing devices, more applications, smaller dimensions and low power consumption requires new architecture and/or material exploration to be the base of the future ICs. CNTs come to light to offer a multitudinous solutions to the scaling of silicon based devices. Carbon nanotubes (CNTs) can be considered as single layer thick sheet of rolled graphite (SWNT). CNTs have taken much attention due to their abilities to carry high current. SWNTs are attractive material due to their unique electrical properties. SWNTs are drawn a significant attention to be integrated into future logic switches, and interconnects.

CNTFET is a three terminals logic switch. The device consists of semiconducting nanotube (channel) sited between the source and the drain contacts, the third terminal is the gate that controls the electrostatic of the device. An extensive work is made recently to understand the device physics, and properties. High carrier mobility, superconducting material, high stability, high scalability, ballistic or near-ballistic transport, the ability to be integrate with high-k materials, low power, low leakage, and the electrical properties that can either be metallic or semiconducting; A list of the major properties that made the carbon nanotube based field effect transistor the future building block of the future nano-electronic circuits. All these decencies have made the CNTFET the first candidate to replace the conventional MOSFET for the future nano-electronic technology.

CNTFET using carbon nanotube as semiconducting channel and silicon substrate wafer was fabricated in 1998. This transistor had reported a poor functionality. Since that time the carbon nanotube based FET got extensive attention due to its outstanding properties. CNTFET shows an excellent compatibility with CMOS manufacturing process due to its similarities in structure and electrical operations. Other decency that n-type and p-type of CNTFET can be the same size as opposite to CMOS technology where p-type has to be 2 to 3 times larger than n-type. Despite their functioning similarity, the CNTFET electrical switching principles and the physics dependent have not fully explored. There a set of numerical approximations as the base of the CNTFET operations, those numerical models that depends on certain condition and structure have not become an evaluation standard.

1.4.4 Multi-gate Transistors

As needed to keep Silicon technology as the base technology while modernizing future devices; cost is an important factor. Tri-gate also known as FinFET was introduced due to its similarities to conventional MOSFET. The fin shape introduces a gate voltage that surrounds the channel from three sites; hence charges below the transistor are removed. This structure present a better control over short channel effect. The new structure also shows a higher I_{on}/I_{off} ratio as compared to conventional MOSFE. FinFETs present a better performance, lower leakage current, and fabrication compatibility with CMOS process [8]. Down-scaling of the MOSFET was the only road to achieve high performance and low power consumption. The shrinking of the gate length has been very aggressive. According to the International technology Roadmap for Semiconductors (ITRS) projection of 2020-2025 the gate length of the MOSFET can be scaled down to 5-7 nm range. The planar MOSFET physics may not be able to maintain the basic principle of operation [6]. By that time other technologies could be ready for a smooth transition away from the conventional MOSFE. New devices like tunnel transistors or the current 3D device are very promising to take over. The FinFETs have substantial progress since it came out in 2012. FinFET second generation is already on the way. Intel marketed 22 nm FinFET in 2012, this announcement followed by promises of 14 nm FinFET by Global Foundries and Taiwan Semiconductor Manufacturing Co. Ltd (TSMC) [7].

1.4.5 Tunneling Field Effect Transistors (TFETs)

The tunneling field effect has widely explored and multiple proposals are presented. The tunneling phoneme was introduced to overcome the thermal voltage limitation of the conventional MOSFET. Multiple proposals based on Band-To-Band tunneling (BTBT) that include several material and structures were suggested. Band-To-Band tunneling devices recommended by numerous scholars' shows that the subthreshold swing can be lower and 60mV/decade (at room temperature) since its independent of the thermal voltage (KT/q) [4]. There are many demonstrations showing a lower subthreshold swing using the BTBT phenomena. Zener or Esaki diode concept was utilized to build T-FETs either based on silicon tunneling or CNTs tunneling. The tunneling robustness is depends on the width of the depletion region of the P-N junction, and thus the doping profile in both junction and the channel. For high doping the depletion with is small which allows a better tunneling.

Merging SWCNTs and band-to-band tunneling phenomena (BTBT) have been a hot subject that encountered intense research in recent years. BTBT is the ability of electrons tunnel from the valence band through the semiconductor band-gap to the conduction band or verse versa [2]. This phenomenon of BTBT will enable the subthreshold slop to go below the thermal voltage limitation (60 mV/ decade).

A widely known arrangement of BTBT devices is based on p-i-n joint. This pattern introduced in [3] where carbon nanotube (CNT) was employed as the channel. CNT placed between the n-doped drain and the p-doped source to give p-i-n. This geometry

shows a subthreshold slope around 40mV/ decade. In [4] two geometries were compared; p-i-n and n-i-n CNT based. Both geometries have the advantage of driving a high current, functionality in high frequency, and low off-current. This paper also indicates the possibility of subthreshold slope lower than the thermionic-emission limit of 60mV/ decade. In [5] a dual-gate nanowire field effect transistor (NW-FET) built upon BTBT was proposed. This device principle of operation is based on gated Esaki diode. The need of what's called in some literature "Green" devices. Those types of devices are not governed by $kT/q \sim 60\text{mV/ decade}$ limit requires the exploration of ground-breaking materials. Tunneling in state-of-the-art group III and V was proposed to overcome some of the concerns presented by the previews design. Tunneling FET based on tunnel III-V staggered hetrojunctions were considered due to their small bandgap and their compatibility with current CMOS process. Those type of devices also employed gated p-i-n junction. The devices of this manner achieve a low subthreshold swing; however III-V tunneling transistors physics not fully clear to demonstrate a high on-state current.

1.4.6 Negative Capacitance Gate Stock Transistors

It is clear that lowering the threshold voltage and supply voltage of the single transistor will lower the overall power dissipation. This goal was accomplished by down-scaling the lengths of the device. The physics limitations have put an end to this road (mainly due to increase of short channel effect). Various materials and architecture were investigated to break the 60mV/ decade thermionic limit and realize high performance and low power dissipation. New alternative are coming out to overcome the physic

limitation of the planar MOSFET. Ferroelectric materials is widely explored and considered ground-breaking into nanotechnology ultra-low-low-power designs. Previous research shows that replacing the ordinary gate insulator stack with a negative capacitance gate stack will provide a power boosting to the device allowing it to operate under low voltage. The negative capacitance gate stack is explained in [10] and the concept was proved in [9]. This proposal provides a steep subthreshold slope, and the ability to operate in low voltage (reduced threshold voltage). More details on this subject are presented in chapter 6.

1.5 Contribution

In this study a concept of a new field effect transistor (FET) based on ferroelectric insulator is presents. The proposed design is named *Silicon-on-Ferroelectric Insulator field effect transistor (SOF-FET)*. The design combines the concepts of negative capacitance in ferroelectric material and silicon-on-insulator (SOI) device. The design proposes that by burying a layer of ferroelectric insulator inside bulk silicon substrate an effective negative capacitance (NC) can be achieved. The NC effect can provide internal signal boosting that leads to lower subthreshold swing, which is the prime requirement for ultra-low-power circuit operation. In addition to introducing the concept of a new device *SOF-FET*, this paper presents closed form models to calculate the subthreshold swing of the proposed device. These models are used to analyze the dependence of subthreshold swing on the material and geometric parameters of the device. Current-voltage (I-V) characteristics of the proposed device have also been derived. It is

demonstrated that by carefully optimizing the thickness of the ferroelectric film, dielectric property of the insulator, and the doping profile of the device channel, the subthreshold swing and the threshold voltage can be lowered.

CHAPTER 2

CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Wide varieties of materials are investigated currently to be considered for the future ICs designs. One of these materials is carbon nanotube (CNTs). This chapter includes review of the fabrication and application of carbon nanotubes, as well as the advantage and utilization in field effect transistors designs.

2.1 Introduction

Down-scaling path of the traditional MOSFET reaches its technological, economic and, most importantly, fundamental physical limits. Before the dead-end road, a broad research to find substitution materials as well as new architectures to the current technology. CNTFETs have explored extensively as a major candidate to replace the traditional MOSFET. High chemical stability, robustness, and ballistic transportation are the major properties that give CNTFET an excellent advantage over any other proposals [13]. Furthermore, the compatibility to be incorporated with high- κ gate dielectrics and a high ON state current compare it to the conventional MOSFET makes the carbon nanotubes based FET a promising future. Carbon nanotubes are made of carbon atoms sheets that take cylindrical form. Two type were introduced; single-walled carbon nanotubes (SWNTs) and multi-walled carbon nanotubes (MWNTs). SWNTs are made of one single carbon sheets rolled cylindrically, and MWNTs are made of multiple layers of carbon sheets. Another interesting decency of carbon nanotube is that can be metallic or

semiconductor with a band gap depending on its diameter [14]. The band gap of the semiconductor tubes scales inversely with the tube diameter [15].

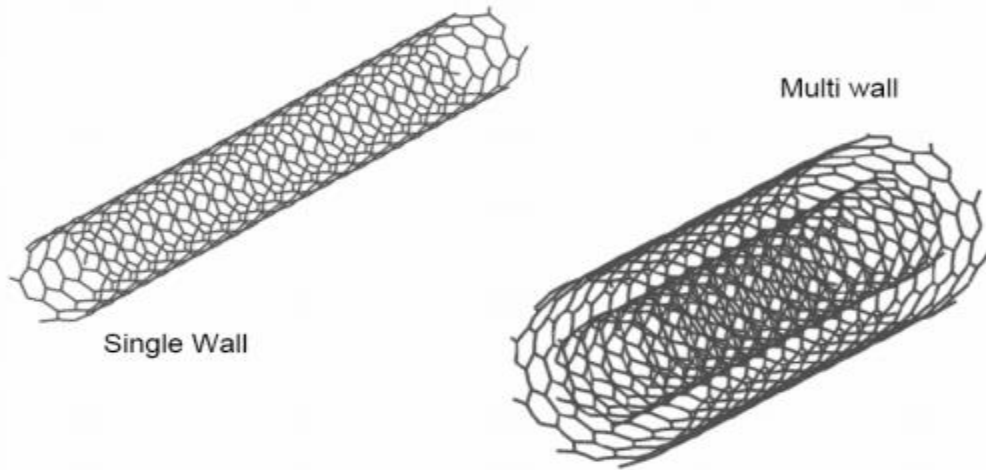


Figure 2.1: Single and multiwall carbon nanotubes [16].

The structure of a SWNT (one-dimensional (1-D)) is defined by the Hamada vector $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ (this vector represent the way the graphene sheet is wrapped) most of the time is indicated by a pair of indices (n, m). n and m are integers that denote the number of unit vectors along two directions in the honeycomb crystal lattice of graphene. The properties of CNTs changes significantly with the (n, m) values. Depending on their (n, m) values, nanotubes can be metallic or semiconductor. This extraordinary electrical property has encouraged their use as semiconducting channels in field effect transistors as well as metallic wires [16, 17].

The diameter of the nanotube is function of the n and m indexes $d = \frac{a}{\pi}(n^2 + m^2 + nm)^{\frac{1}{2}}$, where: a = 0.246 nm. Another interesting phenomenon is that CNTs allows

electrical transportation with small diameter, in addition that tube-FETs under ambient conditions are always p-type with holes is the majority carriers [18]. Figures 2.2 and 2.3 provide a close view to the structure

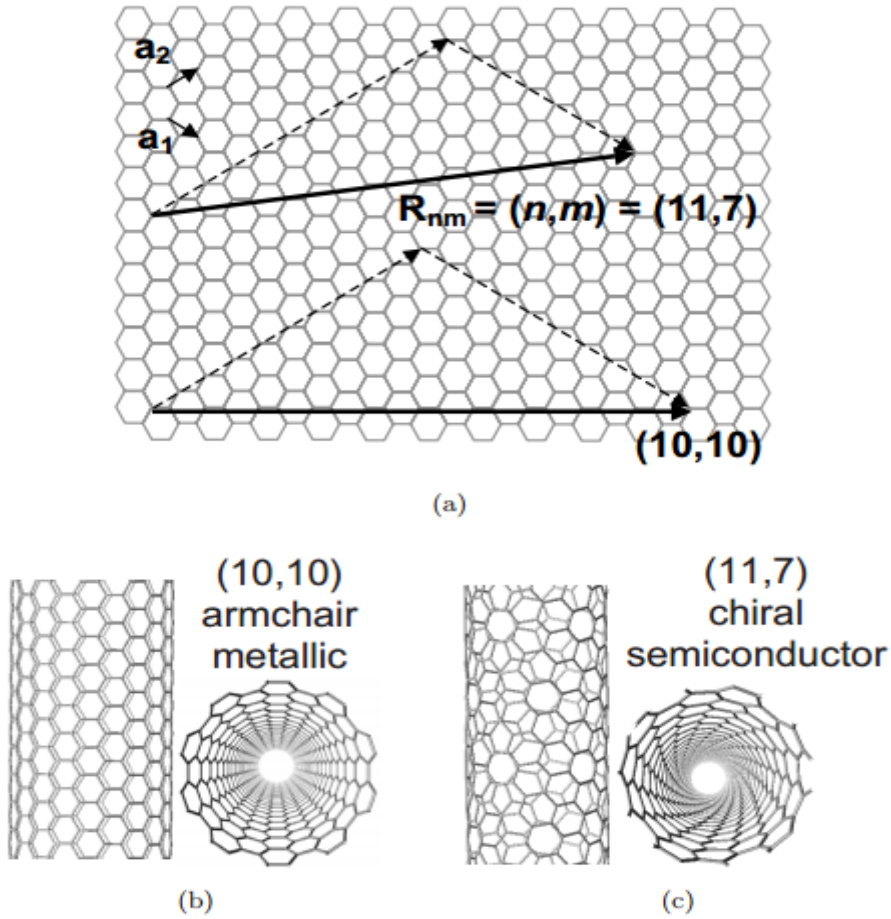


Figure 2.2: Folding of graphene into nanotubes. (a) Various chiralities of carbon nanotubes can be obtained by folding along different the Hamada vector. (b) and (c) are schematics of (10, 10) and (11, 7) nanotubes. A (n, m) tube is metallic when $n = m$ (armchair). A nanotube with $n-m = 3j$, where j is an integer, is a semi-metal with a curvature-induced band gap on the order of few meV. A nanotube is semiconducting when $n- m \neq 3j$ [17].

The electrical properties of CNTs changes with the geometrical changes (depends on how they rolled up). For semiconductors, the Fermi level is between the band gap of

conduction band and the valences band. For metallic conductors, the band gap is zero and the Fermi level is in the overlapped area of conduction band and the valences band. Then, a portion of valence electrons can travel across the material [13].

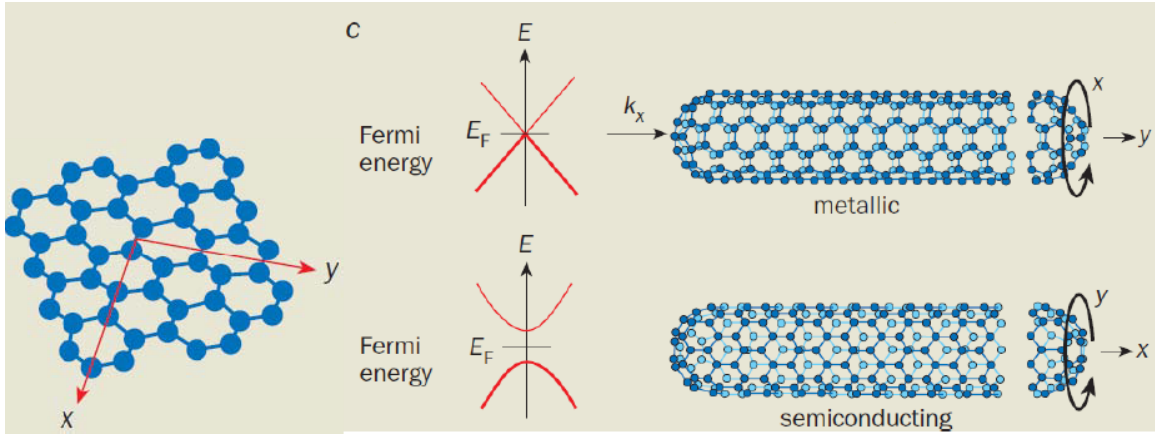


Figure 2.3: Carbon nanotube metal and semiconductor bandgap [25].

2.2 Ballistic Transport and Mean Free Path

The electrons in carbon nanotubes experience a negligible or no scattering (no resistivity in the medium) due to atoms or impurities, scattering this phenomenon is called ballistic transport. When the electronic mean free path of a wire l is larger than the length of the wire L ($l > L$), the electron transport in the wire is ballistic (Figure 2.4). These considerations imply that a minimum resistance of $h/4e^4$ (about 6.5 K Ω) is present in a SWNT with a single channel of conduction [25, 26].

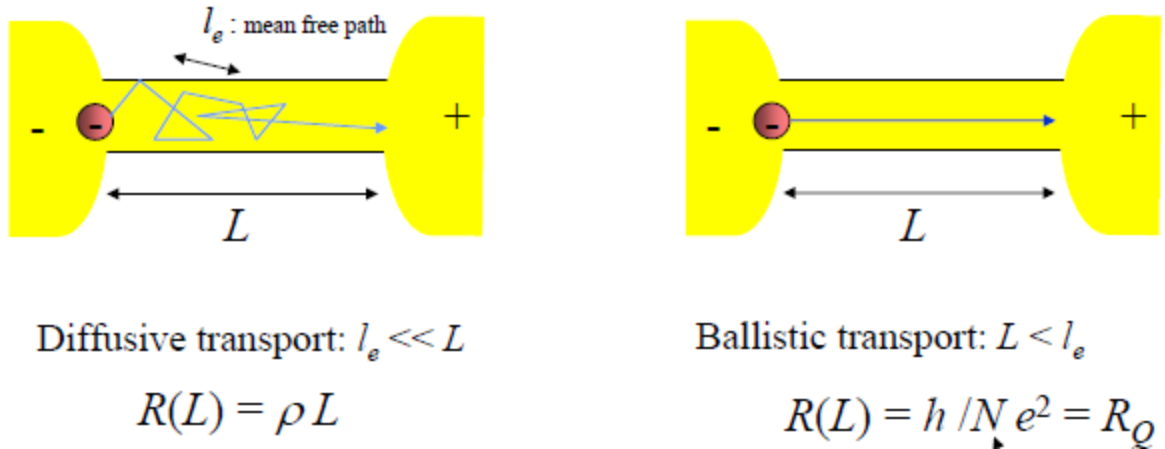


Figure 2.4: Electron Transport in 1D Channel [26].

Resistance of N-1D channel is given by: $R(L) = \frac{h}{Ne^2} + \frac{h}{Ne^2} \frac{L}{l_e}$, for a nanotube, N=4 (2 from spin and 2 from k and K')

2.3 Unique Properties of Carbon Nanotubes

Carbon nanotubes have numerous advantages that make it a hot research topic in semiconductor technology. Some of these qualities are listed below.

- ✓ High mobility at high electric field inductance can make a Superconducting FET.
- ✓ Small size: ~1 nm diameter (down to ~10 atoms around the circumference).
- ✓ High ON/OFF ratio with small diameter.
- ✓ Electronic Properties: can be either metallic or semiconducting depending on diameter and orientation of the hexagons.
- ✓ Mechanical: Very high strength, modulus, and resiliency.
- ✓ Physics: model system for 1D density of electronic states.

- ✓ Single molecule Raman spectroscopy, luminescence and transport properties.
- ✓ Integration ability with high- κ materials.
- ✓ Chemical bonding and surface stability

2.4 Carbon Nanotube Field Effect Transistors

Field effect transistors are switches that control the current flow using an electric field. For a positive gate voltage charges at the metal side of the metal-oxide capacitor attract negative charge at the semiconductor side. As the positive charge at the gate is increased (gate voltage increases), the negative charge in the semiconductor increases until the region beneath the oxide becomes an n-type semiconductor region, and channel formed between the source and the drain. Through this channel current can flow between drain and source.

The same philosophy is applied in the CNTFET where SWNT is used as the conducting channel between source and drain. Applying a gate voltage (changing the energy bands in the conducting channel) the SWNT conductance changes and current can flow between the drain and source accordingly. The basic structure of a CNTFET is shown in Figure 2.5.

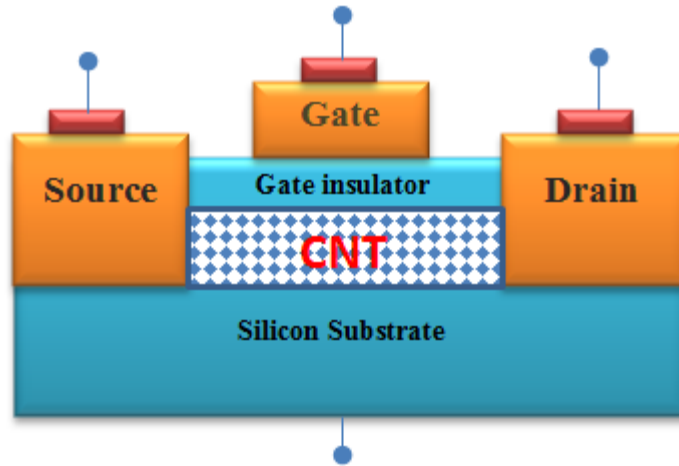


Figure 2.5: A schematic of a typical carbon nanotube FET

For a typical nanotube FET a cylindrical conducting tube placed between the drain and the source on the top of an insulator. Therefore a capacitor formed between the metal area of the gate (top plate) and the insulating layers and the semiconductor channel (bottom plate). The direct tunneling leakage can be reduced by using a high-k gate insulator. High-k insulator also support charges injection efficiency into transistors channels [29].

2.5 Carbon Nanotube Basics and Theoretical Considerations

The voltage difference between the gate and the substrate is denoted V_{gb} will cause a potential ψ_{ox1} , and ψ_{ox2} drops in both oxide areas, a potential drop in the substrate ψ_{subs} , in addition to a potential across the CNT ψ_{cnt} . This potential distribution across the device also depends on the work function Φ_{ms} defined as the total of work function difference between the gate and carbon nanotube material Φ_{mc} and the carbon nanotube and the substrate Φ_{cs} . Φ_{ms} is expressed as follow [20, 21, 24]:

$$\Phi_{ms} = \Phi_{mc} + \Phi_{cs}$$

The gate voltage V_G required to produce the surface potential ψ_S based on the electrostatic capacitance relations of the capacitance model is determined as [23]:

$$\psi_S = V_G - \frac{Q_{cnt}}{C_{ox1}}$$

Where: C_{ox1} is the nanotube to gate capacitance. The gate voltage that produces a potential drop in CNT is determined from [23]:

$$V_G = V_{fb} + \psi_S - Q_{cnt}/C_{ox1}$$

The oxide capacitance between the carbon nanotube and the surface of the substrate is given by [24, 20]:

$$C_{ox2} = \frac{2\pi\epsilon_{ox2}L}{\ln\left(\frac{T_{ox2} + r + \sqrt{T_{ox2}^2 + 2T_{ox2}r}}{r}\right)}$$

Where: r is tube radius, T_{ox1} and T_{ox2} are gate and substrate oxide thicknesses, ϵ_{ox2} oxide permittivity, and L is the length of the carbon nanotube.

2.6 Capacitance Modeling of CNT-FET

SWNTs shows very interesting phenomenon where CNTFETs under ambient conditions are always p-type with holes as the majority carriers the number of carrier in the channel n_{cnt} , determine the amount of charges in the nanotube Q_{cnt} . Experimentally, the nanotube shows that the charge carriers have an intrinsic mobility at room temperature that is higher than other semiconductors. Moreover, carrier scattering is suppressed in the

small diameter nanotubes, as a result, a ballistic transport and high carrier mobility can be accomplished [29].

The quantum capacitance for one dimension semiconductor CNTs is approximated as in [30].

$$C_Q = \frac{2vq^2}{\hbar v_F}$$

Where: v_F is the Fermi velocity, \hbar is Planck's constant, q is the magnitude of the electronic charge, and v is a constant.

$$\frac{1}{C} = \frac{1}{C_{ox1}} + \frac{1}{C_Q}$$

The total charges on the nanotube, Q_{cnt} , depends on carrier density n_{cnt} ,

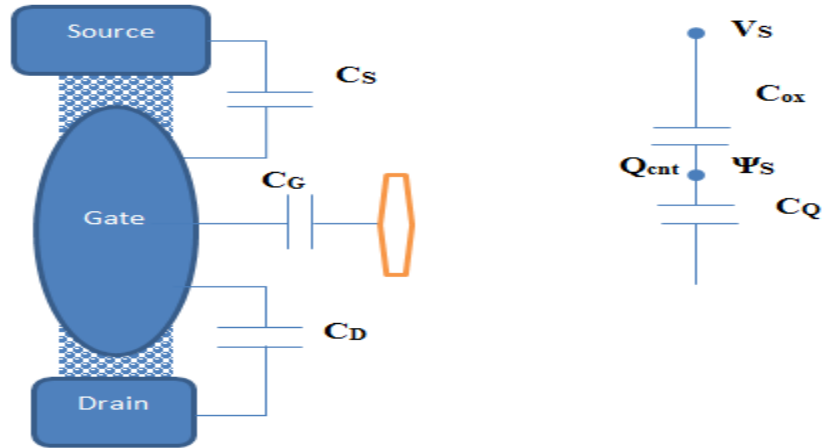


Figure 2.6: Circuit model for carbon nanotube field effect transistor. The surface potential ψ_S , is controlled by the gate voltage V_G , this potential also create capacitance coupling between the drain and source in addition to the gate capacitance [27].

CHAPTER 3

MULTI-GATE TRANSISTORS - FINFET

This chapter provides an understanding of the basics of FinFET device as well as the electrical mode of operation. Understandings of the various parameters that control the performance of the new device are listed. This chapter also includes a list of advantages and the strong interest over other technologies, in addition to its feature in analog IC design.

3.1 Introduction Into SOI and Multi-gate Devices

As the transistor shrinks the length also shrinks reducing the gate capability to control the channel. This dimensional reduction causes a current flow even at the absence of gate voltage (off-state current) as a result the power consumption at idle state increase drastically. This leakage current is increased at every transistor generation. In order to lower this effect while maintaining a high performance, various schemes were introduced. Some of these proposals come to fabrication phase like SOI-FET and FinFET others have not made it to that level. SOI and FinFET have increased the manufacturing complexity by adding layers or incorporating new materials.

One of the major issues of the short channel is the drain induced barrier lowering (DIBL). The barrier to carrier diffusion from the source into the channel is reduced. This uncontrollable concern at short channel causes the drain current to increase with increasing the drain bias. DIBL is the source of reduction of threshold voltage of the transistor at higher drain voltages as well as the increase of the subthreshold current

(off-state current I_{off}). The Figure 3.1 is short explanation of the matter of DIBL. At long channel the drain has not effect on the electron that located in the source. In this case only the gate that controls the flow of the electrons. The situation of short channel the source and the drain are placed close to each other and the drain voltage contribute in the electrostatic of the device [31]. At short channel not only the gate voltage that control the electrons flow but also the drain voltage does. The designers noticed that a single gate will not be sufficient to eliminate the effect of DIBL. To improve the gate control, a supplementary gate was incorporated in several proposals. Figure 3.1 demonstrate the concept of moving from single gate to double gate in short channel devices. The integration of this additional gate varied through the applications.

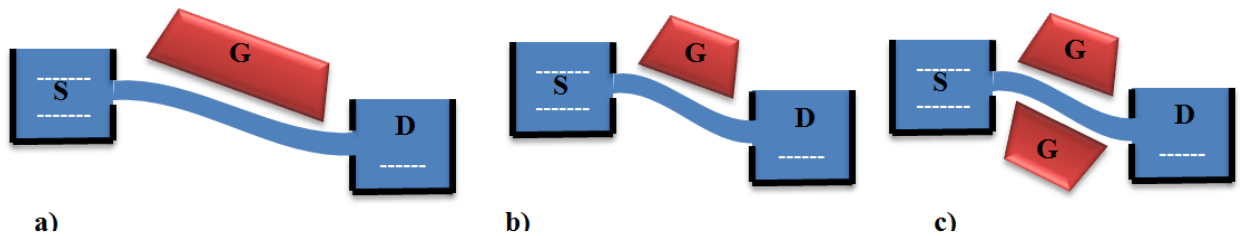


Figure 3.1: DIBL effect and the need of double gate devices [31]

3.2 Silicon-On-Insulator Transistors (SOI)

SOI arrangement is one of the approaches used in current technology to overcome some of SCE related issues. This technology has a similar geometry to the original MOSFET and has kept the silicon as the fundamental material. The idea behind SOI MOSFET is to separate or isolate the active regions of the device from the reliant on influence of the underlying silicon substrate. SOI — silicon-on-insulator, refers to

placing a thin layer of silicon on top of an insulator such as SiO_2 . The devices will be built on top of the thin layer of silicon. One of the major source of parasitic capacitance is from the source and drain to substrate junctions. SOI can reduced the capacitance at the source and drain junctions significantly by excluding the depletion regions extending into the substrate. SOI substrate leads to a dielectric isolation of the devices to lower the influence of the parasitic effects experienced in bulk devices. SOI has many promising features over the bulk technology. The demand for a high-speed high-performing, low power devices leads to aggressively reducing the fabrication process to go beyond ultra-deep sub-micron (UDSM) technologies such 32-nm, and 22-nm.

The device down-scaling of MOSFET has led to a higher off-state current. As a result the subthreshold swing increases significantly. Silicon-on-insulator (SOI) was presented to limit the influence of the underlying silicon substrate and leads to a progress over short channel effects. Merging this idea with scaling the gate length of MOSFETs has enhanced the speed of the device in addition to improving the short channel effect. Majumdar et al. show that a fully depleted SOI (FDSOI) transistors is the expected idea to bring down the technology under 22-nm. They have also indicate that using back-gated extremely thin silicon-on-insulator (ETSOI) device with thin buried oxide (BOX) will also lower the threshold voltage and allows lower voltage operation [3].

3.3 The Road to Multi-gate Devices

Short channel has reduced the time necessary for the electrons to travel from the source to drain hence faster device. The biasing of the substrate in the SOI devices creates a buried gate. The substrate acts as an additional gate and the device perform as vertical double gate transistor. The buried oxide prevents any leakage in the substrate leading to a better biasing. The device to device threshold variation in the conventional MOSFET can be limited by setting the operating area on insulator and lowering channel doping which's allowable in SOI technology.

The Figure 3.2 displays a series of thought that allowed for better electrostatic or better gate control. In planar device the electrostatic is controlled by one gate. This single gate lost its potential at sub-nano-scale level. SOI technique is a simple way to overcome some of the SCE concerns. A thin oxide film is incorporated in the simple way to improve the device electrostatic. The thoughts moved through the years to integrate an actual gate for an easy biasing. However the bottom gate added serious difficulties to the fabrication process. These difficulties were solved by moving to 3D architecture (FinFET or/and Tri-gate). Moving through those proposals (Figure 3.2), various architecture to gain a better control over the channel is publicized where now a wide research are investigating the Gate-All-Around (GAA) or nano-wire designs [31, 3].

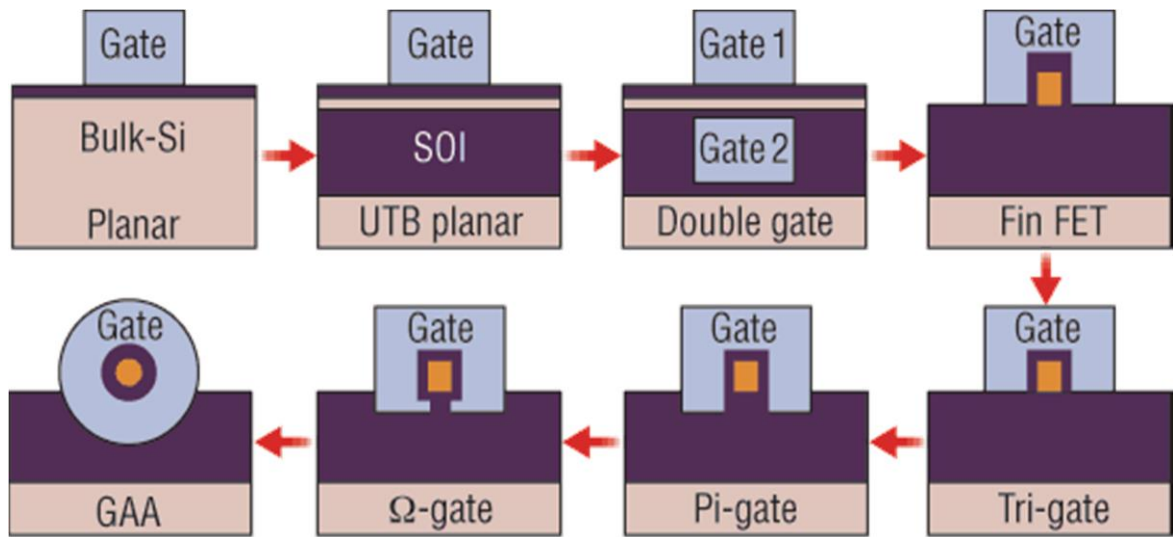


Figure 3.2: The road the Multi-gate Transistors [31, 3]

3.4 Introducing the FinFET

As the MOSFET channel length scaled down the gate control over the channel decreases. One way to bring back a full gate control is to add another gate to help the existing gate and/or sitting the device on an insulator where the body acts as a second gate. Both technologies have tested to show a better performance in the extended down-scaling trend of the conventional MOSFET. However, still plenty of improvement to get better performance. The 3D devices are suggested to extend Moor's Law, and to lower the power consumption. FinFET or Tri-gate comes to light as a first replacement to conventional MOSFET. The device shows the ability to support farther scaling. Figure 3.2 shows the scaling history and the road to 3D devices [40].

Over last 40 years, shorting the channel was the key to increase the performance and decrease the power consumption of the conventional MOSFET. Farther scaling causes increases of the short channel effect. This effect that includes a significant increase of the off-state current therefore increases power consumption. The FinFET come to existence to solve the down-scaling related issues. FinFET was introduced due to its similarities to conventional MOSFET (silicon based device). The fin shape introduces a gate voltage that surrounds the channel from three sites; hence charges below the transistor are removed. This structure present a better control over short channel effect. Therefore the effective switching capacitance is reduced, and the dynamic power dissipation is reduced as result [34].

The Tri-gate structure comes to light to improve the gate electrostatic over the channel. The new structure shows a higher performance that made it the first candidate to substitute the conventional MOSFET. The device also shows a future scalability to continue Moor's Law. Furthermore, the device is compatible with silicon fabrication process. The device has history back to 1990 when first introduced by Hisamoto et al. [35]. The FinFET manufactured in 2012, moreover, Intel's first 22nm bulk-FinFET based CMOS is available in market currently [37]. This announcement followed by promises of 14 nm FinFET by Global Foundries and Taiwan Semiconductor Manufacturing Co. Ltd (TSMC) [48]. The new structure comes on two modules SOI and bulk FinFET. The most common module is SOI FinFET due to its manufacturing simplicity and better performance. Silicon-on-insulator (SOI) was introduced to extend the bulk MOSFET

scaling low-power applications. FinFET have merged with SOI to take advantage of both emerging technologies. Most of FinFET are fabricated on SOI substrate, silicon bulk FinFETs also was considered due its better heat dissipation and low wafer cost in addition to simplicity of integration with today's planar CMOS design methodology and automation techniques. Meanwhile, the SOI-FinFETs have a high wafer cost and low heat dissipation.

To maintain the benefits of technology scaling at the 22nm node and beyond, FinFET and (Ultra-Thin-Body) UTB-SOI show better performance. Both FinFET and UTB-SOI permit lower threshold voltage (V_{TH}) and lower supply voltage (V_{DD}). Therefore low power consumption. Body thickness is another parameter that control SCE. To lower random dopant fluctuation and for better mobility undoped body is used. Moreover, SOI-FinFET provides a speed improvement due to the elimination of the junction capacitance between source/drain and body. Figure 3.3 displays the future scaling and the progress toward SOI-FinFET structures at sub-nano-scale.

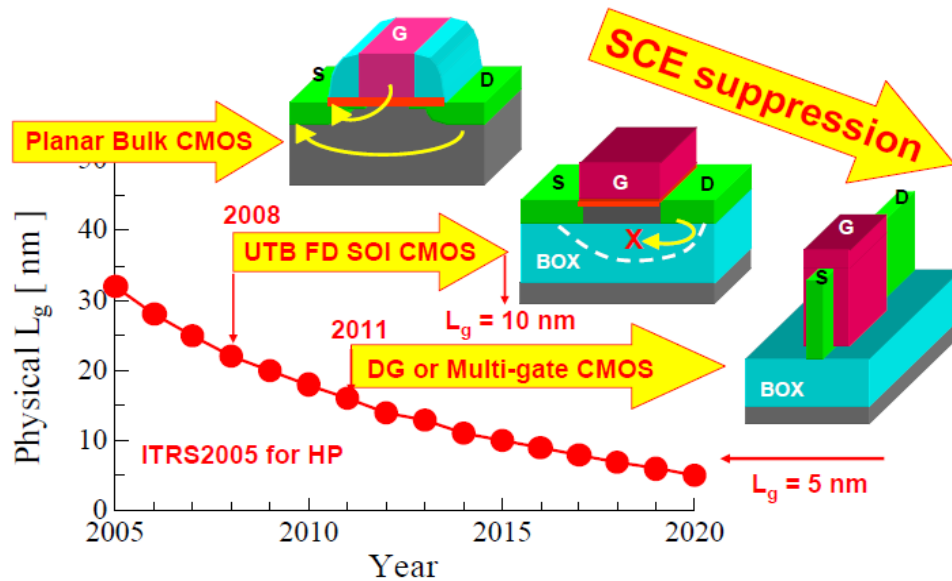


Figure 3.3: Background and motivation behind switching to 3D device [39].

3.5 FinFET Structure Analysis

The FinFET process is similar to that of MOSFET. The two structures of the FinFET (SOI and planar) are displayed in Figure 3.4. A cut-way view of the FinFET internal structure is shown in Figure 3.5.b and 3.5.c. In this device only source and drain implants, then gate fabricated. The undoped channel eliminates Coulomb scattering due to impurities, resulting in higher mobility in FinFETs and removes excessive random dopant fluctuations RDF. Undoped channel FinFET is overlooked currently to control the issue of significant device-to-device threshold voltage variations. This type of device channel is managed by the gate work function that requires a different material to serve as gate metal [40-42]. A higher I_{on}/I_{off} can be achieved with lightly doped channel as it reported in [49].

The FinFET operation is comparable to that of conventional MOSFET. The only exception here is that the on-state and off-state is controlled by the surrounding gate. The FinFET geometry has helped to increase the gate capacitance for the same oxide thickness compared to planar devices.

Many ICs based on FinFETs technology have already been fabricated, ranging from digital logic, SRAM, DRAM to flash memory. FinFETs offer numerous advantages to be used in multiple ultra-large-scale integration (ULSI) circuit. This technology have reduced the SCEs, and leakage current, in addition to reduced channel leading to a power consumption reduction. FinFET are mostly fabricated on silicon-on-insulator (SOI) [32]. SOI-FinFET works with lower supply voltage, threshold voltage less sensitive to gate length, derives a high on-state current, lower off-state current comparable to bulk counterpart, and lower subthreshold swing [38].

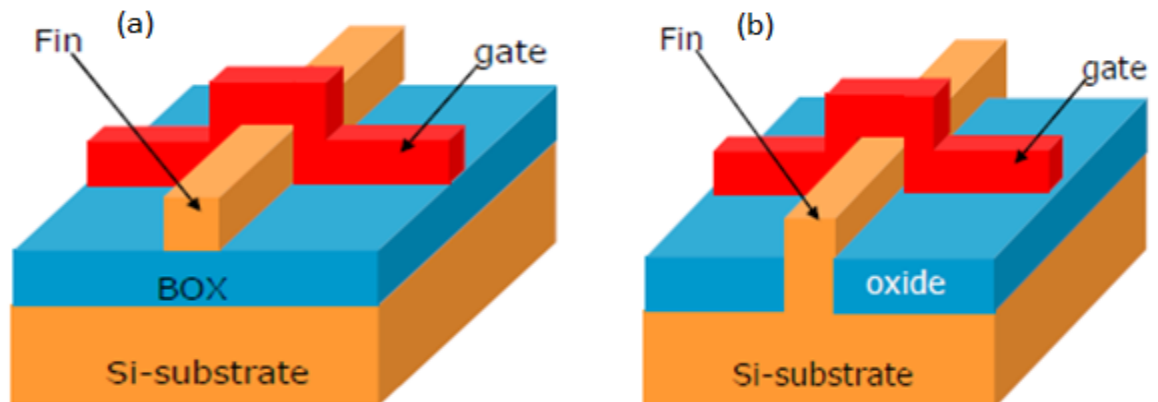


Figure 3.4: FinFET structures; (a) SOI FinFET, (b) Bulk FinFET [44]

The SOI-FinFET ability to operate in lower supply voltage and low threshold voltage make it suitable for Low standby Power (LSTP) Applications [45].The device

also shows suppressed leakage current and superior short channel effects [47]. In this work we are focusing on SOI-FinFET since it is the best fit for ultra-low-power designs. A close view of the device is presented in Figure 3.4. The Fin width has a major impact on the performance of the device. A small W_{Si} is required for a better gate control over the channel. Hence, Small W_{Si} allows for a small subthreshold swing and less DIBL [48]. A various fin aspect ratio ($AR = \text{the fin height} / \text{the effective fin width}$) is studied in [50]. This geometrical ratio has a significant effect on the channel controllability, therefore the short channel effect (SCE) and the parameters related to it.

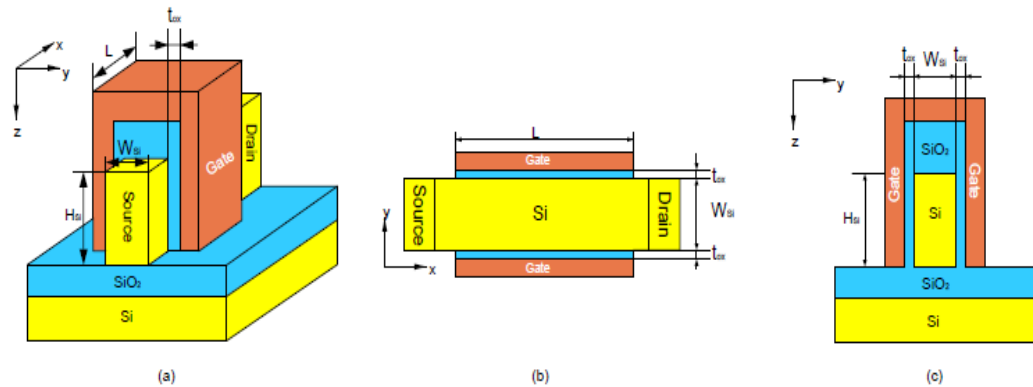


Figure 3.5: FinFET illustrations; (a) 3D schematic view of SOI FinFET, (b) Horizontal cross-section along transistor gate, (c) Vertical cross-section along transistor gate. H_{Si} and W_{Si} represent fin height and width, respectively, L is the gate length, t_{ox} is the gate oxide insulator [43].

The width of a FinFET is quantized due to the vertical gate structure. The minimum transistor width is related to the fin height by [8]:

$$W_{min} = 2H_{fin} + T_{fin} \quad (3.1)$$

Where H_{fin} is the height of the fin and T_{fin} is the thickness of the silicon body. To obtain higher drive currents additional fins must be applied in parallel. The total physical width of the transistor is [8]:

$$W_{total} = nW_{min} = n \times (2H_{fin} + T_{fin}) \quad (3.2)$$

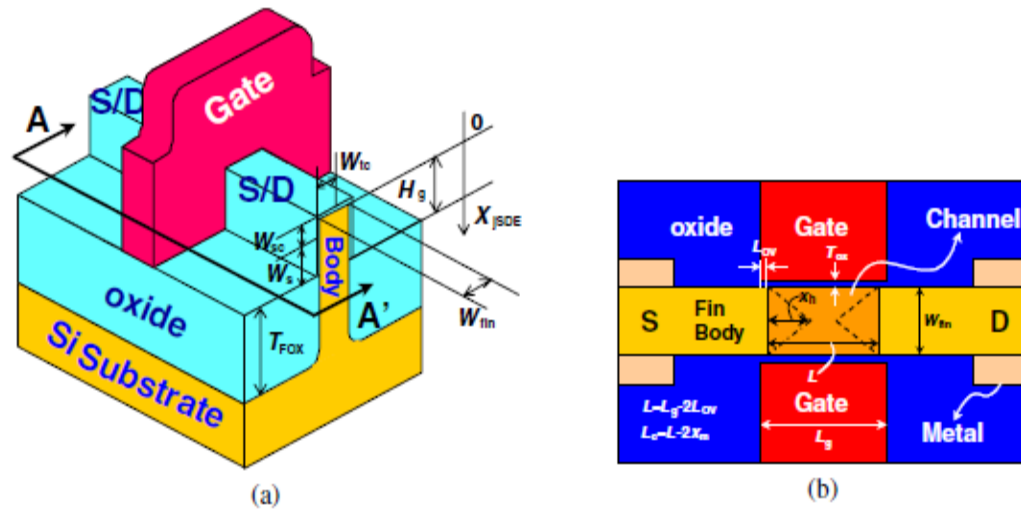


Figure 3.6: (a) 3-D schematic view of bulk FinFET. H_g and W_{fin} represent fin height and width, respectively. (b) 2-D cross-sectional view of the bulk FinFET cut along A–A' in (a). The T_{ox} and x_h represent gate oxide thickness and charge-sharing length, respectively [57].

3.6 FinFET Advantages

Double or multiple gates designs offer variety of advantages that include scaling to very short gate length. Silicon-on-insulator (SOI) was introduced to extend the bulk MOSFET scaling low-power applications. FinFET have merged with SOI to take advantage of both emerging technologies. Most of FinFET are fabricated on SOI

substrate, silicon bulk FinFETs also was considered due its better heat dissipation and low wafer cost in addition to simplicity of integration with today's planar CMOS design methodology and automation techniques. Meanwhile, the SOI FinFETs have a high wafer cost and low heat dissipation.

To maintain the benefits of technology scaling at the 22nm node and beyond, FinFET and (Ultra-Thin-Body) UTB-SOI show better performance. Both FinFET and UTB-SOI allow lower V_T and V_{DD} . Therefore low power consumption. Body thickness is another parameter that control SCE. To lower random dopant fluctuation and for better mobility undoped body is used. A list of some of the advantages of FinFET and UTB-SOI [57]:

- Better Swing
- S and V_T less sensitive to gate length and V_{DD}
- No random dopant fluctuation
- No impurity scattering
- Less Surface scattering
- High on-current and lower leakage
- Much Lower off-state current compared to bulk counterpart.
- Lower V_{DD} and power consumption
- Further scaling and low cost

UTB is used to eliminate the leakage path. Since the silicon film is very thin the gate can suppress the leakage efficiently. On the other side SOI FinFET provides a speed improvement due to the elimination of the junction capacitance between source/drain and body.

Many ICs based on FinFETs technology have already been fabricated, ranging from digital logic, SRAM, DRAM to flash memory. FinFET also used in analogue circuit due to their advantages like high-gain and excellent current saturation. A list of advantages and drawback of FinFET is presented below:

Advantages of FinFET for Analog

- ✓ Improved frequency performance
- ✓ Reduced capacitance
- ✓ Higher drive current
- ✓ Reduction in interconnect length / reduced interconnect capacitance
- ✓ Noise and latchup are minimized through reduced substrate coupling
- ✓ Silicon resistors have improved linearity with respect to absolute voltage
- ✓ No reverse biased diodes to substrate
- ✓ Inductor Q enhanced through use of very high resistivity substrates

Drawbacks to FinFET for Analog

- ☒ Poor thermal response due to buried oxide and trench isolation.
- ☒ Quantized widths

3.7 Undoped Channel FinFET

Undoped channel FinFET is overlooked currently to control the issue of significant device-to-device threshold voltage variations. This type of device channel is managed by the gate work function that requires a different material to serve as gate metal. In this device only source and drain implants, then gate fabricated. The undoped channel eliminates Coulomb scattering due to impurities, resulting in higher mobility in FinFETs and removes excessive random dopant fluctuations RDF [40-52].

The FinFET functionality is similar to that of conventional MOSFET. The only exception here is that the on-state and off-state is controlled by the surrounding gate. The FinFET geometry has helped to increase the gate capacitance for the same oxide thickness compared to planar devices. The threshold voltage corresponding to fin gate geometry is shown below [52].

$$V_T = V_{FB} + 2\Phi_B + \frac{Q_{DEP}}{2C_{ox}} \quad (3.3)$$

Where V_{FB} is the flat band voltage, Φ_B is the silicon bulk potential, Q_{DEP} is the depletion charge per unit area in the depleted fin, and C_{OX} is the oxide capacitance per unit area of one gate.

$$V_T = \Phi_{MS} + 2\Phi_B + \frac{qN_{sub}t_b}{2C_{ox}} \quad (3.4)$$

By lowering N_{sub} the threshold voltage can be lowered.

FinFETs offer numerous advantages to be used in multiple ULSI circuit. This technology have reduced the SCEs, and leakage current, in addition to reduced channel effect leading to a power consumption reduction.

CHAPTER 4

SUBTHRESHOLD SWING

Subthreshold swing is an important figure of merit that describes how fast a device can turn ON and switch OFF. In the planar MOSFET, the subthreshold swing is limited by the thermal voltage $\left(\frac{kT}{q}\right) \ln 10$ ($= 60 \text{ mV/decade}$). Subthreshold swing ' S ' represents the behavior of the device at voltage lower than threshold voltage.

4.1 Introduction

One of the issues of down scaling is off-state current (I_{OFF}). Off-state current is increasing on every generation of MOSFETs and can no longer be neglected. I_{OFF} determine the power consumption of chip in its idle state. In another hand the on-state current determine the minimum voltage needed to turn ON a MOSFET. This current as opposed to I_{OFF} is increasing on every generation MOSFETs. One factor that provides a clear understanding of the ratio $I_{\text{ON}}/I_{\text{OFF}}$ is called subthreshold swing. This factor provides design concepts of driving devices with minimum power consumption. As the number of transistors on a chip keeps increasing the power consumption and leakage become the major concern on any ULSI design. Subthreshold circuit design is an ultimate solution to stay within the power budget. The design of ultra-low-power digital circuit in subthreshold regime required a deep study of subthreshold swing and the parameters that control this factor.

To evaluate the power consumption, an extensive work has concentrated on threshold voltage V_T where it's defined to be the amount of voltage required to turn ON the MOSFET. The region where V_T is less than V_{GS} , is called sub-threshold region. One parameter that characterizes the MOSFET is the slope factor "S". S-factor is defined as the change in the gate voltage V_{GS} required to reduce subthreshold current I_{DS} by one decade [54].

4.2 Subthreshold Region

The basic study discussed the MOSFET behavior in linear region and saturation region. The subthreshold region is referring to region where V_{TH} is less than V_{GS} , this region reflects how the MOSFET can switch ON. Figure 4.1 shows the VTC of a MOSFET device in subthreshold region with the drain current in log scale ($\log I_D$) and (V_{GS}) in linear scale. Since 'S-factor' is defined as the inverse of the slope of this VTC, it indicates that the change in V_{GS} needed to change the current I_D by one decade [59]. Normally it is expressed in mV/decade unit. In other word S-factor is the amount of change in V_{GS} required to produce a $10\times$ change in I_D . Experimentally I_D shown to be proportional to $\exp\frac{q(\psi_s)}{nkT}$, with ψ_s is the semiconductor surface potential, k is being the Boltzmann constant, T the absolute temperature, and q the electron charge [54, 55].

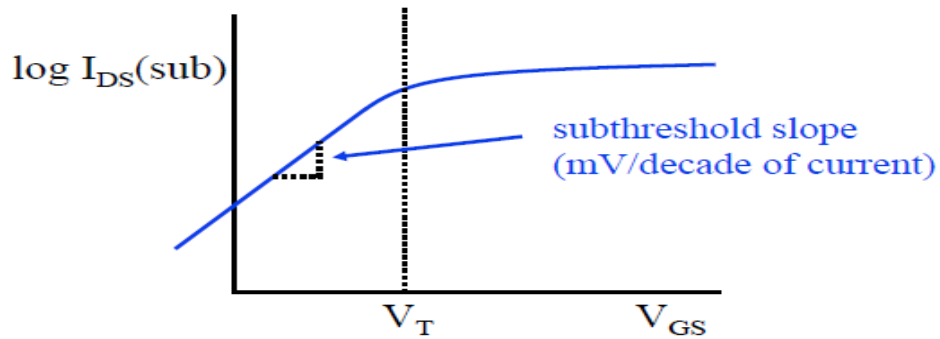


Figure 4.1: Plot describes the exponential relationship between I_{DS} to V_{GS} .

The Figure 4.2 presents the behavior of swing as function of I_{off} and I_{on} . The Figure also shows a useful parameter considered in ICs design which's the ratio I_{on}/I_{off} . I_{on} is a measure of the transistor drive current at fixed $V_{gs}=V_{ds}=V_{DD}$ where I_{off} is measured as the device at the off-state (not totally off due to leakage).

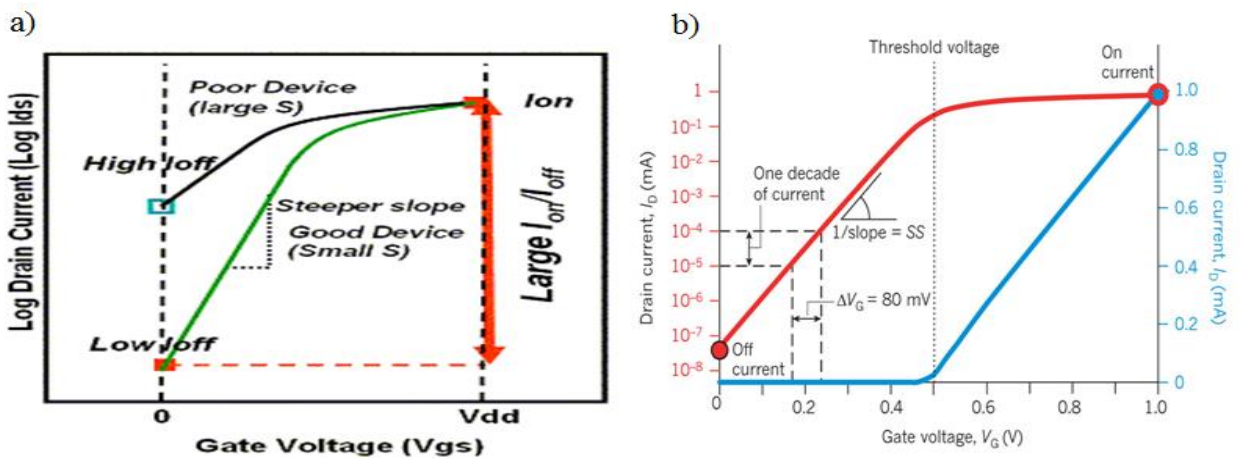


Figure 4.2: Subthreshold swing a) Describe the ratio I_{on}/I_{off} at subthreshold region b) The measurement of subthreshold swing and the on-state and off-state of the device.

Figure 4.2.a shows the need of high I_{on}/I_{off} ratio for better performance where the Figure 4.2.b presents an example of subthreshold swing (S) measurement. A better functionality for ultra-low-power designs is presented in steeper slope (small S) where I_{on}

is measured high and I_{off} is low, hence, reduced threshold voltage. The subthreshold slop is defined as:

$$S^{-1} = \frac{\partial \log I_D}{\partial V_G} = \frac{1}{2.3(k_B T/q)} \frac{\partial \psi_S}{\partial V_G} \quad (4.1)$$

And the subthreshold swing is defined as:

$$S = \frac{\partial V_G}{\partial (\log I_D)} = \frac{\partial V_G}{\partial \psi_S} \frac{\partial \psi_S}{\partial (\log I_D)} = \left(\frac{k_B T}{q} \right) \left(\frac{\partial V_G}{\partial \psi_S} \right) \times \ln(10) \quad (4.2)$$

Where $\frac{\partial V_G}{\partial \psi_S}$ called the body factor and titled η .

V_G is related to ψ_S by a capacitive voltage divider show in Figure 4.3 [55]. ‘S’ could be expressed as:

$$S = \ln(10) \frac{kT}{q} \left(1 + \frac{C_{dep}}{C_{ox}} \right) \quad (4.3)$$

If there is a significant trap density (C_{it} : surface state capacitance):

$$S = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \right) \quad (4.4)$$

$$S_{min} = 2.3(KT/q) = 60 \text{ mV/dec} \quad (4.5)$$

Where C_{dep} is the depletion region capacitance, and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the gate oxide capacitance per unit area. ‘S’ also characterizes the importance of the interface traps on device performance, and can be approximated as in (3) using the capacitive voltage divider as in Figure 4.4. If there is a significant trap density then ‘S’ can be approximated by (4). The depletion region capacitance C_{dep} is proportional to doping density N_A and

W_{dep} is the maximum depletion width in strong inversion. We can write: $C_{dep} = \frac{\epsilon_{si}}{W_{dep}} \propto$

$$\sqrt{\frac{1}{N_A}}$$

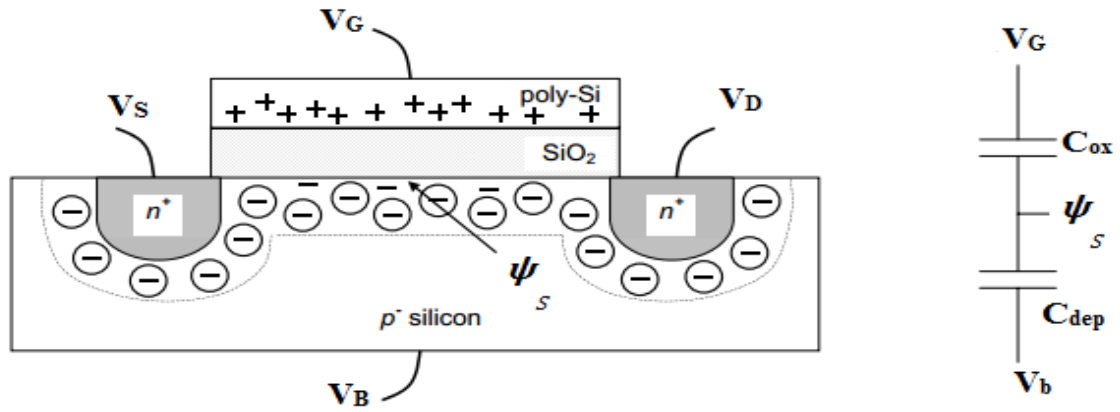


Figure 4.3: MOSFET and its equivalent capacitance coupling [56].

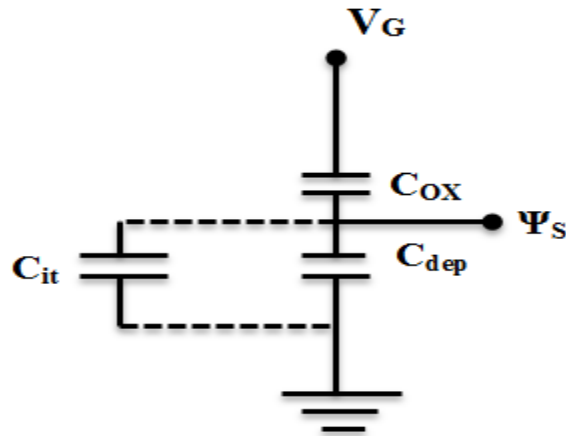


Figure 4.4: MOSFET equivalent capacitance coupling in case of significant trap density
 Smaller value of S gives a better turn-on performance of device, because smaller value of S means for a certain change in current we will need lower voltage change or for a certain change in voltage we can get higher current change leading larger gain from the device.
 From equations (3) and (4) we can predict that if theoretically it is possible to make both

C_{it} and C_{dep} zero in a conventional MOSFET device then the value of S at $T= 300K$ temperature will be 60mV/decade as shown in (5), which is known as the theoretical minimum (S_{min}) subthreshold swing. This value can be achievable only in the oxide thickness in silicon device approaches to zero. However, under any practical scenario this is not possible, and the factor η in (3) and (4) will be always larger than 1 ($\eta \geq 1$). Therefore, S in silicon device is larger than 60mV/decade (typical it is in the range of 80-120mV/decade).

4.2 How to Achieve S Less Than 60mV/ decade

The body factor is defined earlier as:

$$\eta = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_{dep}}{C_{ox}} \quad (4.6)$$

The equation (6) shows that η has multiple key dependencies that have significant impact on the value of S . below is list of those key parameters and how they related to S .

- ✚ The gate oxide capacitance per unit area is defined as $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ where t_{ox} gate oxide thickness and ϵ_{ox} is the permittivity of the oxide. Decreasing t_{ox} will give a large C_{ox} accordingly a lower η . Hence, a sharper subthreshold can be achieved ($t_{ox} \downarrow \rightarrow C_{ox} \uparrow \rightarrow \eta \downarrow \rightarrow$ Sharper subthreshold).
- ✚ Higher dielectric constant (high-k) such as HfO_2 to replace SiO_2 is becomes necessary requirement for gate insulator. High-k lead to high oxide capacitance

which leads to high I_{ON} and decrease gate tunneling by several orders also leads to low I_{OFF} .

- ✚ Sub-threshold doping: It's clear that the sub-threshold voltage is controlled by doping of the channel. The thickness of the depletion layer is depends of doping level. A lower doping will cause a thicker depletion layer, therefore a higher depletion capacitance, and a softer subthreshold. ($N_A \uparrow \rightarrow C_{dep} \uparrow \rightarrow \eta \uparrow \rightarrow$ Softer subthreshold)
- ✚ Substrate bias: When a substrate bias is applied the depletion thickness increases, and the subthreshold swing decreases. ($|V_{bs}| \uparrow \rightarrow C_{dep} \downarrow \rightarrow \eta \downarrow \rightarrow$ Sharper Subthreshold)
- ✚ Temperature: At room temperature (300 K), the ideal limit of S is 60 mV /decade. Normally, devices always work in higher temperature due to heat dissipation; the S will be higher at greater temperature than room temperature. S can be also lowered at lower temperature. The equations (3) and (4) show that the subthreshold swing is proportional to temperature T. moreover the subthreshold drain current proportional to $1/T$ ($T \uparrow \rightarrow$ Softer Subthreshold).

There is a trade-off between V_T and ON/OFF current. Low V_T is required to have a high on-current, where V_T is needed for low off-current. The equation (4.7) shows the saturation drain current dependencies of supply voltage/power and subthreshold voltage.

$$I_{DSAT} \propto (V_{DD} - V_T)^\alpha \quad 1 < \alpha < 2 \quad (4.7)$$

The leakage mostly happened when the circuit inactive, this waste of power represents in I_{OFF} . To reduce the device leakage a long-channel and large threshold voltage are required. Conversely, performance and power budget are compromised.

4.3 High-k Gate Insulator

The electric field is the key to speed up the channel formation of the transistor, therefore a fast switching. Lowering the gate oxide thickness improved the electric field applied by the gate at every technology node. Hence, increasing the gate capacitance and thereby drive current. At sub-nano scale, SiO_2 can no longer serve this purpose due to the physics limitation (as the thickness scales below 2nm), and leakage upsurge. Farther scaling would increase the electrons tunneling therefore increases gate current leakage. To overcome this issue a new materials with high dielectric constant (high- κ) were used in current process to serve as gate oxide. Some of these materials are presented in table 4.1.

Table 4.1: Some of the high-k materials and their properties [57]

| <i>Dielectric</i> | <i>Dielectric constant (bulk)</i> | <i>Bandgap (eV)</i> | <i>Conduction band offset (eV)</i> | <i>Leakage current reduction w.r.t. SiO₂</i> | <i>Thermal stability w.r.t. silicon (MEIS data)</i> |
|--|-----------------------------------|---------------------|------------------------------------|---|---|
| Silicon dioxide (SiO ₂) | 3.9 | 9 | 3.5 | N/A | >1050°C |
| Silicon nitride (Si ₃ N ₄) | 7 | 5.3 | 2.4 | | >1050°C |
| Aluminum oxide (Al ₂ O ₃) | ~10 | 8.8 | 2.8 | 10 ² -10 ³ × | ~1000°C, RTA |
| Tantalum pentoxide (Ta ₂ O ₅) | 25 | 4.4 | 0.36 | | Not thermodynamically stable with silicon |
| Lanthanum oxide (La ₂ O ₃) | ~21 | 6* | 2.3 | | |
| Gadolinium oxide (Gd ₂ O ₃) | ~12 | | | | |
| Yttrium oxide (Y ₂ O ₃) | ~15 | 6 | 2.3 | 10 ⁴ -10 ⁵ × | Silicate formation |
| Hafnium oxide (HfO ₂) | ~20 | 6 | 1.5 | 10 ⁴ -10 ⁵ × | ~950°C |
| Zirconium oxide (ZrO ₂) | ~23 | 5.8 | 1.4 | 10 ⁴ -10 ⁵ × | ~900°C |
| Strontium titanate (SrTiO ₃) | | 3.3 | -0.1 | | |
| Zirconium silicate (ZrSiO ₄) | | 6* | 1.5 | | |
| Hafnium silicate (HfSiO ₄) | | 6* | 1.5 | | |

*Estimated value.

The new gate insulator materials that are investigated have to fit certain requirements.

These requirements are discussed in [58, 59].

CHAPTER 5

TUNNELING FIELD EFFECT TRANSISTORS

The tunneling field effect has widely explored and multiple proposals are presented. The tunneling phoneme was introduced to overcome the thermal voltage limitation of the conventional MOSFET. Multiple proposals based on Band-To-Band tunneling (BTBT) that include several material and structures were suggested. Band-To-Band tunneling devices recommended by numerous scholars' shows that the subthreshold swing can be lower and 60mV/decade since its independent of the thermal voltage (KT/q).

5.1 Introduction

The demand for fast computing devices, more applications, smaller dimensions and low power consumption requires new architecture and/or material exploration to be the base of the future ICs. Field effect transistors in general have marvelous progress in the last few years. This progress that covers but not limited to down-scaling and power supply reduction has managed to increase the number of devices in single ship. Power management and heat dissipation are two major concerns in current IC design. Down-scaling of the MOSFET was the only road to achieve high performance and low power consumption.

Recently, the new born FinFET shows that the silicon devices will remain the base of the future ICs for few generations. Tri-gate also known as FinFET was introduced due to its

similarities to conventional MOSFET. The fin shape introduces a gate voltage that surrounds the channel from three sites. This structure present a better control over short channel effect. The new structure also shows a higher I_{on}/I_{off} ratio as compared to conventional MOSFE. FinFETs present a better performance, lower leakage current, and fabrication compatibility with CMOS process [64]. However, the value of S is limited by the thermal voltage " kT/q ". S still has a minimum value of 60mV/decade at room temperature.

Currently, no proposal based on non-silicon material has succeeded to be considered as potential changeover from the existing silicon based FETs. New alternative are coming out to overcome the physic limitation of the planar MOSFET. The tunneling field effect has widely explored and multiple proposals are presented. The tunneling phenomena were introduced to overcome the thermal voltage limitation of the conventional MOSFET. Multiple proposals based on Band-To-Band tunneling (BTBT) that include several material and structures were suggested. Band-To-Band tunneling devices recommended by numerous researchers' shows that the subthreshold swing can be lower than 60mV/decade (at room temperature) since it's independent of the thermal voltage (KT/q) [4].

5.2 Tunneling Phenomena- Esaki Tunnel Diode

Tunnel diode is p-n junction where the charges can cross the barrier if the barrier is too small as opposed to the conventional transport where the carriers require higher energy than the barrier height. One way to lower the depletion region (thin region

between p and n) is to use a highly doped p and n regions. This method will increase the probability of electrons/ holes to tunnel from one region to the other. By Applying a forward bias voltage the electrons in the conduction band of the n region will tunnel to the empty states of the valence band in p region. This phenomenon will cause a current flow called forward bias tunnel current. A maximum current can be reached if the bias voltage increase and the electrons of the n-region are equal to that of the holes in the valence band of p-region. As the bias voltage keep increases the number of electrons that able to tunnel decreases. Thus, the tunneling current decreases. As more forward voltage is applied, the barrier potential lowered. In this stage the tunneling current stops and the current flow due to the electron hole injection increase. In case of reverse bias (small negative voltage), the electrons in the valence band of the p-side tunnel towards the empty states of the conduction band on the n-side. This phenomena creates a large tunneling current that increase significantly with slim increase of the reverse bias voltage [66].

5.3 Various Tunneling Field Effect Transistors

Hitachi in 1988 proposed new type of MOSFET. The device was based on Band-To-Band Tunneling (BTBT) and they called it B²T-MOSFET. the device takes advantage of diffusion difference of N⁺-doped source and P⁺-doped drain, and the channel is p-doped for p-type devices and n-doped for n-type devices. This new proposal suffers from hole-trapping in n-type MOSFET. This issue causes hot-carrier-induced-degradation, where the threshold voltage decreases and the conductance increase [67].

5.3.1 Inter-band SOI

Subthreshold swing is an important figure of merit that describes how fast a device can turn ON and switch OFF. In the MOSFET, the subthreshold swing is limited by the thermal voltage $\left(\frac{KT}{q}\right) \ln 10$ ($= 60 \text{ mV/decade}$). In [71] an analytical inter-band SOI tunnel transistor shows a subthreshold below 60 mV/decade . The device geometry is shaped as a lateral $p^+ \text{-} n^+$ tunnel junction formed in ultrathin semiconductor body. The junction is sited in top of a silicon insulator (SOI structure). The gate is placed over the p-side for superficial electrostatic control. The device geometry is shown in Figure 5.1.

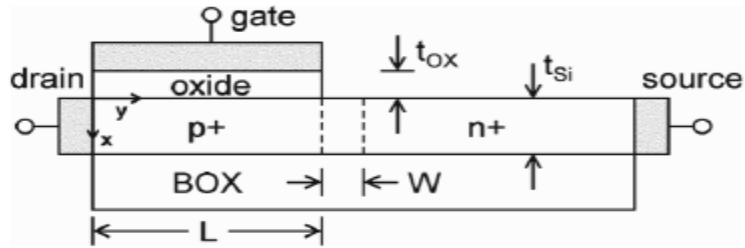


Figure 5.1: Schematic cross section of an inter-band tunnel transistor where the ultrathin Si is heavily doped to form a $p^+ \text{-} n^+$ tunnel junction, and the gate is placed over the fully depleted p-side [71].

The device 2-D simulation illustrate a subthreshold of about 7 mV/decade occurs near $V_{GS} = 0.07 \text{ V}$. This device also can achieve an on-state current of $850 \mu\text{A}/\mu\text{m}$ using a Ge channel, and a low off-state current ($< 0.1 \text{ nA}/\mu\text{m}$).

5.3.2 Carbon Nanotubes CNT

The carbon nanotubes offer an admirable fit as a channel for the future field effect transistors. Quantum mechanical tunneling of carriers from valence band to conducting

band and vice versa presents a great advantage due to the small band gap. BTBT introduce the possibility of accomplishing a subthreshold slop less than 60mV/ decade at room temperature. Whereas the BTBT current in silicon is small, the CNTs show the possibility of producing a large BTBT current. In [61], a device structure was submitted, and a numerical analysis was simulated. This paper shows that a much steeper band banding can accomplished and a 46mV/decade subthreshold swing can be reached. This simulation also shows that BTBT is intensely depends on the doping profile of the S/D regions. The off-state current can be lowered by using a low S/D doping profile. The proposed structure is shown in Figure 5.2.

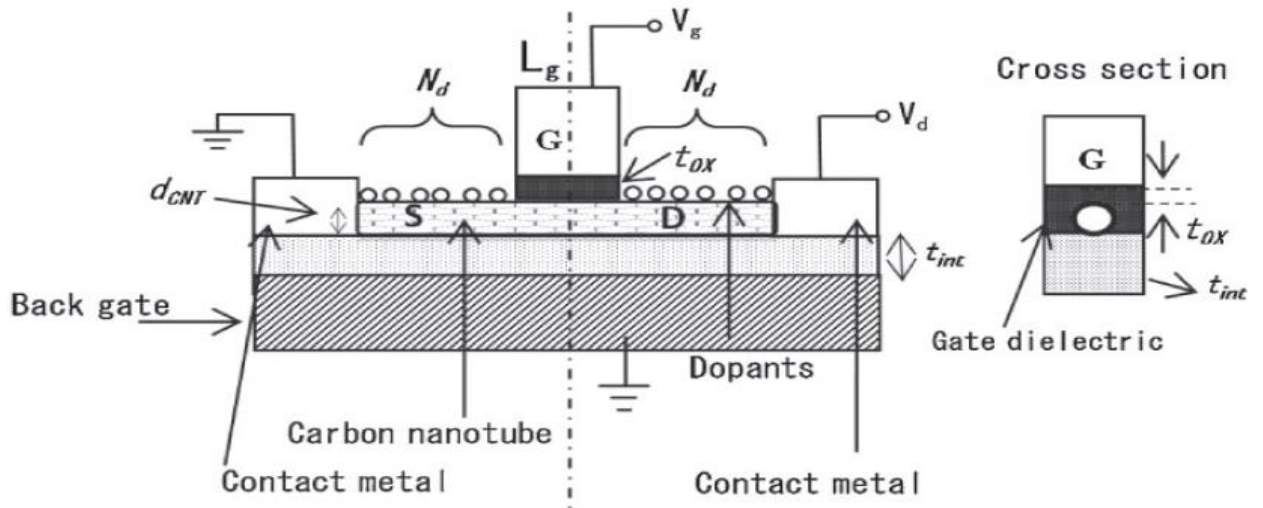


Figure 5.2: Carbon nanotubes tunneling field effect transistors [60]

The amplification of the off-state current has put a dead end to any farther scaling of the conventional MOSFET. In [67] a numerical simulation presented based on gated p-i-n junction. The device employed carbon nanotube with a p-doped source side and n-doped drain side. The gate voltage controls the band bending of the channel. For a given

gate voltage, if the conduction channel is above the valence band of the source the carriers cannot tunnel cross, due to channel width that act as barrier. Oppositely, by having the conduction channel is below the valence band of the source carrier can tunnel through generating a drain current for a given $V_{DS} > 0$. A sharp switching can be achieved providing a subthreshold swing less than 60mV/decade. The Figure 5.3 shows the structure and the band diagram of the studied device.

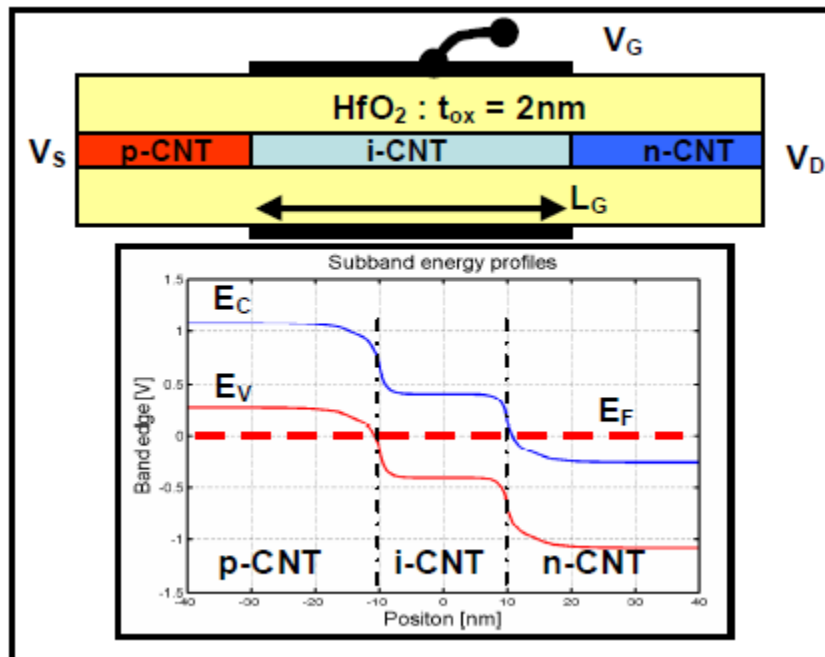


Figure 5.3: Simulated carbon nanotube p-i-n device with cylindrical high-k gate: $t_{OX} = 2\text{nm}$ (HfO_2 , $k \sim 16$), (13,0) zigzag CNT, $d_{\text{CNT}} = 1\text{nm}$, $E_G = 0.8\text{eV}$, $L_G = 20\text{nm}$. The source/drain doping is $1.0 \times 10^7 \text{cm}^{-1} = 1 \text{dopant/nm}$ (for comparison (13,0) CNT has 122 carbon atoms/nm). The equilibrium band structure is also shown.

The numerical simulation in [67] of different CNTs structures was present in Figure 5.3.

(10, 0) CNTs that have a small band gap (1eV) provide a large $I_{\text{on}}/I_{\text{off}}$ ratio ($>10^8$ at V_{DD}

=0.4 V) and a subthreshold swing of 25mV/decade. Three different CNTs structures were tested, the Figure 5.4 illustrate the result.

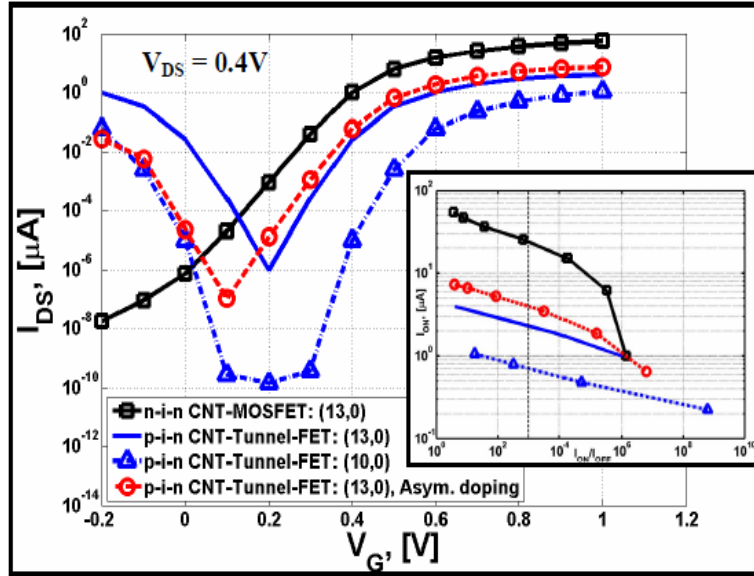


Figure 5.4: Ballistic I_{DS} - V_{GS} for three p-i-n Tunnel-FETs and a CNTMOSFET. Inset: corresponding I_{ON} vs. I_{ON}/I_{OFF} results at $V_{DD} = 0.4\text{V}$. Asymmetric doping (dashed curve) is: heavily doped source ($1.5 \times 10^7 \text{cm}^{-1}$) and lightly doped drain ($0.25 \times 10^7 \text{cm}^{-1}$) respectively [67].

In this research a large on-current was produced ($> 1\mu\text{A}/\text{tube}$), and demonstration of subthreshold swing lower than 60 mV/decade, as well as high I_{on}/I_{off} ratio.

Reducing the power consumption, while keeping the I_{on}/I_{off} ratio constant is a major challenge of gate length scaling in modern technology. Logic switches with altered operations were proposed to overcome the 60 mV/decade limitations. In [78] a new concept of a device based upon BTBT in nanowire FET (NW-FET) was introduced. The device employed a dual-gate carbon nanotube that controls the tunneling of carries between the both doped-extended drain and source. The device is based on Esaki diode

that includes a negative gate voltage that is applied on the p-portion of the p-n junction. This device proposal presents the possibility of having a subthreshold slop that is far below 60mV/decade. The Figure 5.5 displays the band diagram of the gated p-n-junction. The BTBT probability $T(E)$ between the source and the channel is approximated for a triangular potential using the WKB approximation and its given as: $T(E) =$

$$\exp\left(-\frac{4\sqrt{2m^*E_g^2}}{3|e|\hbar\xi}\right)$$

where m^* is the effective carrier mass, E_g is the band gap, $\xi = (E_g +$

$\Delta\Phi)/\lambda$ is the electric field in the transition region, $\lambda = \sqrt{\frac{\varepsilon_{nt}}{\varepsilon_{ox}}d_{ox}d_{nt}}$ is the screening

Length, ε_{nt} and ε_{ox} are the dielectric constants of the gate oxide layer and CNT, d_{ox} is the thickness of the gate oxide and d_{nt} is the diameter of CNT.

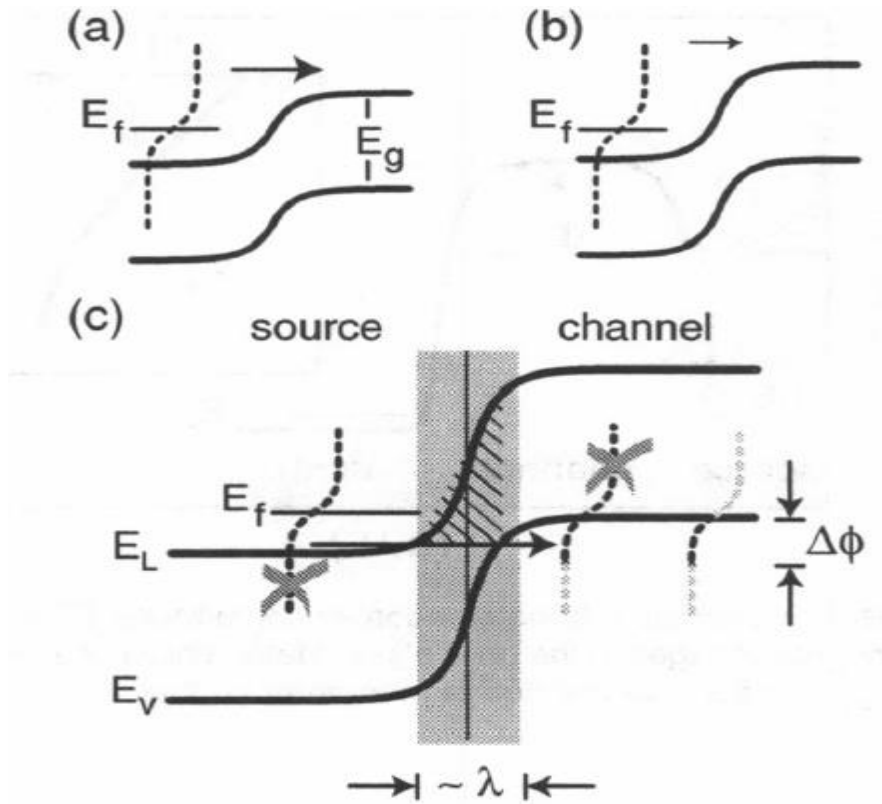


Figure 5.5: Source-channel diode for three different gate voltages. (a) and (b) Thermal emission of carriers over the barrier gets exponentially suppressed. (c) If E_v in the channel is lifted above E_L in source, BTB tunneling occurs. The particular band profile acts as band pass filter that cuts off the high and low energy tail of $f_s(E)$ [68].

A small effective mass and characteristic in addition to 1D electronic transportation leads to high on-current and low subthreshold swing. A small band gap can also increase the probability of tunneling, on the other hand increases the I_{off} . CNTs are suitable due to their 1D transport, small m^* and diameter d_{nt} and reasonable E_g . In addition, their integration ability with high- κ materials that provides a small λ .

This device was fabricated using a high doped silicate substrate (back gate), separated from the nanotube by a 10nm, an extended-doped source/drain of length L_{bg} around

200nm. An aluminum gate placed in top of the SiO₂ to avoid any influence of the back gate on the channel. An Al₂O₃ of 4nm employed as the gate oxide. Latterly, the nanotube is connected with titanium contacts. Figure 5.6 displays the fabricated device.

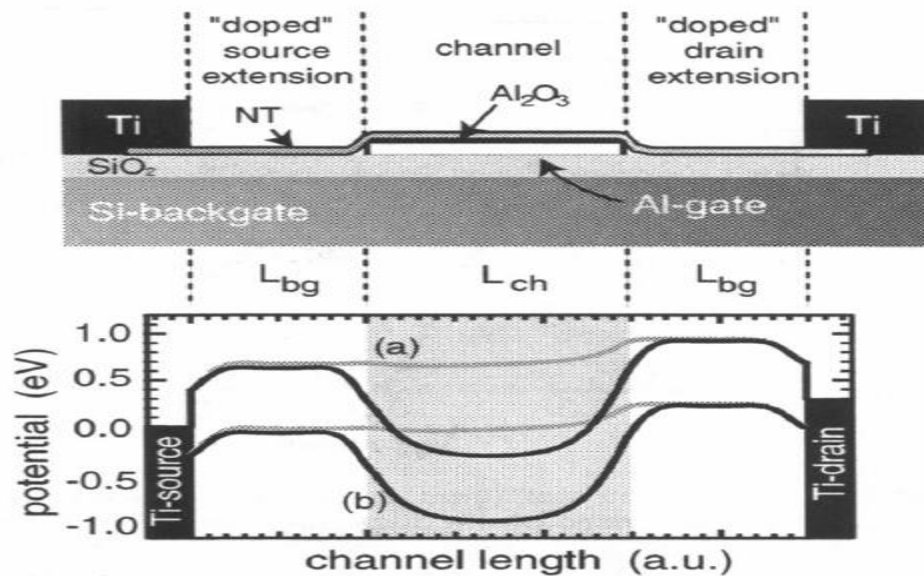


Figure 5.6: Schematics of the dual-gate CNTFET. Source/drain extensions are electrostatically “doped” with the silicon back-gate. The lower part shows the band profile for (a) the device operated as conventional p-type FET and (b) operated in the BTB tunneling regime [67].

This device illustrates a subthreshold swing of 15mV/decade.

5.3.3 Graphene Nanoribbon GRN

Graphene nanoribbon (GNR) is considered a noble fit for nanotechnology. Tunneling field effect transistors based on GNR have shown great compensations over other nano-materials. Low bandgap (bandgap depending on their width), high mobility, and near- ballistic performance are some of the major advantages of the GNR. A structure of p-channel GNR tunnel transistor is proposed by [62] shown in Figure 5.7. In

this structure, the source is heavily n-doped and the drain is heavily p-doped. The Zener tunneling probability was calculated by applying the WKB approximation to a triangular potential with a barrier height of E_G (bandgap) [62, 63].

$$T_{WKB} = \exp\left(-\frac{\pi}{4} \frac{E_G^2}{\hbar v_F q \xi}\right)$$

Where ξ is the electric field across the tunnel junction, \hbar is the Planck constant, and v_F is the Fermi velocity of carriers in graphene.

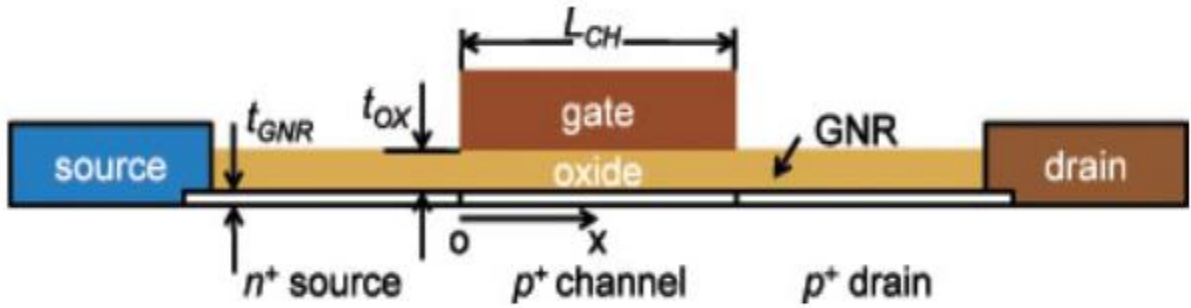


Figure 5.7: The proposed structure of the graphene nanoribbon FET [62].

The device geometry shown in Figure 5.7, the calculations illustrate that an on-state current density of $800\mu\text{A}/\mu\text{m}$ can be reached and an off-state current of $26\text{ pA}/\mu\text{m}$. The device also demonstrates an I_{on}/I_{off} ratio of more than seven orders of magnitude, and a very low subthreshold swing.

5.1.1 Silicon Nanowires

Silicon Nano-wires (SiNW) have gotten a much attention in the emerging technology. In [60] a vertical gate-all-around GAA nanowire (NW) based tunneling field-effect transistor (TFET) was Fabricated using a top-down compatible process technology.

The TFET operated as gated p^+i-n^+ in reverse bias mode. The device designs such that no tunneling occurs in the off-state due to large barrier between the source and the drain. The proposed structure presented in Figure 5.8.

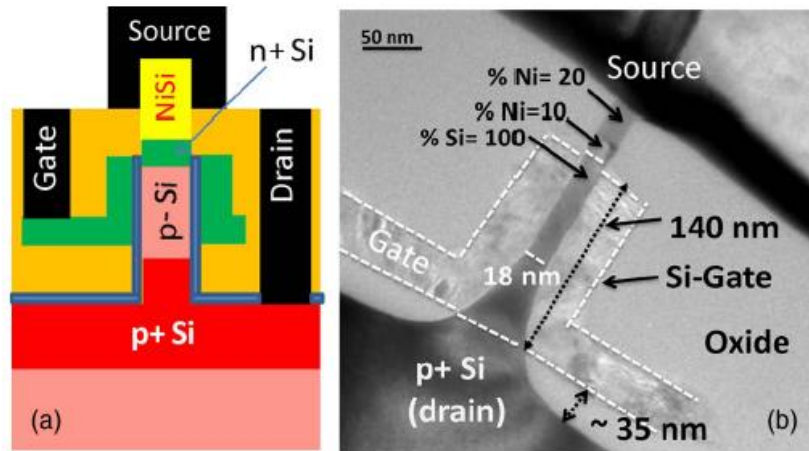


Figure 5.8: (a) Device schematic and (b) TEM image of the fabricated device with a nanowire diameter of ~ 18 nm and a gate length of ~ 140 nm [60].

By pulling down the energy band of the channel region and reducing the width of the barrier, the carrier can tunnel from the valence band to the conduction band. Henceforth, the on-state current is generated. This device offered a high I_{on}/I_{off} ($\sim 10^5$) and subthreshold of 50 mV/decade for about three of drain current and 30 mV/decade for more than one decade of drain current.

5.3.4 Staggered Hetrojunctions

Multiple geometry and material considered based on gated $p-i-n$ junction. [64] Proposed a tunneling FET based on tunnel III-V staggered hetrojunctions. The device used high-k dielectric as gate oxide (Al_2O_3), $Al_{0.5}Ga_{0.5}As_{0.3}Sb_{0.7}$ as source, $In_{0.8}Ga_{0.2}As$

as channel, and $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}$ as drain. Material lineup of the device is shown below. This device operated at 0.3V, derives an on-state current of 0.4mA/ μm and has an off-state current of 50nA/ μm . Even though tunneling field effect transistors in many research shows the possibility of having a subthreshold swing lower than 60 mV/decade at room temperature, the devices suffer from low on-current (lower than in MOSFETs). In [64], the focuses on the GaSb/InAs(Sb) hetero-structure, that forms a broken type II band alignment. The device with p+/n doping profile hetero-structure was investigated and shows a high on-current. Material lineup of this type of devices is shown in Figure 5.9.

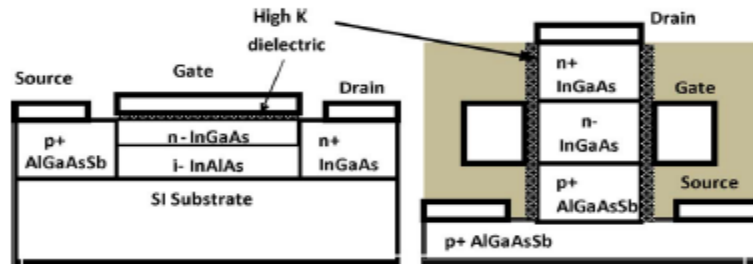


Figure 5.9: Schematic drawing of the prototype TFET device with planar and multi-gate embodiments [64].

Since silicon indicated a poor qualification in the revolutionary tunneling field effect transistors (large band gap is one of the disqualifications (1.1 eV)). New materials were investigate and considered to bring better outcome. Materials such as SiGe with lower band gap (~0.9 eV) shows a superior advantages over silicon on gated diodes devices. [72] proposed a tunneling FET using strained-Si/strained-Ge lateral heterojunctions(HTFET). This combined structure has type-II band alignment, and provides a small energy barrier tolerating an enhanced tunneling at the heterointerface

along with a large band gap past the interference region. Figure 5.10.a illustrates the simulated structure. Figure 5.10.b shows the band diagrams that describe the concept of operation of the device. The device operation explained as follow: by applying a gate voltage a the energy band overlap at the heterointerface allowing the electrons to tunnel from the valence band of the strained Ge to the conduction band of the strained Si. The advantage of this proposal is the high tunneling rate established by short tunneling barrier at the injection region, and large band gap way from that region.

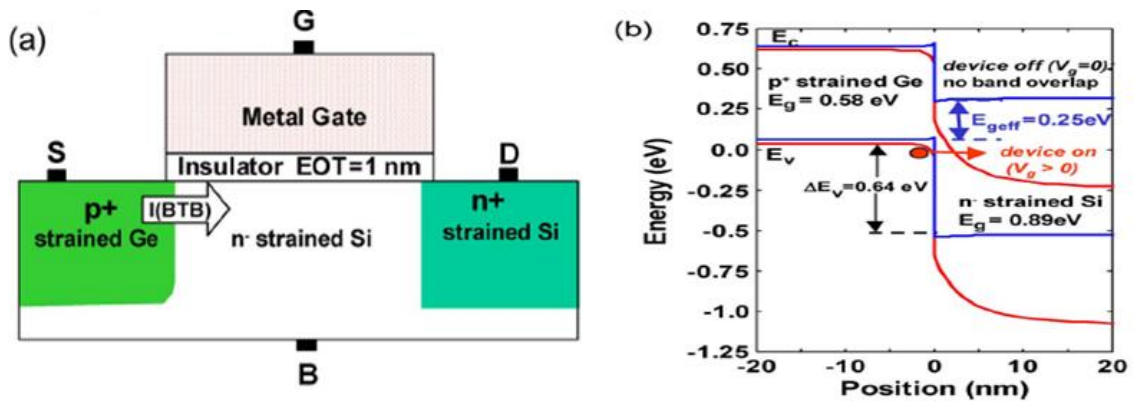


Figure 5.10: (a) Schematic of the simulated HTFET with a metal gate with $L_{gate}=35$ nm and a gate insulator with $EOT=1$ nm. (b) Energy band diagrams near the strained-Ge/strained-Si heterointerface in the OFF and ON states of the HFET [72].

Since there are several proposals related to the tunneling phenomena, none of those proposals have the practicability to become the base of the future ICs design especially in the ultra-low-power applications.

CHAPTER 6

I-MOS AND NANOWIRE FETS

I-MOS and the Nanowire Field effect transistor are two proposals that show a promising future in the ULP designs. These proposals are extensively studied by various groups illustrate a subthreshold swing exceptionally low.

6.1 Impact Ionization Transistors

Impact ionization is different proposal to design transistors. High energetic charge carriers (electrons) strike a molecule causing a mobility of the electrons of that atom. The liberated electrons gain enough energy to move from valence band to the conducting band creating an electron hole pair. The free electrons may move fast enough to knock other electrons, creating more free-electron-hole pairs creating more charge carrier. Based on this concept the *impact-ionization metal-oxide-semiconductor (I-MOS)* was designed.

I-MOS devices first proposed in 2002 by Gopalakrishnan et al [74]. The device enticed an extensive consideration especially in ultra-low-power designs. The ability for this proposal to achieve a low subthreshold swing has drawn researcher's attention in the last decade. The I-MOS was design based on PiN structure and a gate partially covering the intrinsic area at the source side [73]. Figure 6.1 displays the most common structure of this proposal. To reduces the influence of the drain bias on the breakdown voltage and to improve the short channel effect the drain extension in this design is lightly doped [74]. As point out in various section of this research, the thermal limitation " KT/q " or (60mV/

decade at room temperature) is the bottom limits of the subthreshold swing that can be achieved by the conventional MOSFET. I-MOS was proposed to solve some of scaling problem (mainly short channel effect). This device simulation also shows that the subthreshold swing much lower than the above declared [73, 74].

Simulation in [73, 74], claimed that the device can produce a subthreshold swing below 5mV/ decade. Hence, a very high I_{on}/I_{off} and low off-state leakage.

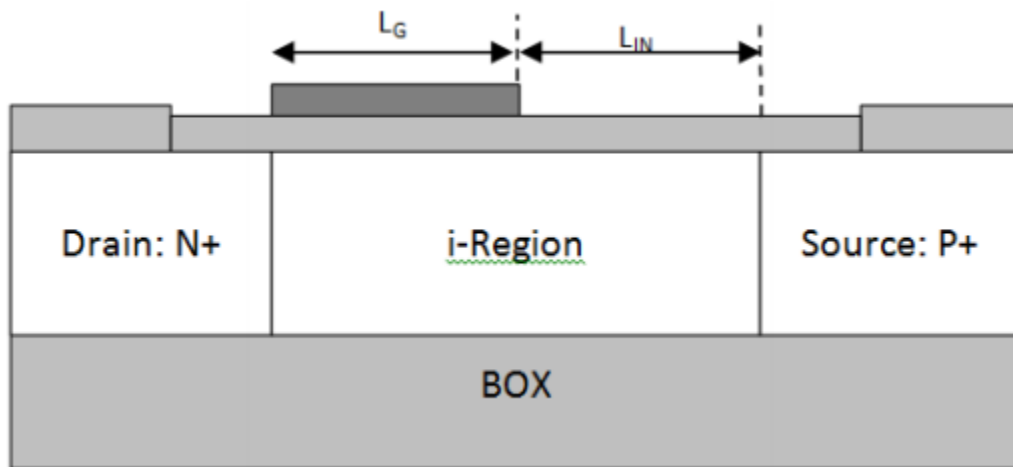


Figure 6.1: The basic structure of Lateral I-MOS [74]

One of the draw backs of the I-MOS is the requirement of a fairly large source bias V_S for the I-MOS. Few adjustment based on the same concept to overcome this issue are proposed in [76].

The I-MOS suffer from reliability and threshold voltage stability in addition to integration difficulties to existing CMOS technology (fabrication process). To accomplish a subthreshold swing better than “ KT/q ” and maintain a lower supply voltage different structure I-MOS was proposed. The L-shaped I-MOS (LI-MOS) was proposed

to overcome the previously discussed issues of the I-MOS [79]. This proposal achieves a subthreshold swing below 5mV/decade.

6.2 Nanowire Transistors

As the transistor shrinks the length also shrinks reducing the gate capability to control the channel. This dimensional reduction causes a current flow even at the absence of gate voltage (off-state current) as a result the power consumption at idle state increase drastically. This leakage current is increased at every transistor generation. In order to lower this effect while maintaining a high performance, various schemes were introduced. Nanowire (NW-FET) and Tri-gated field effect transistor are one of the proposals presented to overcome the issues of scalability. These architectures propose a better gate control over the channel. However, in the thermionic emission, carriers are thermally excited in the source, and then they go over the potential barrier beneath the gate. Thermionic emission carrier transport limits the subthreshold swing to “ KT/q ” or 60 mV/ decade. Several approaches to outperform this limit are presented in new physics, new structure, and/or new materials are investigated over the years.

Nanowire architecture was utilization in tunneling carrier transport to break the thermal limits of the subthreshold swing. This methodology has some limitations of low on-state current, and the steepest switching slope is not sustained across the whole turn-on curve [78, 79].

In [78, 79], 13mV/dec and an on-state current $I_{ON} = 4.5\text{mA}/\mu\text{m}$ at $V_{DD} = 0.4\text{V}$ was reported. This proposal exploit InGaAs-InALAs pair placed in between the source and

the channel. The device structure is presented in Figure 6.2. The area between the source and the channel of NW-FET was devised by interposing a superlattice (SL) as shown in Figure 6.2.b.

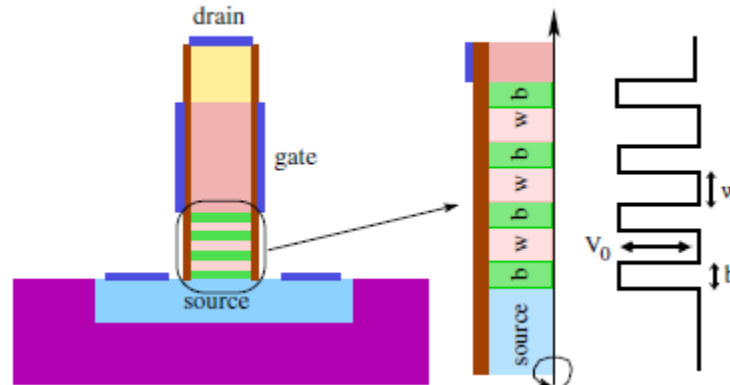


Figure 6.2: Pictorial view of the nanowire cross section and of the band diagram. The SL is realized with multiple barrier (b) and well (w) layers interposed between the source and the channel. Different materials can be used for the source, superlattice, channel and drain regions [78].

CHAPTER 7

FERROELECTRIC BASED FIELD EFFECT TRANSISTORS

As needed to keep Silicon technology as the base technology while modernizing future devices; cost is an important factor advance researches introduced multiple substitution. Scientists and engineers are investigating new physics, new materials as well as new devices structure that can lead to steep subthreshold swings less than 60mV/decade. The currently marketed FinFET has shown a better performance compared to the conventional MOSFET. This device has geometrical improvements that allow a better channel control. In previous chapters, we have introduced another focus of the research that concern using different materials. Materials like Carbon Nanotube, and Graphite shows superior performance. Other alternative that uses new physics is currently explored. Band-To-Band tunneling has been introduced for high performance and low power consumption.

In this chapter, new and different propositions to reduce subthreshold swing are presented. Those proposals require integrating a ferroelectric materials to operate in negative region (negative capacitance) into MOSFET basic structure.

7.1 Negative capacitance Concept:

The subthreshold swing well defined in chapter 4, for convenient the definition is repeated in this section.

$$S^{-1} = \frac{\partial \log I_D}{\partial V_G} = \frac{1}{2.3(k_B T/q)} \frac{\partial \psi_S}{\partial V_G} \quad (7.1)$$

And the subthreshold swing is defined as:

$$S = \frac{\partial V_G}{\partial (\log I_D)} = \frac{\partial V_G}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log I_D)} = \left(\frac{k_B T}{q} \right) \left(\frac{\partial V_G}{\partial \psi_s} \right) \times \ln(10) \quad (7.2)$$

Where $\frac{\partial V_G}{\partial \psi_s}$ called the body factor and titled η .

V_G is related to ψ_s by a capacitive voltage divider show in Figure 7.1 [92]. ‘S’ could be expressed as:

$$S = \ln(10) \frac{kT}{q} \left(1 + \frac{C_s}{C_{INS}} \right) \quad (7.3)$$

Considering the coupling capacitance between the gate voltage and the bulk to estimate “S”. Figure 7.1 illustrate the capacitance involved in the estimation. For a short channel modeling, analytical solution used voltage-doping transformation (**VDT**) is considered. This estimation also considered linearly varying potential **LVP** approximation to obtain the swing voltage [82, 84]. The body-factor of Si-bulk MOSFET can be approximated as in (7.4)

$$\eta = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{INS}} \quad (7.4)$$

ψ_s Semiconductor surface potential

η Body factor

C_s Semiconductor capacitance

C_{INS} Gate insulator capacitance

If $0 < \eta < 1$ As a result $\frac{C_s}{C_{INS}} < 0$ therefor $C_{INS} < 0$ a negative capacitance is needed to

achieve a subthreshold swing lower than $S < 60$ mV/ decade.

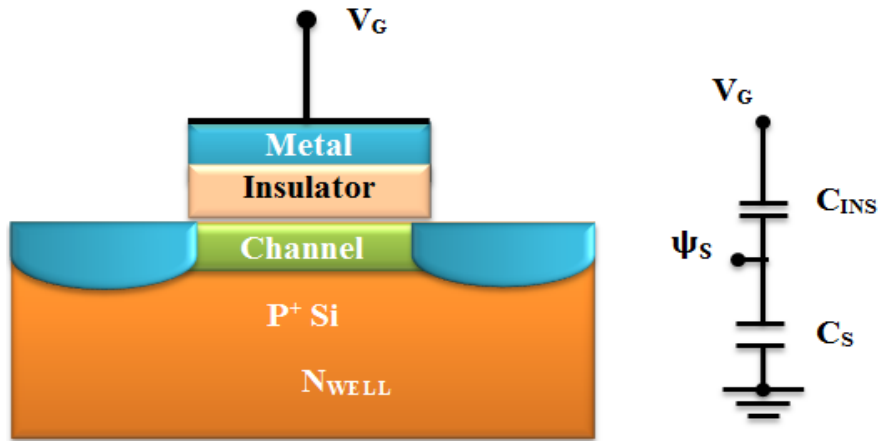


Figure 7.1: Si-Bulk MOSFET and its equivalent capacitance coupling

For stability device the overall capacitance has to remain positive. As well as keeping similar transistor operation where the Negative capacitance will act as an amplifier promoter.

7.2 Ferroelectric Material Properties

Ferroelectric properties, materials have been overlooked in the last 10 years. This interest has been driven by the exciting possibility of using ferroelectric thin films for a gate stack MOSFET. The hysteresis properties made it possible for Ferroelectric Random Access Memory or F-RAM to be present in commercial production. Figure 7.2 explains the hysteresis properties and the charges loading of certain ferroelectric materials. The charge on a ferroelectric capacitor does not go back to zero at 0V unlike linear and paraelectric capacitors. Some of the charge inside the capacitor will be trapped (cannot come out), and yet it still has zero volts on it. The reason is that the ferroelectric material between the plates of the capacitor has a naturally occurring built-in electric

field. That electric field pulls in from the circuit just the right amount of excess charge of the opposite polarity to cancel itself at the surface of each plate. Therefore, even though the excess charge on each plate [85].

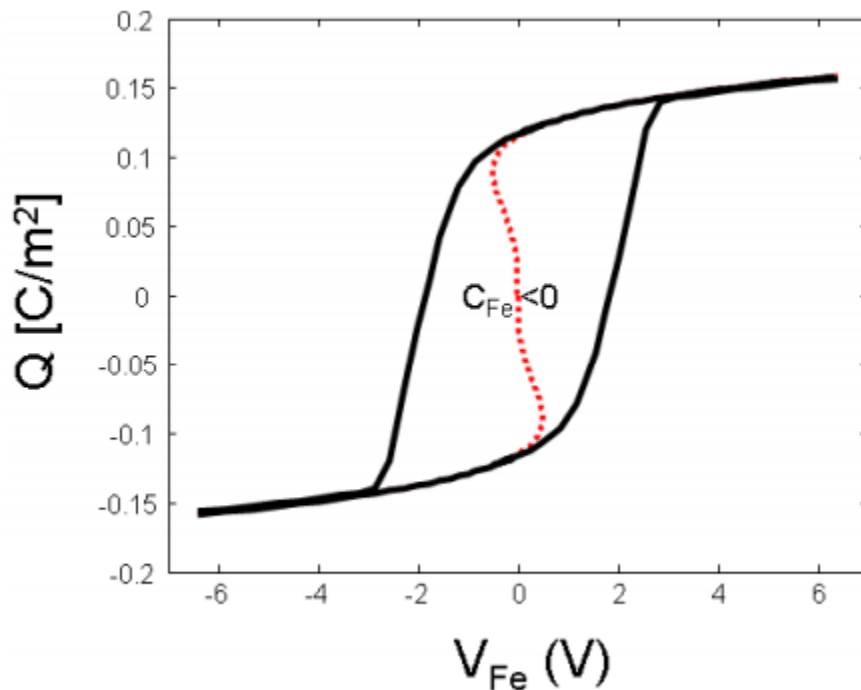


Figure 7.2: Hysteretic behavior of ferroelectric material [85]

7.3 Negative Capacitance

Ferroelectric materials introduced a new hypothesis of negative capacitance. The concept was observed by Ershov in 1998, reinstated by Salahuddin and Datta 10 years later. In 2011, I. Khan et. Al presented evidence of ferroelectric negative capacitance in nano-scale hetero-structures. Negative capacitance refers to the power boost provided by capacitor made with a ferroelectric material paired with a dielectric (electrical insulator) [9]. Integration a ferroelectric material into current MOSFET architecture will reserve the

same field effect transistor operations, as well as compatibility with CMOS existing fabrication technology.

7.4 Subthreshold Slope Lower Than 60mV/ decade

In this section multiple approaches to lower sub-threshold slope are explored. A major research nowadays based on Ferroelectric material as source of negative capacitance. The idea is integrating a ferroelectric layer into MOSFET physical structure to lower its subthreshold slope. Salahuddin et al. show that a ferroelectric insulator of right thickness will amplify the gate voltage and leading to values of sub-threshold lower than 60mV/ decade. This idea was based on integrating a negative capacitance provided by the ferroelectric material with no change in the basic transistor operation. Their objective is to reduce the body factor η ($\frac{\partial V_g}{\partial \psi_s} < 1$) which different from other proposals that assumes that η cannot be changed and intending an alter transistor operation principals. Furthermore, [81] suggested a gate stack constitute of a metal-ferroelectric will provide a new mechanism to set-up the semiconductor surface potential ψ_s above the gate voltage. The capacitive voltage divider formed by C_{FE} will provide a new and stable operation region of the FET. This phenomenon will deliver a steeper sub-threshold slope ($S < 60$ mV/ decade). The concept of a metal-ferroelectric FET has not been established, and the impact of the integrating a negative capacitance on drain current is not demonstrated yet.

7.5 Non-Hysteretic Negative Capacitance FET

Non-Hysteretic negative capacitance was proposed to improve subthreshold swing. The research on [82] show that a 30 mV/ decade can be achieved. The structure is shown in Figure. 7.3, the bottom layer (N_{well}) is heavily doped p-type to determinate the depletion region and to cutoff the sub-threshold leakage path. The channel is a thin semiconductor on conductor (TSOC). A ferroelectric (FE) film is deposited over a metal/high-k dielectric stack.

Metal-Ferroelectric gate stack FET (considered as voltage amplifier) suggested in [9, 82]. The subthreshold swing is reduced by a factor β ($\beta = \Delta V_{MOS}/\Delta V_G$). β is derived from capacitive voltage divider model shown in Figure 7.3.

$$\Delta V_{MOS} = \Delta V_G * C_{FE}/(C_{FE} + C_{MOS}) \quad (7.5)$$

Where: C_{MOS} is the series combination of C_{ox} and C_{DEP} .

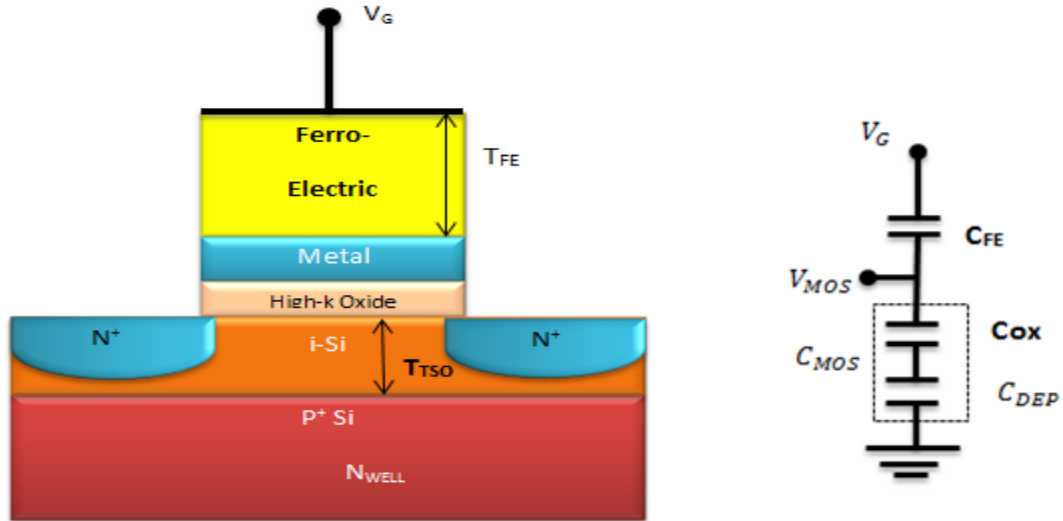


Figure 7.3: Cross section and the capacitance representation of NCFET [82].

$$\Delta V_{MOS} = \Delta V_G * |C_{FE}| / (|C_{FE}| - C_{MOS}) \quad (7.6)$$

To have a large β the denominator has to be very small:

$$|C_{FE}| - C_{MOS} \approx 0 \rightarrow |C_{FE}| \approx C_{MOS}$$

Conversely, C_{MOS} is not constant through the variation of V_G causing unstable device, and $|C_{FE}|$ required to be larger than C_{MOS} . To achieve that condition a thin semiconductor on conductor (TSOC) of thickness T_{TSOC} was incorporated to make C_{DEP} larger and insensitive to gate bias. Consequently a smaller sub-threshold swing can be succeeded.

7.6 Fe-FET with P(VDF-TrFE)/SiO₂ Gate Stack

Salvatore et al. research's demonstrate experimentally that a 13mV/ decade in Fe-FETs with 40nm P(VDF-TrFE)/ SiO₂ could be achieved at room temperature by integration a thin ferroelectric layer (negative capacitance) into a gate stack. The negative ferroelectric capacitance was integrated to lower the η -factor by providing voltage amplification. The added layer introduces a positive feedback that increases the polarization. A positive oxide capacitance was also included in series with the negative capacitance to solve the stability issue [84]. The charges presented by the positive feedback can described as:

$$Q = C_{gate}(V_G + \alpha_F Q) \quad (7.7)$$

The η -factor becomes:

$$\eta(V_G) = 1 - \frac{C_S}{C_{ins-eq}(V_G)} (\alpha_F C_{ins-eq}(V_G) - 1) \quad (7.8)$$

Where: $1/C_{ins-eq} = 1/C_{ox} + 1/C_{ins-eq}(V_G)$

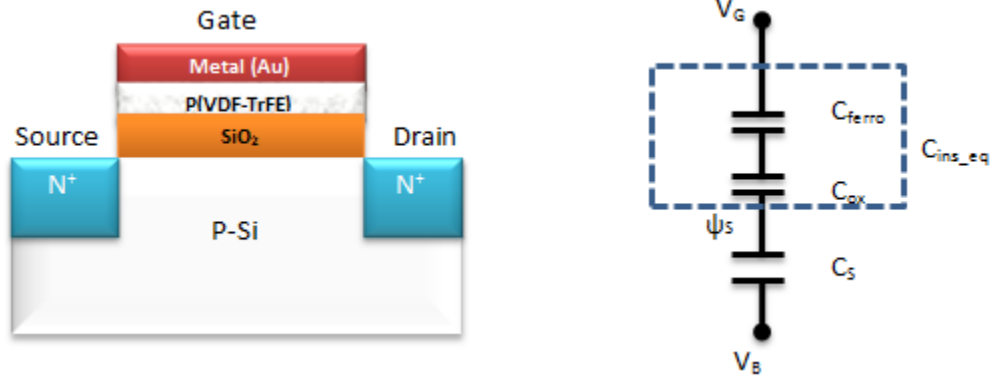


Figure 7.4: Fe-FET and equivalent capacitive divider [84].

For $\alpha_F C_{ins} > 1$ the η -factor is smaller than 1

The design of this experiment is placing a 40 nm P(VDF-TrFE) on top of 10nm SiO₂ gate stack.

Several suggestions were studied to incorporate ferroelectric negative capacitance into the MOSFET existing design. One of the suggestions is double ferroelectric gate MOSFET presented in Figure [7.5]. This idea is similar to the one discussed above except that a double gate lead a better channel control [83].

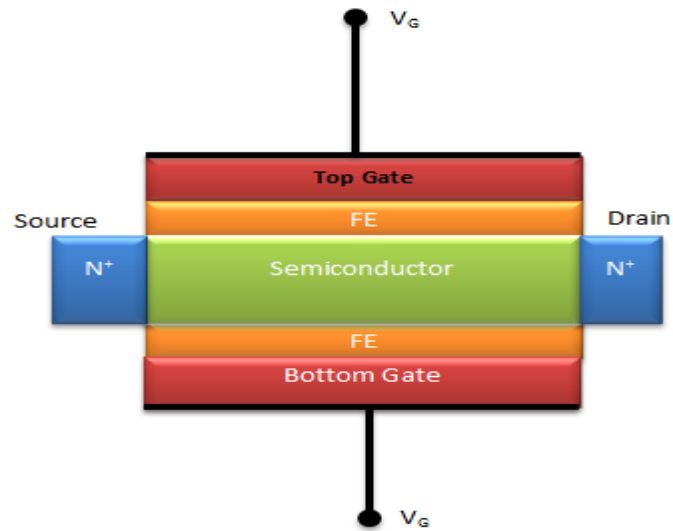


Figure 7.5: Cross-sectional view of a double-gate negative capacitance FET [83].

In [86] a different gate stack was introduced to break the 60 mV/decade limitation. This gate stack contains a Metal-Ferroelectric-Metal-Oxide-Semiconductor. This gate structure as mentioned earlier has a subthreshold swing down to 46mV/ decade. Few other proposals that show different gate stacks were proposed as well but not listed in this paper.

CHAPTER 8

AN ANALYTICAL MODEL TO APPROXIMATE THE SUBTHRESHOLD SWING FOR SOI-FINFET

In this chapter, an analytical model to approximate the subthreshold swing for a SOI-FinFET is introduced. This model only consider the structure of the SOI-FinFET, it doesn't count for the doping attenuation of the channel which is undoped or slightly doped. The model presents an approximation that is based on capacitive coupling model in subthreshold regime. This model also covers the effect of various design parameters on the subthreshold swing of SOI-FinFET. The subthreshold swing or inverse subthreshold slope (S) of a SOI-FinFET is approximated slightly above 60mV/decade.

8.1 Introduction

As needed to keep Silicon technology as the base technology while modernizing future devices; cost is an important factor. Tri-gate also known as FinFET was introduced due to its similarities to conventional MOSFET. The fin shape introduces a gate voltage that surrounds the channel from three sites presenting better control over short channel. The new structure also shows a higher I_{on}/I_{off} ratio as compared to conventional MOSFE. FinFETs present a better performance, lower leakage current, and fabrication compatibility with CMOS process [87]. Various device characteristics like drive current (I_{on}), subthreshold swing (S), and buried-insulator-induced barrier lowering (BIIBL) are depends on the high-aspect-ratation of the "fin" structure. This parameter presents a

significant challenge for process control and design flexibility [88, 89]. One of the FinFET design parameters is the fin width which requires being around half the channel length. The gate geometry plays a decisive key that controls the performance of the FinFETs. Simulations by [89] show that DIBL and subthreshold swing goes up when the fin aspect ratio ($AR = \text{the fin height} / \text{the effective fin width}$) goes below 1.5. They also show that the ratio controls the SCEs and the on-current of the device. The vertical architectures of the device make it very compact compared to Conventional MOSFET; other parameters are shown in Figure 8.1.

A theoretical analysis to calculate the subthreshold swing of SOI-FinFET is presented in this chapter. This approximation is based on coupling capacitance of the device; it doesn't count for the doping attenuation of the channel which is undoped or slightly doped. As we dialing with different structure a multiple coupling capacitance will be considered. The fin shape introduces a gate voltage that surrounds the channel from three sites. The gate will form coupling capacitance not just through the fin formed channel, but through the silicon dioxide on both sides of the fin (Figure 8.1).

8.2 SOI FinFET Subthreshold Swing

8.2.1 Model Approach

Studying of subthreshold swing is an important aspect to control the I_{ON} current and I_{OFF} current. Down-scaling at every technology node is disproving the subthreshold swing. This parameter is evaluated in mV/decades. η (body-factor) is the voltage divider

ratio of the fraction of V_{GS} appearing at the channel interface as ψ_S . For an ideal planar MOSFET device at room temperature η is close to 1. There are multiple ways to lower S , substrate thickness, buried oxide film thickness, and the fin's width are some of the parameter will be studied through this approximation.

Figure 8.1; illustrate various capacitances that are created between different materials. Capacitance is present every time two conductors placed closely separated by an insulating material. In the next section an approximated calculations of those capacitance is presented.

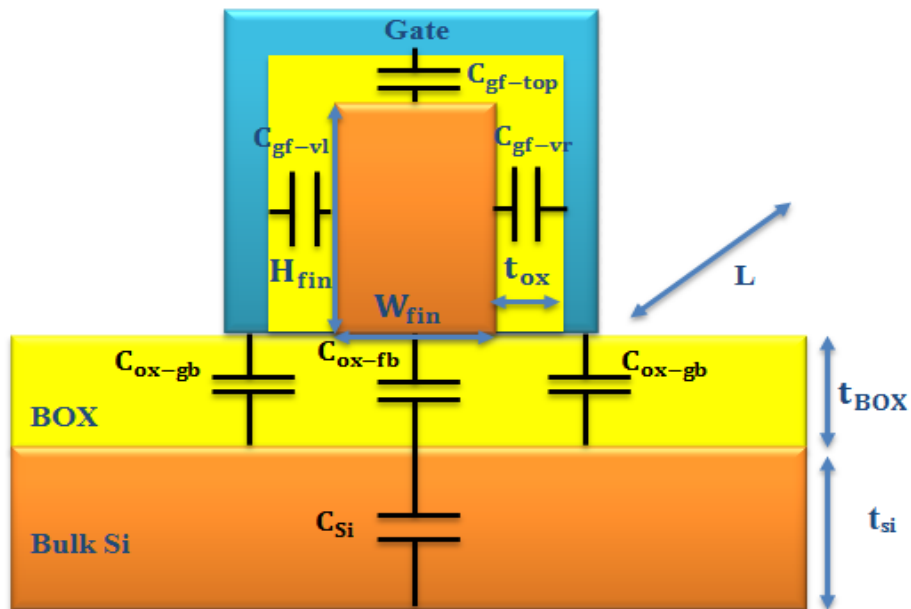


Figure 8.1: SOI FinFET Cross Section: H_{Si} represent the fin height, W_{Si} is the channel width, t_{BOX} is the buried oxide thickness, and L is the channel length, t_{ox} is the gate channel insulator thickness.

8.2.2 SOI FinFET Capacitance Calculations

Capacitance is present every time two conductors placed closely separated by an insulating material. Two square lines capacitance is based on their physical structure. Using Yang formula, an approximation of the capacitance of two square lines shown in Figure 8.2 is calculated. The total capacitance per unit length that includes fringing is [96, 97]:

$$C = \epsilon \frac{w}{h} \left[1 + \frac{2h}{\pi w} \ln \left(\frac{\pi w}{h} \right) + \frac{2h}{\pi w} \ln \left(1 + \frac{2t}{h} + 2 \sqrt{\frac{t}{h} + \frac{t^2}{h^2}} \right) \right] \quad (8.1)$$

Where: $2h$ is the distance between the two plates, w , and t are the length and the width of the top plate respectively.

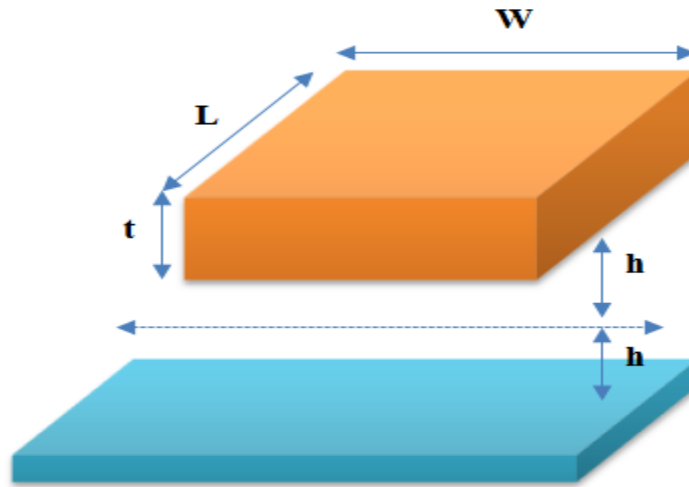


Figure 8.2: Two conducting plate

From Figure 8.2, the total gate-channel capacitance is:

$$C_{gf} = C_{gf-top} + C_{gf-vl} + C_{gf-vr} \quad (8.2)$$

Where: C_{gf-top} , C_{gf-vl} , and C_{gf-vr} represent the capacitances of top plate (capacitance created between the top gate and the channel), vertical left, and vertical right capacitance created between the vertical gates and the channel (see Figure 8.2 for details). For uniform dispersed gate-shape both capacitance C_{gf-vl} and C_{gf-vr} are assumed to be equal.

Using Yang formula, an approximation of the capacitance formed by the bridge-shape gate and the channel can be obtainable [96, 97].

$$C_{gf-vl} = \epsilon_{ox} \frac{2H_{fin}}{t_{ox}} L \left[1 + \frac{t_{ox}}{\pi H_{fin}} \ln \left(\frac{2\pi H_{fin}}{t_{ox}} \right) + \frac{t_{ox}}{\pi H_{fin}} \ln \left(1 + \frac{2W_{fin}}{t_{ox}} + 2 \sqrt{\frac{2W_{fin}}{t_{ox}} + \frac{4W_{fin}^2}{t_{ox}^2}} \right) \right] \quad (8.3)$$

Similarly:

C_{ox-top} and C_{ox-fb} are the front and back oxide capacitances

$$C_{gf-top} = \epsilon_{ox} \frac{2W_{fin}}{t_{ox}} L \left[1 + \frac{t_{ox}}{\pi W_{fin}} \ln \left(\frac{2\pi W_{fin}}{t_{ox}} \right) + \frac{t_{ox}}{\pi W_{fin}} \ln \left(1 + \frac{4(H_{fin} - t_{ox})}{t_{ox}} + 2 \sqrt{\frac{2H_{fin}}{t_{ox}} + \frac{4H_{fin}^2}{t_{ox}^2}} \right) \right] \quad (8.4)$$

$$C_{ox-fb} = \epsilon_{ox} \frac{2W_{fin}}{t_{BOX}} L \left[1 + \frac{t_{BOX}}{\pi W_{Si}} \ln \left(\frac{2\pi W_{fin}}{t_{BOX}} \right) + \frac{t_{BOX}}{\pi W_{fin}} \ln \left(1 + \frac{4(H_{fin} - t_{ox})}{t_{BOX}} + 2 \sqrt{\frac{2H_{fin}}{t_{BOX}} + \frac{4H_{fin}^2}{t_{BOX}^2}} \right) \right] \quad (8.5)$$

8.2.3 SOI FinFET Approached Capacitive Network and Subthreshold Swing Calculation.

Considering the coupling capacitance between the gate voltage and the bulk to estimate the subthreshold swing ‘S’. Figure 8.1 shows the capacitance involved in this approximation. For a short channel modeling, analytical solution used voltage-doping

transformation (VDT) is considered [94]. This estimation also considered linearly varying potential (LVP) approximation to obtain the swing voltage [93].

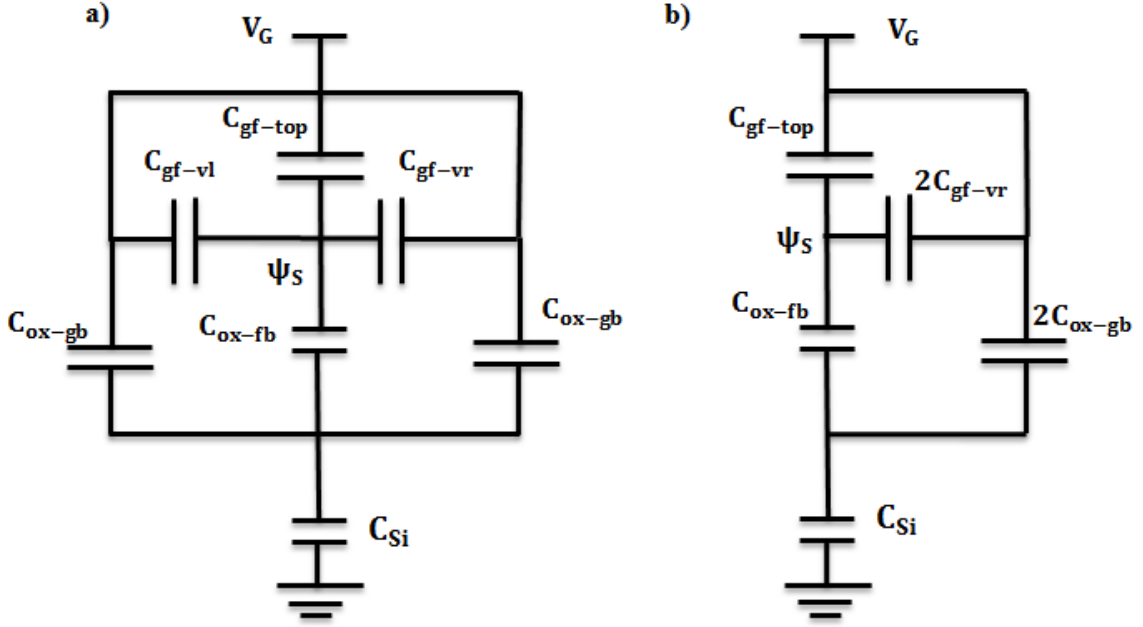


Figure 8.3: SOI FinFET approached capacitive network a) Equivalent capacitive model of SOI FinFET b) Simplification of Equivalent capacitive model of SOI FinFET

The Figure 8.3.a illustrates the capacitive network presentation of SOI-FinFET, where the Figure 8.3.b shows a capacitive simplification of the capacitive network.

The body-factor η (please see the Appendix for detail calculations) can be evaluated as:

$$\eta = 1 + \frac{C_{ox-fb} \times C_{Si}}{(C_{gf-top} + 2 \times C_{gf-vr}) \times (C_{ox-fb} + C_{Si} + 2C_{ox-gb}) + 2 \times C_{ox-fb} \times C_{ox-gb}} \quad (8.6)$$

$$\eta = 1 + \frac{C_{ox-fb} \times C_{Si}}{C_{gf} \times (C_{ox} + C_{Si}) + C_{ox-fb} (C_{ox} - C_{ox-fb})} \quad (8.7)$$

Where: C_{gf} is the total gate-channel capacitance, C_{ox-fb} is the capacitance formed between the conducting channel and the silicon substrate, C_{ox} represent the total capacitance

created between the working area of the device and the silicon substrate, C_{Si} is the silicon film capacitance ($= \frac{\epsilon_{Si}}{t_{Si}}$, ϵ_{Si} being the silicon permittivity and t_{Si} the silicon film thickness), and C_{BOX} is the oxide film capacitance ($= \frac{\epsilon_{ox}}{t_{BOX}}$, ϵ_{ox} being the oxide permittivity and t_{BOX} the oxide film thickness). SOI FinFET offers near-ideal coupling, which gives a value of η close to unity. However, subthreshold swing depends on several parameters: BOX thickness, channel dimensions (fin height and width), channel length, and the silicon wafer thickness.

8.3 Simulation, Discussion, and Considerations

Through this study a complete analysis of multiple factors that can be evaluated to improve the subthreshold swing. The thickness of the buried oxide presents a tradeoff between thermal effect and the electrical properties of the device. A thinner BOX is required for better heat dissipation, and prevents electric field penetration through the BOX. Thinner BOX lowers the depletion layer that reduces the parasitic capacitance and lead to speed improvement and reduction of power consumption. However, a thinner BOX will increase the parasitic coupling capacitance with substrate [95].

The Figure 8.4 presents the relation between the subthreshold swing versus substrate thickness and buried oxide film thickness.

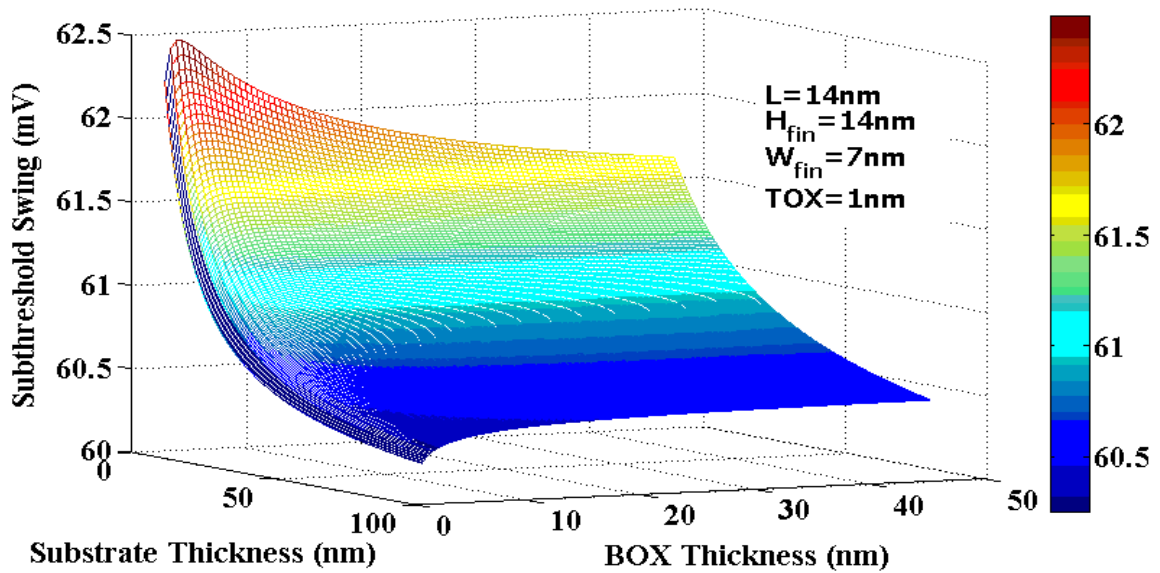


Figure 8.4: Plot of subthreshold swing versus substrate thickness and buried oxide film thickness.

This figure is a demonstration of the dependency of subthreshold swing on the ratio ($T_{\text{Si}}/T_{\text{BOX}}$). When that ratio is larger than 1, S is smaller. Therefore SOI-FinFET on a thin BOX and thicker substrate gives a better subthreshold swing.

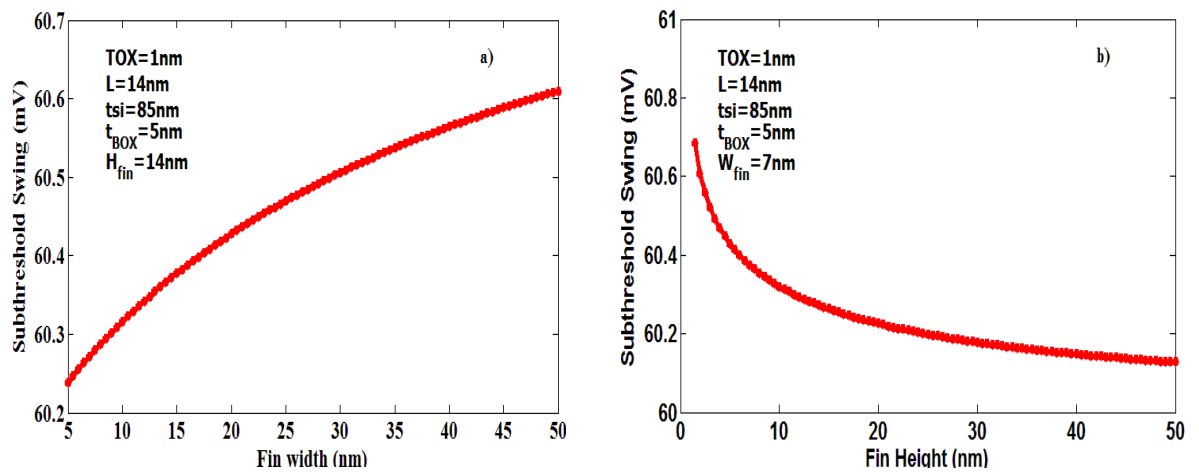


Figure 8.5: a) Subthreshold swing versus the fin width b) Subthreshold swing versus fin height.

The results demonstrate that a small Fin width and a large fin height are required to achieve a better subthreshold swing.

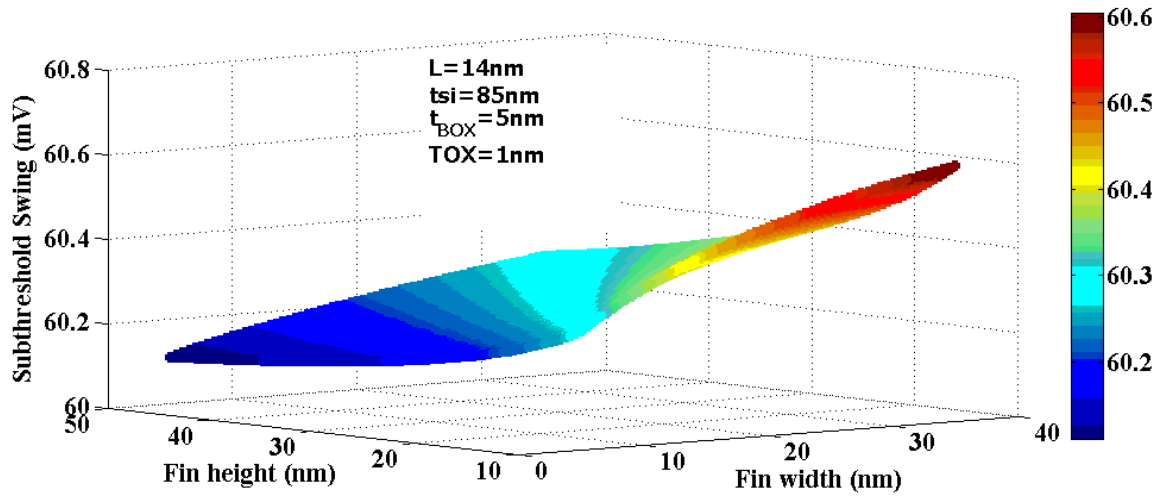


Figure 8.6: Subthreshold swing for various values for both the height and the width of the fin. This figure illustrate that the ratio fin height over fin width must be very large than 1 to achieve a subthreshold close to 60 mV/decade.

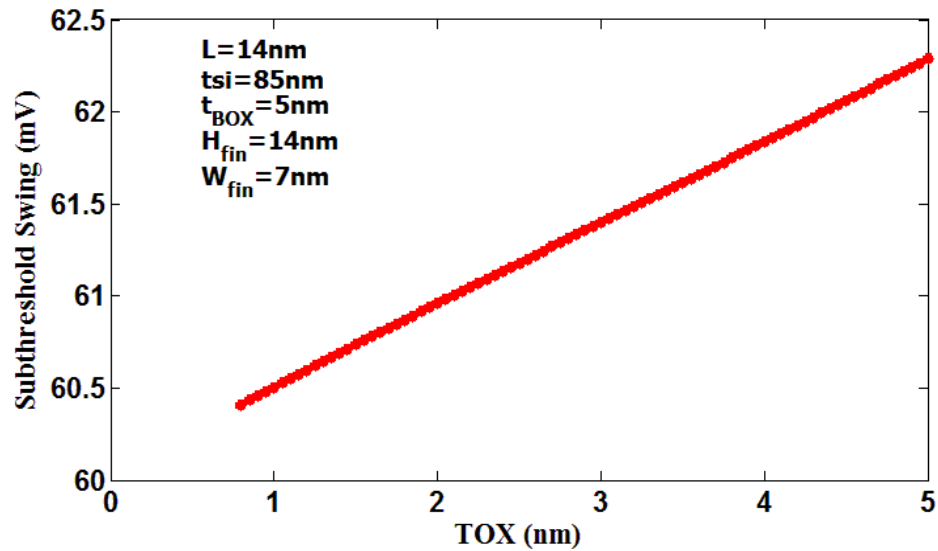


Figure 8.7: Subthreshold swing versus oxide thickness: By lowering the gate dioxide thickens a subthreshold swing closer to 60 mV/ decade can be obtained.

8.4 Conclusion

In this chapter, we have studied the subthreshold swing of SOI FinFET device. We proposed an analytical model to approximate the subthreshold swing based on capacitive coupling model in subthreshold regime. We have also demonstrated the impact of the wafer thickness, the buried oxide film thickness (BOX), the width and the height of fin, and the gate oxide thickness (TOX) on the subthreshold swing. This approximation we have shown that the ratio t_{Si}/t_{BOX} has a significant effect on the swing. SOI FinFET on a thin BOX and thicker substrate gives a better subthreshold swing. A fin width much smaller than the fin height and small TOX is required to accomplish a subthreshold swing slightly close to 60mV/decade.

CHAPTER 9

SILICON-ON-FERROELECTRIC INSULATOR

FIELD EFFECT TRANSISTOR (SOF-FET)

This chapter presents the concept of a new field effect transistor based on ferroelectric- insulator. The proposed design is named *Silicon-on-Ferroelectric Insulator field effect transistor (SOF-FET)*. The design combines the concepts of negative capacitance in ferroelectric material and silicon-on-insulator (SOI) device. The design proposes that by burying a layer ferroelectric insulator inside bulk silicon substrate an effective negative capacitance (NC) can be achieved. The NC effect can provide internal signal boosting. It is demonstrated that by carefully selecting thickness of the ferroelectric film inside the device the subthreshold swing and the threshold voltage can be lowered. Lower subthreshold swing is a prime requirement for ultra-low-power design.

9.1 Introduction

The demand for longer battery life in portable and wireless applications that demand high-speed computation and complex functionality with low power consumption makes ultra-low-power design one of the most prominent areas in VLSI [96]. As Moore's Law is destructively followed in the last few decades, CMOS technology is approaching its physical and material limits. Scientists and engineers are looking for innovative techniques and new technologies at the architecture, circuit and device levels. Design of

ultra-low-power integrated circuits in nano-scale domain requires device operation in subthreshold region, where the energy consumption will be reduced exponentially with the reduction of supply voltage (in super-threshold region the dependency is quadratic). It is possible to ensure ultra-low-power operation if device construction and geometry can be tuned to operate in the subthreshold region of the conventional devices [97, 98]. This requires new devices (beyond the capabilities of conventional MOSFET) suitable for extremely low power operation [99]. This paper proposes a new device concept to increase the efficiency of subthreshold operation. The objective is to lower subthreshold swing (S) by utilizing negative capacitance effect. Conventional bulk silicon MOSFET has a theoretical minimum of $S_{\min} = 60\text{mV/decade}$, whereas the practical values are much higher. This fundamental limit of S is the primary bottleneck of subthreshold circuit design using bulk silicon MOSFET. Technological breakthrough at the device level is required to cross this subthreshold swing limit.

9.2 The Concept of Negative Capacitance

Even with the most ideal scenario the limit for the conventional MOSFET is $S = 60\text{ mV/decade}$ due to non-scaling of the thermal voltage kT/q . One way to achieve a lower value of S is to develop a negative capacitance (NC) effect in the device structure. The NC effect in a semiconductor device was first observed in [117]. The NC effect implies that the voltage of a capacitor decreases as charge is added. Considering the coupling capacitance between the gate voltage and the bulk as shown in Figure 9.1, the

body factor can be defined as $\eta = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_{Body}}{C_{INS}}$. Here ψ_s is the surface potential, C_{Body} is the semiconductor capacitance and C_{INS} is the gate insulator capacitance. For $0 < \eta < 1$ we must have $\frac{C_{Body}}{C_{INS}} < 0$ or $C_{Body} < 0$, which means a negative capacitance is needed to achieve a sub-threshold swing lower than $S < 60\text{mV/decade}$.

In [9, 86] it is suggested that by replacing the standard insulator (SiO_2) of MOSFET with a ferroelectric insulator of the right thickness a negative capacitance can be achieved that arises from the hysteresis of internal positive feedback of ferroelectric capacitor. In [9], proof of the hypothesis of negative capacitance effect in a nanoscale ferroelectric-dielectric heterostructure is provided. Negative capacitance refers to the power boost provided by the capacitor made with a ferroelectric material paired with a dielectric (electrical insulator) [9]. Integration of ferroelectric materials into current MOSFET architecture will preserve the same field effect transistor operations, as well as compatibility with existing CMOS technology.

9.3 Proposed Silicon-On-Ferroelectric Insulator (SOF) Field Effect Transistor

This chapter presents a concept of a new transistor design using ferroelectric insulator embedded inside silicon substrate. The construction of the new device is similar to silicon-on-insulator (SOI) device. We propose to replace the buried silicon dioxide (SiO_2) insulator layer in SOI device with a layer of ferroelectric insulator and a layer of thin film buffer insulator. We formally name this new device *Silicon-on-Ferroelectric Insulator field effect transistor (SOF-FET)*. The proposed *SOF-FET* can have two

variants – fully depleted and partially depleted *SOF-FET*. Figure 9.1 presents the concept and the physical construction of the proposed fully depleted *SOF-FET*.

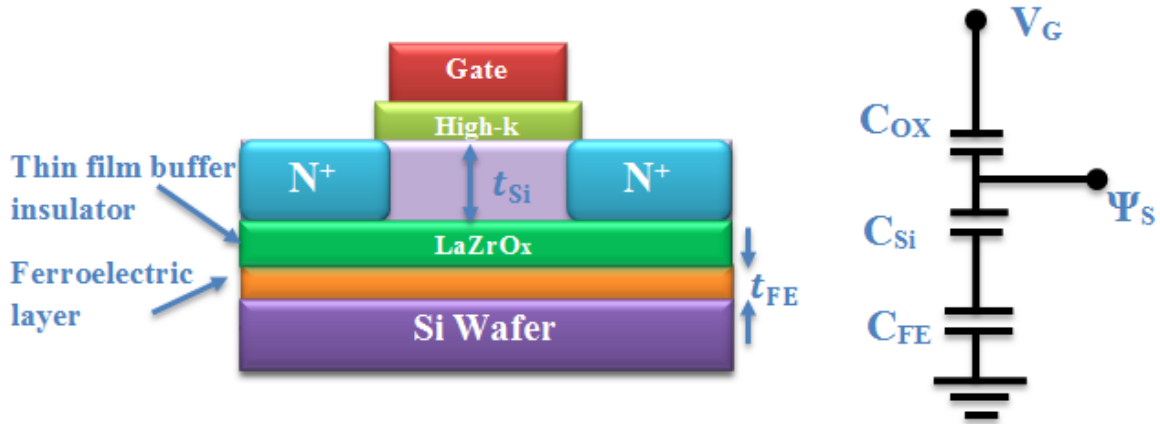


Figure 9.1: Proposed *SOF-FET* and its equivalent capacitive divider.

The idea here is to use the ferroelectricity decencies as pre-existing boost for the device. It takes advantage of the charges that trapped into the ferroelectric film that can be collected after the application of a smaller gate voltage. Hence a channel between the drain and the source can be developed by low gate voltage. This proposed design takes advantage of ferroelectric negative capacitance and SOI technology. The idea is to place a thin layer of ferroelectric material on top of silicon substrate. The ferroelectric material making direct contact with the silicon creates an intermediate silicate layer. The effect of charge between silicon and ferroelectric film can be minimized by inserting a buffer insulator layer. This layer is often inserted between the ferroelectric film and silicon substrate. These insulating materials are required to hold a high dielectric constant, high thermal stability, low leakage current, and good interface property with silicon substrates.

Materials such as HfO_2 , Y_2O_3 , and DyScO_3 , have been considered for nonvolatile memory design structures [101]. There are multiple researches to merge silicon and ferroelectric materials. $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$ (piezoelectric) family considered good candidate for various devices. PZT is a perovskite-type ferroelectric material [8]. A simple and effective way to achieve better temperature stability is integrating a fix capacitor with good temperature stability in series with temperature sensitive capacitor [101].

The threshold voltage of a MOSFET is affected by the voltage difference between the source and the bulk. This voltage changes the width of the depletion layer leading to changes of the charges in this region. Integration of a ferroelectric negative capacitance as thin films in Si-bulk MOSFET shrinks the depletion layer. The main idea here is to lower the depletion layer under source and the drain. Hence, the depletion capacitance decreases ($C=\epsilon A/d$). Integrating a negative capacitance of the right thickness will also have a major impact on the capacitance coupling of the device. By combining both ideas a sharper sub-threshold voltage can be accomplished.

9.4 *SOF-FET* Device Physics and Mode of Operation

The mode of operation of the *SOF-FET* is presented here. By applying a positive gate voltage less than threshold voltage the electrons start their attraction toward the gate insulator. Correspondingly, the ferroelectric film helps developing the channel at low voltage. The polarity of the upper plate of the negative capacitance repulses the electron toward construction the channel. The electrons needs less energy to move from the valance band to conduction band. Reasonably, using a bottom gate requires a voltage to

be connected to it. Nevertheless, using a ferroelectric layer ensure the same concept of double gate devices. The ferroelectric film provides a bias supply to the device that could be considered as bottom gate. Figure 9.2 displays the concept of switching ON. Similarly switching OFF requires disconnecting the gate voltage consequently, the surface potential (channel voltage) will be converge to null. Therefore, the negative capacitance will be disconnected and the device completely OFF.

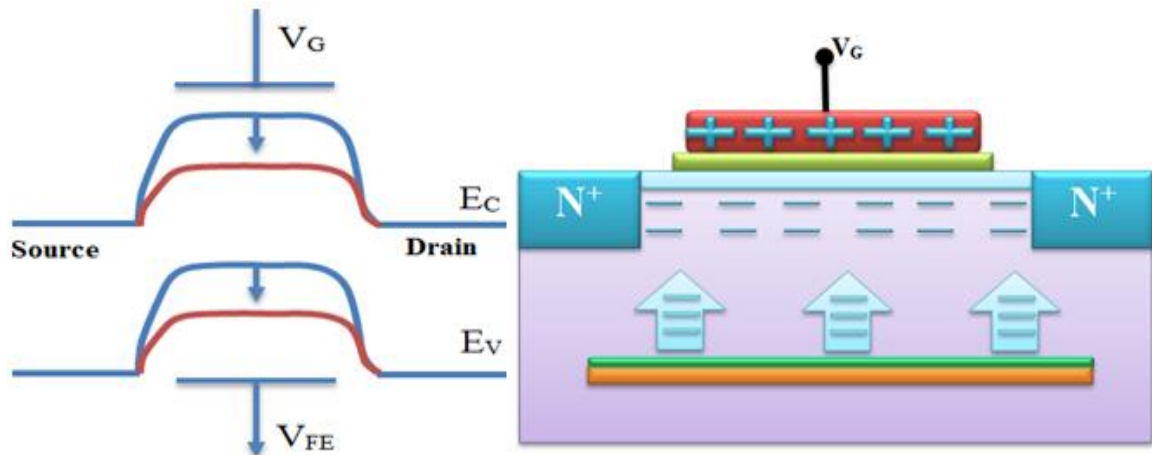


Figure 9.2: *SOF-FET* band diagram for $0 < V_G < V_{TH}$ and $V_{FE} > 0$ Gate voltage attracted electrons and pushes holes away similarly the ferroelectric film repulses electrons to the top of the silicon therefore a n type channel is formed promptly. *SOF-FET* transistor begins to conduct.

9.5 Subthreshold Behavior of Proposed SOF-FET

9.5.1 Subthreshold Swing of SOF-FET

The concept of negative capacitance extracted from ferroelectric materials has been over looked in the last few years. The hysteresis properties made it possible for

ferroelectric material to be considered in various IC designs. The charge on a ferroelectric capacitor does not go back to zero at 0V unlike linear and paraelectric capacitors. Some of the charge inside the capacitor will be tripped (cannot come out), and yet it still has zero volts on it. The reason is that the ferroelectric material between the plates of the capacitor has a naturally occurring built-in electric field. That electric field pulls in from the circuit just the right amount of excess charge of the opposite polarity to cancel itself at the surface of each plate. Therefore, even though the excess charge on each plate repels itself, it is held in place by the electric field emanating from the ferroelectric material [103].

From the structure of Figure 9.1 using the analysis of chapter 4 and 8 we can calculate the body-factor of the *SOF-FET* as shown in (9.1). Where κ represent the ratio of $C_{\text{Body}} / C_{\text{ox}}$ as displayed in (9.2), C_{Body} represents the series association of C_{Si} and C_{Fe} , and C_{FE} represents the negative capacitance extracted by integrating a thin ferroelectric layer.

$$\eta = 1 + \kappa \quad (9.1)$$

$$\kappa = \frac{C_{\text{Body}}}{C_{\text{ox}}} = \frac{C_{\text{Si}}C_{\text{Fe}}}{C_{\text{ox}}(C_{\text{Si}} + C_{\text{Fe}})} = -\frac{C_{\text{Si}}|C_{\text{Fe}}|}{C_{\text{ox}}(C_{\text{Si}} - |C_{\text{Fe}}|)} \quad (9.2)$$

To have body-factor less than one ($\eta < 1$) κ must be negative quantity, and for stability reason κ must satisfy the condition in (9.3):

$$-1 < -\frac{C_{\text{Si}}|C_{\text{Fe}}|}{C_{\text{ox}}(C_{\text{Si}} - |C_{\text{Fe}}|)} < 0 \quad (9.3)$$

For $C_{FE} < 0$ and $C_{Si} > |C_{FE}|$ the portion $\frac{C_{Si}|C_{FE}|}{C_{ox}(C_{Si}-|C_{FE}|)} < 1$ attenuate to be less than zero leading to a body factor (η) ranged between 0 and 1. The second stability condition can be also derived from (9.3) and it's shown in (9.4) where we have:

$$\frac{C_{Si}}{C_{ox}} < \frac{C_{Si} - |C_{FE}|}{|C_{FE}|} = \frac{C_{Si}}{|C_{FE}|} - 1 \rightarrow \frac{C_{Si}}{C_{ox}} > 0 \quad (9.4)$$

This condition of $0 < \eta < 1$ yields to a sharper subthreshold slope. Since the device operation is similar to that of the MOSFET, this approach will lead to a subthreshold swing (S) much lower than 60mV/decade. S can be written as:

$$S = 2.3 \frac{kT}{q} \left(1 + \frac{C_{Body}}{C_{ox}} \right) = 2.3 \frac{kT}{q} \left(1 - \frac{C_{Si}|C_{FE}|}{C_{ox}(C_{Si} - |C_{FE}|)} \right) \quad (9.5)$$

This design requires a careful planning, where the thickness and the placement of ferroelectric layer will control the subthreshold swing. At the threshold voltage the device is turned ON (when the gate voltage is equal to the threshold voltage), the depletion layer capacitance per unit area reaches a minimum C_{Dmin} and is given by: $C_{Dmin} = \frac{\epsilon_{Si}}{W_{Dmax}}$ (ϵ_{Si} is the permittivity of Silicon). The depletion layer thickness follows The gate oxide capacitance is given by: $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, which is inversely proportional to oxide thickness (here ϵ_{ox} is the permittivity of the oxide), and $C_{FE} = \epsilon_{FE}/t_{FE}$ is the ferroelectric material capacitance per unit area (t_{FE} is the thickness of the ferroelectric film, ϵ_{FE} is the permittivity of ferroelectric material). The subthreshold swing of the proposed **SOF-FET** depends of several parameters the most significant is the thickness of the ferroelectric film, the depleted silicon, and the gate oxide. The developed model (9.5) is based on the

approximation that the impact of the unipolar junctions between the top plate of the negative capacitance and the diffusion areas (drain and source) can be ignored due to their minor effect on overall device operation.

9.5.2 Threshold Voltage of SOF-FET

The capacitive model of Figure 9.1 can be used to derive a model for the threshold voltage of the proposed **SOF-FET**. Using the structure of Figure 9.1 we can derive a first order approximation of V_{TH} as illustrated in (9.6)-(9.9). From the derived model (9.9), it is observed that the threshold voltage of the proposed **SOF-FET** depends on the thickness of the ferroelectric material.

$$\psi_S = \frac{C_{ox}}{C_{ox} + C_{Body}} (V_G - V_{FB}) \quad (9.6)$$

$$V_G = \psi_S \left(1 + \frac{C_{Body}}{C_{ox}} \right) + V_{FB} \quad (9.7)$$

$$V_{TH} = V_G |_{\psi_S = 2\psi_b} \quad (9.8)$$

$$V_{TH} = 2 \frac{KT}{q} \ln(N_A/n_i) \left(1 + \frac{C_{Body}}{C_{ox}} \right) + V_{FB} \quad (9.9)$$

Here $\psi_b = \frac{KT}{q} \ln(N_A/n_i)$ is the difference between Fermi and intrinsic levels. When $V_{GS} > V_{TH}$ (n-type FET), the semiconductor/oxide interface is inverted (inversion layer is formed). Here, $V_{FB} = \psi_{MS} - Q_{SS}/C_{ox}$ is the flat band voltage, Q_{SS} is the surface state charge of the channel, $\psi_{MS} = \psi_{Si} - \psi_F = \frac{-E_g}{2} - \psi_F$ is the work function difference

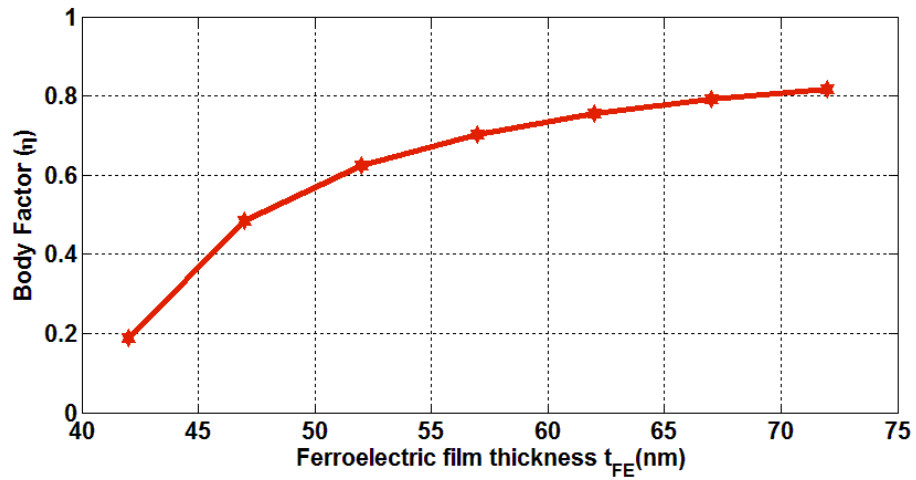
between the gate and the channel, $\psi_F = \frac{kT}{q} \ln(N_A/n_i)$ is the Fermi potential, and E_g is the silicon energy band gap.

9.6 Impacts of Ferroelectric Film Thickness

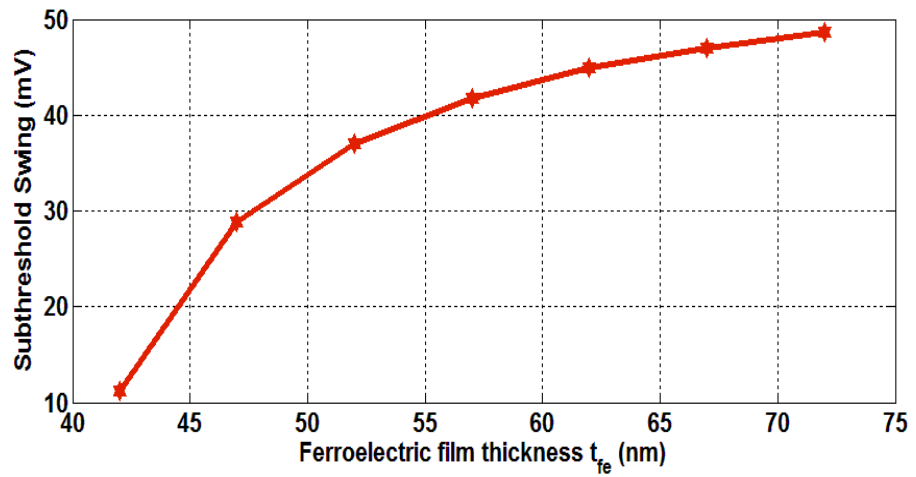
From the derived models (9.5) and (9.9) it can be observed that there are several factors that can be adjusted to lower the threshold voltage and the subthreshold swing. Equation (9.5) indicates that depressing the depleted silicon and increasing the oxide capacitance are two possibilities. However, the thickness of the ferroelectric material has to be selected carefully to maintain a stable device. The depleted thin silicon film (t_{Si}) and the ferroelectric film thickness (t_{FE}) are two parameters that can be adjusted to manage the device stability. Figure 9.3 present the dependency of the body-factor, subthreshold, and threshold voltage.

Normally, the applied gate voltage inverts the doping of silicon directly under the gate to form a channel between the source and drain. The trapped charges in ferroelectric material will help forming the channel at lower voltage. Smaller thickness of ferroelectric film gives higher negative capacitance ($C_{FE} = \epsilon_{FE}/t_{FE}$) leading to higher trapped charge in the film. This helps the creation of the channel at a lower V_T . With thicker ferroelectric film the device will behave like regular SOI device, where the ferroelectric material and buffer insulator will serve as low conducting material. This will increase both V_T and S . When the device is turning OFF the ferroelectric capacitance starts collecting charge from the channel. This quick evacuation improves the device turn OFF speed. This

trapped charge in the ferroelectric capacitance will again aid formation of the channel when the device switches back to on-state.



a)



b)

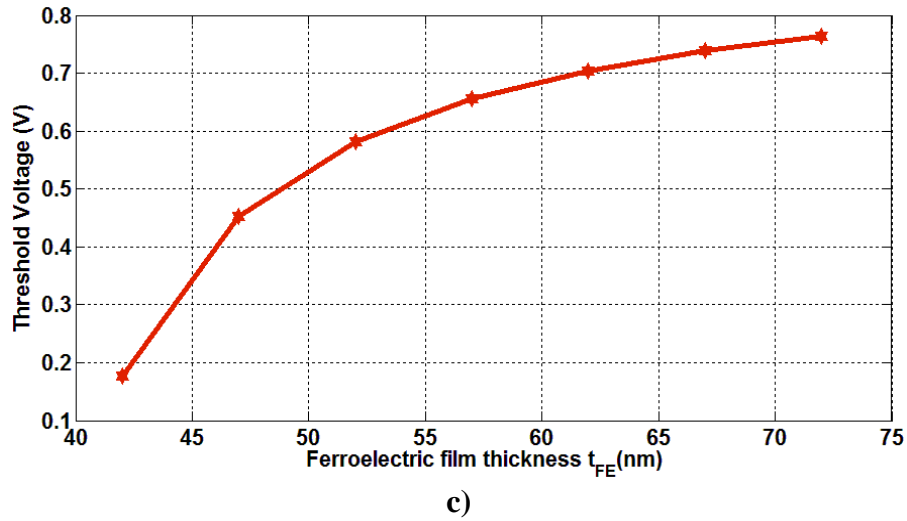


Figure 9.3: Plot of the a) body-factor, subthreshold swing, and threshold voltage for a t_{FE} vary from 40nm to 75nm

Normally, the applied gate voltage inverts the doping of silicon directly under the gate to form a channel between the source and drain. The trapped charges in ferroelectric material will help forming the channel at lower voltage. Smaller thickness of ferroelectric film gives higher negative capacitance ($C_{FE} = \epsilon_{FE}/t_{FE}$) leading to higher trapped charge in the film. This helps the creation of the channel at a lower V_T . With thicker ferroelectric film the device will behave like regular SOI device, where the ferroelectric material will serve as the buffer insulator or a low conducting material. This will increase both V_T and S . When the device is turning OFF the ferroelectric capacitance starts collecting charge from the channel. This quick evacuation improves the device turn OFF speed. This trapped charge in the ferroelectric capacitance will again aid formation of the channel when the device switches back to ON state.

9.7 Impacts of Channel Doping

From (9.5) and (9.9), it can be deduced that the subthreshold swing and the subthreshold voltage of the proposed device are dependent on the doping profile of the channel. The thickness of the depletion layer also depends of the doping level. A lower doping will cause a thicker depletion layer, therefore a higher depletion capacitance $\left(W_{dep} \propto \sqrt{\frac{1}{N_A}} \ \& \ (C_{dep} \propto \sqrt{N_A})\right)$. Hence, the magnitude of the body factor will decrease resulting in increase of subthreshold swing, because in the proposed device we have to make sure that the body-factor remains between 0 and 1 by ensuring the following conditions: $-1 < \kappa = -\frac{C_{Si}|C_{Fe}|}{C_{ox}(C_{Si}-|C_{Fe}|)} < 0$. A numerical simulation of various doping profile is presented in Figure 9.4 to observe its effect on the value of S. It can be seen that the device will have a better operation with low doping profile. This is a significant advantage compared to the conventional and other FETs. Ability to maintain lower doping profile in the proposed device will limit the effect of non-uniform lateral doping of short channel devices, therefore will decrease the off-state current. Low doping also removes excessive random dopant fluctuations (RDF) and eliminates the issue of significant device-to-device threshold voltage variations.

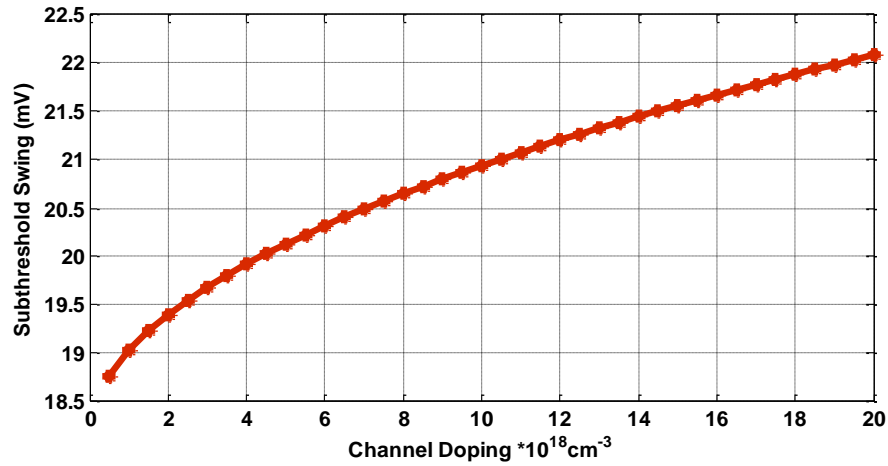
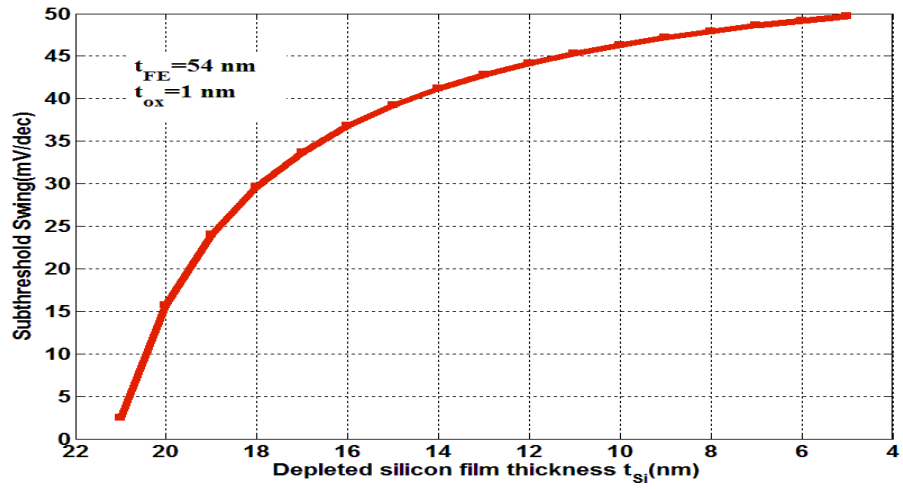


Figure 9.4: Numerical simulation of the subthreshold swing and its dependencies on the channel doping. A doping between $5 \times 10^{17} \text{ cm}^{-3}$ and $2 \times 10^{19} \text{ cm}^{-3}$ was considered for this purpose.

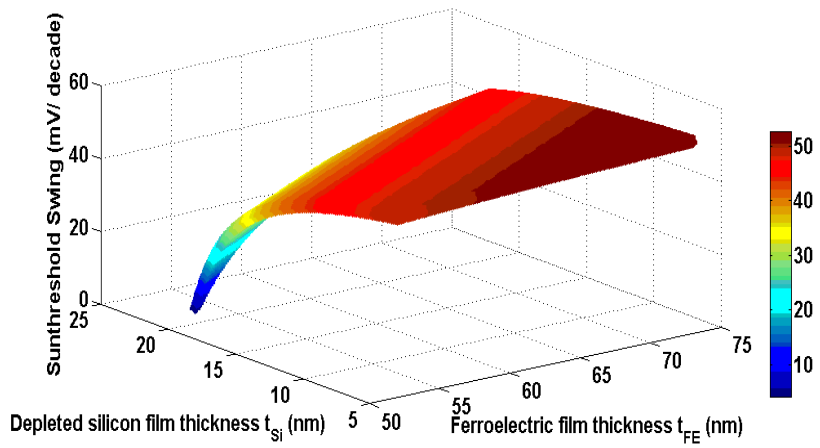
9.8 Impacts of Various Design Elements

From (9.5) and (9.9), it can be deduced that the subthreshold swing and the subthreshold voltage of the proposed device are dependent on the gate oxide thickness, the ferroelectric film thickness and the depleted thin silicon film. These elements regulate the promptness of channel formation, therefore the sharpness of the subthreshold slop.

If the thicknesses of the elements mentioned before are selected cautiously, the magnitude of the body-factor will decrease. In the proposed device we have to make sure that the body-factor remains between 0 and 1 by ensuring the following conditions: - $1 < \kappa < 0$ and other stability condition and analytics that listed in various section of this chapter. A numerical simulation of these elements and their impact on the subthreshold swing is presented in Figure 9.5.



(a)



(b)

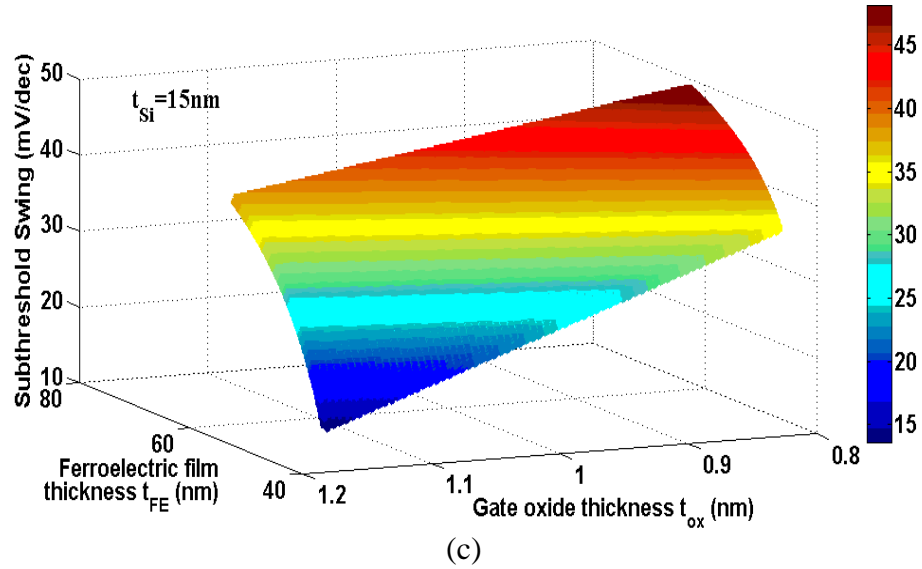


Figure 9.5: Plot of S a) @ various depleted silicon film thickness t_{Si} b) @ various ratio t_{Si}/t_{FE} c) @ various ratio t_{ox}/t_{FE}

Figure 9.5.a demonstrates that at $t_{FE} = 54nm$ a large thickness of the depleted silicon film improves S . This improvement is limited by the first stability condition presented in (9.4). It can be seen from Figure 9.5.b that the ratio $\frac{t_{Si}}{t_{FE}}$ has to be greater than 2 for a lower S . In this case a subthreshold swing less than 5mV/decade can obtain. This is a significant advantage compared to the conventional and other emerging technologies FETs.

9.9 Impact of Gate Insulator Property

The impacts of gate insulator property on the behavior of the proposed SOF-FET can be noticed from the (9.5) and (9.9). It can be seen that the ferroelectric capacitance ($C_{FE} = \epsilon_{FE}/t_{FE}$) and the gate oxide capacitance (ϵ_{ox}/t_{ox}) adjusted to realize a practical body-factor for a stable device. Many promising high-k dielectric materials and various

ferroelectric materials have been investigated recently for application in DRAM. Values and other considerations are presented in [10, 102].

Multiple dielectrics can be numerically simulated in order to get an idea about the gate dioxide suitable for a low body-factor. Using high-k gate oxide requires a thinner ferroelectric film (24 nm to 74 nm) to keep the body factor in a realistic range. However, SiO₂ can also be employed. In this case a thicker ferroelectric film is needed to accomplish a practical body factor, hence a low subthreshold swing. Furthermore, technology scaling, fabrication process and variation of ferroelectric materials may restrict the use of certain gate oxide materials.

CHAPTER 10

CURRENT-VOLTAGE CHARACTERISTICS OF SOF-FET

10.1 Subthreshold Region

To understand the behavior and performance of the proposed *SOF-FET* we investigated the (I-V) characteristics of the device both in the subthreshold regime and saturation regime. For this we have utilized the model used for SOI device, but the parameters are derived from the proposed device structure. An accurate model for subthreshold operation of SOI-MOSFET is presented in [104, 105]. The current at that region is defined as in (10.1).

$$I_{\text{Sub}} = 2\mu C_{\text{ox}} \frac{W}{L} \left(\frac{KT}{q}\right)^2 |\eta - 1| \exp\left(\frac{V_{\text{GS}} - V_{\text{TH}}}{\eta KT/q}\right) \left[1 - \exp\left(-\frac{V_{\text{DS}}}{KT/q}\right)\right] \quad (10.1)$$

Where W and L are the dimensions of the device, V_{TH} is the threshold voltage, and η is the body-factor. Correspondingly, the body-factor calculated to be $\eta=0.33$ and subthreshold swing is 19.9 mV/decade. The subthreshold region (I-V) characteristic ($I_{\text{DS}}-V_{\text{GS}}$) of the *SOF-FET* device is as shown in Figure 10.1. For a threshold voltage of 0.2V and body-factor $\eta=0.33$, off-current ($V_{\text{GS}}=0\text{V}$) is about 954nA/ μm (note that the leakage current is depends on how fast the ferroelectric capacitor can help evacuate the carriers of the channel).

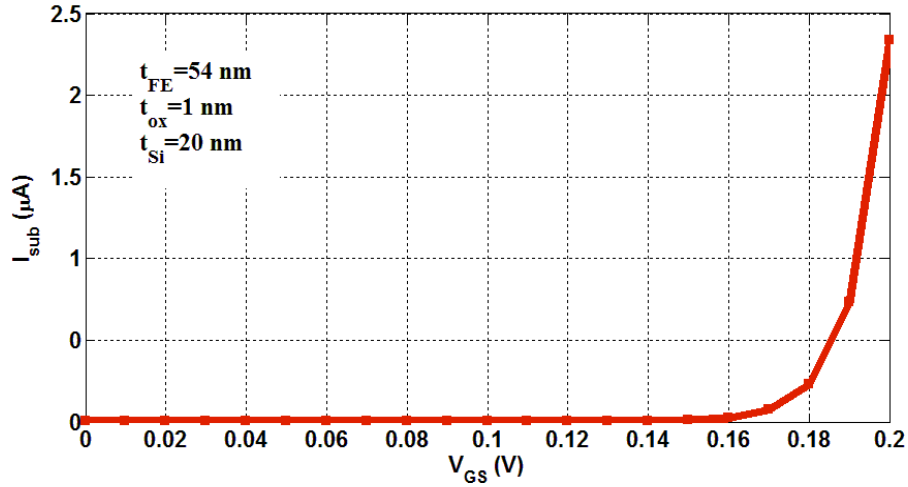


Figure 10.1: The transfer characteristic of the *SOF-ET* at subthreshold region (for $V_{GS} < V_{th}$)

10.2 Linear and Saturation Region

A model of saturation drain current of MOSFET is proposed by (10.2) [105]. This model contains the influence of the body-effect coefficient and the channel length modulation.

$$I_{Dsat} = \frac{1}{2\eta} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda(V_{DS} - V_{Dsat})) \quad (10.2)$$

With a typical value of channel length modulation of 0.01/V, I-V characteristic (drain current vs. drain voltage) of the proposed device is presented in Figure 10.2 for different body-factor values. The simulation shows the dependency of the drain current on the body-factor. Note that as η increases the drain current decrease significantly. It is observed that like conventional FET the current initially increases linearly after the threshold voltage, and then the device gets saturated.

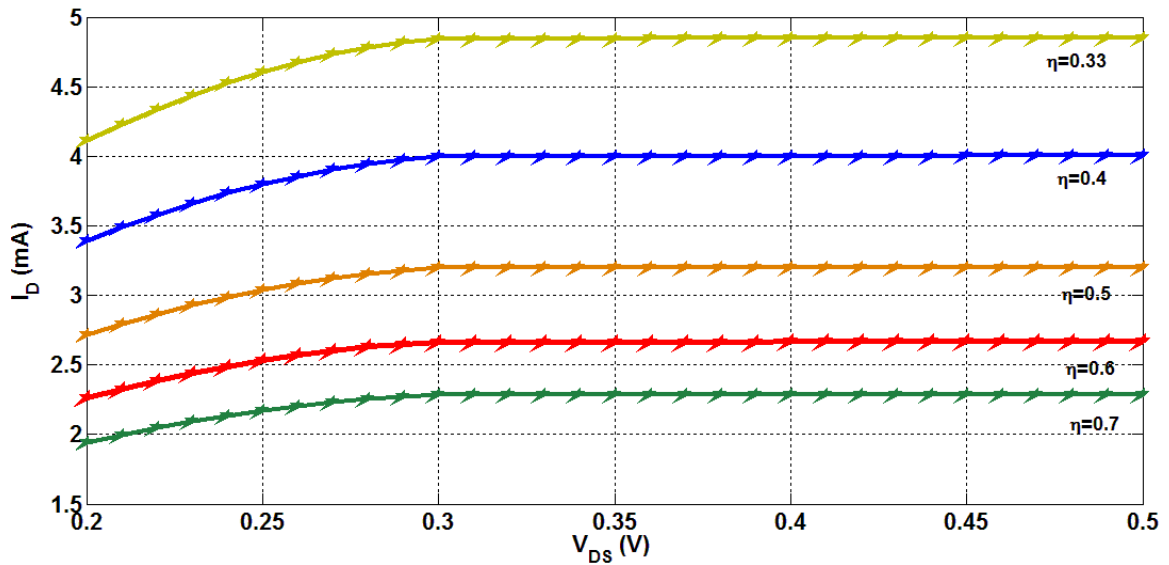


Figure 10.2: I-V characteristic and the impact of the body-factor on drain current.

The Figure also shows that the device can provide a large on-state current for small body-factor. This simulation demonstrate that the device derive a current of $2.4\mu\text{A}/\mu\text{m}$ at threshold voltage ($V_{th}=V_{GS}$). The saturation current of this proposal is $4.8\text{mA}/\mu\text{m}$. Notice also that deferent body factors can generate various threshold voltages and on-state current. Other observation is the ability of the device to saturate early.

CHAPTER 11

ADVANTAGES, MANUFACTURING PROCESS AND FUTURE WORK OF THE PROPOSED DEVICE

11.1 Advantages of the *SOF-FET*

This proposal conserves the same carrier transport mechanism. Thus a high on-state current can be derived at low threshold voltage. This proposal has serious advantages that make it preferred over other ultra-low power design especially ferroelectric based designs. The fabrication process is similar to currently used SOI CMOS technology (principally fully depleted SOI structure). Since high doping increases threshold voltage this proposition perceptibly, can be design with a low channel doping. In addition, having a ferroelectric film act as supplement gate causes the short channel effects (SCEs) to decrease giving the possibility of shrinking the device. Furthermore, this design structure keeps the operating area of the device similar to the conventional MOSFET. As well as the electric field (gate voltage) applied to construct the channel will not be deviated by integration an additional material or two on the gate stock. Thus this structure provides a stable gate voltage compared to gate stock structure discussed in the other sections. The advantages briefly listed here:

Advantages

- ✓ Speed: fast switching on and off
- ✓ Power: operate at low threshold voltage and supply voltage
- ✓ Integration capability in current CMOS technology.

- ✓ Low off-state current
- ✓ Low leakage: removes all the injected carries when the device switching from on to off state.
- ✓ High on-state current
- ✓ All the advantage of SOI technology

However the involvement of the ferroelectric film in this design obliges restraints due to intrinsically unstable negative capacitance [105]. These restraints capitalized in temperature dependency of the ferroelectricity behavior of the material. In [97] a dielectric deviation of ferroelectric material was reported due to temperature variant. This deviation obliges a thoughtful design to distinguish an accurate polarization under external electric field.

Wide and various researches are heading toward investigating ferroelectric materials and their properties. The material integration into logical switch requires a deep investigation to determine its performance and stability in the IC working atmosphere. One of the parameters that concern the integrating of any new material into IC is temperature. In [104] stated that nowadays devices are operated at 100 C or higher temperature. The cooperation of the ferroelectric material and preserving negative region operation at innumerable temperature condition is beyond the scoop of this paper (considered as future work). However, [104] have focused on the temperature dependency of this material and a behavior model was derived.

11.2 Discussion on Potential Manufacturing Process

The existing processing and fabrication technologies for Silicon-On-Insulator technology (SOI) and Silicon-On-Sapphire (SOS) can be adopted for the proposed device. Instead of a single layer of insulator as in SOI and SOS devices, there will be a thin layer of ferroelectric material and another thin layer of buffer insulator over the wafer of the device (Figure 11.1). Both the ferroelectric and buffer insulating layers should have thicknesses of few nanometers to maintain a small subthreshold swing. Several ferroelectric materials were explored by several research groups to be used in semiconductor device. Successful growth of ferroelectric materials on silicon will open the door for further progress in IC design.

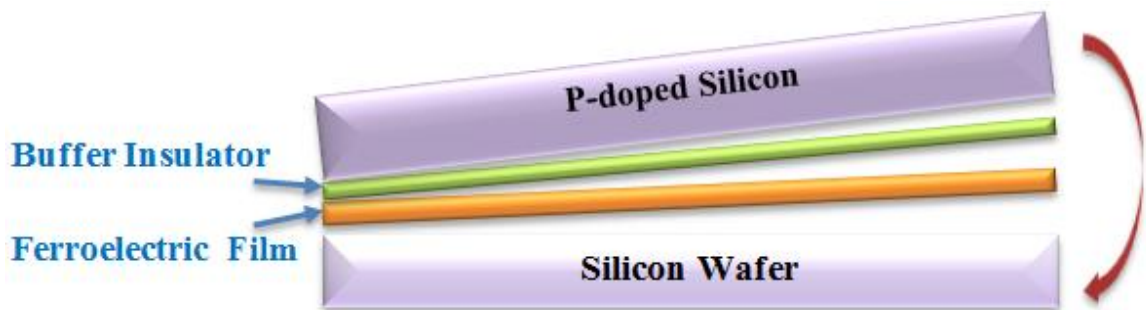


Figure 11.1 Multilayer wafer viewing the ferroelectric material and the buffer insulator placement

The interest of integrating ferroelectric materials with silicon has grown recently especially in the nonvolatile ferroelectric memories. An approach of depositing $\text{La}_x\text{Sr}_{1-x}\text{TiO}_3$ (LSTO) and SrTiO_3 (STO) onto silicon wafers are reported by [107, 108]. Ferroelectric material sensitivity to temperature causes formation of intermediate layer on the silicon (structural changes in lattice). To solve this issue an insulator layer placed in

between the active device and the ferroelectric material. A group of materials to serve this purpose are studied in [109]. This layer roll is to manage the stability between the silicon and the ferroelectric materials. The buffer insulator layer must hold a high dielectric constant, and high thermal stability.

The deposition of the ferroelectric materials on silicon wafer is hot research topic nowadays due to potential advantages that could be gained from this reparation. Various methods to deposit a thin film of ferroelectric material on silicon were recommended. Spin-coating and thermal annealing process used to deposit thin film of Ferroelectric lead calcium titanate $[(\text{Pb}_{0.76}\text{Ca}_{0.24}) \text{TiO}_3]$ on platinum-coated silicon substrates was described in [124]. Ferroelectric nature of the martial was preserved after the deposition. Molecular beam epitaxy (MBE) was also used to deposit epitaxial SrTiO_3 films on (001) Si substrates via a kinetically controlled growth process [111, 112]. Physical and chemical deposition techniques have proved successful deposition of PZT films [113, 114]. $\text{Pb}(\text{Zr}_x\text{T}_{1-x})\text{O}_3$ (PZL) and $(\text{Pb}_{1-2/3y}, \text{La}_y)(\text{Zr}_{1-x}, \text{Ti}_x)\text{O}_3$ (PLZT) have publicized numerous advantages, therefore well-thought-out for the ferroelectric random access memories (Fe-RAM) designs. PZT were prepared by several methods. However, pulsed laser deposition is a suitable method for preparation of highly oriented multicomponent thin films [115].

11.3 Conclusion and Future Work

We are performing further investigation to study the feasibility of the concept of the proposed device. Good news is that the ferroelectric materials have already been integrated into silicon for memory circuit design. However, the integration of

ferroelectric materials into semiconductor devices is not an easy task. High temperature is still an issue that will lead to semiconductor-ferroelectric interference. In the foreseeable future silicon technology will still remain the base technology while modernizing future devices. Since process maturity and cost are important factors, sudden shift from silicon base is not feasible. Therefore, effort to integrate different materials into silicon platform always gets huge attention. We expect that our proposed design will open the door for a new generation of ferroelectric material based devices for high performance and extremely low power consumption. SOF-FET is promising for future ultra-low-power applications, because it demonstrates ability to replace the silicon-bulk based MOSFET, and offers subthreshold swing significantly lower 60mV/decade and reduced threshold voltage to form a conducting channel. The *SOF-FET* can also solve the issue of junction leakage (due to the presence of unipolar junction between the top plate of the negative capacitance and the diffused areas that form the transistor source and drain). In this device the charge hungry ferroelectric film already limits the leakage.

APPENDIX

This appendix contains vital information. Estimation of the Body Factor (η) of SOI

FinFET

For convenience the equivalent circuit (Figure 9b) of the internal device capacitances of SOI-FinFET is copied here again in Figure A1.

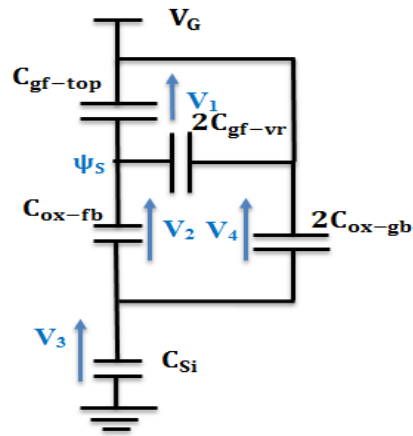


Figure A1: An equivalent circuit model of SOI-FinFET capacitances.

For the ease of calculation and handling let us use the following notation for the capacitances.

$$C_1 = C_{gf-top} + 2C_{gf-vr} \quad (A1)$$

$$C_2 = C_{ox-fb} \quad (A2)$$

$$C_3 = C_{Si} \quad (A3)$$

$$C_4 = 2C_{ox-gb} \quad (A4)$$

Here C_1 and C_2 are in series and their equivalent capacitance can be given by (A5). And the equivalent capacitance C_{eq} can be given by (A6).

$$C_o = C_1 C_2 / (C_1 + C_2) \quad (A5)$$

$$C_{eq} = (C_o + C_4) C_3 / (C_o + C_3 + C_4) \quad (A6)$$

The total charges distributed in the capacitive network can be written as: $q = V_G C_{eq}$.

V_G is the total voltage applied on the network (gate voltage).

Since C_1 and C_2 are in series, thus, share the same charge. Similarly C_1, C_2, C_4 shared the same charges with C_3 . By considering the same ideologies of a current flow past a given point (if V_i is the voltage across the capacitor C_i , the charges is defined by the relation $Q_i = C_i V_i$). The total charges can be expressed as shown in the equations below:

$$q = C_1 V_1 + C_4 V_4 \quad (A7)$$

$$q = C_2 V_2 + C_4 V_4 \quad (A8)$$

$$q = C_3 V_3 \quad (A9)$$

$$q = C_{eq} V_G \quad (A10)$$

Furthermore, since C_1 and C_2 share the same charges and V_1 and V_2 are the voltages across each of them, we have: $C_1 V_1 = C_2 V_2$ hence $V_1 = C_2 V_2 / C_1$

From Kirchhoff's Loop Rule: $V_1 + V_2 = V_4$ (Figure A1 shows the loop).

Substitute for V_1 its equivalent expression to get:

$$V_4 = V_2(C_1 + C_2)/C_1 \quad (\text{A11})$$

By equating (A9) and (A10) we get the expression (A12).

$$V_3 = C_{\text{eq}}V_G/C_3 \quad (\text{A12})$$

Substituting (A11) into (A8) to get:

$$q = \left[C_2 + (C_2 + C_1) \frac{C_4}{C_1} \right] V_2 \quad (\text{A13})$$

Equating the equations (A10) and (A13) and solve for V_2 to get:

$$V_2 = \frac{C_{\text{eq}}V_G}{C_2 + (C_2 + C_1) \frac{C_4}{C_1}} \quad (\text{A14})$$

We have:

$$\psi_S = V_2 + V_3 \quad (\text{A15})$$

Replacing (A12) and (A14) into (A15) to get:

$$\psi_S = C_{\text{eq}}V_G \left[\frac{C_1C_2 + C_1C_3 + (C_2 + C_1)C_4}{\{C_1C_2 + (C_1 + C_2)C_4\}C_3} \right] \quad (\text{A16})$$

Solving for V_G to get:

$$V_G = \frac{1}{C_{\text{eq}}} \frac{\{C_1C_2 + (C_1 + C_2)C_4\}C_3}{C_1C_2 + C_2C_3 + (C_2 + C_1)C_4} \psi_S \quad (\text{A17})$$

The body factor η can evaluated as:

$$\eta = \frac{1}{C_{\text{eq}}} \frac{\{C_1C_2 + (C_1 + C_2)C_4\}C_3}{C_1C_2 + C_2C_3 + (C_2 + C_1)C_4} \quad (\text{A18})$$

The equation (A18) simplified to:

$$\eta = 1 + \frac{C_2 C_3}{C_1 (C_2 + C_3 + C_4) C_2 C_4} \quad (\text{A19})$$

Replacing C_{eq} , C_1 , C_2 , C_3 , and C_4 with their values (A1, A2, A3, and A4) to get:

$$\eta = 1 + \frac{C_{ox-fb} \times C_{Si}}{(C_{gf-top} + 2 \times C_{gf-vr}) \times (C_{ox-fb} + C_{Si} + 2C_{ox-gb}) + 2 \times C_{ox-fb} \times C_{ox-gb}} \quad (\text{A20})$$

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VITA

Azzedin Es-Sakhi was born in 1980. He received his first B.S. degree in Science & Technology in 2002 from Cadi Ayyad University, Faculty of Science and Technology, Morocco. In 2011, he received his second B.S. degree in Electrical and Computer Engineering from University of Missouri-Kansas City (UMKC). He is currently working toward his Master of Science (MS) in Electrical and Computer Engineering at UMKC under Dr. Masud Chowdhury.

His research interests include analyzing the Prospects of Emerging FinFET, Carbon nanotube based FET Devices, and technologies for Ultra-Low-Power Subthreshold Design. Investigation of a New Field Effect Transistor (FET) Design based on Ferroelectric Material to Utilize Negative Capacitance Effect in Subthreshold Designs.