ENERGY AND DATA CONVERSION CIRCUITS FOR LOW POWER SENSORY SYSTEMS

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ENERGY AND DATA CONVERSION CIRCUITS FOR LOW POWER SENSORY SYSTEMS

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ABSTRACT

This dissertation focuses on the problem of increasing the lifetime of wireless sensors. This problem is addressed from two different angles: energy harvesting and data compression. Energy harvesting enables a sensor to extract energy from its environment and use it to power itself or recharge its batteries. Data compression, on the other hand, allows a sensor to save energy by reducing the radio transmission bandwidth.

This dissertation proposes a fractal-based photodiode fabricated on standard CMOS process as an energy harvesting device with increased efficiency. Experiments show that, the fractal based photodiodes are 6% more efficient compared to the conventional square shaped photodiode. The fractal shape photodiode has more perimeter-to-area ratio which increases the lateral response, improving its efficiency.

With increased efficiency, more current is generated but the open-circuit voltage still remains low (0.3V - 0.45V depending on illumination condition). These voltages
have to be boosted up to higher values if they are going to be used to power up any sensory
circuit or recharge a battery. We propose a switched-inductor DC-DC converter to boost
the low voltage of the photodiodes to higher voltages. The proposed circuit uses two on-
chip switches and two off-chip components: an inductor and a capacitor. Experiments
show a voltage up to $2.81V$ can be generated from a single photodiode of $1\text{mm}^2$ area.
The voltage booster circuit achieved a conversion efficiency of $59\%$.

Data compression was also explored in an effort to reduce energy consumption
during radio transmission. An analog-to-digital converter (ADC), which can jointly per-
form the tasks of digital conversion and entropy encoding, has also been proposed in this
dissertation. The joint data conversion/compression help savings in area and power re-
sources, making it suitable for on-sensor compression. The proposed converter combines
a cyclic converter architecture and Golomb-Rice entropy encoder. The converter hard-
ware design is based on current-mode circuits and it was fabricated on a $0.5\ \mu m$ CMOS
process and tested. Experiment results show a lossless compression ratio of $1.52$ and a
near-lossless compression of $5.2$ can be achieved for $32 \times 32$ pixel image.
The faculty listed below, appointed by the Dean of the School of Graduate Studies, have examined a dissertation titled “Energy and Data Conversion Circuits for Low Power Sensory Systems,” presented by Suvradip Ghosh, candidate for the Doctor of Philosophy degree, and hereby certify that in their opinion it is worthy of acceptance.

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CHAPTER 1

INTRODUCTION

Advances in CMOS technology have enabled the fabrication of on-chip sensory systems that integrate sensors, computational and communication circuits. However powering these devices for extended period of time remains an issue. An effective solution to extend the life of these sensors would be to harvest ambient energy to power these sensors or recharge the batteries. On-chip energy harvesting is especially appealing because it can reduce fabrication costs and reduce size. An energy collection device that is readily available in standard CMOS processes is a simple photodiode. It has been demonstrated previously [29], [23], [80] that integrated photodiodes can be used to power up small circuits.

Another approach in extending the life of sensors is to reduce the power consumption. Radio communications is one of the most energy-demanding operations that a wireless sensor must perform. Thus, reducing the amount of data transmitted wirelessly has the potential to reduce power consumption and increase the sensor’s battery lifetime. Data compression techniques can be employed to reduce the number of bits that are to be transmitted. However, standard data compression algorithms require significant memory and processing resources precluding their direct implementation at the sensor level. Moreover, standard data compression is performed entirely in the digital domain. Given that most sensors outputs are analog, the sensor’s output needs to be converted to digital
before it can be compressed. Hence, there is an opportunity to perform some of the oper-
tions required for compression in the analog domain with simple and low-power circuits. 
In this work compression is achieved with an ADC that can simultaneously quantize and 
compress a signal.

1.1 Literature Review

An attempt on improving the efficiency of photodiodes for on-chip solar energy 
harvesting is presented in [29], [28]. Authors employ P-diff/N-well finger-like photodiodes 
with vertical optical diffraction gratings. The goal of these vertical diffraction 
gratings was to increase the optical efficiency of the photodiodes. These gratings help 
reflect and diffract the light back and forth. By realizing various heights of these gratings, 
the direct reflection of the light was reduced and more light was diffracted towards the 
photodiode. These gratings also creates a vertical parallel plate storage capacitance that 
can be used to store the harvested energy. A drawback of this approach is that light has 
to hit the chip surface at a certain incident angle for the diffraction grating to be useful. 
Increase in optical efficiency was achieved at the cost of low output voltage. 

Our approach increases the efficiency of the energy-harvesting photodiodes by 
employing diodes with fractal geometries that have large perimeter-to-area ratios. The 
motivation for using a fractal shape is that an increase in perimeter will lead to an in-
crease in the photodiode’s peripheral response. The peripheral response is a mechanism 
by which photo-generated carriers are collected by the lateral depletion regions. This 
mechanism leads to a photoactive area that may be much larger than the original $p - n$
junction area [32]. This phenomenon is called the edge effect [72]. According to edge effect the amount of charges collected increases due to lateral diffusion. In applications such as imaging, the peripheral response gives rise to lateral crosstalk which degrades the contrast of an image [73]. However, for energy collection it is a desirable feature.

Various researchers [31], [68] have worked towards solving for the exact solution of the peripheral response of photodiodes. They have proven with numerical analysis that lateral photoresponse contribute to the net charges collected when these diodes are used as photodiodes. In [1], a two dimensional model was proposed to solve for the current contributed by the lateral diodes. The approach is two dimensional because, when light hits these lateral diodes, the concentration \(e-h\) pairs generated due to the incident photons vary along the depth of the junction and the distance from the \(p-n\) junction.

Fractal-based geometries have been applied to the design of other devices such as integrated capacitors that exploit the lateral flux resulting in a 2.3 increase in the capacitance per unit area [67]. The space-filling property of fractals has been used in the design of antennas to maximize the length of the radiating material [25]. Fractal-shaped \(p-n\) junctions are suggested in [30] as a means to improve the time response of photodiodes employed in optical communications. Distributed and fractal pixel sensors are described in [37]. In that study the aim was a reduction in spatial aliasing by designing distributed pixels that approximate a sinc sampling function.

The photodiodes available in standard CMOS have a relatively low open-circuit voltage, around 0.40V to 0.55V depending on the illumination conditions. Higher voltages are needed to be able to charge a battery or to power up the sensor’s circuitry. The
conventional approach to generating higher voltages is to serially stack several photodiodes. In standard CMOS, it is difficult to stack photodiodes because photodiodes share the same substrate. Another challenge found in standard CMOS is the presence of current losses due to parasitic photodiodes. If the parasitic current losses are not properly compensated, the amount of harvested power can be significantly decreased. If a silicon-on-insulator (SOI) fabrication process is employed, photodiodes can be isolated and they can be easily stacked. Moreover, parasitic photodiodes are eliminated in a SOI process. However, SOI is a much more costly technology than standard CMOS.

Several efforts have been undertaken to address the challenges of on-chip solar cell integration in standard CMOS processes. In [2] a voltage between 0.6V to 0.83V is generated by connecting a P-diff/N-well and a P-sub/N-diff photodiodes in series. However, this approach is limited to only two serially-connected photodiodes. Moreover, the substrate has to be left floating to a potential that depends on the light intensity. Hence, the voltage threshold of transistors integrated on the same substrate with the photodiodes is not well defined.

In [39] current losses due to parasitic diodes are compensated by employing additional photodiodes. Although this approach enables the stacking of photodiodes and generates voltages between 0.84V to 1.3V, its efficiency is quite low (0.3% to 0.06%). Moreover, additional silicon area is needed for parasitic current loss compensation. In [29], photodiodes fabricated in a standard CMOS process are employed as solar cells to harvest energy. An open circuit output voltage of 1.09 V was obtained by stacking photodiodes. However, the stacked photodiodes have to reside in different integrated circuits.
to allow the microchip substrate to be tied to a non-ground potential. In [69] photodiodes fabricated in a triple-well fabrication process are employed for energy harvesting. A triple-well process enables the stacking of photodiodes fabricated on the same microchip. However, they still suffer from losses due to parasitic photodiodes. In this dissertation, a voltage boost circuit has been defined, which can boost the voltage generated by the photodiodoes to $2.81V$ which are sufficient to recharge a battery or power a sensor.

Addressing the problem of lowering the power consumption spent during transmissions, different hardware implementation of on-sensor compression have been reported. Typically, to compress a sensor’s output, it is first converted to a digital representation by means of an ADC. Once in the digital domain, the data is decorrelated and compressed by means of an entropy encoder. Entropy encoders operate exclusively in the digital domain. Thus, separate circuits for conversion and compression are normally needed. The combination of the analog-to-digital conversion and entropy coding operations in a single circuit has the potential to lower power and area requirements of the sensor. However, to make this possible new architectures are needed that enable to jointly perform analog-to-digital conversion and entropy encoding operations.

In [59] a simplified version of the Huffman encoder is integrated with a 12-bit successive approximation ADC. The goal was to reduce the conversion time by producing shorter codewords for input voltage ranges that occur more often. However, due to the complexity of the Huffman encoder, the input was divided in only three regions and each region was assigned a codeword. Although sub-optimal, it reduces power consumption
and conversion time by not generating unnecessary bits. The circuit implementation employs a charge redistribution digital-to-analog converter (DAC) to perform the successive approximation conversion. This approach was later improved and incorporates variable resolution and conversion rates [20].

Another approach combines vector quantization with the design of an ADC [51]. In that work the boundaries of the ADC quantization bins are continuously updated via a neural network learning rule. The complexity of this approach increases with the size of the input vector due to the fact that one ADC per input dimension is used. Additional space is required to store a tree that encodes the parameters of the converter.

In [42] a dual-slope integrating ADC is combined with a Golomb-Rice entropy encoder. The digital counter that is normally present in an integrating ADC is employed to perform the division operation required by the Golomb-Rice algorithm. The concept can also be extended to single-slope converters. A theoretically optimum rule to adapt the encoder to the statistics of the input is also provided. The drawback of this converter is its long conversion times. For an N-bit resolution conversion $2^{N+1}$ clock cycles are needed.

A successive approximation converter with compressed output was reported in [21]. Compression is achieved by coarsely dividing the input range into three regions and assigning a codeword to each region. Hence, it provides sub-optimal compression, nevertheless is helps to reduce power consumption by generating fewer number of bits.

Other hardware implementation of on-sensor compression include on-sensor 2-D analog discrete cosine transform (DCT) [36], [5], analog implementation of a 1-D and
2-D Haar wavelet transform for image compression [57], and quadrant tree decomposition (QTD) [74], [3]. In [36] and [57] the entropy coding is performed off chip, however, the clear goal of such efforts is ultimately total on-sensor integration of all data acquisition, compression, and transmission functions. The QTD compression approach does not employ an entropy coder. However, QTD results in expansion rather than compression for signals that exhibit moderate to high levels of activity. We propose an ADC that can jointly perform the tasks of conversion and compression.

1.2 Summary of Contributions

The main contribution of the work are as follows:

- Firstly, we address the problem of low efficient on-chip solar cell. We implemented photodiodes with fractal-based geometries, that helped improve the perimeter-to-area ratio, which in-turn increased the effective photo-active area of the photodiode. The fractal geometry yielded in more charges to be collected increasing the efficiency by 6% compared to regular geometric shaped photodiodes.

- Secondly, a DC-DC boost convert circuit is implemented on-chip, to boost the output voltage of a photodiode to higher values that can be used to power up a sensor or recharge the batteries. The effect of parasitic photodiodes is addressed and a solution to minimize their impact is presented. A theoretical analysis of a switched-inductor DC-DC converter is carried out and a mathematical model of the energy harvester is developed. Measurements taken from a fabricated integrated circuit are presented. Measurement results show that voltages of up to $2.81V$ (depending on
illumination and loading conditions) can be generated from a single photodiode. The energy harvester achieves a maximum efficiency of 59%.

- An ADC that can jointly perform the tasks of conversion and compression was devised. The compression is performed in the analog domain, giving us the advantage of reducing the size, complexity of the circuit and the overall power consumption compared to circuits that perform these tasks separately. The proposed compressing ADC is based on an cyclic converter architecture and generates Golomb-Rice code-words at its output (the Golomb-Rice encoder is a type of entropy encoder that has low circuit complexity yet provides competitive compression ratios [26]). The basic observation that enables the proposed ADC to jointly quantize and encode analog signals is that changing the loop gain in a cyclic converter leads to the generation of unary codes which are an important part of Golomb-Rice codes. The proposed converter also addresses the drawbacks of the converters in [26] and [21].

The chapters in the dissertation are organized as following: Chapter 2 discusses the basic background of a photodiode, fractal structures, boost converted and cyclic architecture based ADC. Chapter 3 presents the current equations for vertical and lateral-photo-responses. It also discusses the experiment setup used to test thees photodiodes and analyze test results. Chapter 4 presents detailed mathematical analysis of the lateral capacitance of capacitor fabricated in the area surrounding the fractal based photodiode. Chapter 5 presents the proposed boost converter circuit that boosts the photodiode open circuit voltage to a higher value that can power the sensory circuit. Chapter 6 presents the proposed ADC that helps reduce the power consumption of the sensory system.
CHAPTER 2

BACKGROUND

In this chapter, we discuss the background on why silicon based diodes are suitable to work as solar cells. We derive the basic current equation for a photodiode. Then we discuss the how fractal base photodiode can increase the perimeter-to-area ratio without increasing the physical area of the photodiode. In the last section we discuss the functioning of a boost converter and cyclic architecture based ADC.

2.1 Photodiodes

Electrons in free space, effectively have a continued range of energies, but when the electrons are associated to an atom, they acquire discrete energy levels. When a number of atoms come together to form a crystal, these discrete energy levels form a continuous energy band. The highest level of energy at which electrons exist at absolute zero temperature is called the valance band. Energy bands beyond the valance band, where electrons are free from binding with its atom is called the conduction band. These bands are separated by a gap known as forbidden energy gaps or band gap.

For a pure intrinsic semiconductor, the bang gap energy $E_g$ is of the range of $0.67eV - 1.12eV$. This energy can be provided by the photons of light within the visible spectrum. When photons hits an electron, it gives up its energy, leaving the electron in an excited state. If the energy absorbed by the electron is more than the band gap energy, the
electron moves to the conduction band, leaving behind a hole in its place in the valance band. These holes, like electrons, act as charge carriers. When an electron moves, it leaves behind a hole in its place. Thus, these electrons-holes help conducting electricity. If these electrons can be collected before they lose their excited state and recombine, this can be used to produce a small current, drive a small circuit.

When a p-n junction is formed, the electrons tend to flow or diffuse from higher concentration to lower concentration, that is, from n-type into the p-type semiconductor leaving behind positive charges. Similarly, the holes from p-type flow into n-type leaving behind negative charge. This process goes on till the n-type side of the diode develops sufficient positive charge to repel the holes that are flowing in from p-type or when the p-type side builds sufficient negative charge to repel any further diffusion of electrons from n-type. Thus, a potential barrier also called depletion region is formed at the p-n junction (Fig. 1). When light hits this region, more electrons are excited and they try to flow across this barrier and increasing the charge across the depletion region. This potential barrier holds the excited electrons from going back to its ground state. If a load is connected between p and n, due to this potential difference, a current will flow through the load.

In a standard CMOS process, there are three different combinations to form a photodiode:

- Psub/Ndiff
- Psub/Nwell
- Nwell/Pdiff
Psub is always connected to the lowest potential (ground in most cases) to avoid forward biasing of any p-n junction across the chip. For p-n junction to act as a solar cell, both p and n terminals have to be freely available. In case 1 and 2, as the diode consists of Psub, they cannot be used as solar cell but they can be used as light sensors in image sensing. Case 3 configuration can be used as a solar cell as as both the Nwell and Pdiff terminals are freely available. Figure 2 shows a cross-sectional view of the photodiode.It also shows the spread of the depletion region of the diode formed by Nwell/Pdiff. Based on the geometry of the spread, the photo-response of a diode can be divided into

- vertical photo-response
- lateral photo-response

Vertical photo-response is due the photo-generated carriers along the flat area of the photodiode. Lateral photo-response lies along the lateral depletion regions spread through out the perimeter of the diode. When light is illuminated on a CMOS process based photodiode, electron-hole pairs are generated all over the diode. Since the depletion
region of the lateral photodiode is exposed to light directly, all the e-h pairs generated in this region easily diffuse across the junction and are available for collection. The goal of my research is to increase this contribution of lateral photodiode towards the total charge collected. This can be achieved if the perimeter-to-area ratio is increased. Attempts have been made to increase this ratio by using fringe like diode [], which has a very high perimeter-to-area ratio, but this is achieved at the expense of vertical area. A fractal base geometries has a good balance between the vertical area and the perimeter of the diode. We have implemented three different fractal geometry. In the following sections we discuss about fractal geometry and how they help increase the perimeter-to-area ratio.

![Figure 2: CMOS diode](image)

### 2.2 Fractals

A fractal is a concept introduced by Benoit B. Mandelbrot [49] that denotes a large class of objects that have the basic property of self-similarity and scale invariance.
Fractals can be constructed by the repeated application of a rule to an initial geometrical shape or seed or can also be created from mathematical formulas. Many natural objects like mountains, the coastline of an island or a fern can be described with the help of fractals.

The photodiode design presented in this work is based on the quadric Koch island curve. We chose this fractal because it requires only right angle corners which makes it easier to design the corresponding layout. To construct the *quadric Koch Island* fractal we start with an initial square. This initial shape is called the *initiator*. A *generator* is then applied to each side of the initiator and the process is repeated on each side of the resulting curve. Figure 3 shows one iteration of this process. In principle this procedure can repeated indefinitely resulting in a true fractal, however, in practice it is limited by the design rules and lithography resolution of the targeted fabrication process.

The fractal dimension \( D \) is a concept that is used to describe the complexity of a fractal. For flat fractals the dimension is a real number between one and two. A higher dimension means that the fractal covers a flat surface more efficiently. For our application, fractals with higher dimensions would be desirable. All dimensional \( D \)satisfy

\[
D = \frac{\log N}{\log \left( \frac{1}{r} \right)} \tag{2.1}
\]

where \( N \) is the number of segments of the initiator (18 in this case) and \( r \) is the ratio of the generator segment size to the initiator segment size (1/6 in this case). For the quadric Koch island fractal the dimension is \( \log 8 / \log 6 = 1.6131 \).

An additional feature of the quadric Koch island that is useful in the intended application is that the area remains the same while the perimeter increases. For a general
initiator, the perimeter is proportional to the area

\[ P_0 = k \cdot \sqrt{A} \quad (2.2) \]

where \( k \) is the proportionality constant depending on the geometry of the initiator. For a square \( k = 4 \). After \( n \) successive iterations, the perimeter of the quadric Koch island is given by

\[ P_n = (Nr)^n k \cdot \sqrt{A} \quad (2.3) \]

The length of each segment of the fractal at the \( n^{th} \) iteration is:

\[ \ell_n = (r)^n \ell_0 \quad (2.4) \]
where $\ell_0$ is the initial length of a side of the initiator. From equation (2.3) it seems that an arbitrarily long perimeter can be achieved by simply increasing the number of iterations. However, $n$ will be ultimately limited by the design rules of the targeted process. For a P-Diff/N-Well diode on a 0.5$\mu$m CMOS process, the minimum is 0.9$\mu$m.

Although a fractal has the same area, it needs more enclosing area. This excess area can be used to build capacitors, that help store charge extracted from the photodiode. These capacitors have partial fractal structure which help in increasing capacitance per unit area. We discuss the increase in capacitance due to partial fractal structures in chapter 3. In the following sections we will look into different fractal structures that can be implemented for the design of solar cells. We will derive mathematical expression for perimeter, enclosed area, residual area and its perimeter for all the structures we discuss. Later in this section, we will discuss structures that are not completely fractal but increase the perimeter by a certain factor.

2.2.1 Quadratic Koch Island

Koch Island is a base-motif fractal with a polygon as the base and the motif is any curve. Let $\ell$ denote the length of each side of the initiator and $\ell_n$ be the length of each line segment after $n$ iteration. The $n = 0$ case is the initiator. In the $n = 1$ case, each line segment is replaced by the generator and the resulting geometry is given above in Fig. 4. For $n = 2$ each line segment in Fig. 4 is replaced with the same generator and the ratio $r$ of generator line segment size to the line segment of the fractal for $n = 1$ is $1/6$.

The ratio $r$ doesn’t change with number of iteration $n$ and as we are using the
same generator with $N = 18$, $D$ remains constant.

**Perimeter of Fractal**

With every iteration, the length of the line segment reduces $(1/6)$ times the previous iteration. After $n$ iterations, we have infinite number of small line segments with the length $\ell_n = (\ell/6^n)$ thus increasing the perimeter. The total perimeter can be calculated as shown in Table 3.
Table 1: Ratio $r$

<table>
<thead>
<tr>
<th>Iteration</th>
<th>$r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n = 1$</td>
<td>$r = \frac{\ell}{\ell/6} = \frac{1}{6}$</td>
</tr>
<tr>
<td>$n = 2$</td>
<td>$r = \frac{\ell}{\ell/6^2} = \frac{1}{6}$</td>
</tr>
<tr>
<td>$n = 3$</td>
<td>$r = \frac{\ell}{\ell/6^3} = \frac{1}{6}$</td>
</tr>
<tr>
<td>$n = 4$</td>
<td>$r = \frac{\ell}{\ell/6^4} = \frac{1}{6}$</td>
</tr>
<tr>
<td>$n = n$</td>
<td>$r = \frac{\ell}{\ell/6^n - 1} = \frac{1}{6}$</td>
</tr>
</tbody>
</table>

Table 2: Length $\ell$

<table>
<thead>
<tr>
<th>Iteration</th>
<th>$\ell$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n = 1$</td>
<td>$\ell_1 = \frac{\ell}{6}$</td>
</tr>
<tr>
<td>$n = 2$</td>
<td>$\ell_2 = \frac{\ell}{6^2}$</td>
</tr>
<tr>
<td>$n = 3$</td>
<td>$\ell_3 = \frac{\ell}{6^3}$</td>
</tr>
<tr>
<td>$n = 4$</td>
<td>$\ell_4 = \frac{\ell}{6^4}$</td>
</tr>
<tr>
<td>$n = n$</td>
<td>$\ell_n = \frac{\ell}{6^n}$</td>
</tr>
</tbody>
</table>

Generalizing the expression for perimeter for $n^{th}$ iteration, we can write

$$P_n = 4(Nr)^n \ell$$  \hspace{1cm} (2.5)$$

Thus from equation (2.5) we see that the perimeter increases exponentially with $n$. Fig 5 shows a plot of perimeter with respect to $n$.

**Enclosing Area**

From Fig. 4 we see the enclosing area (in red square) is greater than the original square of length $\ell$. This extra area (enclosed area minus the fractal area) can be used to fill with other circuits on the chip or can be used build capacitors. The enclosed area increases with increase in $n$. The increase is very high for lower values of $n$, typically $0 < n < 3$. For higher values of $n (>3)$ the increase is negligible because the enclosing area
Table 3: Perimeter $P_n$

<table>
<thead>
<tr>
<th>Iteration</th>
<th>Perimeter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n = 0$</td>
<td>$P_0 = 4\ell$</td>
</tr>
<tr>
<td>$n = 1$</td>
<td>$P_1 = 4\frac{18}{6}\ell = 12\ell$</td>
</tr>
<tr>
<td>$n = 2$</td>
<td>$P_2 = 4(\frac{18}{6})^2\ell = 36\ell$</td>
</tr>
<tr>
<td>$n = 3$</td>
<td>$P_3 = 4(\frac{18}{6})^3\ell = 108\ell$</td>
</tr>
<tr>
<td>$n = n$</td>
<td>$P_n = 4(\frac{18}{6})^n\ell = 4(3)^n\ell$</td>
</tr>
</tbody>
</table>

$(A_{enc})$ is proportional to $r^n$ (eq. (2.6)) which means with increase in $n$ the term $r^n$ reduces exponentially thus reducing $A_{enc}$ (see Fig. 6).

\[ A_{enc} \propto r^n \]  

(2.6)

The residual area can be roughly computed as eq. (2.7).

\[ \Delta A = A_{enc} - A_{fr} \]  

(2.7)

**Iteration $n = 1$**

The enclosing square (red square from Fig. 4) has a length of

\[ \ell_1 = \ell + 4 \times \frac{\ell}{6} \]

Thus area will be

\[ A_{E1} = \ell_1^2 = \left( \ell + 4 \times \frac{\ell}{6} \right)^2 \]

Residual area will be

\[ \Delta A_{1R} = A_{E1} - A_{fr} \]

\[ \Delta A_{1R} = \left[ \ell + 4 \times \frac{\ell}{6} \right]^2 - \ell^2 \]
Total perimeter of the residual area can be calculated by following the same way we did for the Koch Island.

\[ \Delta P_1^R = P_1 + 4 \times \left[ \ell + 4 \times \frac{\ell}{6} \right] - 2 \times 4 \times 2 \left( \frac{\ell}{6} \right) \]

**Iteration** \( n = 2 \)

Enclosed area will be the square in green, the length of the square is

\[ \ell_2 = \ell + 4 \times \left( \frac{\ell}{6} \right) + 4 \times \left( \frac{\ell}{6^2} \right) \]

the area will be

\[ A_2^E = \ell_2^2 = \left[ \ell + 4 \times \left( \frac{\ell}{6} \right) + 4 \times \left( \frac{\ell}{6^2} \right) \right]^2 \]

In this fractal after \( n = 2 \) there develops a small area (shown in blue hash lines Fig. 8) which cannot be utilized to place capacitors due to the design rule constrains. Instead we
fill in this area with photodiode. We will calculate that small area and then later use it to find the residual area that can be used for capacitors.

From Fig. 8, we split the area into two parts. Firstly, the four squares marked 1, 2, 3 and 4 with net area of \([4 \times (\ell/6^2)^2]\) and secondly the rectangle area marked as 5 with area of \([(4\ell/6^2) \times (2\ell/6^2)]\). Therefore the total area \(A_{sml}^2\)

\[
A_{sml}^2 = 4 \times \left(\frac{\ell}{6^2}\right)^2 + 4 \frac{\ell}{6^2} \times 2 \frac{\ell}{6^2}
\]

So, the useful residual area is

\[\Delta A_R^2 = A_F^2 - A_f - 4A_{sml}^2\]

We will calculate the perimeter of the small area which too cannot be used.

\[P_{sml}^2 = 16 \times \frac{\ell}{6^2} + 4 \times \frac{\ell}{6^2}\]
To calculate the net perimeter of the residual area, we need to subtract two small fragments of length \((2l/6^2)\) twice, because this length is common for both the enclosing square and the fractal. So the net perimeter of the residual area is

\[
\Delta P^R_2 = P_2 + 4\ell_2 - 4 \left( P_{2^{sm1}} + 4 \times \frac{\ell}{6^2} \right)
\]
Iteration $n = 3$

At $n = 3$, two line segments of $[2(\ell/6^3)]$ are added to both ends of the existing length of the enclosing square.

$$\ell_3 = \ell_2 + 4 \times \frac{\ell}{6^3}$$

The enclosed area becomes

$$A^E_3 = \left[ \ell + 4 \times \left( \frac{\ell}{6} \right) + 4 \times \left( \frac{\ell}{6^2} \right) + 4 \times \left( \frac{\ell}{6^3} \right) \right]^2$$
To obtain a general equation for the small area $A_{sml}^n$, we applied the third iteration just for the small area that we cannot use to place capacitor (see Fig. 9). The area in brown is the extra area that is added to the previously existing area shown in blue. The area in brown can be expressed

$$A_{3,add}^{sml} = 4 \times \left( \frac{\ell}{6^3} \right)^2 + \frac{2\ell}{6^3} \times \left[ 4\ell \frac{\ell}{6^3} + 4\ell \frac{\ell}{6^3} \right] + 2 \left[ 4 \left( \frac{\ell}{6^3} \right)^2 + \frac{2\ell}{6^3} \times \left( \frac{4\ell}{6^3} \right) \right]$$

Total area of the brown and the blue region

$$A_{3}^{sml} = A_{2}^{sml} + A_{3,add}^{sml}$$

So, the useful residual area is

$$\Delta A^R_3 = A^E_3 - A_{fr} - 4A_3^{sml}$$

Perimeter of the small area

$$P_{3}^{sml} = 16 \times \left( \frac{18}{6} \right) \times \left( \frac{\ell}{6^2} \right) + 4 \times \frac{\ell}{6^2} + 4 \times \frac{\ell}{6^3} + 16 \times \frac{\ell}{6^3} + 2 \left[ 16 \times \frac{\ell}{6^3} + 4 \times \frac{\ell}{6^3} \right]$$

Net perimeter of the residual area is given as

$$\Delta P^R_3 = P_3 + 4l_3 - 4 \left( P_{3}^{sml} + 2 \times \frac{4l}{6^3} \right)$$

**Iteration $n = m$**

For any value of $n$ the enclosing square length $l_n$ is expressed as:

$$l_n = \left[ \ell + 4 \times \frac{\ell}{6} + 4 \times \frac{\ell}{6^2} + \ldots + 4 \times \frac{\ell}{6^n} \right]$$
Figure 9: Residual area to be neglected at $n = 3$

\[
= \ell + \frac{4 \ell}{6} \left[ 1 + \frac{1}{6} + \frac{1}{6^{(n-1)}} \right]
\]

\[
= \ell + 4 \times \frac{\ell}{6} \times \sum_{k=0}^{n-1} 6^{-k} \quad \forall n \geq 1
\]

Using the sum formula for finite geometric series progression (note that both the numerator and denominator will give positive integers for $z \in Z$)

\[
\sum_{p=0}^{N} z^p = \frac{z^{N+1} - 1}{z - 1}
\]

So, the length $\ell_n$ can be expressed as

\[
\ell_n = \ell + \frac{4 \ell}{6} \times \left[ 1 - \left( \frac{\ell}{6} \right)^n \right]
\]

\[
\ell_n = \ell + \frac{4 \ell}{6} \times \left[ 1 - \left( \frac{1}{6} \right)^n \right]
\]
Thus the enclosing area is expressed as

\[ A_n^E = \ell_n^2 = \left[ \ell + \frac{4\ell}{5} \times \left\{ 1 - \left( \frac{1}{6} \right)^n \right\} \right]^2 \]

In general, whenever we go higher on \( n \), there is a small area added to the already existing area. This area first appears at \( n = 2 \) and then on for all values of \( n \geq 2 \), an area \( A_{n,add}^{sml} \) adds up. A general expression for \( A_{n,add}^{sml} \) can be written as

\[
A_{n,add}^{sml} = \sum_{k=2}^{n} 2^{k-2} \left[ 4 \left( \frac{\ell}{6^n} \right)^2 + \frac{2\ell}{6^n} \times \frac{4\ell}{6^k} \left\{ 1 + \frac{\ell}{6} + \ldots + \frac{\ell}{6^{n-k}} \right\} \right]
\]

So the total unusable area is

\[
A_n^{sml} = A_{n-1}^{sml} + A_{n,add}^{sml} = A_{n-1}^{sml} + \sum_{k=0}^{0} A_{n-k,add}^{sml}
\]

\[
= A_{n-2}^{sml} + \sum_{k=0}^{1} A_{n-k,add}^{sml}
\]

\[
= A_{n-3}^{sml} + \sum_{k=0}^{2} A_{n-k,add}^{sml}
\]

\[
\vdots
\]

\[
= A_1^{sml} + \sum_{k=0}^{n-2} A_{n-k,add}^{sml}
\]

But \( A_1^{sml} = 0 \), as the extra area appears only at \( n = 2 \), so:

\[
A_n^{sml} = \sum_{k=0, n > 2}^{n-2} A_{n-k,add}^{sml}
\]

\[
A_n^{sml} = \sum_{k=2, n \geq 2}^{n} 2^{k-2} \left[ 4 \left( \frac{\ell}{6^n} \right)^2 + \frac{2\ell}{6^n} \times \frac{4\ell}{6^k} \left[ 1 - \left( \frac{1}{r} \right)^{n-k+1} \right] \right] \quad (2.8)
\]
Net residual area that is useful to lay capacitors

\[ \Delta A_n^R = A_n^E - A_{fr} - 4 \times A_{n^{sml}} \]

Perimeter of the small area \( n = m; n \geq 2 \)

\[ P_{n^{sml}} = \sum_{k=2}^{n} 2^k \frac{\ell}{6^k} \left[ 4 \times \sum_{p=0}^{k} r^p \times \left\{ (N r)^{k-p} + 1 \right\} \right] \]  \hspace{1cm} (2.9)

Net perimeter of the residual area for \( n \geq 2 \)

\[ \Delta P_n^R = P_n + 4l_n - 4 \left( P_{n^{sml}} + 2^n \times \ell r^n \right) \] \hspace{1cm} (2.10)

2.2.2 Koch Island

This has square structure as the initiator and the generator is as shown in Fig. 10. It has \( N = 8 \) and \( r = 1/4 \). The dimension \( D \) of this fractal structure is \( \log 8 / \log 4 = 1.5 \), which is within the range \( 1 < D < 2 \). This fractal increase the perimeter by \( 2^n \) times, \( n \) being the number of iteration.

**Iteration \( n = 1 \)**

Replacing every line segment of the initiator with the generator forms the structure as shown in Fig. 13. The perimeter of the structure with \( n = 1 \) would be

\[ P_1 = 4 \times (8) \times \left( \frac{\ell}{4} \right) = 4N r \ell \] \hspace{1cm} (2.11)

\( \frac{\ell}{4} \) \rightarrow Every segment is multiplied by \( 1/4 \), \( r \)

\( 8 \rightarrow \) Number of segment in the generator, \( N \)
4 \rightarrow \text{Number of line segments in the initiator}

The blue square in Fig. 13 represents the enclosing area of the fractal. The enclosed square length $l_1$ can be expressed as

$$l_1 = \ell + 2 \times \left( \frac{\ell}{4} \right)$$

Thus the enclosed area $A_1^{\text{enc}}$ is

$$A_1^{\text{enc}} = l_1^2 = \left[ \ell + 2 \times \left( \frac{\ell}{4} \right) \right]^2$$

The residual area (or combined area of $I$, $II$, $III$ and $IV$) can be expressed as

$$\Delta A_1^{\text{res}} = A_1^{\text{enc}} - A_{fr}$$

$$\Delta A_1^{\text{res}} = \left[ \ell + 2 \times \left( \frac{\ell}{4} \right) \right]^2 - \ell^2$$

$$\Delta A_1^{\text{res}} = \frac{5\ell^2}{4}$$

Figure 10: Generator with $N = 8$, $r = 1/4$
Figure 11: Koch Island at $n = 1$

Total perimeter of the residual area can be calculated by adding up the total perimeter of the enclosing square and the fractal and then subtracting the common perimeter from it. The total perimeter will be $[P_1 + 4 \times (\ell + 2 \times (\ell/4))]$ and the common perimeter will be twice of $[4 (\ell/4)]$, this segment is common for both the perimeter we are adding. So, the perimeter is expressed as

$$\Delta P^{res}_1 = P_1 + 4 \left[ \ell + 2 \times \left( \frac{\ell}{4} \right) \right] - 2 \times 4 \times \frac{\ell}{4}$$

(2.14)

$$P^{enc}_1 = 12\ell$$
The perimeter can be also calculated as

\[ P_{1}^{\text{enc}} = 4 \left( \frac{3\ell}{4} + \frac{2\ell}{4} + \frac{7\ell}{4} \right) = 12\ell \]

**Iteration n = 2**

For \( n = 2 \), we replace every line segment in Fig. 11 with the same generator (Fig. 10) with length of each segment as \( \ell/4^2 \) (see Fig. 12). The perimeter of this structure is computed as,

\[ P_{2} = 4 \times (8)_1 \times (8)_2 \times \left( \frac{\ell}{4^2} \right) = 4(Nr)^2\ell \quad \text{(2.15)} \]

(Note: 1 and 2 are just subscripts used to distinguish between two 8s)

\( \ell^2/4 \rightarrow \) The length of line segment for \( n = 1 \) is multiplied by \( 1/4 \), \( r \)

\( (8)_2 \rightarrow \) Number of segment in the generator for \( n = 2 \) case, \( N \)

\( (8)_1 \rightarrow \) Number of segment in the generator for \( n = 1 \) case, \( N \)

\( 4 \rightarrow \) Number of line segments in the initiator

The blue square in Fig. 12 is the same enclosing area as in Fig. 11 (just a bit magnified). The enclosing square (blue square) length has increased on both ends by \( \ell/4^2 \).

So the new length is

\[ l_2 = \ell + 2 \times \left( \frac{\ell}{4^2} \right) + 2 \times \left( \frac{\ell}{4^2} \right) \]

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So the enclosing area is

\[
A_{2}^{enc} = l_2^2 = \left[ \ell + 2 \times \left( \frac{\ell}{4} \right) + 2 \times \left( \frac{\ell}{4} \right) \right]^2 \tag{2.16}
\]

Residual area is computed as

\[
\Delta A_{2}^{res} = A_{2}^{enc} - A_{fr}
\]

\[
\Delta A_{2}^{res} = \left[ \ell + 2 \times \left( \frac{\ell}{4} \right) + 2 \times \left( \frac{\ell}{4} \right) \right]^2 - \ell^2 \tag{2.17}
\]
We do not further simplify, because in this form it will be easy to generalize for \( n = m \).

Now let’s calculate the perimeter of the four regions can be expressed as

\[
\Delta P_{res}^2 = P_2 + 4 \left[ \ell + 2 \times \left( \frac{\ell}{4} \right) + 2 \left( \frac{\ell}{4^2} \right) \right] - 2 \times 4 \times \frac{\ell}{4^4} \tag{2.18}
\]

**Iteration** \( n = m \)

Let’s rewrite the perimeter equations for \( n = 1 \) and \( n = 2 \) (Eq. (22) & (26)) and establish a trend (we would do the same for rest of the parameters)

\[
P_1 = 4 \ (N_r)^1 \ell
\]

\[
P_2 = 4 \ (N_r)^2 \ell
\]

As we can see as \( n \) increases, \( 4\ell \) remains constant but \( (N_r) \) keeps on increasing exponentially. Therefore, if we write a general equation for the perimeter for \( n^{th} \) iteration,

\[
P_n = 4 \ (N_r)^n \ell
\]

As per the enclosed area, with every increase in iteration, a term \( \left[ 2 \times \left( \frac{\ell}{4^n} \right) \right] \) is added to the previous length of the enclosing square. This can be written as

\[
l_n = \ell + 2 \times \frac{\ell}{4} + 2 \times \frac{\ell}{4^2} + \cdots + 2 \times \frac{\ell}{4^{n-1}} + 2 \times \frac{\ell}{4^n} = \ell + 2\ell \times \sum_{k=1, n \geq 1}^{n} \frac{1}{4^k}
\]

Enclosed area is expressed as

\[
A_{enc}^n = l_n^2 = \left[ \ell + 2\ell \times \sum_{n=1}^{n} \frac{1}{4^n} \right]^2
\]

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This fractal does not have any unused area as in quadratic Koch island, this makes the implementation of this fractal more convenient. Even though the increase in perimeter is exponential in Koch island, the perimeter grows \(2^n\) every iteration. As this fractal too, has larger enclosing area, we propose a semi-fractal structure in section 2.2.3 which helps increase the perimeter and also keep the enclosing area lower.

2.2.3 Proposed Semi-Fractal Structure

Here is the proposed semi-fractal. It was designed by us just to implement our concept of fractal on solar cell. This fractal increases the perimeter by \(2.14^n\) times which is in between the Koch island and the quadratic Koch island. The \(D\) of the fractal is 
\[
\log{15}/\log{7} = 1.39,
\]
which is again \(1 < D < 2\). The generator for this fractal is shown in Fig. 13.

![Figure 13: Generator](image)

**Iteration** \(n = 1\)

The perimeter of the fractal can be computed as
\[
P_1 = 4 \times \left(\frac{15}{7}\right) \times \ell = 4Nr\ell
\]
Enclosed area is as shown in blue square. The length of the blue square is

\[ l_1 = \ell + 2 \times \frac{\ell}{t} \]

The enclosed area is defined as

\[ A_{1E}^E = l_1^2 = \left[ \ell + 2 \times \frac{\ell}{t} \right]^2 \]

The residual area is marked as \( I, I', II \ldots IV' \) in Fig. 14. The total residual area can be calculated as

\[ \Delta A_{1E}^R = A_{1E}^E - A_{fr} \]

Areas marked with same roman numerical (normal and hash) can be combined to form one capacitor. So, the total area can be divided by 4 and then it can be split in the ratio of 5 : 3 (\( I : I' \)), to find the individual area. To calculate the net perimeter of the residual area, we can add the perimeter of the enclosing square, the fractal and then subtract the common length from them.

\[ \Delta P_{1R}^R = 4l_1 + P_1 - 2 \times 4 \times 2 \times \frac{\ell}{t} \]

**Iteration** \( n = 2 \)

Fig. 15 shows the fractal after second iteration. The perimeter of the fractal can be calculated as

\[ P_2 = 4 \times \left( \frac{15}{t} \right)^2 \times \ell = 4(Nr)^2 \ell \]

Enclosed area is as shown in red square. The length of the square is

\[ l_2 = l_1 + 2 \times \frac{\ell^2}{t} \]
The enclosed area is defined as

\[ A^E_2 = l_2^2 = \left[ l_1 + 2 \times \frac{\ell^2}{l} \right]^2 \]

In this fractal we use the same approach as used for the quadratic Koch island. We first calculate the small area (shown in blue shading) that cannot be used to fill with capacitors and we will calculate the useful residual area. Area of one of the blue region is given by

\[ A^{sm}_2 = \left( \frac{\ell^2}{l} \right)^2 + \frac{2 \ell^2}{l} \times \frac{\ell^2}{l} \]
Residual area is calculated as follows

\[ \Delta A_2^R = A_2^E - A_{fr} - 4 \times 2 \times A_{sml}^2 \]

Perimeter of the blue region can be written as

\[ P_{sml} = \frac{6 \ell^2}{l} + \frac{2 \ell^2}{l} \]

Net perimeter of the residual area that is used for capacitors

\[ \Delta P_2^R = 4l_2 + P_2 - 2 \times 4 \times 2^2 \times \frac{\ell^2}{7} - 4 \times 2 \times P_{sml}^2 \]
**Iteration** \( n = 3 \)

The perimeter of the fractal can be computed as

\[
P_3 = 4 \times \left( \frac{15}{7} \right)^3 \times \ell = 4(Nr)^3 \ell
\]

Enclosing square length is

\[
l_3 = l_2 + 2 \times \frac{\ell^3}{7}
\]

The enclosed area is defined as

\[
A^E_3 = l_3^2 = \left[ l_2 + 2 \times \frac{\ell^3}{7} \right]^2
\]

Here we calculate the extra area added to the existing area

\[
A_{3,add}^{sml} = \left( \frac{\ell^3}{7} \right)^2 + \frac{2\ell^2}{7} \times \frac{\ell^3}{7} + \frac{3\ell^3}{7} \times \frac{\ell^3}{7} + 2 \left[ \left( \frac{\ell^3}{7} \right)^2 + \frac{2\ell^3}{7} \times \frac{\ell^3}{7} \right]
\]

Residual area is calculated as follows

\[
\Delta A^R_3 = A^E_3 - A_f - 4 \times 2 \times \left( A_2^{sml} + A_{3,add}^{sml} \right)
\]

Perimeter of the blue region can be written as

\[
P^{sml}_3 = \frac{6\ell^2}{7} \left( \frac{15}{7} \right) + \frac{2\ell^2}{7} + \frac{3\ell^3}{7} + \frac{7\ell^3}{7} + 2 \times \left[ \frac{6\ell^3}{7} + \frac{2\ell^3}{7} \right]
\]

Net perimeter of the residual area that is used for capacitors

\[
\Delta P^R_3 = 4l_3 + P_3 - 2 \times 4 \times 2^3 \times \frac{\ell^3}{7} - 4 \times 2 \times P^{sml}_3
\]
Figure 16: Additional area when \( n = 2 \)

**Iteration** \( n = n \)

The perimeter of the fractal can be computed as

\[
P_n = 4 \times (N r)^n \times \ell \tag{2.19}
\]

Enclosing square length is

\[
l_n = \ell + 2 \times \ell / 6 (1 - r^n)
\]

The enclosed area is defined as

\[
A_n^E = l_n^2 = \left[ \ell + 2 \times \ell / 6 (1 - r^n) \right]^2
\]

Area to be subtracted

\[
A_{n, add}^{sm} = 2^{n-2} \times 3 \times \left( \ell / 7^n \right)^2 + \sum_{k=0}^{n} 2^{k-3} \left[ \left( \ell / 7^n + 2\ell / 7^{k-1} \times \ell / 7^n + 3\ell / 7^n \times \ell / 7^k \right) \{1 + r + \cdots + r^{n-k}\} \right]
\]

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\[ A_{n,\text{add}}^{\text{sml}} = 2^{n-2} \times 3 \times \left( \frac{\ell}{7^n} \right)^2 + \frac{\ell^2}{7^n} \sum_{k=3, n \geq 3}^{n} 2^{k-3} \left[ r^n + 2r^{k-1} + 3r^k \left\{ \frac{1 - r^{n-k+1}}{1 - r} \right\} \right] \]

Table 4: Residual area for semi-fractal

<table>
<thead>
<tr>
<th>Residual area</th>
<th>Iteration</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Delta A_R^n = A_R^n - A_{fr} )</td>
<td>( n \leq 1 )</td>
</tr>
<tr>
<td>( \Delta A_R^n = A_R^n - 4 \times 2 \times (A_{2}^{\text{sml}}) )</td>
<td>( n = 2 )</td>
</tr>
<tr>
<td>( \Delta A_R^n = A_R^n - 4 \times 2 \times (A_{2}^{\text{sml}} + A_{n,\text{add}}^{\text{sml}}) )</td>
<td>( n &gt; 2 )</td>
</tr>
</tbody>
</table>

Perimeter to be subtracted after \( n = 2 \)

\[ P_{n}^{\text{sml}} = \sum_{k=2, n \geq 2}^{n} 2^{k-1} \left[ 6 \times (N_r)^{n-k} \times \frac{\ell}{7^k} + \frac{2\ell}{7^k} + \frac{3\ell}{7^{k+1}} \left\{ \frac{1 - r^{n-k}}{1 - r} \right\} + \frac{7\ell}{7^n} \left\{ \frac{N^{n-k}}{N - 1} \right\} \right] \]

Net perimeter of the residual area that is used for capacitors

\[ \Delta P_{n}^{R} = 4l_n + P_{n} - 4 \times 2^n \times \frac{\ell}{l_n} - 4 \times P_{n}^{\text{sml}} \]

To summarize the all the fractals, Table 5 summarizes the increase in perimeter-to-area ratios of the three geometries implemented on CMOS process photodiode. The factor

Table 5: Perimeter-to-area Ratio

<table>
<thead>
<tr>
<th>Geometry</th>
<th>Perimeter-to-area ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quadratic Koch Island</td>
<td>( 3^n )</td>
</tr>
<tr>
<td>Koch Island</td>
<td>( 2^n )</td>
</tr>
<tr>
<td>Semi-Fractal</td>
<td>( 2.14^n )</td>
</tr>
</tbody>
</table>

of increase depends of type of generator used and the number of iteration. Due to the
limitation of photolithography resolution and fabrication design rules, we were able to implement a maximum iteration of 3. As the iteration increased the total spread out area (enclosing area) also increased. In these areas, a metal-metal capacitor were fabricated. For $1mm \times 1mm$ photodiode area (initiator area), in the enclosing area we were able to get a total of $400pF$ capacitor. The increased perimeter of these capacitors were able to store more charge in the form of lateral flux, which helped increasing the total capacitance per area. Expression for increased capacitance is discussed in chapter 4.

### 2.3 Boost Converters

A DC-to-DC converter circuit is need to boost the output of the photodiodes. The open-circuit voltage of the diodes are in the range of $0.3V$ to $0.45V$ (depending on illumination conditions). It is necessary to boost these voltages to values beyond to the operating voltages of the sensory circuits. In this section, we discuss the a basic operating principle of an inductor-based boost converter circuit. Figure 17 shows a basic circuitry of a boost converter. The switch used can be a NMOS switch. In the following analysis, we assume the input to be a constant voltage source. The diode is an ideal diode with no voltage drop across it and the on-resistances of the switch is zero.

#### 2.3.1 Circuit Analysis

The circuit function is based on charging and discharging of an inductor. In the charging phase also called as the *on-state*, the switch ($S_1$) is turned on and the inductor is charged by the input voltage source. In the discharging phase also called the *off-state*, the switch ($S_1$) is turned off. In this phase, the inductor discharges through the load capacitor
Figure 17: Boost converter circuit

and load. The diode ($D_s$) stops the load capacitor ($C_L$) from discharging during the on-state.

2.3.1.1 On-State

In this state the switch $S_1$ is turned on. The current flows in the clockwise direction through the inductor ($L$) storing the energy in form of magnetic field. The polarity of the inductor is shown in the figure. For the given closed loop, the current in through the inductor can be given as

$$\frac{\Delta I_L}{\Delta t} = \frac{V_{in}}{L}$$

(2.22)

At the end of on-state the change in current ($\Delta I_L^{ON}$) is given as

$$\Delta I_L^{ON} = \int_0^{DT} dI_L$$

Replacing $I_L$ from 2.22 in the above equation

$$\Delta I_L^{ON} = \int_0^{DT} \frac{V_{in}}{L} dt = \frac{V_{in}}{L} DT$$

(2.23)
where $D$ is the duty cycle of the pulse of frequency $1/T$ that turns the switches on and off. $DT$ is the on time of the circuit. During this phase, $D_s$

### 2.3.1.2 Off-State

In this state switch $S_1$ is turned off. The inductor will be cut off from the input voltage supply, so the current will tend to drop to zero. The inductor trying to maintain the previous state of current will now act like a voltage source to the rest of the circuit. During this phase, the inductor will maintain the same direction direction of current, but as the inductor act as a voltage source, its polarity will change. The inductor will discharge through the load and the rest of the circuit, which will cause its voltage to decrease over time. Also during this time, the capacitor $C_L$ in parallel with the load will charge up to the voltage presented by the inductor. For the given loop, the current can be expressed as

\[
\frac{\Delta I_L}{\Delta t} = \frac{V_{out}}{L}
\]  

(2.24)
At the end of off-state the change in current ($\Delta I_{LOFF}^L$) is given as

$$\Delta I_{L}^{OFF} = \int_{DT}^{T} dI_{L}$$

Replacing $I_L$ from 2.24 in the above equation

$$\Delta I_{L}^{OFF} = \int_{DT}^{T} \frac{V_{out}}{L} dt = \frac{V_{in}}{L} (1 - D) T$$

(2.25)

As the energy remains constant, the current at the end of off-state should be equal to current at the start of on-state. So, the net change in current should be equal to zero.

$$\Delta I_{L}^{ON} + \Delta I_{L}^{OFF} = 0$$

(2.26)

Substituting the values of $\Delta I_{L}^{ON}$ and $\Delta I_{L}^{OFF}$ in 2.26 we get

$$\frac{V_{out}}{V_{in}} = \frac{-D}{1 - D}$$

The “−” suggest that the polarity of output voltage will opposite to that of input voltage. This cycle continues indefinitely and the output voltage delivered to the load will be higher than the input voltage.
In chapter 5, the analysis takes into consideration the on-resistance of the switches and the voltage drop across the diode ($D_s$). Also the input voltage source is replaced by a electrical equivalent photodiode. The modelling of photodiode is also discussed. A new and improved circuit that will help reduce the losses due to the switches and improve the circuit efficiency is also presented.

2.4 Cyclic Analog-to-Digital Converter

As mentioned in chapter 1, we implement a cyclic architecture based analog-to-digital converter (ADC). In this section we discuss the operation of a conventional cyclic ADC. Figure 20 shows a block diagram of the ADC. The advantage of the this architecture is that it requires less amount of analog circuitry as it uses the same circuitry to perform conversions cyclically in time.

Figure 20: Cyclic ADC block diagram
2.4.1 Circuit Operation

The input signal is sampled by the sample and hold block. This sampled signal $S_{in}$ is compared to the reference signal $S_{ref}$ by the comparator block. If $S_{in} > S_{ref}$ then the binary output is "1" else the output will be "0". If the binary output of the previous bit is ($B_N = 1$) then residual signal is computed as $S_{res} = S_{in} - S_{ref}$ else $S_{res} = S_{in} + S_{ref}$. This residual signal is fed into the amplifier with gain 2 and then it is compared to the reference signal. This process continues till the desired number of resolution is achieved. Figure 21 shows the algorithm flow graph of the ADC.

In chapter 6 we discuss detailed architecture of every block used in the ADC. We also mention the modification made in the flow graph algorithm to obtain Golomb-Rice code while the digital conversion process.
START

$S = S_{in}$

$S > 0$

Yes: $B_i = 1$

$S = S_{res} = 2(S_{in} - S_{ref})$

$i = i + 1$

No: $B_i = 0$

$S = S_{res} = 2(S_{in} + S_{ref})$

$i > N$

Yes: STOP

No: $S = S_{res} = 2(S_{in} - S_{ref})$

Figure 21: Cyclic ADC state diagram
CHAPTER 3
PHOTODIODE THEORY AND EXPERIMENT

When light is incident on the diode, there will be electron-hole pairs created throughout \( p^+ \) and \( n^- \) regions. As a result, a reverse bias current will be generated. The electric field in the depletion region will quickly sweep the electrons into the \( n^- \) region and the holes to the \( p^+ \) region. The current contributed by the \( e - h \) pairs generated in the depletion region is called the *Drift Current* (shown in Fig 22).

The \( e - h \) pairs created outside of the depletion region, the minority charges of each region will flow towards the depletion region. The minority charges that successfully make it to the depletion region will be swept across by the electric field. The current generated by the flow of these charges are called *Diffusion Current*.

![Drift Current and Diffusion Current](image)

Figure 22: Drift current and diffusion current

At this point we would like to introduce the term *quantum efficiency* (QE). QE
is the ratio of useful charge collected to the number of photons hitting the surface of photodiode per second. QE mainly depends on the type of material used as photodiode and the wavelength of the incident light. QE can be mathematically represented as

\[
QE = \frac{\text{electrons/sec}}{\text{photons/sec}} = \frac{\text{power/unit area}}{(\text{energy of one photon}) \times (\text{total number of photons in unit area})}
\]

(3.1)

In section 3.1 we derive expression for the current generated by the vertical photodiode. Section 3.2 discusses the current contributed by the lateral diode. In section 3.4 we discuss the experiment performed on these photodiodes and analyse the test results.

### 3.1 Vertical Current 1-D Model

![Figure 23: Vertical diode and lateral diode](image)

The vertical diode, as mentioned before, is spread across the area of the diode. We can assume that the entire diode is illuminated uniformly. In a vertical diode, the rate of generation of electron-hole pair will vary along the depth from the surface of the diode. Hence, we consider a 1-D model in this case.
Assume a monochromatic incident photon flux $F_0 \text{photons/cm}^2 \cdot \text{s}$ at the surface $y = 0$ (Fig. 24). If $F(y)$ is the photon flux at depth $x$ then the number of photons absorbed per second for $\Delta x$ is given by

$$F(y) - F(y + \Delta y) \approx \alpha F(y) \cdot \Delta y \quad (3.2)$$

where $\alpha$ is the absorption coefficient in $\text{cm}^{-1}$ and is dependent on the wavelength. In

```
Figure 24: Flow of electrons and holes
```

limit the Eq. 3.2 is written as

$$\frac{dF(y)}{dx} = -\alpha F(y) \quad (3.3)$$

Solving Eq. 3.3 we get

$$F(y) = F_0 \cdot e^{-\alpha y} \quad (3.4)$$

The generation rate at $y$ is

$$G(y) = \frac{d}{dy}(F_0 - F(y)) = \alpha F_0 e^{(-\alpha y)} \quad \text{e-h pair/cm}^2 \cdot \text{s} \quad (3.5)$$
3.1.1 Drift Current Density

Drift current is due to the electron-hole pair generated in the depletion region. The current density can be expressed as

\[ J_{\text{drift}} = -q \int_{y_p}^{y_n} G(y) \, dy \]

\[ J_{\text{drift}} = q F_0 (e^{-\alpha y_p} - e^{-\alpha y_n}) \quad \text{amp/m}^2 \] \hspace{1cm} (3.6)

3.1.2 Diffusion Current

Diffusion current has two components,

- Current due to holes generated in the n-type quasi-neutral region
- Current due to electrons generated in the p-type quasi-neutral region

**Current due to electrons generated in the p-type quasi-neutral region**

\[ J_{\text{diff}}^{n} = -q D_n \frac{\partial n_p(y,t)}{\partial y} \bigg|_{y=y_p} \] \hspace{1cm} (3.7)

\( n_p \) is photo generated minority carrier density

\( D_n \) is the diffusion constant of electrons (in cm\(^2\)/s)

To get an expression for \( n_p(y) \), we solve the continuity equation

\[ \frac{\partial n_p(y,t)}{\partial t} = D_n \frac{\partial^2 n_p(y,t)}{\partial y^2} + G(y) - R(y) \] \hspace{1cm} (3.8)

\( R(y) \) is the recombination rate = \( \frac{n_p}{\tau_n} \)

For steady state \( \frac{\partial n_p(y,t)}{\partial t} = 0 \), thus

\[ D_n \frac{\partial^2 n_p(y,t)}{\partial y^2} + \alpha F_0 e^{-\alpha y} - \frac{n_p(y)}{\tau_n} = 0 \]
\[ \frac{\partial^2 n_p(y, t)}{\partial y^2} - \frac{n_p(y)}{D_n \tau_n} + \frac{\alpha F_0 e^{-\alpha y}}{D_n} = 0 \] (3.9)

The generic solution is of the form

\[ n_p(y) = Ae^{y/L_n} + Be^{-y/L_n} + Ce^{-\alpha y} \] (3.10)

\[ \frac{\partial n_p(y, t)}{\partial y} = \frac{A}{L_n} e^{y/L_n} - \frac{B}{L_n} e^{-y/L_n} - \alpha Ce^{-\alpha y} \] (3.11)

\[ \frac{\partial^2 n_p(y, t)}{\partial y^2} = \frac{A^2}{L_n^2} e^{y/L_n} - \frac{B^2}{L_n^2} e^{-y/L_n} - \alpha^2 Ce^{-\alpha y} \] (3.12)

Boundary condition for the electrons are given in Table 6

<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( n_p(0) = 0 )</td>
</tr>
<tr>
<td>(b)</td>
<td>( n_p(y_p) = 0 )</td>
</tr>
</tbody>
</table>

For case (a)

\[ -(A + B) = C \] (3.13)

or case (b)

\[ \frac{A}{L_n} e^{y/L_n} - \frac{B}{L_n} e^{-y/L_n} - \alpha Ce^{-\alpha y} = 0 \] (3.14)

From Eq. 3.9

\[ \frac{A^2}{L_n} e^{y/L_n} - \frac{B^2}{L_n} e^{-y/L_n} - \alpha^2 Ce^{-\alpha y} - \frac{A e^{y/L_n} + Be^{-y/L_n} + Ce^{-\alpha y}}{D_n \tau_n} + \frac{\alpha F_0 e^{-\alpha y}}{D_n} = 0 \] (3.15)

For \( y = 0 \) Eq. 3.15 reduces to
\[ \frac{A^2}{L_n} - \frac{B^2}{L_n} - \alpha^2 C - \frac{A + B + C}{D_n L_n} + \frac{\alpha F_0}{D_n} = 0 \]

For boundary condition \( y = 0, A + B + C = 0, \)
\[ \frac{1}{L_n} \left( A + B \right) + \alpha^2 C = -\frac{\alpha F_0}{D_n} \]

From Eq. 3.13
\[ \frac{1}{L_n} (-C) + \alpha^2 C = -\frac{\alpha F_0}{D_n} \]
\[ C = \frac{\alpha F_0 L_n^2}{D_n (1 - \alpha^2 L_n^2)} \quad (3.16) \]

Now Eq. 3.13 and Eq. 3.14 reduces to 2 variable 2 Eqs.
\[ A e^{y_p/L_n} - (A + C) e^{-y_p/L_n} + C e^{-\alpha y_p} = 0 \]
\[ A (e^{y_p/L_n} - e^{-y_p/L_n}) + C (e^{-\alpha y_p} - e^{-y_p/L_n}) = 0 \]
\[ A = \frac{C (e^{-\alpha y_p} - e^{-y_p/L_n})}{2 \sinh(y_p/L_p)} \quad (3.17) \]
\[ B = -(C + A) \quad (3.18) \]

The constants are summarized in Table 7

<table>
<thead>
<tr>
<th>Table 7: Vertical p-act diffusion current constants</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>( C )</td>
</tr>
<tr>
<td>( A )</td>
</tr>
<tr>
<td>( B )</td>
</tr>
</tbody>
</table>
Thus current generated can be expressed as

\[ J_{n_{\text{diff}}}^n = -qD_n \frac{\partial n_p(y, t)}{\partial y} \bigg|_{y=y_p} \]

\[ \frac{\delta n_p(y, t)}{\delta y} \bigg|_{y=y_p} = \frac{A}{L_n} e^{y_p/L_n} - \frac{B}{L_n} e^{-y_p/L_n} - \alpha C e^{-\alpha y_p} \]

Thus the current is

\[ J_{n_{\text{diff}}}^n = -qD_n \left( \frac{A}{L_n} e^{y_p/L_n} - \frac{B}{L_n} e^{-y_p/L_n} - \alpha C e^{-\alpha y_p} \right) \text{ amp/m}^2 \] (3.19)

**Current generated due to holes created in n-region**

\[ J_{p_{\text{diff}}}^p = -qD_p \frac{\partial p_n(y, t)}{\partial y} \bigg|_{y=y_n} \]

Solving the continuity equation for steady state

\[ D_p \frac{\partial^2 p_n(y, t)}{\partial y^2} + \alpha F_0 e^{-\alpha y} - \frac{p_n(y)}{\tau_p} = 0 \]

\[ \frac{\partial^2 p_n(y, t)}{\partial y^2} - \frac{p_n(y)}{D_p \tau_p} + \frac{\alpha F_0 e^{-\alpha y}}{D_p} = 0 \] (3.20)

The generic solution is of the form

\[ p_n(y) = Pe^{y/L_p} + Qe^{(-y/L_p)} + Re^{-\alpha y} \] (3.21)

\[ \frac{\partial p_n(y, t)}{\partial y} = \frac{P}{L_p} e^{y/L_p} - \frac{Q}{L_p} e^{-y/L_p} - \alpha Re^{-\alpha y} \] (3.22)

\[ \frac{\partial^2 p_n(y, t)}{\partial y^2} = \frac{P^2}{L_p} e^{y/L_p} - \frac{Q^2}{L_p} e^{-y/L_p} - \alpha^2 Re^{-\alpha y} \] (3.23)

Boundary condition for holes is given in Table 8

From case (a)

\[ p_n(y_n) = Pe^{y_n/L_p} + Qe^{-y_n/L_p} + Re^{-\alpha y_n} = 0 \]
Table 8: Boundary condition in n-type region

<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( p_n(y_n) = 0 )</td>
</tr>
<tr>
<td>(b)</td>
<td>( p_n(y_p') = 0 )</td>
</tr>
</tbody>
</table>

\[
P e^{y_n/L_p} + Q e^{-y_n/L_p} = -R e^{-\alpha y_n} \tag{3.24}
\]

For case (b)

\[
p_n(y_p') = P e^{y_n'/L_p} + Q e^{-y_n'/L_p} + R e^{-\alpha y_n'} = 0
\]

\[
P e^{y_n'/L_p} + Q e^{-y_n'/L_p} = -R e^{-\alpha y_n'} \tag{3.25}
\]

From Eq. 3.22 and Eq. 3.23

\[
\frac{P^2}{L_p} e^{y/L_p} - \frac{Q^2}{L_n} e^{-y/L_p} + \alpha^2 R e^{-\alpha y} - \frac{P e^{y/L_p} + Q e^{(-y/L_p)} + R e^{-\alpha y}}{D_p \tau_p} + \frac{\alpha F_0 e^{-\alpha y}}{D_p} = 0
\]

\[
\frac{1}{L_p^2} (P e^{y/L_p} + Q e^{-y/L_p}) + \alpha^2 R e^{-\alpha y} - \frac{P e^{y/L_p} + Q e^{(-y/L_p)} + R e^{-\alpha y}}{D_p \tau_p} + \frac{\alpha F_0 e^{-\alpha y}}{D_p} = 0 \tag{3.26}
\]

Applying boundary condition (a) on Eq. 3.26

\[
\frac{1}{L_p^2} (P e^{y_n/L_p} + Q e^{-y_n/L_p}) + \alpha^2 R e^{-\alpha y_n} - \frac{P e^{y_n/L_p} + Q e^{(-y_n/L_p)} + R e^{-\alpha y_n}}{D_p \tau_n} + \frac{\alpha F_0 e^{-\alpha y_n}}{D_p} = 0
\]

Using Eq. 3.24

\[
\frac{1}{L_p^2} (-R e^{-\alpha y_n}) + \alpha^2 R e^{-\alpha y_n} + \frac{\alpha F_0 e^{-\alpha y_n}}{D_p} = 0
\]

\[
R = \frac{\alpha F_0 L_p^2}{D_p (1 - \alpha^2 L_p^2)} \tag{3.27}
\]

From Eq. 3.25

\[
Q = \frac{-R e^{-\alpha y_n'} - P e^{y_n'/L_p}}{e^{-y_n'/L_p}} \tag{3.28}
\]
Further, solving for \( P \)

\[
P = -R e^{-\alpha_y n} - \frac{e^{-\alpha_{y'} n} + \frac{y_n - y_n'}{L_p}}{e^{y_n/L_p} - e^{(2y_n' - y_n)/L_p}}
\]  

(3.29)

| Table 9: Vertical n-well diffusion current constants |
|----------------|---|
| Constant | Value |
| \( R \) | \( \frac{\alpha F_0 L_p^2}{D_p (1 - \alpha^2 L_p^2)} \) |
| \( Q \) | \( -R e^{-\alpha_{y'} n} \frac{e^{y_n/L_p}}{y_{n'}} - \alpha Re^{-\alpha y_n} \) |
| \( P \) | \( -R e^{-\alpha y_n - \alpha_{y'} n} + \frac{y_n - y_n'}{L_p} \) |

Current is expressed as

\[
J_{\text{diff}}^p = -q D_p \left( \frac{P}{L_p} e^{y_n/L_p} - \frac{Q}{L_p} e^{-y_n/L_p} - \alpha Re^{-\alpha y_n} \right) \text{amp/m}^2
\]  

(3.30)

**Current generated in p-sub**

Drift current:

\[
\dot{j}_{\text{drift~p-sub}} = q \int_{y_n}^{y_p'} G(y) dy = q \int_{y_n}^{y_p'} \alpha F_0 e^{-\alpha y} dy = q F_0 (e^{-\alpha y'} - e^{-\alpha y_n})
\]

Diffusion current:

\[
D_n \frac{\partial^2 n_{\text{p-sub}}(y)}{\partial y^2} + \alpha F_0 e^{-\alpha y} - \frac{n_p(y)}{\tau_n} = 0
\]  

(3.31)

The generic solution is of the form

\[
n_{\text{p-sub}}(y) = Ke^{y/L_n} + Me^{-y/L_n} + Ne^{-\alpha y}
\]  

(3.32)

\[
\frac{\partial n_{\text{p-sub}}(y)}{\partial y} = \frac{K}{L_n} e^{y/L_n} + \frac{M}{L_n} e^{-y/L_n} - \alpha Ne^{-\alpha y}
\]  

(3.33)
\[
\frac{\partial^2 n_{\text{psub}}(y)}{\partial y^2} = \frac{K e^{y/L_n}^2}{L_n} + \frac{M e^{-y/L_n}^2}{L_n} + \alpha^2 Ne^{-\alpha y}
\] (3.34)

Boundary condition for electrons is given in Table 10

Table 10: Boundary condition in p-sub region

<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( n_{\text{psub}}(y_p') = 0 )</td>
</tr>
<tr>
<td>(b)</td>
<td>( n_{\text{psub}}(y_w) = 0 )</td>
</tr>
</tbody>
</table>

From (a)

\[
n_{\text{psub}}(y) = Ke^{y_p'/L_n} + Me^{-y_p'/L_n} + Ne^{-\alpha y_p'} = 0
\] (3.35)

From (b)

\[
n_{\text{psub}}(y) = Ke^{y_w/L_n} + Me^{-y_w/L_n} + Ne^{-\alpha y_w} = 0
\] (3.36)

Replacing the general solution into the diffusing current Eq. 3.31

\[
K e^{y/L_n}^2 + M e^{-y/L_n}^2 + \alpha^2 Ne^{-\alpha y} - \frac{Ke^{y/L_n} + Me^{-y/L_n} + Ne^{-\alpha y}}{D_n \tau_n} + \frac{\alpha F_0 e^{-\alpha y}}{D_n} = 0
\]

For \( y = y_p' \)

\[
\frac{1}{L_n} \left( Ke^{y_p'/L_n} + Me^{-y_p'/L_n} \right) + \alpha^2 Ne^{-\alpha y_p'} - \frac{Ke^{y_p'/L_n} + Me^{-y_p'/L_n} + Ne^{-\alpha y_p'}}{D_n \tau_n} + \frac{\alpha F_0 e^{-\alpha y_p'}}{D_n} = 0
\]

Replacing the boundary conditions

\[
N = \frac{\alpha L_n^2 F_0}{D_n (1 - \alpha^2 L_n^2)}
\] (3.37)

\[
K = -N \left( e^{-(\alpha y_p' + w/L_n)} - e^{-(\alpha w + y_p'/L_n)} \right) 
\frac{2 \sinh ((y_p' - y_w)/L_n)}{2 \sinh ((y_p' - y_w)/L_n)}
\] (3.38)
Table 11: Vertical p-sub diffusion current constants

<table>
<thead>
<tr>
<th>Constant</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N$</td>
<td>$\frac{\alpha L_n^2 F_0}{D_n(1-\alpha^2 L_n^2)}$</td>
</tr>
<tr>
<td>$K$</td>
<td>$-N \left( \frac{e^{-(\alpha y'_p+w/L_n)}-e^{-(\alpha w+y'_p/L_n)}}{2 \sinh ((y'_p-w)/L_n)} \right)$</td>
</tr>
<tr>
<td>$M$</td>
<td>$N e^{-\alpha y'_p} + Ke^{y'_p/L_n}/e^{-y'_p/L_n}$</td>
</tr>
</tbody>
</table>

$$M = -\frac{N e^{-\alpha y'_p} + Ke^{y'_p/L_n}}{e^{-y'_p/L_n}}$$ \hspace{1cm} (3.39)

Current is expressed as

$$J^{n}_{diff} = -q D_n \frac{\partial n_{psub}(y,t)}{\partial y}|_{y=y'_p}$$

$$J^{n}_{diff} = -q D_n \left( \frac{K e^{y'_p/L_n}}{L_n} + \frac{M}{L_n} e^{-y'_p/L_n} - \alpha N e^{-\alpha y'_p} \right) \text{amp/m}^2 \hspace{1cm} (3.40)$$

These current equations when plotted with data accrued from [] give the following plot.

### 3.2 Lateral Current 2-D Model

#### 3.2.1 Drift Current

Drift current in depletion region is given as

$$J_{drift} = -q \int_{-x_p}^{x_n} \int_{0}^{y_n} G(y) dy dx$$

$$J_{drift} = q F_0(1 - e^{-\alpha y_n})(x_n + x_p) \text{A/m} \hspace{1cm} (3.41)$$
3.2.2 Diffusion Current

3.2.2.1 Electrons in p-act region

To calculate the diffusion current in the p-region, let’s start with the continuity equation. We consider the minority concentration of electrons changes along both x-axis and y-axis

\[
D_n \left[ \frac{\partial^2 n_p(x, y)}{\partial x^2} + \frac{\partial^2 n_p(x, y)}{\partial y^2} \right] + G(y) - R(x, y) = \frac{\partial n_p(x, y)}{\partial t}
\]

Where \( G(y) = \alpha F_0 e^{-\alpha y} \) and \( R(x, y) = \frac{n_p(x, y)}{\tau_n} \). In steady state \( \frac{\partial n_p(x, y)}{\partial t} = 0 \). Thus

\[
D_n \left[ \frac{\partial^2 n_p(x, y)}{\partial x^2} + \frac{\partial^2 n_p(x, y)}{\partial y^2} \right] + \alpha F_0 e^{-\alpha y} - \frac{n_p(x, y)}{\tau_n} = 0 \quad (3.42)
\]
Boundary condition:

Table 12: Boundary condition in p-act region

<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( n_p(-x_p, 0) = 0 )</td>
</tr>
<tr>
<td>(b)</td>
<td>( n_p(-x_p, y_p) = 0 )</td>
</tr>
<tr>
<td>(c)</td>
<td>( n_p(-x_{pp}, 0) = 0 )</td>
</tr>
<tr>
<td>(d)</td>
<td>( n_p(-x_{pp}, y_{pp}) = 0 )</td>
</tr>
</tbody>
</table>

As the generation term is exponentially proportional to \((-\alpha y)\), we can write \( n_p(x, y) \) as

\[
n_p(x, y) = f(x)e^{-\alpha y}
\]

Let \( f(x) \) be expressed as equation 3.43

\[
f(x) = A \sinh[k_1(x + x_p)] + B \sinh[k_1(x + x_{pp})] + C
\]

(3.43)

Applying boundary condition to equation 3.43

Table 13: Boundary condition in p-act region

<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>( n_p(-x_p, 0) = 0 )</td>
<td>( B = \frac{-C}{\sinh[k_1(-x_p + x_{pp})]} )</td>
</tr>
<tr>
<td>(c)</td>
<td>( n_p(-x_{pp}, 0) = 0 )</td>
<td>( A = \frac{-C}{\sinh[k_1(-x_{pp} + x_p)]} )</td>
</tr>
</tbody>
</table>

\[
\frac{\partial n_p(x, y)}{\partial x} = \frac{\partial f(x)}{\partial x} e^{-\alpha y}
\]

\[
\frac{\partial^2 n_p(x, y)}{\partial x^2} = \frac{\partial^2 f(x)}{\partial x^2} e^{-\alpha y}
\]

\[
\frac{\partial n_p(x, y)}{\partial y} = -\alpha f(x)e^{-\alpha y}
\]
\[ \frac{\partial^2 n_p(x, y)}{\partial y^2} = \alpha^2 f(x)e^{-\alpha y} \]

Equation 3.42 can be written as

\[
D_n \left[ \frac{\partial^2 f(x)}{\partial x^2} e^{-\alpha y} + \alpha^2 f(x)e^{-\alpha y} \right] + \alpha F_0 e^{-\alpha y} - \frac{f(x)e^{-\alpha y}}{\tau_n} = 0
\]

\[
\frac{\partial^2 f(x)}{\partial x^2} + \left( \alpha^2 - \frac{1}{L_n^2} \right) f(x) + \frac{\alpha F_0}{D_n} = 0 \tag{3.44}
\]

Substituting \( \alpha^2 - \frac{1}{L_n^2} = u \) and \( \frac{\alpha F_0}{D_n} = v \) in equation 3.44

\[
\frac{\partial^2 f(x)}{\partial x^2} + uf(x) + v = 0 \tag{3.45}
\]

From equation 3.43 \( \frac{\partial^2 f(x)}{\partial x^2} \) can be expressed as

\[
\frac{\partial^2 f(x)}{\partial x^2} = Ak_1^2 \sinh [k_1(x + x_p)] + Bk_1^2 \sinh [k_1(x + x_{pp})]
\]

Equation 3.45 can be written as

\[
Ak_1^2 \sinh [k_1(x + x_p)] + Bk_1^2 \sinh [k_1(x + x_{pp})] + uA \sinh [k_1(x + x_p)] + uB \sinh [k_1(x + x_{pp})] + uC + v = 0
\]

\[
A \sinh [k_1(x + x_p)] (k_1^2 + u) + B \sinh [k_1(x + x_{pp})] (k_1^2 + u) + uC + v = 0 \tag{3.46}
\]

Apply boundary condition (a) on Eq. 3.46

\[
B \sinh [k_1(x + x_{pp})] (k_1^2 + u) + uC + v = 0
\]

Substituting value of \( B \) from Table 13 case (a)

\[
-C(k_1^2 + u) + uC + v = 0
\]

\[
C = \frac{v}{k_1^2} \tag{3.47}
\]

59
Substituting value of \( C \) from equation 3.47 in value of \( B \) from Table 13 case (a)

\[
B = \frac{-v}{k_1^2 \sinh [k_1(-x_p + x_{pp})]} \tag{3.48}
\]

Substituting value of \( C \) from equation 3.47 in value of \( A \) from Table 13 case (c)

\[
A = \frac{-v}{k_1^2 \sinh [k_1(-x_{pp} + x_p)]} \tag{3.49}
\]

Substituting values of \( A, B \) and \( C \) from equations 3.49, 3.48 and 3.47 respectively into 3.46, we get

\[
\frac{-v \sinh [k_1(x + x_p)]}{k_1^2 \sinh [k_1(-x_{pp} + x_p)]} (k_1^2 + u) + \frac{-v \sinh [k_1(x + x_{pp})]}{k_1^2 \sinh [k_1(-x_p + x_{pp})]} (k_1^2 + u) + u \frac{v}{k_1^2} + v = 0
\]

\[
\frac{\sinh [k_1(x + x_p)]}{k_1^2 \sinh [k_1(-x_{pp} + x_p)]} (k_1^2 + u) + \frac{\sinh [k_1(x + x_{pp})]}{k_1^2 \sinh [k_1(-x_p + x_{pp})]} (k_1^2 + u) - u \frac{1}{k_1^2} - 1 = 0
\]

\[
\frac{(k_1^2 + u)}{k_1^2 \sinh [k_1(-x_{pp} + x_p)]} \{ \sinh [k_1(x + x_p)] - \sinh [k_1(x + x_{pp})] \} - u \frac{1}{k_1^2} - 1 = 0 \tag{3.50}
\]

Substituting \( x = \frac{x_p - x_{pp}}{2} \) in equation 3.50

\[
\frac{(k_1^2 + u)}{k_1^2 \sinh [k_1(-x_{pp} + x_p)]} \left\{ \sinh \left[ k_1 \left( \frac{x_p - x_{pp}}{2} \right) \right] - \sinh \left[ k_1 \left( \frac{x_{pp} - x_p}{2} \right) \right] \right\} - u \frac{1}{k_1^2} - 1 = 0
\]

\[
\frac{2(k_1^2 + u) \sinh [k_1(x_p - x_{pp}/2)]}{k_1^2 \sinh [k_1(-x_{pp} + x_p)]} - u \frac{1}{k_1^2} - 1 = 0
\]

Noting \( \frac{\sinh(x/2)}{\sinh(x)} = \frac{1}{2 \cosh(x/2)} \)

\[
\frac{(k_1^2 + u)}{k_1^2 \cosh [k_1(x_p - x_{pp}/2)]} - u \frac{1}{k_1^2} - 1 = 0
\]

\[
\frac{(k_1^2 + u)}{\cosh [k_1(x_p - x_{pp}/2)]} - u - k_1^2 = 0
\]
\[
\begin{align*}
k_1^2 \left( \frac{1}{\cosh [k_1(x_p - x_{pp}/2)]} - 1 \right) + u \left( \frac{1}{\cosh [k_1(x_p - x_{pp}/2)]} - 1 \right) &= 0 \\
\left( \frac{1}{\cosh [k_1(x_p - x_{pp}/2)]} - 1 \right) (k_1^2 + u) &= 0 \\
(k_1^2 + u) &= 0
\end{align*}
\]
\[
k_1^2 = -u = \frac{1}{L_n^2} - \alpha^2
\]
\[
k_1 = \sqrt{\frac{1}{L_n^2} - \alpha^2} \quad (3.51)
\]

**Special Case :** \( \alpha L_n = 1 \)

\[
u = 0 \Rightarrow \alpha^2 = \frac{1}{L_n^2} \text{ or } \alpha L_n = 1
\]

Equation 3.44 reduces to
\[
\frac{\partial^2 f(x)}{\partial x^2} + v = 0
\]
\[
\frac{\partial^2 f(x)}{\partial x^2} = -v \partial x^2
\]

Double integrating
\[
f(x) = -\frac{v}{2} \cdot x^2 + C_1 x + C_2
\]

Using boundary conditions (a) and (c) we get
\[
f(-x_p) = -\frac{v}{2}(-x_p)^2 - C_1 x_p + C_2 \quad (3.52)
\]
\[
f(-x_{pp}) = -\frac{v}{2}(-x_{pp})^2 - C_1 x_p + C_2 \quad (3.53)
\]

 Subtracting equation 3.52 from 3.53 we get
\[
C_1 = -\frac{v}{2} (x_{pp} + x_p) \quad (3.54)
\]
Substituting value of \( C_1 \) from 3.54 back into 3.52

\[
C_2 = -\frac{v}{2} (x_{pp} \cdot x_p)
\]  

(3.55)

**Current due to electrons in p-act region**

The constants \( A, B \) and \( C \) of \( f(x) \) is summarised in Table 14

<table>
<thead>
<tr>
<th>Constant</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C )</td>
<td>( \frac{\alpha F_0}{D_n k_1^2} )</td>
</tr>
<tr>
<td>( B )</td>
<td>( -\frac{\alpha F_0}{D_n k_1^2 \sinh[k_1(-x_p+x_{pp})]} )</td>
</tr>
<tr>
<td>( A )</td>
<td>( -\frac{\alpha F_0}{D_n k_1^2 \sinh[k_1(-x_{pp}+x_p)]} )</td>
</tr>
</tbody>
</table>

Diffusion current density can be expressed as

\[
\dot{j}_{diff,pact} = -qD_n \frac{\partial n_p(x,y)}{\partial x} \bigg|_{x=-x_p} = -qD_n e^{-\alpha y} (Ak_1 \cosh[k_1(-x_p + x_p)] + Bk_1 \cosh[k_1(-x_p + x_{pp})])
\]

(3.56)

**Current during special case**

Using the values of constants \( C_1 \) and \( C_2 \) as summarised in Table 15 we compute the current for the special case.

\[
\frac{\partial n_p(x,y)}{\partial x} \bigg|_{x=-x_p} = e^{-\alpha y} \left( \frac{\alpha F_0}{D_n} x_p - \frac{\alpha F_0}{2D_n} (x_{pp} + x_p) \right) \Rightarrow \frac{\alpha F_0}{2D_n} (x_p - x_{pp}) e^{-\alpha y}
\]

\[
\dot{j}_{diff,pact} = -q\frac{\alpha F_0}{2} (x_p - x_{pp}) e^{-\alpha y} A/m
\]

(3.57)
Table 15: Constants of $f(x)$ during special case

<table>
<thead>
<tr>
<th>Constant</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>$-\frac{\alpha F_0}{2D_n} (x_{pp} + x_p)$</td>
</tr>
<tr>
<td>$C_2$</td>
<td>$-\frac{\alpha F_0}{2D_n} (x_{pp} \cdot x_p)$</td>
</tr>
</tbody>
</table>

Diffusion current due to holes in N-well region

Diffusion current due to holes in n-region:

$$D_p \left[ \frac{\partial^2 p_n(x, y)}{\partial x^2} + \frac{\partial^2 p_n(x, y)}{\partial y^2} \right] + G(y) - R(x, y) = \frac{\partial p_n(x, y)}{\partial t}$$

Where $G(y) = \alpha F_0 e^{-\alpha y}$ and $R(x, y) = \frac{p_n(x, y)}{\tau_p}$. In steady state $\frac{\partial p(x, y)}{\partial t} = 0$. Thus

$$D_p \left[ \frac{\partial^2 p_n(x, y)}{\partial x^2} + \frac{\partial^2 p_n(x, y)}{\partial y^2} \right] + \alpha F_0 e^{-\alpha y} - \frac{p_n(x, y)}{\tau_p} = 0 \quad (3.58)$$

Boundary condition:

Table 16: Boundary condition in p-act region

<table>
<thead>
<tr>
<th>Case</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>$p_n(-x_n, 0) = 0$</td>
</tr>
<tr>
<td>(b)</td>
<td>$p_n(-x_n, y_n) = 0$</td>
</tr>
<tr>
<td>(c)</td>
<td>$p_n(-x_{nw}, 0) = 0$</td>
</tr>
<tr>
<td>(d)</td>
<td>$p_n(-x_{nw}, y_n) = 0$</td>
</tr>
</tbody>
</table>

As the generation term is exponentially proportional to $(-\alpha y)$, we can write $p_n(x, y)$ as

$$p_n(x, y) = f(x)e^{-\alpha y}$$

Using the same approach as for the diffusion current due to electrons in p-act region and using the boundary conditions given in Table 16, currents are calculated.

$$j_{diff\_nwell} = -qD_pe^{-\alpha y} (Ak_1 + Bk_1 \cosh [k_1(x_n - x_{nw})]) \ A/m \quad (3.59)$$
where $A$, $B$ and $C$ are given in

<table>
<thead>
<tr>
<th>Constant</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C$</td>
<td>$\frac{\alpha F_0}{D_p k_1}$</td>
</tr>
<tr>
<td>$B$</td>
<td>$-\frac{\alpha F_0}{D_p k_1^2 \sinh[k_1(x_n-x_{nw})]}$</td>
</tr>
<tr>
<td>$A$</td>
<td>$-\frac{\alpha F_0}{D_p k_1^2 \sinh[k_1(x_{nw}-x_n)]}$</td>
</tr>
</tbody>
</table>

For special case, using the values of $C_1$, $C_2$ given in Table 18, the current density is

<table>
<thead>
<tr>
<th>Constant</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>$-\frac{\alpha F_0}{2D_p}(x_{nw} + x_n)$</td>
</tr>
<tr>
<td>$C_2$</td>
<td>$-\frac{\alpha F_0}{2D_p}(x_{nw} \cdot x_n)$</td>
</tr>
</tbody>
</table>

$$j_{diff, pact} = -q \frac{\alpha F_0}{2} (x_{nw} - x_n) e^{-\alpha y} A/m$$ (3.60)

### 3.3 Comparison between different structures of diode

Using the current density expression derived in section 3.1 and 3.2 we do a theoretical analysis between performances of different structures of photodiodes that were designed and fabricated using 0.5µm CMOS technology. Each photodiode has a total spread out area of 1mm² but the perimeter of each structure is different. For our simulation we use solar irradiance $G$ (W/m² s nm) provided by American Society for Testing and Materials (ASTM) Terrestrial Reference Spectra for Photovoltaic Performance Evaluation (http://rredc.nrel.gov/solar/spectra/am1.5/). To calculate the photon flux density
$F_0 \ (\text{photons/m}^2 \cdot \text{s})$ from irradiance, $G$, we use eq. 3.61

$$F_0 \left( \frac{\text{photons}}{\text{m}^2 \cdot \text{s}} \right) = G \left( \frac{W}{\text{m}^2 \cdot \text{s} \cdot \text{nm}} \right) \times \lambda(\text{nm}) \times \frac{\lambda(m)}{h(J \cdot \text{s} \cdot \text{c(m/s)}} \quad (3.61)$$

Values in parenthesis in equation 3.61 are the units of each parameter. $h$ is plank’s constant and $c$ is the velocity of light in free space. Fig. 26 shows the spread of the photon flux density over the wavelength of light.

![Figure 26: Photon flux density Vs. wavelength](image)

Two diode structures were fabricated

1. Square (or control) diode

2. Fractal diode
As mentioned above, both structures have the same dye area, thus the current contributed by the vertical diode is same. Fig. 27 shows the total vertical current generated by the photodiodes when the photon flux density (Fig. 26) is incident on the a $1mm \times 1mm$ diode. The total lateral current of a square diode perimeter is shown in fig. 28. Adding vertical and lateral is shown in fig. 29.

For square diode, the lateral current contribution is very minimal, thus adding vertical and lateral current does not change shape of the plot. But as we increase the perimeter by applying fractal based geometries on the square diode, the lateral current contribution increases. Fig. 30 shows the increase in lateral current as number of iteration increases.

Fig. 31 shows the addition of vertical and lateral current for increasing perimeter.
As the number of iteration increase, the contribution of lateral diode become dominant and the current shape changes to that of lateral current.

Fig. 32 shows the percentage of excess current produced with increased perimeter. We fabricated 2 more structures, a stripe type and enclosed fractal type diode. To increase the perimeter of these diodes, we increase the number of stripes in the former and the increase the iteration of the latter. The increased perimeter leads to large lateral current, but at the cost of vertical diode current. In these structures, as we increase the perimeter, we sacrifice a lot of vertical diode area, which are the dominant contributor in the total current. To increase the contribution of the lateral diode, we to increase the perimeter to a extent that our current 0.5µm CMOS technology will not support.
Three chips containing fractal shaped and square shaped photodiodes were fabricated in a 0.5 µm CMOS process. The diodes are implemented as a N-well/P-diff junction that sits on a p-substrate. Figure 106 shows the photodiodes geometries fabricated. The diodes were tested by exposing them to lights of different wavelength within the visible spectrum. I-V plots were measured for every wavelength for each structures.
3.4.1 Experiment Setup

This experiment is performed to find the response of the solar cell to different wavelength of the visible spectrum. As the absorption coefficient $\alpha$ varies with wavelength, it is necessary to find the response of solar cell when illuminated with light of different wavelength. We also check the response under the normal sunlight. The experimental setup is shown in Fig. 34, consists of an optical table, a laser source that can be tuned to different wavelengths, a collimator lens, a tunable optical power meter, a source meter (Keithley 2400) and a computer to accrue data from the source meter.

The laser source is tuned to a particular wavelength and its output power is measured with the power meter tuned to the same wavelength. The collimator lens is used
give a flat distribution of light. The power sensor of the power meter is mounted on a flexible mount because once it measures power, it has to removed from the line of sight between the laser and the chip. The fabricated chip was mounted on a firm support as we do not want the chip to move while the experiment is conducted. Leads from the chip are connected to a solder-less bread board.

The I-V curve for each diode was acquired using the source meter. The diode junction voltage is swept by the source meter from $-0.3\, V$ to $0.5\, V$ with $0.8\, mV$ steps and the resulting diode current was measured. To minimize noise, 1000 sweeps were performed and averaged to obtain a cleaner I-V curve. This procedure was repeated for all the diodes for the wavelengths of: $488\, nm$, $520\, nm$, $568\, nm$ and $647\, nm$. These measurements were also performed with direct sunlight too.
3.4.2 Measurement Results

Figures 35 and 36 shows the I-V curves of the fractal and rectangular photodiodes when they are illuminated with four different visible spectrum wavelengths. The measured laser output power varied for different wavelengths, hence we normalized the data and plotted the charges collected, for the incident power. From the I-V curves we observe that the fractal photodiode consistently collects a larger photo-current than the rectangular diode. In the figures the voltage range of interest when the photodiode works as a solar cell is shown. Beyond $0.5 \, V$ we observe the exponential behavior typical of a forward-biased diode. For negative bias voltages the photodiode still outperforms the rectangular one. The conversion efficiency of both diodes was also computed and compared. The
photon flux, $F_0$, for each wavelength was calculated using the following equation:

$$F_0 = \frac{P_w}{A} \frac{1}{E_{ph}}$$

(3.62)

where, $P_w$ is the output power of the laser, $A$ is the cross area of the laser beam and $E_{ph}$ is the photon energy at a particular wavelength. is given by:

$$E_{ph} = \frac{h \cdot c}{\lambda}$$

(3.63)
Finally, the conversion efficiency was estimated using:

\[ \eta = \frac{I_{\text{diode}}}{qA_{\text{diode}}F_0} \times 100\% \quad (3.64) \]

where \( q \) is the electron charge, \( A_{\text{diode}} \) is the area of the diode and \( I_{\text{diode}} \) is the diode current in the region of interest (the current is fairly constant in this region). Figure 37 and 38 shows the computed conversion efficiency of both diodes for the different wavelengths at which measurements were taken. At 514 nm the proposed fractal photodiode is up 10% more efficient than the rectangular one in Fig. 37. A spectral response of both diodes is also observed that is consistent with the theoretical efficiency calculations of silicon diodes [12].

The I-V curves for both diodes were also measured under sunny outdoor conditions to simulate a practical energy-harvesting scenario. These I-V curves are shown in Fig. 39. The incident light power was measured with a broadband optical power meter.
Figure 35: Charge collected per unit area for different wavelengths (chip 1)

(Scientech 361) to be 100 mW. The detector area of this meter is $6.157 \times 10^{-4} \text{m}^2$. The photon flux was then calculated using Eq. 3.62 and found to be $4.536 \times 10^{20} \text{photons/m}^2 \cdot \text{s}$. In this calculation we employed $\lambda = 555 \text{nm}$ which is the standard for white light photometry. The efficiency for the rectangular photodiode turned out to be 35% and the efficiency of the fractal photodiode 41%. Thus a 6% overall improvement was achieved by the designed fractal diode. Larger improvements in efficiency can still be achieved if a second or third iteration of the chosen fractal is employed to further increase the diode perimeter.
Figure 36: Charge collected per unit area for different wavelengths (chip 2)

Figure 37: Efficiency curve for all wavelengths for quadratic Koch island fractals
Figure 38: Efficiency curve for all wavelengths for modified fractals

Figure 39: I-V curve recorded under sun
CHAPTER 4

LATERAL CAPACITANCE

Capacitors are an important component in integrated circuits. Capacitors are used in data converters, switch capacitor circuits, sample and hold circuits to name a few. Capacitors occupy considerable amount of area, hence area efficient capacitors are desirable. Current CMOS technology gives four types of capacitors: gate capacitors, junction capacitors, thin insulator capacitors and metal-to-metal capacitors. The gate and junction capacitors have high capacitance per unit area but are very non-linear and need extra biasing voltage to operate. Thin insulator capacitors use a thin oxide to achieve high density [10]. The capacitance density is much higher than standard metal-to-metal capacitors, but the need for additional masks and process steps make these capacitors expensive. A standard metal-to-metal capacitors are very linear and exhibit low dependence on temperature. The density of these capacitors are very low because of the thick oxide layer between them. With technology scaling the vertical spacing remains constant, thus the capacitor continues to occupy more area dye area. Hence, with given technology constrains, we need to design capacitor with high capacitance per area. One approach on achieving higher capacitance can be by increasing the later flux capacitors.

A capacitor characteristically has two electrical field of lines: vertical and lateral (Fig. 40). The design rule constrains (DRC) of the standard CMOS technology states that the area of the bottom plate of a metal-to-metal capacitor should be more than the top
plate. According to the DRC there should be a minimum distance of $0.5\mu m$ between the edges of two metals. This provides more lateral area providing an opportunity to exploit the lateral capacitance more effectively. Figure 41 shows a 3-D view of a metal-to-metal capacitor fabricated in CMOS technology with field lines. The vertical field lines (shown in black in Figure 41) gives rise to parallel plate capacitance which can be calculated using the classic equation 4.1.

$$C_{Total} = \frac{\varepsilon_0 \cdot \varepsilon_{SiO_2} \cdot \Delta A}{H}$$ (4.1)
$\varepsilon_0$ is permittivity of free space. Scaling in technology doesn’t change the distance between the plates ($H$) and silicon dioxide ($SiO_2$) is the standard inter-level oxide layer with $\varepsilon_{SiO_2} = 3.9$. So, with all the parameters constant, the capacitance is directly proportional to the area $\Delta A$. Thus, exploiting the lateral flux capacitance becomes important. As discussed in section 2.2 the residual area around the photodiode can be utilized to fabricate metal-to-metal capacitors. Capacitors filling these areas will have partial fractal structures, giving more perimeter compared to a regular square or rectangular shaped capacitor of same area. Section 2.2 derives expressions for the lateral length of the residual area. In section 4.1 we study the lateral electric field lines and derive an expression for fringe capacitance per unit length.

### 4.1 Fringe Capacitance

Fringe capacitance exists along the perimeter of the top and the bottom plate. The lateral electric field line density is shown in Figure 42. To derive an approximate expression for fringe capacitance let us consider the following case where two conductors placed close to each other and have the electric field lines as shown in Figure 43.

To calculate the capacitance, we can transform the elliptical system to a parallel plate system using conformal mapping [7], [48]. We need to transform the existing elliptical system to a confocal elliptical system. This can be done by

$$f = \sqrt{(S^2 - H^2)} \quad if \quad S > H$$
Figure 42: Electric field lines of a fringe capacitance

\[ f = \sqrt{(H^2 - S^2)} \quad \text{if} \quad H > S \]

\( f \) being the focus of the inner most ellipse.

The outermost ellipse is represented as

\[
\frac{x^2}{(S + W')^2} + \frac{y^2}{(H + T')^2} = 1 \tag{4.2}
\]

\( T' \) is the thickness and \( W' \) is the width of the equivalent transformed confocal elliptical system. \( W' \) can be determined my equating the foci of innermost and the outermost ellipses and is expressed as

\[
\sqrt{(S + W')^2 - (H + T')^2} = \sqrt{S^2 - H^2}
\]

\[
W' = \sqrt{T'^2 + 2HT' + S^2 - S} \tag{4.3}
\]
The electric field lines in the transformed system are represented as a confocal ellipse system and the electric potential contours are represented as confocal hyperbolas (Figure 45). This system can be transformed to an equivalent parallel plate system by transforming $xy$ coordinate to $uv$ coordinate system by

$$u + jv = F(x + jy)$$

From $[ ]$, $F = \cos^{-1}$ is a function that can be used to map elliptical geometry to linear geometry.

$$\cos(u + jv) = (x + jy)$$

$$\cos u \cdot \cosh v - j \sin u \cdot \sinh v = (x + jy)$$

$$x = \cos u \cdot \cosh v \quad (4.4)$$

$$y = -\sin u \cdot \sinh v \quad (4.5)$$
Eq. 4.4 and 4.5 can be written as

\[
\cos u = \frac{x}{\cosh v} \tag{4.6}
\]
\[
\sin u = \frac{-y}{\sinh v} \tag{4.7}
\]

Squaring Eq. (4.6) and (4.7) and adding them

\[
\cos^2 u + \sin^2 u = \left( \frac{x}{\cosh v} \right)^2 + \left( \frac{-y}{\sinh v} \right)^2
\]
\[
1 = \frac{x^2}{\cosh^2 v} + \frac{y^2}{\sinh^2 v}
\]

Using the expression \( \cosh^2 v = \sinh^2 v + 1 \), we have

\[
\frac{x^2}{\sinh^2 v + 1} + \frac{y^2}{\sinh^2 v} = 1
\]
Multiplying both sides with $\sinh^2 v + 1$ gives

$$x^2 + y^2 \left( \frac{\sinh^2 v + 1}{\sinh^2 v} \right) = \sinh^2 v + 1$$

$$x^2 + y^2 + \left( \frac{y^2}{\sinh^2 v} \right) = \sinh^2 v + 1$$

rearranging

$$\frac{y^2}{\sinh^2 v} + (x^2 + y^2 - 1) - \sinh v = 0$$

Let $\lambda = \sinh^2 v$

$$\left( \frac{y^2}{\lambda} \right) + (x^2 + y^2 - 1) - \lambda = 0$$

Multiplying both sides with $\lambda$ gives

$$-\lambda^2 + (x^2 + y^2 - 1)\lambda + y^2 = 0$$
This is form of quadratic equation, \( A\lambda^2 + B\lambda + C = 0 \) with \( A = 1 \), \( B = (x^2 + y^2 - 1) \), \( C = y^2 \) and the solution for \( \lambda \) is given by

\[
\lambda = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}
\]

\[
sinh^2 v = \lambda = \frac{x^2 + y^2 - 1}{2} \pm \sqrt{\left(\frac{x^2 + y^2 - 1}{2}\right)^2 + y^2}
\]

\[
v = sinh^{-1} \left[ \frac{x^2 + y^2 - 1}{2} \pm \sqrt{\left(\frac{x^2 + y^2 - 1}{2}\right)^2 + y^2} \right]
\]  

(4.8)

Similarly solving Eq. 4.6 and 4.7 for \( u \) we get

\[
u = \cos^{-1} \left[ \frac{x^2 + y^2 + 1}{2} \pm \sqrt{\left(\frac{x^2 + y^2 + 1}{2}\right)^2 + x^2} \right]
\]  

(4.9)

After transforming the elliptical system into rectangular system (see Figure 46), becomes a finite parallel plate of length \( u_m - u_1 \) and with a spacing of \( v_n - v_1 \).

The capacitance can be expressed as

\[
C_{\text{fringe}} = \varepsilon_d \frac{v_n - v_1}{u_m - u_1}
\]  

(4.10)

\( \varepsilon_d \) is the permittivity of the dielectric between the two conductors. As seen from Fig. 2.10, \( u \) varies from 0 to \( \pi/2 \).

\[
u_m - u_1 = \frac{\pi}{2}
\]  

(4.11)

\( v_1 \) corresponds to the innermost ellipse and can be computed by replacing \( x = S/f \) and...
$y = 0$ in Eq. 4.8 and $v_n$ corresponds to the outermost ellipse and can be computed by replacing $x = (S + W')/f$ and $y = 0$.

$$v_1 = \sinh^{-1} \left( \frac{(S/f)^2 - 1}{2} \pm \sqrt{\left( \frac{(S/f)^2 - 1}{2} \right)^2} \right)$$

$$v_1 = \sinh^{-1} \left( \frac{S}{f} \right)^2 - 1 ; v_1 = \sinh^{-1} 0 = 0$$

Neglecting $v_1 = 0$,

$$v_1 = \sinh^{-1} \frac{H}{f}$$

Similarly,

$$v_n = \sinh^{-1} \frac{H + T'}{f}$$
Therefore

\[ v_n - v_1 = \sinh^{-1} \frac{H + T'}{f} - \sinh^{-1} \frac{H}{f} \]

Using the expression \( \sinh^{-1} x = \ln \left[ x + \sqrt{x^2 + 1} \right] \)

\[ v_n - v_1 = \ln \left[ \frac{H + T'}{f} + \sqrt{\left( \frac{H + T'}{f} \right)^2 + 1} \right] - \ln \left[ \frac{H}{f} + \sqrt{\left( \frac{H}{f} \right)^2 + 1} \right] \]

after simplification we get

\[ v_n - v_1 = \ln \left[ \frac{H + T' + \sqrt{S^2 + T'^2 HT'}}{S + H} \right] \] (4.14)

Replacing Eq. 4.11 and Eq. 4.14 in Eq. 4.10

\[ C_{fringe} = \frac{\varepsilon_d}{\pi/2} \ln \left[ \frac{H + T' + \sqrt{S^2 + T'^2 HT'}}{S + H} \right] \] (4.15)

Eq. 4.15 is the approximate expression for fringe capacitance between two conductors.

Note that as \( S \rightarrow 0 \), \( C_{fringe} \) increases. For \( S = 0 \), Eq. 4.15 reduces to

\[ C_{fringe} = \frac{\varepsilon_d}{\pi/2} \ln \left[ \frac{H + T' + \sqrt{T'^2 + HT'}}{H} \right] \] (4.16)

In Eq. 4.16 we need to determine \( T' \) accurately to get a good estimate of the fringe capacitance. We can represent \( T' = \eta T \), where \( \eta \) is an empirical parameter. \( \eta \) can be empirically expressed as

\[ \eta = \exp \left( \frac{W + S - \sqrt{S^2 + T^2 + 2HT'}}{\tau H} \right) \] (4.17)
$\tau$ is a fitting parameter independent of geometry. The value of $\tau$ is found out to be 3.7 [7].

Total capacitance of a parallel plate capacitor can be expressed as

$$C_{total} = C_{parallel} \times Area + C_{fringe} \times Perimeter$$  \hspace{1cm} (4.18)

As the iteration of the fractal based photodiode increases, the perimeter of the capacitor will also increase almost the with same proportion as shown in fig. 47.

![Figure 47: Perimeter of capacitor Vs Iteration](image)
CHAPTER 5

BOOST CONVERTER

This chapter addresses the problem of on-chip solar energy harvesting and present a circuit that can be employed to generate high voltages from integrated photodiodes. Photodiode stacking is avoided using DC-DC converters. Switched-capacitor and switched-inductor DC-DC converters are evaluated. The effect of parasitic photodiodes is addressed and a solution to minimize their impact is presented. A theoretical analysis of a switched-inductor DC-DC converter is carried out and a mathematical model of the energy harvester is developed. Measurements taken from a fabricated integrated circuit are presented.

5.1 On-chip Solar Cell

As discussed in section 2.1, an Nwell/Pdiff configuration diode can be used as a solar cell in standard CMOS process. Figure 48 shows a cross-sectional view of the photodiodes. As shown in the figure, a parasitic diode \( D_2 \) exists between Nwell/Psub region. When light is incident on the photodiode, electron-hole pairs are formed all over the region. The holes generated in Nwell region try to diffuse through the depletion regions of \( D_1 \) and \( D_2 \) into Pdiff and Psub regions respectively. Similarly the electrons generated in Pdiff and Psub regions try to diffuse into Nwell region. If the Psub is left floating, we can collect more number of charges, thus more current is generated. This sounds tempting but, as the Psub is shared by rest of the circuit components on the chip,
depriving the Psub with electrons may effect the normal functioning of rest of the chip. Hence, the Psub has to be grounded.

A common feature of most DC-DC converter architectures is that the input voltage source, the converter and the load need to have a common ground as illustrated in Fig. 49. As a result when the voltage source is replaced with on-chip photodiode $D_1$ the photodiode’s cathode, or equivalently the N-well, has to be tied to ground. Short circuiting Nwell/Psub to ground, reduces the depletion region potential across diode $D_2$ and all the holes generated in the Nwell region flows to ground and thus less charges is collected across Nwell/Pdiff. To demonstrate this effect, current vs. voltage (I-V) curve was measured for a photodiode of size $982\mu m \times 1047\mu m$ under direct sunlight illumination conditions. Measurement was taken for $D_1$ when the N-well is tied to ground and when it is left floating. Fig. 51 shows the measured I-V curve of a P-diff/N-well. The I-V curves were measured with a source meter (Keithley 2400). As observed, the current through $D_1$ is significantly higher when the N-well is left floating than when it is tied to ground. Hence, more energy can be harvested if the N-well is left floating than if it is tied to ground. To take advantage of this observation, DC-DC converters will have to be modified to maximize the energy that can be harvested from the photodiode.

### 5.2 Energy Harvesting Circuits

The losses due to the parasitic diode $D_2$ can be avoided by using a circuit that isolates the load circuit from the photodiode. The load isolation can be accomplished employing a flying capacitor or with a flying inductor. The flying capacitor or inductor
is employed to store and transfer energy from the photodiode to the load while providing isolation. Thus, connecting the N-well of the parasitic diode $D_2$ to ground is avoided.

The capacitor-based energy harvesting circuit is shown in Fig. 52 while the inductor-based energy harvesting circuit is shown in Fig. 53. In both cases a two phase non-overlapping clock with phases $\phi_1$ and $\phi_2$ and extra switches ($M_1$ to $M_4$) are needed. During phase $\phi_1$ the energy storage element (capacitor or inductor) is charged by connecting it in parallel with the photodiode $D_1$. During phase $\phi_2$ the energy stored in the capacitor or the inductor is transferred to the load. In the flying inductor circuit one of the switches is replaced with a diode ($D_s$) to avoid energy transfer from the load side to the photodiode side when the inductor is in charging phase.

A feature of the inductor-based over the capacitor-based harvesting circuit is that
the former has the ability to boost the photodiode’s inherently low voltage and directly generate the voltage level required by the load. On the other hand, the capacitor-based circuit has be modified to generate high voltages. A series-parallel charge pump, for instance, can be employed to boost the photodiodes voltage. In the following section we analysis both capacitor and inductor based boost circuit.

5.3 Circuit Analysis

An analysis of the energy harvesting circuit is necessary to optimize it and to provide an insight into its operation. However, analysis done in section 2.3 assumed an ideal voltage source but in our case the input is a photodiode which has an unique non-linear characteristic that introduces effects that are not present in the design of standard charge pump/boost converter circuits. To simplify the analysis of a charge pump/boost converter with a photodiode, the photodiode is sometimes modelled as a constant current
Figure 50: Cross-section diagram of on-chip photodiodes and their connection to a DC-DC converter.

source [85], a piece-wise linear circuit [84] or it is assumed to operate in close proximity of the maximum power point (MPP) [18]. In this work we carry out an analysis that does not make these assumptions, resulting in a more generic model that allows us to estimate more precisely the performance of the proposed energy harvesting circuit. Our analysis is then employed to find the conditions that optimize the operation of the energy harvester.

5.3.1 Photodiode Model

Our analysis requires an accurate model of the photodiode. A photodiode working in the photo-voltaic mode is typically modeled using the equivalent circuit shown in Fig. 54 [86]. We will use the model in Fig. 54 in our analysis and simulations to assess the performance of the proposed energy harvesting circuit. The photodiode’s model
Figure 51: Measured I-V curves of a P-diff/N-well photodiode ($D_1$) under direct sun illumination conditions when the N-well is left floating and when it is tied to ground.

includes a current source, $I_{ph}$, that represents the photogenerated current. $I_{ph}$ is a function of the illumination intensity and when $R_s$ is close to zero, it can be approximated by the photodiode’s short-circuit current. The equivalent circuit also includes a diode to model the typical knee in the I-V curve. The current through this diode is given by $I_d=I_s(e^{V_d/nV_T} - 1)$, where $I_s$ is the reverse saturation current, $n$ is the diode ideality factor and $V_T$ is the thermal voltage. The thermal voltage is defined as $V_T=k_bT_C/q$ where $k_b$ is Boltzmann’s constant, $T_C$ is the photodiode’s temperature and $q$ is the electron charge. $V_d$ is the voltage across the diode. The capacitor represents the photodiode’s junction capacitance $C_j$. The resistance $R_{sh}$ is a shunt resistance that models the load presented to the current harvested near the edges of the device and $R_s$ is the diode’s series resistance.
due to the device contacts and connections [64].

The model parameters can be extracted from measured I-V curves using curve fitting [27] or iterative techniques [35]. To extract the photodiode model parameters, the I-V curve shown in Fig. 51 (with the N-well floating) is used. Given that an I-V curve is a DC measurement, the capacitor $C_j$ can be assumed to be an open circuit when performing the I-V curve based parameter estimation. Considering $C_j$ as an open circuit and using the iterative technique presented in [35] yields the following parameter values: $I_{ph}=52.3 \, \mu A$, $R_{sh}=1 \, M\Omega$, $n=1.15$, $I_s=1 \, pA$ and $R_s=0 \, \Omega$. The junction capacitance $C_j$ is a function of the
diode voltage $V_d$. To simplify our analysis, the value of $C_j$ is approximated with its zero-bias value $C_{j0} \times A$, where $C_{j0}$ is the zero-bias capacitance per unit area of the P-diff/N-well junction and $A$ is the area of the photodiode. Circuit simulations show that the error introduced by the zero-bias $C_j$ approximation is very small. The fabricated photodiode has an area of $982 \, \mu m \times 1047 \, \mu m$, which yields an estimated junction capacitance value of $C_j = 735 \, pF$. Fig. 55 shows the measured and modelled I-V curves.

5.3.2 Maximum Power Point (MPP) Calculation

The efficiency of the energy harvester circuit will be evaluated using the following expression [78]:

$$
\eta = \frac{P_{out}}{P_{in,max}} \times 100\% = \frac{V_{out} \times I_L}{V_{mpp} \times I_{mpp}} \times 100\% \quad (5.1)
$$
where, $V_{mpp}$ and $I_{mpp}$ are the photodiode’s voltage and current at the MPP, $P_{in,max} = V_{mpp} \times I_{mpp}$ is the maximum power that the photodiode can provide, and $P_{out} = V_{out} \times I_L$ is the power delivered to the load.

An analytical expression that calculates an approximate value for the MPP has been derived in [66]. The approximate MPP value is within a neighborhood $\varepsilon$ of the true MPP, where $\varepsilon = nV_T$. In this section, a simple analytical expression that predicts the MPP with a slightly better accuracy than the expression provided in [66] is derived. The derived MPP expression allows for more accurate estimations of $P_{in,max}$.

From Fig. 54 and taking into account that $R_s = 0$, the following expression for the photodiode power can be written:

$$P_{in} = V_{D1} \times I_{D1} = V_{D1} \left[ I_{ph} - I_s \left( e^{V_{D1}/nV_T} - 1 \right) - \frac{V_{D1}}{R_{sh}} \right] \quad (5.2)$$
Making $\partial P_{in}/\partial V_{D1} = 0$ and considering $R_{sh} \approx \infty$ results in:

$$I_s e^{V_{D1}/nV_T} \left(1 + \frac{V_{D1}}{nV_T}\right) = I_{ph} + I_s$$

Equation (5.3) can be solved using the Lambert-W function [13] to yield:

$$V_{mpp} = nV_T \times W(a) - nV_T$$

and

$$I_{mpp} = I_{ph} + I_s - \frac{I_s \times a}{W(a)}$$

where, $W(\cdot)$ is the Lambert-W function and $a = e^1 \times \left(\frac{I_{ph} + I_s}{I_s}\right)$. Fig. 56 shows the photodiode output power as given in (5.2) for different photocurrent, $I_{ph}$, levels. The
MPP estimated by equation (5.4) are marked in the figure with dots. A comparison with the MPP value estimated by the analytical expression provided in [29] is also shown. Notably, the MPP expression derived above provides a slightly better estimation of the MPP.

Figure 56: Photodiode output power as a function of the photodiode voltage $V_{D1}$ for different values of the photo-generated current. The estimated location of the MPP is marked with dots.

Assuming $R_{sh} = \infty$ for simplicity, the open-circuit voltage of the photodiode can
be found to be:

$$V_{oc} = nV_T \log \left( \frac{I_{ph} + I_s}{I_s} \right)$$  \hspace{1cm} (5.6)

### 5.4 Charge Pumps

In our analysis we replace the diode $D_p$ with the model presented in Fig. 54. The transistors are modeled by the transistors’ ON resistance $R_{on}$, which is assumed to be equal for both transistors since the transistors’ source voltages are either ground or close to ground. For our analysis we assume the load to be a load capacitor $C_L$ parallel to a resistor $R_L$.

#### 5.4.1 Circuit Analysis at $\phi_1 = 1$

In Fig. 57, the photodiode $D_p$ charges the capacitor $C_c$. Applying KVL in loop, we get

$$V_D = V_C + 2R_{on} \times I_C$$  \hspace{1cm} (5.7)

To find the current expression we differentiate eq. 5.7 w.r.t time and rearranging

Figure 57: One stage charge pump at $\phi_1 = 1$
the terms, we get

\[
\frac{dV_C}{dt} = \frac{dV_d}{dt} - 2R_{on} \times \frac{dI_C}{dt}
\]  

(5.8)

Applying KCL to the loop, we have

\[
I_C = I_{ph} - I_d - I_{Rsh}
\]

(5.9)

Current through diode \(I_d\) can be expressed as \(I_s \left( e^{V_d/nV_T} - 1 \right) \), \(I_s\) being the dark current of the photodiode. Current \(I_{Rsh}\) can be expressed as \(V_d / R_{sh}\). Replacing these values in eq. 5.9, we express \(I_C\) as

\[
I_C = I_{ph} - I_s \left( e^{V_d/nV_T} - 1 \right) - \frac{V_d}{R_{sh}}
\]

(5.10)

To calculate the value of \(dI_C/dt\), we can

\[
\frac{dI_C}{dt} = \frac{dI_C}{dV_d} \times \frac{dV_d}{dt}
\]

Differentiating eq. 5.10 w.r.t \(V_d\),

\[
\frac{dI_C}{dV_d} = - \frac{I_s}{nV_T} e^{V_d/nV_T} - \frac{1}{R_{sh}}
\]

Thus \(dI_C/dt\) is expressed as

\[
\frac{dI_C}{dt} = - \left[ \frac{I_s}{nV_T} e^{V_d/nV_T} + \frac{1}{R_{sh}} \right] \frac{dV_d}{dt}
\]

(5.11)

Replacing eq. 5.11 in eq. 5.8 and simplifying we get

\[
\frac{dV_d}{dt} = \frac{I_{ph} - I_s \left( e^{V_d/nV_T} - 1 \right) + \frac{V_d}{R_{sh}}}{c \left[ 1 + 2R_{on} \left\{ \frac{I_s}{nV_T} e^{V_d/nV_T} - \frac{1}{R_{sh}} \right\} \right]}
\]

(5.12)
5.4.2 Circuit Analysis at $\phi_2 = 1$

Fig. 58 shows the equivalent circuit of In this phase the charged capacitor discharges through the load. Applying KCL for the loop, we get

$$I_L = I_C - I_{CL}$$  \hspace{1cm} (5.13)

Applying KVL for the loop

$$V_C = V_L + 2R_{on}I_C$$  \hspace{1cm} (5.14)

Differentiating eq. 5.14 w.r.t. $dt$, we get

$$\frac{dV_C}{dt} = \frac{dV_L}{dt} + 2R_{on}\frac{dI_C}{dt}$$  \hspace{1cm} (5.15)

Current $I_L$ through load capacitor $C_L$ can be expressed as

$$I_{CL} = C_L \frac{dV_L}{dt}$$

Replacing $I_{CL}$ from eq. 5.13, we get

$$\frac{dV_L}{dt} = \frac{I_C - I_L}{C_L}$$  \hspace{1cm} (5.16)
Current $I_C$ through charging capacitor can also be expressed as

$$I_C = -C \frac{dV_C}{dt} \quad (5.17)$$

The $-$ sign indicates that the capacitor is discharging. Rearranging eq.5.17 we get

$$\frac{dV_C}{dt} = -\frac{I_C}{C} \quad (5.18)$$

Replacing eq. 5.16 and 5.18 into eq. 5.15 and simplifying it, we get

$$\frac{dI_C}{dt} = \frac{I_L}{2R_{on}^2 \frac{C}{C+C_L}} - \frac{I_C}{2R_{on}^2 \frac{C}{C+C_L}} \quad (5.19)$$

Solving the differential eq. 5.19, we get

$$I_C = \beta - (\beta - I_C(0)) e^{-\frac{t}{\alpha}} \quad (5.20)$$

where

$$\alpha = \frac{1}{2R_{on}^2 \frac{C}{C+C_L}}$$

$$\beta = \frac{C}{C+C_L} \frac{C}{2R_{on}^2 \frac{C}{C+C_L}}$$

and the initial current of charging capacitor $I_C(0)$ is defined as

$$I_C(0) = \frac{V_{C1} - V_{L1}}{2R_{on2}}$$

Thus being the initial voltage at $C_L$.

Using the above derived equations, we predict the output of the charge pump under different conditions. We vary the switching frequencies, with 50% duty cycle, and the charging capacitance $C_C$. Fig. 59 shows a approximate output voltage prediction.
Figure 59: Simulation output of single stage charge pump at different switching frequencies and different $C_C$ values.

5.4.3 Hardware Measurements

To test the concept of energy harvesting using on-chip solar cells, an integrated circuit (IC) was designed and fabricated using a 0.5 $\mu$m standard CMOS fabrication process. The IC includes a rectangular P-diff/N-well photodiode, a capacitor bank and NMOS transistor switches. A photograph of the integrated circuit is shown in Fig. 60. The area of the photodiode is 982 $\mu$m $\times$ 1047 $\mu$m. The fabricated IC is an experimental microchip and includes photodiodes of different geometries for experimental purposes. The switches were covered with a metal layer to prevent light from affecting their behavior. The integrated capacitors are combined in parallel to create charging $C_C$ and load capacitors $C_L$. 
Figure 60: Photograph of fabricated CMOS integrated circuit. The integrated circuit contains a P-diff/N-well photodiode, a capacitor bank and NMOS transistor switches. The switches are covered by a metal layer to protect them from light.

5.4.4 Test Setup

A printed circuit board (PCB) (shown in fig.61) was designed and fabricated to host the fabricated microchip. The PCB includes a CPLD that is employed to generate a clock signal with variable frequency. A test setup was built to collect measurements. Fig. 62 shows a diagram of the test setup. A white LED was employed as the light source. The light source is connected to a power supply whose current output can be regulated to control the intensity of the light beam. The PCB is mounted in front of the light beam and the output voltage of the energy-harvesting circuit is monitored with an oscilloscope. To measure $I_{ph}$, the photodiode is disconnected from the energy-harvesting circuit and connected to a source meter (Keithley 2400). The I-V curve of the photodiode is then measured with the source meter. $I_{ph}$ is taken as the photodiode current at 0 V bias. A $1M\Omega$ resistor parallel to $200pF$ capacitor was used as load.
5.4.5 Measurements (Charge pump)

A combination of four charging capacitors with four switching frequencies were measured. Fig.63 shows the output of a single stage charge pump. We observe, with increase in switching frequency, the output of the charge pump does not depend on the charging capacitor $C_C$. Using high switching frequency is not efficient, as the power spent of generating such high switching frequency would be more than power delivered by the charge pump.

However, higher output voltage can be generated by using multiple stages of charging and discharging. Fig.64 show 2-stage implementation. The output voltage is $2 \times$ of the 1-stage charge pump. The difference is operation is that in Phase I ($\phi_1$), both $C_C$’s are charged in parallel, charging them to same voltage $V_C$ (assuming the drop across
Figure 62: Diagram of the test setup. The light source intensity is controlled with a power supply. The I-V curve of the photodiode is measured with a source meter. The output voltage is measured with an oscilloscope.

the switch is negligible). During Phase II ($\phi_2$), both $C_C$’s are connected in series and discharged. Fig. 65 shows the output of a 2-stage charge pump.

As the the switches used are not ideal, there is some loss due to the ON resistances ($R_{on}$), thus the voltage on both $C_C$’s are not equal, and the output is less that double compared to 1-stage charge pump. The output can be further increased by adding more stages to the charge pump.

5.4.6 Limitations of charge pump

The main advantage of a capacitor based boost circuit is that, the circuit can be completely integrated onto a single chip. But there are some limitations to this approach
The on chip capacitor suffers from bottom plate parasitic capacitance [61] which is as large as 20% of the total capacitance. When capacitors $C_C$ and $C_L$ are charged, the bottom plate capacitance gets charged too. This charge discharges to ground and thus reduces the net output voltage delivered to the load, reducing its efficiency.

- Accurate charge pumps require substantially large capacitors on the order of micro-Farads which are difficult to integrate on chip [64].

- To boost the voltage to higher values, we need more stages of capacitors. Each capacitor stage adds 3 more switches to the existing switches. Every switch has a ON resistance losses, which will eventually reduce the total output power delivered.
to the load. The ON resistance of the switches is inversely proportional to the aspect ratio \((w/l)\) of the NMOS.

\[
R_{on} \propto \frac{1}{(w/l)}
\]

To reduce the \(R_{on}\), we can increase the width \(w\) of the switch. But with so many switches needed, increasing \(w\) will cost in more silicon area.

- As the number of stages grows, the switches connected to the upper end of the series connected \(Ccs\) (during Phase II), will need higher operating voltage to keep the switch ON. To turn ON a switch, the \(V_{gs}\) voltage has to be more than the threshold voltage \(V_{th}\) of the NMOS. As we go up the series connected \(C_C\), the source voltage \(V_s\) increases, reducing \(V_{gs}\). Thus for multi-stage charge pump we need different level of operating voltages \(V_{DD}\).
Due to the above mentioned limitations, we use inductor based boost converter circuit. As state-of-the-art inductors can be as small as $0.5 \times 1 \times 0.5 \text{mm}^3$, co-packaging an off-chip inductor with the sensor IC is an viable solution for producing miniaturized energy-harvesting sensor nodes [38]. In section 5.5 we focus on inductor-based solar energy harvesting circuits for integrated photodiodes.

### 5.5 Boost Converter

Figures 66 and 67 show the equivalent circuit of the energy harvester when $\phi_1 = 1$ and when $\phi_1 = 0$, respectively. The equivalent circuits are employed to model the operation of the inductor-based energy harvester and to guide its design.

The diode $D_s$ is assumed to have zero ON resistance and a drop voltage of $V_{don}$. 

Figure 65: Output of 2-stage charge pump captured by oscilloscope
Figure 66: Equivalent energy harvesting circuit when $\phi_1 = 1$.

volts when conducting. Capacitance $C_d$ is the parallel equivalent capacitance of $C_D$ and $C_j$.

Two distinct modes of operation can be distinguished for the energy harvesting circuit, namely continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The circuit operates in CCM if the current through the inductor does not fall to zero throughout a switching period. On the other hand, if the inductor current falls to zero before the end of a switching phase, the harvesting circuit is said to operate in DCM. DCM typically occurs when the harvesting circuit operates at light load conditions generating large inductor current variations [22]. The difference between these two modes is shown graphically in Fig. 68 and 69 where the current through the inductor, $I_i(t)$, is depicted.
5.5.1 CCM Analysis

Fig. 68 shows a typical steady state inductor current waveform in CCM. $T_1$ denotes the time for which $\phi_1 = 1$ while $T_2$ denotes the time for which $\phi_1 = 0$.

From the circuit in Fig. 67 we can write the following expression for $I_i$ when $\phi_1 = 0$:

$$I_i(t) = I_i(T_1) - \frac{1}{L} \int_{T_1}^{t} V_i \, dt$$  \hspace{1cm} (5.21)

Replacing $V_i = V_{out} + V_{don}$ in (5.21) and assuming a capacitor $C_L$ large enough to keep $V_{out}$ constant (small-ripple approximation), equation (5.21) can be solved to yield:

$$I_i(t) = I_i(T_1) - \frac{(t - T_1)}{L} (V_{out} + V_{don})$$  \hspace{1cm} (5.22)

The condition for CCM operation is $I_{i0} > 0$. Given that $I_i(T_1 + T_2) = I_{i0}$, the
Following expression for \( I_{i0} \) can be found:

\[
I_{i0} = I_i(T_1) - \frac{T_2}{L} (V_{out} + V_{dom})
\] 

Equation (5.22) can also be used in DCM analysis provided that \( I_{i0} = 0 \) before the end of a switching period. In steady state, the load current \( I_L \) is equal to the average current through the diode \( D_s \). Therefore, we can write:

\[
I_L = \frac{1}{T} \int_{T_1}^{T_1+T_2} I_i(t) \, dt
\] 

where \( T = T_1 + T_2 \). Replacing (5.22) in (5.24) and solving for \( V_{out} \) results in:

\[
V_{out} = \frac{2L}{(1-d)T} I_i(T_1) - \frac{2LI_L}{(1-d)^2 T} - V_{dom}
\]

where, \( d = T_1/T \) is the clock’s duty cycle. According to (5.25), the output voltage can be increased by increasing the value of the inductance \( L \). However, due to the small-package
constraints of the target application, $L$ is kept below $47 \, \mu H$. In principle, $V_{out}$ could also be increased by increasing the duty cycle or the switching frequency. However, changing $d$ and $T$ also affects the value of $I_i(T_1)$. In the next subsection, an expression for $I_i(T_1)$ will be derived that will allow us to consider the overall effects of $d$ and $T$ on $I_i(T_1)$.

### 5.5.2 DCM Analysis

From Fig. 69 we note that $I_i(T_1 + \delta T) = 0$. Replacing this result in (5.22) and solving for $\delta$ yields:

$$\delta = \frac{LI_i(T_1)}{(V_{out} + V_{don}) T} \quad (5.26)$$

![Figure 69: Inductor current waveform in DCM.](image)

The condition for DCM operation is $\delta < (1 - d)$. As before, in steady state the load current $I_L$ is equal to the average current through the diode $D_s$. Therefore, we can
write:

\[ I_L = \frac{1}{T} \int_{T_1}^{T_1 + \delta T} I_i(t) \, dt \quad (5.27) \]

Replacing (5.22) and (5.26) in (5.27) and solving for \( V_{out} \) yields:

\[ V_{out} = \frac{LI_i^2(T_1)}{2TI_L} - V_{don} \quad (5.28) \]

Notably, in DCM the output voltage has a quadratic dependence on \( I_i(T_1) \) and is inversely proportional to the load current \( I_L \). An expression for \( I_i(T_1) \) will be derived next to facilitate the calculation of \( V_{out} \). Once \( V_{out} \) is known, both the output power \( P_{out} = V_{out} \times I_L \) and the efficiency can be calculated.

### 5.5.3 Inductor Current

From Fig. 66 we can write the following relationships:

\[ I_i = I_{ph} - I_d - C_d \frac{dV_d}{dt} - \frac{V_d}{R_{sh}} \quad (5.29) \]

and

\[ \frac{dI_i}{dt} = \frac{V_d}{L} - \frac{2R_{on}}{L} I_i \quad (5.30) \]

The non-linear dependence of \( I_d \) on \( V_d \) precludes an explicit solution of the equation system above. To circumvent this problem we employ Taylor series to linearize the current \( I_d \) around the steady state average value of the photodiode voltage \( V_d \). Fig. 70 shows the approximate behavior of \( V_d \) in steady state. In the figure, \( V_{dm} = (V_{d0} + V_{d1})/2 \) is the average value of \( V_d \).

Applying Taylor series, the current \( I_d \) can be approximated around \( V_{dm} \) as follows:

\[ I_d = c_1 + c_2(V_d - V_{dm}) \quad (5.31) \]
where, $c_1 = I_s\left(e^{V_{dm}/nV_T} - 1\right)$ and $c_2 = (I_s/nV_T)e^{V_{dm}/nV_T}$. From (5.31) we can write:

$$\frac{dI_d}{dt} = \frac{dI_d}{dt} + c_2 \frac{dV_d}{dt} \tag{5.32}$$

Taking the derivative of (5.29) with respect to time yields:

$$\frac{dI_i}{dt} = -\frac{dI_d}{dt} - C_d \frac{d^2V_d}{dt^2} - \frac{1}{R_{sh}} \tag{5.33}$$

Replacing (5.32) in (5.33) and equating the result with (5.30) results in a second-order differential equation which can be employed to solve for $V_d$ when $\phi_1 = 1$:

$$V_d(t) = -\frac{K_3}{K_2} + c_4 e^{-t/\tau_1} + c_5 e^{-t/\tau_2} \tag{5.34}$$

where,

$$K_1 = -\frac{c_2}{C_d} - \frac{1}{C_d R_{sh}} - \frac{2R_{on}}{L}$$

$$K_2 = -\frac{1}{LC_d} \left(1 + c_2 2R_{on} + \frac{2R_{on}}{R_{sh}}\right)$$

$$\tau_1 = \frac{K_1}{2} - \frac{1}{2} \sqrt{\frac{K_1^2}{4} + 4K_2}$$
\[ \tau_2 = \frac{-1}{\frac{K_1}{2} + \frac{1}{2} \sqrt{K_1^2 + 4K_2}} \]

\[ K_3 = -\frac{-2R_{om}}{LC_d} \left( c_1 - I_{ph} - c_2 V_{dm} \right) \]

\[ c_4 = \left( \frac{\tau_1}{\tau_1 - \tau_2} \right) \left( V_{d0} + \frac{K_3}{K_2} \right) \]

\[ c_5 = \left( \frac{\tau_2}{\tau_2 - \tau_1} \right) \left( V_{d0} + \frac{K_3}{K_2} \right) \]  

(5.35)

Given that \( V_{d1} = V_d(T_1) \) and using (5.34) we can write:

\[ V_{d1} = -\frac{K_3}{K_2} + c_4 e^{-T_1/\tau_1} + c_5 e^{-T_1/\tau_2} \]  

(5.36)

To solve for \( V_d \) when \( \phi_1 = 0 \), we notice that from Fig. 67 we can write:

\[ C_d \frac{dV_d}{dt} = I_{ph} - I_d - \frac{V_d}{R_{sh}} \]  

(5.37)

Replacing (5.31) in (5.37) results in a first-order differential equation that can be solved to yield:

\[ V_d(t) = -\frac{K_5}{K_4} \left( 1 - e^{-t/\tau_3} \right) + V_{d1} e^{-t/\tau_3} \]  

(5.38)

where,

\[ K_4 = -\frac{c_2}{C_d} - \frac{1}{C_d R_{sh}} \]

\[ K_5 = \frac{I_{ph} - c_1 + c_2 V_{dm}}{C_d} \]

\[ \tau_3 = \frac{1}{K_4} \]  

(5.39)

Given that \( V_{d0} = V_d(T_2) \) and using (5.38) we can write:

\[ V_{d0} = -\frac{K_5}{K_4} \left( 1 - e^{-T_2/\tau_3} \right) + V_{d1} e^{-T_2/\tau_3} \]  

(5.40)

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The steady-state values of $V_{d0}$ and $V_{d1}$ can be found using the iterative procedure outlined in Listing 1 below. In the iterative procedure the variable $k$ represents the iteration number.

Listing 1. Iterative procedure to find steady-state values $V_{dm}$, $V_{d0}$ and $V_{d1}$

1) $k=0$
2) Set $V_{d0}[k]=V_{d1}[k]=V_{oc}$
3) Use (22) to find $V_{d1}[k+1]$
4) Use (26) and $V_{d1}[k+1]$ to find $V_{d0}[k+1]$
5) Update $V_{dm} = (V_{d0}[k+1]+V_{d1}[k+1])/2$
6) $k=k+1$
7) If $k>200$ end
8) Go to 3)

Once the steady-state value of $V_{dm}$, $V_{d0}$ and $V_{d1}$, along with the coefficient values in (5.35), are found, an expression for $I_i$ when $\phi_1 = 1$ can be obtained by replacing (5.31), (5.33) and (5.34) in the (5.29)-(5.30) equation system and solving the resulting differential equation. The obtained expression for the inductor current is:

$$I_i(t) = I_{i0}e^{-t/\tau_4} + \frac{c_6}{2R_{on}}\left(1 - e^{-t/\tau_4}\right) + \frac{c_{471}}{L - 2R_{on}\tau_1}\left(e^{-t/\tau_4} - e^{-t/\tau_1}\right) + \frac{c_{572}}{L - 2R_{on}\tau_2}\left(e^{-t/\tau_4} - e^{-t/\tau_2}\right)$$

(5.41)

where,

$$c_6 = -\frac{K_3}{K_2}$$

$$\tau_4 = \frac{L}{2R_{on}}$$

(5.42)

To demonstrate the validity of the model derived above, the inductor current waveform, $I_i(t)$, was calculated using (5.41) and using the Spectre circuit simulator. Fig. 71
shows the inductor current waveforms generated by the model and the circuit simulator for the following parameter values: $I_{ph} = 52 \, \mu A$, $L = 47 \, \mu H$, $I_{i0} = 0 \, A$, $T = 8 \, \mu s$ and $d = 0.5$. The figure shows three cases: $R_{on} = 250 \, \Omega$, $R_{on} = 100 \, \Omega$ and $R_{on} = 50 \, \Omega$.

Notably, the derived expression for $I_i(t)$ agrees very well with the output of the Spectre circuit simulator. More importantly, the expression for $I_i(t)$ allows us to explore the design space of the DC-DC converter without having to rely on a high-end circuit simulator. According to equations (5.25) and (5.28), $V_{out}$ is maximized when $I_i(T_1)$ is maximum. In the next section we will the mathematical model derived to find the circuit parameter values that maximize the output voltage and consequently the efficiency of the energy harvesting circuit.

5.5.4 Model-Based Design Optimization

From Fig. 71 it is clear that low $R_{on}$ values result in higher peak inductor currents, and correspondingly higher output voltages, as the power losses due to the on-resistance of the switch transistors are reduced. Hence, low $R_{on}$ values are preferred to achieve high conversion efficiencies. The value of $R_{on}$ for a NMOS transistor is given by:

$$R_{on} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_{TH})} \quad (5.43)$$

where, $\mu_n$ is the electron mobility, $C_{ox}$ is the capacitance per unit area of the gate oxide, $W$ is the width of the transistor’s gate, $L$ is the length of the transistor’s gate, $V_{GS}$ is the steady-state transistor’s gate-to-source voltage and $V_{TH}$ is the threshold voltage of the transistor. From (5.43), $R_{on}$ decreases as $W$ increases. However, as $W$ is increased,
Figure 71: Inductor current $I_i(t)$ waveforms calculated using the derived expression in (5.41) and using the Spectre circuit simulator for three different values of $R_{on}$.

the gate capacitance, $C_g = WLC_{ox}$, also increases resulting in higher dynamic power losses due to the need to charge and discharge $C_g$ as the transistor is turned on and off. Thus, the transistor width $W$ cannot be made arbitrarily large.

The analysis presented in [81] shows that the optimal $W$, at which the combined effect of conduction losses due to $R_{on}$ and dynamic losses due to $C_g$ is minimized, results in extremely wide transistors. Hence, they conclude that in the interest of saving silicon die area, smaller than optimal transistor widths can be employed. In this work we employ
transistors with a gate width of 90 µm which result in an on-resistance of approximately 50 Ω.

From equations (5.25) and (5.28), it is clear that a large inductance value maximizes the output voltage of the energy harvesting circuit. However, a large inductor will have a large physical size and might not be suitable for integration with a small sensor unit. Hence, the inductance value is limited to 47 µH as this is an inductor that is commercially available in packages as small as 1×2×1 mm³.

5.5.5 CCM and DCM Operation

\[ \frac{L}{T_2} I_i(T_1) - V_{don} > V_{out} \]  

(5.44)

Similarly, replacing the DCM condition \( \delta > (1 - d) \) in equation (5.26) results in the following output voltage lower bound:

\[ V_{out} > \frac{L}{T_2} I_i(T_1) - V_{don} \]  

(5.45)

Comparing (5.44) and (5.45), it is clear that the energy harvesting circuit provides a higher output voltage if it operates in DCM. Hence, we focus on the DCM for the rest of this paper.

For convenience, actual measurements of the harvester performance are taken using a resistive load instead of a constant current load. Thus, we can write: \( I_L = V_{out} / R_L \), where \( R_L \) is the load resistance and \( I_L \) is the load current. Replacing \( I_L = V_{out} / R_L \) in (5.28) results in the following quadratic equation:
\[ V_{out}^2 + V_{don}V_{out} - \frac{LR_LI_1^2(T_1)}{2T} = 0 \]  

which can be solved to obtain:

\[ V_{out} = \sqrt{\frac{V_{don}^2}{4} + \frac{LR_LI_1^2(T_1)}{2T} - \frac{V_{don}}{2}} \]  

\[ P_{out} = \frac{V_{out}^2}{R_L} \]  

Fig. 72 shows the conversion efficiency of the energy-harvesting circuit as the switching clock period \((T)\) and the clock’s duty cycle \((d)\) are varied. The efficiency was calculated using (5.1) and (5.48). The following parameters were used to generate the plot: \(I_{ph} = 50 \, \mu A\) (outdoor light conditions), \(R_L = 500 \, k\Omega\), \(V_{don} = 0.3 \, V\), \(L = 47 \, \mu H\), \(R_{on} = 50 \, \Omega\) and \(C_d = 33 \, nF\). From the figure, efficiencies greater than 60\% can be achieved for switching frequencies in the range of 200 kHz to 4 MHz \((0.25 \, \mu s \leq T \leq 5.0 \, \mu s)\) and duty cycles above 4\%.

Figures 73 and 74 show the conversion efficiency and output voltages of the energy-harvesting circuit as the duty cycle of the clock signal is varied, and for different values of the photogenerated current \(I_{ph}\). The resistance load is kept fixed at \(R_L = 500 \, k\Omega\) and the switching frequency is set to 200 kHz. Notably, as the illumination level changes, the duty cycle needs to be adjusted correspondingly to achieve maximum conversion efficiency. Moreover, from Fig. 74, as the illumination level decreases, the maximum output voltage that can be obtained also decreases.

Fig. 75 shows a plot of \(V_{dm}\), the average photodiode voltage \((V_d)\) in steady state, as
Figure 72: Conversion efficiency of the proposed energy-harvesting circuit operating in DCM as a function of duty cycle \( (d) \) and clock period \( (T) \).

the duty cycle is varied and for the same conditions as Figs. 73 and 74. Fig. 75 also shows (with color dots) the location of the maximum power point voltage \( (V_{mpp}) \). Comparing Fig. 75 with Figs. 73 and 74, it can be seen (as expected), that the maximum conversion efficiency is achieved for the same duty cycle that results in the average voltage across the photodiode being equal to \( V_{mpp} \).

Fig. 76 shows the output voltage of the energy-harvesting circuit for different values of the load resistance \( R_L \) as the duty cycle is varied and for a fixed value of \( I_{ph} \). As the load resistance decreases, the output voltage decreases. However, the maximum output voltage is achieved for the same duty cycle value regardless of the load resistance value. Hence, to achieve maximum conversion efficiency, the duty cycle needs to be adjusted only in response to changes in the illumination levels.
5.5.6 Test Setup and Measurements

The test setup is same as for charge pump. The power supply current of the light source was adjusted until $I_{ph}$ reached a value of 50 $\mu$A to simulate outdoor illumination levels (approx. 60 klux). The average output voltage of the energy-harvesting circuit was then measured with the oscilloscope.

Fig. 77 shows the output voltage as predicted by (5.47) (shown with dotted lines) and actual voltage measurements (shown with circles) as the duty cycle is varied. An inductor value of $L = 47 \, \mu$H and a capacitance $C_D$ of 33 nF were employed. Three different values of resistor were used for the load: 198 k$\Omega$, 330 k$\Omega$ and 990 k$\Omega$. Given that the oscilloscope probe has a finite impedance (approximately 700 k$\Omega$) the effective
load seen by the energy-harvesting circuit is lower than the resistors employed. Taking into account the probe impedance, the effective load resistance values ($R_L$) are 154 kΩ, 224 kΩ and 410 kΩ. The switching frequency was set to 200 kHz ($T = 5 \mu s$). Notably, the output voltage predicted by the theoretical model agrees very well with the measurements. The maximum output voltage obtained for $R_L = 410$ kΩ is 2.24 V for a duty cycle of 4.5% which corresponds to a power delivered to the load of 12.24 $\mu W$ and a conversion efficiency of 59%. The maximum output voltage obtained with only the oscilloscope probe loading the circuit is 2.81 V. Fig. 78 shows an oscilloscope capture of the corresponding output voltage. The output voltage ripple is due to the switching activity and can be improved by employing a larger load capacitance $C_L$. 

Figure 74: Output voltage of the energy-harvesting circuit operating in DCM as a function of duty cycle ($d$) for different photogenerated current levels $I_{ph}$. 

![Output voltage of the energy-harvesting circuit operating in DCM as a function of duty cycle ($d$) for different photogenerated current levels $I_{ph}$](image-url)
Figure 75: Average photodiode voltage ($V_{dm}$) as a function of duty cycle ($d$) for different photogenerated current levels $I_{ph}$.

Higher efficiencies can be achieved if the switching frequency is increased as predicted by Fig. 72. However, in our experiments, for switching frequencies beyond 250 kHz, the conversion efficiency started to decrease. The lower efficiencies at higher switching frequencies are due to the combined effects of parasitic capacitive and inductive elements of the PCB and the IC package and the limited self-resonance frequency (SRF) of the inductor employed. The efficiency, however, can be improved by co-packaging the IC and the inductor to minimize parasitic effects.

The proposed energy-harvesting circuit requires two off-chip components ($C_D$ and $L$). Due to their relatively large values (by integrated circuits standards), these components cannot be integrated on chip. However, they can be co-packaged with the final IC as state-of-the-art off-chip capacitors and inductors of the requires values are on the
Figure 76: Output voltage of the energy-harvesting circuit operating in DCM as a function of duty cycle \(d\) for different load resistances \(R_L\).

order of \(1 \times 2 \times 1 \text{ mm}^3\). An external Schottky diode was employed in our experiments because the IC fabrication process that was used did not have a Schottky diode option. However, many CMOS fabrication process support the Schottky diodes. Alternatively, at the expense of more silicon area, a self-synchronized MOS switch [38] can be employed instead of the Schottky diode.
Figure 77: Output voltage of the energy-harvesting circuit as predicted by theoretical model (dotted lines) and from hardware measurements (circles).

Figure 78: Voltage output of energy-harvesting circuit captured by an oscilloscope ($R_L = 410 \, \text{k}\Omega$).
CHAPTER 6

CYCLIC ADC AND ENTROPY ENCODER

Another method to improve the life of a wireless sensor is to reduce its power consumption. In a sensor, radio communications is one of the most power demanding operations. One way to reduce the radio transmission power is to compress the sensor data so that fewer bits have to be transmitted. This makes the implementation of a compression scheme on the sensor node a desirable feature provided that it consumes a fraction of the power spent on radio transmissions.

The operations required in data compression can be broadly classified in two categories: pre-processing and encoding. The pre-processing step aims at transforming the signal of interest so that it can be efficiently encoded. Pre-processing can be achieved by operations as simple as taking the difference between two consecutive samples or by more complex operations such as applying an energy-compacting transform like the discrete cosine transform (DCT) or a wavelet transform. Another effective method of pre-processing the data could be The encoding step, also known as entropy encoding, involves assigning variable-length codewords to input symbols according to their probability of occurrence. Shorter codewords are assigned to highly probable symbols, while longer codewords are assigned to less probable symbols.

Compression can be classified as Lossy and Lossless compression. Lossy compression techniques achieve higher compression ratio by discarding some bits, which once
lost cannot be restored. One of the major example of lossy compression is the JPEG compression. Lossy compression techniques are majorly applied in digital camera photography. In lossless data compression, no data bits are lost and the original data to be reconstructed from a compressed data. As no bits are lost during compression, the compression ratios achieved with this techniques are not very high, typically in the range of 2 to 4. The most popular examples of lossless compression are WINZIP, PNG etc. In our research we focus on lossless data compression.

6.1 Preliminaries

The Golomb-Rice codes form a family of codes parameterized by an integer \( m > 0 \). The encoding algorithm considers non-negative integers as input. To encode an integer \( n \), the algorithm proceeds to divide \( n \) by \( m \). The division results in a quotient, \( q \), and a reminder \( r \), i.e. \( n = q m + r \), where \( q = \lfloor n/m \rfloor \) and \( \lfloor y \rfloor \) is the greatest integer less than or equal to \( y \), \( 0 \leq r < m \). The quotient \( q \) is encoded with a unary code and the remainder \( r \) is encoded with a Huffman code of length \( \log_2 m \) if \( r < 2^{\lfloor \log_2 m \rfloor + 1} - m \) or lengths \( \lfloor \log_2 m \rfloor + 1 \) otherwise [26].

When \( m \) is a power of two, i.e. \( m = 2^k, k = 0, 1, 2, \ldots \), the encoding is a very simple procedure. As before, the quotient \( q \) is encoded with a unary code but the reminder \( r \) is encoded with a natural binary code. The quotient and the reminder codes are separated by a ‘0’ bit which is also called the comma bit. The length of the codeword is \( l_{n,k} = k + 1 + \lfloor n/m \rfloor \). The Golomb codes for the special case \( m = 2^k \) are also known as Golomb-Rice codes because they were independently developed by Rice. Due to their low complexity
and good compression performance, the Golomb-Rice codes were recommended by the Consultative Committee for Space Data Systems, the JPEG-LS standard, and in the H.264 standard for lossless audio compression [44].

### 6.2 Proposed Compressing ADC

The proposed compressing converter is based on a cyclic converter architecture that is modified to generate Golomb-Rice codewords at its output. A current-mode implementation is pursued here due to the advantages of current-domain processing such as large dynamic range, ease of implementation of arithmetic operations such as addition and subtraction, reduction of voltage settling times, and compactness of the resulting circuits [56].

The key observation that allows us to combine a cyclic ADC with the Golomb-Rice entropy encoder is that the division by $2^k$ required by the coding algorithm can be performed by slightly modifying a cyclic converter. Figure 79 shows a block diagram of the modified cyclic ADC. In the traditional cyclic converter the loop gain $G$ is set to 2 and the current $I_k$ is set equal to the reference current $I_{\text{ref}}$ of the converter.

The proposed converter works in two phases: Phase I and Phase II. In Phase I the unary code is generated and in Phase II the binary code is generated. This unary code represents the quotient while the reminder is represented by the binary code of $N$ resolution.

Phase I starts by sampling the input current $I_{\text{in}}$ and setting the gain $G$ equal to 1. $I_k$ is set to $2^kI_{\text{LSB}}$, where $I_{\text{LSB}} = I_{\text{ref}}/2N$ and $N$ is the bit resolution of the converter.
The switch $S_1$ is pulled down to close the analog loop. The residual current $I_{\text{res}}$ circulates within the loop. When the comparator outputs a '0', it indicated the end of Phase I or the unary code. This '0' bit is also called as the comma bit.

In Phase II, the gain $G$ is set to 2 and the ADC works as a conventional cyclic ADC. The residual current $I_{\text{res}}$ circulates in the loop, till the desired resolution is achieved. Hence, bit generated during Phase I and Phase II combined together produce a code equivalent to the Golomb-Rice code.

To produce effective compression the converter needs to continuously adapt its parameter $k$ to the statistics of the input. There are several ways in which this can be accomplished. A simple way to adapt the parameter $k$ is based on the codewords that have been previously generated (see Fig. 80). Since the adaptation rule is based on previous
codewords, a decoder can compute the correct value of $k$ and decompress the data stream. A low-complexity adaptation rule is used here. The basic idea of the adaptation rule is to minimize the length of the total codeword by monitoring the length of the unary code and the MSB of the binary code. If unary code is generated for few conversation cycle, $k$ is increased till no more unary code is generated. If no unary code is generated for few conversion cycles, the MSB is monitored. If the MSB is 1, no changes are made to $k$. Else if the MSB is 0, $k$ is decremented till the MSB is 1. A fail safe algorithm is also included. If the unary code for one conversion hits a maximum limit (set by user), the the conversion cycle is aborted and the $k$ value is set to its maximum [43].

![Figure 80: Compressing ADC in a feedback configuration to adapt the parameter $k$ to the statistics of the input.](image)

6.2.1 Hardware Design

The converter was designed using current-mode circuits due to their complexity advantages when implementing addition and subtraction operations. Current-mode cyclic converters, however, may suffer from device mismatch leading to imprecise gain values
in the converter. The problem of mismatch can be minimized by employing dynamic current storing techniques in which a gain of 2 is obtained by copying a current into two different current memory cells and then adding their currents together [11]. Fig. 81 shows the schematic diagram of the proposed compressing converter. The converter employs the dynamic current storing technique.

Three memory cells are employed in this design. Each current memory cell consists of a transistor $M_x$, a capacitor $C_x$ and an amplifier $A_x$. The amplifiers are employed to increase the output impedance of the memory cells and the accuracy of current cells. The current $I_k$ is generated by a current bank consisting of $\sum_{k=0}^{N} 2^k$ transistors. These transistors connected as several unit-value current sources that are combined in parallel by a decoder to generate the desired $I_k$ current value.

In Phase I the circuit operates as follows: the input current $I_{in}$ is first compared with $I_{sign}$ by closing $SW_1$ and $SW_8$. If $I_{in} > I_{sign}$ then the residual current $I_{res} = |I_{in} - I_{sign}|$ is stored in the first current memory cell by closing $SW_1$, $SW_2$, $SW_3$ and $SW_8$. This current is then copied into the third memory cell by closing $SW_6$, and $SW_7$ while opening $SW_1$, $SW_3$ and $SW_8$. If $I_{in} < I_{sign}$, then the $I_{res}$ is directly stored in the third memory cell. When the current is copied to the memory cells, the comparator is held at its threshold voltage ($2.5V$). Next, $I_{res}$ is compared with $I_k$ by closing the $SW_6$ and $SW_8$ while opening all other switches. If $I_{res} > I_k$, the capacitor $C_4$ is charged and comparator outputs a ’1’ else if $I_{res} < I_k$, $C_4$ discharges and the comparator gives a ’0’. If $I_{res} > I_k$, $SW_2$ and $SW_3$ are closed and the current $I_{res} - I_k$ gets stored into the first current memory cell. This process is repeated until the output of the comparator is ’0’. At this point, the
Unary code has been fully generated and the converter moves to Phase II.

Figure 81: Schematic diagram of the proposed compressing ADC with Golomb-Rice code outputs

In Phase II, the $2 \times$ gain is obtained by storing a copy of $I_{res}$ in the first and second memory cells and then copying their into the third memory cell. The $2I_{res}$ current is compared with $I_k$ by closing the switches $SW_6$ and $SW_8$ and opening all other switches. The comparator generates an output bit based on this comparison. If $I_{res} > I_k$, the current $I_{res} - I_k$ is stored in the first and second memory cells, otherwise, $I_{res}$ is stored in the first and second memory cells. The process is repeated until $k$ bits are generated. At this point a complete codeword has been generated and the conversion process ends. Figure 82 shows layout of the proposed ADC designed using Cadence Virtuoso tools and fabricated
The above ADC is built up of op-amps, current mirrors, transmission gate (TG) switches, current bank, a $3 \times 8$ decoder and an inverter based comparator. To understand the complete performance of the ADC we do small signal analysis of each of these components separately. In this section we do small signal analysis and compare our data obtained from SpecterS simulations.

### 6.3 ADC Component Analysis

The above ADC is built up of op-amps, current mirrors, transmission gate (TG) switches, current bank, a $3 \times 8$ decoder and an inverter based comparator. To understand the complete performance of the ADC we do small signal analysis of each of these components separately. In this section we do small signal analysis and compare our data obtained from SpecterS simulations.

#### 6.3.1 Single Stage Op-amp

One op-amp is used per memory cell, $A_1$, $A_2$ and $A_3$ (Fig. 82). The op-amps help increase the output impedance of the NMOS/PMOS that are used to store the current. Two op-amps configurations are used: NMOS differential pair input and PMOS differential
pair input. We will analysis the NMOS differential pair input type op-amp in this section.

Fig. 83 shows the transistor level circuit diagram of the op-amp. The capacitors shown in fig. 83 are internal capacitors. These capacitors effect the performance of the amplifier at high frequencies. In our case we have only shown those capacitance that are connected to the output terminal.

![Figure 83: Differential amplifier schematic](image)

Fig. 84 shows its equivalent small signal circuit. The small signal analysis help determine the performance of the amplifier at higher frequencies. The sources of $M_1$, $M_2$, $M_3$, $M_4$ are grounded. In small signal analysis, the node at $S_1$ and $S_2$ and the $V_{dd}$ act as virtual ground because, voltages at these nodes do not change with time, hence a constant. Capacitors $C_{dg4}$ and $C_{gd2}$ are connected between input and output terminals. Applying Miller effect, we split the capacitor as $C_{gdx}(1 + |A_v|)$ at the input and $C_{gdx}(1 + 1/|A_v|)$
at the output, where $A_v$ is the DC gain of the circuit. $A_v$ is represented as

$$A_v = g_{m1} \times (r_{o2} \| r_{o4})$$  \hspace{1cm} (6.1)$$

For AC analysis, we will include the capacitors at the output node into our gain equation 6.1 and we get

$$A_v(\omega) = g_{m1} \times (r_{eq} \| C_{eq})$$

$$A_v(\omega) = g_{m1} \times \left( \frac{r_{eq}}{1 + j\omega r_{eq} C_{eq}} \right)$$  \hspace{1cm} (6.2)$$

We use eq. 6.2 to plot the gain and phase margin of the amplifier with respect to frequency as shown in figure 85. We fed the amplifier with a sinusoidal type input voltage at frequency of 100KHz, and based on the gain at 100KHz the output voltage has been plotted (Figure 86).

6.3.2 Cascode Current Mirror

A cascode current mirror is used to feed the ADC. The mirror helps converting the sink input to a source input for the ADC. Figure 87 shows the cascode mirror implemented on the ADC. Figure 88 shows the small signal equivalent circuit of a cascode current.
mirror. From Fig. 88 $v_{out}$ can be expressed as

$$v_{out} = r_o2(i_{out} - g_{m2}v_s2) + r_o4(i_{out} - g_{m4}v_s4)$$

But, $i_{in} = 0$, $V_{sg4} = -V_{s4} = -i_{out}r_o2$ and $V_{sg2} = 0$, $v_{out}$ can be expressed as

$$v_{out} = i_{out}(r_o2 + r_o4 + g_{m4}r_o2r_o4)$$

Therefore $R_{out}$ can be written as

$$R_{out} = g_{m4}r_o2r_o4 \quad (6.3)$$

6.4 ADC Characterization

There are large number of figure of merits for an analog-to-digital converter that can specify its performance. Following are a few we measured for the proposed ADC:

6.4.1 Offset Error

Offset error is the deviation in the A/D converter’s behaviour at zero. Offset error calculated as the deviation of the actual transition voltage from the ideal 1/2 LSB [34].

\[
E_{off} = \frac{V_{0.01}}{V_{LSB}} - \frac{1}{2} LSB
\]

6.4.2 Gain Error

Gain error is the difference between the full scales values of the ADC to its ideal value, once the offset error has been removed. The gain error in LSB can be expressed

Figure 86: Output of amplifier for a sinusoidal input at 100KHz
as [34]

\[ E_{gain} = \left( \frac{V_{1-1}}{V_{LSB}} - \frac{V_{0-01}}{V_{LSB}} \right) - (2^N - 2) \]

6.4.3 Differential Nonlinearity

For an ideal ADC, all the code width are precisely 1 LSB apart. Differential Nonlinearity (DNL) is defined as the deviation of the code transition widths from the ideal width of 1 LSB. For an ideal converter DNL would be zero everywhere.

6.4.4 Integral Nonlinearity

Integral Nonlinearity (INL) is the distance of the code centers in ADC characteristics from the ideal line. If all code centers land on the ideal line then the INL is zero everywhere.
6.4.5 Signal-to-Noise-Distortion Ratio

Signal-to-noise-and-distortion ratio (SNDR) is the ratio of the input signal amplitude to the rms sum of all other spectral components. For an M-point FFT of a sine wave test, if the fundamental is in frequency bin $m$ (with amplitude $A_m$), the SNDR can be calculated from the FFT amplitudes [46]

$$SNDR = 10 \log \left[ A_m^2 \left( \sum_{k=1}^{m-1} A_k^2 + \sum_{k=m+1}^{M/2} A_k^2 \right)^{-1} \right]$$

To avoid any spectral leakage around the fundamental, often several bins around the fundamental are ignored. The SNDR is dependent on the input-signal frequency and amplitude, degrading at high frequency and power. Measured results are often presented in plots of SNDR versus frequency for a constant-amplitude input, or SNDR versus amplitude for a constant-frequency input.
6.4.6 Effective Number of Bits

Effective number of bits (ENOB) is simply the signal-to-noise-and-distortion ratio expressed in bits rather than decibels by solving the “ideal SNR” equation

\[ SNR = 6.02N + 1.76dB \]

for the number of bits N, using the measured SNDR

\[ ENOB = \frac{SNDR - 1.76dB}{6.02dB/bit} \]

6.5 ADC Characterization Test

The ADC was subjected to two different test:

- Histogram test of linearity: Performed to calculate the DNL and INL of the ADC
- Fast Fourier test to compute SNDR and ENOB

6.5.1 Histogram Test of Linearity

The linearity of the ADC can be determined by performing Histogram test [16]. A histogram of output digital codes are recorded for a large number of samples for an input ramp signal. The results are compared to the number of samples expected from theoretical ramp probability-density function (PDF). The PDF of a ramp is a straight line and can be defined as

\[ p(V) = \frac{I_{LSB}}{I_{max} - I_{min}} \]

Due to the statistical nature of this test, the length of the data record for the histogram test can be quite large [16]. The number of samples, \( M \), required for a high-confidence
measurement is

\[ M = \frac{\pi 2^{N-1} Z_{\alpha/2}^2}{\beta^2} \]

where \( N \) is the number of bits, \( \beta \) is the DNL measurement resolution, and for 99% confidence level \( Z_{\alpha/2} = 2.576 \). For a 7 bit resolution ADC, number of samples should be \( M = 133,420 \).

### 6.5.2 Fast Fourier Transform

The frequency-domain tests use the direct application of the fast Fourier transform. Taking the FFT of the output data while driving the A/D converter with a single, low distortion sine wave, the SNDR and ENOB, can be calculated.

### 6.6 Hardware Measurement

The proposed compressing ADC was fabricated on a 0.5\( \mu \)m CMOS process. A printed circuit board (PCB) to host the fabricated chip and supporting circuitry was also designed and fabricated (see Fig. 89). Special attention was placed on the PCB design to minimize noise coupling between the digital and analog domains. On-board digital-to-analog converters (DACs) were employed to generate bias voltages and a CPLD was employed to implement the state machine and to transmit the generated codewords to a PC for signal decompression and reconstruction. The input current is generated with an on-chip current conveyor. The impact of charge injection from switches \( SW_3, SW_5 \) and \( SW_7 \) is minimized by increasing the channel length of transistors \( M_1, M_2 \) and \( M_3 \) and by using half-size dummy transistors in series with switches \( SW_3, SW_5 \) and \( SW_7 \). Capacitor
sizes are $C_1 = C_2 = C_3 = 2pF$.

The converter was first characterized in terms of nonlinearities and signal-to-noise ratio (SNR). The characterization was carried out for fixed values of the parameter $k$ in non-adaptive mode (Adaptation Rule is not employed). Table 19 shows the SNDR and ENOB results obtained. Figure 90 shows the integral non-linearity (INL) of the converter for different values of $k$. Notably, the non-linearity errors increase as $k$ decreases. The reason for this increase is that small values of $k$ and large input values produce long unary codes which translates into the residual current $I_{res}$ getting copied multiple times in the current memory cells. With each copy a small error due to the non-idealities in analog circuits is introduced and accumulated.
Table 19: SNDR and ENOB

<table>
<thead>
<tr>
<th>$k$</th>
<th>SNDR(dB)</th>
<th>ENOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>(111)$_b$</td>
<td>32.79</td>
<td>5.15</td>
</tr>
<tr>
<td>(110)$_b$</td>
<td>32.86</td>
<td>5.17</td>
</tr>
<tr>
<td>(101)$_b$</td>
<td>31.81</td>
<td>4.99</td>
</tr>
<tr>
<td>(100)$_b$</td>
<td>29.94</td>
<td>4.68</td>
</tr>
<tr>
<td>(011)$_b$</td>
<td>28.62</td>
<td>4.46</td>
</tr>
<tr>
<td>(010)$_b$</td>
<td>25.03</td>
<td>3.87</td>
</tr>
<tr>
<td>(001)$_b$</td>
<td>20.79</td>
<td>3.16</td>
</tr>
<tr>
<td>(000)$_b$</td>
<td>7.069</td>
<td>0.88</td>
</tr>
</tbody>
</table>

6.7 Finite State Machine

A finite state machine (FSM) controls the switch activity and is responsible for adapting the parameter $k$ to the statistics of the input so that compression is achieved. Figure 91 shows the flow diagram of the FSM implemented. The functioning of the FSM is similar to the process defined in section 6.2.1. The adapt feature is implemented by monitoring the output of the comparator. We initiated three internal counters: $up$, $unary\ cap$ and $down$ that help monitoring the output of the comparator.

In Phase I, if the comparator output is ”1” (after the sign bit has been transmitted), while computing the unary code, the FSM is pushed into $S4$ state. When the FSM enters $S4$, $up$ and $unary\ cap$ counters are incremented. The $up$ counter is incremented only when FSM enters the state for the first time. This count denotes that the final output of the ADC will contain at least one unary code. The $unary\ cap$ counts the number of unary codes in one single output of the ADC. If the unary code limit (set by user) is hit in a single conversion cycle, then the FSM stops and moves to the $STOP$ state. It restarts the conversion process for the same input signal but with highest resolution ($k = 7$ in this
Figure 90: INL

In Phase II, when the binary code is computed, if the comparator output is "0", the FSM goes into \textit{S12} state. Here the \textit{down} counter is incremented, only if it is the first binary bit and no unary bit was produced before it. This counter counts till it reaches its limit (\textit{D} in this case), then it decrements \textit{k} by 1. This process continues, till the first binary
bit is 1. In both cases new $k$ values are stored in a register and later fed into the FSM at the adaptive $k$ state $APK$. The FSM code was written in VHDL and implemented using a Xilinx 384 CPLD.

Table 20 shows the complexity of the FSM for a standard cyclic converter and for
the proposed modified converter. The complexity is shown in terms of number of registers (D-FFs) and number of logic gates. The table also shows the overhead or the additional logic needed to convert a standard cyclic converter into a compressing converter. Notably, at the control logic level, 29 additional flip-flops and 509 gates are needed to design a compressing cyclic ADC. The traditional approach in which the ADC and the entropy encoder are separate yields a higher complexity in the digital circuitry - a standalone Golomb-Rice entropy encoder requires 214 D-FFs, 16 adders, 16 comparators totaling over 1200 gates [43].

### 6.8 Test Setup

Multiresolution decomposition (MRDC) is an image processing technique in which the resolution of an image is progressively increased or decreased. In our research, we employ MRDC to generate image of lower resolution that serves as an prediction of pixel values in higher resolution image. The basic concept is depicted in fig. 92. The algorithm works with one level of decomposition. It takes the original image $H^0$ of size $N \times N$ pixels (with $N$ even) and generates image $H^1$ of size $\frac{N}{2} \times \frac{N}{2}$. The pixel value at location $(r, c)$ in $H^1$ is computed as follows:

$$H_{r,c}^1 = \frac{1}{4} \left( H_{2r,2c}^0 + H_{2r+1,2c}^0 + H_{2r,2c+1}^0 + H_{2r+1,2c+1}^0 \right)$$  \hspace{1cm} (6.4)
Figure 92: Multiresolution decomposition (a) Input image matrix, (b) average matrix, (c) residual matrix

where \( r = 0, 1, 2 \ldots N/2 - 1, c = 0, 1, 2 \ldots N/2 - 1 \). Thus, each pixel in \( H^1 \) is the average of the four pixels in the spatially equivalent \( 2 \times 2 \) block in \( H^0 \). The image \( H^1 \) has a resolution four times smaller than \( H^0 \). The low resolution image \( H^1 \) is employed as a predictor of the higher-resolution image \( H^0 \). A prediction residual image \( R^1 \) of size \( N \times N \) is computed as follows:

\[
R^1_{r,c} = H^0_{r,c} - H^1_{u,v}
\]

where \( u = \lfloor r/2 \rfloor, v = \lfloor c/2 \rfloor \) and \( \lfloor . \rfloor \) is the greatest integer function. For smooth areas in an image, a pixel value will be very close to the average of itself and its closest neighbors. Thus, the prediction residual on those regions will be zero or very close to zero. For regions in the image with edges or texture, the absolute value of the prediction residual will increase. For most natural images, the distribution of the prediction residuals peaks at
zero and falls exponentially as the residual absolute value increases. Prediction residuals of natural images often follow a Laplacian distribution. We take advantage of this type of distribution by using an entropy encoder to encode the residual images and achieve compression. An entropy encoder assigns short codewords to frequent residual values and longer codewords to less-frequent residual values.

The $H^1$ matrix can be converted to digital using an ADC. Compression at this level is mainly achieved due to the reduction in the size of the actual image by 4 times. But high compression ratios can be achieved for the residual matrix $R^1$ due to its Laplacian distribution nature. Note, that we only need to transmit 3 out of every 4 pixels in the residual images $R^1$ because the 4-pixel averages are already available to the decoder from the previous level of decomposition.

The original image can be recovered by rearranging Eq.(6.5) as

$$H^0_{r,c} = H^1_{u,v} + R^1_{r,c}$$  \hspace{1cm} (6.6)

Note, to recover the last pixel of each $2 \times 2$ matrix, we can use

$$H^0_{2r+1,2c+1} = 4H^1_{r,c} - H^0_{2r,2c} - H^0_{2r+1,2c} - H^0_{2r,2c+1}$$  \hspace{1cm} (6.7)

32 × 32 images captured by a CMOS camera was used as test subjects. The first level of decomposition was performed creating $H^1$ and $R^1$ matrix. These matrices were fed into the ADC for conversion and compression. The data was transmitted to the computer using UART communication protocol. Fig. 93(b) represents the histogram of input image shown in fig. 93(a). Note the histogram has 2 peaks, one at 0 representing white color and another at 150 representing black color.
Applying first level of decomposition produces an average image matrix as shown in fig. 94(a) with its histogram shown in fig. 94(b).

The residual image matrix and its histogram is shown in fig. 95(a) and 95(b) respectively. The histogram for residual matrix takes shape of laplacian distribution, which make compression of residual matrix more effective.

These images were fed into the ADC and recovered implementing the eqs.(6.6) and (6.7) using MATLAB. Fig. 96 shows the images recovered. More images were used to demonstrate the compression of the ADC. Figs. show the images fed into the ADC with their recovered image. To have a fair comparison, we plotted the image in 1-D, to estimate the accuracy of the ADC.

The compression ratio’s are given in Table 21. Images sizes more than $32 \times 32$ pixel were also tested. The compression results are shown in Table 22.
Figure 94: Average input image

Table 21: Compression ratios

<table>
<thead>
<tr>
<th>Images</th>
<th>C.R (with DC)</th>
<th>C.R (w/o DC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td>1.6927</td>
<td>1.8388</td>
</tr>
<tr>
<td>M</td>
<td>1.5612</td>
<td>1.6351</td>
</tr>
<tr>
<td>K</td>
<td>1.9072</td>
<td>1.7847</td>
</tr>
<tr>
<td>C</td>
<td>1.7546</td>
<td>1.806</td>
</tr>
</tbody>
</table>

Table 22: More compression ratios

<table>
<thead>
<tr>
<th>Images</th>
<th>Lossless Compression Ratio</th>
<th>Near Lossless Compression Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$\delta = 1$</td>
</tr>
<tr>
<td>Cameraman</td>
<td>1.5362</td>
<td>2.6265</td>
</tr>
<tr>
<td>Einstein</td>
<td>1.6927</td>
<td>2.6265</td>
</tr>
<tr>
<td>Lena</td>
<td>1.4119</td>
<td>1.9722</td>
</tr>
<tr>
<td>Elaine</td>
<td>1.32</td>
<td>1.8184</td>
</tr>
<tr>
<td>Plus</td>
<td>1.3556</td>
<td>1.6586</td>
</tr>
<tr>
<td>Eye</td>
<td>1.1029</td>
<td>1.4592</td>
</tr>
</tbody>
</table>
Figure 95: Residual input image

Figure 96: Recovered images from ADC
Figure 97: $U$ Average image

Figure 98: $U$ Residual image
Figure 99: $U$ Image

Figure 100: $K$ Average image
Figure 101: $K$ Residual image

Figure 102: $K$ Image
Figure 103: $C$ Average image

Figure 104: $C$ Residual image
Figure 105: $C$ Image
CHAPTER 7

CONCLUSION

We address all the problems we discussed in chapter 1. To summarize the contribution of this work

- The problem of low efficient on-chip solar cell was addressed. With theory and experiments we were able to collect more charges by implementing fractal based geometries on solar cells. We achieved 6% more efficiency.

- Utilizing the residual area around the fractal based photodiode to lay parallel plate capacitors increased the capacitance per unit area by 4%.

- The low output voltage of photodiode was successfully boosted up using external inductors, upto 2.81V, sufficient enough to drive a circuit.

- An ADC that can jointly perform conversion and compression was designed, implemented and tested. We were able to achieve lossless compression ratios up to 1.8 and near lossless 5.2 for 32×32 images. It reduced the over all logic by 50% helping reduce the area and also reducing the total power consumption.
APPENDIX I

The appendix contains details of the chip fabricated

Figure 106: Chip containing ADC and 2nd order koch island fractal shaped diode.
Figure 107: Chip containing ADC and 2nd order koch island fractal shaped diode block diagram.
Table 23: Pin number and function for fig. 106

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Package pin#</th>
<th>Pin Name</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A1</td>
<td>CAP-TOP</td>
<td>Capacitor top plate</td>
</tr>
<tr>
<td>2</td>
<td>C2, C3</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>3-14</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>15</td>
<td>J1</td>
<td>CP-SW1</td>
<td>Charge pump-switch 1</td>
</tr>
<tr>
<td>16</td>
<td>J2</td>
<td>CP-SW2</td>
<td>Charge pump-switch 2</td>
</tr>
<tr>
<td>17</td>
<td>K1</td>
<td>CP-SW3</td>
<td>Charge pump-switch 3</td>
</tr>
<tr>
<td>18</td>
<td>J3</td>
<td>CP-SW4</td>
<td>Charge pump-switch 4</td>
</tr>
<tr>
<td>19</td>
<td>K2</td>
<td>N-FRAC</td>
<td>N-well of Fractal diode</td>
</tr>
<tr>
<td>20</td>
<td>K3</td>
<td>P-FRAC</td>
<td>P-act of Fractal diode</td>
</tr>
<tr>
<td>21</td>
<td>J4</td>
<td>CP-OUT</td>
<td>Charge pump output</td>
</tr>
<tr>
<td>22</td>
<td>K4</td>
<td>CP-SW5</td>
<td>Charge pump-switch 5</td>
</tr>
<tr>
<td>23</td>
<td>K5</td>
<td>CP-SW6</td>
<td>Charge pump-switch 6</td>
</tr>
<tr>
<td>24</td>
<td>J5</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>25</td>
<td>K6</td>
<td>OPAMP-IN(-)</td>
<td>Opamp inverting input</td>
</tr>
<tr>
<td>26</td>
<td>J6</td>
<td>OPAMP-IN(+)</td>
<td>Opamp non-inverting input</td>
</tr>
<tr>
<td>27</td>
<td>K7</td>
<td>OPAMP-BIAS</td>
<td>Opamp bias voltage (0.9V)</td>
</tr>
<tr>
<td>28</td>
<td>J7</td>
<td>OPAMP-OUTPUT</td>
<td>Opam output</td>
</tr>
<tr>
<td>29</td>
<td>K8</td>
<td>ADC-RBIAS</td>
<td>1.13 V (for 0.5μA $I_{LSB}$)</td>
</tr>
<tr>
<td>30</td>
<td>J8</td>
<td>ADC-K2</td>
<td>ADC Resolution MSB</td>
</tr>
<tr>
<td>31</td>
<td>K9</td>
<td>ADC-K1</td>
<td>–</td>
</tr>
<tr>
<td>32</td>
<td>J9</td>
<td>ADC-K0</td>
<td>ADC Resolution LSB</td>
</tr>
<tr>
<td>33</td>
<td>K10</td>
<td>ADC-REFPOS</td>
<td>1.0 V</td>
</tr>
<tr>
<td>34</td>
<td>H9</td>
<td>ADC-IREF-OUT</td>
<td>Output of reference bank</td>
</tr>
<tr>
<td>35</td>
<td>J10</td>
<td>ADC-IREF-IN</td>
<td>Input of reference current into ADC</td>
</tr>
<tr>
<td>36</td>
<td>H10</td>
<td>ADC-AIN</td>
<td>Analog (current) input to ADC</td>
</tr>
<tr>
<td>37</td>
<td>G9</td>
<td>ADC-SW1</td>
<td>Sampling switch</td>
</tr>
<tr>
<td>38</td>
<td>G10</td>
<td>ADC-SW2</td>
<td>Current memory $A_1$ switch, located at drain of transistor</td>
</tr>
<tr>
<td>39</td>
<td>F10</td>
<td>ADC-SW3</td>
<td>Current memory $A_1$ switch, located at gate of transistor</td>
</tr>
<tr>
<td>40</td>
<td>F9</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>Pin#</td>
<td>Package pin#</td>
<td>Pin Name</td>
<td>Comment</td>
</tr>
<tr>
<td>------</td>
<td>--------------</td>
<td>---------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>41</td>
<td>E10</td>
<td>ADC-SW4</td>
<td>Current memory $A_2$ switch, located at drain of transistor</td>
</tr>
<tr>
<td>42</td>
<td>E9</td>
<td>ADC-SW5</td>
<td>Current memory $A_2$ switch, located at gate of transistor</td>
</tr>
<tr>
<td>43</td>
<td>D10</td>
<td>ADC-SW6</td>
<td>Current memory $A_3$ switch, located at drain of transistor</td>
</tr>
<tr>
<td>44</td>
<td>D9</td>
<td>ADC-SW7</td>
<td>Current memory $A_3$ switch, located at gate of transistor</td>
</tr>
<tr>
<td>45</td>
<td>C10</td>
<td>ADC-SW8</td>
<td>Connected between reference current and input current</td>
</tr>
<tr>
<td>46</td>
<td>C9</td>
<td>ADC-NEG</td>
<td>Voltage of inverting terminal of diff. amp (2.6 V)</td>
</tr>
<tr>
<td>47</td>
<td>B10</td>
<td>ADC-PBIAS</td>
<td>Bias voltage of p-input type diff. amp. (4.0 V)</td>
</tr>
<tr>
<td>48</td>
<td>B9</td>
<td>ADC-NBIAS</td>
<td>Bias voltage of n-input type diff. amp. (1.0 V)</td>
</tr>
<tr>
<td>49</td>
<td>A10</td>
<td>ADC-OUT</td>
<td>Output of ADC</td>
</tr>
<tr>
<td>50</td>
<td>B8</td>
<td>CC-VBIAS</td>
<td>Current conveyor bias (4.0 V)</td>
</tr>
<tr>
<td>51</td>
<td>A9</td>
<td>CC-RIN</td>
<td>Resistor input of current conveyor</td>
</tr>
<tr>
<td>52</td>
<td>A8</td>
<td>CC-VCTRL</td>
<td>Voltage of inverting terminal of diff amp. (2.5 V)</td>
</tr>
<tr>
<td>53</td>
<td>B7</td>
<td>CC-IMP-BIAS</td>
<td>Diff. amp bias (2.5 V)</td>
</tr>
<tr>
<td>54</td>
<td>A7</td>
<td>CC-IOUT</td>
<td>Output of current conveyor</td>
</tr>
<tr>
<td>55</td>
<td>A6</td>
<td>VCO-VCTRL</td>
<td>Control voltage for VCO</td>
</tr>
<tr>
<td>56</td>
<td>B6</td>
<td>VCO-OUT</td>
<td>VCO output</td>
</tr>
<tr>
<td>57</td>
<td>A5</td>
<td>VCO-OUT(INV)</td>
<td>VCO output inverted</td>
</tr>
<tr>
<td>58</td>
<td>B5</td>
<td>PG-IN</td>
<td>Pulse generator input</td>
</tr>
<tr>
<td>59</td>
<td>A4</td>
<td>PG-OUT</td>
<td>Pulse generator output</td>
</tr>
<tr>
<td>60</td>
<td>B4</td>
<td>P-RECT</td>
<td>P-act connection of rectangular diode</td>
</tr>
<tr>
<td>61</td>
<td>A3</td>
<td>N-RECT</td>
<td>N-well connection of rectangular diode</td>
</tr>
<tr>
<td>62</td>
<td>B3</td>
<td>CP-IN</td>
<td>Charge pump input</td>
</tr>
<tr>
<td>63</td>
<td>A2</td>
<td>CP-VDD</td>
<td>Charge pump VDD</td>
</tr>
<tr>
<td>64</td>
<td>B2</td>
<td>CAP-BOT</td>
<td>Capacitor bottom plate</td>
</tr>
</tbody>
</table>
Figure 108: Bonding diagram
Figure 109: Package diagram
Figure 110: Chip containing solar cells and charge pump/boost converter circuit.
Table 25: Pin number and function for fig. 110

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Package pin#</th>
<th>Pin Name</th>
<th>Comment</th>
</tr>
</thead>
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<tr>
<td>1, 3-4</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>J11</td>
<td>P-FRAC(3)</td>
<td>P-act of Fractal diode</td>
</tr>
<tr>
<td>8</td>
<td>J12</td>
<td>N-FRAC(3)</td>
<td>N-well of Fractal diode</td>
</tr>
<tr>
<td>9-10</td>
<td>H10-H11</td>
<td>CAP(2/3)</td>
<td>133.564pF</td>
</tr>
<tr>
<td>11-12</td>
<td>H12-G10</td>
<td>CAP(3/3)</td>
<td>115.917pF</td>
</tr>
<tr>
<td>13-14</td>
<td>G11-G12</td>
<td>CAP(1/4)</td>
<td>144.745pF</td>
</tr>
<tr>
<td>15-16</td>
<td>F10-F11</td>
<td>CAP(2/4)</td>
<td>90.2512pF</td>
</tr>
<tr>
<td>17</td>
<td>F12</td>
<td>N-STRIP</td>
<td>N-well for strip type diode</td>
</tr>
<tr>
<td>18</td>
<td>E10</td>
<td>P-STRIP</td>
<td>P-act for strip type diode</td>
</tr>
<tr>
<td>19-20</td>
<td>E11-E12</td>
<td>CAP(3/4)</td>
<td>120.563pF</td>
</tr>
<tr>
<td>21-22</td>
<td>D10-D11</td>
<td>CAP(4/4)</td>
<td>132.237pF</td>
</tr>
<tr>
<td>23-24</td>
<td>D12-C10</td>
<td>CAP(1/1)</td>
<td>131.9163pF</td>
</tr>
<tr>
<td>25-26</td>
<td>C11-C12</td>
<td>CAP(2/1)</td>
<td>131.9163pF</td>
</tr>
<tr>
<td>27-28</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>29</td>
<td>B11</td>
<td>VDD</td>
<td>VDD</td>
</tr>
<tr>
<td>30</td>
<td>A11</td>
<td>N-FRAC</td>
<td>N-well for fractal diode</td>
</tr>
<tr>
<td>31</td>
<td>B10</td>
<td>P-FRAC</td>
<td>P-act for fractal diode</td>
</tr>
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<td>A10-C9</td>
<td>CAP(3/1)</td>
<td>131.9163pF</td>
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<tr>
<td>34-35</td>
<td>B9-A9</td>
<td>CAP(4/1)</td>
<td>131.9163pF</td>
</tr>
<tr>
<td>36-37</td>
<td>C8-B8</td>
<td>CAP(1/3)</td>
<td>144pF</td>
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<tr>
<td>38-39</td>
<td>A8-C7</td>
<td>CAP(1/2)</td>
<td>60.5103pF</td>
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<tr>
<td>40-41</td>
<td>B7-A7</td>
<td>CAP(2/2)</td>
<td>134.881pF</td>
</tr>
<tr>
<td>42</td>
<td>C6</td>
<td>N-RECT</td>
<td>N-well for rectangular diode</td>
</tr>
<tr>
<td>43</td>
<td>B6</td>
<td>P-RECT</td>
<td>P-act for rectangular diode</td>
</tr>
<tr>
<td>44-45</td>
<td>A6-C5</td>
<td>CAP(3/2)</td>
<td>125.511pF</td>
</tr>
<tr>
<td>46-47</td>
<td>B5-A5</td>
<td>CAP(4/2)</td>
<td>122.316pF</td>
</tr>
<tr>
<td>48-49-50</td>
<td>C4-B4-A4</td>
<td>NMOS-SW1</td>
<td>NMOS switch (d-g-s)</td>
</tr>
<tr>
<td>51-52-53</td>
<td>C3-B3-A3</td>
<td>NMOS-SW2</td>
<td>NMOS switch (d-g-s)</td>
</tr>
<tr>
<td>54-64</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>65-66-67</td>
<td>E1-F3-F2</td>
<td>NMOS-SW3</td>
<td>NMOS switch (d-g-s)</td>
</tr>
<tr>
<td>68-69-70</td>
<td>F1-G3-G2</td>
<td>NMOS-SW4</td>
<td>NMOS switch (d-g-s)</td>
</tr>
<tr>
<td>Pin#</td>
<td>Package pin#</td>
<td>Pin Name</td>
<td>Comment</td>
</tr>
<tr>
<td>------</td>
<td>--------------</td>
<td>----------</td>
<td>---------</td>
</tr>
<tr>
<td>71</td>
<td>G1</td>
<td>NMOS-VDD</td>
<td>NMOS switches are isolated from the surrounding circuits using VDD ring</td>
</tr>
<tr>
<td>72</td>
<td>H3</td>
<td>NMOS-GND</td>
<td>Substrate surrounding NMOS switches are grounded</td>
</tr>
<tr>
<td>73</td>
<td>H2</td>
<td>PMOS-GND</td>
<td>PMOS switches are isolated from the surrounding circuits using GND ring</td>
</tr>
<tr>
<td>74</td>
<td>H1</td>
<td>PMOS-VDD</td>
<td>Substrate surrounding PMOS switches are connected to VDD</td>
</tr>
<tr>
<td>75</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>76</td>
<td>J2</td>
<td>TS-VDD(ext)</td>
<td>External guard ring for transmission gate switches connected to VDD</td>
</tr>
<tr>
<td>77</td>
<td>J1</td>
<td>TS-GND(ext)</td>
<td>External guard ring for transmission gate switches connected to GND</td>
</tr>
<tr>
<td>78</td>
<td>K3</td>
<td>TS-GND(int)</td>
<td>Internal GND of transmission gate switches</td>
</tr>
<tr>
<td>79</td>
<td>K2</td>
<td>TS-VDD(int)</td>
<td>Internal VDD of transmission gate switches</td>
</tr>
<tr>
<td>80, 84-85</td>
<td>K1, M2-L3</td>
<td>TS-SW1</td>
<td>Transmission gate switch (I/O-I/O-G)</td>
</tr>
<tr>
<td>81-82</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>83</td>
<td>L2</td>
<td>GND</td>
<td>Chip ground</td>
</tr>
<tr>
<td>86-87-88</td>
<td>B8</td>
<td>TS-SW2</td>
<td>Transmission gate switch (I/O-I/O-G)</td>
</tr>
<tr>
<td>89-90-91</td>
<td>M4-K5-L5</td>
<td>TS-SW3</td>
<td>Transmission gate switch (I/O-I/O-G)</td>
</tr>
<tr>
<td>92-93-94</td>
<td>M5-K6-L6</td>
<td>TS-SW4</td>
<td>Transmission gate switch (I/O-I/O-G)</td>
</tr>
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<td>95-98</td>
<td>–</td>
<td>Not connected</td>
<td>Not connected</td>
</tr>
<tr>
<td>99, 103-104</td>
<td>K8, L9-M9</td>
<td>PMOS-SW1</td>
<td>PMOS type switch (g,d-s)</td>
</tr>
<tr>
<td>100, 105-106</td>
<td>L8, K10-L10</td>
<td>PMOS-SW2</td>
<td>PMOS type switch (g,d-s)</td>
</tr>
<tr>
<td>101, 107, 2</td>
<td>M8, M10-L1</td>
<td>PMOS-SW3</td>
<td>PMOS type switch (g,d-s)</td>
</tr>
</tbody>
</table>
Figure 111: Bonding diagram
Figure 112: Package diagram
REFERENCE LIST


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[71] Shao, H., Tsui, C.-Y., and Ki, W.-H. An inductor-less micro solar power management system design for energy harvesting applications. In Circuits and Systems,


VITA

Suvradip Ghosh was born on August 2, 1982 in Tamil Nadu, India. He graduated high school in May 1999 from Kendriya Vidyalaya Vayu Sena Nagar, Nagpur, Maharashtra, India. He attended Sri Ramdeobaba College of Engineering and Management, affiliated to Nagpur university, from 1999-2003 where he graduated with his Bachelor of Science degree in electrical engineering.

He worked for Cognizant Technology Solutions, Hyderabad, India as programmer analyst from May 2004 until July 2006.

From fall 2006, he attended University of Missouri-Kansas City for his Master of Science degree. In fall 2009, he joined the Ph.D. program. His primary discipline for Ph.D. was electrical engineering with physics as co-discipline. He graduated with Ph.D. degree in December 2013. He is currently working as memory design engineer.