SILICON CARBIDE AS A PHOTO CONDUCTIVE SWTICH MATERIAL FOR HIGH POWER APPLICATIONS

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SILICON CARBIDE AS A PHOTOCONDUCTIVE SWITCH MATERIAL FOR HIGH POWER APPLICATIONS

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ABSTRACT

High voltage, high current, low inductance, fast resistive transition, and precise control are the critical component parameters of a semiconductor switch that can enable the fielding of a compact pulse power system. Extrinsic, semi-insulating Silicon Carbide (SiC) photo-conductive switches have the potential to fulfill these critical requirements. The availability of this type of switch also enables innovative approaches to pulse power system design and implementation.

This research work discusses the effort at the Electrical and Computer Engineering (ECE) department at the University of Missouri Columbia (UMC) in developing this technology through simulation and experiments with SiC material. Specifically, the rationale for employing extrinsic photo-conductivity, as well as the role of compensation mechanisms have been demonstrated, modeled, and analyzed. The device material fabrication methods and package structures developed to date are discussed. The behavior and the response of two compensated structures are discussed in terms of recombination time and optical sensitivity. Material characterization showing agreement with the experimental results was based on choosing the right parameters on trap levels and compensation mechanisms. The experimental switching results with both intrinsic and compensated SiC photo switches using sub-bandgap photon energy for code calibration and high power PCSS analysis are presented and compared with

semiconductor physics models. The methods used to determine the density and recombination cross section of interband dopants are also presented.

Analyses show that premature breakdown occurs primarily due to impact ionization and subsequent charge accumulation near the anode. For the shallow donor, deep acceptor type compensated material, a p^+ layer next to the cathode results in field homogenization in the bulk. As a result the hold off voltage of the switch is improved by many orders of magnitude. The minimum thickness of the p^+ layer necessary to avoid premature breakdown is also discussed.

The transient response with the improved switch configuration was studied in detail to find out the effectiveness of the p^+ layer in improving the performance with laser illumination. Initial kinks observed in the photocurrent with the blocking contact have been studied and are presented here. The reasons were analyzed and a remedy has been suggested.

Chapter 1

Introduction

A continuing theme in the development of a compact pulsed power electrical system is to design the perfect switch. Perfection is an unobtainable goal but a switch that can efficiently work on a broader range of applications is a significant step towards that goal. The purpose of this chapter is to give a perspective on the applications of switches in high power generation along with the advantages of using photo conductive semiconductor switches (PCSS) in these applications.

A switch should satisfy certain criteria, perhaps a "wish list" for being called an ideal switch. No single switch can satisfy all the requirements; kilovolts to megavolts operating range, kilo to mega amperes of current handling capabilities, sub-nanosecond to millisecond pulse lengths, more than hundred million pulses lifetime, single pulse to gigahertz frequency range, less than a picosecond risetime, higher efficiencies, reliable, compact size, and low cost, but should be able to satisfy the basic requirements of the application.

Pulse power switches have traditionally been gas discharge devices [1] such as thyratrons and spark gaps. They have been implemented in high power pulsed lasers, power conditioning systems, impulse radar, high power microwave generators, and various other applications. Disadvantages of these switches, however, include large size, jitter, longer onset times, limited power handling capabilities, maintenance and the like

etc. Optically activated semiconductor switches, on the other hand, offer a number of advantages over these conventional switches such as picosecond jitter, nanosecond closure, a higher current density, a controllable current conduction time, a high blocking electric field, an improved voltage level, the simultaneous or phased closure of many switches, small size and low loss conduction. These advantages make optically activated switches a desirable component in these applications.

There exists a wide variety of optically activated switches available e.g. PIN diodes, Metal semiconductor field effect transistor (MESFET), Optothyristors and PCSSs. PIN diodes have limited power handling capabilities because of the junction limitation. MESFET's have a moderate current capacity while performance is limited by gate capacitance. Optothyristors can handle a large current, but have longer turn on times. Since a PCSS can handle much higher powers (MW) along with a nanosecond risetime and controllable pulse width, it has been selected for this research.

An application of using a PCSS is in the stacked Blumlein line pulse generator module which requires a relatively short (ps to 10s of ns) pulse. A stacked Blumlein generator consists of a number of Blumlein line pulse generator modules as illustrated in Fig. 1.1 [2]. Each Blumlein module determines the length of the output pulse while the optical switch closure determines the rise time of the pulse. In the matched load case, the output voltage is equal to input voltage for the single Blumlein module case. N Blumlein modules can be connected in series to produce an output voltage into a matched load of NZ_0 of NV_1 where Z_0 and V_1 are the characteristic impedance and voltage of each Blumlein module.

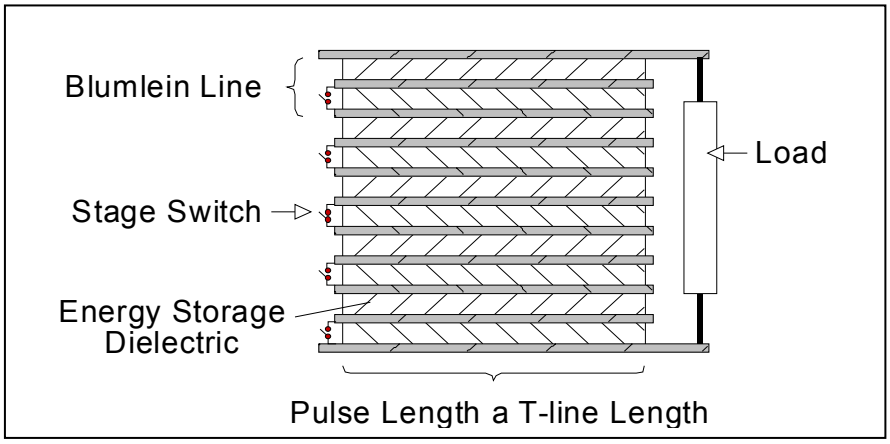


Figure 1.1. A photo conductively switched stacked Blumlein

This research effort is directed towards the development of a photoconductive semiconductor switch that can satisfy the design criterion of optimum operation of a pulsed power system. Specifically the design and fabrication of a SiC PCSS is the ultimate goal of this work. However, a brief history, analysis and the research development of other semiconductor materials is also provided in order to maintain continuity.

The organization of the rest of the thesis is as follows. Chapter 2 briefly explains the fundamental operation of a PCSS along with the different types available and the theory based on much earlier work by Lampert et al explaining the fundamentals of current injection in solids. Chapter 3 presents literature review, where the performance of a working GaAs PCSS is summarized with a brief introduction of semi insulating materials. Chapter 4 describes the advantages of using SiC over GaAs, University of Missouri (UMC) switch geometry design, and the mathematical modeling of the switch. Chapter 5 explains the importance of material characterization using different approaches

and preliminary switch simulation data that includes the effect of Fermi level on material response. Chapter 6 presents the experimental transient response for a low bias and its use in calibrating the simulation code. This provides insight in predicting high voltage switch behavior as is explained in Chapter 7. This is followed by conclusions and a discussion of future work in Chapter 8.

Chapter 2

Background

Semiconductor materials can be classified, depending on the response of the material to majority carrier injection, as a relaxation type and lifetime type. In case of the relaxation type behavior in which the Debye length is much greater than the diffusion length ($L_D >> L_O$), the injection of majority carriers leads to majority carrier depletion; for the lifetime type materials ($L_O >> L_D$), it leads to majority carrier augmentation. The behavior of a semiconductor is further complicated by the presence of traps sites. Henisch and coworkers have shown that the depletion of majority carriers upon injection of minority carriers is greatly reduced when a large density of traps exists; then, the material behaves as a lifetime type instead of the relaxation type. Thus, traps affect the material behavior by modifying the space charge and electric field distribution as well as providing an alternative recombination-generation mechanism affecting the lifetime of the carriers. The high resistivity, compensated materials used for photoconductive semiconductor switches (PCSS's), infrared detectors and the like etc. are lifetime type semiconductors. Hence, a further study of this material type is necessary in order to understand and predict the correct response of the PCSS. This chapter starts with the working principle of a PCSS device and the different types available. It then explains the effect of the location of trap level on the material response. An old theory devised in the

1960's is then revisited with a brief summary of the behavior of high resistivity materials in the presence of traps.

2.1. Photoconductive Semiconductor Switch (PCSS) Theory

The basic optically controlled semiconductor switch [3] is used to connect a source to a load.

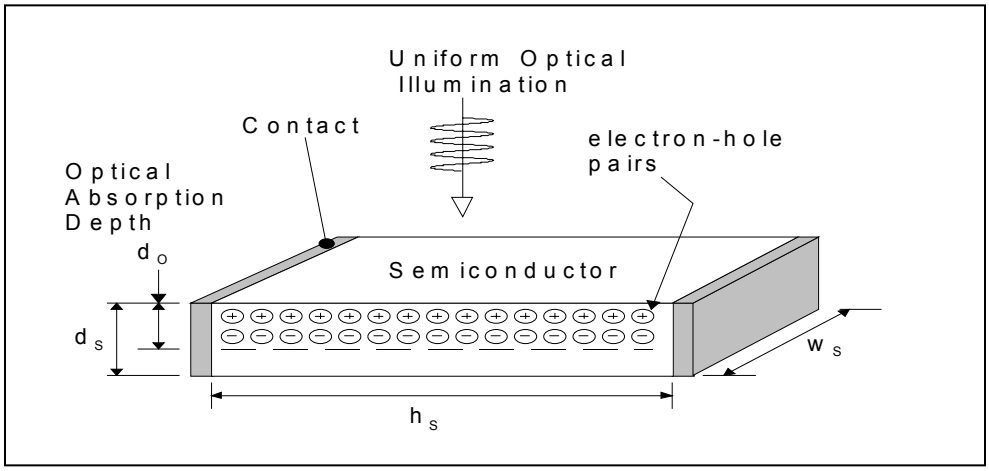


Figure 2.1. Illustration of Photoconductive Switch

The PCSS shown in Fig. 2.1 consists of a block of semiconductor material of height h_s, width w_s and thickness d_s. Thickness d_s should be greater than or equal to the optical absorption depth, d_o, to ensure that all of the optical energy is being absorbed in the bulk of the switch. The length of the switch h_s is determined by the dielectric strength of the semiconductor surface in Fig. 2.1. The width, w_s, of the switch is determined by the current density required to avoid filamentary conduction, where a smaller area carries a large amount of current. The planer, insulating, photoconductive medium is changed into a conductor by illuminating the face of the switch with a uniform optical intensity source between the contacts.

2.1.1. Types of Photoconductive semiconductor switches

2.1.1.1. According to the mode of operation

1. Linear photoconductive semiconductor switch

The linear mode is characterized by one electron hole pair produced for each photon absorbed. Therefore the conductivity of the material is, to the first order, linearly proportional to the total photon flux illuminating the semiconductor material and the switch conductivity approximately follows the shape of the optical drive pulse. The switch closes as the optical intensity increases, remains closed while illuminated, and opens with characteristic time constant related to the carrier lifetimes after the optical pulse is removed.

2. Non-linear photoconductive semiconductor switch

In GaAs, when the bias electric field across the switch exceeds approximately 4-8 kV/cm, a transition occurs to a nonlinear mode that exhibits high gain and extended conduction. This is referred to as lock-on [4]. In lock-on, the field across the switch drops to 3-5KV/cm but the current does not decrease and continues to flow as if it has locked on to a value. In lock-on the laser pulse can, if strong enough, determine the closing time of the switch, as in the linear mode, but the switch then remains closed or "locked-on" until the current is interrupted by the circuit. In summary, when the non linear electric field threshold for GaAs is reached, the turn-on speed of the switch is determined by the avalanche process, in which carriers are generated by impact ionization, independent of the laser rise time. The pulse amplitude locks on to a characteristic electric field until the current through the switch is turned off. If the laser

rise time is faster than the avalanche rise time and the laser amplitude is high enough, the optically generated carriers can dominate, and the switch turn-on is faster than its characteristic avalanche time. The switch will still lock on even though the optical pulse from the laser may have ended.

The mechanisms leading to avalanche such as risetime and lock-on are not well understood. Theoretically, several explanations can be found for this non-linear switching behaviour. Trap filling and impact ionization of traps are among the possible explanations [5, 6].

2.1.1.2. According to the geometry

1. Lateral Switch

The switch geometry is as shown in Fig. 2.2.

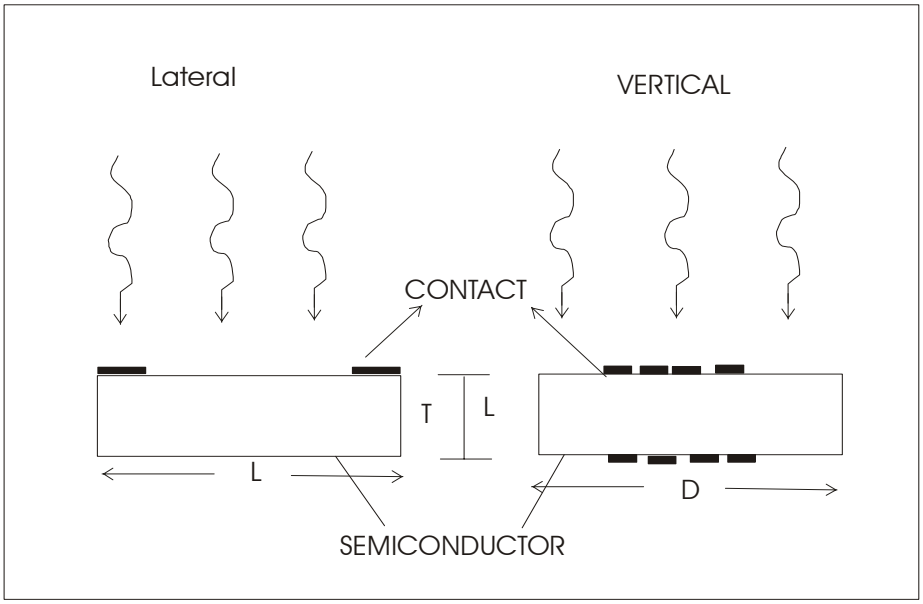


Figure 2.2. PCSS switch configurations

This represents simplest design to couple optical energy into the switch. It is easy to diagnose and understand. Whether the light is absorbed in a few micrometers or several hundred micrometers, all of it is absorbed in the active region of the switch. For uniformly illuminated linear switch, the minimum switch resistance is reached immediately. Space charge or transit time limited current flow is not an issue. In a uniformly illuminated, lateral, linear switch, the peak current and rise time depend only on the magnitude and shape of the optical pulse, the carrier recombination time, and the configuration of the switch in an external circuit. A disadvantage of the lateral switch geometry is the exposure of the wafer surface to the maximum electric field. Electrical breakdown is usually significantly lower than the bulk electrical breakdown strength of the material.

2. Vertical Switch

A configuration that increases the voltage hold-off (level of voltage it can sustain before breaking down) of a PCSS by reducing fields near the switch surfaces is the vertical configuration as shown in Fig. 2.2. The first obstacle to such geometry is that, at least one of the electrical contacts to the switch must be transparent to the optical trigger. This problem is overcome with a metallic grid, very thin metallic layers, or epitaxially grown, doped semiconductor layers. The absorption depth of the optical trigger plays an important role. For a linear PCSS, if all the carriers are created or injected near the contact, a prompt displacement current will be seen, but “closure” of the switch will not occur until a path of carriers crosses the gap. Careful tuning of the trigger wavelength to the switch thickness might optimize switching efficiency and rise times, but different

wavelengths or different materials would be required to produce different size switches to handle different peak voltages.

2.1.2. Photoconductivity

Photoconductivity can be of two types:

1. If the photon energy is greater than the band gap then it is called Intrinsic photoconductivity.
2. If the photon energy is less than the band gap, i.e. if traps are used to generate the free carriers, then it is called as Extrinsic photoconductivity

2.1.3. Linear Switch On-Off Resistance:

The open or off state resistance, R_{so} of the switch is determined by the dark or steady state resistivity of the semiconductor slab, ρ_o or

$$R_{so} = \frac{\rho_o . h_s}{w_s . d_s} \tag{2.1}$$

This naturally leads to the requirement that the semiconductor material be intrinsic or compensated such that the dark resistivity is large and the corresponding open resistance is large.

The conduction or on state resistance of the PCSS is given by [7]

$$R_c = \frac{h_s^2 . E_p}{(1-r).\mu_s . q_e . E_o} \tag{2.2}$$

Under the assumption that material recombination time T_r is much greater than the electrical pulse.

where h_s = Height of Switch in cm

E_p = Photon Energy in eV

q_e = electron charge in C

E_o = Total optical energy incident of the photo switch in J

μ_s = Sum of hole and electron mobilities in cm^2/V-s

r = Surface reflection coefficient

If the time resolution of the pulse is greater than the recombination time T_r then switch waveform follows the light pulse.

$$R_c = \frac{h_s^2 . E_p}{(1-r).\mu_s . q_e . T_r . E_o} \tag{2.3}$$

The plot of the change in resistance with the electrical pulse width is shown in Figure 2.3.

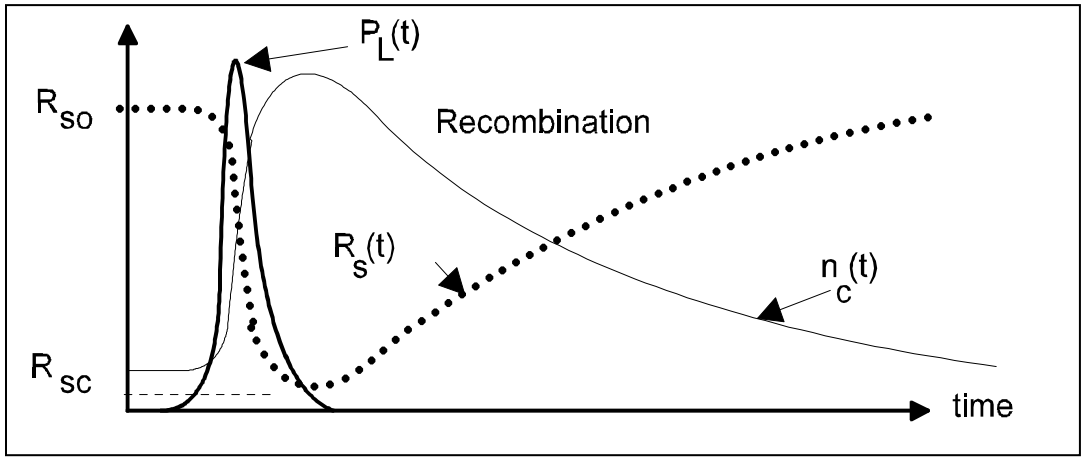


Figure 2.3. Effect of illumination on switch resistance $R_s(t)$, carrier generation $n_C(t)$ with optical illumination $P_L(t)$ [7]

The switch opening time is dependent on the material recombination time as mentioned in Fig. 2.3. The design of the switch conduction resistance is a trade-off between low switch resistance and the energy required to obtain a low switch resistance. A linear photo-switch is desirable because the conduction resistance, the current density, and the

conduction time can be determined by controlling the optical source and the material recombination time.

2.2 Theory of Current Injection in Solids

Many experimental methods have been developed to characterize a semiconductor material with respect to its doping. Some of these techniques include Hall effect measurement, geometric magneto resistance, capacitance voltage profiling and space charge limited current injection. One of these techniques, the space charge limited current injection in solids is discussed in detail by M A Lampert [8]. Injection currents in an insulator can be a powerful probe in the study of insulators. Their major contribution is obtaining information about defect states in the forbidden gap. The current voltage characteristics can be used to obtain the nature of a particular defect state in the material along with its location with respect to the band edges.

In this chapter single carrier injection into an insulator will be considered and an understanding of the theory of current injection with emphasize on the defect states in the material will be developed. Then, two carrier injection effects will be briefly discussed.

2.2.1. Perfect Insulator:

First, consider the perfect insulator, free of traps with a negligible concentration of free carriers at thermal equilibrium. Diffusive currents in the bulk will be neglected. Note that diffusion is more prominent in the vicinity of the contacts and neglecting these current does not affect the bulk properties of the insulator. Then, one can write the current density as

$$J = \rho\upsilon = Q/t \tag{2.4}$$

where ρ is the average injected free charge concentration, υ is the average drift velocity of the free electrons, Q is the total injected free charge per unit area between the cathode and the anode.

The quantities, υ and t, and ρ and Q are related by

$$t = L/\upsilon \text{ and } Q = \rho L \tag{2.5}$$

where L is the distance between the anode and the cathode.

From elementary electrostatics it is known that the total charge put unit area on the plate of a parallel plate capacitor is given by

$$Q_0 = C_0 V \text{ and } C_0 = \varepsilon / L \tag{2.6}$$

where ε is the dielectric constant of the medium between the plates.

Substituting Q and C_0 from Eq. 2.6 into Eq. 2.5 and then into Eq. 2.4, the result is

$$J = \varepsilon\upsilon V / L^2 \tag{2.7}$$

The electron drift in the conduction band of the solid is marked by frequent collisions with the thermal vibrations, the impurities and structural defects in the solid. As field strengths not strong enough for the non linear effects, one can write

$$\upsilon = \mu E = \mu(V/L) \text{ and } t = L^2/\mu\upsilon \tag{2.8}$$

Substituting Eq. 2.8 in Eq. 2.7, the result is

$$J = \varepsilon\mu(V^2/L^3) \tag{2.9}$$

Eq. 2.9 is the limiting form of the current-voltage characteristics for an imperfect insulator at an applied voltage that is high enough so that the total number of injected electrons exceeds the total number of initially empty electron traps in the material. This

represents the highest one carrier injection current that a given insulator with a specific cathode to anode spacing can carry.

2.2.2 The trap free insulator with thermal free carriers

The next step in complexity is the inclusion of thermally free carriers (n_0) to the problem of Section 2.2. A possible source of such electrons is the shallow donor trap level that is so close to the conduction band that they can be assumed to be completely ionized at room temperature.

Ohm's law will be observed at low voltages and is given as

$$J = en_0\mu(V / L) \tag{2.10}$$

As the voltage in increased, the injected charge increases. Once the injected electron concentration, n_i, becomes comparable to the thermally generated free carrier concentration, n_0, one can expect departure from Ohm's law to the trap free square law.

The crossover voltage from Ohm's law to the trap free square law is given by

$$V_X = (en_0L^2 / \varepsilon) \tag{2.11}$$

2.2.3. Insulator with traps

The presence of electron traps in the insulator results in greatly reduced current at low voltages because the injected carriers get captured by initially empty electron traps thus immobilizing them. On the other hand, the amount of excess charge that can be supported by an insulator at an applied voltage is the same whether the charge is trapped or free.

Thus, for a parallel plate condenser one can now write

$$Q = (\rho + \rho_t)L = C_0 V = (\varepsilon / L)V \tag{2.12}$$

where ρ_t is the average, injected trapped charge concentration.

The appropriate form of current voltage characteristics can be obtained by considering the relationship between the trapped and free electron concentrations. This relationship can be expressed using the thermodynamic Fermi level, F_0. For non degenerate semiconductors, the free electron concentration at thermal equilibrium is given by

$$n_0 = N_C \exp[(F_0 - E_C)/kT] \tag{2.13}$$

where N_C is the effective density of states in the conduction band, E_C is the lowest level of the conduction band energy, k is Boltzmann's constant, and T the temperature in Kelvin. The concentration of the filled traps, $n_{t,0,}$ is then given by

$$n_{t,0} = \frac{N_t}{1 + (1/g)\exp[(E_t - F_0)/kT]} \tag{2.14}$$

where N_t is the concentration of traps and g is the degeneracy factor for the traps.

A crucial factor to remember is that this theory does not consider the change in the trap cross section with respect to the electric fields that are assumed to be constant. Thus, the balance between the free and trapped electrons is reached as if the crystal were in thermal equilibrium, only with the free electron concentration n, achieved under injection instead of the true thermal equilibrium, n_0. The corresponding Fermi level is called Quasi Fermi level. Thus,

$$n = n_i + n_0 = N_C \exp[(F - E_C)/kT] \tag{2.15}$$

$$n_t = n_{t,i} + n_{t,0} = \frac{N_t}{1 + (1/g)\exp[(E_t - F)/kT]} \tag{2.16}$$

where n_i is the average excess injected free electron concentration and $n_{t,i}$ is the average, injected, excess trapped electron concentration.

2.2.4 Shallow Traps

An electron trap at energy level E_t is said to be shallow if F lies below E_t (E_t-F/kT>1). Therefore, from Eqn. 2.16 we can write,

$$\frac{n}{n_t} = \frac{N_C}{gN_t}\exp\left(\frac{E_t - E_C}{kT}\right) = \theta \tag{2.17}$$

where θ is a constant, independent of the injection level, as long as the trap remains shallow. The shallow traps of concentration N_t substantially affect the space charge limited injection current if θ<<1. Eqn 2.12 can then be written as

$$Q = \rho_t L = \rho L/\theta = (\varepsilon/L)V \tag{2.18}$$

From Eqns 2.4, 2.9 and 2.18 one we can write

$$J = \theta\varepsilon\mu\left(\frac{V^2}{L^3}\right) \tag{2.19}$$

This has the effect of changing the slope of the IV characteristics.

If the Fermi level F is below the trap level as is the case for shallow traps, it keeps on rising as the injection of carriers increases. At some voltage V it will cross the trap level E_t. This cross over will change the slope of the IV characteristics so that now, most of the trap levels are filled completely and so that the injected charge will directly account for the increased current flow. The voltage at which this happens is called $V_{TFL,}$ and this phenomenon is named the Trap Filling Limited (TFL) law (Fig. 2.4a).

For a shallow trap level case, from Eqns 2.10, 2.19 at crossover one can write

$$V_X = (en_0L^2/\theta\varepsilon) \tag{2.20}$$

2.2.5 Deep Traps

An electron trap is said to be deep if F lies below E_t : $\frac{E_t - F}{kT} < 1$. In thermal equilibrium, the number of traps not occupied by electrons (hole occupancy) is given by

$$p_{t,0} = N_t - n_{t,0} \cong \frac{N_t}{g} \exp\left(\frac{E_t - F_0}{kT} \right) \tag{2.21}$$

As mentioned for the shallow trap case, Ohm's law will apply until the thermally free carrier concentration, $n_{0,}$ is higher than the injected free electron charge, n_i. Once these two become comparable, there will be an upwards shift in the quasi Fermi level from the Fermi level. Since the free electron concentration $n = n_i + n_0$ doubles at the cross over point, there will be a shift in the quasi Fermi level location precisely by 0.7kT. This motion is sufficient to fill all the deep traps. The cross over voltage V_x is

$$V_X \cong \frac{Q_{TFL}}{C_0} \cong \frac{ep_{t,0}L^2}{\varepsilon} \tag{2.22}$$

where the subscript TFL is used to denote the trap filled limit.

The behaviour of the deep and shallow trap levels is shown in Fig. 2.4. In both cases one starts with Ohm's law characteristics (Eqn. 2.10). In the case of deep traps (Fig. 2.4a), the cross over voltage V_x (Eqn. 2.22), is obtained when n_i becomes equal to n_0. Then, this characteristic coincides with the trap free square law (Eqn. 2.11).

In case of shallow traps, after following Ohm's law, the current follows the square law given by Eqn. 2.19. Once the Fermi level crosses energy level E_{t2} (Fig. 2.4b), V_{TFL2}, this characteristic merges with the trap free square law.

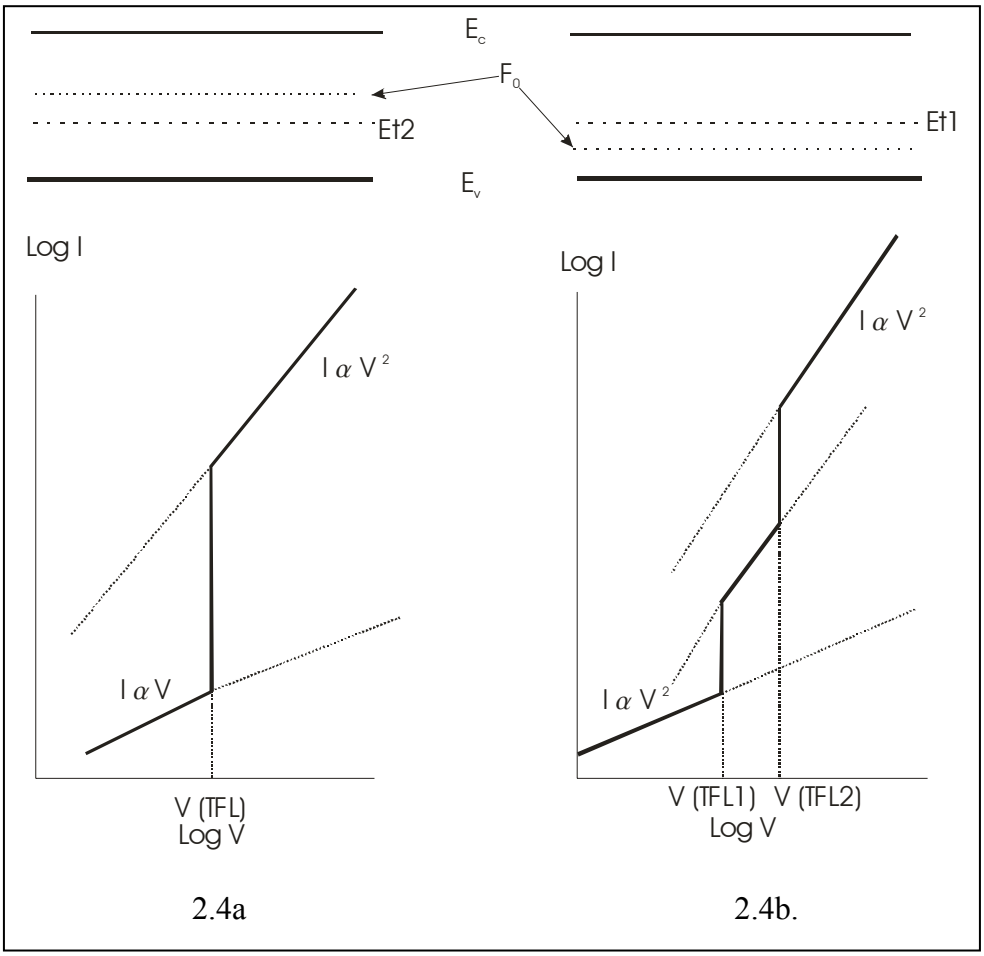


Figure 2.4. IV characteristics for a deep (2.4a) and shallow trap (2.4b) respectively

2.2.6. Two carrier injection

By making one contact to the semiconductor or insulator hole injecting and the other one electron injecting it is possible to obtain double injection. Because the injected electrons and holes can largely neutralize each other, a two carrier injection current will be larger than either single carrier current. A new limitation arises because of the presence of carriers of both polarities, namely Recombination. The carriers can recombine before they complete their respective transits between the cathode and the

anode. The recombination can be a two step process through a localized recombination center N_R as shown in Fig. 2.5 [8].

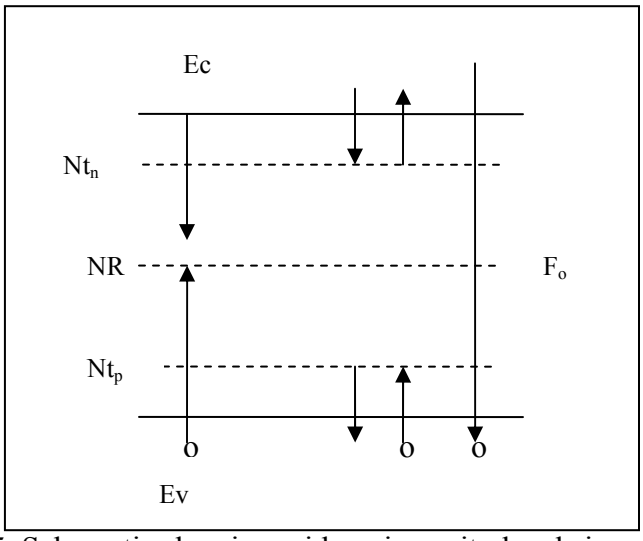


Figure 2.5. Schematic showing midgap impurity levels in a semiconductor. N_{tn} denotes electron traps, N_{tp} denotes hole traps and N_R denotes recombination centers

First a center captures an electron, then a hole or vice versa. In the steady state the capture of electrons and the capture of holes by corresponding recombination centers are equal because of the kinetic equilibrium requirement. The capture can be a single step process directly across the bandgap. The localized electron and hole traps are shown in Fig. 2.5. There can be a tri-molecular recombination process (Auger Recombination). It is generally present at high carrier concentration ($\sim 10^{18}/cm^3$). Hence, it is neglected for the current analysis.

Two factors arise when one tries determine what limits the current flow in an insulator, either recombination or charge neutralization or both. To understand this in more detail one can start with double carrier injection in an insulator.

2.2.7. Plasma injected into an insulator

It is assumed that the total numbers of electrons and holes are equal and that they have equal lifetimes. The concentration of defect states is also assumed to be negligible initially. The total current density is the sum of the electron and hole current densities, which is given as

$$J = en(\upsilon_n + \upsilon_p) \tag{2.23}$$

where v_n and v_p are the average electron and hole drift velocities, respectively.

n = p is the condition for injected plasma.

The relationship between injected charge and voltage is same as before in Section 2.2 namely,

$$Q = \rho L \cong C_0 V = (\varepsilon / L)V \tag{2.24}$$

To obtain the current-voltage characteristics it is necessary to obtain the relationship between the injected charge Q and the current density.

The plasma is non-neutral because the carriers injected at cathode and anode, must travel a finite distance before they can recombine. Hence, define

$$\delta = Q / enL \cong (t_n + t_p) / \tau \tag{2.25}$$

where t_n and t_p are the electron and hole transit times, respectively, and τ is the common average lifetime for the injected electrons and holes.

The smaller the lifetime, the greater will be recombination; hence the greater the departure from neutrality. On the other hand, the smaller the transit time, the more carriers can survive recombination, achieving neutralization.

$$Q \approx enL[(t_n + t_p) / \tau] \tag{2.26}$$

Noting that $t_n = L/v_n$ and $t_p = L/v_p$, and combining Eqns, 2.24-2.26,

$$J \approx \varepsilon \tau \mu_n \mu_p \frac{V^3}{L^5} \tag{2.27}$$

Equation 2.27 is called the double injection cubic law and is the limiting current in a semiconductor or insulator. Similar treatment can be given for semiconductor injected plasma with the only difference being the inclusion of finite thermally free carrier concentration. Due to the added terms n_0, p_0 representing equilibrium electron and hole concentrations respectively, one obtains [8]

$$J \approx e(n_0 - p_0)\tau \mu_n \mu_p (\frac{V^2}{L^3}) \tag{2.28}$$

Eqns 2.27 and 2.28 indicate the maximum two carrier injection current in an insulator and semiconductor, respectively, before breakdown occurs.

Chapter 3

Material Properties and PCSS literature

In the last chapter, the basic of a PCSS along with the current injection theory in solids that limits the total current flow in a semiconductor was discussed. In this chapter the material properties of some basic PCSS materials namely Si, GaAs and SiC will be considered. After an understanding of the compensation mechanisms and the Fermi level is established, the details of some specific PCSS literature that was a vital point in this study will be explored.

3.1 Material Properties

Two semiconductor materials are commonly used for high speed photoconductive switches - Silicon and Gallium Arsenide. These materials are commonly used by the semiconductor industry, and considerable effort has gone into their study. A third material of promise is SiC because of its high voltage hold-off and superior thermal properties.

3.1.1 Silicon

Silicon is most thoroughly understood semiconductor material. Silicon has a band gap of approximately 0.9eV. It strongly absorbs Nd:YAG laser light at wavelength,

λ = 1.06 μm. The absorption depth at this wavelength is 1mm. Being an indirect bandgap material Si has a long (microsecond to millisecond) carrier lifetime t_R and is useful for producing wide electrical pulses using narrow nanosecond optical pulses. Two drawbacks of Si are its high leakage current and thermal runaway. Properties of Si are given below in Table 3.1[9].

Properties	Si
Band Gap	1.12 eV
Critical breakdown field strength	$3x10^5$ V/cm
Electron mobility	1500 cm^2/V-s
Hole mobility	600 cm^2/V-s
Saturation velocity	$2x10^7$ cm/s
Thermal conductivity	1.45 watt/cm°C
Intrinsic carrier concentration	$1.6x10^{10}$ cm^{-3}
Work function	4.8 eV
Dielectric constant	11.8

Table 3.1. Properties of Si at 300 K

3.1.2 GaAs

GaAs has a bandgap of approximately 1.42eV, which corresponds to an optical absorption of approximately 890nm. A large concentration of defects even in the purest available GaAs results in deep energy states within the bandgap that contribute electrons and holes to the conduction process. GaAs can therefore be switched with a 1.06μm light source using extrinsic generation of carriers. The absorption depth at this wavelength is ~

1 cm [7]. In GaAs, resistivity values on the order of 10^7-10^8 Ω-cm can be obtained. GaAs, being a direct bandgap material, has carrier lifetimes in Pico to few nanoseconds. GaAs switches can be used in applications where nanosecond closure times are required. However, an interesting feature of GaAs is the lock-on effect at higher bias voltages leading to non-linear behaviour. In these cases, the switch remains closed for long periods of time (microseconds to milliseconds).Table 3.2 lists the properties of GaAs [9].

Properties	GaAs
Band Gap	1.43 eV
Critical breakdown field strength	$4x10^5$ V/cm
Electron mobility	8500 cm^2/V-s
Hole mobility	400 cm^2/V-s
Saturation velocity	$1x10^7$ cm/s
Thermal conductivity	0.46 watt/cm°C
Intrinsic carrier concentration	$1.1x10^7$ cm^{-3}
Work function	4.7 eV
Dielectric constant	10.9

Table 3.2. Properties of GaAs at 300 K

3.1.3 SiC

SiC has a structure that depends on the formation of Si and Carbon layers and has more than 170 polytypes [10]. The polytypes are named based on the crystal structure (Cubic or hexagonal). For example 3C-SiC is cubic, 2H SiC is hexagonal, and all others are mixtures of cubic and hexagonal layers. Fig. 3.1 shows two of these polytypes, 3C

and 4H (one hexagonal layer one cubic layer). Also, 6H SiC has one hexagonal layer and two cubic layers. Depending on the polytype crystal structure, the band gap varies from 2.2 to 3.3 eV. Drift velocity is $2x10^7$ cm/s [9]. The breakdown electric field varies from 2500 to 5000 kV/cm. Thermal conductivity is 4.9 W/cm°K.

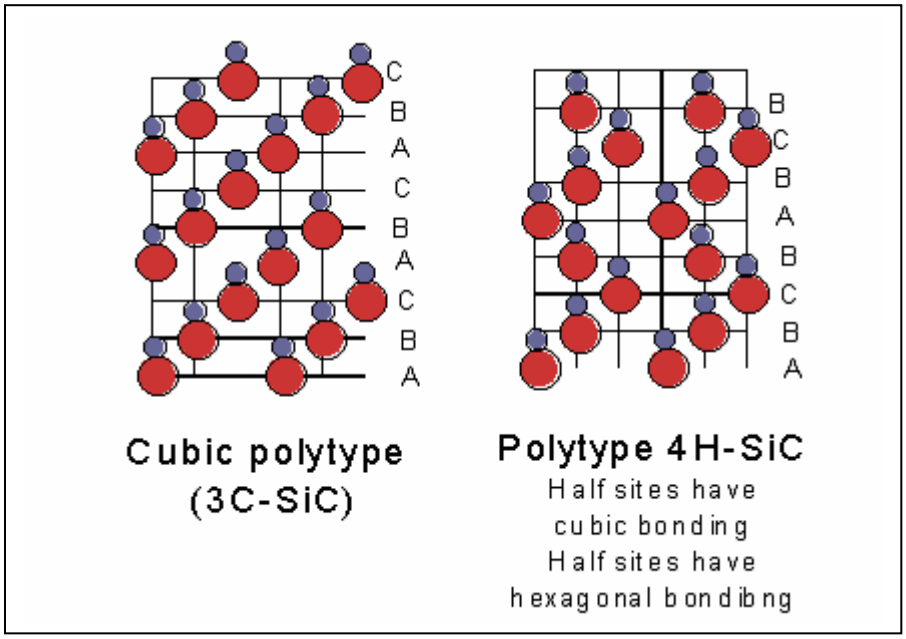


Figure 3.1. Different polytypes lattice arrangement [10]

SiC classification also includes a basal type (C plane) and "a" plane (Fig. 3.2) depending on the crystal growth and machining. Evidently, C plane SiC indicates a large micropipes density, causing the breakdown of the devices much earlier than expected. A micropipe is a defect in SiC (Fig. 3.3). The micropipe density in A plane is parallel to the surface hence preferred for UMC vertical switch geometry (breakdown would not be affected by micropipes). Recently SiC manufacturing companies have claimed C plane material with zero micropipes.

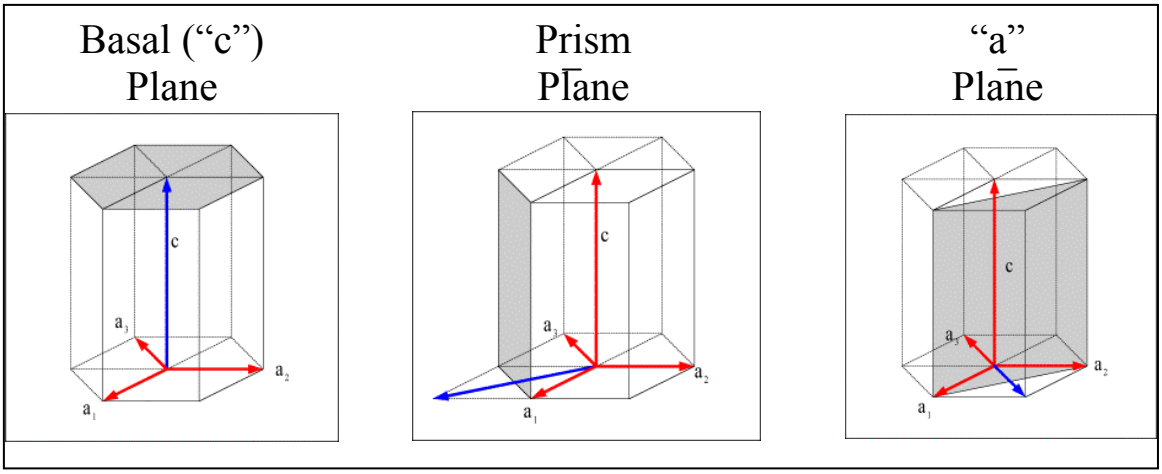


Figure 3.2. Crystal planes in SiC

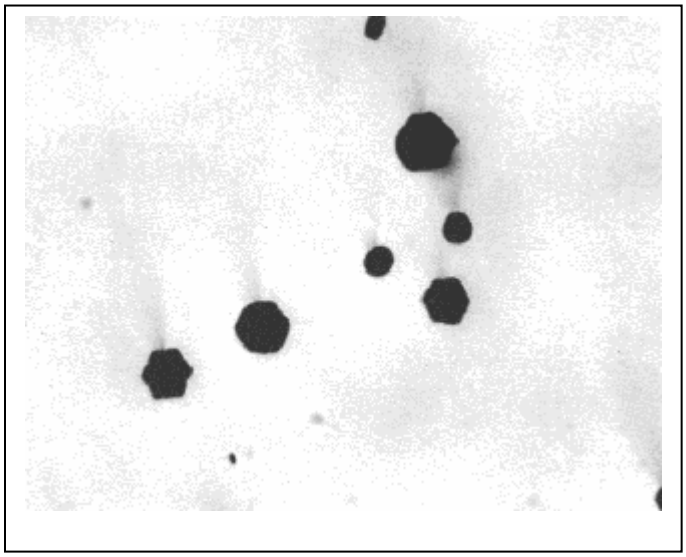


Figure 3.3. Micropipes in SiC

In this analysis we have considered 6H type SiC has been considered in detail for reasons that will be clear in the next chapter. Now, 6H SiC has a bandgap of approximately 3.02eV, which corresponds to an optical absorption of approximately 410nm. In this case, also one will obtain a large concentration of deep levels, resulting in deep energy states within the bandgap that contribute electrons and holes to the conduction process; 6H SiC can therefore be switched with a 1.06 μm and or a 532 nm light source using extrinsic

generation of carriers. The location of the trap levels responsible for this is a part of this research. The optical absorption depth will also be discussed in detail, it ranges over few cm [10]. In 6H SiC, resistivity values on the order of 10^{11}-10^{12} Ω-cm can be obtained. SiC, being an indirect bandgap material, has longer carrier lifetimes; 200ns to few microseconds; are expected. Table 3.3 gives all the basic properties of two types of SiC studied in this research [11].

Properties	4H SiC	6H SiC
Band Gap	3.2 eV	3.02 eV
Critical breakdown field strength	$3x10^6$ V/cm	$3x10^6$ V/cm
Electron mobility	800 cm^2/V-s	200-300 cm^2/V-s
Hole mobility	60 cm^2/V-s	50 cm^2/V-s
Saturation velocity	$2x10^7$ cm/s	$2x10^7$ cm/s
Thermal conductivity	5 watt/cm°C	5 watt/cm°C
Intrinsic carrier concentration	~$1x10^{-8}$ cm^{-3}	~$1x10^{-6}$ cm^{-3}
Dielectric constant	9.6	9.6

Table 3.3. Properties of SiC at 300 K

3.2. Compensation Mechanisms in SI GaAs

The optically activated switches discussed here are bulk semiconductor devices which consist of Semi-Insulating (SI) GaAs. The primary material used in photo-switches is Liquid-encapsulated Czochralski (LEC) grown GaAs, in which deep donors are compensated by shallow acceptors (DDSA). In the DDSA compensation scheme, illustrated in Fig. 3.4 [12], a balance is obtained between the deep lying EL2 and shallow

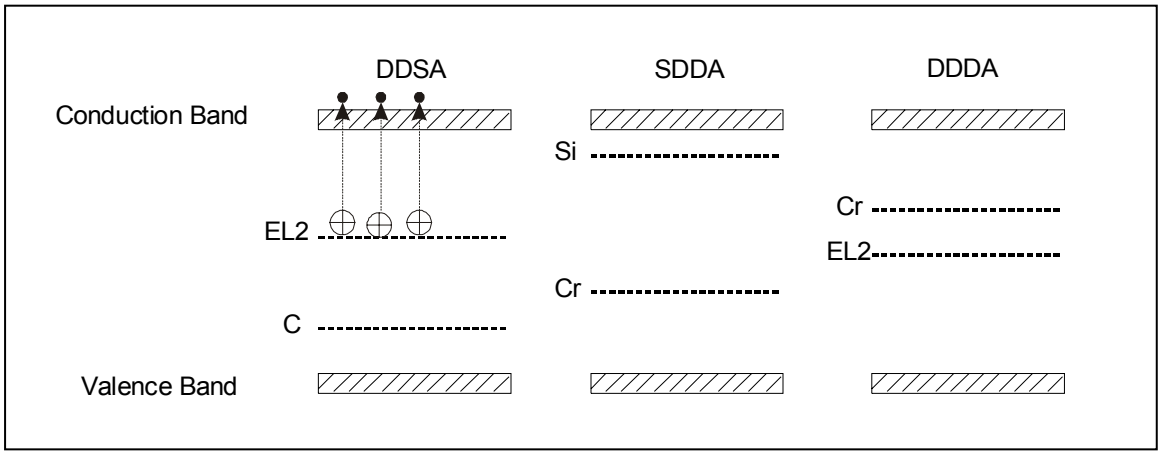


Figure 3.4. Compensation structures in Semi insulating GaAs

acceptor impurities, generally Carbon. The bulk resistivity is on the order of $10^7 - 10^8\ \Omega - cm$. There are two more types of compensation mechanisms Shallow Donor and Deep Acceptor (SDDA), in which a balance is obtained between Chromium (Cr) deep level acceptors and Silicon shallow donors. This type of material is grown by the horizontal Bridgman (HB) technique. A third type is Deep Donor Deep Acceptor (DDDA) in which EL2 is compensated by Cr deep acceptors. More information can be found in references [13]-[15].

3.3. Previous Photo Switch Work

3.3.1. Linear Si and GaAs PCSS

The example of an optically controlled semiconductor switch was explained previously in Section 1 in Chapter 2. In this section the performance of a GaAs and a Si linear PCSS will be compared.

As mentioned previously, the length of the switch is determined by the dielectric strength of the semiconductor material surface and is given by,

$$h_s = \frac{V_o}{E_m} \tag{3.1}$$

where V_o is the maximum voltage applied to the switch and E_m is the operating surface electric field. Experimentally obtained values of E_m for Si and GaAs are 90 kV/cm and 140 kV/cm [16] respectively. Therefore, a 1cm switch should be capable of operating at 50-60KV for Si and ~100KV for GaAs. These are ideal values, but most of the time the switches break down earlier due to the non uniform electric fields at the contacts, surface defects, and the like.

The semiconductor-wavelength pair determines the optical absorption depth

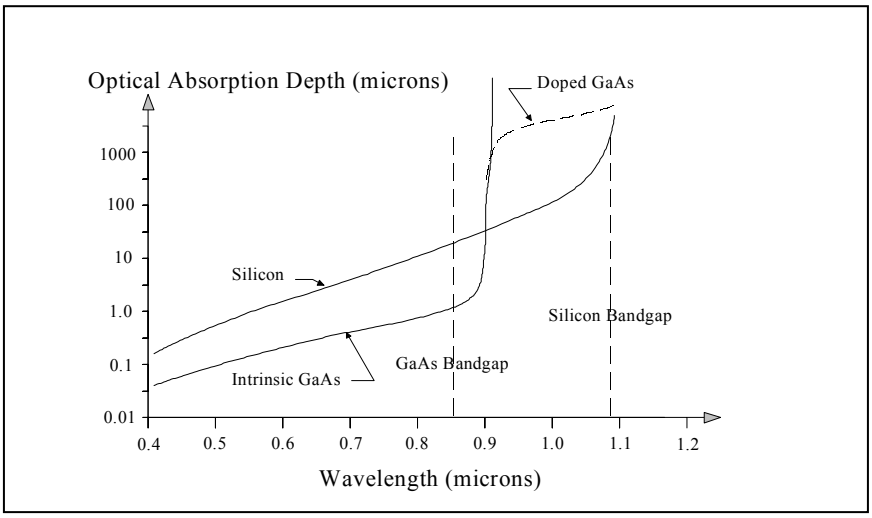


Figure 3.5. Optical absorption depth d_o versus wavelength λ

and is graphed versus wavelength in Fig. 3.5 [7]. For silicon, the wavelength must be less than 1.09 μm, corresponding to a bandgap energy of 1.142ev and for GaAs, the wavelength must be less than 0.89 μm, corresponding to a bandgap energy of 1.39ev; see Fig. 3.5. These are the limits for extrinsic and intrinsic conductivities for Si and GaAs respectively. From Fig. 3.5, note that the optical absorption depth for intrinsic GaAs near

the band edge is less than $10\,\mu m$. Above the band edge for GaAs, intrinsic GaAs becomes transparent with an optical absorption depth of up to several centimeters, while an optical absorption depth of extrinsic GaAs, i.e. the absorption depth of GaAs with donor impurity concentration, can be several millimeters. For optimum use of the optical energy, the switch depth d_0 should be 4-5 times the optical absorption depth.

Generally, the switch resistance is chosen to be 5-10% of the total circuit resistance because the optical energy required is reduced by a factor of 5 to 10. Work at Los Alamos Laboratory determined that the maximum practical carrier density in Si is approximately $5\times10^{17}\,cm^{-3}$, being limited by practical considerations of thermal runaway, Auger absorption, and free carrier absorption [17]. The carrier density limit and drift velocity for conduction fields on the order of 4 kV/cm correspond to a maximum current density on the order of 50 kA/cm^2 in Si. If the maximum carrier density for GaAs is similar to that for Si while the drift velocity is much larger, the maximum current density will be on the order of $500\,kA/cm^2$. Using the optical absorption depth d_o for a semiconductor wavelength pair, the practical current density per unit width of the switch face can be determined from

$$I_w = J_{\max} \bullet d_o \text{ [A/m]} \tag{3.2}$$

For Si this quantity is about 5kA/cm and for GaAs, it is about 0.5kA/cm. Note that these values are obtained based on the intrinsic optical absorption depths for Si and GaAs. If one uses the extrinsic absorption depth for GaAs, this number will change. The carrier density in that case is dependent on the extrinsic doping level and is approximately $1x10^{16}$ /cm^3.

The recombination times for Si, an indirect bandgap material, can range from 100 nano seconds to a few milliseconds depending upon the dopants present. At the other extreme, the recombination times of GaAs, a direct band gap material can range from a few nanoseconds in intrinsic GaAs to several tens of picoseconds in a heavily doped material. The recombination time is very important in a PCSS because the carriers lost to recombination must be replaced by optical input or the electrical pulse through the switch must be limited to a fraction of the characteristic semiconductor recombination time. The faster recombination time is an advantage it is desired to open the switch. In most power applications, the switch material is chosen to provide a recombination time that is much longer than the electrical pulse through the switch.

In all bulk semiconductor switches, the voltage applied is limited by the surface dielectric strength and thermal runaway. The surface dielectric strength can be accounted for by careful surface preparation. In this case, the applied voltage is limited by the bulk operating strength of the switch material. However, the thermal runaway limit is dependent on the amount of thermal energy deposited in the switch while the voltage is applied. The integral of the power deposited in the switch during charge must be less than a characteristic value that is dependent on the bulk resistivity of the material. Semi insulating GaAs with a bulk resistivity of ~10^7 Ω-cm, can sustain a given voltage for a much longer period of time than Si with bulk a resistivity of ~10^4 Ω-cm.

The energy dissipated in a bulk semiconductor switch during pulse charge is given by

$$E_d = \int_o^{T_c} \frac{V_s^2(t)}{R_0} dt < E_c \tag{3.3}$$

where $V_s(t)$ is the switch charge voltage as a function of time and R_0 is the bulk resistance of the switch. Experimental work at Los Alamos Laboratory [17] shows that, as the operational voltage increases, the charge time decreases.

Linear		
Parameter	Si	GaAs
Switch voltage (kV)	123	155
Max. Current (kA)	3	7
Peak power (MW)	65	120
Rise time (ps)	200	430
Electric field (kV/cm)	82	100
Device Lifetime (# pulses)	$1x10^7$	$4x10^6$

Table 3.4. Comparison of Linear GaAs and Si switch characteristics [18]

3.3.2. Inhibited carrier injection with the help of n^+ layer at cathode in DDSA GaAs

GaAs with n^+ layer at cathode

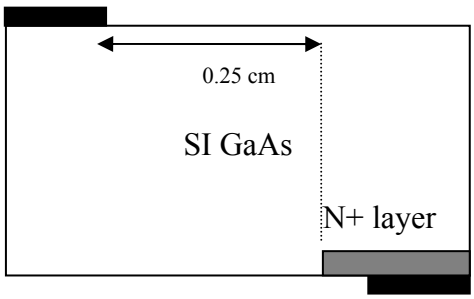


Fig 3.6. SI GaAs (DDSA) with n^+ layer at cathode trap density = $3.006x10^{15}/cm^3$, carbon concentration = $3x10^{15}/cm^3$ [19]

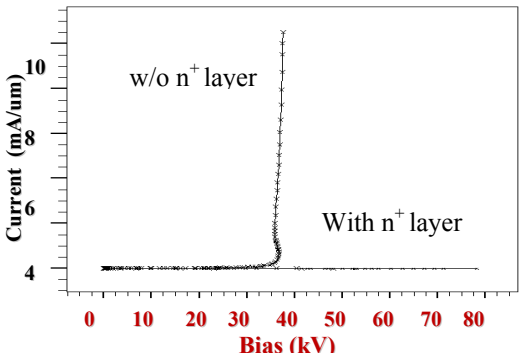


Fig 3.7. IV characteristics of NM switch with and without an n^+ layer [19]

The geometry of the New Mexico PCSS is as shown in Fig. 3.6. One reason for the premature breakdown is attributed to changes in the material characteristics during device operation. This is true for the DDSA type material, where filling the traps prior to the breakdown at 34kV (Fig. 3.7) and the subsequent inhomogeneous nature of the device affect switching beyond a certain voltage [19]. Trap filled regions are formed near the cathode initially, spreading to the anode later, and ultimately interfering with the conduction mechanism.

A method to achieve higher hold-off voltages

One way of improving the device hold-off characteristics is to shift the formation of the trap filled regions to higher voltages. This is possible through mechanisms that would suppress electron injection until a higher voltage bias (>34kV) is reached. Simulations of the structure with an n^+ region next to the cathode showed marked improvements in the operating voltage of an opposed contact DDSA type switch. The reason for such a response is attributed to the interaction between an SI layer and the n^+ region adjacent to it. As detailed in [20]-[22], the introduction of a 20 μm x 200 μm, $1\times10^{18}/cm^3$ doped n^+ region has two important effects: 1) it shifts the high E field region from the contact to a region near the n^+ diffused layer and 2) it lowers the high E field near the contact. The nature of the n^+-SI contact also results in inhibiting electron injection until a higher voltage bias is reached.

3.4. Fermi level calculations for GaAs

The electrostatic properties of a material depend on the location of the Fermi level in the material. Further analysis of solving the carrier continuity equation and Poisson's equation depends on the correct calculations of the Fermi level. Hence we present the Fermi level calculations for a Semi Insulating material here [21].

3.4.1. Fermi level calculations for a DDSA type material

Consider the case of a DDSA type GaAs material, where a balance is obtained between a deep lying donor level N_{dd} (EL2) and a shallow acceptor level N_{sa} (Carbon). In a bulk semiconductor, space charge neutrality requires that

$$P - N + N_D - N_A = 0 \tag{3.4}$$

Hence, in this case one can write

N_{sa} = Ionized N_{dd}, or

$$\frac{N_{dd}}{1 + g_{dd} \exp[(E_F - E_{dd})/k_B T]} = N_{sa} \tag{3.5}$$

Solving for E_F, one obtains

$$E_F = E_{F,si} = E_{dd} - k_B T \ln g_{dd} + k_B T \ln(\frac{N_{dd}}{N_{sa}} - 1) \tag{3.6}$$

where N_{dd} = Density of the deep donor level /cm^3, N_{sa} = Density of the shallow acceptor level /cm^3, N_{da} = Density of the deep acceptor level /cm^3, N_{sd} = Density of the shallow donor level /cm^3, g_{dd} = Occupancy of the deep donor level, g_{da} = Occupancy of the deep acceptor level, E_F = Fermi energy level eV, E_{dd} = Deep donor energy level eV, E_{da} = Deep acceptor energy level eV, k_B = Boltzmann's constant, and T = Temperature in K

3.4.2 Fermi level calculations for SDDA type material

For a SDDA type material one can write an equation similar to Eqn 3.6 above, replacing deep donor by deep acceptor (Cr) and shallow acceptor by shallow donor (Si).

The equations in this case are as follows.

N_{sd} = Ionized N_{da}

$$\frac{N_{da}}{1+(1/g_{da})\exp[(E_{da}-E_F)/k_BT]} = N_{sd} \tag{3.7}$$

This gives

$$E_{F,si} = E_{da} - k_BT\ln g_{da} - k_BT\ln(\frac{N_{da}}{N_{sd}} - 1) \tag{3.8}$$

The location of the Fermi level is dependent on the compensation ratio $m=N_{da}/N_{sd}$. This is an interesting feature of the semi insulating materials. The effect m on the photocurrent response, recombination and slope of the IV characteristics is discussed in later chapters.

3.5 Limitations of the current state of the art

Semi-insulating GaAs has been employed as a photo-switch material over Si due to its availability, high electron mobility, and large dark resistivity. The potentially large mobility reduces the optical energy requirements necessary to produce a given conduction resistance. In addition, the large dark resistivity is essential to minimize resistive dissipation during voltage application. More importantly, GaAs materials can be triggered into conduction through the optical seeding of avalanche processes that reduce the optical closure energy by three to four orders of magnitude. However, the related filamentary conduction has been shown to damage bulk photo-conductive material, and high current densities at the contact limit the power handling capability of these

avalanche photo-switches. The filamentary current limits are 20A/filament for 10ns pulses. Chapter 4 will provide a comparison of GaAs material to SiC, where a theoretical comparison of the physical parameters is performed.

Chapter 4

Rationale for SiC investigation

Both Si and GaAs have been used as PCSS material for high power applications. Because of its superior electrical characteristics, GaAs is preferred over Si in most pulse power generation circuitry. However, when operated at a high repetition rate at a sustained high power level, GaAs switches are limited by poor thermal conductivity and are susceptible to failure either through premature breakdown or burnout. When photo-conductive switches are operated in the non-linear mode, filamentary conduction and charge trapping result in contact and bulk material damage. Linear mode operation, in which the current is distributed over a large cross section, is an alternate approach to switch design for high power operation. In any high power system, the PCSS material must meet the rigorous requirements of high fields, large current densities, and high thermal conductivity. Hence, this chapter focuses on the advantages of SiC over previously used PCSS materials. The compensation mechanisms are discussed next, followed by the UMC switch geometry. The mathematical modeling of the switch is explained in the, last section.

4.1 Rationale for Investigation of SiC

A new candidate for an active photo conductive material in a high field photo switch is semi insulating (SI) SiC. The two types, SDDA and DDSA semi insulating SiC

are compensated in much the same manner as SI GaAs. The interband gap states determine the optical absorption depth for photons with energy less than the bandgap. Table 4.1 compares the properties of SiC with GaAs. The properties of SiC that make it a viable material for a high power PCSS are explained in the next few paragraphs.

Table 4.1 [23] compares different parameters of 6H SiC with GaAs. Note that the

Parameter	**GaAs**	**6H-SiC**	**Unit**
Band Type	Direct	Indirect	
Band Gap	1.43	3.02	eV
Electron Mobility @ 3 kV/cm	6000	40	cm^2/V-s
Electron Mobility @ 10 kV/cm	1500	200	cm^2/V-s
Max E-Field	250	3000	kV/cm
Dark Resistivity	10^7	10^9-10^{11}	Ohm-cm
Max Drift Velocity	$2x10^7$	10^7	cm/s
Recombination time	0.5	200-800	ns
Thermal Conductivity	0.55	4.9	W/cm-K

Table 4.1. Comparison of material properties of GaAs and SiC

maximum electric field that can be supported in SiC is 12 times higher than GaAs. Also, note that the mobility of GaAs at conduction electric field strength of 3 kV/cm is 20 times greater than for SiC at conduction electric field strength of 10 kV/cm. These parameters affect the conduction voltage drop and the power dissipated in the switch as well as the optical closure energy requirements.

Consider a comparison between a GaAs switch and a SiC switch. Assume that the operating electric field for SiC is only 6 times greater than that for GaAs. This assumption is appropriate since the thickness of the SiC will be 1/6 of that for GaAs, so that during conduction, the SiC switch will have a similar conduction voltage, but a larger conduction electric field strength. In addition, the conduction mobility of GaAs is 6 times that of SiC. Therefore, the conduction resistances of a SiC switch and a GaAs switch are as follows

$$R_{C-GA} = \frac{E_\lambda \cdot {h_{s-GA}}^2}{\mu_{e-GA} \cdot q_e \cdot E_{o-GA}} \tag{4.1}$$

and

$$R_{C-SC} = \frac{E_\lambda \cdot {h_{s-SC}}^2}{\mu_{e-SC} \cdot q_e \cdot E_{o-SC}} \tag{4.2}$$

so that the ratio of optical control energies that result in the same conduction resistance using the same photon energy is given by

$$\frac{{h_{s-GA}}^2}{\mu_{e-GA} \cdot E_{o-GA}} = \frac{{h_{s-SC}}^2}{\mu_{e-SC} \cdot E_{o-SC}} \tag{4.3}$$

$$\begin{aligned} \frac{E_{o-SC}}{E_{o-GA}} &= \left(\frac{h_{s-SC}}{h_{s-GA}}\right)^2 \cdot \left(\frac{\mu_{e-GA}}{\mu_{e-SC}}\right) \\ &= \left(\frac{E_{B-GA}}{E_{B-SC}}\right)^2 \cdot \left(\frac{\mu_{e-GA}}{\mu_{e-SC}}\right) \approx 0.16 \end{aligned} \tag{4.4}$$

This result indicates that only 16% of the optical energy is necessary to produce the same conduction resistance as in the GaAs switch. Conversely, the same optical energy will produce a conduction resistance that is 16% of that in the GaAs switch. The mobility estimates probably make these conclusions conservative.

In addition, the dark resistivity of GaAs is approximately 4 orders of magnitude lower than that for semi-insulating SiC and thus the "off" state power dissipation of a SiC switch is reduced by the same factor.

The design and comparison of a GaAs photo-switch and a SiC photo-switch, illustrated in TABLE 4.2 [23], point out the advantages of employing SiC. The designs in TABLE 4.2 assume a quantum absorption efficiency of unity, a lossless optical transfer of optical energy into the conduction region, and a switch conduction area of 1 cm x 1 cm. The depth of the conduction region is determined by the optical absorption depth that is assumed to be 1 cm.

The first order comparison in TABLE 4.2 indicates that a 1 square cm conduction area can conduct ~ 2.5 kA with a conduction drop of 200-300 Volts while blocking 10 kV. These parameters indicate a voltage switching efficiency of 97.5 percent, assuming the source and load impedances are appropriately matched.

Note from the previous comparable designs that, the current density in SiC can be similar to that in GaAs, even though the mobility of SiC is only $1/20^{th}$ that for GaAs. Furthermore, the conduction voltage drop in a SiC switch is essentially the same as in a GaAs switch when the SiC is operated at a larger conduction electric field. Thus, the advantages of the SiC switch are made possible by operating the SiC material at a high blocking electric field, which justifies the focus on the development of high electric field packaging. In addition, the order of magnitude larger thermal conductivity of SiC as compared to GaAs enables higher average power operation with SiC.

Parameter	GaAs	6H-SiC	6H-SiC
Blocking Voltage V	1.00E+04	1.00E+04	2.00E+04
Blocking Electric Field Max V/cm	1.00E+05	5.00E+05	5.00E+05
Bulk material thickness mm	1.00	0.20	0.20
cm	0.1	0.02	0.02
Conduction Electric field V/cm	3.00E+03	1.00E+04	1.00E+04
Conduction electron mobility $cm^2/V\text{-}s$	6.00E+03	1.00E+02	1.00E+02
Photo Carrier Density cm^{-3}	1.00E+15	5.00E+15	5.00E+15
Conduction Current Density A/cm^2	2880.00	1600.00	1600.00
Conduction Voltage	300.00	200.00	200.00
Conduction Impedance V	0.104	0.125	0.125
Wavelength m	1.06E-06	5.32E-07	1.06E-06
Photon Energy J	1.87E-19	3.74E-19	1.87E-19
Optical Closure Energy J/cm^3	1.87E-04	1.87E-03	9.35E-04
Prototype 1 square cm switch			
Switch height cm	1.00E-01	2.00E-02	2.00E-02
Switch width cm	1	1	1
Optical Absorption Depth cm	1	1	1
Conductivity mho/cm	9.60E-01	1.60E-01	1.60E-01
Conduction Resistance Ohm	1.04E-01	1.25E-02	1.25E-02

Table 4.2. Comparison of switch parameters for GaAs and SiC

4.2. Compensation Mechanisms in 6H SiC

The objective was to evaluate the performance of 6H SiC; all the results from this point will be discussed with respect to 6H-SiC semi-insulating materials that are grown through the compensation process. Compensation results when the ionized donor and acceptor densities effectively cancel each other such that the net density of free carriers in the semiconductor is very small. Vanadium is responsible for two different trap levels in

6H SiC and hence was considered further. The two types of compensation structures investigated are: (1) deep trap donor levels compensated by shallow level dopants, termed the DDSA structure and (2) shallow donor dopants compensated by deep acceptor levels, termed the SDDA structure. At room temperature, the shallow dopant level is completely ionized, and the deep traps are partially ionized, which makes the material semi-insulating. In 6H SiC the two deep trap levels, both acceptors and donors, are formed by Vanadium. The V^{3+}/V^{4+} acceptor trap level is present at 0.74 eV or 0.68 eV from the conduction band [24], and a deep donor trap level (V^{4+}/V^{5+}) is present at 1.6eV (Fig. 4.1), close to the middle of the band gap [25]. Deep levels other than Vanadium [26], because of their low concentration, are usually not used in an analysis. The shallow dopant that is compensated is Nitrogen or Boron. Nitrogen is absorbed at porous graphite parts and Boron is inherently present in crucible material [27-28]. Thus, the material is classified as shallow donor-deep acceptor (SDDA, V^{3+}/V^{4+} compensated with Nitrogen) or deep donor shallow acceptor (DDSA, V^{4+}/V^{5+} compensated with Boron) type.

Nitrogen in the SDDA type 6H-SiC is located at energy levels $E_C - 0.081$, $E_C - 0.138$ and $E_C - 0.142$eV from the conduction band and is completely ionized at room temperature [11]. The acceptor level is a hole trap. It is neutral when empty and negatively charged when filled. Thus, an acceptor-like trap is negatively charged and may emit an electron. This explains the location of the acceptor like trap closer to the conduction band. In DDSA SiC, Vanadium is compensated by Boron at an energy level $E_V + 0.3$ from the valence band [25]. The donor level is an electron trap. It is positive when empty and neutral when filled. Note that the location of the vanadium acceptor

level in the upper half of the bandgap is unusual and hence discussed in detail in the next section.

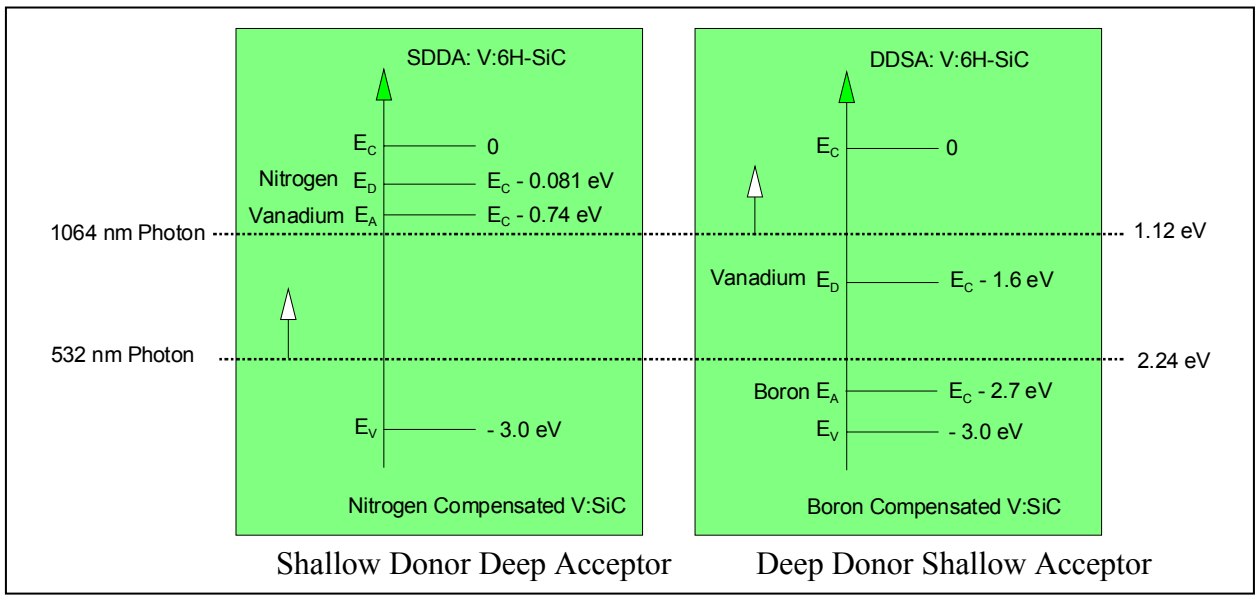


Figure 4.1. Vanadium Compensation Structures in Silicon Carbide

The cross sections for the deep donor level are not published yet because of its location deep in the band gap [24]. The resistivity values obtained for the SDDA material are ~10^{11} Ω-cm and for the DDSA material are ~10^{15} Ω-cm [10]. The DDSA material has a higher resistivity because of its deep location in the bandgap. No data has been published on the lifetimes of these trap levels to date.

4.2.1. Explanation of location of vanadium deep acceptor in the upper half of the bandgap

The position of the levels in the band gap has nothing to do with the classification as acceptor or donor. Isolated atoms develop a term scheme (atomic configuration), which is governed by ionization energies. If such an atom is brought into a crystal, the term scheme can be modified quite heavily due to electronic and spin interactions (that's just what solid state physics is all about). Consider rare-earth atoms in semiconductors,

which keep their term scheme quite independently of the host (i.e. lattice, crystal material). The position of the term scheme in relation to the band gap of the host is fixed by the electron affinity (or, work function). So, vanadium has three charge states with its two transitions lying in the band gap (is has even more, but the V^{3+}/V^{2+}, for example, lies somewhere else, i.e. within a band of SiC. That's quite common. Vanadium has something like a "negative-U" effect: The negative charged state lies at higher energies than the positive charged state. Most of the time, this condition is reversed. This condition occasionally led the acceptor level to be in the upper part of the band gap. It's an acceptor level, because it traps electrons and not holes, regardless where it resides in the band gap. Vanadium-doped SiC (more vanadium than nitrogen, with no other impurities around) has n-type conductivity. This is coming from the acceptor level emitting electrons in the conduction band. This is clear if one notes that the position of the acceptor level - it's in the upper half of the bandgap." An acceptor trap is neutral when empty and negatively charged when filled." This is the definition, and this is why one calls this level "acceptor".

Similar behavior is not observed in Si or GaAs due to the small band gap. A level lying close to the valence band will act as an acceptor. If the site is a donor, it would be completely neutral or inactive because there is no vacancy for the electron. In SiC, the band gap is so large, that deep acceptors and donors can reside in a broad range within the band gap and are active trapping centers and, because the shallow donors/acceptors are even closer to the band edges, the phenomena stated above may not occur [29].

4.3. UMC Switch Design Method and Geometry

The UMC switch geometry is shown in Fig. 4.2a. The length and the width of the device are 1.2 cm x 1.2 cm and is approximately 350-400 μm in depth. The radius of contact curvature is 0.2cm. The contact leaves the 6H SiC slab around 0.4cm from the center of the switch. The nickel silicide contacts have a resistivity of about 1×10^{-5} Ω-cm [31]. The actual contacts are made up of NiSi2/Ti/Pt/Au/Cu layers with thicknesses 200/200/100/100/500 nm respectively. The SiC component of the PCSS in Fig 4.2b can be seen as the small rectangular disc in the middle of the contacts.

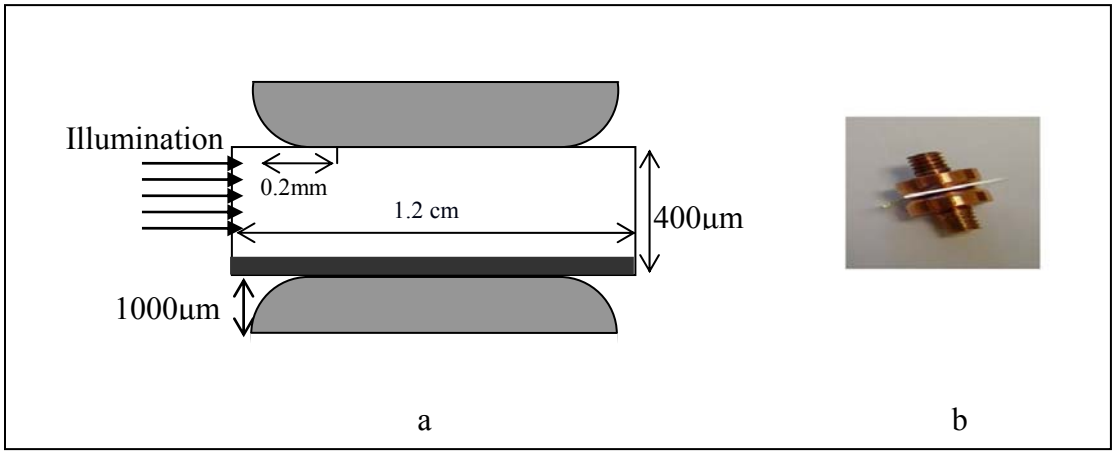


Fig 4.2. UMC switch geometry (a) and prototype switch (b)

4.3.1. Design modifications

Other work in photo conductive switches are presently limited by their performance due to the current density at the contacts which damage the contact depositions or damage the bulk material causing switch failure [31]. Other mechanisms such as surface flashover and field inhomogeneties at the contacts are among the main limitations to the longevity of the switch [32]. Hence the UMC approach was to improve the packaging of the PCSS so that the high electric fields at the surface and any other

inhomogeneties at the surface can be minimized and the current density would then be uniform across the switch electrode.

The switch geometry has been studied earlier in [33]. A homogeneous electric field inside the switch can be obtained with the help of curved contacts [33]. The void where the contact leaves the switch slab is filled with a high permittivity (high K) material (some sort of polymer). The high K material reduces the electric field intensity in the gaps, reducing the formation of fringing fields. Thus, the surface can be prevented from being damaged due to high field levels. A basic explanation of the operation of the high K material is as follows.

An electric field is said to be spatially continuous if it does not exhibit abrupt changes in either its magnitude or its position as a function of space. Even though the field is continuous in each of the two media individually, it might not be continuous at the boundary between the two, if a surface charge exists along the boundary. The tangential component of the electric field is continuous across the boundary between any two media with any permittivity values. The normal component of the electric flux density changes abruptly at a charged boundary between the two different media, and the magnitude of change is equal to the surface charge density. In the present case, the two media are the SiC slab and the high permittivity material around it. The charge at the surface can be considered as the dangling bonds at the SiC surface. The boundary condition requires that the sum of the product of the electric flux density and the permittivity in the two media must be equal to the surface charge density. To maintain the boundary condition as the permittivity is increased, the electric field must decrease in proportion. Thus, one can achieve lower electric fields at the surface by increasing the

permittivity value. Soon, saturation is reached since the surface charge is limited. Hence, after a permittivity value of 25 is reached the effectiveness of a high K material is limited (Fig. 4.3). Even though the simulations were performed with GaAs, the performance of the high K material is expected to be similar for SiC, or as a matter of fact, for all other semiconductors since the basic principle remains the same, and the result was indeed similar.

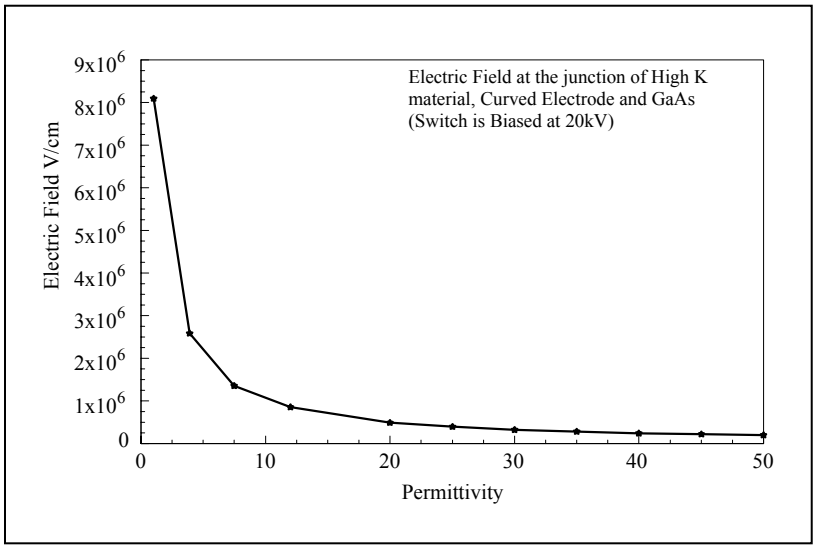


Figure 4.3. Change in electric field at the triple point with high K dielectric material

4.4. Switch Fabrication

The switches were fabricated at the Lawrence Livermore National Laboratories (LLNL). A square, A-plane SI 6H SiC slab (1.2cm x 1.2cm x 0.04cm) was used instead of the C-plane to avoid the micropipes problem [34]. Both of the surfaces were polished before the contact deposition. A 200 nm Nickel layer was first sputtered through the mask. Then, the contact was annealed for 2 minutes at 1273 ˚K. This formed a uniform NiSi layer. A 100 nm Titanium layer was then deposited over the NiSi layer, followed by a deposition of a 100 nm Platinum layer and a 500 nm Gold layer. Indium solder was

then used to connect the gold layer to copper electrodes. The radius of the Nickel Silicide contacts is 0.2cm (Fig. 4.2). A p^+ and or n^+ layer of thickness 10μm with a concentration of $1e^{18}/cm^3$ (Fig. 4.2) can be deposited at one or both the electrodes through ion implantation prior to the contact formation. This novel switch design was then used for the experiments. Before the experiments were conducted, mathematical modeling of the switch was carried out to predict the switch behavior along with the switch material characterization. This was required, since not enough information was available from the vendor about the switch material and dopant densities. The next section details the simulation software used along with the mathematical models used in this study of a PCSS.

4.5. Mathematical Modeling of the Switch and Device Construction

4.5.1. Software

The Atlas and Devedit modules of the Silvaco code ™, which provide two- and three-dimensional device simulations, were used in the present study. The Devedit, a device editor, was used to fabricate the switch. The Atlas part interfaced with Blaze, which incorporated group III-V materials, and was used to determine the characteristics of the switch.

Silvaco is a comprehensive software tool that can perform semiconductor device process and circuit simulations and includes numerous models and parameters that can be defined for any specific situation to obtain optimal results. The code, with a main interface (Atlas) and other interactive tools, provides for two-dimensional and three-dimensional semiconductor device simulations that also include thin film transistors

(TFT's), quantum devices, heterostructures, and power devices. The device to be simulated can be fabricated using the Athena or Devedit process module interfaced with Atlas, and the resulting mesh can be used for simulation. Furthermore, in a mixed mode environment, the device can be placed in a circuit, and the effects of any changes in the device parameters on the overall circuit can be studied. In addition to the drift-diffusion model, one can study such "non-local" effects as velocity overshoot, reduced energy-dependent impact ionization, and the like using the energy balance model, wherein such transport parameters as mobility and impact ionization become functions of the local carrier temperature rather than the local electric field. Finally, the code also has a provision to incorporate user defined functions through a C- interpreter. Further details about the software can be found in [35].

4.5.2. Simulation Mesh

The simulation mesh is shown in Figure 4.4. To eliminate the convergence

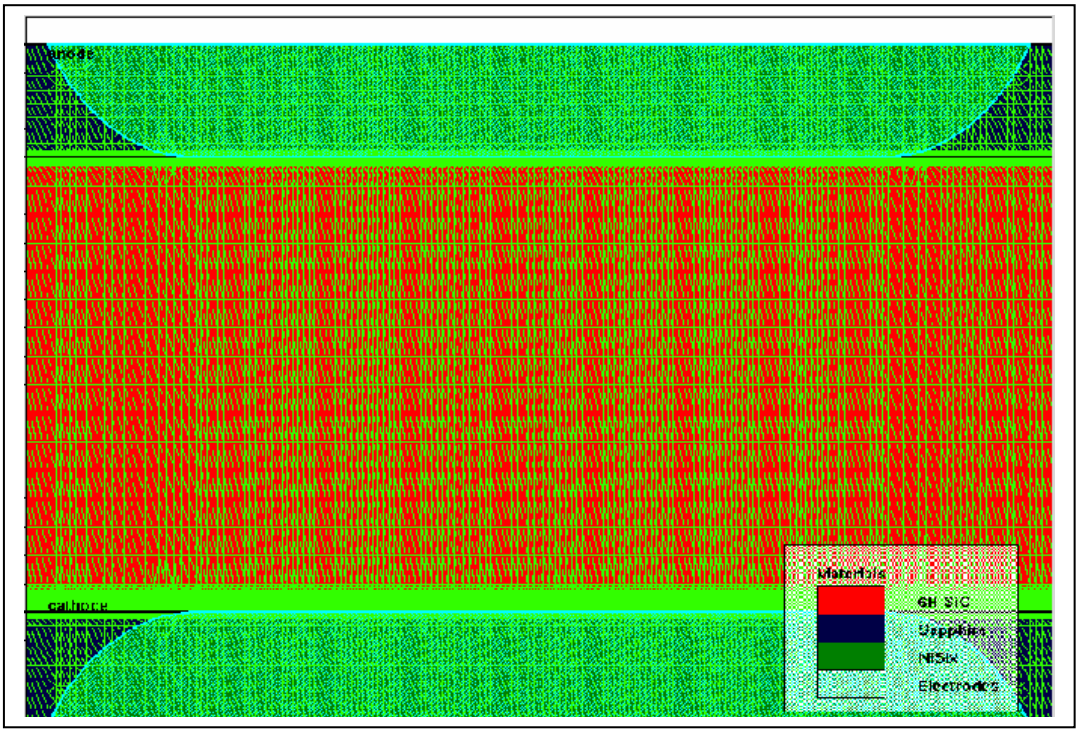


Figure 4.4. Mesh definition

Problem, the mesh was made finer near the surface and in the curved part of the contacts.

The mesh is a crucial parameter in obtaining the correct simulation results. There is a trade off between the accuracy and the numerical efficiency. Typical crucial areas were

1. High electric fields at the electrodes
2. Recombination effects near the electrodes
3. Areas of high impact ionization
4. Areas of trap filling

The three most important factors to look for were

1. Ensure high mesh density in the high field areas
2. Avoid obtuse triangles in the current path or high field areas
3. Avoid abrupt discontinuities in the mesh density

The basic mesh definitions were done in atlas or Devedit. Devedit has an inbuilt algorithm which can be used to get a better quality mesh definition. The simulation device consisted of 10,500 mesh points with a transient response simulation time of around 15 hours on a xenon two process system.

4.5.3. Mathematical modeling of the PCSS

High resistivity, compensated semiconductors with high trap densities have conduction characteristics that are similar to ‘lifetime’ materials as opposed to intrinsic ‘relaxation’ materials [36]. Simulations, therefore, involved the solution of the basic semiconductor continuity and Poisson’s equations shown below. The generation and

recombination terms, however, were defined through traps and dopant parameters that were inherent to the material.

$$\frac{\partial n}{\partial t} = \frac{1}{q} div J_n + G_n - R_n \tag{4.5}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} div J_p + G_p - R_p \tag{4.6}$$

$$J_n = qn\mu_n E_n + qD_n \nabla n \tag{4.7}$$

$$J_p = qp\mu_p E_p - qD_p \nabla p \tag{4.8}$$

$$\frac{dE}{dx} = \frac{q}{\varepsilon}(p - n + N_t^+) \tag{4.9}$$

Here, q is magnitude of the charge on an electron ($1.6\times10^{-19} C$) , n and p are the electron and hole concentrations respectively, J_n and J_p are the electron and hole current densities, G_n and G_p are the generation rates of electrons and holes respectively, R_n and R_p are the recombination rates for electrons and holes respectively, μ_p and μ_n are the hole and electron mobilities respectively and, D_n and D_p are the electron and hole diffusivities respectively. Models emphasizing physical parameters such as trap level, its density of state, energy states and their cross sections along with SRH and Auger recombination models, concentration and field dependent mobility models, and impact ionization were also considered and solved analytically. These parameters influence carrier lifetimes, pulse decay, diffusion and the Debye length. In fact, the trap concentration level and its effect on the Debye Length, has a major influence in making a high resistivity compensated material behave like a ‘lifetime’ semiconductor, as detailed in [36].

For compensated materials, additional equations and models are required to compute the densities of the trapped carriers that relate to the generation and recombination terms in Eqns (4.5) and (4.6) presented above. These models use electron and hole capture cross sections, the density of trap centers, degeneracy of the electron and hole trap centers, and the Fermi level position for computation. The models thus incorporate the physics associated with charge exchange, along with the conduction and valance bands, changes in space charge density and recombination statistics in the solution. The densities of trapped carriers at a trap center for respective carrier types are given by Eqns (4.10) and (4.11) [35].

$$n_t = \sum_{\alpha=1}^{k} n_t^{\alpha} \qquad (4.10) \qquad p_t = \sum_{\beta=1}^{m} p_t^{\beta} \qquad (4.11)$$

where k = number of acceptor like traps, m = number of donor-like traps, and n_t^{α}, p_t^{β} are defined as

$$n_t^{\alpha} = N_{ta}^{\alpha} \frac{K_n^{\alpha} + G_p^{\alpha}}{G_p^{\alpha} + G_n^{\alpha} + K_p^{\alpha} + K_n^{\alpha}} \qquad (4.12) \qquad p_t^{\beta} = N_{td}^{\beta} \frac{K_p^{\beta} + G_n^{\beta}}{G_p^{\beta} + G_n^{\beta} + K_p^{\beta} + K_n^{\beta}} \qquad (4.13)$$

$$K_p = p\sigma_p V_p \qquad (4.14) \qquad K_n = n\sigma_n V_n \qquad (4.15)$$

$$G_p = \frac{1}{\gamma}\sigma_p V_p n_i \exp\left(\frac{\varepsilon_i - \varepsilon t}{kT}\right) \qquad (4.16) \qquad G_n = \frac{1}{\gamma}\sigma_n V_n n_i \exp\left(-\frac{\varepsilon_i - \varepsilon t}{kT}\right) \qquad (4.17)$$

where, ε_i = intrinsic Fermi level position, γ = degeneracy factor of the trap level, V_n and V_p = thermal velocities, σ_n and σ_p = carrier capture cross sections, N_{ta} and N_{td} = Density of trap centers, and ε_t = Energy level of the discrete trap state. Subscripts n and p are used for electrons and holes respectively.

The trap occupancy factor was incorporated through Eqns (4.18)-(4.21)

$$F_n = \frac{v_n \sigma_n + e_p}{v_n(\sigma_n + \sigma_p) + (e_n + e_p)} \tag{4.18}$$

$$F_p = \frac{v_p \sigma_p + e_n}{v_n(\sigma_n + \sigma_p) + (e_n + e_p)} \tag{4.19}$$

$$e_n = g_0 . v_n . \sigma_n . n_i . \exp \frac{E.level - E_i}{kT_L} \tag{4.20}$$

$$e_p = \frac{1}{g_0} . v_p . \sigma_p . n_i . \exp \frac{E_i - E.Level}{kT_L} \tag{4.21}$$

where υ_n and υ_p are thermal velocities for electrons and holes respectively, σ_n and σ_p are capture cross sections, e_n and e_p are emission rates, n and p represent electron and hole densities respectively and n_i is the intrinsic carrier concentration. Also, E_i is the intrinsic Fermi level position, E.level is the energy level of each discrete trap level in the bandgap, g_0 is the degeneracy factor of the trap center, k is Boltzmann's constant and T_L is the lattice temperature. Also, the trap generation and recombination term was included by using the following equation [9].

$$R = \sum_{\alpha=1}^{k} R_n^{\alpha} + \sum_{\beta=1}^{m} R_p^{\beta} \tag{4.22}$$

where k is the number of donor like traps, m is the number of acceptor like traps and $R_{n,p}$ can be written as [35]

$$R_{n,p} = \frac{pn - n_i^2}{\tau_n [p + \frac{q}{g_0} n_i \exp \frac{E_i - E}{kT_L}] + \tau_p [n + g_0 . n_i \exp \frac{E - E_i}{kT_L}]} \tag{4.23}$$

Consequently, the electron and hole lifetimes are trap dependent as shown

$$\tau_{n,p} = \frac{1}{\sigma_{n,p} . v . N_T} \tag{4.24}$$

where N_T is the discrete trap density /cm^3.

To account for the effects of trapped charge, an additional charge term is assigned to the right hand side of Poisson's Eqn (4.9). This charge term is equal to the difference in the densities of the trapped carriers multiplied by the electronic charge. The recombination models defined by Eqns (4.5) and (4.6) also needed modification with a correction term that accounts for trapping and detrapping effects. The transient solution should account for trap density changes over time through the solution of additional trap rate equations.

Chapter 5

Preliminary PCSS Experiments (DC) and Analysis

In the simulation process, a reasonable match of the measured and simulated I-V characteristics ensures that the correct material has been used in the analysis. Measured material parameters are therefore very essential as simulation input. However, it is not always possible to obtain all the material parameters necessary. The reason is that some parameters vary from one batch to another and also between vendors (who usually do not volunteer information on trap levels, cross sections etc). Some of the material data used in the simulations was provided by the vendor, while the trap energy level and cross-sections were taken from [11]. No information on the compensation ratio (defined later) was available and its value was therefore adjusted to match the experimental IV. This chapter describes the process of obtaining the correct material properties along with a preliminary switch analysis.

5.1 Low voltage Experimental I-V Characteristics

The switch material used has to be correctly modeled so that a good match between the experimental characteristics and simulations can be obtained. This would help in understanding the behaviour of the switch at higher voltages as well as with illumination. Hence two different methods were researched for material characterization. The methods relied on obtaining the low voltage I-V characteristics and then matching

those to the simulation. First the Fermi level calculations were done followed by characterization. The trap type (donor or acceptor) and its density were not provided by the vendor, so a convenient method to calculate the exact trap concentration was needed.

5.1.1. Experimental I-V test setup

A variable DC power supply was used to bias the switch through a high value resistor to limit the current. A Pico ammeter (least count of a femto ampere) was used to measure current through the switch along with a voltmeter with an internal resistance of 100MΩ to measure the voltage drop across the switch.

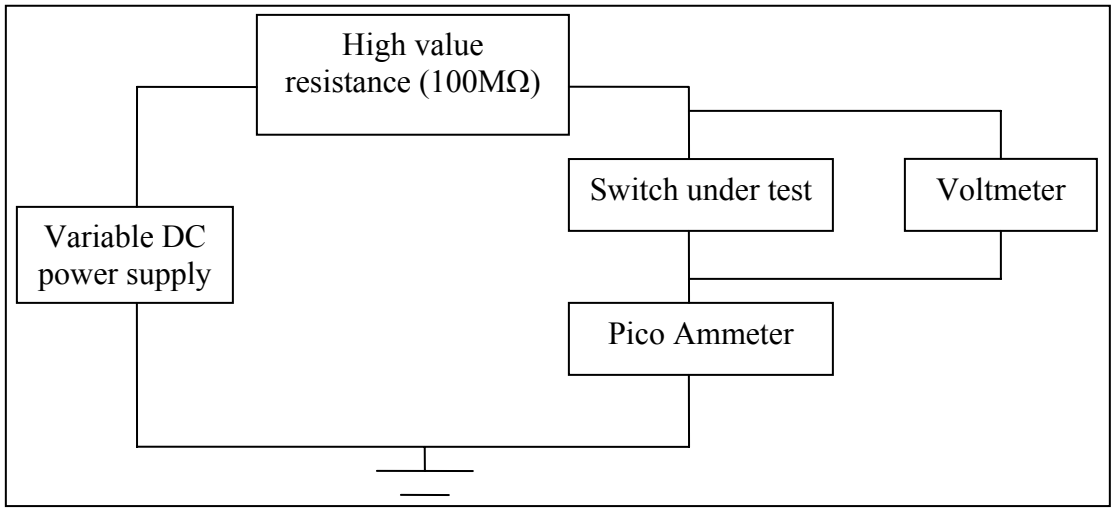


Figure 5.1 Experimental test setup for DC I-V characteristics

The voltage was increased from 0 to 2000V in steps of 10V and the current values were recorded. Since the voltage magnitudes were small, this particular set of I-V characteristics were indicated as low voltage and were analyzed and matched for correct material characterization. There were four different types of switches available for this study as shown in Fig. 5.2 (types A, B, C, and D). Hence, each type was tested and the current values were recorded. Type A was uncompensated, whereas types B, C, and D materials were compensated. Two different trends were observed in the I-V

measurements (Fig. 5.3). Type A was uncompensated and hence a higher value of current was observed as expected (initial resistance = 60MΩ). Types B also followed type A behaviour and hence it was concluded that it had to have a very small number of traps (initial resistance = 1MΩ). Types C and D did not show a significant current flow up to 2000V (less than 1 μA). Hence, types C and D materials were identified as compensated with high resistivities suitable for the PCSS's (initial resistance = 70MΩ each).

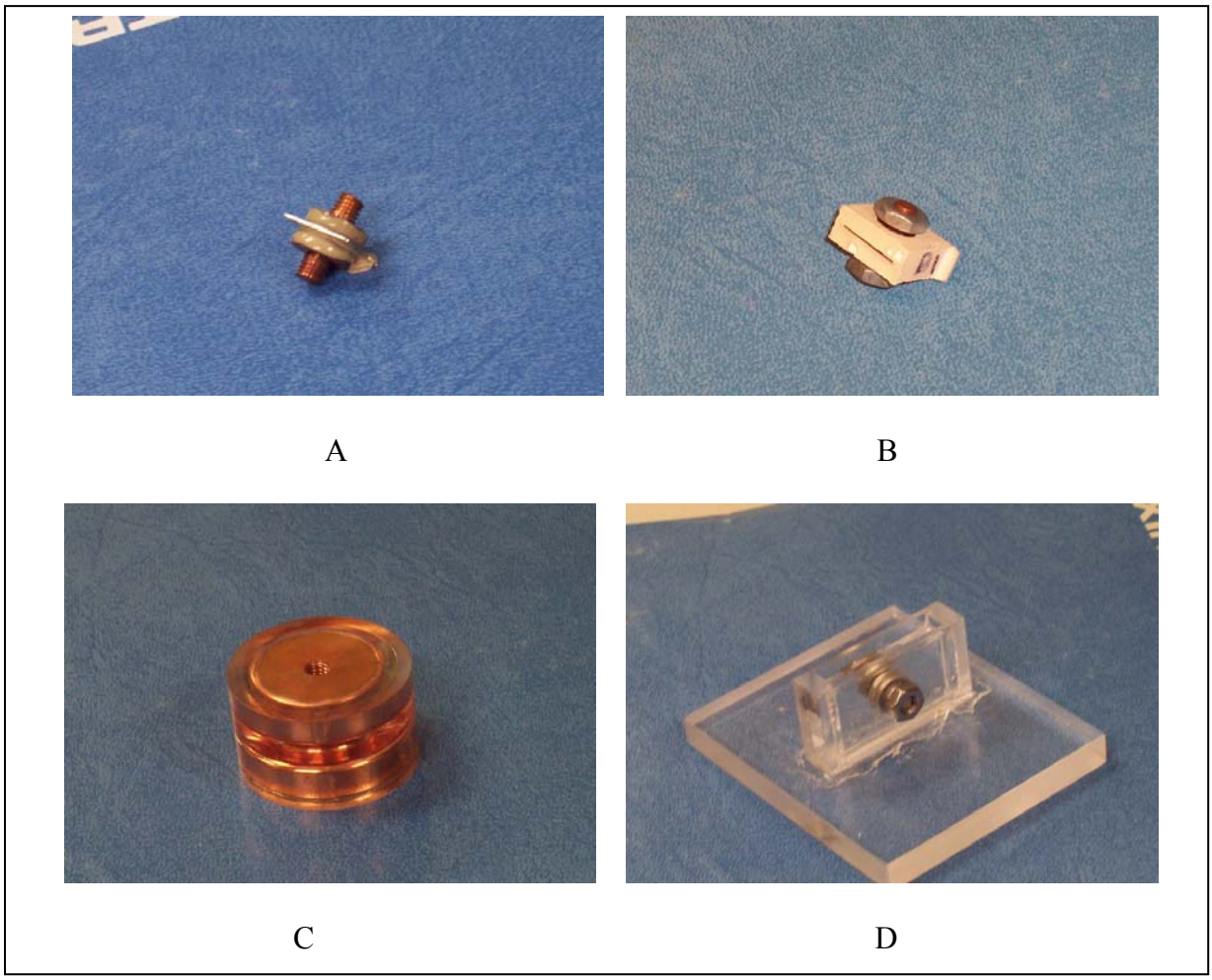


Figure 5.2. SiC switches available for testing A is intrinsic SiC with ceramic encapsulation, types B,C and D were compensated with ceramic, plastic and gel encapsulation respectively

As the I-V characteristics were obtained, simulations were carried out to match the simulated IV to the experimentally obtained characteristics. The vendor provided some information about the doping in the material [37]. Compensated switches had Vanadium along with an n-type impurity concentration in the 2-7x10^{15}/cm^3 range. Using this data as the initial guess for the simulations, two methods were studied.

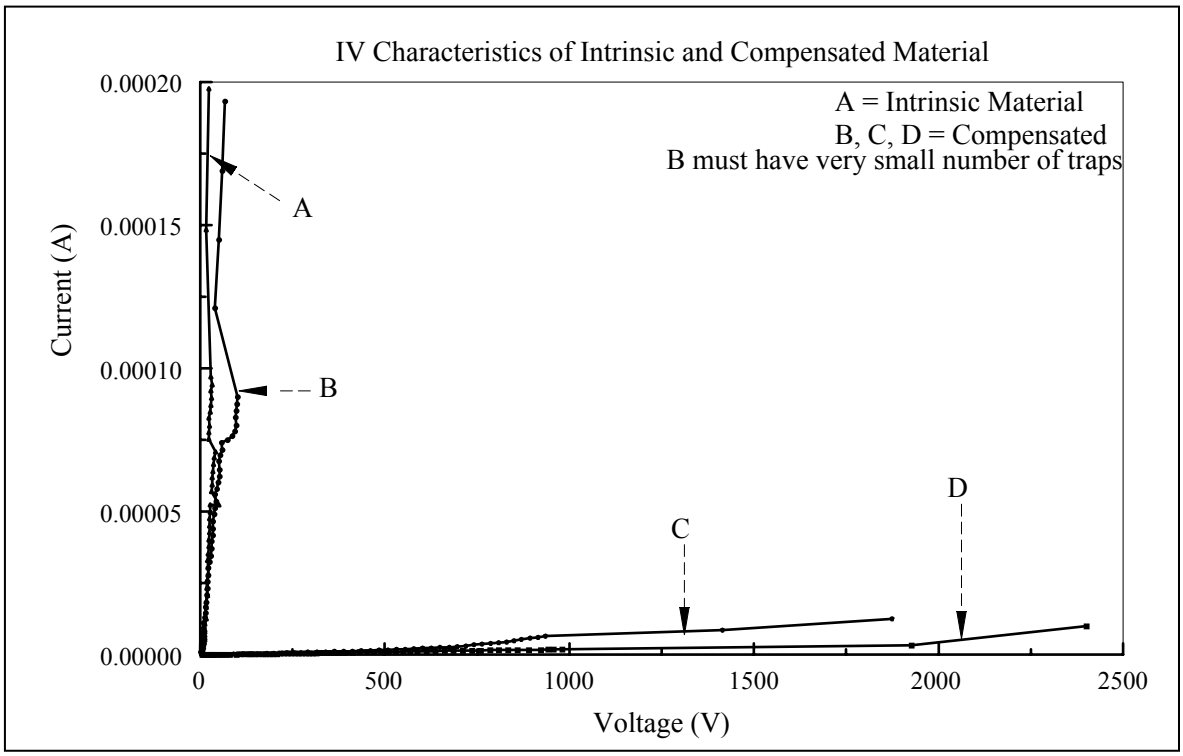


Figure 5.3. Experimental I-V characteristics (Low voltage) for material characterization

5.1.2. Method I : From the I-V characteristics

The equations used here are already explained in Chapter 2 and are reproduced here for simplicity. The first equation is the same for obtaining the trap filling limited current (Eqn 5.1). The second equation is Ohm's law (Eqn 5.2). The third equation gives the unoccupied trap concentration (Eqn 5.3).

$$V_{TFL} \cong \frac{Q_{TFL}}{C_0} \cong \frac{ep_{t,0}L^2}{\varepsilon} \Rightarrow p_{t,0} = \frac{\varepsilon V_{TFL}}{eL^2} \tag{5.1}$$

$$J = en_0\mu(V \ / L\ ) \Rightarrow n = \frac{JL}{e\mu V_{TFL}} \tag{5.2}$$

$$E_C - F = -kT\ln(\frac{n}{N_C}) \tag{5.3}$$

$$p_{t,0} = N_t - n_{t,0} \cong \frac{N_t}{g}\exp\left(\frac{E_t - F_0}{kT}\right) \tag{5.4}$$

The V_{TFL} can be obtained from the I-V characteristics, which can then be substituted in the Ohm's law equation to obtain the carrier concentration. Knowing the current, one can calculate the carrier concentration (Eqn.5.2). From carrier concentration one can calculate the Fermi level location (Eqn. 5.4). This result, when substituted into Eqn 5.4 along with $P_{t,0}$ obtained from Eqn 5.1, one can calculate the total trap concentration. The current and voltage measurements have to be accurate for this particular method for accurate trap calculations. Generally this method is used with the I-V characteristics obtained under inert conditions such as dark, thermal isolation. Since this was not possible because of the laboratory constraints, a different approach was then used.

5.1.3. Method II: From the slope of the I-V characteristics

From the equations of the Fermi level (in Chapter 3), the location of the Fermi level is dependent on the compensation ratio m, which then affects the free carrier concentration (Eqn. 5.5) that appears in the exponential factor. In other words, by Ohm's law, the current density is proportional to the carrier concentration. Hence, as the

compensation ratio, m, changes, the location of the Fermi level changes, affecting the free carrier concentration.

$$n_0 = N_C \exp[(F_0 - E_C)/kT] \tag{5.5}$$

A set of simulations was carried out using Matlab with different compensation ratios. The change in the slope of the I-V characteristic with the compensation ratio is shown in Fig. 5.4. Here, average mobility was assumed.

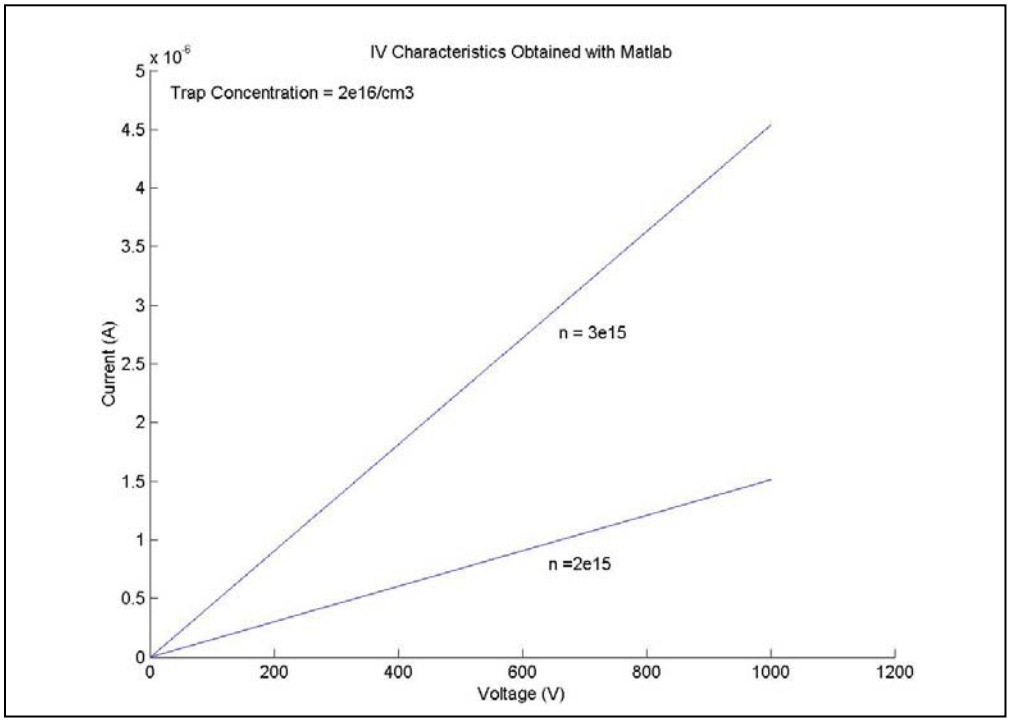


Figure 5.4. IV characteristics obtained with Matlab

Hence, by matching the experimentally obtained I-V characteristic's slope and the current magnitude to the simulations, the exact trap concentration and dopant (Nitrogen) density can be obtained. To implement this method, Fermi level calculations were done first. The effect of Fermi level on various parameters like recombination, material

polarity and the like was also studied to understand the PCSS behaviour at different biasing condition as explained in the next few sections.

5.1.3.1 Fermi Level calculations

There is a strong temptation to model the n^+-SI and p^+-SI junction behaviour using the same device physics equations that are required for p-n junction analysis. However this might lead to erroneous results, since the behaviour of deep levels in SI materials is significantly different than the single dominant shallow level. The difference lies mainly in the ionization of the deep trap level, which may be only partially ionized, and its ionization may change with operating conditions. Hence, to understand the behaviour of these junctions, the derivation and effect of the Fermi level on the electrostatic properties were studied in detail.

The location of the Fermi level in the bulk semi-insulating region can be determined from space charge neutrality requirements. Since the position of the Fermi level can be influenced by any of the many impurity levels, as well as by the free carrier densities, the conditions for charge neutrality become more difficult to isolate. Shockley devised a convenient method to graphically locate the Fermi level. Here, the net positive and net negative contributions to the space charge on a logarithmic scale are summed as a function of energy. Equating the net positive and net negative contributions allows the Fermi level to be located at the intersection of the two curves. The plots were obtained with the help of a mathematical tool MathCAD ™. The equations derived with the help of Darling's [21] analysis for SI GaAs will be shown in the following. The treatment

varies for DDSA and SDDA type semi insulating materials since the deep and shallow levels have different polarities.

I. Fermi level calculations for DDSA 6H SiC

Consider the case of DDSA SiC, where a balance is obtained between the deep lying donor level N_{DD} (V^{4+}/V^{5+}) and shallow acceptor N_{sa} (Boron). In the bulk of semiconductor, space charge neutrality requires that

$$P - N + N_D - N_A = 0 \tag{5.6}$$

Hence in this case one can write

N_{sa} = Ionized N_{DD}

$$\frac{N_{dd}}{1 + g_{dd} \exp[(E_F - E_{dd})/k_B T]} = N_{sa} \tag{5.7}$$

Solving for E_F, leads to,

$$E_F = E_{F,si} = E_{dd} - k_B T \ln g_{dd} + k_B T \ln(\frac{N_{dd}}{N_{sa}} - 1) \tag{5.8}$$

where N_{dd} = Density of the deep donor level /cm^3, N_{sa} = Density of the shallow acceptor level /cm^3, N_{da} = Density of the deep acceptor level /cm^3, N_{sd} = Density of the shallow donor level /cm^3, g_{dd} = Occupancy of the deep donor level, g_{da} = Occupancy of the deep acceptor level, E_F = Fermi energy level eV, E_{dd} = Deep donor energy level eV, E_{da} = Deep acceptor energy level eV, k_B = Boltzmann's constant, and T = Temperature in K

II. Fermi level calculations for SDDA 6H SiC

For a SDDA type material, one can write equation similar to those above, replacing deep donor by deep acceptor and shallow acceptor by shallow donor.

The equations in this case are as follows.

N_{sd} = Ionized N_{DA}

$$\frac{N_{da}}{1+(1/g_{da})\exp[(E_{da}-E_F)/k_BT]} = N_{sd} \tag{5.9}$$

This gives

$$E_{F,si} = E_{da} - k_BT\ln g_{da} - k_BT\ln(\frac{N_{da}}{N_{sd}} - 1) \tag{5.10}$$

Observe the dependency of the Fermi level on the compensation ratio in Eqns (5.8) and (5.10).

5.1.3.2. Calculations for Shockley plots

The procedure for constructing Shockley plot is as follows.

1. Calculate the density of states in the conduction and valence bands.
2. Calculate the hole density at the top of valence band and the electron density at the bottom of the conduction band using the data in step 1.
3. Plot the electron and hole densities from 0 to 3.02 eV. The intersection of the electron and hole density curves gives the intrinsic energy location in the material.
4. Similarly, depending on the material type e.g. SDDA or DDSA, the ionized densities of the donors and /or acceptors can be calculated. When the ionized densities are plotted as in step 3, the intersection of the two curves gives the Fermi energy location.

   The above procedure has been implemented to construct Shockley plots.

The density of states in the conduction band and valence band are given in [9]

$$N_C = 2\left(\frac{2\pi m_{de}k_BT}{h^2}\right)^{1.5} \tag{5.11}$$

$$N_V = 2\left(\frac{2\pi m_{dh} k_B T}{h^2}\right)^{1.5} \tag{5.12}$$

where m_{de} is the effective conduction band mass of an electron for 6H SiC a value of 2.13×10^{-30} kg

m_{dh} is the effective valence band mass of a hole for 6H SiC (9.1×10^{-31} kg)

k_B is Boltzmann's constant

T is temperature

h is Plank's constant

The hole density at the top of the valence band is given by [9]

$$N_h = N_V \exp\left[\frac{-q(E - E_V)}{k_B T}\right] \tag{5.13}$$

The electron density at the bottom of the conduction band is given by [9]

$$N_e = N_C \exp\left[\frac{-q(E_C - E\ )}{k_B T}\right] \tag{5.14}$$

where E_C and E_V are the maxima and minima of the conduction and valence band energies respectively.

The energy is varied from 0 to Ec = 3.02 for 6H SiC and the corresponding N_h and N_V values are plotted with respect to energy as shown in the Fig. 5.5. The intersection of the two curves gives the intrinsic Fermi energy $E_i \sim 1.511$eV.

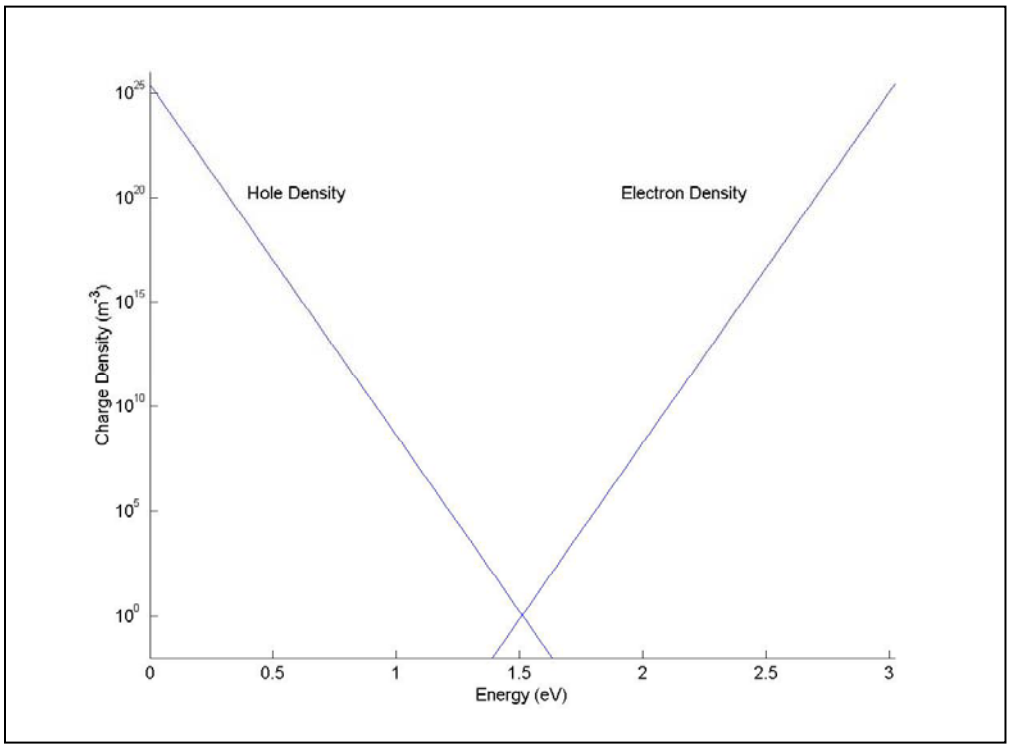


Figure 5.5. Graphical calculation of Intrinsic Energy E_i

I. Shockley plots for DDSA 6H SiC

The number of ionized donors and acceptors as given in [8], are

$$N_{di} = N_{dd}\left[1 - \frac{1}{1+\exp\left[\frac{q(E_d - E}{k_B T}\right]}\right] \tag{5.15}$$

$$N_{ai} = N_{sa}\left[\frac{1}{1+\exp\left[\frac{q(E_a - E}{k_B T}\right]}\right] \tag{5.16}$$

where E_d is the energy of the deep donor level ($V^{4+/5+}$) = 1.6eV

E_a is energy of the shallow acceptor (Boron) = 0.03eV

Here, $N_{dd} = 2x10^{16}/cm^3$ and $N_{sa} = 2x10^{15}/cm^3$.

Again the energy is varied from 0 eV to 3.02 eV and the corresponding N_{di} and N_{ai} values are plotted (Fig 5.6). The intersection of the two curves gives the location of the Fermi level about 1.639eV. It can also be calculated from Eqn. 3 and can be verified from the plots.

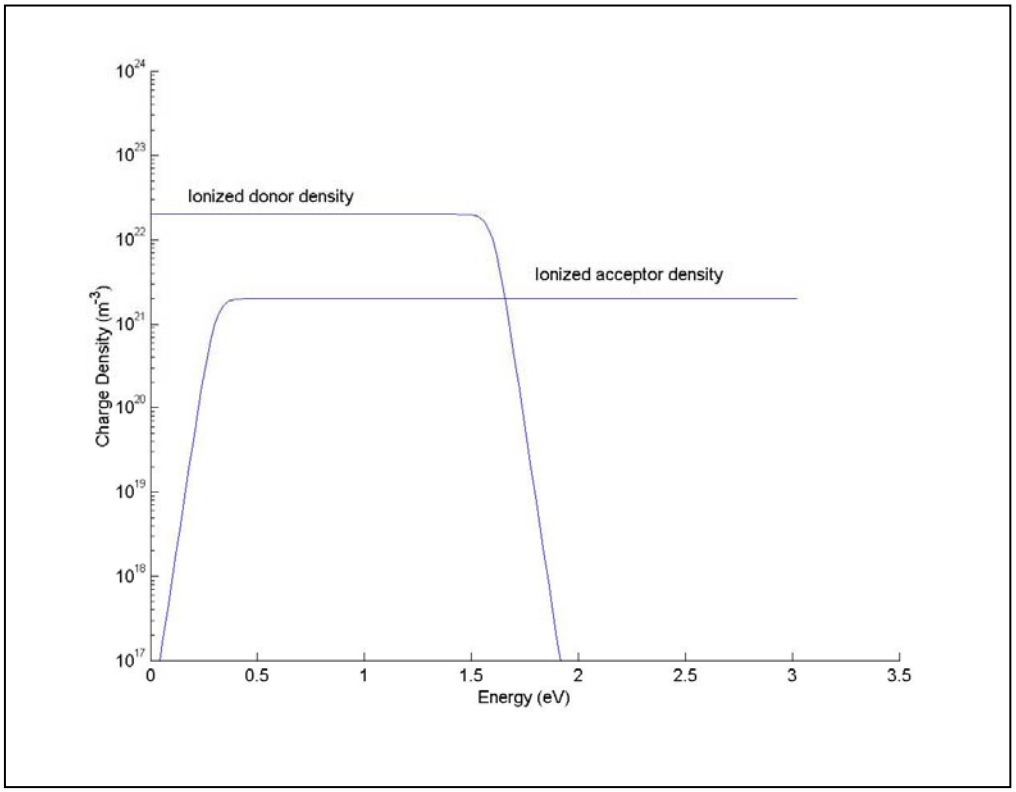


Figure 5.6. Shockley plots for DDSA SiC

II. Shockley Plots for SDDA SiC

The procedure for obtaining the Shockley plots for SDDA type SiC is similar to that given above for DDSA SiC with some minor differences. The deep trap level is now acceptor and the shallow level is donor. The intrinsic energy location is the same as for

the DDSA (Fig.5.5). The Shockley plot is shown in Fig. 5.7. The Fermi level is located at approximately 2.187eV from the valence band edge.

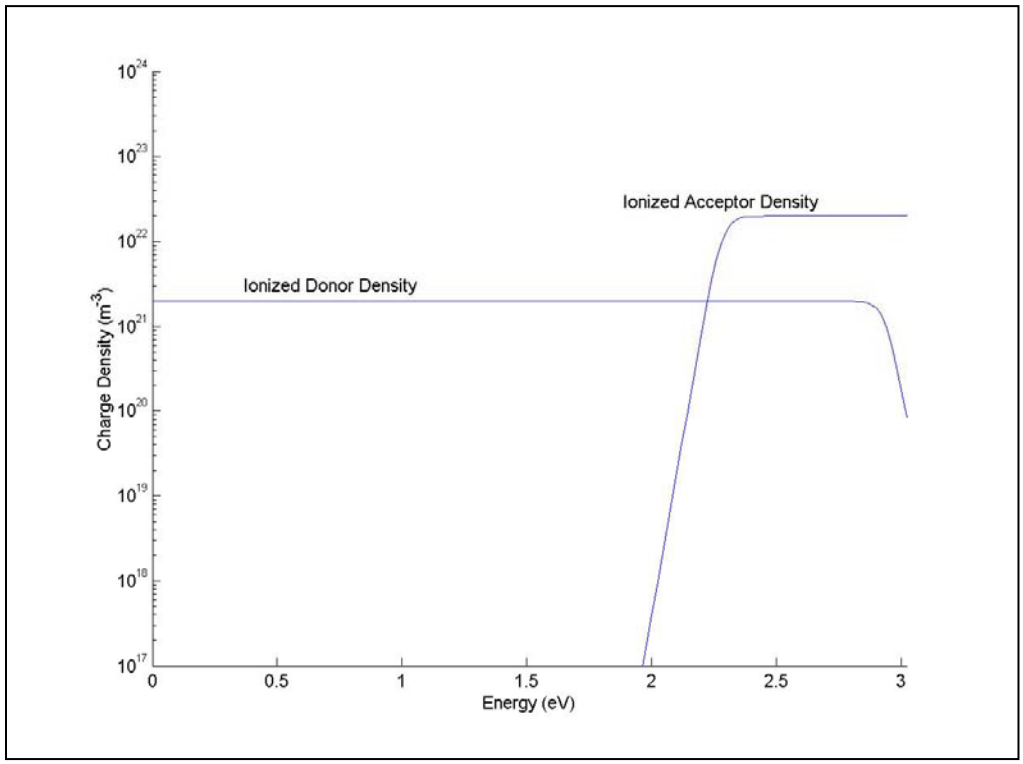


Figure 5.7. Shockley plots for SDDA SiC

The Shockley plot helps in obtaining the exact location of the Fermi level in the material. In the case of both DDSA and SDDA types, the Fermi level is locked to a location near the deep trap level making the material semi insulating. The effect of the Fermi level on different parameters such as the Polarity of the material, the Photo Current and the recombination rate is explained below.

5.1.3.2. Effect of Fermi level on material polarity

From Section 5.1.3.1, the material polarity is dependent on the compensation ratio, m. Hence, after finding out the exact location of the Fermi level in the available SI SiC material, the next step was to analyze the material polarity along with the application

of a p^+/n^+ layer and its effect on the material behaviour for improving the hold-off voltage.

From the Fermi level equations for DDSA (Eqn. 3) and SDDA (Eqn 5.) type materials, we define the compensation ration, $m = N_{dd}/N_{sa}$ for the DDSA material and $m = N_{da}/N_{sd}$ for the SDDA material. Depending on the compensation ratio, four different cases exist as follows.

1. $N_V > N_D - N_A > 0$: Vanadium compensates shallow donors, which may themselves be partially compensated by acceptors. Nitrogen donors are compensated by V^{3+}/V^{4+}. The Fermi energy is observed to be close to the acceptor level. As the compensation ratio $m = \frac{N_V}{N_D - N_A}$ increases, the Fermi level moves further down. This type of material can be classified as SDDA (Shallow donor deep acceptor).

2. $N_V > N_A - N_D > 0$: Vanadium compensates shallow acceptors which may themselves be partially compensated by donors. Boron is compensated by V^{4+}/V^{5+} donor level formed by vanadium. The Fermi level is pinned to the deep donor level. As the compensation ratio $m = \frac{N_V}{N_A - N_D}$ increases, the Fermi level moves upwards. This type of material can be classified as DDSA.

3. $N_D > N_V + N_A$: Domination of shallow donors leads to n type conducting behaviour.

4. $N_A > N_V + N_D$: Domination of shallow acceptors leads to p type conducting behaviour.

For cases 1 and 2, some arbitrary values of the trap density and the n or p type shallow impurity were considered (the compensation ratios used in this case are from the GaAs experimental data [19, 21, 38]; no such data has been published for SiC until now). The

locations of the Fermi level and the intrinsic Fermi level were calculated in a similar way as was done in the previous section for Shockley plots. The material remains n type as long as the Fermi level E_F lies above the intrinsic Fermi level E_i and vice a versa. The importance of evaluating the material type will be elaborated on when the discussion on improving the breakdown voltage of SiC switches in a later section.

Case 1 DDSA

Material Parameter	C1	C2	C3	C4
Trap Density /cm^3	3.006e^{15}	3.18e^{15}	8e^{16}	2e^{16}
Boron Density /cm^3	3e^{15}	3e^{15}	5e^{16}	2e^{15}
Compensation ratio (m)	1.002	1.06	1.6	10
Fermi Level (E_F) eV	1.421	1.51	1.569	1.639
Intrinsic Fermi (E_i) eV	1.51	1.51	1.51	1.51
Type	P	$E_f = E_i$	N	N

Table 5.1. Compensation ratio and its effect on DDSA material polarity

The effect of the compensation ratio, m, on the polarity of DDSA SiC is given in Table 5.1. The material polarity remains p type as long as m is equal to or less than 1.06. Otherwise it is n type.

Case 2 SDDA

Material Parameter	C1	C2	C3	C4
Trap Density /cm^3	3.006e^{15}	3.18e^{15}	8e^{16}	2e^{16}
Nitrogen Density /cm^3	3e^{15}	3e^{15}	5e^{16}	2e^{15}
M	1.002	1.06	1.6	10
Fermi Level (E_F) eV	2.405	2.317	2.257	2.187
Intrinsic Fermi (E_i) eV	1.51	1.51	1.51	1.51
Type	N	N	N	N

Table 5.2. Compensation ratio and its effect on SDDA material polarity

The effect of compensation ratio, m, on the polarity of SDDA SiC is given in Table 5.2. The material is n type irrespective of the value of the compensation ratio m.

5.1.4. I-V matching

The concentration of nitrogen dopant, as supplied by the vendor, was found to be between 2-7×10^{15}/cm^3. Vanadium trap concentration was increased in steps to obtain a compensation ratio that matches the measured I-V. A good match was possible for vanadium concentration of 2×10^{16} /cm^3, which gives a compensation ratio of 10. Since there are two trap levels present in the semi-insulating 6H SiC [24], simulations were also carried out with two traps and also with each individual trap present in the material. The best correlation with the measured I-V characteristics was possible with one single trap level at Ec-0.74 eV (2.28 eV). This level is assumed to be the dominant trap level and is used in subsequent simulations. The dominance of the single trap level was expected due to its proximity to the Fermi level as discussed below.

In trap-dominated materials, the trap energy level, its density and capture cross sections also affect the material parameters and its charge conduction characteristic. Material parameters affected include the location of the Fermi level (E_F), which determines whether a trap level (E_t) is shallow or deep. For a shallow trap, E_F lies below the trap level and for a deep trap, E_F lies above E_t. The location of the Fermi level in the bulk of the semi-insulating region is determined from space charge neutrality requirements. Since the position of the Fermi level can be influenced by any of the impurity levels, as well as the free carrier densities, the conditions for the space charge neutrality for a compensated material become more difficult to isolate. For compensated materials that include traps and donor/acceptor levels, the Fermi level also changes and influences the conduction process. For the SDDA material under consideration, the Fermi

level position can be set as shown in Eqn (5.17). This equation is the same used earlier in Section 5.1.3.1 for SDDA material and repeated here for convenience.

$$E_{F,si} = E_{da} - k_B T \ln g_{da} - k_B T \ln(m-1) \tag{5.17}$$

where $m = \frac{N_{da}}{N_{sd}}$ N_{da} = Density of the deep acceptor level /cm^3, N_{sd} = Density of the shallow donor level /cm^3, g_{da} = Occupancy of the deep acceptor level, E_F = Fermi energy level eV, E_{da} = Deep acceptor energy level eV, k_B = Boltzmann's constant, and T = Temperature in K. This is in contrast to the Fermi level equation for intrinsic material that does not depend on the compensation ratio m. A typical Shockley plot, prior to laser application in the active region of the PCSS, is shown in Fig. 5.7, for a compensation ratio of 10. At the onset of conduction process, the Fermi level tends to move up as more and more trap levels are filled and the compensation ratio changes. On the other hand, the free carrier densities have little or no impact on the position of the Fermi level, which is a characteristic and desirable feature of the semi insulating material. The plot shows a Fermi level at 0.833eV from the conduction band (2.187eV from the valence band). Since the intrinsic energy level is located at 1.511eV from the valence band, the material is n type. Such traps sites, also classified as acceptors (0/-), will influence the conduction process. The Shockley plots are consistent with plots based on similar equations for compensated SDDA GaAs. Here, as the compensation ratio increases the Fermi level moves down and is in agreement with the observations of Bickermann et al [22]. From Fig. 5.8, the simulation I-V matches with the experimental data for the compensation ratio 10. This fit takes into account the compensation ratio as well as the current magnitude.

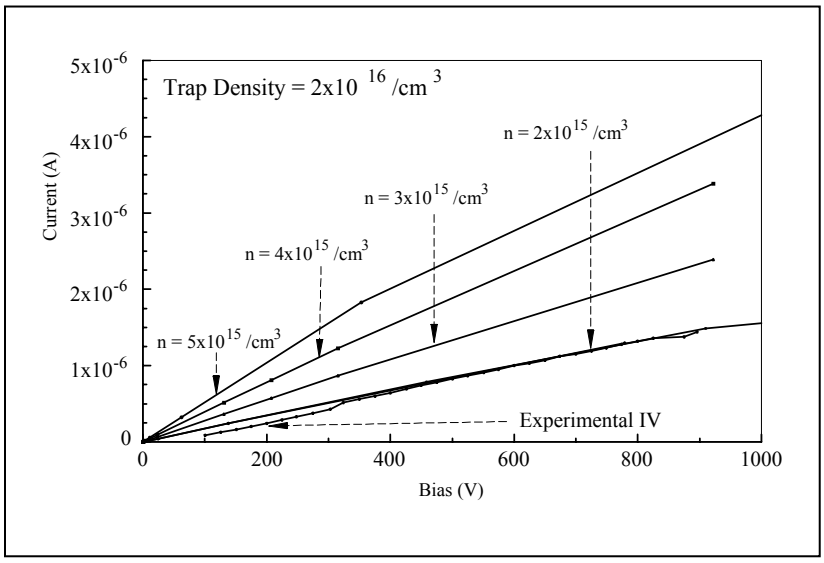


Figure 5.8. Effect of compensation ratio on the slope of the IV characteristics

5.2. Preliminary Switch Simulation Analysis

5.2.1. Current Injection in Solids

The preliminary simulations were conducted to find out the switch behavior with the compensation ratio obtained in the last section. The switch was simulated with the models presented earlier in Chapter 2. Since the objective was to obtain the magnitude of the trap filling limited voltages (Theory in Chapter 2), the switch was assumed to have perfectly ohmic contacts with a single trap level. Both the SDDA and DDSA type materials were considered individually in the switch geometry to be explained earlier.

I. SDDA SiC

Simulation of the SDDA type material with the trap density $2x10^{16}/cm^3$ and a nitrogen dopant of $2x10^{15}/cm^3$ (Column 4 in Table 5.2) produced an I-V characteristic as shown in Figure 5.9. The Vanadium trap level at 0.74 eV from conduction band qualified

as a shallow trap level (according to Lampert's theory) since the Fermi level is located at 0.833 eV from the conduction band, 0.093 eV below the trap level. One can expect $V_{TFL\ I}$ and $V_{TFL\ II}$ region formation with different slopes. If the Fermi level F is below the trap level, as is the case for shallow traps, it keeps on rising as the carrier injection increases. At some voltage V, it will cross the trap level E_t. This cross-over will change the slope of the I-V characteristics, since now most of the trap levels are completely filled. Hence, the injected charge will directly account for the increased current flow. The voltage at which this happens is called as $V_{TFLI,}$ and this phenomenon is named the Trap Filling Limited (TFL) law. Once the Fermi level passes the trap level by 0.7kT [8], the characteristic merges with the trap free square law level marked as $V_{TFL\ II}$. For a switch length of 400μm, the $V_{TFL\ I}$ and $V_{TFL\ II}$ corresponded to 650 V and 25 kV respectively (Fig 5.9).

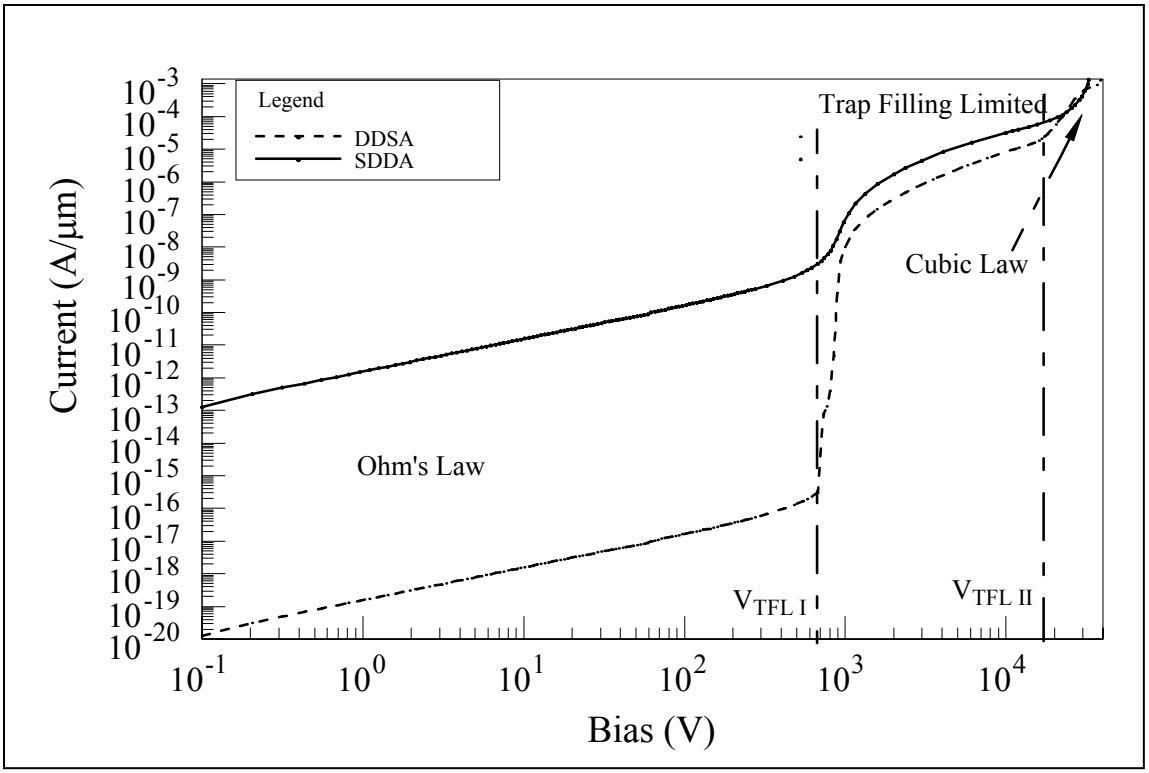


Figure 5.9. SiC Log – Log I-V characteristic

II. 6H DDSA SiC

The DDSA SiC with Vanadium deep donor level and boron shallow acceptors was studied with exactly the same constraints as above. For this case, the trap level qualified as a deep level with a Fermi level located at 1.639 eV; 0.039 eV above the trap level. Ohm's law applied until the thermally free carrier concentration n_0 became higher than the injected free electron charge n_i. Once these two became comparable, an upwards shift in the quasi Fermi level from the Fermi level was observed. Since the free electron concentration $n = n_i + n_0$ doubled at the cross over, the quasi Fermi level jumped up precisely by 0.7kT. This motion was sufficient to fill all the deep traps. The cross over voltage V_{TFL} was similar to the SDDA case. Note that the upward shift for the DDSA case from Ohm's law was much higher than that for the SDDA material due to the deeper location of the trap levels. Also, note that the two curves merged in the trap free square law regime where the effect of traps was negligible and the free carrier concentration dominated the I-V characteristic.

The I-V characteristic obtained in this section was then compared to Lampert's analysis. Few differences in the slopes were observed. The code considered the diffusion current and was not excluded from the analysis. The two carrier injection case was considered. This did not change the basic characteristics until $V_{TFL\ I}$ but had some impact on the $V_{TFL\ II}$ and trap free square law regime. Since, for the SDDA material, $\sigma_P >> \sigma_N$, the lifetime of the injected holes was much smaller than that of the electrons initially. The only limitation to the electron flow is its own space charge. Hence, the I-V characteristic up to $V_{TFL\ II}$ the regime was essentially electron dominated. As the voltage was increased further, the I-V characteristics was dominated by the trap free double injection cubic law.

This can explain the higher slope at the extreme right of the I-V characteristic. Similar arguments can be made for the DDSA type material. Note that experimental observation of the different trends in the I-V characteristic may not be possible depending on the material purity, measurement techniques, the presence of many trap levels and the like.

5.2.2. Effect of traps on recombination time

The main objective here was to find out the lifetimes of the carriers in SiC. The cross sections for the trap level were obtained from [24]. However, no data has been published to date about the lifetimes associated with these trap levels. In this section, a simplified theory is discussed in regard to the effect of the Fermi level on the trap recombination time, followed by experimental matching of the transient PCSS response to the simulations considered in the next chapter.

The location of the Fermi level has a profound effect on the recombination time. This is due to the fact that the occupancy of a trap level is a function of the Fermi level location.

I. SDDA Case

When a trap level is above the Fermi level, it is qualified as a Shallow Trap as discussed earlier in Chapter 2. The number of traps occupied by electrons at room temperature can be found in [8] and is plotted in Fig. 5.10.

$$n_{t,0} = \frac{N_t}{1 + (1/g)\exp[(E_t - E_f)/kT]} \tag{5.18}$$

where $n_{t,0}$ = Filled electron traps at energy level E_t

N_t = Total trap concentration

g = Degeneracy factor = 4 for Acceptor like trap level.

Note that the trap concentration and the n type doping were kept at $2x10^{16}/cm^3$ and $2x10^{15}/cm^3$, respectively, to be consistent with the previous calculations.

From Fig. 5.10, when the quasi Fermi energy is close to the actual Fermi energy, very few traps are occupied by electrons. This scenario changes drastically as the quasi Fermi level moves towards the conduction band due to injection and all the traps are filled with a movement of 0.1eV. Thus, from the analysis in the previous section, biasing the PCSS close to $V_{TFL\ II}$ can ensure the maximum occupancy of the trap level, providing minimum on-state switch resistance.

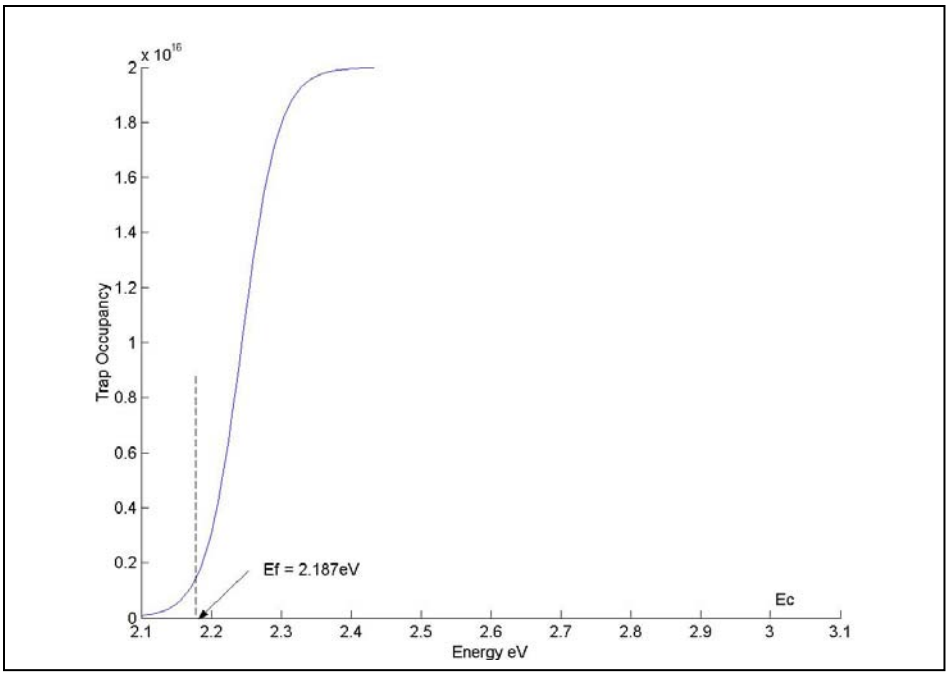


Figure 5.10. Occupancy of a Deep Acceptor trap level with respect to Fermi Level

II. DDSA

Similarly for the DDSA type SiC, the Fermi level is close to the deep donor trap level. In this case, also, the location of the Fermi level changes with the compensation

ratio as mentioned in the previous discussion. The material is n type for a $2x10^{16}/cm^3$ trap concentration and $2x10^{15}/cm^3$ p type doping. The Fermi level lies at 1.639eV from the valence band and is above the trap energy level at 1.6eV, making the trap level deep. In this case, it was easier to calculate the number of traps not occupied by the electrons using [8]

$$p_{t,0} = N_t - n_{t,0} = \frac{N_t}{1 + g\exp[(E_f - E_t)/kT]} \tag{5.19}$$

Therefore $$n_{t,0} = N_t - \frac{N_t}{1 + g\exp[(E_f - E_t)/kT]} \tag{5.20}$$

where $p_{t,0}$ = Number of traps not occupied by the electrons The occupancy of the deep donor trap level with respect to the Fermi energy is as shown in figure 5.11.

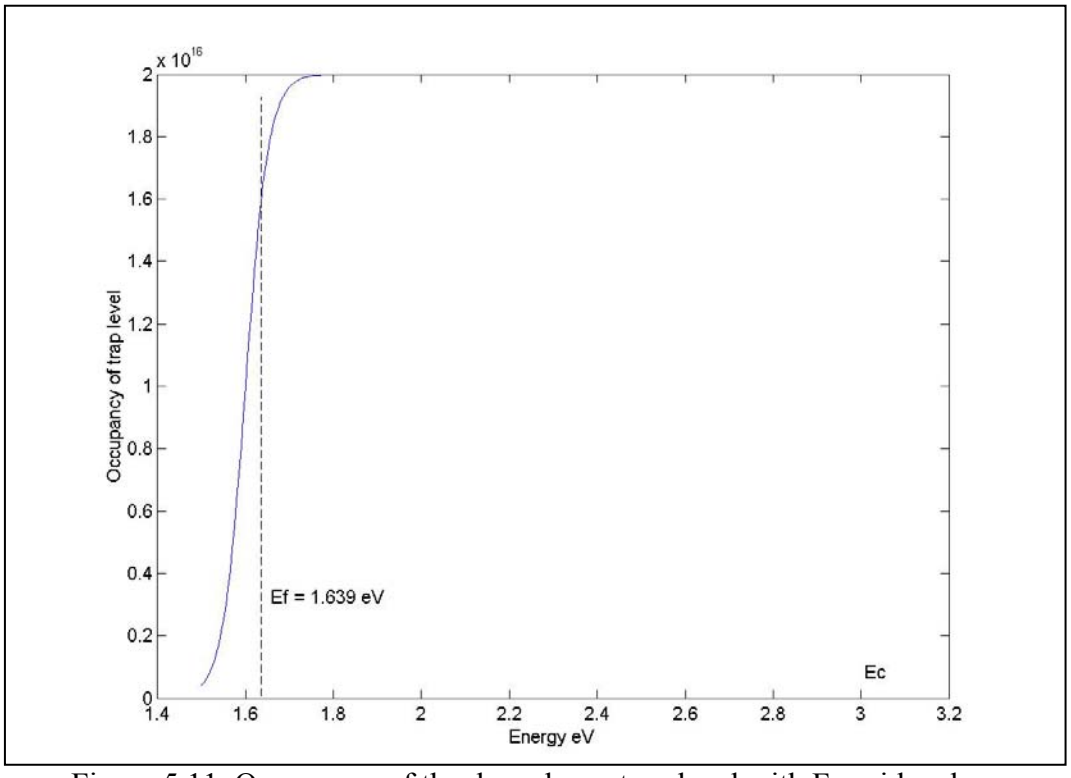


Figure 5.11. Occupancy of the deep donor trap level with Fermi level

Upward movement of the quasi Fermi level due to injection, fills almost all of the traps (Fig. 5.11), thus providing maximum possible switch conduction. In this case also, switch biasing above V_{TFL} will ensure maximum switch current only limited by the external power supply.

In conclusion, a quasi Fermi level shift by 0.1eV from the original location can provide a maximum photocurrent from a particular trap level. This is also important from the biasing point of view because the minimum switch on-state resistance depends on the carrier generation in the illuminated switch.

5.2.3. Effect of Fermi level location on the recombination statistics

Recombination in a semiconductor can be of many different types.

1. Trap Assisted (SRH)
2. Auger
3. Direct (band to band).

SiC, which is an indirect band gap material recombination mechanism number three, but this is insignificant since the analysis is concerned with only one type of carrier polarity. If the carrier densities are small ($<1x10^{18}/cm^3$), Auger recombination can be neglected. The material recombination rate for a large number of traps can be given as in [8]

$$r = n^* < v\sigma > *(N_t - n_t) \tag{5.21}$$

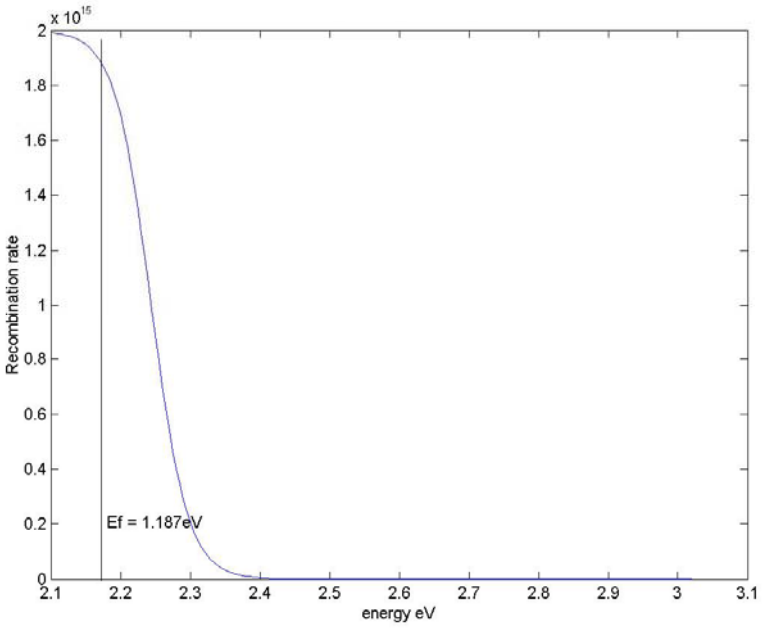
where r = recombination rate, v = carrier thermal velocity, σ = capture cross section, N_t = Total Trap concentration, and n_t = Number of traps occupied by electrons.

Therefore $N_t - n_t$ gives the total number of traps not occupied by electrons.

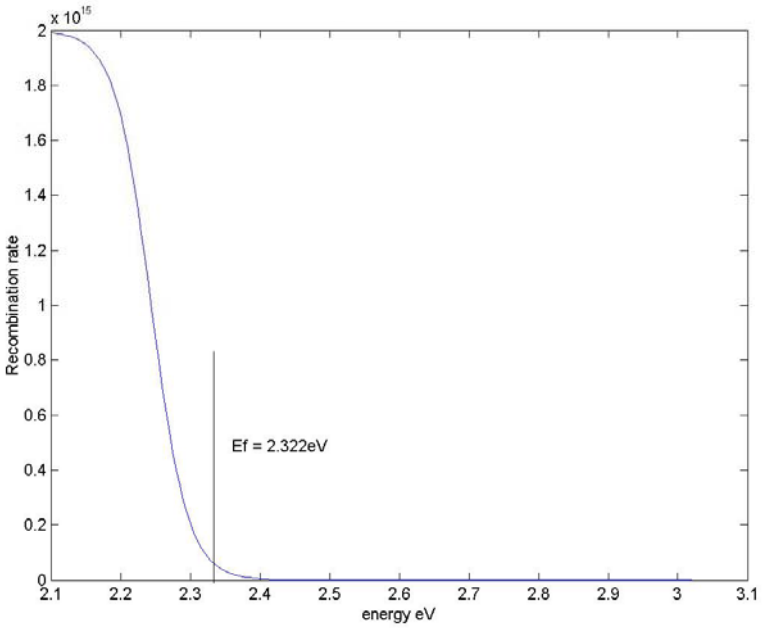
The number of traps not occupied by electrons is indeed dependent of the Fermi level in the material (previous section). Hence, the location of the Fermi level with injection was considered, in order to calculate the trap assisted (Shockley Reed Hall) SRH recombination rate.

I. SDDA

Instead of changing the location of the Fermi energy with biasing, the compensation ratio was changed in this case. The compensation ratios in Columns 1 and 4 in Table 5.2 were used. For a compensation ratio of 10 (m = 10), the recombination rate was significantly higher than the m = 1 case (Fig. 5.12). This was expected since a large number of traps were unoccupied for the higher compensation ratio (previous section).



a. m = 10

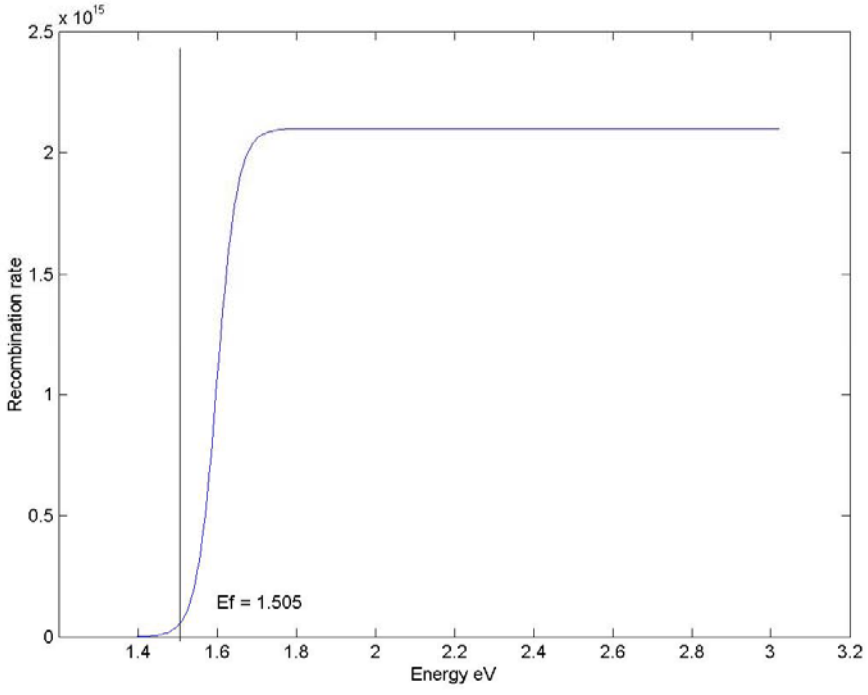


b. m ~ 1

Figure 5.12. Recombination rate as a function of Fermi level in a SDDA 6H SiC

II. DDSA

A deep donor shallow acceptor type of SiC with $2.1x10^{16}/cm^3$ trap concentration and $2x10^{15}$ p type doping was used initially. The Fermi level in this case is locked to 1.505eV just below the deep donor trap level, which is at 1.6eV. This makes the trap level shallow, since it is above the trap level. Calculating the recombination rate with these values and with the help of Eqn 5.21, produced a profile as shown in Figure 5.13a. As can be seen from the plot, as long as the Fermi level is close to the 1.505eV the recombination rate was very small. Changing the compensation ratio, the trap concentration $2x10^{16}/cm^3$ and using $2x10^{15}$ p-type doping established the Fermi level at 1.639eV. This value is above the trap energy at 1.6eV. Calculations indicate a higher recombination rate than in the earlier case.



a. m ~1

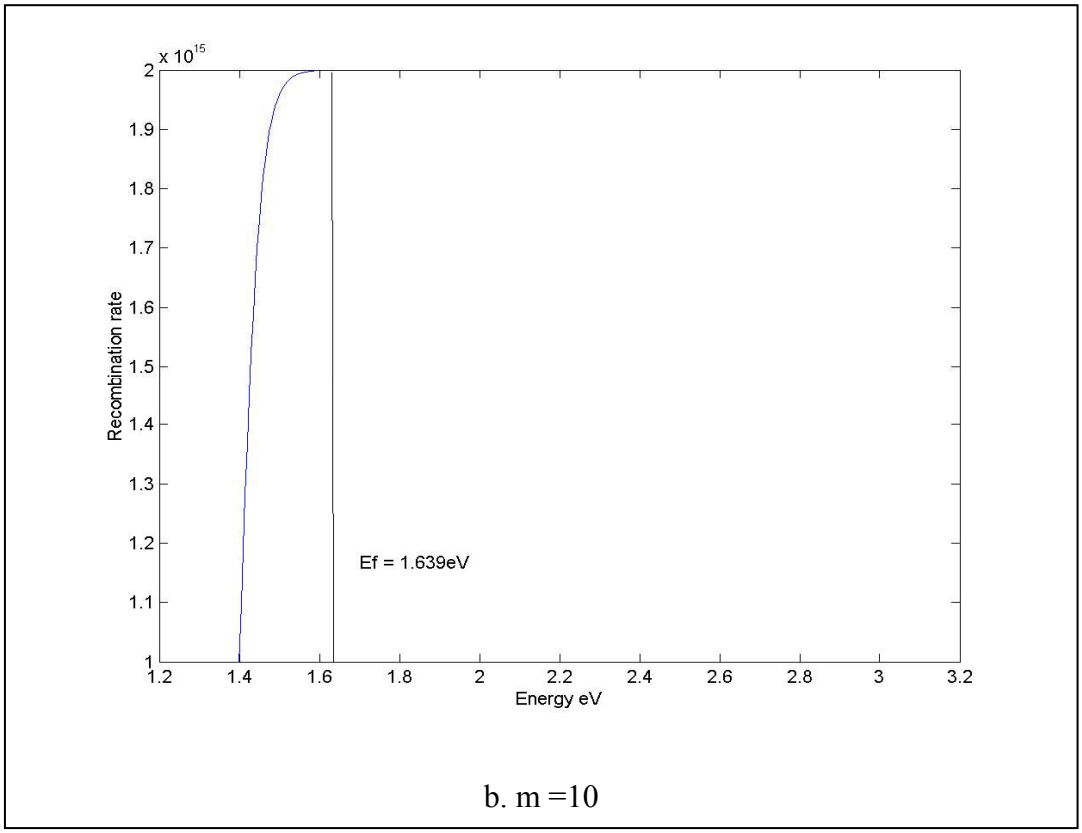


Figure 5.13. Recombination rate as a function of Fermi level in a DDSA 6H SiC

This has a direct impact on the tail current after the end of optical pulse. Hence, precise control of the compensation ratio can provide manipulation of the switch opening time since more empty traps have a higher probability of trapping.

Chapter 6

Transient PCSS Response Experiments and Simulations

One of the most important results of the UMC MURI project was the development of the extrinsic photo-conductive switch approach for the purpose of controlling the current density within the switch. Previous work in high power photoconductive switches employed intrinsic photo conductivity in which the photon energy, used to change the resistance of the semi-conductor material between the contacts, was greater than the band gap energy. Extrinsic photo-conductivity employs photon energies less than the semiconductor band gap energy. The following discussion

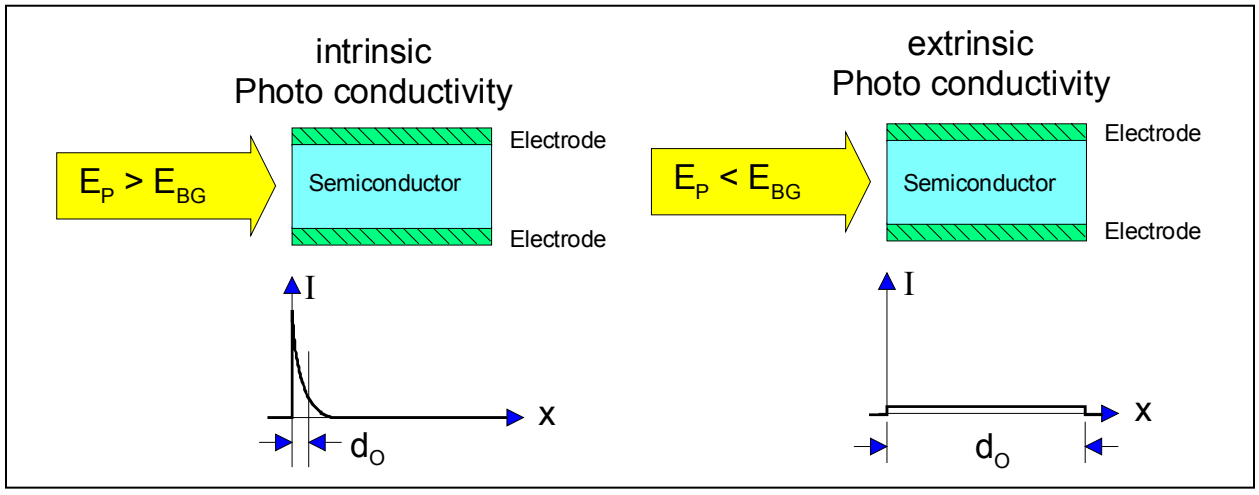


Figure 6.1. Extrinsic vs. Intrinsic Photoconductive Switch Current Densities

involves linear photo-conductivity, both intrinsic and extrinsic, in which each absorbed photon produces only one electron hole-pair and impact ionization is not involved.

In the intrinsic photo conductivity case, the optical absorption depth is on the order of tens to hundreds of microns depending on the photo conductor [7]. The small optical absorption depth results in a very large current density in the switches and a limitation in the current per unit width of the switch. An alternative view is that intrinsic photo conductivity limits the cross sectional area that can be accessed by the optical closure energy. Thus, the current capability of intrinsic photo conductive switches has been limited by the current density damages in the contacts and the bulk semiconductor material. The UMC approach, developed and demonstrated in this project, employed extrinsic photo conductivity in which the density of interband dopants determines the optical absorption depth and thus current density in the switch, in the absence of avalanche conduction due to impact ionization. The difference in extrinsic photo conductive switches and intrinsic photo conductive switches is illustrated in Fig. 6.1. Furthermore, once all the interband dopants have been excited by the absorbed optical energy, no additional current carriers are available and the current density has an upper limit which extends contact lifetime and bulk material lifetime. One important criteria for an extrinsic photo conductive switch is that the background material must have a very large band gap so that avalanche conduction and thermal runaway is improbable. The optical absorption depth was thus required at the wavelength of interest (532, 1064 nm). A literature search indicated that no such data has been published; hence procedures were carried out to measure the optical absorption depth experimentally.

6.1. Optical Absorption Depth Measurement

For measuring the optical absorption depths, following analysis was done.

From Fig. 6.2 (A), the critical angle inside the silicon carbide is

$$\theta_{critical} = \sin^{-1} \frac{1}{n_{SiC}} \tag{6.1}$$

$n_{SiC} = 2.55$, refractive index of silicon carbide

The incident ray will be confined in the silicon carbide for all θ_i because of the following calculation under the condition that

$$\theta_r \geq \theta_{critical} \tag{6.2}$$

and the initial Snell's law for the incident ray (from air to silicon carbide) is

$$\sin\theta_t = \frac{1}{n_{SiC}} \sin\theta_i \tag{6.3}$$

For the refraction inside the silicon carbide, one can use Eqn 6.2 and then

$$\sin\theta_r = \sin(90° - \theta_t) \geq \sin\theta_{critical} \tag{6.4}$$

therefore Eqn 6.4 becomes

$$\sin(90° - \theta_t) = \cos\theta_t \geq \sin\theta_{critical} \tag{6.5}$$

Combine Eqn 6.1and 6.5,

$$\cos\theta_t \geq \frac{1}{n_{SiC}} \tag{6.6}$$

By using Eqn 6.3 and 6.6, the following condition will be derived

$$\cos\theta_t = \sqrt{1 - \sin^2\theta_t} = \sqrt{1 - \frac{1}{n_{SiC}^2} \sin^2\theta_i} \tag{6.7}$$

Combining Eqn 6.6 and 6.7, the result shows

$$\sqrt{1 - \frac{1}{n_{SiC}^2} \sin^2\theta_i} \geq \frac{1}{n_{SiC}} \tag{6.8}$$

The condition derived from Eqn 6.8 can again be simplified to

$$n_{SiC}^2 \geq 1 + \sin^2 \theta_i \tag{6.9}$$

For $\theta_i = 0 \sim 90°$, the derivation in Eqn 6.9 gives

$$n_{SiC} \geq 1.414 \tag{6.10}$$

Eqn 6.10 is the condition derived by the ray optics for which the optical wave will be totally confined inside the silicon carbide; $n_{SiC} = 2.55$ is used.

From Fig. 6.2 (B),

$$n_{air} \sin \theta_i = n_{SiC} \sin \theta_t = n_{air} \sin \theta_o \tag{6.11}$$

Therefore $\theta_i = \theta_o$, and derived by geometrical derivations,

$$D = \frac{L \cdot \sin(\theta_i - \theta_t)}{\cos \theta_t} \tag{6.12}$$

Optical measurements on the actual switch proved very difficult since only a small edge (400μm) was being utilized. Optical reflections were observed to be large and hence the total laser energy on the other side could not be measured accurately. Hence, accurate measurement could not be done.

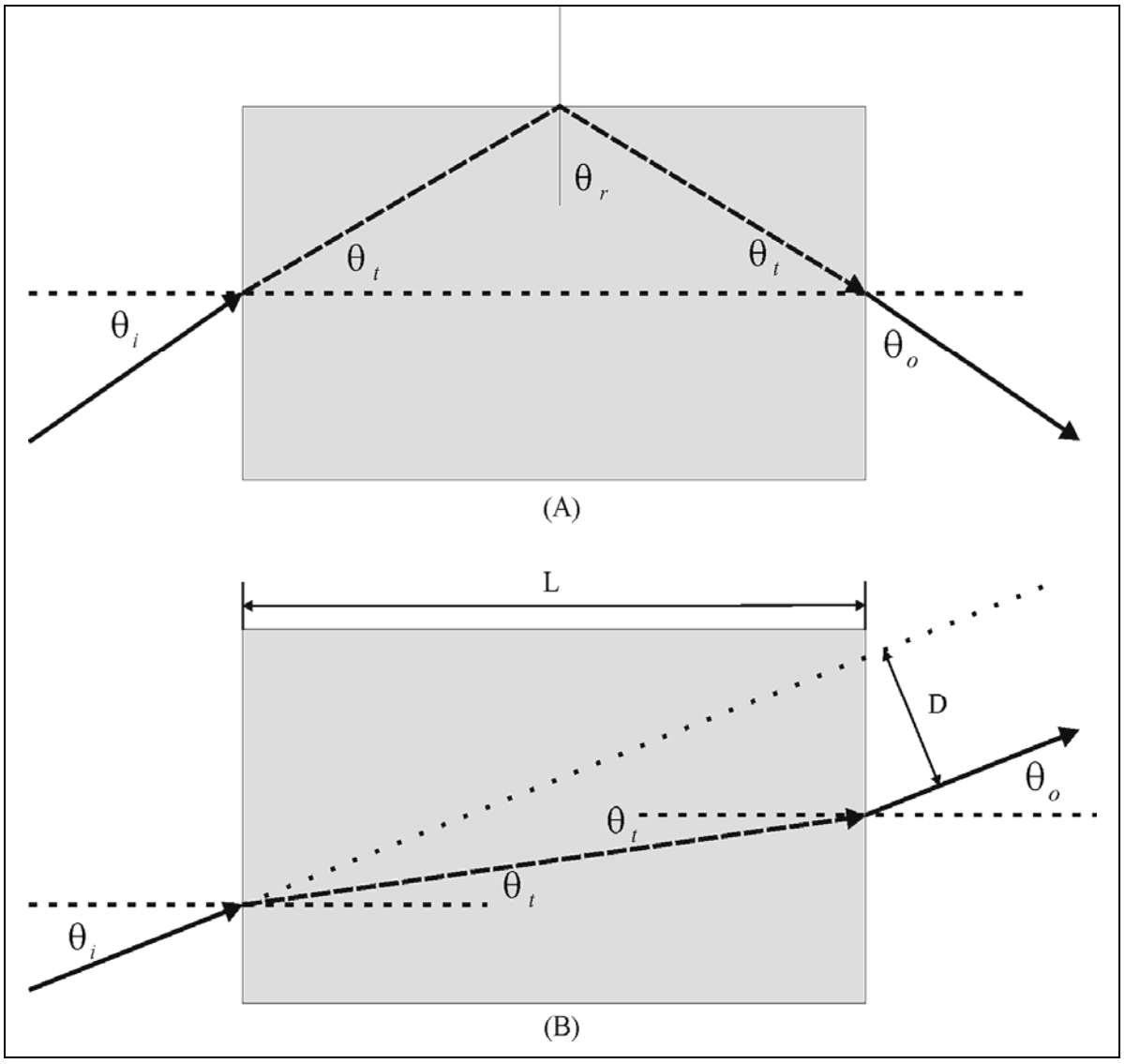


Figure 6.2. Ray Optics for the SiC

A small code was developed at UMC to measure the optical absorption depth and the results are discussed below. Previous work on the optical absorption measurement on 6H SiC was researched again and few citations were found.

As shown in Figure 6.3 [10], the optical absorption coefficient in 6H SiC, at a 532 nm wavelength is ~2.3 cm^{-1} and at a 1.06 μm wavelength it is ~2.1 cm^{-1}. Similar work indicated an optical absorption coefficient of 0.4-0.6 cm^{-1} at a 623 nm wavelength [39].

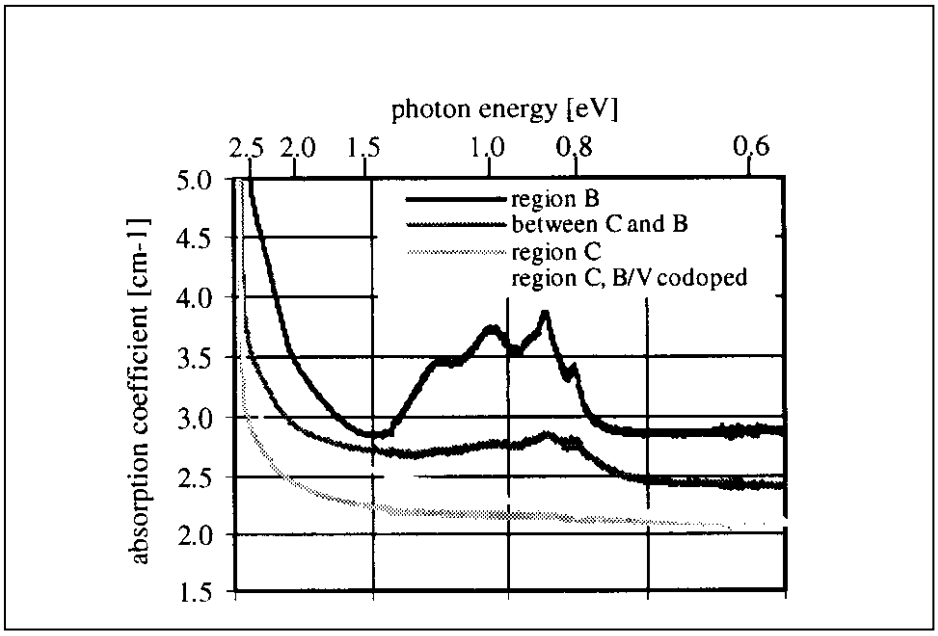


Figure 6.3. Absorption coefficient with wavelength

A Code was developed to model the optical absorption in the PCSS. PCSS geometry used earlier was considered with optical illumination from one side. The following assumptions were made in this analysis.

1. One photon is necessary to create a free electron from the trap level.

2. Quantum efficiency is assumed to be one.

3. 6H SiC has been observed to be transparent for band gap illumination with optical peaks at the wavelengths where the deep trap levels lie [27]. Thus, the laser energy will be absorbed if the trap level has sufficient trapped electrons that can be released.

Otherwise, the material would appear transparent as mention previously by Bickermann et al [27].

4. The capture cross sections of the trap level dictate the probability of capture and release of the trapped electrons.

Our approach focused on calculating the laser energy in the form of photons traveling through the 6H SiC with uniformly distributed ionized trap levels with the probability of capture by the trap level dictated by its cross sections. Thus, the energy required to obtain a particular free carrier density (N) depending on the ionized trap density is tabulated in Table 6.1.

Energy (J)	Photon Energy (J)	N (cm^{-3})
$1x10^{-6}$	$3.73x10^{-19}$	$2.68x10^{12}$
$1x10^{-5}$	$3.73x10^{-19}$	$2.68x10^{13}$
$1x10^{-4}$	$3.73x10^{-19}$	$2.68x10^{14}$
$1x10^{-3}$	$3.73x10^{-19}$	$2.68x10^{15}$
$5x10^{-3}$	$3.73x10^{-19}$	$1.34x10^{16}$
$1x10^{-2}$	$3.73x10^{-19}$	$2.68x10^{16}$
$5x10^{-2}$	$3.73x10^{-19}$	$1.34x10^{17}$
$1x10^{-1}$	$3.73x10^{-19}$	$2.68x10^{17}$

Table 6.1. Number of photons corresponding to energy in joules

From Table 6.1, with 5mJ energy incident on the switch, $3x10^{16}$ photons are available to trigger the trapped electrons from the deep levels into the conduction band. The maximum trap density can be as high as $3x10^{17}/cm^3$ [10], limited by the solubility of

Vanadium in SiC. This density corresponds to 1.728×10^{16} total traps within UMC device dimensions. Assuming that one-half of the total traps are ionized, the energy requirement calculations indicate a value of 6mJ. Note that this calculation does not consider any of the losses in the switch. The ionized trap density for the SDDA material characterized earlier in Chapter 5 is $2 \times 10^{15}/cm^3$. Hence, the total number of ionized traps in 1.2 x 1.2 x 0.04 cm^3 PCSS volume corresponds to approximately 1×10^{14} trapped electrons. Thus, the energy required to trigger all the trapped electrons into the conduction band is about 5×10^{-4} J. The plots of the energy and carrier generation are given below in Figs. 6.4 and 6.5.

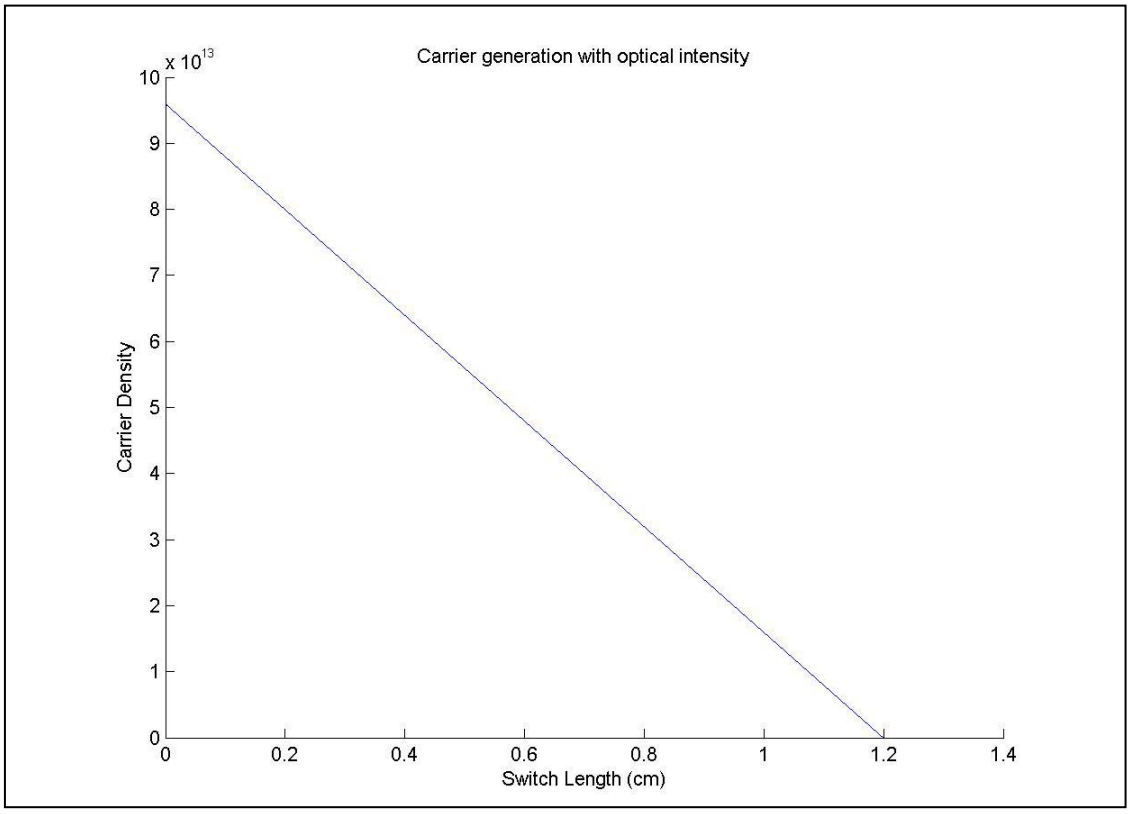


Figure 6.4. Carrier profile in the PCSS with optical intensity

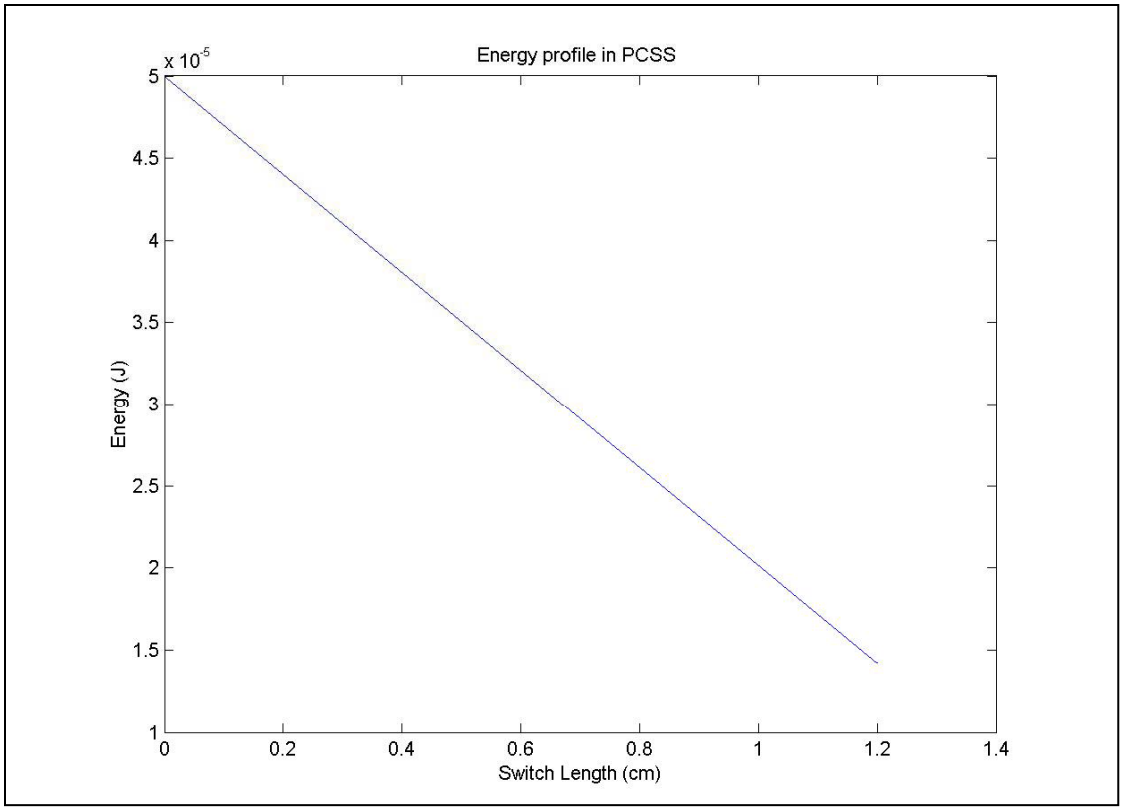


Figure 6.5. Energy profile across the switch

If the input energy is much higher than the total trap density, the remaining energy illuminating the switch is wasted or it just transmitted through the switch. Fig. 6.6 shows the 1mJ switch input on the same PCSS which results in the transmission of the laser energy. A comparison of this data with the actual switch experimental data is done in the next section.

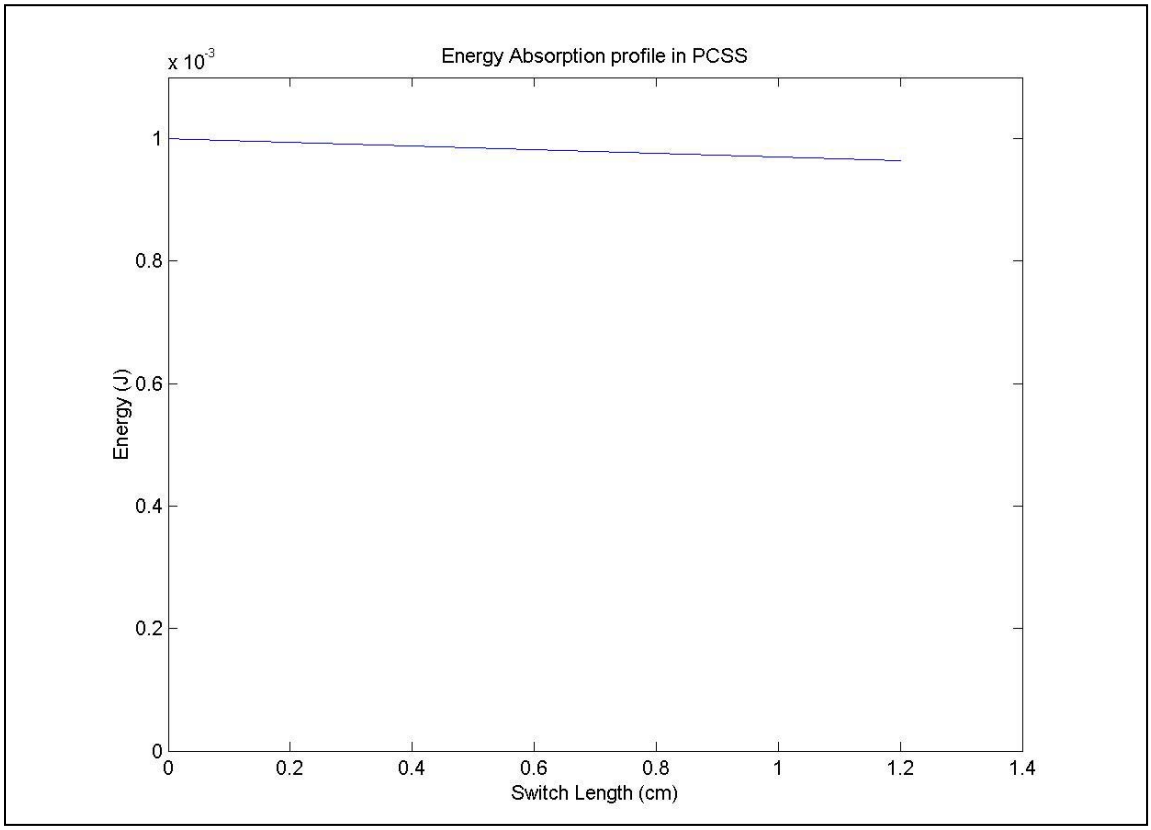


Figure 6.6. Energy profiled in PCSS at 1mJ energy

6.2. Transient Response Test Setup

To obtain the pulsed response of the PCSS, a test set up as described in Fig. 6.7 was prepared. The *test setup* consists of three main systems: the pulse power system, the photonic system, and the measurement system. Moreover, these systems simply provide a voltage pulse to the SiC switch; inject the SiC switch with photonic energy, which induces switch conduction; and record the conduction characteristics of the switch. These three systems combine in what is termed the *test bed*, the area where the SiC switch resides. The pulse power system and photonic system are triggered and synchronized by two linked pulse generators; however, the measurement system is triggered by the current pulse conducted through the SiC switch upon photonic-induced switch closure.

To elaborate, each system consists of several components. The first system described in the test setup is the pulse power system. Forming the pulse power system is a Glassman 0-10kV, 30mA regulated DC voltage supply that charges a 1.4nF capacitor. This capacitor is then dumped into a 14m long RG213/U coaxial transmission line via an optically triggered IGBT circuit. The IGBT is optically coupled to the first Stanford RG535 pulse generator for single shot triggering. Following a single shot execution, the voltage pulse formed from the IGBT circuit travels down the transmission line and arrives at the SiC switch residing in the test bed. This voltage pulse is met at the SiC switch by a 532nm laser pulse generated by the second system, the photonic system.

The second system in the test setup is the photonic system. This system is composed of a Continuum Surelite II Nd:Yag laser that is externally triggered, via the second Stanford RG535 pulse generator, to deliver a 5ns 532nm laser pulse into the SiC switch at the precise time that the voltage pulse arrives. This laser pulse induces electron carriers into the SiC switch, which causes the "closing effect", allowing conduction through the switch. For synchronization purposes, the first aforementioned pulse generator and second pulse generator are externally linked, using the second pulse generator as a reference for timing the voltage pulse. This second pulse generator is set to "single shot" mode thus producing one laser/voltage pulse into the SiC switch, resulting in one "switch closure." Upon this closure, the voltage across and current through the SiC switch are measured via the third system, the measurement system.

The third system in the test setup is the measurement system. This system consists of a "sandwiching-style" test bed, a Tektronix high voltage (HV) probe, a T&M Research Products shunt current probe, and a Tektronix Digital Phosphorous

Oscilloscope. The SiC switch is “sandwiched” or clamped between two electrodes that are bolted to top and bottom cylindrical plates. The cylindrical plates provide a base for which all probes and transmission lines are attached. The plates are separated by threaded fiberglass rods which, when rotated, vary the distance between the plates creating a clamping effect with the electrodes. The HV probe is placed across the cylindrical plates, putting the HV probe in parallel with the SiC switch. The shunt current probe threads into one of the two electrodes and is bolted to the bottom cylindrical plate. This electrode orientation allows the current probe to penetrate into the test bed placing the probe in series with the SiC switch clamping the switch against the electrode bolted to the top cylindrical plate. Both probes are coupled to the oscilloscope. The laser pulse is directed into the center of the *test bed* aimed at the face of the SiC switch that clamped between the top and bottom electrode. The oscilloscope is set to single shot trigger off of a rise in current through the SiC switch detected by the shunt current probe.

The PSICE model of the pulse generating circuit is also shown in Fig. 6.7. It is a CLC circuit with the transmission line forming the second capacitor. The length of the transmission line can be changed to obtain the required impedance (by putting a few in parallel) as well as the delay time. The delay time is approximately 1.5ns per foot. The circuit operation is already explained in the above paragraph. The open load voltage pulse from the test setup is plotted in Fig. 6.8 along with the actual test set up in Fig. 6.9.

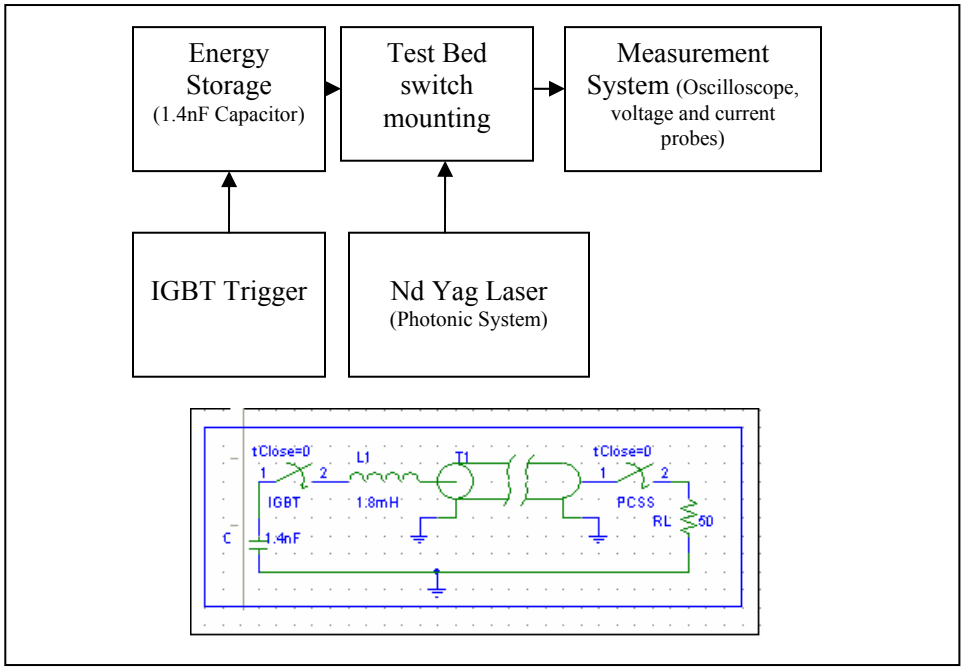


Figure 6.7. PCSS pulse charging setup schematic and PSPICE model

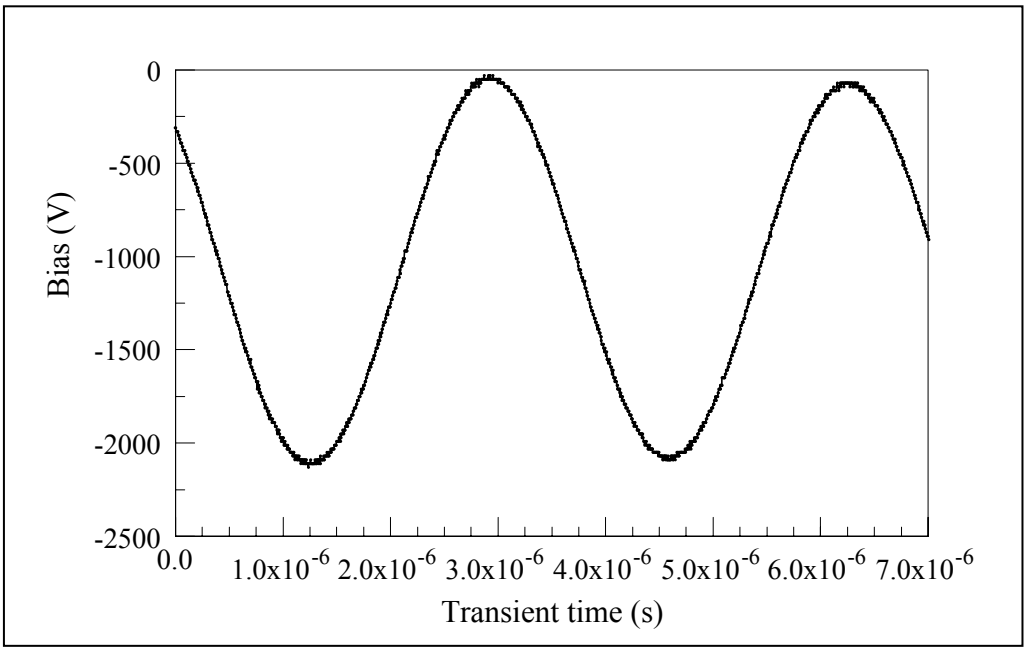


Figure 6.8. Open load voltage pulse from the test setup

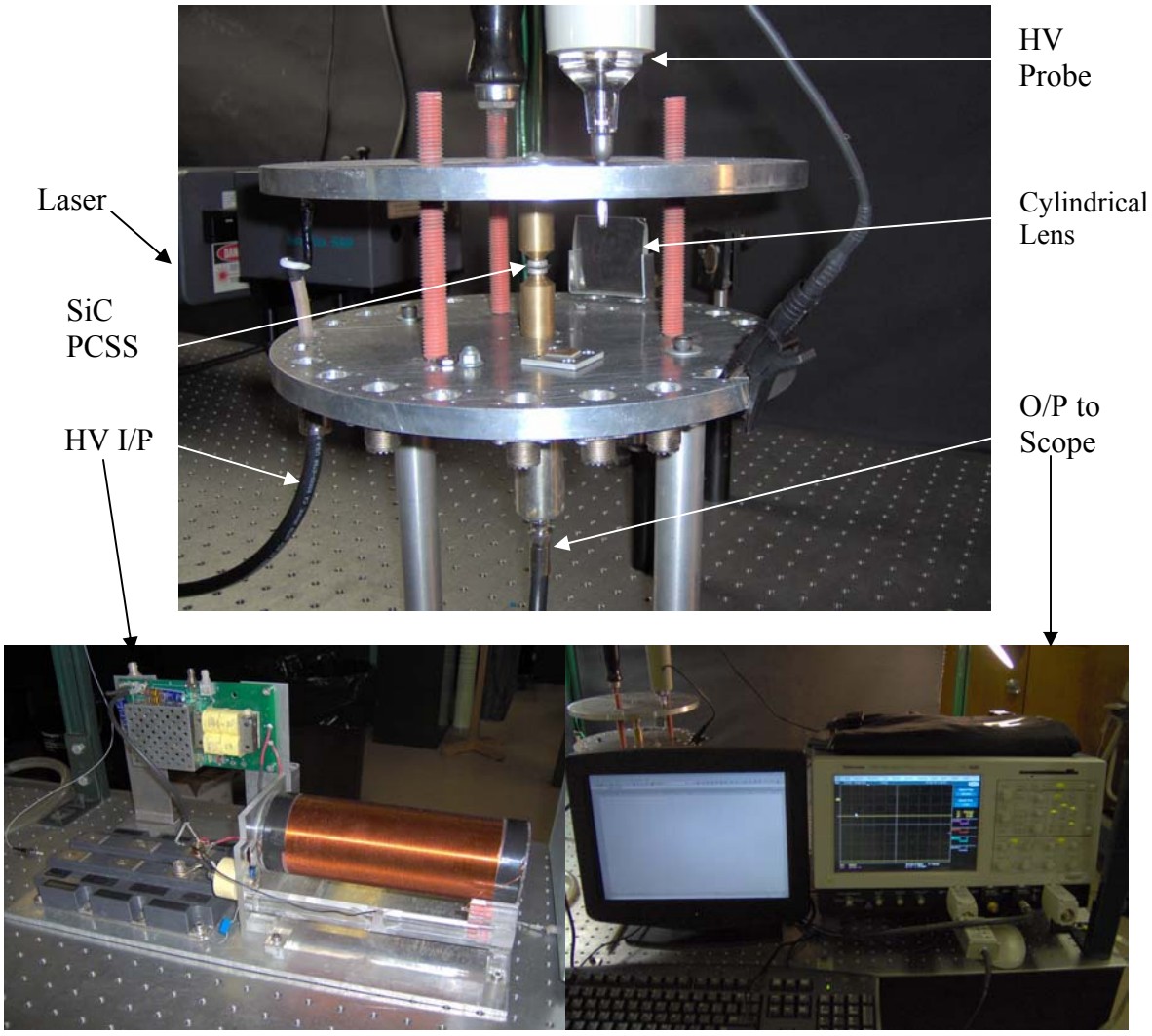


Figure 6.9. UMC Experimental setup

6.3. Low Voltage Switching

After the test pulse, two different tests were performed on the switch design, namely

1. Low voltage (up to 2-3kV) pulse charging with illumination to analyze switch performance along with calibration of the simulation code for high voltage performance predictions.

2. High voltage pulse charging to obtain the breakdown voltage of the switch (explained in the next chapter).

6.3.1. Low voltage Switch illumination data (experiments with simulations)

In the test, a 1 cm diameter laser beam was used to illuminate the center of the switch. The 532 nm 10 ns laser was applied at a charging state of a 340V, 1μs voltage pulse (Fig. 6.10). A Peak photo current of 6A was obtained through a load resistance of 53Ω (ON state switch resistance of ~3 Ω). Note, that this first data set was obtained from LLNL, where most of the switches were manufactured.

To calibrate the simulation code for further analysis of the PCSS, two dimensional (2D) and three dimensional (3D) switches were modeled using the Devedit code of the Silvaco software which are then charged to 400V and illuminated with a laser pulse in Atlas. The mathematical models discussed earlier in Chapter 4 were solved to obtain the photo response of the switch. The code needed some input values such as the optical absorption depth and the like which were provided from the literature as discussed below.

For laser illumination, the optical absorption coefficient from previous calculations was used, and an optical efficiency of 100% was assumed Also, since material in intimate contact with SiC is expected to affect the injection behaviour significantly, only Nickel Silicide is used as contact material for the simulations. The actual contact has three layers of metals, as discussed earlier.

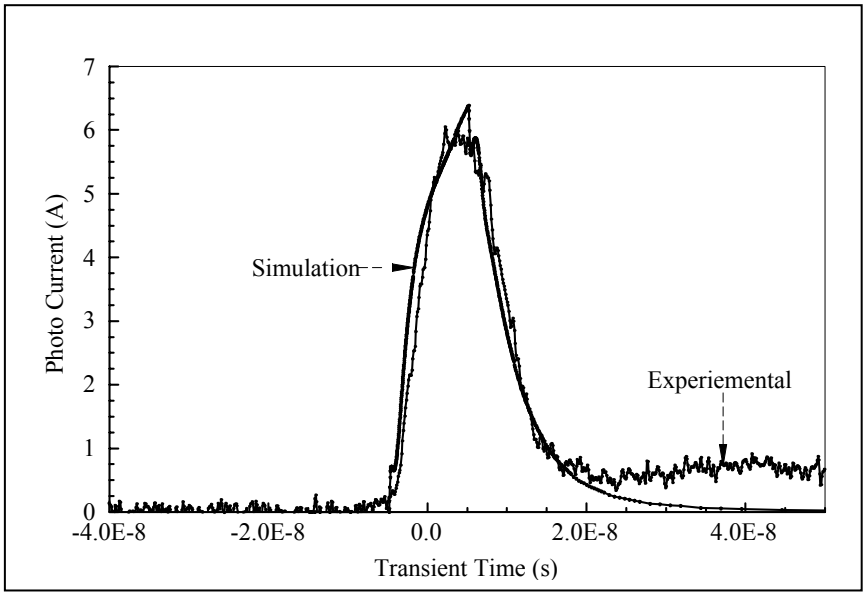


Figure 6.10. Simulation and experimental photocurrent characteristics at low bias

For simulations both SDDA and DDSA type materials were considered even though the material has been earlier verified as SDDA type. The two trap concentrations were assumed to be the same $2x10^{16}/cm^3$ value with n type doping for SDDA and p type for DDSA at a value of $2x10^{15}/cm^3$. Fig. 6.11 shows the response of the PCSS with different material types. The switch opening for the DDSA material was observed to be faster than the SDDA material. This was expected since a deep donor level is an efficient electron trap than the SDDA type. Also note that the current magnitude for the SDDA case is much higher than that for DDSA due to the higher ionization of the deep acceptor level than the deep donor level for the DDSA type.

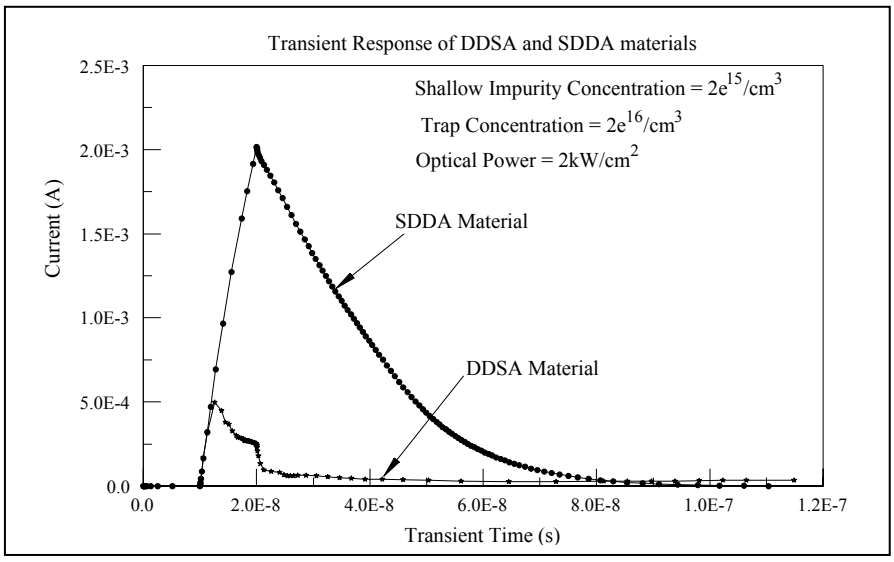


Figure 6.11. Simulation and experimental photocurrent characteristics at low bias

Further simulations with the SDDA type resulted in good agreement with the optical power absorbed at a 532 nm wavelength, which was around ~7kW/cm^2, between the experimental and simulated illumination results (Fig.6.10). it is suspected that a small deep donor level exists in the material, causing a long tail in the experimental photo current characteristic, and this is discussed in the next section. A good match at low power validated the model parameters used in this study and also provided useful insights into the workings of the PCSS during switching, which was the basis for new design changes for high power operations. A comparison with experimental values also indicated that only 5-7% of the optical energy was actually absorbed in the device. This could be attributed primarily to reflections, as well as to low optical and quantum efficiencies and the like [40].

6.3.2. Experimental measurements at UMC

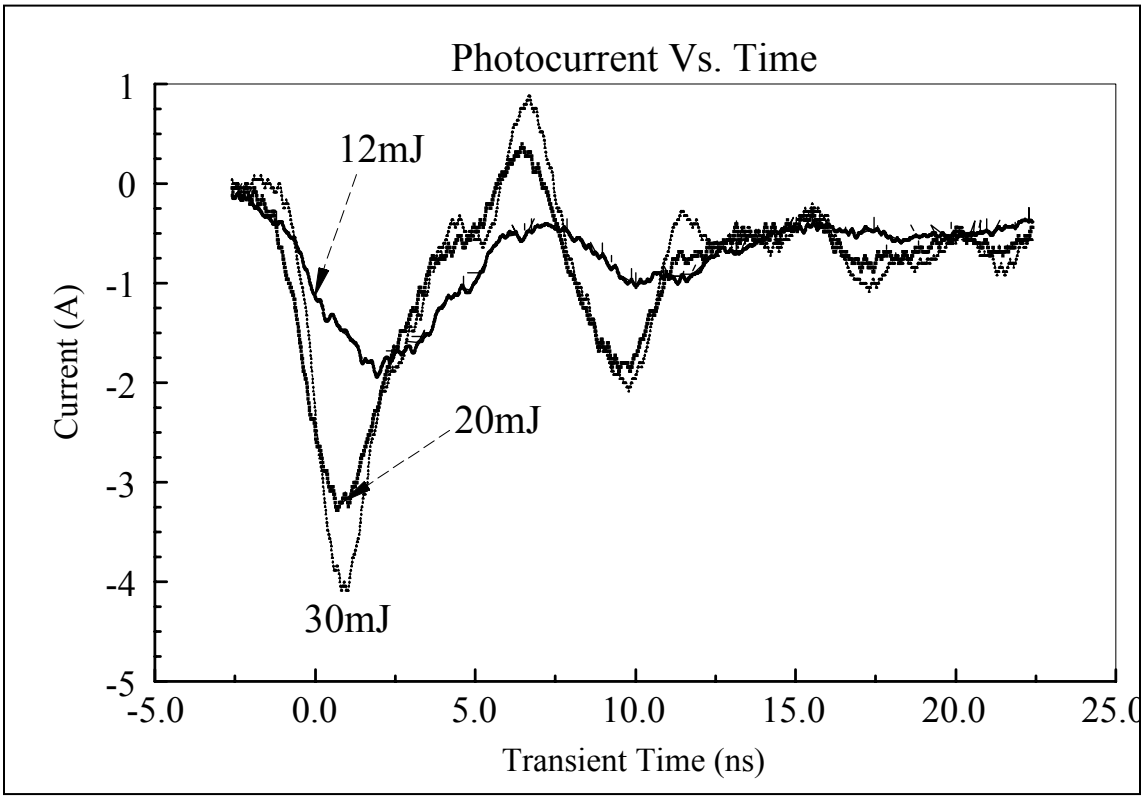


Figure 6.12. Transient response of PCSS with different laser energy
First set of experiments: Voltage ~340V, I_{MAX} ~ 4.5 A

In the test an 8 mm diameter laser beam was used to illuminate the center of the switch. The 532 nm 8 ns laser was applied at a charging state of a 340V, 1μs voltage pulse (Fig. 6.12). A peak photo current of 4A was obtained at an energy input of 30mJ. This energy requirement was much higher than the LLNL testing with only 5mJ of energy. This suggested improper laser beam focusing onto the switch surface and is a part of proposed future research work.

After a few hundred pulses on the PCSS, the high K material (gel) around the switch was observed to be contaminated and was removed for efficient energy delivery to the switch. It indeed increased the photo current with a lower switch resistance obtained

(Fig. 6.13). The high K dielectric was not expected to affect the laser energy delivery to the switch edge and hence the laboratory conditions might be the reason for such an adverse effect on the switch response. With the gel removed from the switch, the laser energy absorption in the PCSS improved significantly. The switch closed with an ON state resistance of a few ohms (Fig. 6.14). The switch voltage and current behavior at 5mJ of energy at 350V is plotted in Fig. 6.15 (obtained from LLNL).

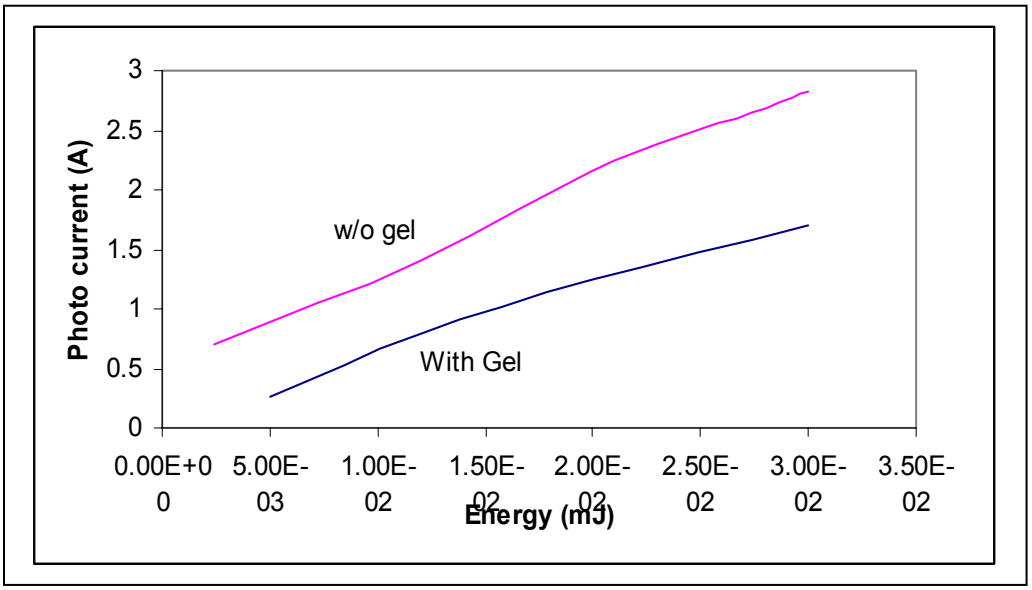


Figure 6.13. PCSS photocurrent with and without high K dielectric surrounding the switch

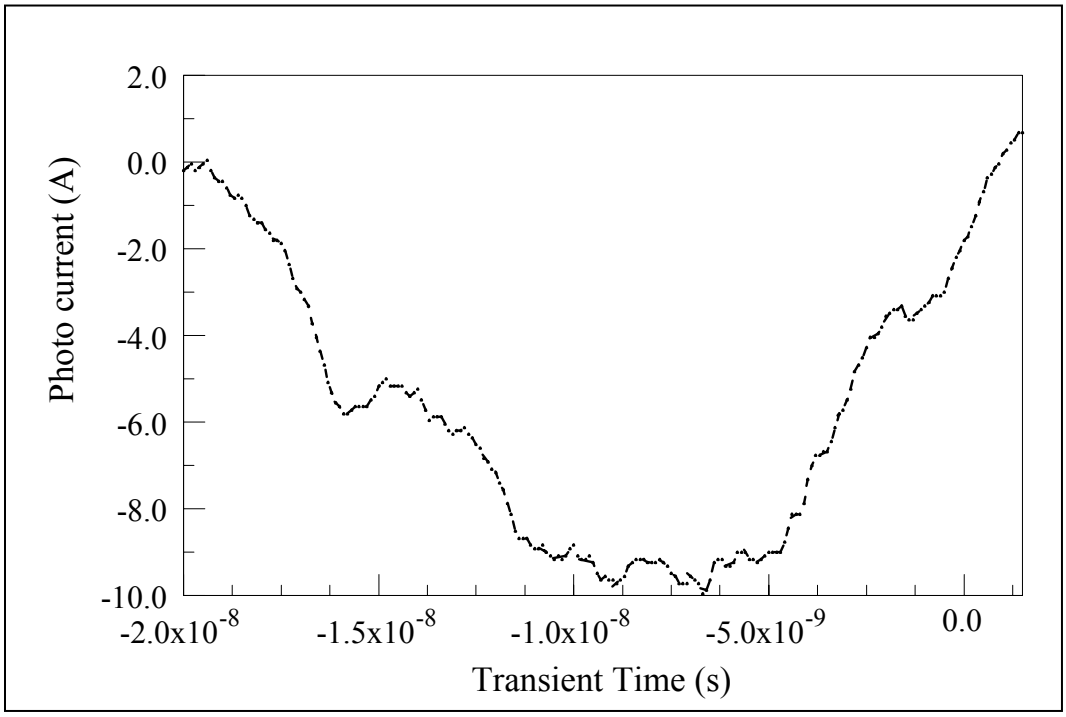


Figure 6.14. Maximum switch current at 340 V

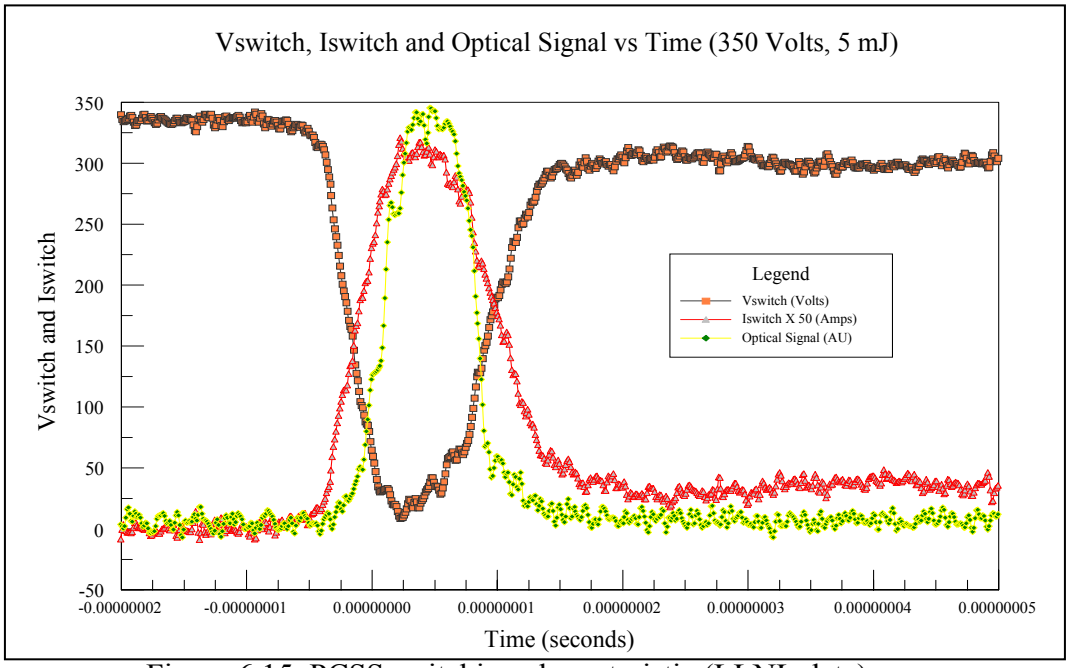


Figure 6.15. PCSS switching characteristic (LLNL data)

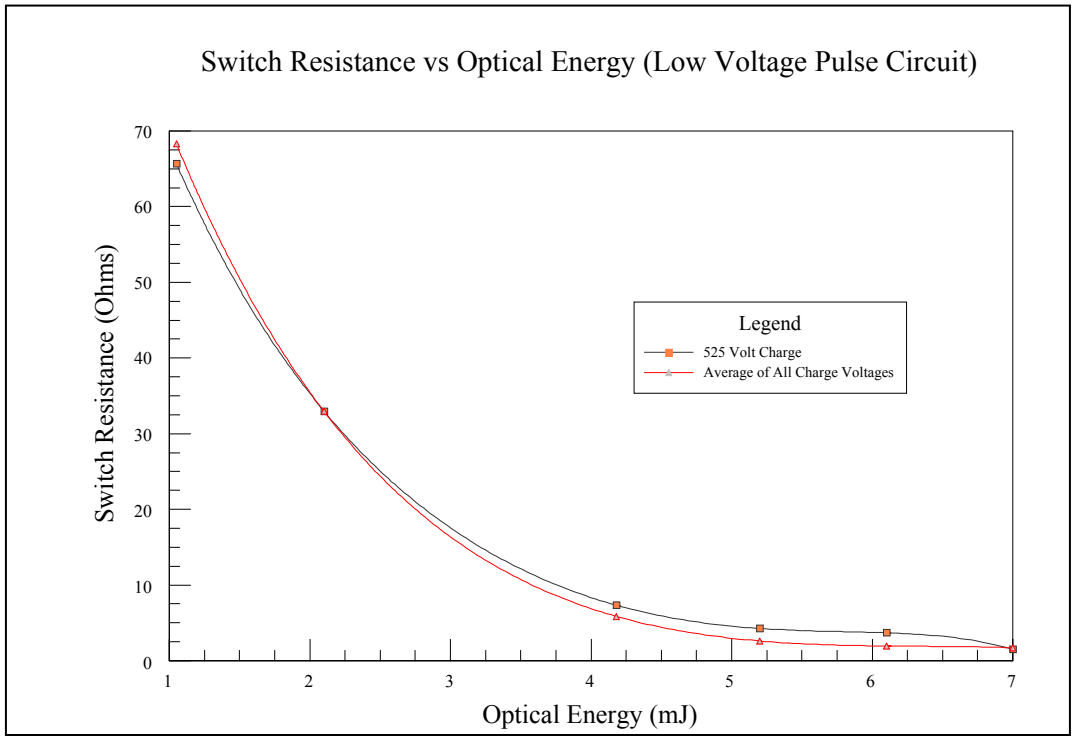


Figure 6.16. Comparison of on state switch resistance with laser energy (LLNL data)

The switch resistance change with the optical energy input was also studied (Fig. 6.16). Theoretical calculations suggest only 0.5 mJ of energy is required to activate all the trapped electrons into the conduction band (only 10% is utilized) (Fig. 6.17). The reflection, quantum efficiency and the like are expected to be reason for this loss.

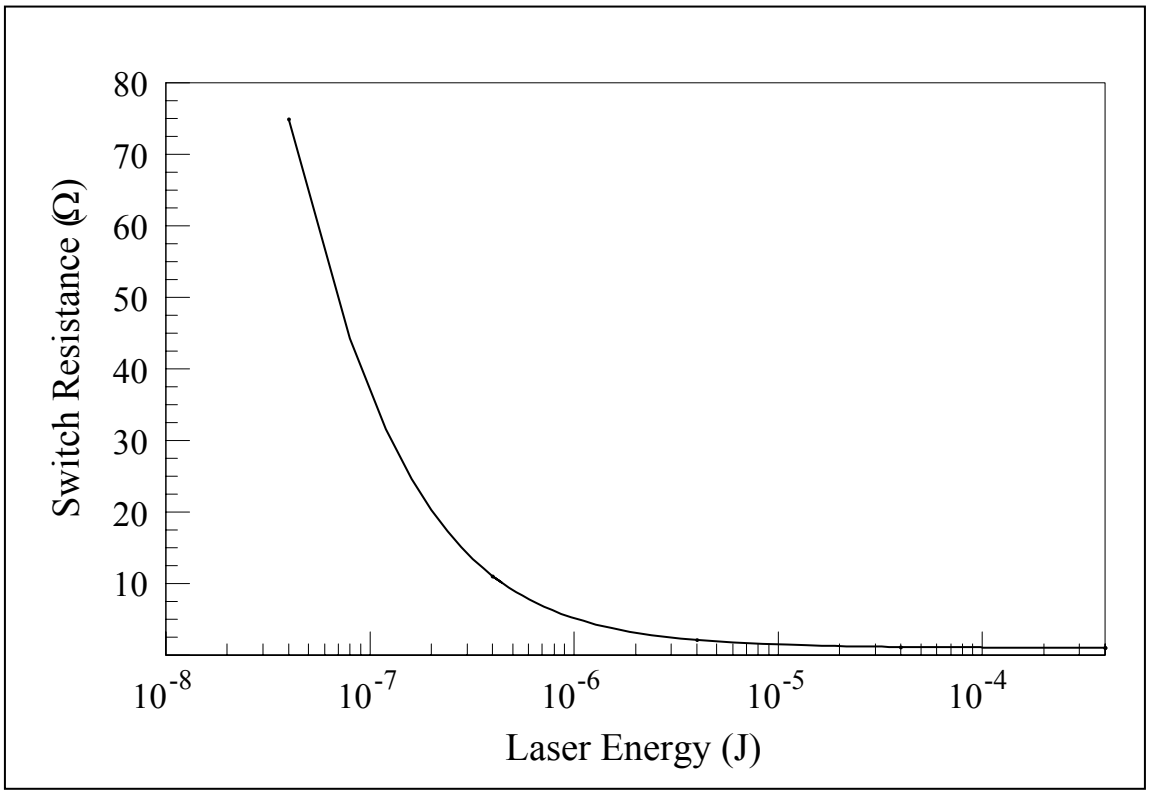


Figure 6.17. UMC Simulation data of switch resistance with illumination energy

The nature of some of the different extrinsic levels being excited at different wavelengths, namely 1064 and 532 nm has been presented earlier in [41]. To understand the behavior of the PCSS at both these wavelengths, both the levels, deep acceptor and deep donor with $2x10^{16}/cm^3$ and $2x10^{15}/cm^3$ concentration were added to the code. Note that this material cannot be called a deep donor deep acceptor since both the levels are not present at the same location inside the material.

Fig. 6.18 shows the photo response with only the SDDA type (with a 1064 nm wavelength) and the combination of DD and DA levels (532nm wavelength). As can be seen from the plot, the SDDA level recombines faster and hence is expected to have a few nano second lifetime. The trap cross section used earlier [24] matches well with the experimental data. Now, for the deep donor level, no such data was available; hence different cross sections were tried until a better fit was obtained between the experimental

and simulation plots. The best fit was obtained for $\sigma_N = 1x10^{-16}$ cm^2 and $\sigma_P = 2x10^{-18}$ cm^2 (Fig. 6.19). This cross section is close to that of the EL 2 level in GaAs [21]. Hence, the performance and behavior of the deep donor vanadium level in SiC can be similar to that of the EL2 level, which needs further study and is a part of future investigation.

The rise time at a 532 nm wavelength was observed to be better than with a 1064 nm wavelength (Fig. 6.18). This can be due to the higher energy transfer into the PCSS at 532 nm (2.33eV) than at 1064 (1.17eV) nm wavelength.

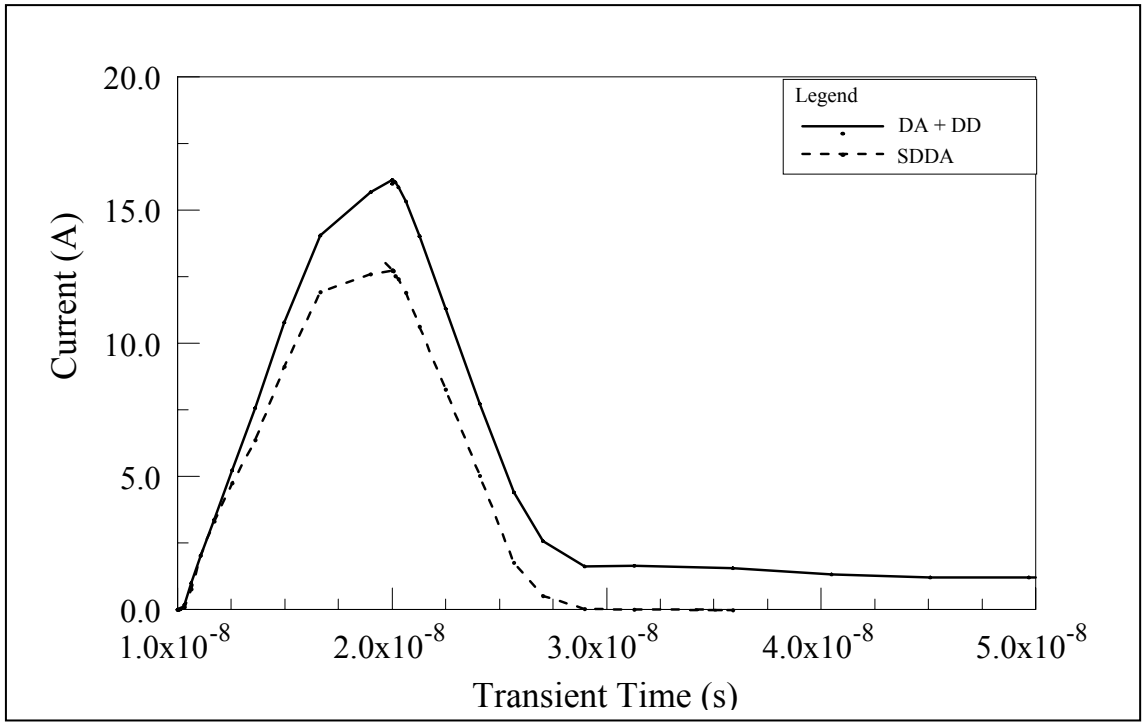


Figure 6.18. Comparison of DD and DA trap level on photo current characteristics versus time

To understand the extended conduction in SiC, different conditions were considered and are discussed in this section. To ensure which deep trap level is responsible for the extended conduction, each one was added to the simulation individually. The long tail in the photo current was observed only for the case of deep

donor (V^{4+}/V^{5+}) present in the material. To verify above arguments, both the vanadium trap levels were added to the simulation and the transient response was obtained with 1064 nm and 532 nm wavelengths (Fig. 6.18). As can be from Fig. 6.18, the long tail in the photocurrent was observed only with the activation of deep donor level.

A few more simulations were carried out with the objective of finding out the relation between the compensation ratio and the tail in the photocurrent, mainly its magnitude. To understand this, a detailed analysis was carried out with two different compensation ratios 2 (m1) and 10 (m2) at a 532 nm wavelength. The material Fermi level location and polarity were calculated using the same equations as in chapter 5. The PCSS was carefully observed for the electron and hole concentrations, potential distribution, electric field profiles and trap occupancies before, during and a few hundred nanoseconds after the laser illumination. For both materials, since m was greater than 1.06 (See Tables 5.1 and 5.2), the material polarity was N. During illumination, the electrons from the deep donor level were released into the conduction band and thus the free electron concentration increased by many (~10) orders of magnitude. Since the laser energy was greater than the half of the bandgap (2.33 eV), a large number of holes were also created in the valence band by two photon absorption (TPA) [42]. By this process there was a drastic increase in the free hole concentration as well. A few hundred nanoseconds after the end of the laser pulse, the free carrier densities were analyzed again. For the m1 case, the hole concentration was observed to be greater than the electron concentration making the material p-type. For m2 the electron and hole concentrations were of the same order of magnitude (~10^6). As the compensation ratio $m = \frac{N_V}{N_A - N_D}$ decreases, the Fermi level moves downwards. Due to the downward shift,

the hole concentration was expected to increase. The lower the compensation ratio is (trap concentration is approximately equal to N_v divided by the N_A acceptor concentration), the higher the impact of the downward shift of the Fermi level. Thus, a new equilibrium is reached after the end of illumination, which is much more significant for the m1 case than for m2. Figure 6.19 shows the transient response of the two cases, where persistent conduction was observed only for m1. The switch voltage recovers in around 200 μs. This behavior is similar to the Lock on effect in SI GaAs, where the deep donor EL2 plays a significant role [6]. Even though the reasons for the two materials (GaAs and SiC) are different, the effect is similar.

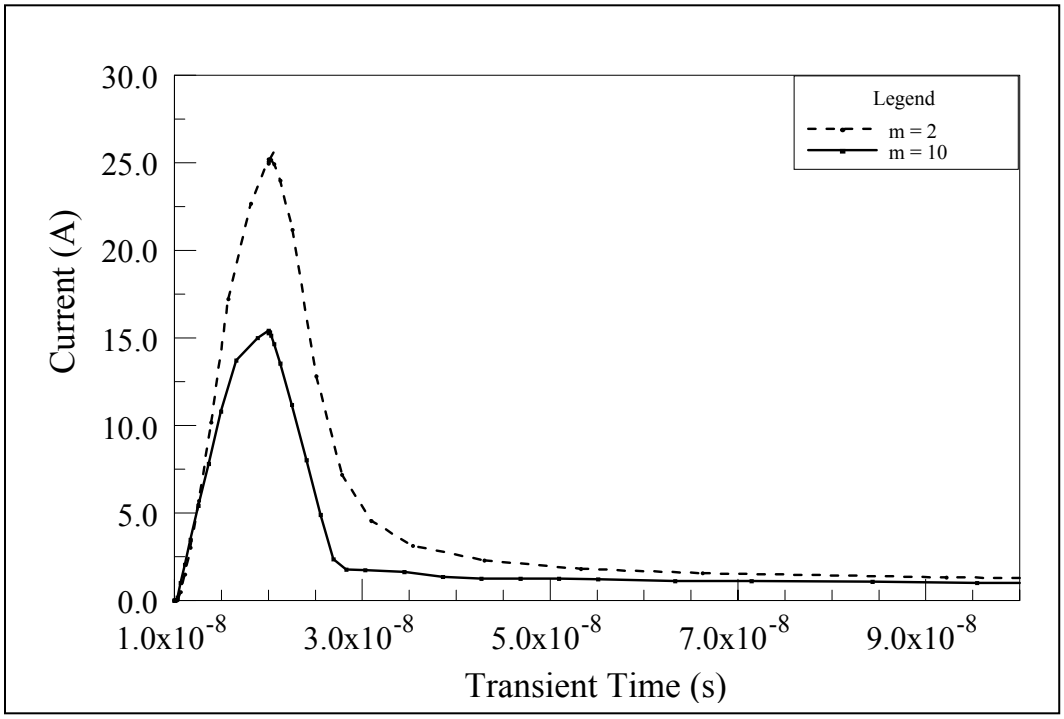


Figure 6.19. Change in photo current with different compensation ratios

The trap cross section was also varied to understand its effect on the tail in the photo current (Fig. 6.20). The best match with the earlier data could be obtained only in the case of a trap cross section $1x10^{-16}$ cm^2. The Fermi level affected by the occupancy associated with a particular trap cross section is expected to be the reason for this photo current tail.

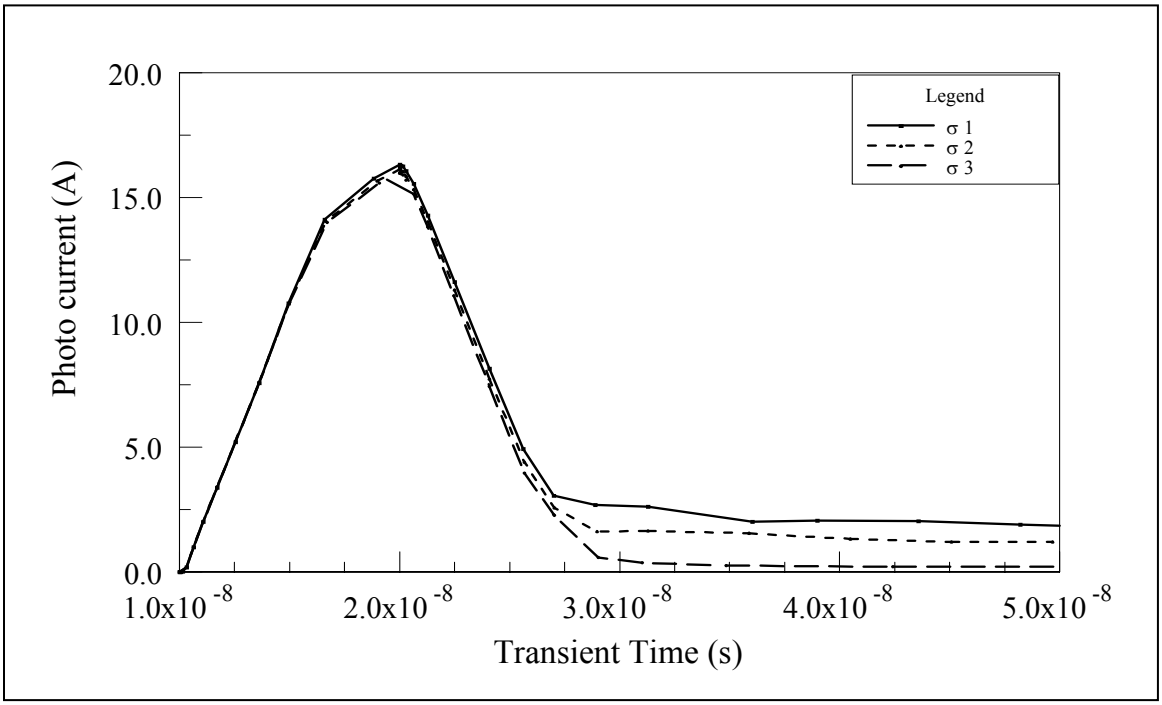


Figure 6.20. Matching of the photocurrent characteristics for trap cross section σ_1 = $1x10^{-15}$, σ_2 = $1x10^{-16}$, and σ_3 = $1x10^{-17}$

Chapter 7

High Voltage Behavior

The material characteristics and the early breakdown mechanisms of a compact SiC PCSS at low fields are analyzed in this chapter. The mechanisms for early breakdown are identified and then design criteria for high bias operation are proposed. A switch design for high field operation is analyzed and its characteristics studied,

7.1. High voltage Switch performance

With the device material type verified for simulations earlier, breakdown analysis and high power design changes were also studied. The initial DC tests of the switch at Lawrence Livermore indicated early breakdown around ~ 18 kV. Fig. 7.1 shows the simulated I-V characteristic at high applied voltage. The electric field, trap occupancy were closely observed as the bias increased which shows a breakdown at 24 KV. The experimental breakdown at ~18 kV has been attributed to a lateral mismatch in the contact layer (Fig 7.2). While trap occupancy was limited to the bulk region, high field regions were observed close to the anode, increasing the impact ionization rate as shown in Fig. 7.3, which ultimately lead to breakdown. The high field region formation close to the anode was further studied to understand the exact reason for such a field formation and is discussed below.

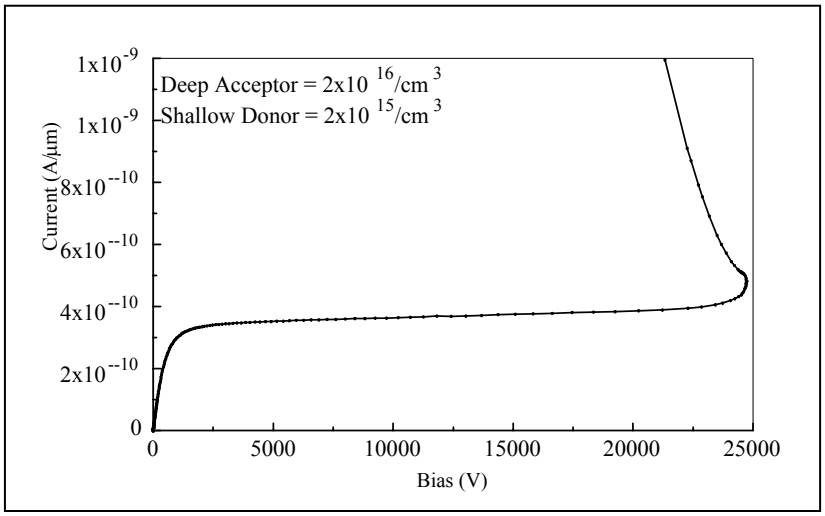


Figure 7.1. Simulated IV till breakdown

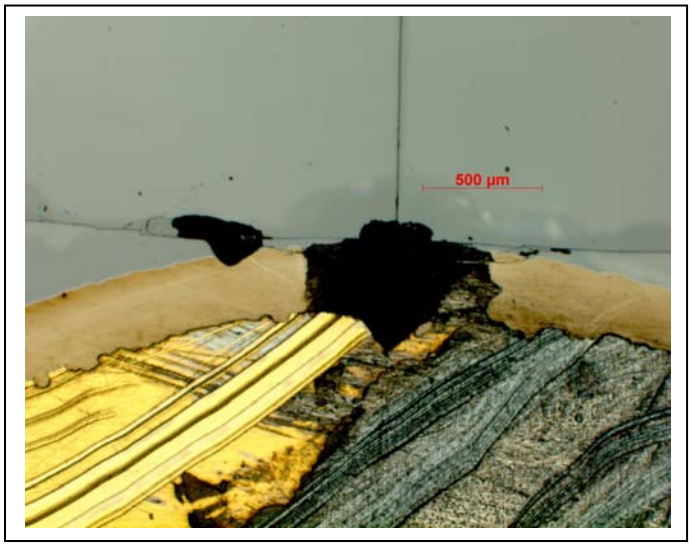


Figure 7.2. Lateral mismatch between the contact layers causing damage to the SiC

The electric field distribution in a PCSS greatly influences the device operation. Hence, the field profile in the bulk is a good measure of the switch performance. The

material hold-off characteristic is influenced by the semi-insulating conductivity of the bulk rather than space-charge depletion, as is the case with a *pn* junction [9]. For the SiC PCSS under consideration, the bulk electric field decreases from the anode to the cathode as in Eqn (7.2), which is based on the solution to Poisson's Eqn (7.1), incorporating trap densities [43].

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_0 \varepsilon_s}[n(x) + N_{di}^{-}(x) - N_{ai}^{+}(x)] \tag{7.1}$$

where n(x) = Electron concentration, N_{di}^{+} = Ionized donor concentration, N_{ai}^{-} = Ionized compensating acceptor concentration and $N_{d,si,eff} = N_d$. Solution for E field gives,

$$E_x(x) = \frac{qN_{d,si,eff}}{\varepsilon}(l - x) \tag{7.2}$$

where l is the length of the switch and x is the distance variable.

The high fields contribute to impact ionization, thus causing a large number of secondary electrons to reach the anode without being collected. The electric fields thus terminate at the 'virtual cathode' very near the anode. The enhanced field results in contact degradation and premature breakdown at 18 kV, as reported earlier [44]. The breakdown mechanism is similar to the gate rupture or burnout of MOSFETs as a result of charge accumulation near the gate, following a single charge particle incident at this region [45].

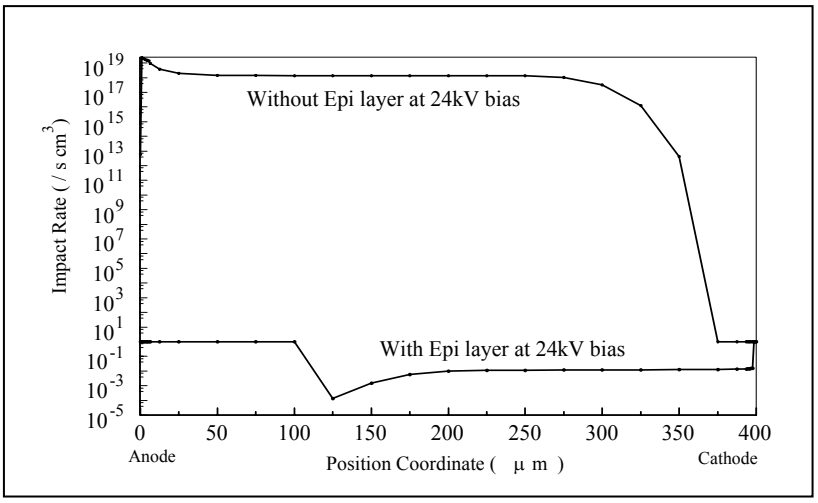


Figure 7.3. Impact ionization profile with and without epi layer at cathode at 24kV

7.2. Improvement in the Hold off Voltage

The switch hold-off voltage can be improved by inhibiting the high field regions being formed at the anode. In other words quenching the impact ionization was needed to improve the switch performance at higher voltages. For a p-n junction diode, the electric field lines in the depletion region are directed against the externally applied electric field. Implementation of such a depletion layer like profile at an electrode can inhibit the carrier injection until a higher bias and also move the location of the high field region into the bulk semiconductor. Details of improving the performance of SDDA type 6H SiC to higher voltages with a similar mechanism were examined, through the application of an epi layer at one of the electrodes or both. Use of an epi layer as well as the scalability of the epi layer thickness was analyzed. This type of retarding field was discussed before by Naz et al but was limited to the DDSA type GaAs [22].

Thus mechanisms that would lower the fields in the bulk material or limit the number of primary electrons to reach the anode could result in a switch operation at higher bias. Such a mechanism for high field operations has been suggested for DDSA

type GaAs [22]. For SiC PCSS, however, simulations suggest that a p^+ region next to the cathode in the SDDA material will also allow higher bias operation, much beyond 18 kV (Fig. 7.4). The physical mechanism for the high bias operations in the SDDA SiC PCSS is different from that of a DDSA GaAs material. In case of the SiC PCSS, the interactions of the p-region and n-type bulk results in electron diffusion towards the p^+ region. The presence of the positively charged ionized donor N_{di}^+ in the bulk opposes the anode field, which results in a substantial lowering of the bulk field, as shown in Fig. 7.5. Impact ionization therefore is reduced substantially and as a result it is possible to increase the bias across the device without premature breakdown (Fig. 7.3). Note that since, with the help of p^+ layer, the electric field inside the switch is lowered, the switch can be more effectively used as a linear switch (all the non-linear effects minimized) avoiding surface flashover, filamentary conduction, premature breakdown etc [46].

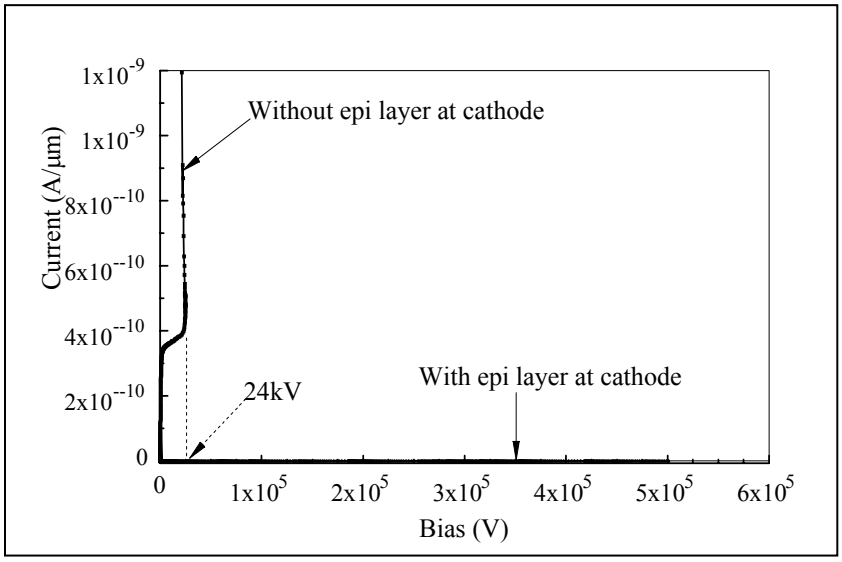


Figure 7.4. Improvement in the hold off voltage due to p^+ layer at cathode

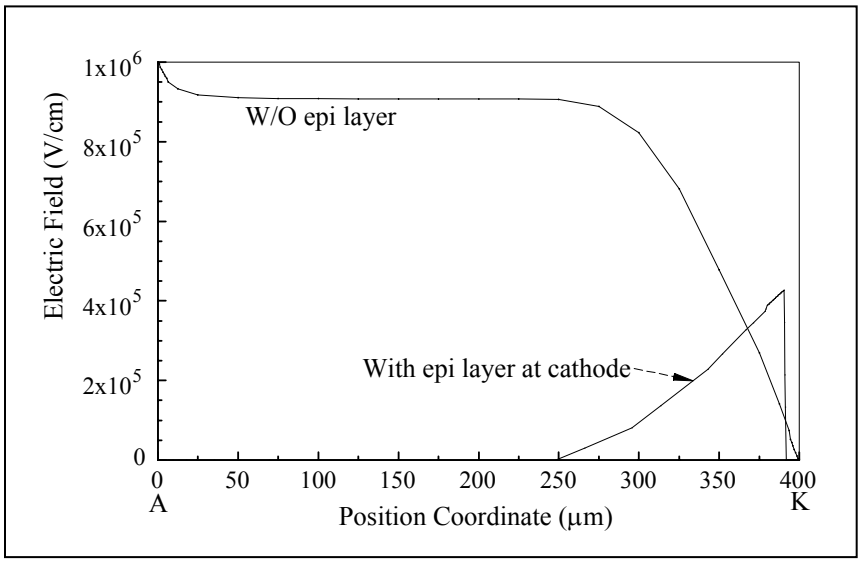


Figure 7.5. Change in the electric field profile from anode to cathode with p^+ layer

The minimum thickness of the p^+ region next to the cathode for the SiC PCSS is also much less than the n^+ region for the DDSA GaAs switch. For a DDSA GaAs PCSS, it was reported that a minimum thickness of 20μm n^+ layer at cathode is required to achieve improvement in the hold off voltage [22].This is primarily due to the fact that the material must be at least a diffusion length in thickness (L_n = 10-15 μm), to be effective [47]. For SiC the diffusion lengths are much smaller [48]. Simulations show that an improvement in the hold off voltage is possible for a few micron thick p^+ epi layers.

7.3. High Voltage Transient Response with illumination (Experimental)

A single PCSS device was tested to electrical failure of the 6H SiC substrate at LLNL. The charge circuit was modified to produce a 3 μs risetime. The 1064 nm, 9mJ, optical pulse was applied after a 5 μs flat top pulse submerged in a transparent liquid dielectric to prevent tracking around the edge of the device. The PCSS failed after

conduction at a pulsed biased voltage of 11kV. This voltage represents an average field of 0.274MV/cm in the SiC substrate [41]. Failure occurred through the bulk of the substrate directly under the edge of the device metallization, the location of greatest electric field enhancement.

7.4. Illumination results for p^+ at cathode for SiC at 30kV

Improved PCSSs design was charged to 30kV and illuminated with a corresponding laser wavelength (532 nm for SiC) in the middle of the voltage pulse. The switch closed following the illumination pulse as shown in Fig. 7.6. The photo current produced an initial kink as shown in Fig. 7.6 in about 1ps. The time required for the electric field to disintegrate is higher is SiC due to the depletion layer. Thus following illumination pulse, the time required for the electric field to disintegrate is higher.

This can be explained with the help of the junction properties for p^+-SI SiC. For SiC the p^+ layer at the cathode forms a reversed biased junction with depletion region concentrated in the SI SiC side. When illuminated, the high field at the electrode sweeps out carriers initially (in Pico seconds see Fig. 7.6). As the time progresses, the electric field profile changes with high field region formed at the anode (Fig. 7.7). (The reason for this is already explained earlier in this chapter). From Fig. 7.7, the magnitude of the electric field at the cathode in the initial stages of the photo current is much higher than the later (1ns) cases giving higher velocity to the electrons. Once the electric field stabilizes, this photo current smoothens out. Note that the persistent conduction (recombination time ~ 90ns with p^+ layer at cathode) is due mainly to the recovery of the electric field at the cathode after the end of laser pulse.

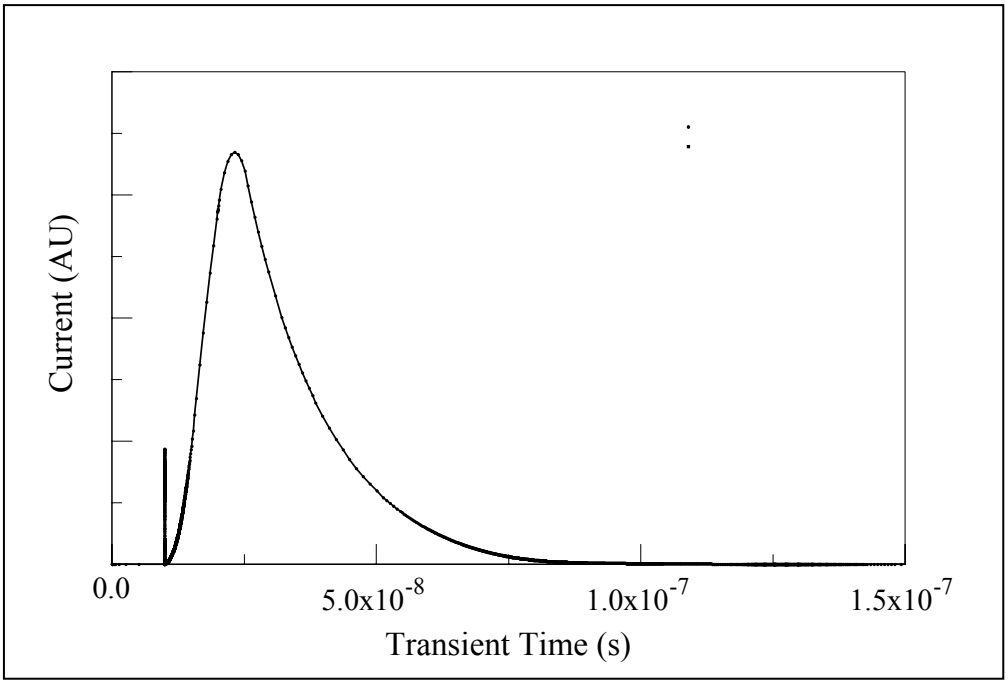


Figure 7.6. SiC (with p^+ layer at K) photo current response

7.5. Replacing 7.3 with forward biased junction p^+ at anode for SiC

When the junction profiles were changed to forward biased junctions (p^+ at Anode) for SiC (Fig. 7.8), SiC PCSS showed delays in the switch opening mainly due to the reversed biased junction at the cathode. Note that the initial kink is not observed for the forward biased junction case (Fig. 7.7).

The new improved PCSS design was then simulated with illumination to observe the effect of p^+ layer on the breakdown voltage at higher bias. The switch can sustain bias as high as ~36kV before breakdown due to avalanche. As the illumination pulse dies, as mentioned earlier the electric field profile changes back to the initial (without illumination). But for a bias of 36kV and above, the electric field redistribution was

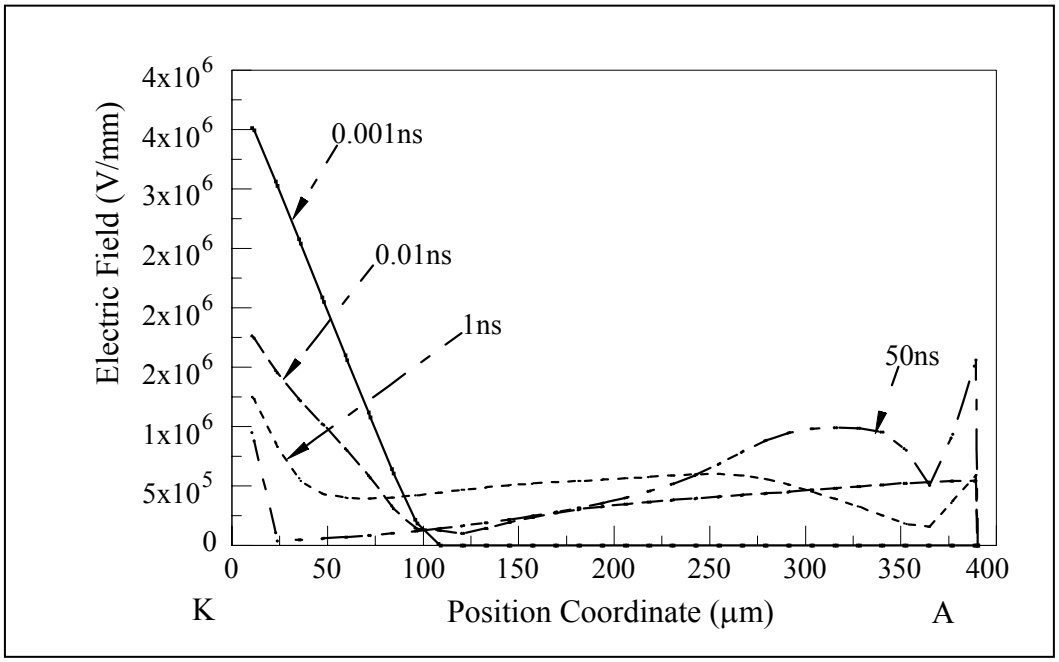


Figure 7.7. Electric field profile between the electrodes with laser illumination

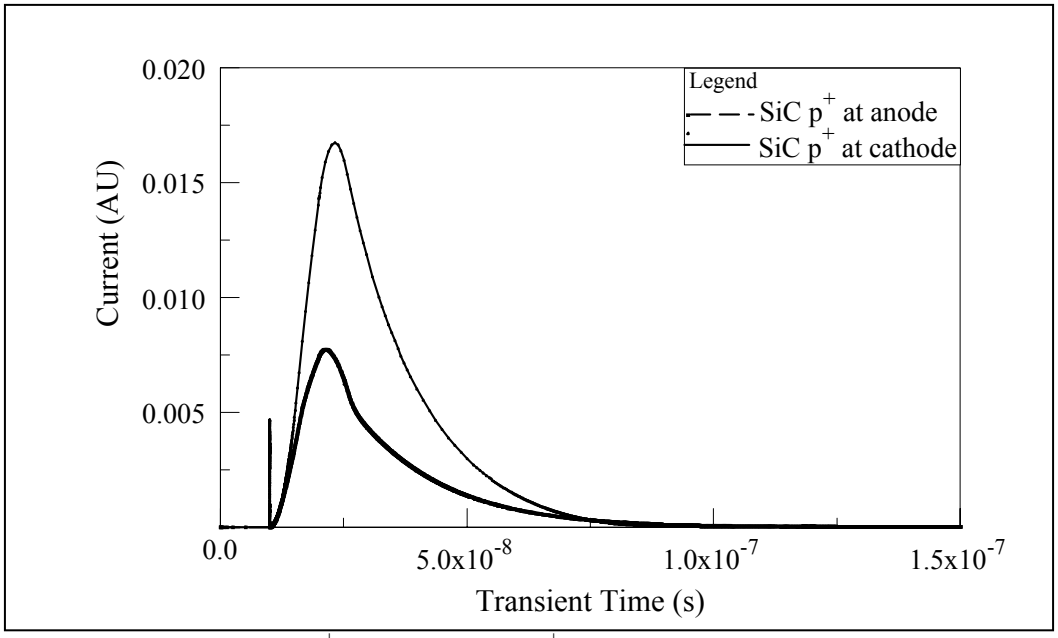


Figure 7.8. SiC with p^+ layer at K and p^+ layer at anode photo current response comparison

observed different than initial switch going into avalanche at the anode and did not reopen until few milli seconds (Fig. 7.9). Thus the p^+ layer effectiveness is expected to be limited to 875kV/cm an improvement of 4 times than the initial design with laser illumination. By increasing the switch length (distance between the contacts) better hold-off is expected for a SiC switch and is a part of future research work.

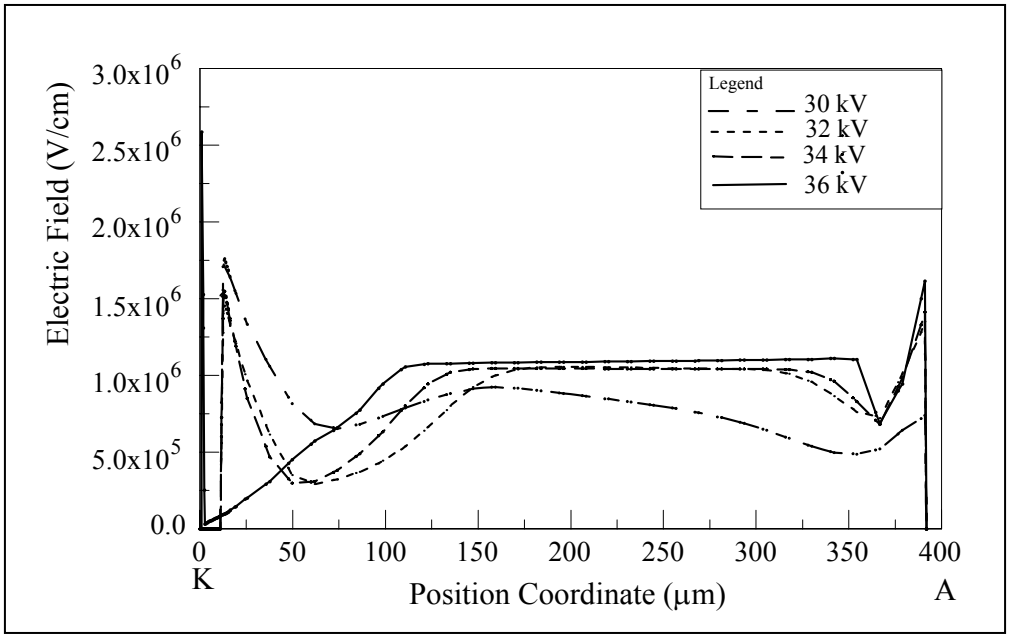


Figure 7.9. Electric Field profile in the PCSS (improved design) at increased bias with illumination

Chapter 8

Summary of work

Semi-insulating, compensated, SiC has been investigated as the working material in a linear, extrinsic photoconductive switch with a new geometry. Two different compensation mechanisms have been analyzed to determine the material characteristics, namely shallow donor deep acceptor with vanadium deep acceptors and nitrogen shallow donors and deep donor shallow acceptors with vanadium deep donors and boron shallow acceptors in SI SiC. The characteristics of a 6H-SiC SDDA PCSS are studied in order to present design changes for such high field applications as in circuits for generating ultra wideband high power microwaves, pulse generation and the like.

The geometry and package as well as the underlying physics have been analyzed for high power operation in the linear mode. Analysis show that the use of a high permittivity material at the triple point helps in minimizing the field enhancement which was the main cause of premature breakdown.

The DC I-V characteristics of PCSS were used to calibrate the simulations and one of the material parameters, such as compensation ratio was adjusted to determine the material composition. The matching of experimental and Simulation IV characteristics ensured proper material identification. Two types of compensation structures were investigated and the role of traps in the compensated material correlated with experimental results.

Preliminary experiments were conducted to obtain the breakdown strength of the PCSS in the UMC geometry. High field region formation at the anode as well as the mismatch in the contact layers were the underlying reasons for the early switch breakdown. Reduction in electron injection was devised through modeling, which involved a through analysis of the device and junction physics increases the blocking voltage of the material. Simulations show that an increase in breakdown voltage is achieved by placing a p^+ layer next to the cathode. The p^+ layer helps in lowering the magnitude of the electric field is also lowered improving the performance further. As a result the hold off voltage of the switch is improved by many orders of magnitude. The minimum thickness of the p^+ layer necessary to avoid premature breakdown is about a diffusion length.

The new improved design was simulated with laser illumination to understand the effectiveness of the blocking p^+ layer. The performance, due to the redistributed electric field after illumination, is limited to 36kV bias (~900kV/cm). This shows an improvement of 4 times over the existing PCSS technology. Increasing the thickness of the switch can be an alternative to obtain higher switch hold-off.

The optical absorption depth in SI SiC was modeled using experimental data and matched to simulations to exactly model the energy input requirement to achieve lowest possible laser energy which was realized to be 0.5 mJ.

Future Research

Even though using high K material is an efficient way to avoid field enhancement at the contacts, the actual filling of gaps between the electrode and SiC proved to be

difficult task. Hence some other method e.g. etching a few hundred micron thick trench in SiC with curved edges and then developing contacts is identified as another way of simplifying the process.

Optical absorption measurement with two different thicknesses with differential measurement is a part of future work. Manipulation of trap density inside the material to obtain the required resistance is important to achieve optimum energy input. The contact made to SiC need to be tested up to 1 million pulses to study their reliability. The use of p^+ layer is to be tested experimentally.

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VITA

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