DEPOSITION AND CHARACTERIZATION OF HIGH PERMITTIVITY THIN-FILM DIELECTRICS

A Thesis presented to the Faculty of the Graduate School
University of Missouri-Columbia

In Partial Fulfillment of the
Requirements for the Degree of

Master of Science

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by

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May 2006

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The undersigned, appointed by the Dean of Graduate School, have examined the thesis entitled

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ACKNOWLEDGEMENTS

Without the assistance of several individuals, this project would not have met with success. I would therefore like to extend my deepest gratitude to my advisor and mentor, Dr. Shubhra Gangopadhyay. Her motivation and insight provided me with the impetus for my graduate education. Without Dr. Shubhra's ever present guidance, my work would have in no way been possible. I will be eternally grateful to her.

I want to recognize all the members of our large group who worked on a range of projects, but were always willing to engage in insightful discussion and share their expertise. Dr. Maruf Hossain was of great help around the lab as I gained knowledge in deposition. He was available at all hours of the day which was of reassurance to me in the early going. Lou Ross and Randy Tindall were also extremely courteous in teaching me the basics of electron microscopy. To Maslina, Venu, Shantanu, Yuanfang, Yun, and all my colleagues, I will always cherish your friendship both inside and outside the laboratory.

I would also like to graciously thank the other two members of my thesis committee, Dr. Lex Akers and Dr. Suchi Guha. A genial acknowledgement is in order for Dr. Keshab Gangopadhyay as well, who provided valuable suggestions as I approached the end of my research.

The staff of the engineering department, in particular Betty Barfield, Susan Wayt, and Shirley Holdmeier were always generous and I am indebted to them.

Finally, I wish to dedicate this work to my loving parents. Their lifelong support and caring has been instrumental in my life. Thank you all.

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ABSTRACT

As integrated circuit (IC) devices scale to ever smaller nodes, replacing the front end dielectric has become a primary challenge. To enable greater device densities, control power consumption, and enhance performance, a new class of insulators with large dielectric constants (high-κ) will need to be employed as a replacement for oxides and oxynitrides of silicon. A variety of semiconductor devices ranging from metal oxide semiconductor field effect transistors to flash and dynamic random access memories stand to benefit from new high-κ dielectric thin-films. In addition, compact capacitors using high-κ dielectrics can enable high density on-chip energy storage. Compounds of HfO_2 and Al_2O_3 are among the leading high-κ candidates. There is also potential in incorporating nanoparticles into an insulating medium to enhance its dielectric constant. Previously, the use of nanoparticles for this purpose has typically been performed using techniques and materials that cannot be readily incorporated into modern IC fabrication. This thesis presents the results of work on reactive electron beam evaporated Al_2O_3 and HfO_2 thin-films, the incorporation of nanoparticles, and the characterization of these films on silicon substrates.

1 Introduction

1.1 Semiconductor Device Scaling

Since Jack Kilby and Robert Noyce invented the integrated circuit (IC) nearly half a century ago, progress made by the semiconductor industry has revolutionized the world. The first commercial microprocessor, the Intel 4004, utilized 2,300 transistors. Today's processors utilize over a quarter billion transistors. Feature sizes once measured in the hundreds of microns are now a few nanometers. This remarkable advancement has brought along with it a host of challenges facing future progress.

The first major power consumption issue was solved with the use of complimentary metal-oxide-semiconductor (CMOS) devices. Where previous NMOS designs consumed power while idle, CMOS designs with complimentary n and p-MOS field effect transistors (MOSFETs) greatly reduced static power consumption. Many other innovations have followed enabling continued scaling. Aluminum interconnects gave way to copper interconnects on the back end. Low-κ dielectrics reduce interconnect RC delays. On the front end, controlling the threshold voltage and reducing sub-threshold leakage have been among the chief concerns in device scaling. Silicon on insulator (SOI) has been employed to control leakage through the substrate bulk, but gate leakage through increasingly thinner oxides continues to pose a challenge.

The threshold voltage for a MOSFET is given below.

$$V_T = V_G = \frac{|Q'_{SD}(\max)|}{C_{OX}} - \frac{Q'_{SS}}{C_{OX}} + \phi_{ms} + 2\phi_f \tag{1.1}$$

In this equation, $|Q'_{SD}(\max)|$ is the depletion charge density, C_{ox} is the field oxide capacitance density, Q'_{ss} is the fixed oxide charge near the interface, φ_{ms} is the metal semiconductor work function difference, and $2\varphi_f$ is the condition for strong inversion. By minimizing the threshold voltage, switching speeds can be increased. Lowering the threshold voltage in general increases the sub-threshold drain to source leakage currents. However, this has been viewed by industry as a necessary compromise for increased performance.

Oxide fixed charge can be minimized in processing, but has reached a point of diminishing returns with current surface preparation and dielectric deposition methods. The depletion charge and φ_f are both controlled in large part by semiconductor doping. In order to maintain MOSFET operational characteristics, the Fermi level, and consequently the doping, cannot be altered significantly. The metal semiconductor work function is minimized by either controlling polysilicon doping or changing the choice of metal in the gate contact and is approximately 0.2 eV.[1] Thus, we can see that the greatest gains to be had in minimizing the threshold voltage are by increasing the field oxide capacitance density. The oxide capacitance is simply the parallel plate capacitance formula.

$$C_{OX} = \frac{A\varepsilon_o\kappa}{t} \tag{1.2}$$

Since we are dealing with capacitance density, the area, A, can be neglected. Therefore, capacitance density can be increased by either decreasing insulator thickness, t, or by increasing the dielectric constant, κ.

As industry begins use of the 65 nm node, field oxide thicknesses have scaled down to 1.0 nm equivalent oxide thickness (EOT). By the 45 nm node, EOT will be less

than 0.5 nm.[1] Insulators of this physical thickness would have unacceptable leakage due to direct tunneling. As such, some stop gap gate dielectrics, notably silicon oxynitride, are under use in the interim before the transition to true high dielectric constant (high-κ) oxides. These films offer only a temporary solution and high-κ films with substantially higher dielectric constants will be required within a few scaling generations. In addition to CMOS devices, a similar problem exists for dynamic random access memory (DRAM) and electronically erasable programmable read only memory (EEPROM). Both DRAM and EEPROM devices will also require high-κ dielectrics for charge storage in the case of DRAMs and charging and discharging in the case of EEPROMs. Another potential use of high-κ dielectrics is in on-chip energy storage devices such as high density capacitors.

In the drive to find a replacement for SiO_2 in CMOS devices, oxides of hafnium and aluminum emerged as leading candidates.[2] Robertson and Peacock have shown that aluminum oxide (Al_2O_3) has excellent conduction and valance band offsets on contact with Si.[3,4] This makes Al_2O_3 ideally suited for use with n and p-type Si over a range of doping levels. Band offsets for some common device dielectrics are given in Figure 1.1.

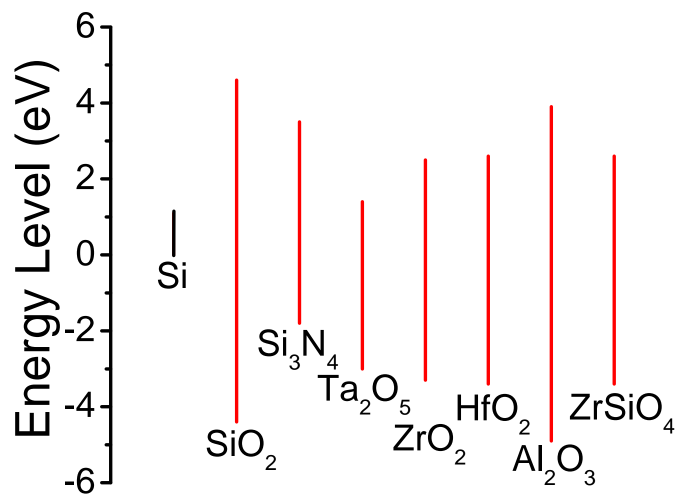

Figure 1.1 Conduction and valance band offsets relative to silicon of various dielectrics. [3]

The drawback is that the intermediate dielectric constant of Al_2O_3 (κ ≈8-12) limits the maximum achievable capacitance density compared with other high-κ dielectrics. Hafnium dioxide (HfO_2) and compounds of HfO_2 are also among the most promising candidates to replace SiO_2. However, while HfO_2 possess a higher dielectric constant (κ ≈20-25) than Al_2O_3, it has narrower band offsets relative to Si. In general, higher relative permittivity dielectrics have smaller bandgaps and poor band offsets, making them less suitable for use on Si. A plot of this relationship for several dielectrics is shown in Figure 1.2.

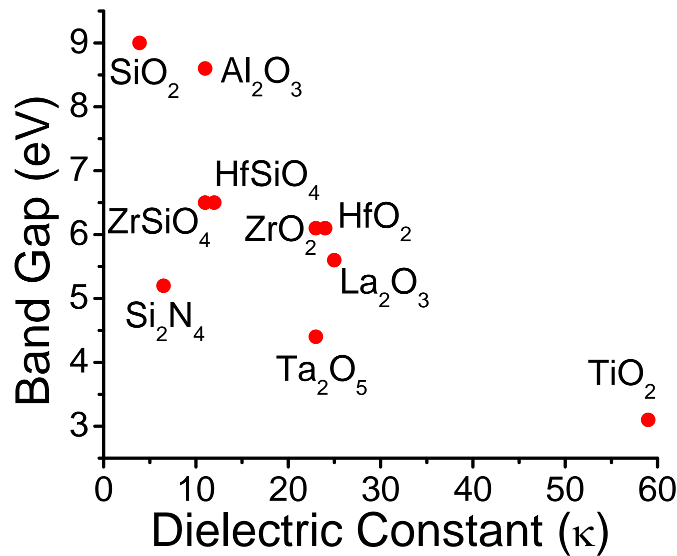

Figure 1.2 Plot of the bandgap versus dielectric constant for various insulators showing the generally inverse relationship between the two. [3]

It is very desirable to find high-κ dielectrics that work well on Si for use in IC and on-chip devices. Semiconductor device grade films of Al_2O_3 and HfO_2 have been successfully deposited on Si.[5,6] However, prior work on using noble metal nanoparticles has focused primarily on polymer and glass dielectrics and processes that are not readily compatible with current IC fabrication.[7-9]

1.2 Research Overview

This work details the results of research on HfO_2 and Al_2O_3 thin-films. This project first began with electron beam (e-beam) HfO_2, and subsequently, Al_2O_3 depositions. HfO_2 was chosen initially because of prior efforts that had gone into successful e-beam evaporation of these films. Both were evaporated under oxygen directly from HfO_2 and Al_2O_3 sources. With a controlled Al_2O_3 deposition process established, ultra thin noble metal layers were evaporated with the intent of forming nanoislands. The first metal attempted was platinum. However, silver was eventually chosen because of better available control over its evaporation rate – which is crucial to depositing nanoparticles. Al_2O_3 films with embedded silver nanoparticles were then deposited to study the effect of the dispersed metal. Sputtering was the third and final phase of this project, focusing on depositing Al_2O_3 directly from an Al_2O_3 target.

The following sections of this thesis are divided as follows. Presented first is an overview of the MOSFET (the MOS capacitor in particular), floating gate transistors and the effect of minute metal particles on permittivity. Second, a discussion on e-beam evaporated Al_2O_3 and HfO_2 stacks is given. Next is a section on Al_2O_3 films with embedded silver nanoparticles. Following this is a section on Al_2O_3 sputtering. Last is a brief discussion on possible future extensions of the work presented up to that point. Included within these sections are the procedures that were followed and the results of various characterization methods.

2 Theory

2.1 MOS System

2.1.1 MOSFET

The MOSFET is a field effect transistor comprised of a drain, source, and gate. Bias applied to the gate controls the flow of electrons (or holes) between the source and drain. The drain and source region are doped of the opposite type of the substrate. MOSFETs can be either enhancement mode or depletion mode devices. Enhancement mode MOSFETs require the formation of an inversion layer to form the conducting channel between source and drain. Depletion mode MOSFETs on the other hand are normally conducting and require a bias to deplete the channel, thereby restraining the flow of carriers between the source and drain. Most MOSFETs are enhancement mode devices and the following sections deal with the operation of enhancement mode, n-chnanel, p-substrate MOSFETs unless otherwise noted.

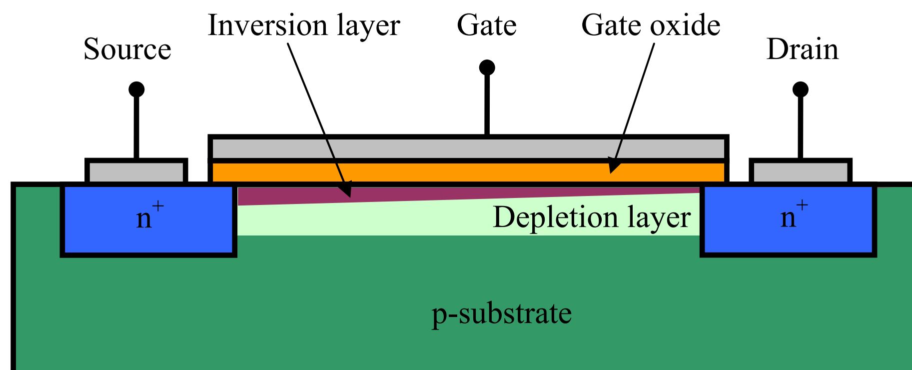

Figure 2.1 n-channel MOSFET with depletion and inversion layers shown

2.1.2 MOS Capacitor

The MOS capacitor is the stack forming the gate in a MOSFET. It is comprised of a metal (or heavily doped polysilicon) top contact and a semiconductor substrate separated by the field oxide. The MOS capacitor itself is a two-terminal device. Bias applied to the metal contact sweeps the MOS structure through accumulation, depletion, and inversion by controlling the buildup of majority and minority carriers in the semiconductor near the oxide through the field effect. The energy band diagram of a MOS system in equilibrium is shown in Figure 2.2.

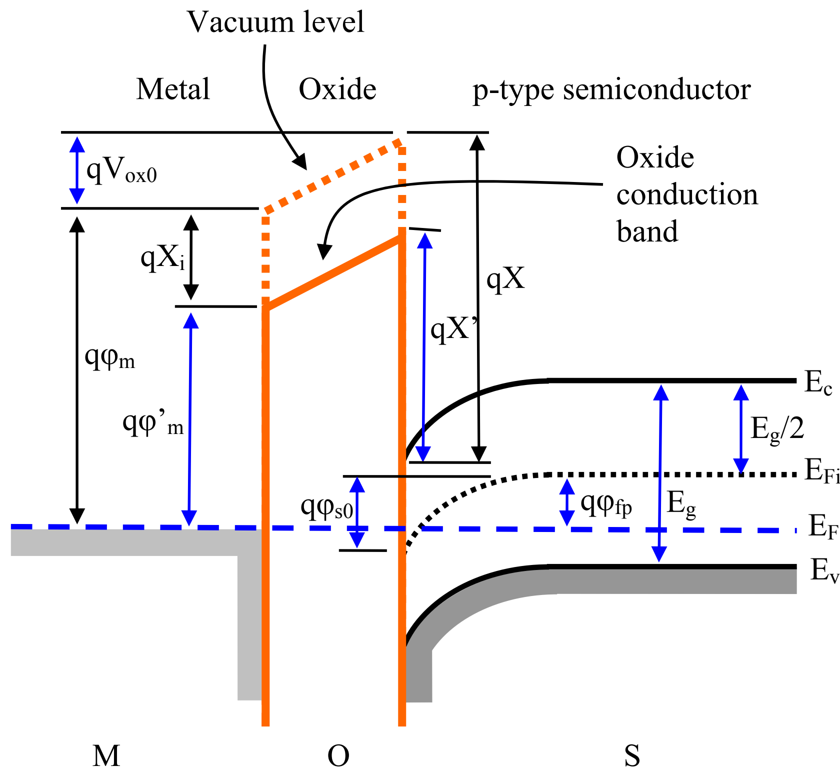

Figure 2.2 Energy band diagram of a MOS system on p-type Si

Some terms in the system will now be defined. E_c and E_v are the conduction and valance bands, respectively. E_{Fi} is the intrinsic Fermi level of the Si and E_F is the Fermi

level. q is the unit electronic charge. $q\varphi_s$ represents the surface potential and is an important term in describing the state of the MOS stack. $q\varphi_f$ is the distance the Fermi energy is from the intrinsic Fermi energy and is dependent on the doping of the semiconductor.

A brief discussion on the three modes of operation for a MOS device will now be presented. In accumulation, a sufficiently negative charge applied to the gate for a p-type semiconductor (positive for a n-type semiconductor) results in the attraction of majority carriers to the region directly beneath the field oxide. This maintains the reverse bias between the gate and drain and gate and source, thereby inhibiting conduction from gate to source. As the bias becomes increasingly more positive (negative for an n-type semiconductor), the majority carriers are repelled away from the surface resulting in the establishment of a depletion region underneath the oxide. As a result of band bending, the intrinsic Fermi level moves toward the Fermi level. When the bias is strongly positive (or negative for a n-type semiconductor), minority carriers from the semiconductor bulk enter the region just below the oxide and establish an inversion region – an n-type region for a p-type substrate and vice-versa. This inversion layer comprised of the minority carriers in the gate semiconductor is of the same polarity as the majority carriers in the drain and source semiconductor. Thus, a conducting channel is formed from the source to drain. The intrinsic Fermi level at inversion is below the Fermi level (in the case of a p-type semiconductor). Energy band diagrams in the various regions are illustrated in the figure below.

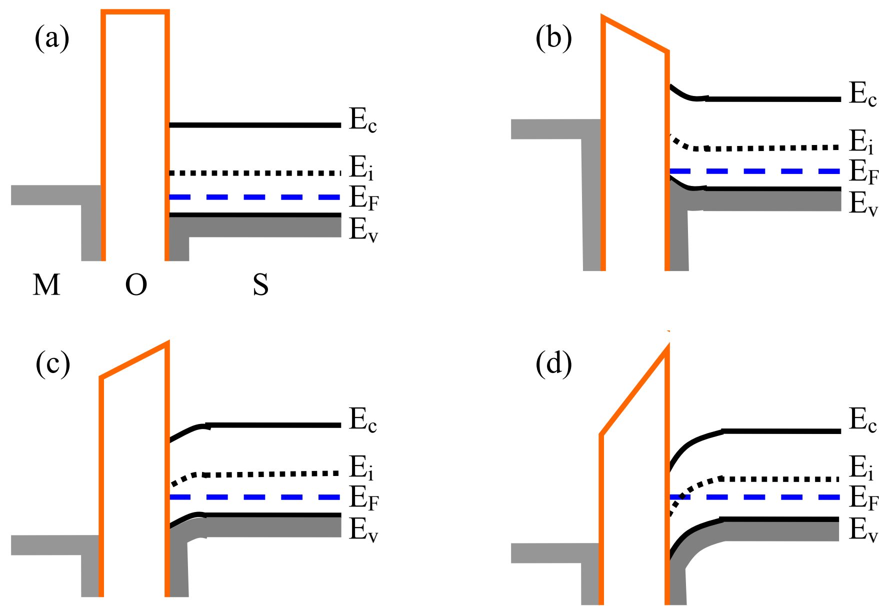

Figure 2.3 Energy band diagram of a MOS system at (a) flatband, (b) accumulation, (c) depletion and (d) inversion. The semiconductor is p-type.

By definition, the surface potential determines which region of operation a MOS device is in. When $q\varphi_s$, which is a function of the applied gate bias, is zero, the device is at the flat band condition with a corresponding bias voltage V_{FB}. When $q\varphi_s = q\varphi_f$, the semiconductor near the oxide effectively has the carrier concentrations of intrinsic Si and the device is at midgap. Here, the semiconductor Fermi level position at the oxide interface is equal to the intrinsic Fermi level position. For strong inversion, $q\varphi_s$ must equal twice $q\varphi_f$. When this occurs, the inversion layer has a minority carrier concentration equal to the majority carrier concentration in the semiconductor far from the interface. That is, the inversion layer has minority carriers of opposite polarity, but equal concentration to the majority carriers in the semiconductor bulk.

We now define V_{FB} and the threshold voltage, V_T. The following derivations are for a p-type semiconductor. Voltage across the gate, V_G, at zero applied bias (in equilibrium), is

$$V_G = V_{OX} + \phi_S + \phi_{ms} \quad (2.1)$$

Where V_{OX} is the voltage across the oxide and φ_{ms} is the metal-semiconductor work function difference. If we define Q_{SS}' as the net fixed charge per unit area in the oxide very near the interface and knowing there is no net charge in the semiconductor, for charge neutrality, we must have

$$Q_{SS}' + Q_m' = 0 \quad (2.2)$$

Here, Q_m' is the charge density on the metal. By the definition of capacitance

$$V_{OX} = \frac{Q'_m}{C_{OX}} \quad (2.3)$$

C_{ox} is the oxide capacitance per unit area. By substitution, the flat band voltage is

$$V_{FB} = V_G = \frac{-Q'_{SS}}{C_{OX}} + \phi_{ms} \quad (2.4)$$

Figure 2.4 illustrates the flat band charge distribution in a MOS stack.

The threshold voltage is now similarly defined. As mentioned earlier, V_T is the voltage at which the surface potential is equal to twice $q\varphi_f$. To establish this condition, the charge in the depletion region must be offset in addition to the flat band criteria. Depletion charge density is

$$|Q'_{SD}(max)| = eN_a x_{dT} \quad (2.5)$$

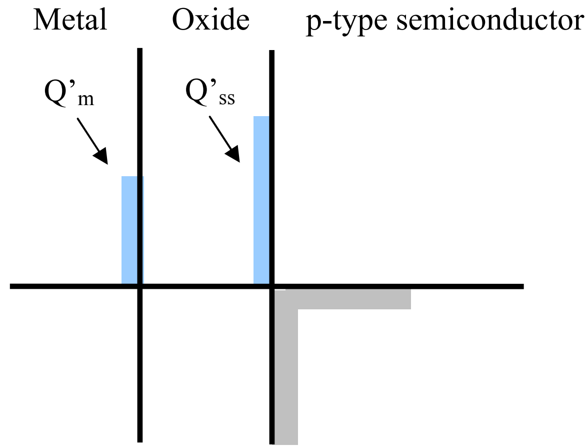

Figure 2.4 Charge distribution in a MOS stack at flat band.

This is a rather straightforward concept as the depletion region charge density per unit area is simply the unit electronic charge times N_a (the doping density of the p-type semiconductor) times the depletion region depth, x_{dT}. From these conditions, the threshold voltage for a p-type semiconductor is

$$V_T = V_G = \frac{|Q'_{SD}(\max)|}{C_{OX}} - \frac{Q'_{SS}}{C_{OX}} + \phi_{ms} + 2\phi_f \tag{2.6}$$

and for a n-type semiconductor, it is

$$V_T = V_G = -\frac{|Q'_{SD}(\max)|}{C_{OX}} - \frac{Q'_{SS}}{C_{OX}} + \phi_{ms} + 2\phi_f \tag{2.7}$$

The charge distribution at threshold is shown in Figure 2.5.

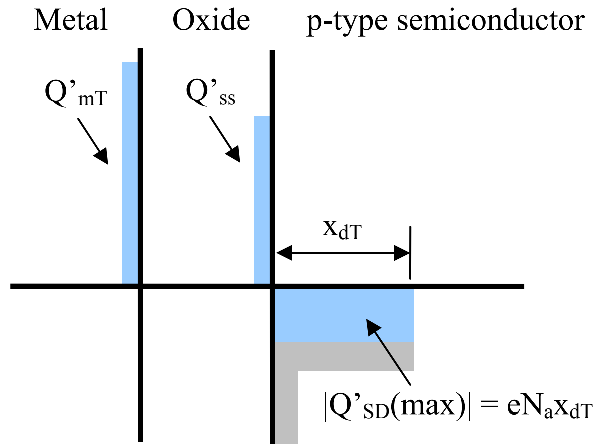

Figure 2.5 Charge distribution in a MOS stack at the inversion threshold.

Ref. 10 provides a more detailed discussion of charge distribution. The MOS capacitor stack is most simply represented by the series combination of the oxide capacitance and a bias dependent semiconductor capacitance (comprised of the depletion/inversion layer capacitance).

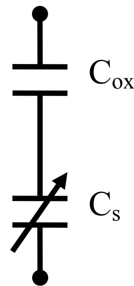

Figure 2.6 MOS equivalent circuit

2.1.3 Direct Tunneling and Field Emission

From the Schrödinger equation, we know that there is a finite probability that a particle can tunnel through a non-infinite barrier. As the barrier width decreases, the probability of a particle penetrating it rises exponentially. In sufficiently thin oxides (below 15 Å), direct quantum mechanical tunneling through the barrier can occur. Also, under oxide band bending, electrons can more readily penetrate a barrier giving rise to

Fowler-Nordheim (F-N) tunneling or field emission. F-N tunneling can occur even in thicker oxides under sufficient band bending. Direct and F-N tunneling are similar in nature, with the basic difference being that direct tunneling occurs through the trapezoidal barrier and F-N tunneling occurs through the upper triangular barrier. In conventional MOSFETs, both tunneling mechanisms can greatly increase oxide leakage currents. Figure 2.7 shows both tunneling mechanisms.

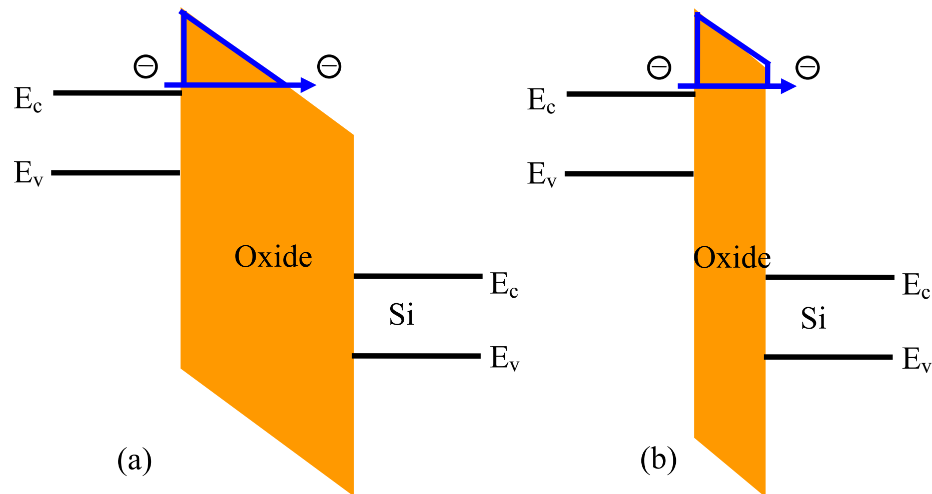

Figure 2.7 Tunneling mechanisms through a MOS oxide. (a) Fowler-Nordheim tunneling and (b) direct tunneling.

Continued tunneling can eventually cause time dependent dielectric breakdown (TDDB). TDDB is caused by electrons emitted from the cathode terminal tunneling into the oxide. Here, they are accelerated by the electric field and can subsequently cause impact ionization events within the oxide, creating electron-hole pairs. Because of the very poor carrier mobilities in insulators, these carriers, in particular holes, can be trapped by oxide defects altering the band structure of the oxide.[11] TDDB is often catastrophic, resulting in permanent damage to the oxide. It is therefore vital to find dielectrics with good band offsets that have high dielectric constants which can maintain physical

thicknesses above 15 Å, while allowing EOTs downwards of 10 Å to curtail charge transport in the field oxide.

Controlled field emission can be advantageously used in floating gate devices. These devices are discussed in greater detail in section 2.2 .

2.1.4 Non-Ideal Effects

A real MOS system usually deviates from theoretical behavior as the result of a few factors. These include oxide charge, work function difference, and interface trapped charge. Interface trapped charge will be discussed in greater detail in the next section.

Oxide charges fall into one of three categories: oxide fixed charge, oxide trapped charge and mobile ions.[12] Fixed charge, Q_f, is independent of oxide thickness as it is located very near the oxide-semiconductor interface (within 30 Å), but entirely within the oxide. It is not dependent on the semiconductor doping, but is dependent on the silicon orientation and oxide deposition and annealing. A positive Q_f results in a negative V_{FB} shift and a negative Q_f results in a positive V_{FB} shift. This can be more clearly explained considering charge neutrality. If a negative bias is applied at the gate, then this charge must be compensated by positive charge somewhere along the MOS stack. Ideally, when Q_f is 0, this charge is compensated entirely by donors in the semiconductor. However if a positive fixed charge is present, then this will partially compensate some of the negative gate charge. This reduces the number of donors in the semiconductor that are required to compensate the charge at the gate and thus reduces the depletion region width. A narrower depletion region raises overall MOS capacitance (since the MOS capacitance is the series combination of the oxide and depletion capacitances), producing a positive

capacitance-voltage (C-V) shift. The opposite is the case for negative fixed charge. The flat band voltage shift due to fixed charges is given as follows

$$Q_f = \frac{1}{d}\int_0^d x\rho_f(x)dx$$

$$\Delta V_f = \frac{Q_f}{C_{OX}} \tag{2.8}$$

Here, $\rho_f(x)$ is the fixed charge density at the interface.

Oxide trapped charges, Q_t, are electrically neutral sites distributed throughout the oxide that can be charged with the introduction of electrons or holes. These sites are usually caused by defects in the oxide bulk. They also cause a voltage shift as follows

$$Q_t = \frac{1}{d}\int_0^d x\rho_t(x)dx$$

$$\Delta V_t = \frac{Q_t}{C_{OX}} \tag{2.9}$$

Here, $\rho_t(x)$ is the *volume* oxide trap density and Q_t is the effective bulk oxide trapped charge density *per unit area* present at the interface.

Mobile charges are typically alkali ions such as sodium and potassium.[13] They are unintentionally introduced during device fabrication as the result of contamination. Unlike the trapped and fixed charges, which are located at a single site, mobile ions move about within the oxide. This results in a bias and bias sweep direction dependent voltage shift or hysteresis. Similar to the localized charges, the voltage shift is given by

$$Q_m = \frac{1}{d}\int_0^d x\rho_m(x)dx$$

$$\Delta V_m = \frac{Q_m}{C_{OX}} \tag{2.10}$$

Again, it should be noted that $\rho_m(x)$ is the *volume* mobile charge density and Q_m is the mobile charge density *per unit area*.

The total flat band voltage shift due to oxide charges is the sum of these three individual voltage shifts.

$$\Delta V_{FB} = \Delta V_f + \Delta V_t + \Delta V_m \tag{2.11}$$

The work function difference between the semiconductor and the gate metal is the other component of flat band voltage shift.

$$\phi_S = \chi + \frac{E_g}{2q} + \phi_f$$

$$\phi_{ms} = \phi_m - \phi_s \tag{2.12}$$

The total flat band voltage shift therefore is

$$\Delta V_{FB} = -\frac{Q_f + Q_t + Q_m}{C_{OX}} + \phi_{ms} \tag{2.13}$$

This is simply an expansion on (2.4).

2.1.5 Interface Defect Density Analysis

Interface trap states arise from the abrupt termination of the crystalline Si lattice. The trap charge is a quantity Q_{it}. Q_{it} are states existing within the bandgap of Si. Shockley *et al.* first found the existence of such states experimentally.[14] It was later shown that this charge is directly related to surface density of Si atoms (~10^{15} cm^{-2} on Si (100)) with measurements on clean Si surfaces in an ultra high vacuum environment.[15] Typically, dielectric deposition on the Si surface and annealing satisfies most of the

charge, thereby reducing this state density by several orders of magnitude, typically to the 10^{10}-10^{12} eV/cm^2 range. States are either donors or acceptors.

Interface defect densities can be calculated using one of a few methods. These include the Terman and Lehovec methods.[16-18] Further information regarding the use of these methods is referred to the appropriate texts. For the work presented here, the conductance method proposed by Nicollian *et al.* was used.[19,20]

Since interface traps are located in the semiconductor bandgap at the oxide-semiconductor interface, their position relative to the Fermi level is affected by band bending. By varying the bias, trap occupancy as governed by the Fermi-Dirac probability function, can be altered. Following is the Fermi-Dirac function where the trap has an energy level, E_T, and g is a spin degeneracy factor of ½ for donors and 2 for acceptors.

$$f(E_T) = \frac{1}{1 + \frac{g \cdot e(E_T - E_F)}{kT}} \tag{2.14}$$

This is also schematically illustrated in Figure 2.8.

When an AC small signal (~30 mV_{p-p}) is superimposed onto the DC bias, the traps very near the Fermi level will be forced to change occupancy as the Fermi level oscillates above and below these trap levels. While the band structure itself can respond instantaneously to this varying bias, the interface traps cannot. There is a lag between the time the Fermi level crosses below an occupied trap and the time at which that trap actually empties. This charge storing characteristic results in a capacitance, C_{it}, measured in parallel with the depletion capacitance. There is a time constant associated with this lag. Also, the filling and emptying of traps with carriers results an energy loss, which must be supplied by the measuring instrument and is observed as a parallel conductance,

G_p. Other factors such as series resistance and leakage can also contribute to energy loss and care should be taken to either correct for or eliminate them.

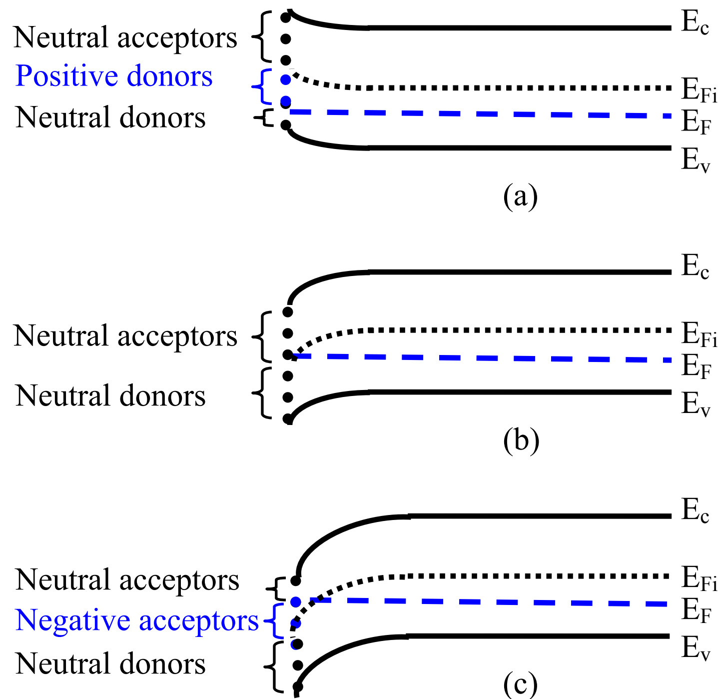

Figure 2.8 Interface trap occupancy relative to the Fermi level at (a) accumulation, (b) midgap, and (c) inversion.

The loss is dominated by majority carrier transitions at the traps and there is an small signal frequency at which it is comparable to the majority carrier transition time constant. When a group of traps have linked capacitances and capture resistances, they behave as one traps of one energy level, yielding the single time constant (STC) model. The equivalent circuit of this model is as follows.

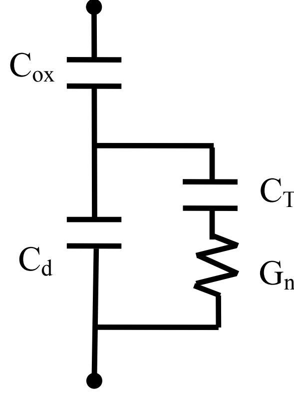

Figure 2.9 Equivalent circuit for STC model. Note the device is in depletion. The series combination of C_T and G_n form the trap admittance Y_{it}.

The admittance of the STC traps is given by

$$Y_{it} = \frac{\omega^2 \tau C_{it}}{1+\omega^2\tau^2} + j\frac{\omega C_{it}}{1+\omega^2\tau^2} \tag{2.15}$$

Which is of the general form

$$Y_{it} = G_p + j\omega C_p \tag{2.16}$$

For the STC model

$$\frac{G_p}{\omega} = \frac{qD_{it}\omega\tau}{(1+\omega^2\tau^2)} \tag{2.17}$$

G_p/ω is maximized for $\omega\tau = 1$ in the STC model.

When the interface traps have energy levels so closely spaced across the bandgap that they are a virtually continuous distribution, it gives rise to the continuum of states model.

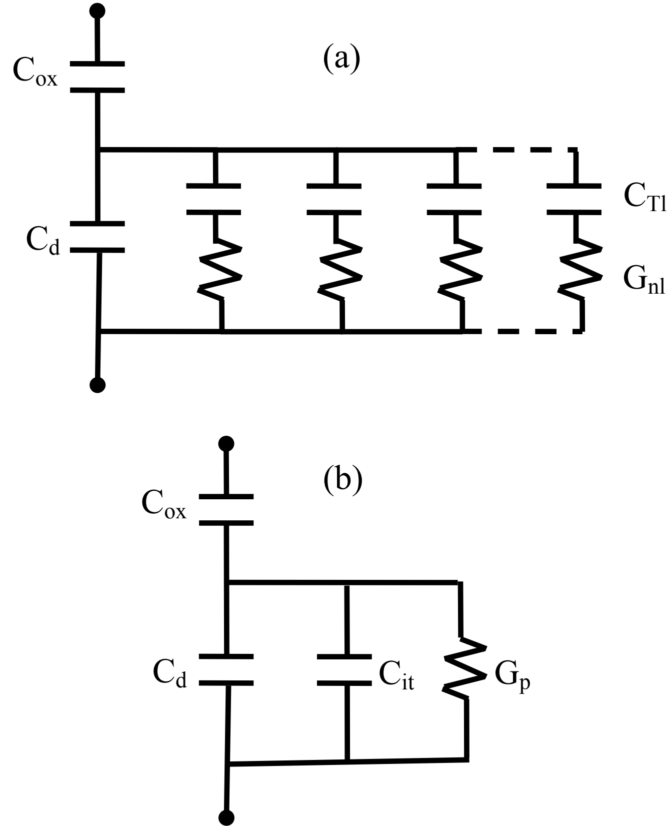

Figure 2.10 (a) Equivalent circuit for continuum model. Note again the device is in depletion. (b) Equivalent lumped model.

The admittance of the continuum lumped model is

$$Y_{it} = \frac{C_{it}}{2\tau}\ln(1+\omega^2\tau^2) + j\frac{C_{it}}{\tau}\tan^{-1}(\omega\tau) \tag{2.18}$$

From this for the continuum model

$$\frac{G_p}{\omega} = \frac{qD_{it}\ln(1+\omega^2\tau^2)}{2\omega\tau} \tag{2.19}$$

G_p/ω is maximized for $\omega\tau = 1.98$ in the continuum model.

For both the STC and continuum models

$$\frac{G_p}{\omega} = \frac{\omega C^2{}_{ox} G_m}{G^2{}_m + \omega^2(C_{ox} - C_m)^2} \tag{2.20}$$

A complete derivation of both of these models and a third model, the statistical model, is presented in Ref. 20.

To effectively perform analysis, the data must typically be corrected for the presence of series resistance, R_s. If the measured admittance across the probe terminals is

$$Y_{ma} = G_{ma} + j\omega C_{ma} \tag{2.21}$$

The $_{ma}$ subscript denotes measured in accumulation. Then, the inverse of the admittance is the impedance, Z_{ma}, of which the real part is the resistance, R_s. The set of equations for corrected capacitance, C_c, and conductance, G_c, are as follows

$$R_s = \frac{G_{ma}}{G^2{}_{ma} + \omega^2 C^2{}_{ma}}$$

$$a = G_m - (G^2{}_m + \omega^2 C^2{}_m) R_s$$

$$C_c = \frac{(G^2{}_m + \omega^2 C^2{}_m) C_m}{a^2 + \omega^2 C^2{}_m}$$

$$G_c = \frac{(G^2{}_m + \omega^2 C^2{}_m) a}{a^2 + \omega^2 C^2{}_m} \tag{2.22}$$

R_s is found using the accumulation capacitance and conductance values at 1 MHz and this value is thereafter used as a constant at all lower frequencies. It is typically less then 1 kΩ for low doped substrates and can be less than 100 Ω for heavily doped substrates.

2.2 Floating Gate MOS Devices

Important classes of non-volatile memory storage elements using the MOSFET structure are floating gate MOS devices first proposed by Kahng and Sze.[21] In this structure, a second gate floats within the oxide, separated from the substrate by a thin insulating layer known as the tunneling oxide. A floating gate device is at the heart of

erasable-programmable read-only memories (EPROM). EPROMs that are electrically erasable are known as EEPROMs, and flash memory is a derivative of EEPROMs.

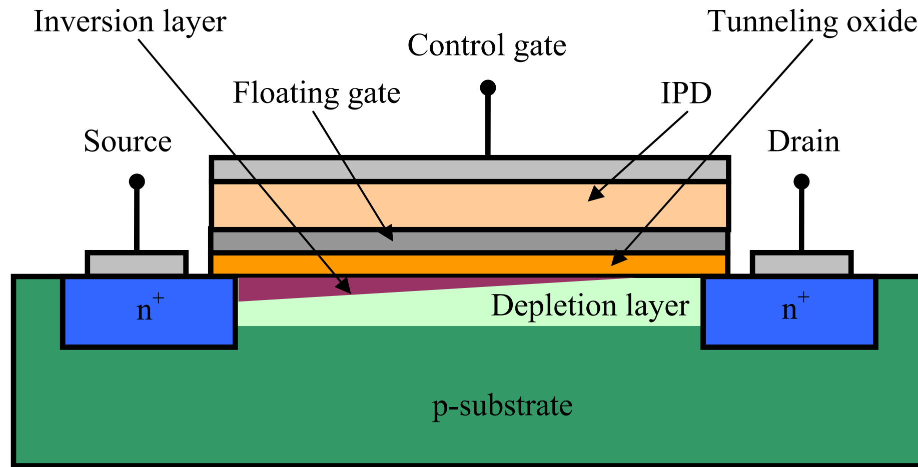

Figure 2.11 Floating gate device. The lower gate is the floating gate and the upper gate is the control gate. IPD is the inter polysilicon dielectric.

The working principle behind EEPROM is charge stored in the floating gate alters the threshold voltage of the transistor. In a manner similar to how oxide charges produce a C-V shift in MOSFET devices, charges on the floating gate alter the turn on characteristics of the floating gate device. The threshold voltage shift is given as

$$\Delta V_T = -\frac{d_2}{\varepsilon_2} Q \tag{2.23}$$

The charging, storage and erase band diagrams are shown below.

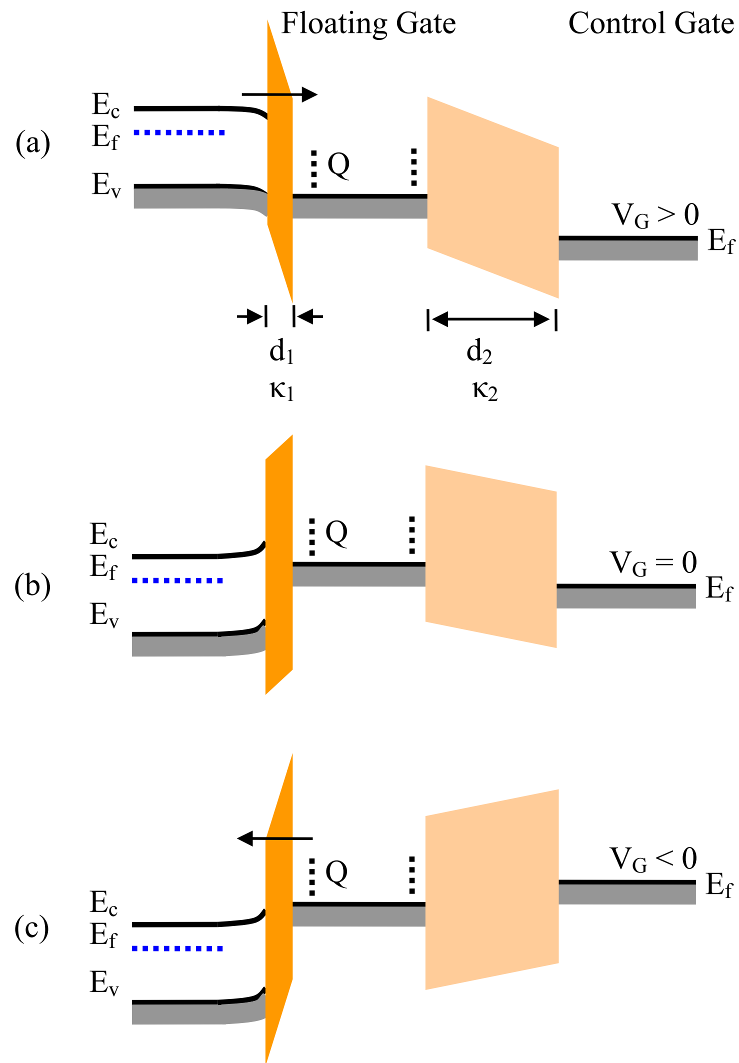

Figure 2.12 Floating gate structure in (a) charging, (b) storage and (c) discharging

Under equilibrium conditions, the floating gate is isolated from both the control gate and the substrate by the insulators. However, when a large bias is applied to the control gate, the two insulating layers will undergo band bending. The thinner tunneling oxide will undergo more severe band bending and charges in substrate can tunnel through the very thin tunneling oxide and be trapped by the floating gate. The mechanism is the F-N tunneling described previously. Because the oxide layer above the floating gate is

thicker (such that tunneling is not prominent), the charges remain trapped at the floating gate, increasing the threshold voltage. This floating gate, similar to the control gate, is typically heavily doped polysilicon. The device can now be “read” by checking its threshold voltage. To erase the device, the gate bias is reversed, thereby allowing charge trapped on the gate to tunnel back into the substrate, restoring the threshold voltage to the lower state.

Alternatively, these devices can be programmed by hot carrier injection. On n-type substrates, the hot carriers are holes and on p-type substrates, the hot carriers are electrons. For devices on p-type substrates, by applying a positive bias to the drain, relative to the source, electrons are accelerated along the channel toward the drain until they reach the pinch off region near the drain. Here, they have sufficient energy to overcome the band offset between silicon and the oxide and can enter the oxide. If a positive potential is present at the floating gate, then the electrons are attracted to the floating gate. Charge slowly builds on the floating gate until a sufficient number of electrons are present to repel further charging. The end result of hot carrier injection is identical to the F-N programming method in that charge is introduced at the floating gate.

While programming can be by either F-N tunneling or hot carrier injection, electrical erasure is almost exclusively by F-N tunneling. Because of the storage and erase mechanisms, floating gate devices have a finite write/erase cycle count, usually in the 10^4-10^6 range.

Tunneling oxide selection is largely dictated by the band offsets and leakage properties of the material. High-κ dielectrics are once again of interest in EEPROM devices. Here, the lower band offsets of high-κ oxides like HfO_2 can actually be

advantageous as it allows for lower operating voltages and thicker tunneling oxides, reducing leakage currents. Consequently, such devices can be programmed using lower voltages, at faster speeds and retain the data for longer periods of time. Interesting multilayer dielectrics comprised of oxides with different dielectric constants and bandgaps have even been proposed to tune the program and erase characteristics of the tunneling oxide.[22]

The permittivity of the oxide between the two gates (inter polysilicon dielectric or IPD) is also important. By increasing the dielectric constant of this oxide, the coupling between the two gates can be enhanced – something that is of substantial importance, particularly as devices are scaling to smaller and smaller features.[23] Again, the result is lower operating voltages and faster programming speeds.

2.3 The Effect of Metal Nanoparticles

While very often floating gate devices are made with a polysilicon gate, the advantages of using metal nanoparticles has been well reported.[24] These include a high density of states, a variety of available work functions enabling excellent control over program and erase characteristics while improving retention time, and charging via a Coulomb blockade effect. Due to the large conduction band state density, metal nanoparticles are better suited for exploiting the later as compared to devices using semiconductor nanoparticles. There is also some potential that nanoparticles behave as dipole oscillators, helping to enhance the permittivity of the medium in which they are dispersed.[25] In addition to conventional high-κ dielectrics, the use of metal nanoparticles to alter the properties of thin-film insulators on silicon is presented in this work.

2.4 Characterization Methods

2.4.1 Ellipsometry

Variable angle spectroscopic ellipsometry (J. A. Woolam V.A.S.E ®) was used to measure the thickness of the dielectric films. V.A.S.E is a non-destructive optical characterization technique. Linearly polarized, monochromatic light incident on a surface is reflected and elliptically polarized. The incident light on a thin-film is either reflected off the film surface or is refracted into the film and undergoes internal reflections within the film before being absorbed by the substrate or emerging from the film. By measuring the polarization change, properties of the film including thickness and refractive index can be extracted.

The general setup of an ellipsometer is shown below. The direction parallel to the plane of incidence is the p-plane and the direction normal to it is the s-plane. N is the complex index of refraction and is equal to n + jk, where n is the index of refraction and k is the extinction coefficient. N varies for each material and is wavelength dependent. If the two Fresnel reflection coefficients (the ratios of incident and reflected light) in the p and s directions are r_p and r_s, then

$$\frac{r_p}{r_s} = \rho = \tan(\Psi)e^{j\Delta} \tag{2.24}$$

Where tan Ψ is the amplitude ratio ($|r_p| / |r_s|$) and Δ is the phase difference ($\delta_p - \delta_s$).

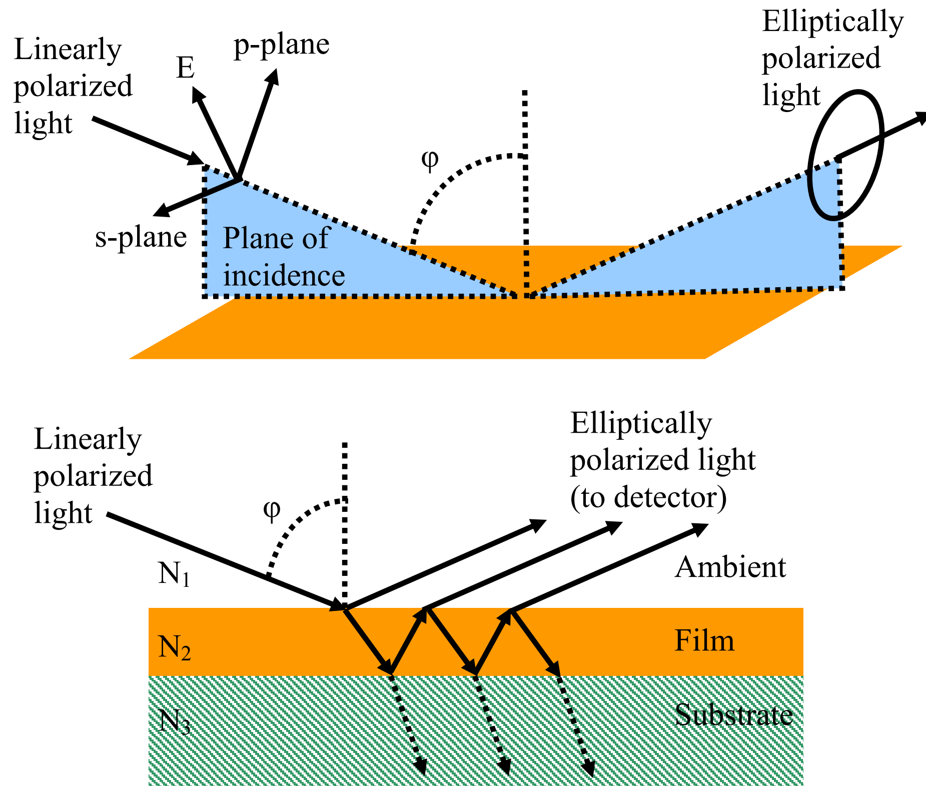

Figure 2.13 Geometry of ellipsometer measurement

V.A.S.E. does not measure the individual Fresnel coefficients, but rather the ratio ρ. A model is then used to fit the experimental Ψ and Δ values to those of known materials and/or Cauchy layers. Recursive methods are used to determine the model parameters (n, k, and thickness) for each layer. For material layers, the refractive indexes (and extinction coefficients) at various wavelengths are known and the thickness is determined. In a Cauchy layer the wavelength dependent refractive index is of the form $n(\lambda) = n_0 + n_1/\ \lambda^2 + n_2/\ \lambda^4$. It is used in cases where the film is of unknown type. The coefficients (n_0, n_1, and n_2) are varied and thus both the refractive index and thickness are solved for simultaneously. A graded Cauchy layer used for depth profiles is comprised of multiple discrete Cauchy layers, each with its own refractive index and thickness.

2.4.2 Electron Microscopy

Scanning electron microscopy (SEM) is used to image small features. In a SEM, an incident electron beam strikes a surface and results in the emission of electrons and x-rays. Beam electrons which are scattered and emerge from the substrate are backscattered electrons (BSEs). Substrate electrons that are ejected as the result of scattering events with the beam electrons are secondary electrons (SEs). BSEs have much higher energies than SEs, allowing them to be detected separately. When the incident beam electrons excite substrate electrons to a higher energy state, the excited electrons emit an x-ray photon when they fall back to their ground state. These photons have an energy and wavelength characteristic of the element from which they were emitted. Energy dispersive spectroscopy (EDS) and wavelength dispersive spectroscopy (WDS) are used to characterize the elemental composition of a material.

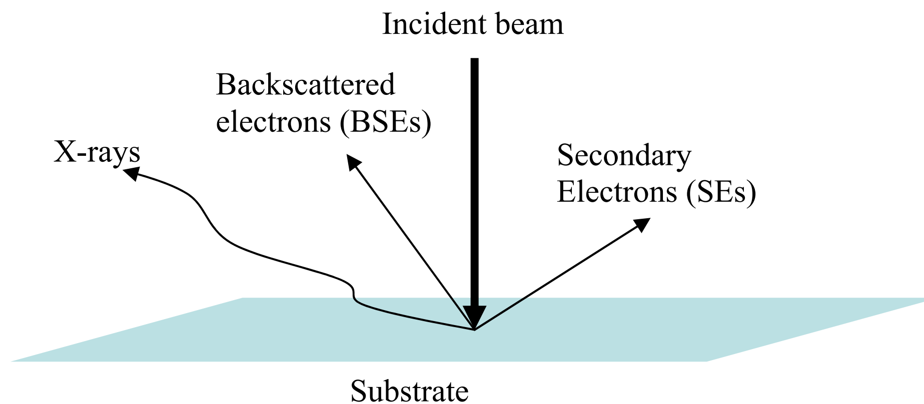

Figure 2.14 Basic electron microscopy

2.4.3 Electrical Characterization

An inductance-capacitance-resistance (LCR) meter and sourcemeter were utilized for all electrical measurements. The HP 4284A LCR meter is capable of measuring two

parameters simultaneously including capacitance-voltage (C-V), conductance-voltage (G-V), and resistance-voltage (R-V). It can provide a ±40 V DC bias and an AC small signal frequency up to 1 MHz. The Keithley 2400 sourcemeter is capable of a ±200 V DC bias and can source or sink 1 A, up to a maximum of 20 W. It was used for all current-voltage (I-V) measurements. The LCR meter and sourcemeter were controlled via a LabVIEW program on the GPIB interface bus. The setup of both is illustrated below (note only the 2400 or 4284A was connected to the probestation at any given time).

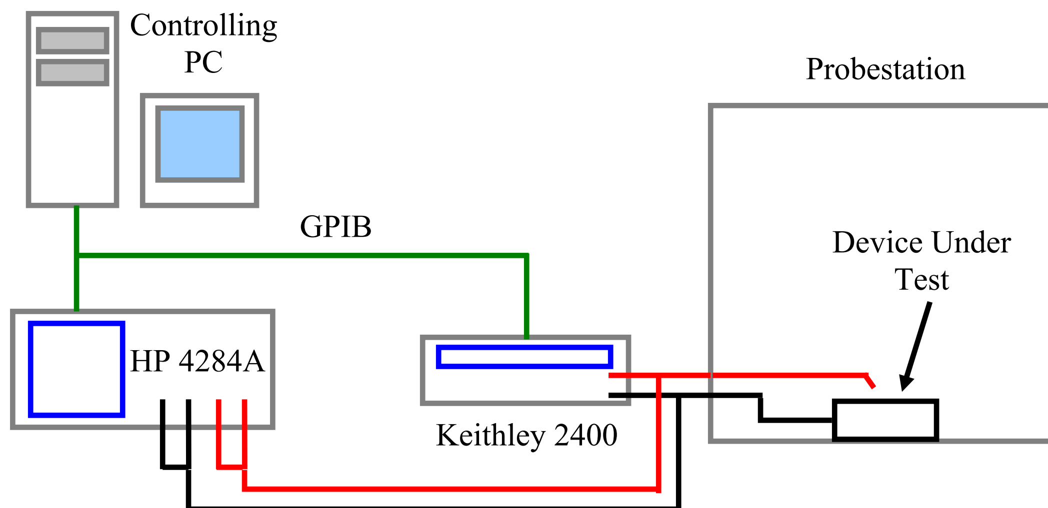

Figure 2.15 Electrical measurement setup

3 Reactive E-beam Evaporation of Al_2O_3/HfO_2 Stacks

3.1 Introduction

As discussed earlier, Al_2O_3 has excellent band offsets on Si, comparable to that of SiO_2. However, its permittivity under the best conditions is ≈12. HfO_2 on the other hand has a higher permittivity, but narrower band offsets. A dielectric stack with Al_2O_3 on Si with HfO_2 over the Al_2O_3 would offer a compromise between intermediate permittivity and narrow band offsets. Such films have already been explored by industry and have been shown to have merit.[26] Unlike using SiO_2 as the intermediate layer through methods such as post HfO_2 deposition oxygen annealing, the use of Al_2O_3 as the intermediate dielectric would yield a higher overall stack permittivity.

E-beam evaporation has been successfully employed to fabricate both device grade Al_2O_3 and HfO_2 films individually.[27,28] However, stacks of both films have primarily been deposited with atomic layer deposition (ALD) chemical vapor deposition (CVD) processes. This chapter details the use of e-beam evaporation to deposit two layer stacks under an oxygen ambient and the characterization of these devices. Both single side polished float zone (FZ) p (1-10 ohm-cm) and p+ (0.0030-0.0070 ohm-cm) Si (100) were used. In this and all sections, the top contact diameter is 75 μm.

3.2 Experiment

3.2.1 Cleaning

Samples were cleaned with a variant of the Shiraki method.[29,30] This procedure is known to remove organics and the native oxide in a series of steps involving the growth and etch of oxide layers. Further, the final step results in a hydrogen passivated surface that is reasonably resistant to the reformation of a native oxide for a period of a few hours. All chemicals were semiconductor grade products from Sigma Aldrich/Riedel-de Haër. The following table details the cleaning procedure used for all samples in this thesis.

Step	Procedure
1	10 min. HNO_3 dip at 90 °C followed by DI water rinse (thick oxide growth)
2	1 min. $HF:H_2O$ (1:3) dip followed by DI water rinse (oxide etch)
3	10 min. $HCl:H_2O_2:H_2O$ dip at 90 °C followed by DI water rinse (thin oxide growth)
4	1 min. $HF:H_2O$ (1:3) dip followed by DI water rinse (oxide etch)
5	10 min. $HCl:H_2O_2:H_2O$ (3:1:1) dip at 90 °C followed by DI water rinse (thin oxide growth)
6	1 min. HF:methanol (1:3) dip without DI water rinse (oxide etch and passivation)
7	Drying under nitrogen

Table 3.1 Silicon substrate cleaning procedure

3.2.2 Deposition

Immediately following cleaning and drying, the samples were transferred to a Kurt J. Lesker AXXIS e-beam evaporation system with a Telemark e-beam power supply and source. A titanium substrate holder was used to secure the samples. The chamber was then pumped down to a base pressure of 5×10^{-7} torr, first with a roughing pump and then a CryoTorr cryogenic pump. Since the evaporation of HfO_2 results in the loss an O atom from the HfO_2 molecule, it must be performed under an oxygen ambient to restore the composition. As such, oxygen was then introduced at the rate of ≈5 sccm from a nozzle placed near the substrate holder. The partial pressure used during deposition was ≈4-5×10^{-5} torr. The pressure of the oxygen reactive gas has an influence on properties of the film including refractive index.[31] For the purposes of this study, both Al_2O_3 and HfO_2 were evaporated under the same oxygen partial pressure. After establishing an oxygen ambient, the substrate was then rotated at 20 RPM and heated to 50 °C to promote uniform adhesion of the evaporated Al_2O_3 and HfO_2.

The evaporation source materials were Al_2O_3 (1.5 mm to 4 mm pieces, 99.99%) from Kurt J. Lesker and sintered HfO_2 pellets (99.9%, excluding Zr, Zr <0.5%) from Alfa Aesar and Kurt J. Lesker placed in carbon crucibles. First, a thin layer of Al_2O_3 of the desired thickness was deposited at ≈0.5 Å/s. Deposition rate and thickness were monitored with a 6 MHz crystal and Sigma software. Then, in-situ, the source was changed to HfO_2, and it was evaporated similarly. Some samples were annealed under a hydrogen ambient, which has been shown to improve the electrical properties of thin-films deposited on Si.[32] These samples were either annealed in-situ in the e-beam system or were transferred ex-situ to an Applied Materials P5000. For samples annealed in the e-

beam, the chamber was first pumped back down to a high vacuum (better than 1×10^{-6} torr). The cryogenic pump valve was then throttled and a flowing hydrogen ambient was formed at 45-50 sccm and a pressure of 4-5×10^{-4} torr. The samples were then annealed at 250-300 °C for 45 min. Annealing in the P5000 was performed at ≈1.0-1.5 torr at a hydrogen flow rate of ≈100 sccm and 250 °C, also for 45 min. Hydrogen was supplied during temperature ramp up and ramp down. Interestingly, while there was a difference between vacuum annealing and hydrogen annealing, there was not a significant difference between in-situ e-beam annealing and ex-situ P5000 annealing despite the hydrogen pressure differences. This is shown in Figure 3.1.

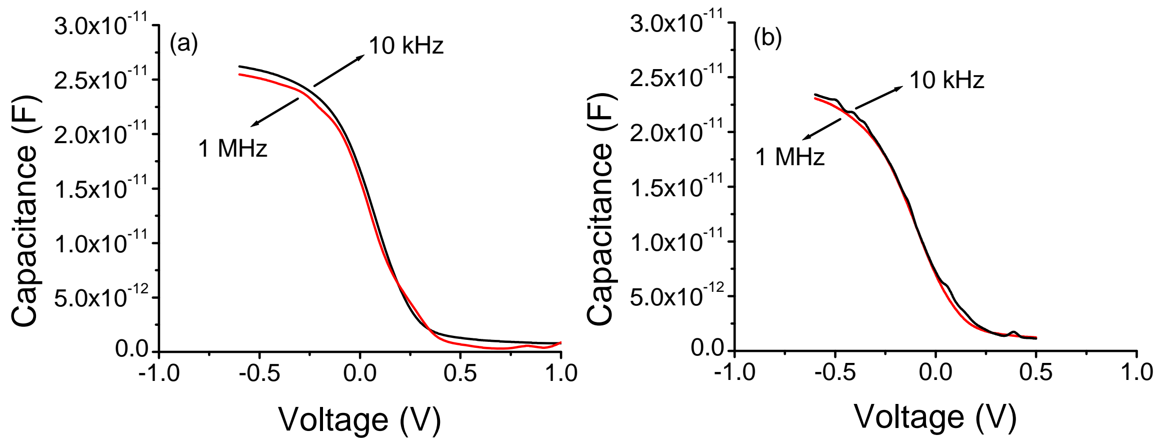

Figure 3.1 Comparison of in-situ e-beam annealing (a) and ex-situ P5000 annealing (b) of a similarly prepared ~20nm Al_2O_3/HfO_2 stack

3.2.3 Metallization

E-beam evaporated titanium was used for all top contacts. The samples were held in a stainless steel holder. A molybdenum shadow mask with 500, 250, 150 and 75 μm diameter apertures was use to pattern the top contacts. 100 – 150 nm of titanium was then evaporated at a high vacuum. Because of the good vacuum under the probestation chuck,

unpolished back side, and moderately low resistivity of the Si used, a metal back contact was not used.

3.3 Characterization

The devices and films were characterized using energy dispersive spectroscopy (EDS), ellipsometry and with LCR and sourcemeters.

3.3.1 Energy Dispersive Spectroscopy

EDS was performed in an Amray 1600T thermionic SEM. For the purposes of this study, a thicker than typical stack was made due to the resolution limits of the beam. Both the Al_2O_3 and HfO_2 were approximately 300 nm in thickness each. The sample was annealed in the e-beam system.

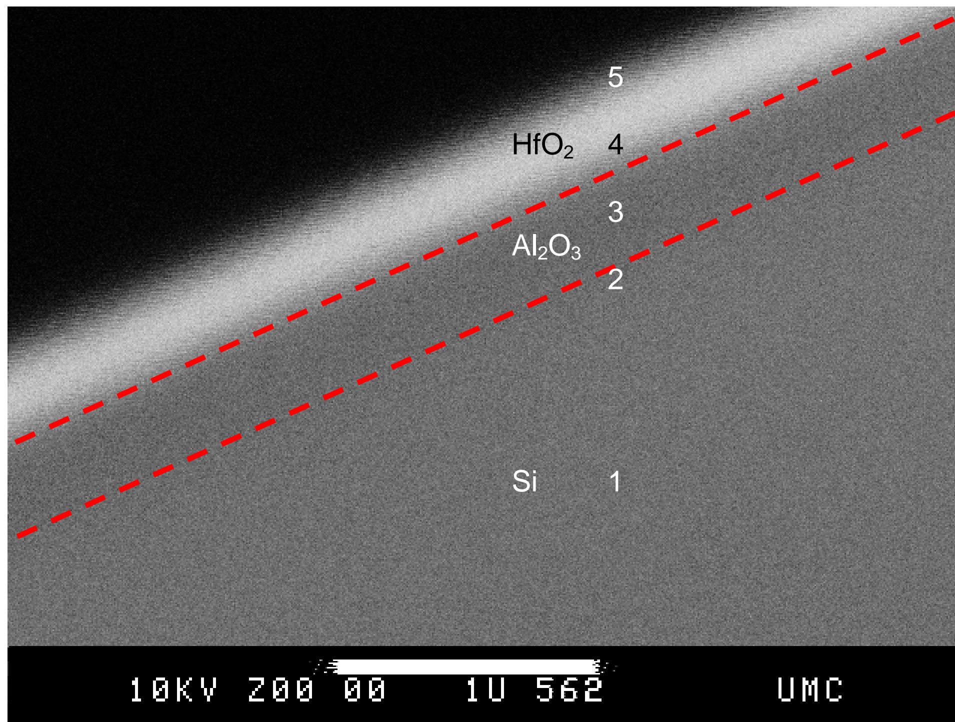

Figure 3.2 Cross-sectional SEM image of the sample taken with the BSE detector in the Amray at 10 kV showing the positions at which the spectra were taken.

Figure 3.2 shows the positions along the cross-section of the sample corresponding to the EDS data in Figure 3.3. The accelerating voltage for both the image and EDS data was 10 kV. The image was taken with a Robinson BSE detector.

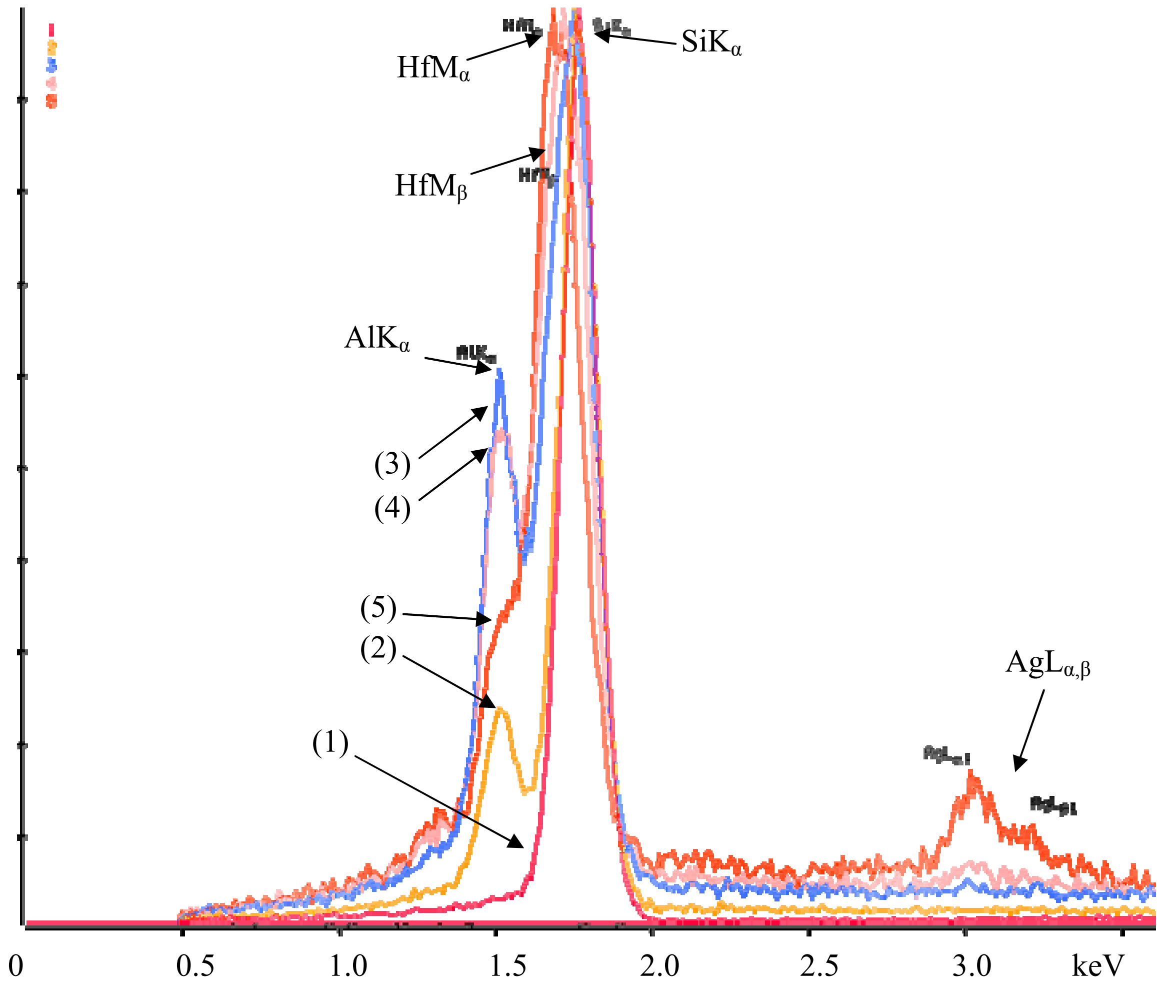

Figure 3.3 Cross-sectional x-ray spectra at 10 kV of annealed sample at the five positions indicated in Figure 3.2. Red (1) is the Si substrate, orange (2) is at the Si:Al_2O_3 interface, blue (3) is in the Al_2O_3, tan (4) is at the Al_2O_3:HfO_2 interface and red-orange (5) is at the edge of the HfO_2. Note the small silver peaks in (5) from the silver paint used to mount the sample to the stub.

3.3.2 Ellipsometry

Because Al_2O_3 and HfO_2 have different refractive index values, a graded Cauchy layer was used to study the refractive index change through the thickness of the sample in the multilayer stacks. For the e-beam evaporated annealed samples, over numerous depositions, the refractive index at 630 nm of HfO_2 films was found to be 1.87±0.008 and for Al_2O_3 films it was found to be 1.66±0.076. For Al_2O_3, the measured refractive index is within the range reported by others for thin-films.[33] The HfO_2 value is somewhat lower than what is reported in literature.[34] However, as mentioned previously, the refractive index is dependent on deposition conditions. Values between reactive e-beam evaporated samples varied very little as evidenced by the fairly small standard deviation. An example of a graded Cauchy depth profile is shown below for some samples, comprised approximately half and half of Al_2O_3 and HfO_2.

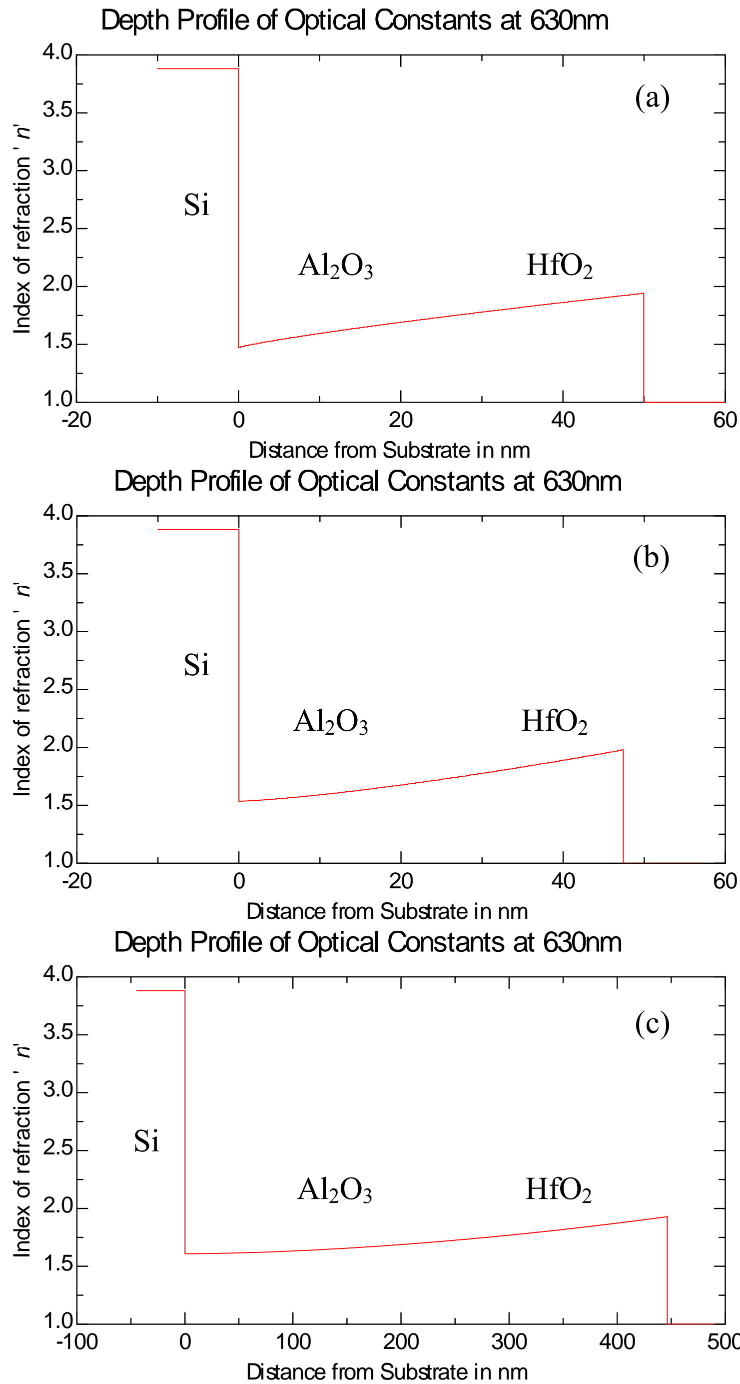

Figure 3.4 Refractive index depth profile for (a) an annealed 50 nm Al_2O_3/HfO_2 sample, (b) an unannealed 48 nm Al_2O_3/HfO_2 sample, and (c) an annealed 450 nm Al_2O_3/HfO_2 sample.

The refractive index does not change suddenly at where the Al_2O_3/HfO_2 interface would be expected, but instead varies gradually through the thickness of the film. This implies

that the interface is not abrupt. Thus, there is the strong possibility that the Al_2O_3 and HfO_2 combine to form hafnium aluminate with varying hafnium and aluminum compositions. The general depth profile shape of the annealed 50 nm sample is different from that of the other two samples in that it is more linear. In the case of the unannealed 48 nm sample, it also follows a smooth transition, but the refractive index is less linear with slightly better defined Al_2O_3 and HfO_2 regions. The annealed 450 nm sample also has more clearly separated Al_2O_3 and HfO_2 layers. Annealing in thinner films likely promotes hafnium aluminate formation over much of the thickness. However, even simply depositing the two dielectrics is enough to form a gradual interface. For thicker films, annealing is still not sufficient to form a hybrid through the entire film.

3.3.3 Electrical Characterization

Electrical characterization was primarily performed with the HP 4284A LCR meter for C-V and G-V measurements and a Keithley 2400 sourcemeter for I-V measurements.

The effect of hydrogen annealing on Al_2O_3/HfO_2 stacks is similar to that of earlier work on HfO_2 stacks alone.[28] That is, the frequency dispersion and accumulation capacitance saturation is improved with hydrogen annealing. The effect of annealing on a 15 nm stack comprised of 4 nm Al_2O_3 and 11 nm HfO_2 is in Figure 3.5.

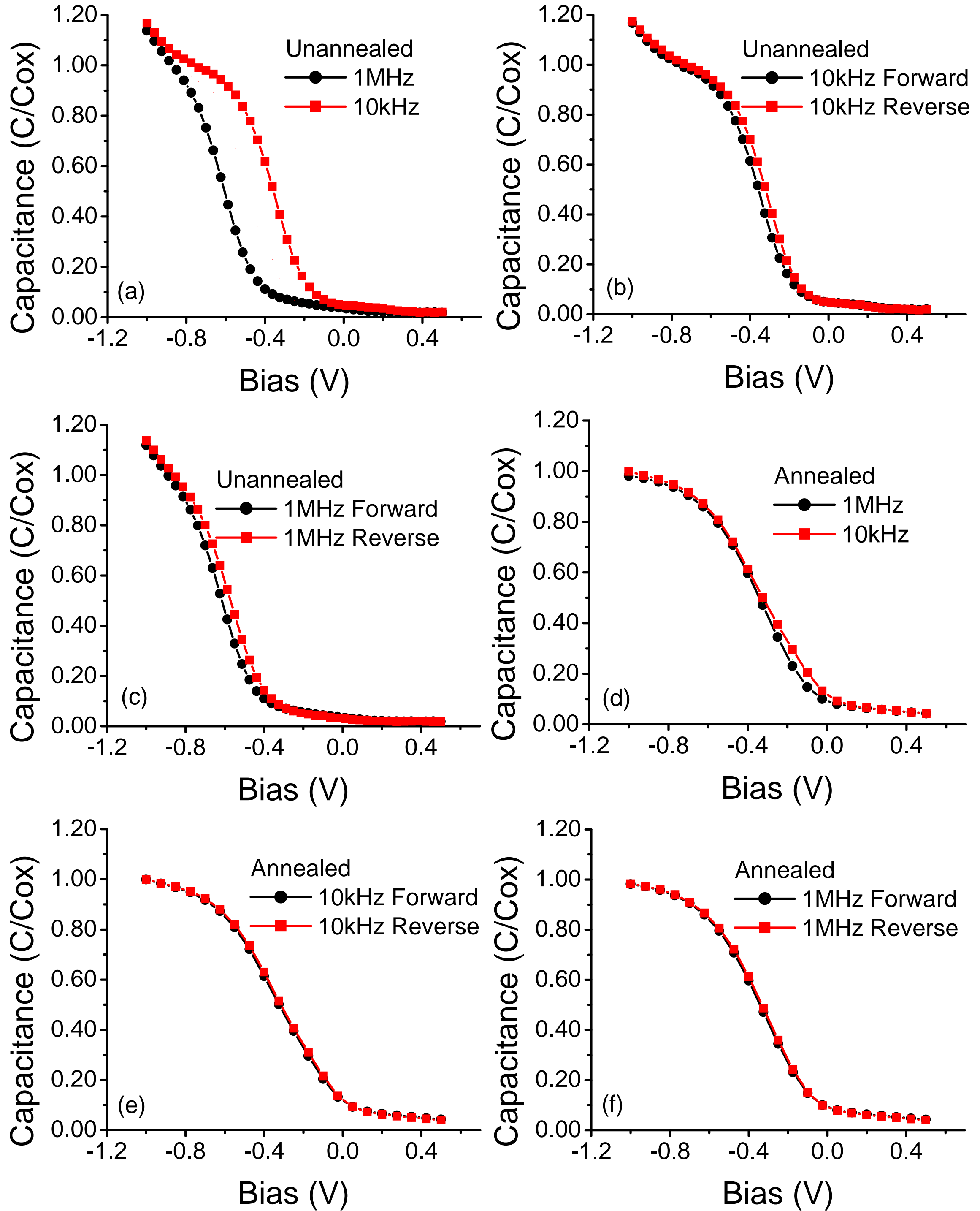

Figure 3.5 Effect of P5000 ex-situ annealing on the 15 nm sample. All plots are normalized. (a) and (d) is a comparison of unannealed and annealed accumulation capacitance saturation. (b) and (c) are the unannealed hysteresis and (e) and (f) are the annealed hysteresis.

As expected, the most significant effects of annealing were the reduction in frequency dispersion and better accumulation capacitance saturation. Both of these are the result of interface state passivation and a more homogenous dielectric after annealing. Interestingly, there is little hysteresis in both the unannealed and annealed samples, though annealing does improve it by a small degree. This is different from what has been reported earlier.[28] It indicates a minimal presence of mobile ionic charges, reaffirming that the cleaning process is effective. There is also a very minimal positive voltage shift in the C-V curves after annealing. The capacitance saturation above also suggests that leakage current density should be reduced. Shown below is the current density before and after annealing over the same bias range as the C-V curves above.

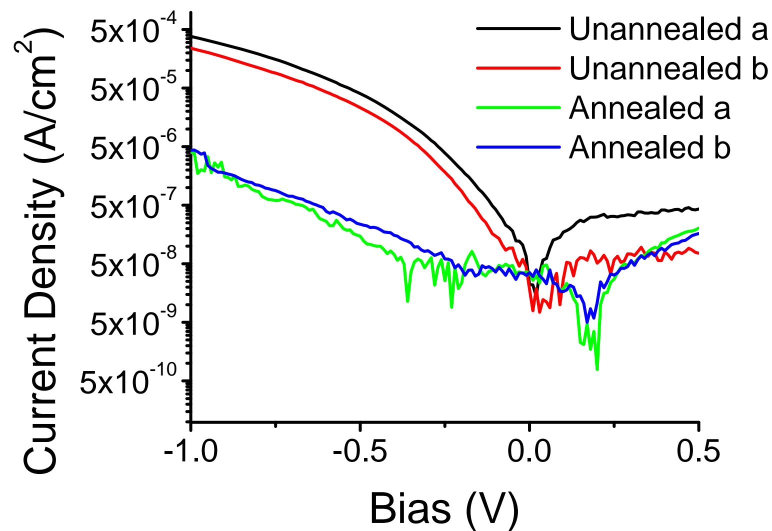

Figure 3.6 Current density of the 15 nm Al_2O_3/HfO_2 sample before and after annealing

As expected, the current density greatly decreases after annealing. A reduction in the current density of nearly two orders of magnitude occurs as a result of annealing. This is attributed to interface state passivation and better homogeneity in the dielectric bulk.

The dielectric constants of these stacks are almost directly related to the ratio of Al_2O_3 to HfO_2. This allows for a tunable compromise between lower leakage currents and better band offsets with a thicker Al_2O_3 layer relative to the HfO_2 and a higher stack capacitance with thicker HfO_2 relative to the Al_2O_3. Unlike using SiO_2 as the intermediate dielectric layer, Al_2O_3 has a dielectric constant two to three times greater, thus increasing overall stack capacitance.

Figure 3.7 shows the relationship between dielectric constant and the composition of the dielectric film. Note that each of the plotted dielectric constant values is the average of samples with nearly identical fractional thicknesses of HfO_2 relative to Al_2O_3.

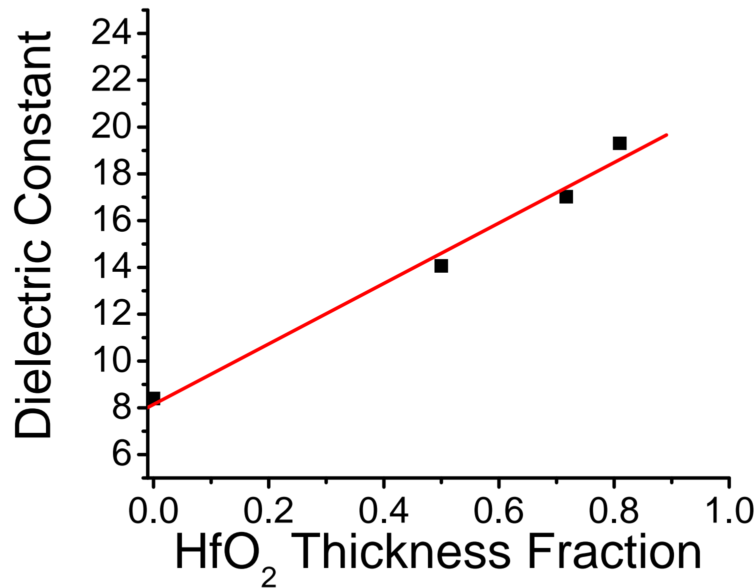

Figure 3.7 Average dielectric constant versus fractional thickness of HfO_2 in an Al_2O_3/HfO_2 stack

The fit of the experimental data points is linear. This would not be expected if the two dielectric layers were modeled as capacitors in parallel. Therefore, it is plausible that after annealing, the films are actually hafnium aluminate ($Hf_xAl_yO_z$) with varying aluminum and hafnium content. EDS measurements in the thermionic SEM lacked the resolution to confirm this. However, EDS measurements in a field emission SEM with

better resolution could be used to conclusively determine the composition of the stacks after annealing. As mentioned prior, the smoothly varying refractive index depth profile also seems to be in agreement with a compound of Al_2O_3 and HfO_2 forming at the interface between the two.

4 Al_2O_3 Dielectric Films with Silver Nanoparticles

4.1 Introduction

Previous efforts to incorporate metal nanoparticles in dielectrics have dealt largely with polymer and mica templates and used electrodeposition to create the metal nanoparticles.[7-9] In this chapter, the results of e-beam evaporated silver incorporated into Al_2O_3 are discussed. Analysis of films with and without silver on both p and p^+-Si are presented. Deposition and annealing were performed in the e-beam system as in the previous chapter.

4.2 Experiment

4.2.1 Fabrication

Two sets of samples were fabricated, a control set without silver nanoparticles and an experimental set with silver nanoparticles. In each set, samples were prepared on both p and p^+-Si (100) with resistivities of 1-10 Ω cm and 0.0030-0.0070 Ω cm, respectively. With the exception of the silver, all samples were prepared identically. The Si substrates were first cleaned with the modified Shiraki process to remove the native oxide and provide a clean, hydrogen passivated surface. After drying under nitrogen, they were immediately transferred to the e-beam evaporation system. On achieving a base pressure of 5×10^{-7} torr, the substrates were heated to 50 °C and oxygen was introduced at 5 sccm and 5×10^{-5} torr. For control samples without silver, 8.73±0.078 nm of Al_2O_3 was then evaporated at 0.5 Å/s. For samples with incorporated silver nanoparticles, Al_2O_3,

approximately 3 nm in thickness, was deposited and the chamber again pumped down to 5×10^{-7} torr. An ultra-thin layer of silver nanoparticles (silver from Kurt J. Lesker, 1/8" dia. 99.9% pellets), less than a nanometer in thickness, were deposited under high vacuum. Oxygen was then reintroduced and ≈3 nm of Al_2O_3 was again evaporated. This process was repeated until the film consisted of three layers of Al_2O_3 with two intermediate layers of silver nanoparticles. Similar to the control sample, the film was 9.60±0.066 nm in total thickness. Thicknesses were again measured with ellipsometry. For the film without silver, the refractive index at 630 nm was found to be 1.67±0.100 and for the sample with silver it was 1.78±0.064. The samples were then annealed, in-situ, in a 45 sccm, 5×10^{-4} torr hydrogen ambient at 250 °C for 45 min, similar to the stacks in the previous chapter. After annealing, a shadow mask was used to pattern the titanium gates on the film. Transmission electron microscope (TEM) images from a JEOL 1200EX verified the presence of silver "nanoislands" or nanoparticles. Figure 4.1 shows a top down view of one layer of silver nanoparticles.

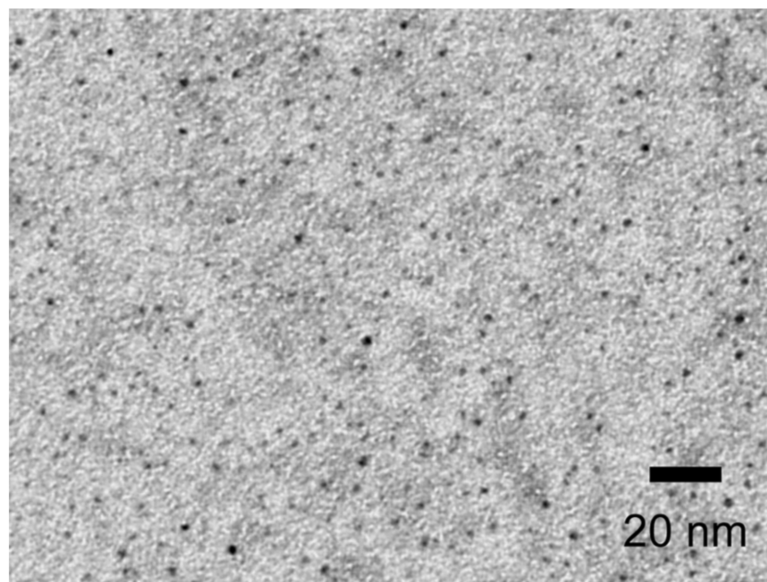

Figure 4.1 Top down TEM image showing one layer of silver nanoparticles in Al_2O_3

Image analysis yielded a mean particle diameter of 2.04±1.23 nm. A size distribution histogram is shown below.

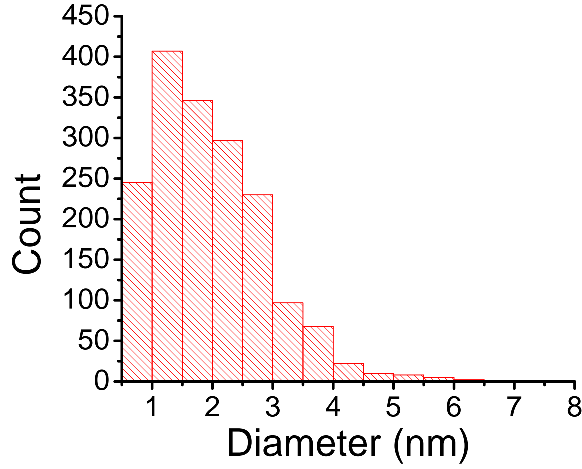

Figure 4.2 Size distribution of the silver nanoparticles

Roy *et al.* and Banerjee *et al.*, have shown that silver particles less than ≈3 nm in diameter exhibit insulating properties.[35,36] Because each Al_2O_3 layer is thin, the silver particles are closely distributed in the direction perpendicular to the plane shown in Figure 4.1. It is this direction that we are most interested in as the applied electric field is present across the thickness of the dielectric layer, from the gate down to the Si.

4.3 Characterization and Analysis

4.3.1 Characterization on p^+-Si

Electrical characterization was performed using the LCR meter. The C-V and G-V measurements were taken from 1 kHz to 1 MHz. The p^+-Si:dielectric:Ti structure was characterized first. From an electrical standpoint, the p^+-Si behaves similar to a metal and the device is thus comparable to a simple metal-insulator-metal (MIM) capacitor. The electric field across the dielectric was kept below the typical breakdown field for Al_2O_3.[37]

The dielectric constant was found based on the geometry of the device, where thickness of the film, area of the gate, and capacitance were known. The dielectric constants are plotted in Figure 4.3. As would be expected, the control sample exhibits fairly minor frequency dependence on p^+-Si. However, the sample with silver nanoparticles exhibits a frequency dependent enhancement of κ. Compared to the control sample, the silver bearing sample shows approximately a doubling in dielectric constant.

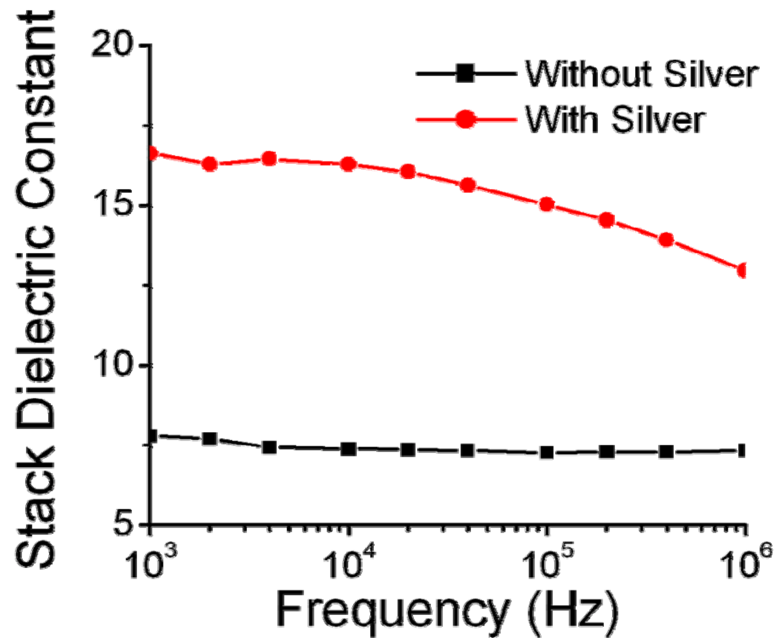

Figure 4.3 Dielectric constants of the two samples with and without silver

In explaining the frequency dependent nature of this permittivity increase, two mechanisms are considered. The first is space charge polarization at the nanoparticle:dielectric interfaces. This is likely most applicable to the particles above the conductor/insulator threshold for silver. Charge accumulation at the heterogeneous nanoparticle:dielectric interfaces will produce an increase in capacitance pronounced most at lower frequencies.[38] The silver nanoparticles are also thought to behave like induced dipoles with a frequency dependent response to the small signal. This has been

observed in nanocomposite dielectrics with embedded metal nanoparticles.[25,39,40] Therefore, the second mechanism is a dipole polarization component. When the small signal frequency is sufficiently lower than the relaxation frequency of the silver nanoparticles, dipole polarization will contribute to the overall permittivity of the nanocomposite. The nanoparticle dipole moments can follow the changes in an adequately low frequency small signal.[38] However, when the small signal frequency approaches the dipole relaxation frequency this ability decreases (typically occurring in the microwave region). It is suggested that dipole polarization is the principal permittivity *enhancing* mechanism in this nanocomposite system, particularly with regards to the smaller nanoparticles below the conduction threshold of silver. Between these two constituent mechanisms, the measured dielectric constant decreases with increasing frequencies. Considering space charge polarization, the dielectric constant drop at lower frequencies (around 1 kHz) is explained. The drop at higher frequencies (around 1 MHz) is then accounted for by dipole polarization. The reduced effectiveness of both then would account for the general decrease in dielectric constant with increasing frequency. It is noted that both of these polarization mechanisms are lossy.

The dissipation factors, *D*, for the control and experimental samples over the measured frequency range are summarized below.

Sample	1 kHz	10 kHz	100 kHz	1 MHz
Without Silver	0.074	0.011	0.007	0.003
With Silver	0.155	0.089	0.115	0.085

Table 4.1 Dissipation factors of the two samples over the tested frequency range

The increase in *D* in the experimental sample is attributed to losses from charge accumulation at the nanoparticle:dielectric interfaces (at lower frequencies) and losses due to the alignment of the nanoparticle dipoles with the varying small signal (at higher frequencies).[38] There is possibly then some conceivable lower and upper frequencies (corresponding to the relaxation frequency) beyond which the *D* should begin to decrease. Due to limitations of the setup, measurements well outside of the reported frequency range were not feasible.

4.3.2 Characterization on p-Si

In addition to the MIM structures, identical films forming metal-insulator-semiconductor (MIS) structures on p-Si were also characterized. I-V measurements on the p-Si:dielectric:Ti structure are shown in below. Leakage of both samples is roughly 10^{-4} A/cm^2 in accumulation (V_{fb} – 0.5 V = -0.70 V with silver and -1.25 V without silver) whereas the leakage of virtually identically processed 5 nm HfO_2 is 10^{-2} A/cm^2.[28] This indicates that the addition of silver does not make the dielectric notably leakier and is in line with similarly fabricated high-κ thin-films.

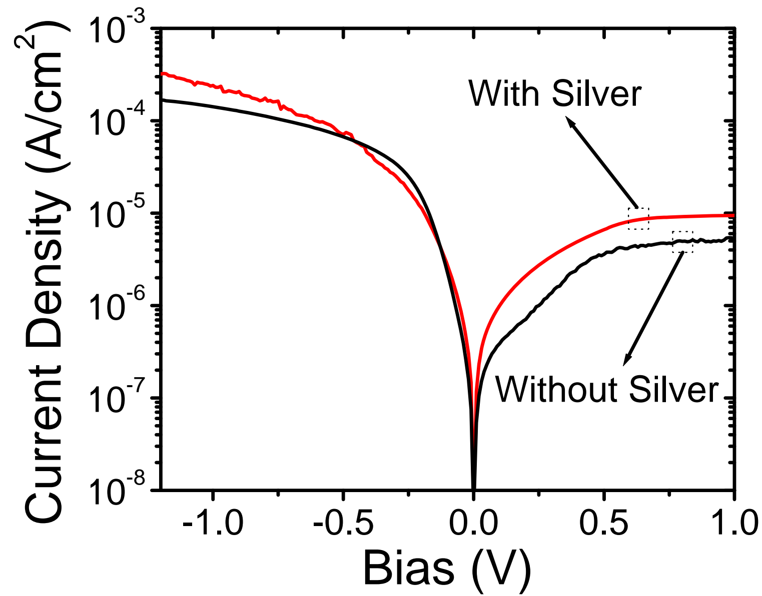

Figure 4.4 Current density plots for both films

While the nanoparticles are within the Al_2O_3 bulk, they are believed to establish locations of quantum confinement (QC) within the nanocomposite dielectric. Because of the close proximity of the first and second silver nanoparticle layers with the Si substrate and gate interfaces respectively, resonant tunneling to and from the QC sites is possible.[41] That is, as the Fermi level crosses the energy level energy level of a nanoparticle, carriers can tunnel through the first Al_2O_3 layer and onto the silver nanoparticles within the oxide. Charge loading and unloading onto the nanoparticles is measured as an increased conductance in the experimental sample as shown in the Figure 4.5 G-V curves.[42] This is also supported by the observed “hump” in the low frequency C-V curves of Figure 4.5, which is the result of resonant tunneling events involving silver nanoparticles.

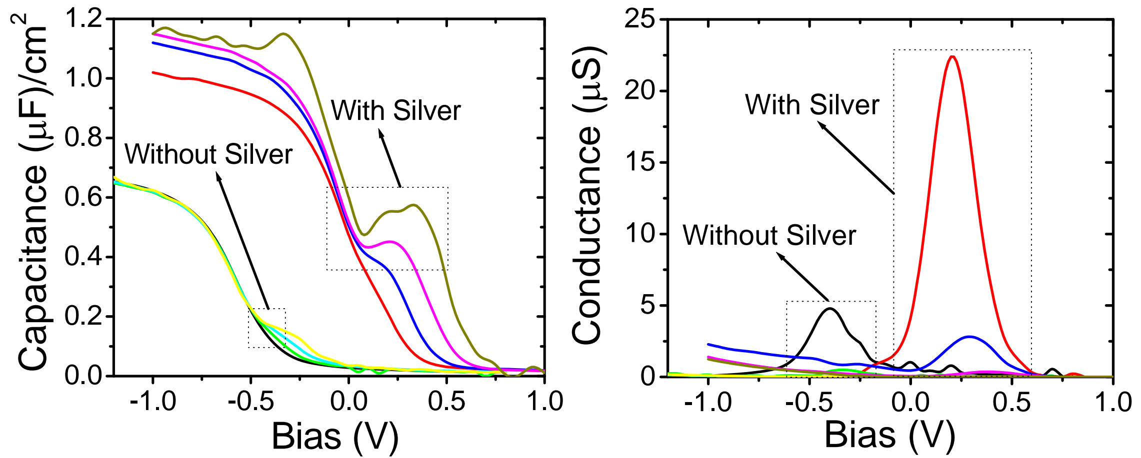

Figure 4.5 Capacitance-voltage and measured conductance-voltage curves on p-Si. The group of four curves on the left is from the control sample and the group of four curves on the right is from the experimental sample. Within each group, frequencies left to right are 1 MHz, 100 kHz, 10 kHz, and 1 kHz.

Others have observed similar behavior in Si nanoparticles embedded in SiO_2.[43] Further supporting this concept, there is a memory effect as shown in Figure 4.6.

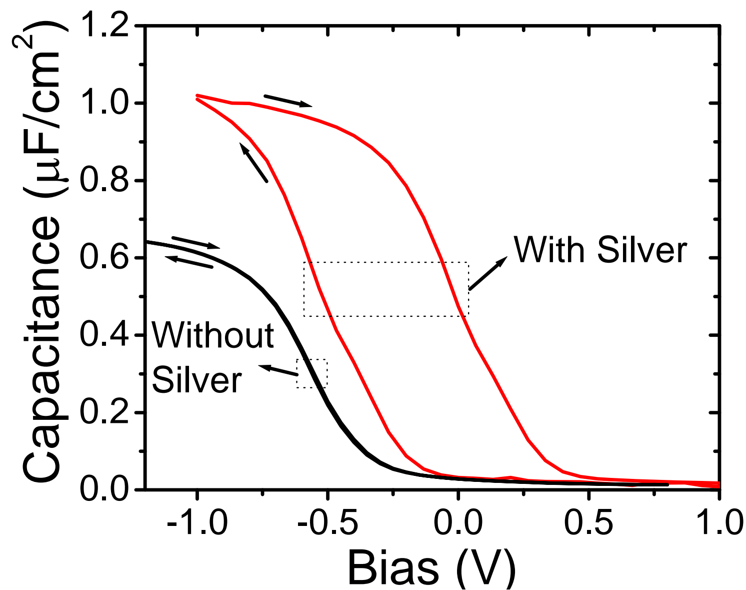

Figure 4.6 Hysteresis at 1 MHz for the control and experimental samples on p-Si

A hysteresis window of approximately 0.5 V is present in the experimental sample whereas virtually none is present in the control sample. Using this hysteresis (Δ =0.5 V) and $N_t = C_{ox}\Delta/q$, the charge density, N_t, is found to be 3.18×10^{12} charges/cm^2. The device thus behaves as a floating gate memory device utilizing the nanoparticles as charge storage locations.[44]

Defect densities are calculated by sweeping the bias from accumulation, through depletion, and into inversion. The series resistance, R_s, values are 720 Ω and 1003 Ω for the control and silver samples, respectively. From chapter 2 G_p/ω and D_{it} are calculated using either the single time constant (STC) model or the continuum model. The appropriate model to use was determined by fitting the experimental G_p/ω points to the theoretical curves for the STC and continuum models. After plotting the experimental points with the theoretical STC and continuum G_p/ω curves, the control sample was found to fit the continuum model from midgap (E_C-E_F ≈0.56 eV) through strong inversion (E_C-E_F ≈0.21 eV) and the silver sample was found to roughly fit the STC model. Selected G_p/ω curves are shown below.

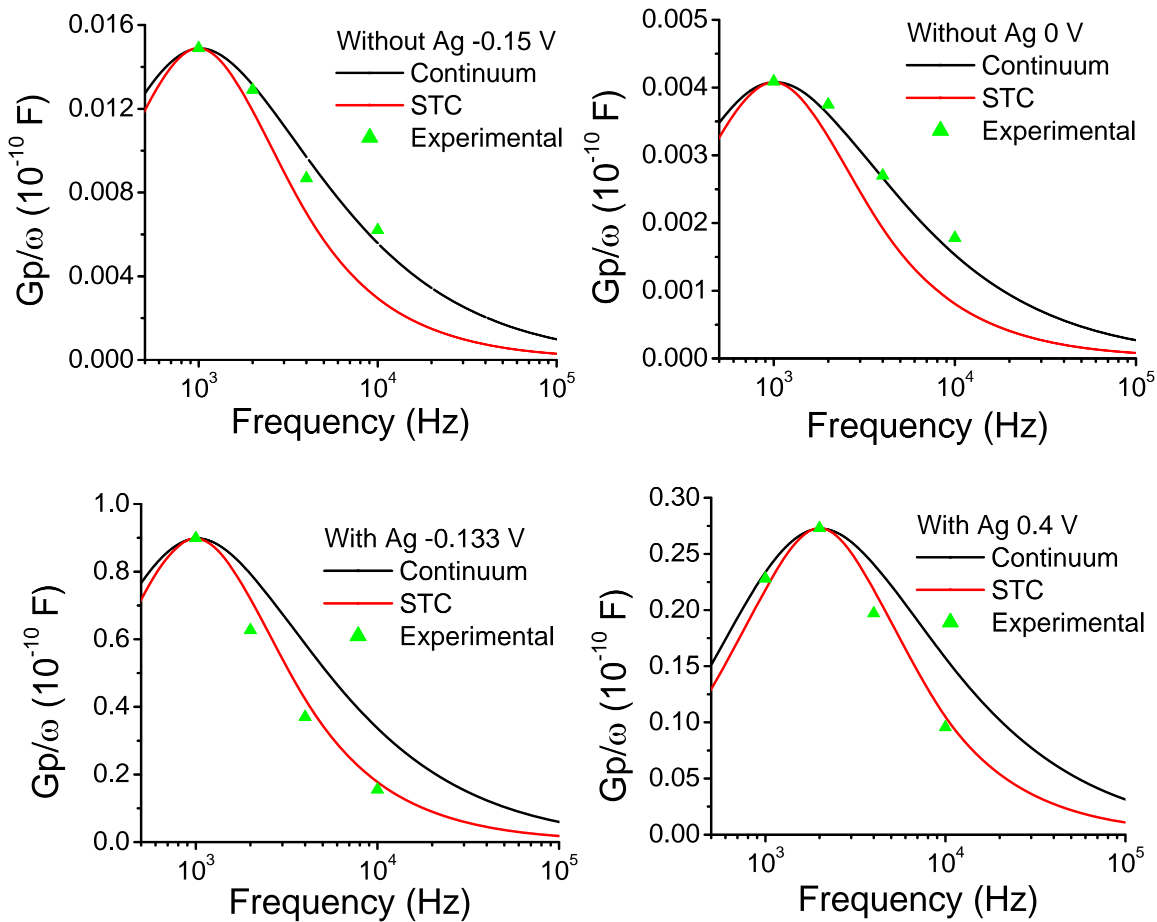

Figure 4.7 Selected G_p/ω plots showing fit of data from samples with and without silver to the continuum and STC models.

The D_{it} values versus energy are plotted in Figure 4.8. From these plots, it is evident that the sample with silver nanoparticles has roughly an order of magnitude increase in apparent interface trap density versus the control sample.

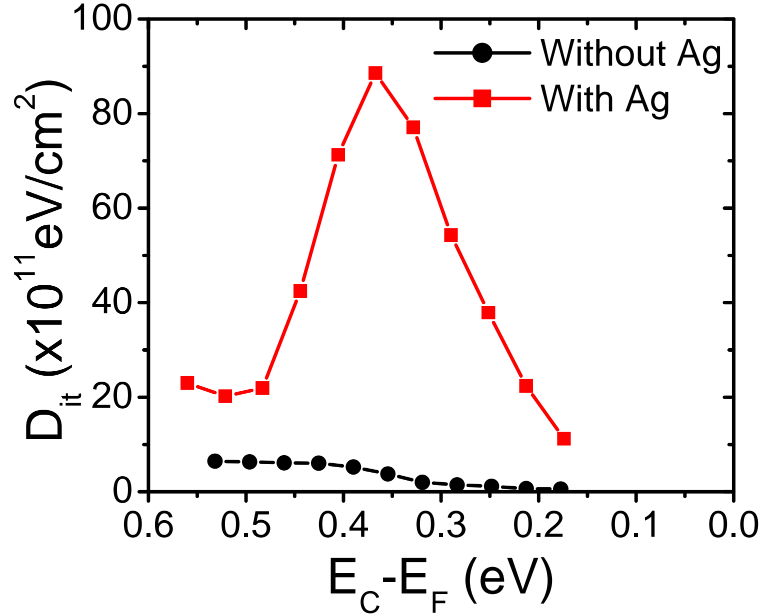

Figure 4.8 Interface defect density (D_{it}) versus energy for both the control sample and the sample with silver nanoparticles

The D_{it} value for the silver sample peaks approximately 0.35 eV from the conduction band edge at 8.86×10^{12} eV/cm^2 with τ =7.96×10^{-5} s. This indicates a maximum of interface defects near this Fermi energy in the bandgap. In comparison, the maximum D_{it} value for the control sample is 6.46×10^{11} eV/cm^2 with τ =3.15×10^{-4} s, near midgap. The apparent increase in D_{it} along with the change from a continuum to STC fit in the sample with silver nanoparticles might suggest that the addition of silver results in a discrete trap level in the Si bandgap at the dielectric:Si interface.

An important point should be made here. Since the silver nanoparticles themselves are not exactly at the interface and because of the low temperature processing, it would seem that the dielectric:Si interface should not be affected. Bearing this in mind, the calculated D_{it} value of the experimental sample should be interpreted with caution. The D_{it} increase is tied to an increase in conductance which may well be the sole result of

the QC behavior described prior. If that is in fact the case, then D_{it} as calculated for the experimental sample would have little meaning. On the other hand it is possible that the interface is somewhat perturbed by the deposition of silver and subsequent annealing. A consequence of this would then be an actual increase in D_{it}. Further study is needed before conclusions can be drawn on this matter.

5 Sputtering of Al_2O_3

5.1 Introduction

Al_2O_3 and HfO_2 sputtering is often performed from an aluminum or hafnium target under either an oxygen ambient or with an post deposition anneal under oxygen.[45,46] This is typically done because of the slow deposition rate of RF sputtering oxides directly. However, with an eye towards co-sputtering Al_2O_3 in the future along with noble metals or other materials, a process for depositing Al_2O_3 thin-films under a typical argon ambient was developed. Substrates were cleaned using the method discussed earlier, but because the sputtering system did not have the capability of flowing hydrogen, in-situ annealing was performed under a high vacuum. A 1 kW RF power source was used.

5.2 Experiment

Upon cleaning and drying the p-Si substrates, they were transferred to the load lock of an AJA sputtering system. The Al_2O_3 was a 3" diameter by 0.25" thick target bonded to a copper backing plate from Kurt J. Lesker (Al_2O_3 99.99%). The main chamber was kept below 5×10^{-8} torr base pressure with a Pfeiffer turbo pump. After transferring the substrates to the main chamber, a plasma strike was performed at a 25 mtorr partial pressure of argon and a RF power of 50 W. Following this, the argon pressure was lowered to 4 mtorr and the RF power was ramped up to 200–300 W for deposition. At 300 W, the deposition rate was approximately 1 nm/min. For samples that

were annealed, immediately following deposition, the chamber was pumped down to a high vacuum and the substrate heated to 250 °C for 45 min.

5.3 Characterization

C-V and I-V characterization was performed on the films. Figure 5.1 shows a comparison between the unannealed and vacuum annealed samples. Thickness of the unannealed sample was 28 nm with a refractive index of 1.24 and for the annealed sample it was 26 nm with a refractive index of 1.53 at 630 nm.

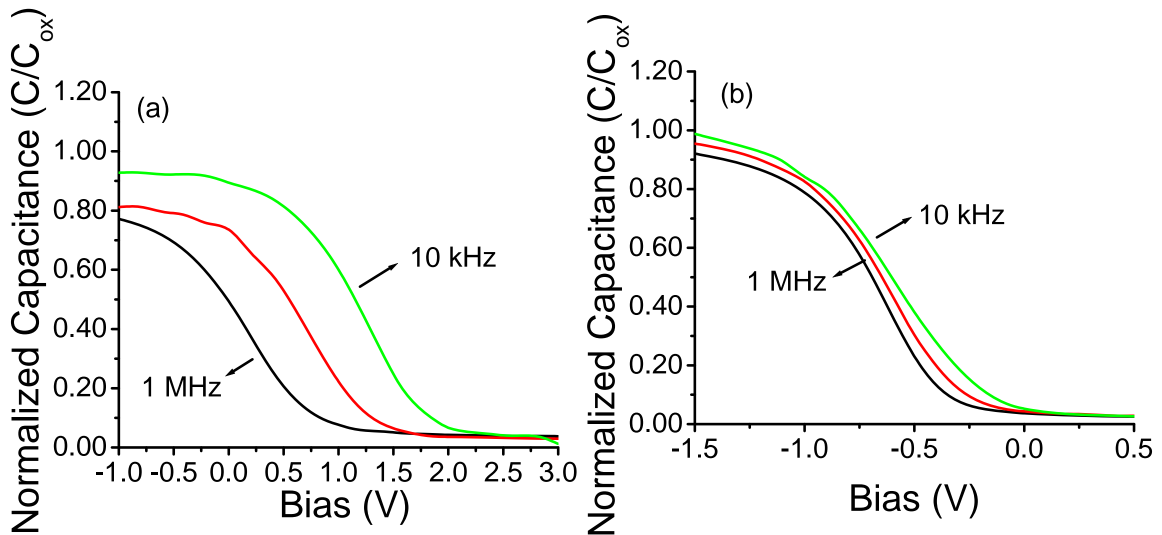

Figure 5.1 Unannealed (a) and vacuum annealed (b) C-V curves of sputtered Al_2O_3 samples

The frequency dispersion is quite large before annealing and even with a vacuum anneal, it is greatly reduced. However, a hydrogen anneal would likely further improve the frequency dispersion. Current density for the annealed sample is given below over the same bias range as in the C-V curve above.

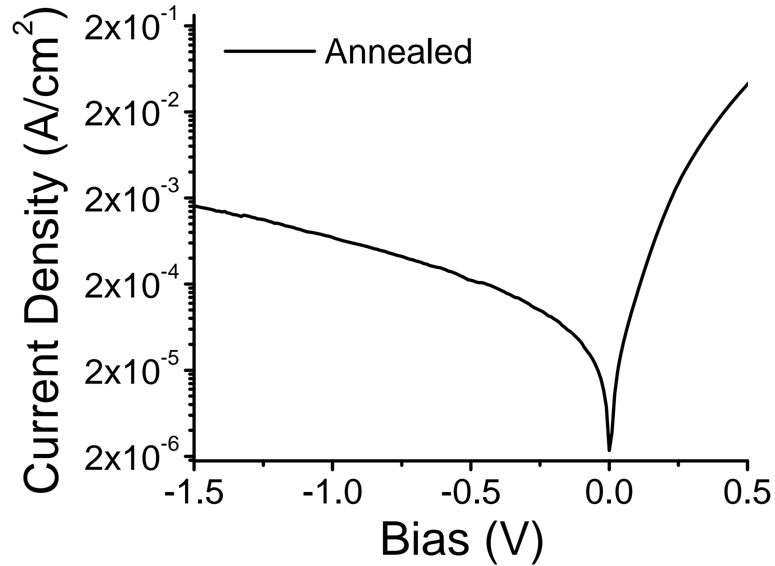

Figure 5.2 Current density of the sputtered Al_2O_3 sample after annealing

The current density here is higher than for the e-beam evaporated stacks. Here again, ex-situ hydrogen annealing should lower leakage currents compared to vacuum annealing. More likely, though, are benefits from sputtering in an oxygen rich ambient or subsequent oxygen annealing. The low refractive index of both the as deposited and annealed samples implies a lower density film compared to the reactive e-beam deposited films. This, along with the I-V data, in turn implies that the purely argon plasma sputtered Al_2O_3 suffers from voids. The sputtering data presented here is limited in scope and was intended mainly to establish the basis for future depositions.

6 Conclusions and Future Work

6.1 Conclusions

The first step of this research was to deposit Al_2O_3 films to provide a possible intermediate dielectric layer between HfO_2 and Si. It was shown that the dielectric constant of the stack could be varied by adjusting the ratio of Al_2O_3 to HfO_2. EDS and ellipsometry measurements were used to verify properties of the dielectric. Electrical measurements revealed that e-beam evaporated stacks with Al_2O_3 have low as deposited hysteresis and that their frequency dispersion can be greatly reduced with hydrogen annealing.

With a process for reactive Al_2O_3 evaporation established, the next step was working on methods to alter properties of the dielectric films using silver nanoparticles. Thin silver layers evaporated between Al_2O_3, forming nanoparticles, revealed that there is a memory effect and an enhancement of the dielectric constant. Most importantly, the technique used for deposition of these films could be readily adapted for use in industry.

Finally, a brief set of experiments to sputter Al_2O_3 under an argon ambient were performed. This could allow other materials, in particular metals, to be co-sputtered to embed nanoparticles into the film with the control and versatility inherent to sputtering. Sputtering or post deposition annealing under an oxidizing ambient might potentially preclude the co-sputtering of certain metals which would react with the oxygen.

6.2 Future Work

The films produced over the course of this research were developed with the intent of them eventually finding use in a device. Industry already has plans for the impending transition to high-κ gate dielectrics. However, the use of metal nanoparticle bearing films in memory devices is a promising application in future devices, as is increased polarizability. There are some improvements that need to be made to these films before they can be utilized in devices.

Reducing the frequency dependence of the dielectric with the silver nanoparticles is one such requirement. Improving particle size variation and distribution might help in this regard. While e-beam evaporation processes may enable this, a process with superior control over deposition, such as sputtering is suggested. Co-sputtering from the metal and dielectric targets simultaneously, with the metal deposition rate set at a small fraction of the dielectric deposition rate is one possible method. Chemical vapor deposition from precursors is another method, but establishing the process and refining it might prove more challenging. As different metals have unique properties such as work functions and process compatibility, it would also be worthwhile to try various other metals. The large work function and inert properties of platinum, for example, might be worth considering. The dielectric medium into which the particles are dispersed could likewise be expanded by trying other common dielectrics such as SiO_2, SiO_xN_y, and especially next generation dielectrics such as HfO_2.

Further, if it would be possible to alter the geometry of the particles and make them more asymmetric, there is some chance that the permittivity enhancement might be more pronounced if the dipole model holds true. Another crucial point to look at in detail

would be the charge transfer and confinement mechanism. Temperature dependent electrical measurements may provide more insight into the nature of these films. Studying these aspects in detail could open up more applications.

Developing three terminal devices using this dielectric would be the most conclusive test. An example of such a device would be a floating gate transistor for memory applications. However, there is information yet to be gained with continued study of the two terminal MOS stack, especially in regards to the programming and polarization behavior. While optimization may dictate a new choice of metal or deposition process, there is a fair amount research being conducted in this direction. After the films have been satisfactorily characterized with two terminal devices, extending them to three terminal devices should be a logical progression.

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