Public Abstract
First Name:Md
Middle Name:Ebney
Last Name:Jalal
Adviser's First Name:Mahmoud
Adviser's Last Name:Almasri
Co-Adviser's First Name:
Co-Adviser's Last Name:
Graduation Term:SP 2014
Department:Electrical Engineering
Degree:MS
Title:Noise Optimization of Amorphous SixGeyO1-x-y Uncooled microbolometer

A detailed investigation of reduction of low-frequency noise voltage power spectral density (PSD) of silicon germanium oxide (SixGeyO1-x-y) uncooled infrared (IR) microbolometers has been performed. The experimental methods used to conduct the research are presented. The noise reduction was achieved by passivating SixGeyO1-x-y with Si3N4 layers and by annealing the devices in vacuum at 200 °C, 250 °C, or 300 °C with different time interval from 1 to 5 hours.
First, uncooled IR microbolometers with a pixel area of 40×40 μm2 were fabricated (by another research team member) on four wafers with different SixGeyO1-x-y compositions while the other layer thicknesses were fixed. The IR sensitive layer was passivated with Si3N4 thin films for the purpose of reducing the noise. Second, the temperature coefficient of resistance (TCR) and the corresponding resistivity (?) of each devices were measured as a function of temperature between 0 ? 70 oC. The measured TCR and resistivity were -3.518/K and 0.763×103 V2/Hz, -2.590/K and 1.170×103 V2/Hz, -3.864/K and 3.573×103 V2/Hz and -3.103 and 0.730×103 V2/Hz for devices from W01, W02, W03 and W04, respectively. The voltage noise PSD was then measured using a bias current between 0.07 - 0.6 μA across many devices from each wafer, with each device given a unique number for the purpose of tracking them. Before annealing, the lowest noise voltage PSD measured at the corner frequency of several devices (W01D21, W02D45, W03D36 and W04D33) from the four fabricated wafers were 7.59×10-15 V2/Hz, 1.89×10-14 V2/Hz,1.82×10-14 V2/Hz, and 2.79×10-14 V2/Hz, at 25 Hz, 12 Hz, 190 Hz, and 160 Hz respectively. The corresponding 1/f-noise coefficients, Kf, were 3.65×10-14, 3.01×10-14, 1.97×10-14, and 2.74×10-13 respectively. To optimize and reduce the measured noise, the same measured devices and others from each wafer were annealed in vacuum (4mTorr) with different time interval from 1 to 5 hours at either 200 oC, or 250 oC, or 300 oC. The measurements demonstrated that the voltage noise PSD was reduced as the annealing time interval was increased to a certain time period, after that the voltage noise PSD started to increase again. For example, the lowest measured noise of each device (W01D21, W03D45 and W04D33) from the four wafers at the corner frequency, after 3h or 4 h time interval, was 1.96×10-14 V2/Hz at 12 Hz, 1.5× 10-14 at 77.5 Hz, 2.11 ×10-14 at 12 Hz, respectively. However, in wafer 02 (02D45), the voltage noise PSD was 1.13× 10-14 V2/Hz at 23 Hz with 1 h period of annealing. Thus, the results demonstrated that the voltage noise PSD of device W04D33 was significantly lowered after annealing at 300 °C for 4 hours. Annealing devices at higher temperature 300 °C reduced the low frequency voltage noise PSD more than that of 200 °C and 250 °C temperature.
The measured Hooge's parameter of the three devices from W04 after annealing were 2.39×10-13 for W04D43 at 200 °C in 2h period, 2.19×10-16 for W04D11 at 250 °C in 3 h period and 1.36×10-14 for W04D33 at 300 °C in 3 h period. Other devices from W01, W02 and W03 the measured Hooge's parameters decreased after annealing. For example, before annealing the noise parameters (?, ? and Kf ) of the device W01D22 were 1.26, 2.24 and 1.44×10-12 which are 0.95, 2.00 and 2.02×10-13 after annealing, and for the device W03D45 the noise parameters were 1.59, 3.71 and 1.19×10-12 but which were seen 1.50, 1.88 and 7.23×10-14 after annealing, respectively. However, annealing of devices reduced the noise parameter Kf. This clearly indicates that annealing the device at higher temperature enabled the reduction of 1/f-noise. The possible reasons for the reduction of voltage noise are the dangling bonds, grain boundary and crystal structure were repaired in sensing layer after heating the devices. Trapping-detraping mechanism stated inside the interfacial oxide was also a potential source of increasing 1/f noise.