Utilizing the size dependent crystallinity, catalytic activity and charge retention characteristics of ultrafine sub-2 nm Pt nanoparticles in electrochemical/electrical systems

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By

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The undersigned, appointed by the dean of the Graduate School, have examined the dissertation entitled

UTILIZING THE SIZE DEPENDENT CRYSTALLINITY, CATALYTIC ACTIVITY AND CHARGE RETENTION CHARACTERISTICS OF ULTRAFINE SUB-2 NM PT NANOPARTICLES IN ELECTROCHEMICAL/ELECTRICAL SYSTEMS

Presented by

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- a candidate for the degree of doctor of philosophy, and hereby certify that, in their opinion, it is worthy of acceptance.

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MOTIVATION

Use of nanoparticles (NPs) instead of the bulk material in catalytic/electrical systems is a growing trend, which has resulted in more efficient catalytic systems and low-power electrical transduction systems. One reason for this growing trend in the area of catalysis is that NPs have high surface-area-to-volume ratios, which can significantly help reducing the material usage, since a lesser amount of the catalytic material is required. Another important factor that should be taken into consideration is that NPs can exhibit strikingly different reactivity and quantum confinement modulated electrical characteristics than their bulk counterparts. Pt NPs are currently employed for a wide variety of catalytic processes and display catalytic activity which depends on both the size and the crystal structure of these NPs. In the sub-2 nm size range, Pt NPs surrounded by dielectrics have also shown evidence of unique charge retention characteristics due to their low self-capacitance and quantum confinement effects. The interplay between Pt's inherent catalytic properties, enhanced activity at nanoscale surfaces, and quantum confinement modulated charge retention characteristics helps tailor these sub-2nm Pt NPs for a multitude of applications – ranging from single electron memory devices to catalysing triiodide reduction at counter electrodes of dye-sensitized solar cells (DSSC). This dissertation aims to explore and discuss the size dependent application of these sub-2nm Pt NPs in certain electrochemical/electrical systems.

As part of this study, the stability of these sub-2 nm Pt NPs on different supporting surfaces was explored to better understand the role of NP size and surface adhesive forces governing the issue of active surface area loss, a notable concern in systems utilizing Pt NPs as catalysts. From an applications standpoint, with the purpose of analysing the effect of charge transfer characteristics and crystallinity of sub-2 nm Pt NPs in driving reaction kinetics, these Pt NPs were

utilized at DSSC counter electrodes order to efficiently realize the triiodide reduction reaction at the counter electrode of DSSCs. While exploring the stability of these sub-2 nm Pt NPs in acidic environments, evidence of size-dependent hydrogen spillover was also observed for these NPs and a correlation between NP size, crystallinity, support characteristics, and hydrogen spillover was explored. While uncapped Pt NPs are utilized for catalytic applications, to take advantage of their size dependent charge trapping characteristics, capped Pt NPs are typically utilized within electronic devices. To explore the electronic properties of these Pt NPs for device applications, these Pt NPs were electrically probed while embedded within a dielectric film. These Pt NP embedded dielectrics (Al_2O_3 in this study) were studied with intended application in non-volatile memory devices and the role of defects at the Pt NP/dielectric interface in determining the resultant device characteristics was also explored.

SCOPE OF THIS DISSERTATION

This dissertation is divided into 5 chapters dealing with the stability and different applications of sub-2nm Pt NPs in electrochemical/electrical systems. **Chapter 1** aims to introduce the readers to the advantages of size dependent NP utilization in various electrochemical/electronic systems and provides an overview of Sub-2 nm Pt NP deposition and their observed size, areal density and evolution of crystallinity explored through HRTEM analysis. **Chapter 2** discusses the stability of these sub-2nm Pt NPs on different supporting surfaces. The stability of these Pt NPs was explored to better understand the role of NP size and surface adhesive forces governing the issue of active surface area loss, a notable concern in the field of fuel cell research. **Chapter 3** discusses the utilization of these sub-2 nm Pt NPs at DSSC counter electrodes in order to efficiently realize the triiodide reduction reaction at the counter electrode of DSSCs. While exploring the stability of these sub-2nm Pt NPs in acidic environments, evidence of size-dependent hydrogen spillover was also observed for these NPs and a correlation between NP size, crystallinity, support characteristics, and hydrogen spillover was also studied, which is discussed in **Chapter 4**. These Pt NPs were further embedded in Al_2O_3 and electrically probed utilizing capacitance-voltage technique with intended application in non-volatile memory devices. The role of traps at the Pt NP/dielectric interface (a function of Pt NP size, areal density and surface coverage) in determining the experimentally observed device characteristics is discussed in **Chapter 5**.

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CHAPTER 1: INTRODUCTION

Supported nanoscale metal NPs have generated a tremendous interest in the catalysis and electronics communities. Their unique properties are directly related to their size, shape, relative areal density on the supporting surface [1-3]. The electronic properties of the metal within the host environment is also of critical importance. For a NP containing only a few hundred atoms, a large fraction of these atoms are located on the surface. Because surface atoms tend to be typically coordinatively unsaturated (a coordinatively saturated transition metal complex has formally 18 outer shell electrons at the central metal atom), there is a large energy associated with this surface [2]. The smaller the nanocrystal, the larger is the contribution of the surface energy to the overall energy of the system. This is especially the case for metal NPs in the sub-2nm range with high specific surface area (an attribute resultant of the high surface to volume atom ratio); as size of these metal NPs decreases, interfaces of these metal NPs with the surrounding environment start playing a bigger role in determining their electrical/catalytic properties. NPs with high surface area supported on different support materials are used extensively as catalysts for chemical transformations [3]. The surface of these NPs plays an important role in their catalytic properties. The surface atoms usually have fewer adjacent coordinate atoms and unsaturated sites or more dangling bonds are chemically more active compared to the bulk atoms [2]. This enhanced activity at the surface can help optimize Pt usage in catalytic processes.

Apart from enhanced catalytic activity, these Pt NPs have also been known to show interesting electronic properties in the sub-2nm Range. It is fairly well established that as the size of metals approaches nanometer length scales, the finite size leads to unique electronic properties. As the electron band becomes discretized due to quantum confinement, bulk electrical

phenomenon expected off metals (like Ohm's law) also ceases being valid [3]. To add a single charge to this metal NC costs energy because a charge carrier is no longer solvated in an effectively infinite medium, as in the case of bulk metals [3]. Apart from the NP size being a major factor determining its electrical properties, the host environment and surface defects can also play a big role in determining its charge retention/transfer characteristics. The imperfection of the particle surface can induce additional electronic states in the band gap, which can act as charge trap centers [3]. The interplay between Pt's inherent catalytic properties, enhanced activity at nanoscale surfaces, and charge retention characteristics helps tailoring these sub-2nm Pt NPs for a multitude of applications – ranging from single electron memory devices to catalysing triiodide reduction at counter electrodes of dye-sensitized solar cells (DSSC). This dissertation aims to discuss/propose the size dependent applications of these sub-2nm Pt NPs in certain electrochemical/electrical systems.

1.1 Overview of sub-2nm Pt NP growth using tilted-target sputtering (TTS)

Throughout this dissertation, exhaustive HRTEM analysis of Pt NPs deposited using TTS on Al_2O_3 coated TEM grids has been utilized as the model system in order to ascertain Pt NP growth characteristics and the size dependent evolution of their crystallinity. This section aims to provide the readers with an overview of the role of sputtering parameters (especially sputtering time) in determining the Pt NP size distribution, areal density and crystallinity.

1.1.1 Pt nanoparticle deposition on Al_2O_3 using the TTS system

An AJA International ATC 2000 magnetron sputtering system (Figure 1) was used for deposition of the Pt NPs on the Al_2O_3 coated holey-carbon TEM grids. The depositions were performed using a 2-inch diameter Pt target (99.99%, Kurt J. Lesker Co.). Before deposition, the chamber was evacuated to 10^{-7} Torr. A pre-conditional sputtering was done for 10 minutes to clean the target surface. During the Pt depositions, the magnetron sputtering system was operated with the following settings: 10 sccm of ultra-high purity Ar gas (99.9995% purity, Matheson Tri-gas, Inc.), 4 mTorr Ar pressure, 30W RF (13.56 MHz) power, ambient temperature (~300 K), 6-inch target to substrate distance, and substrate rotation of 20 rpm. Pt was deposited on Al_2O_3 coated holey-carbon grids for different durations spanning from 5 s to 120 min. All depositions were done utilizing the tilted target sputtering method described in detail in previous publications [4-8]. The set target angle was 23.8° which yielded the best homogeneity in terms of size distribution.

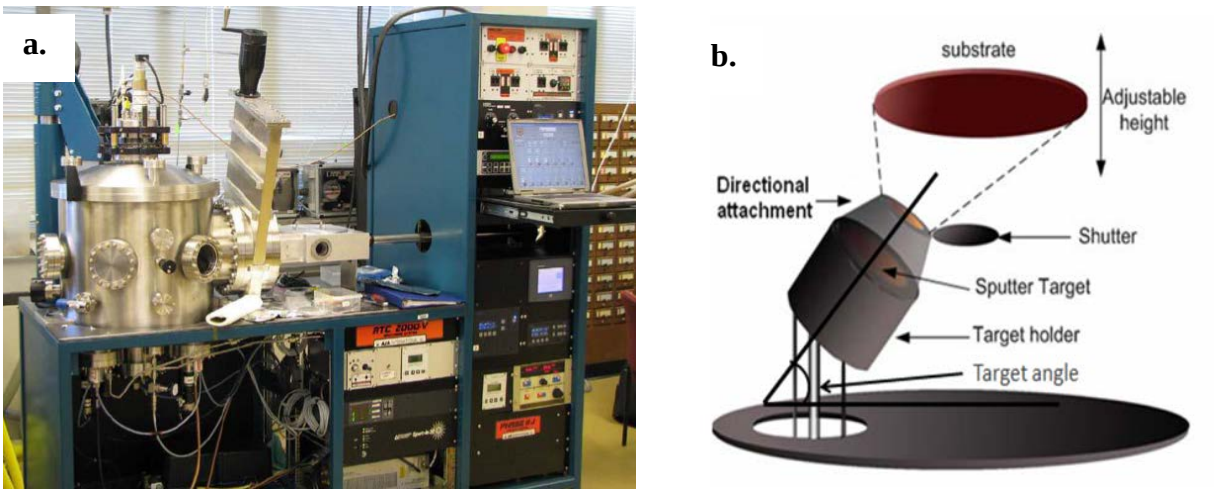


Figure 1: (a) AJA international ATC 2000 magnetron sputtering system Sputtering tool used for NP fabrication and (b) schematic of the TTS system under operation

1.1.2 Pt nanoparticle growth and crystallinity analysis on Al_2O_3 using HRTEM imaging

Exhaustive TEM analysis of Pt NPs was performed using a 5 nm Al_2O_3 coated carbon grid. The Al_2O_3 was deposited using a Kurt J. Lesker AXXIS electron beam evaporator. Details of the Al_2O_3 thin film deposition are available in ref. [5]. The Pt NP images were obtained from a FEI Tecnai F20 200kV high resolution TEM/STEM, more discussion on which is included later in section 1.3.1.The nucleation and growth of metal NPs has been studied in detail by many researchers [9-15]. This section focuses on the growth of Pt NPs prepared by the TTS method using different deposition parameters and shows that the Pt NPs grow two-dimensionally within the deposition time range ($10\ s < t < 30\ s$) and three dimensionally (spherically) in the time range ($30\ s < t < 45\ s$)[16]. Beyond 45 s, particles begin coalescing, and there is a noticeable drop in particle density.

Pt NPs (identified as dark objects in brightfield images of the amorphous support) were observed on an Al_2O_3 surface for short deposition times (up to 60 s). The particle size, areal density and surface coverage of NPs are listed in Table 1. The surface coverage is an indicator of what percentage of the underlying surface are the Pt NPs covering and is essentially a product of the Pt NP 2-D projection area and the areal density. Beyond 60 s of sputtering, these particles begin to coagulate to form islands and thin films. The metal NP growth through coalescence leading to the formation of films is similar to the one described by Beysens et al. al. [9]. HRTEM (i.e. large objective-aperture brightfield electron phase-contrast) images of Pt NPs sputtered on the Al_2O_3 films at different deposition times are shown in Figure 2. It is important to note that Pt NP crystal growth is governed by the growth process of sputtered Pt NPs. The NP growth process is governed by surface energy difference between the incoming Pt atom (surface energy > 2500 dynes/cm) and the substrate [9, 14, 17]. Lattice fringes indicative of crystal periodicity can be seen starting at the

30 s Pt deposition (avg. Pt NP diameter: 1.23 nm). No lattice fringes were detected in HRTEM images of the 10 or 20 s Pt depositions, suggesting Pt nano cluster formation at shorter deposition times. Out of about 298 particles in the 30 s deposition, single {111} or {200} orientation indicative lattice fringes were identified in 29 particles, and cross-fringes in only about 5 particles. The fraction of particles with identified lattice fringes in the longer depositions was greater, i.e. between 40 and 50%.

For instance, in the HRTEM image of a particle on Al_2O_3 with 45 s of Pt sputtering (Figure 3), the spacing between the electron diffraction fringes was approximately 2.2 Å. This fringe spacing corresponds to a {111} lattice plane spacing for a FCC Pt crystal. At longer deposition times, the formation of grain boundaries arising from the coalescence of Pt NPs was observed. The cross-fringe patterns in Figure 3 had spacing & angles characteristic of single-crystal face-cantered-cubic Platinum particles, viewed down the most-open <110>-zone (70-55 degree angles), and less frequently down the <100> direction (90-90 degree angles). No evidence of twinning at longer sputtering times, known to occur for icosahedral Pt NPs as they approach bulk dimensions, was observed in our HRTEM images [18]. In the rare cases when polycrystallinity was evident (~1% of examined grains), it appeared more like high-angle boundaries from the merging of two crystals than the bowtie and butterfly patterns [19, 20] characteristic of icosahedral twins.

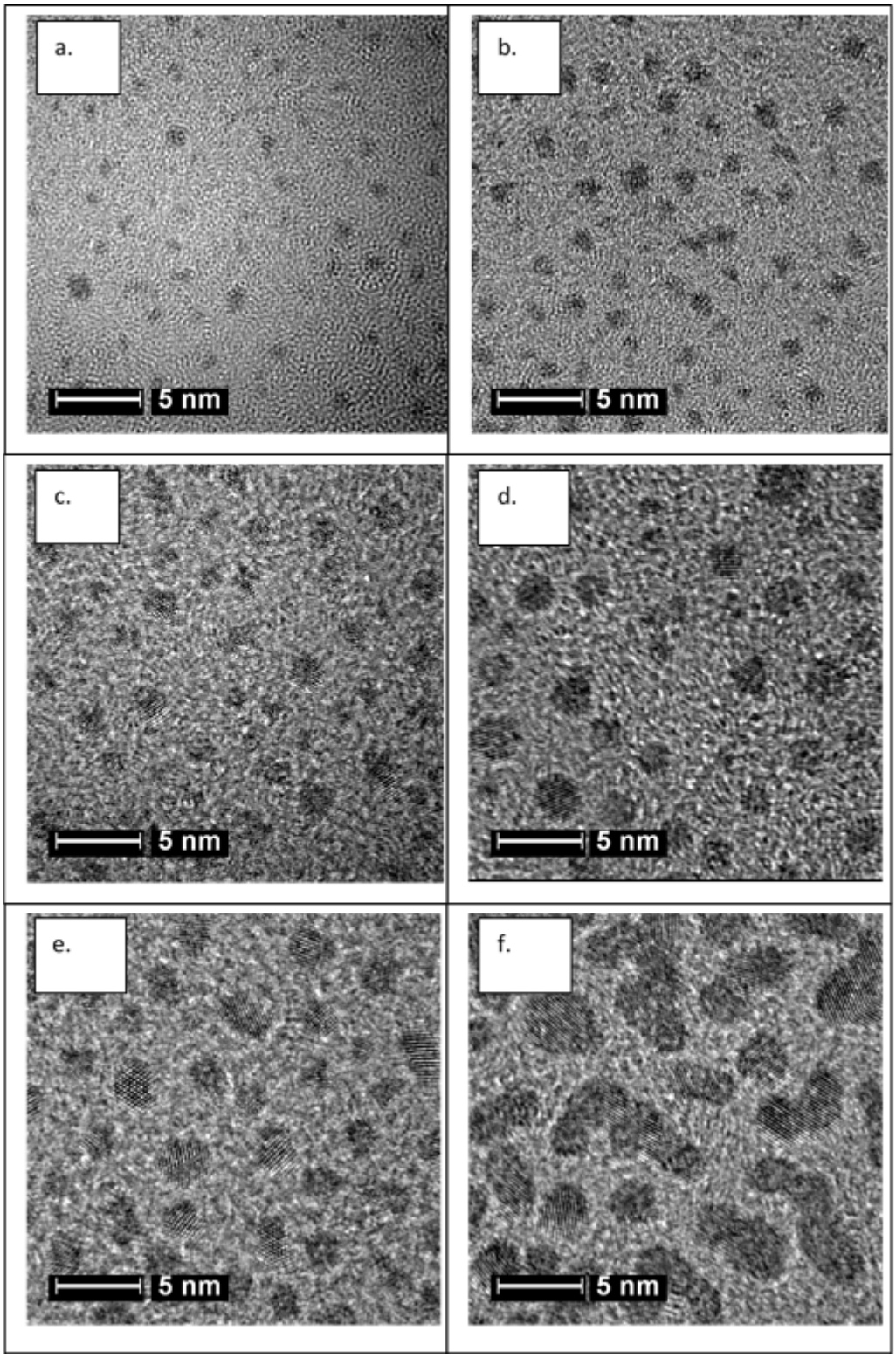


Figure 2: HRTEM images of Pt NPs sputtered at 23.8º target angle for various durations: (a) 10 s, (b) 20 s, (c) 30 s, (d) 45 s, (e) 60 s, and (f) 120 s.

Sputtering Target Angle	Pt deposition time (s)	Mean Particle diameter (nm)	Areal Density ($\times 10^{12}$ cm^{-2})	Surface Coverage (%)
23.8º	**5**	<0.5	<2	-
	10	0.761 (±0.164)	4.71 (±0.42)	2.14
	20	0.926 (±0.239)	5.90 (±0.48)	3.97
	30	1.226 (±0.382)	5.85 (±0.45)	6.90
	45	1.564 (±0.422)	5.92 (±0.52)	11.37
	120	agglomeration	agglomeration	
38.8º	**20**	0.73 (±0.19)	10.92 (±0.62)	4.46

Table 1: Pt NP size distribution, areal density and surface coverage at a sputtering power of 30W at variant deposition times and target angles

FCC growth of Pt NPs is very common in vapour phase metal growth [21-24]. The obtained HRTEM images confirmed nearly equidimensional FCC Pt NPs. It is well accepted that the equilibrium structure for a FCC metal grown in vacuum conditions is a Wulff polyhedron, i.e., a truncated octahedron (which consists of eight hexagonal <111> facets and six square <100> facets) [25-27]. Although truncation of the usual tetrahedral structure composed solely of <111> facets introduces a relatively high energy <100> facet, it helps generate a more spherical structure which further helps minimize the surface energy [25, 27]. This is especially the case of small NPs where surface to bulk atom ratio is larger. Theoretically, it has been shown that for similar FCC metals such as Rh and Pd clusters, the truncated octahedral is metastable and slightly distorted [28]. Strong faceting is not apparent in our experimental images, and preliminary comparison of observed shapes with simulated HRTEM images of variously-shaped particles in a comparably-thick amorphous support suggests that faceting, if present, would show up in the images. This is a topic for future work. Regardless of particle morphology, it's likely that the strong interaction of Pt NPs with surface defects (present in Al_2O_3 films) helps stabilize the resulting surface configuration. In the size-range below 2 nm, where a sizeable fraction of the Pt atoms are on the

surface, these interactions could also prevent Pt crystallization. Our inability to detect crystal periodicities for such particles in 10 and 20 second durations does not prove that those periodicities are absent, since scattering from the Al_2O_3 support might swamp the periodicity-signal. However, lattice-fringe visibility models [29, 30] suggest that for randomly-oriented particles, both (i) the single/cross fringe ratio and (ii) the fraction of particles which show no lattice fringes *independently* determine the periodicity-signal to diffuse-scattering cut-off. Since only the latter fraction (ii) will be increased if a subset of non-crystalline particles has been added to the collection, particles whose size is large enough to allow periodicity-detection in a given support film (as in the 30 second duration specimens described here) may be used to detect addition of a subset of non-crystalline particles, if measurement protocols are carefully defined. The numbers for single/cross fringe-ratio and fraction-crystalline reported above suggest that a subset may be non-crystalline, but this too is a topic for future work.

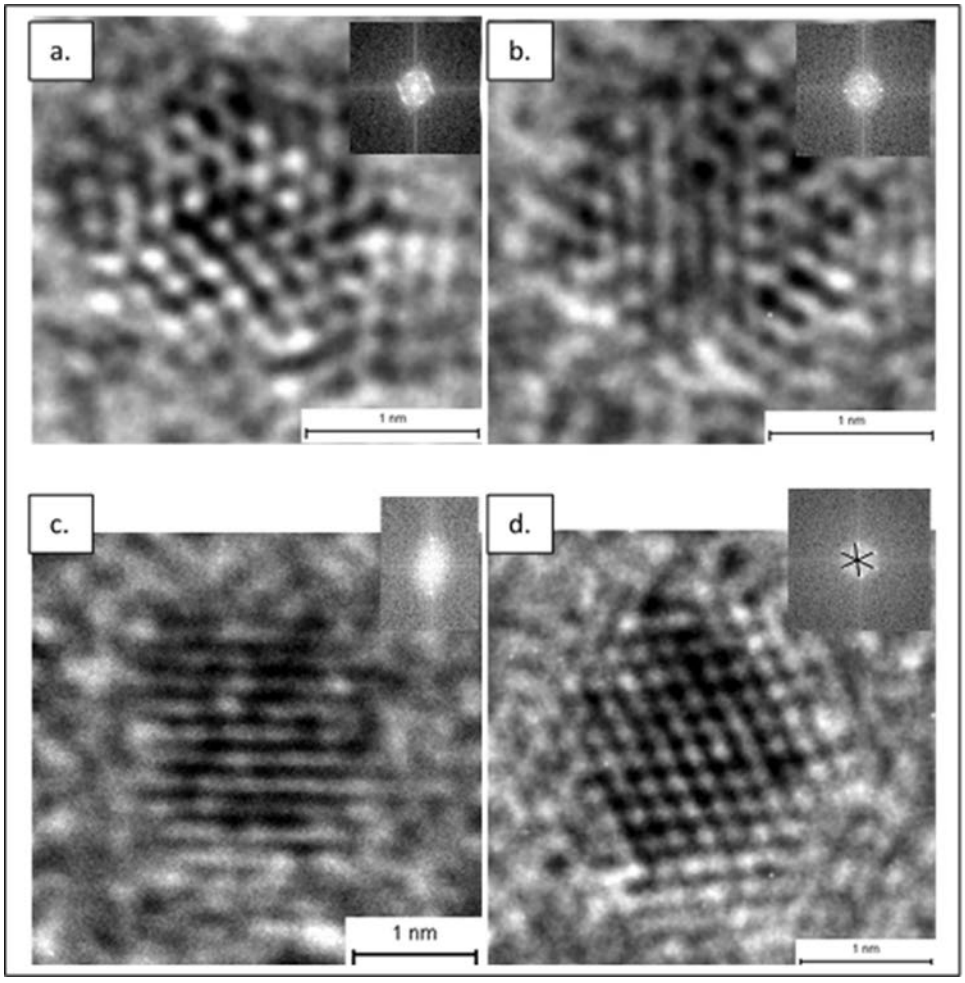


Figure 3: HRTEM images of Pt NPs prepared by sputtering at 23.8º target angle onto Al_2O_3 alongside their corresponding FFT patterns (inset) for (a, b) 30 s and (c, d) 45 s Pt sputtering. The corresponding FFT patterns represent an FCC crystal along the <110> zone axis.

1.1.3. Calculating Pt NP characteristics

TEM images of Pt NPs for different sputter times are in Figure 4. It is observed that particles within a certain deposition time range (30 sec – 60 sec) are spherical in nature and the average volume of an individual particle is given by

$$V_{particle} = (4/3)\ \pi\ (d/2)^3 \quad (1)$$

where d is the mean *observed* diameter of the particle.

The number of Pt atoms present in a given particle (n) can be estimated using the formula

$$n = f\ (V_{particle}/V_{Pt\text{-}atom}) \quad (2)$$

where $V_{Pt\text{-}atom}$ is the volume of an individual Pt atom (atomic radius 139pm [31]) and f is the "packing fraction" that depends on the crystalline structure of the particles (e.g. $f = 0.74$ for Face Centered Cubic (FCC); and $f = 0.68$ for Body Centered Cubic (BCC)).[32] Given the low values that were obtained for the number of atoms per particle (~50, or lower) and based on TEM analysis, it was concluded that at lower deposition times (t < 30sec) the particles are present as non-crystalline aggregates. However, for calculating the Pt loading for crystalline Pt NPs (t > 30sec), the packing fraction for FCC crystals was used since Pt naturally forms FCC crystals.[33] The amount (mass) of Pt present per unit surface area (the Pt loading) is then calculated as

$$\text{Pt loading} = \rho_{Pt}\ N_p\ \langle V_{particle} \rangle \quad (3)$$

where ρ_{Pt} is the density of Pt (21.45 g/cm^3) [34], N_p is the average particle density and $V_{particle}$ is the average particle volume. Since the value of density used is that for FCC Pt, the packing fraction

does not have to explicitly taken into account for this calculation. The nominal thickness ($\delta_{nominal}$) of the film is given as

$$\delta_{nominal} = N_p \, V_{particle} \quad (4)$$

The NP surface area per unit mass of Pt is obtained as

$$\text{Pt NP surface area} = (4 \pi (d/2)^2) / (4/3 \pi (d/2)^3 \rho_{Pt}) \quad (5)$$

For a uniform Pt film (such as a 50nm film used in current DSSCs), the Pt loading is calculated by multiplying the film thickness (δ) by the density of Pt (ρ_{Pt}). For a 50 nm film, the loading is calculated to be 107.25 μg cm^{-2}, and for a 2 nm film used previously by some researchers for DSSC counter electrodes, [35-40] the Pt loading was calculated to be 4.29 μg cm^{-2}. Dividing this Pt loading by that for a 50 nm, or 2 nm Pt film yields the relative Pt loadings. The assumption that the Pt is present in the form of spheres no longer holds true for longer durations of deposition where particles coalesce to form elongated worm-like islands, and hence certain quantities are not evaluated for the 120 sec deposition. It is understood that while applying a spherical NP model, the calculated surface area might be an over-approximation over the real surface area as a certain part of the NP surface area would not be accessible to reactants due to its strong bonding and close proximity to the underlying substrate.

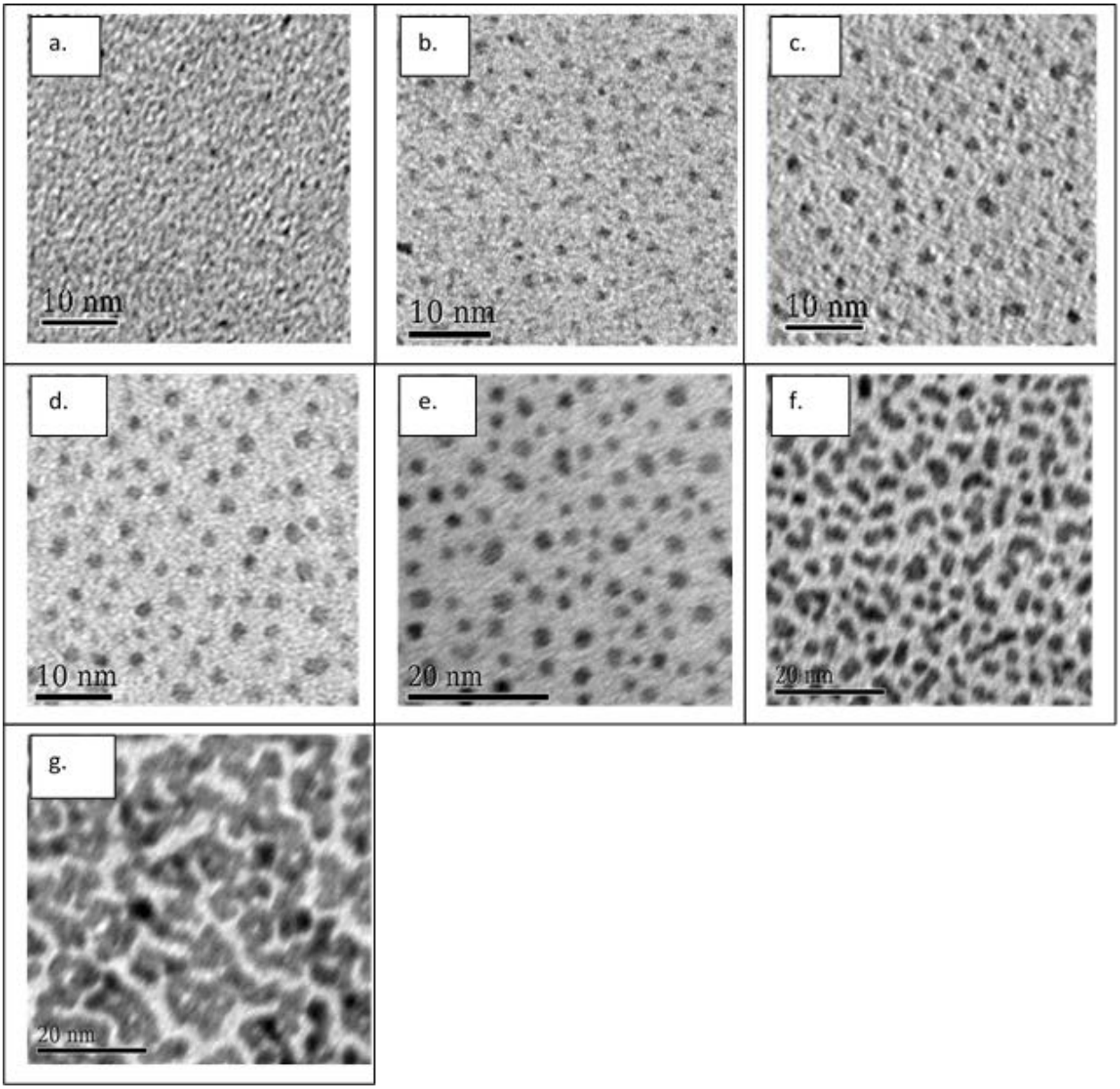


Figure 4: Representative TEM images of Pt NPs sputtered for different times: (a) 10 s, (b) 20 s, (c) 30 s, (d) 45 s, (e) 60 s, (f) 120 s, and (g) 5 min.

1.1.3. Experimental prediction of nominal thickness of sputtered Pt

An Agilent 5500 AFM system was used to measure the average thicknesses at three different regions for Pt deposition times of 20 min, 30 min, 50 min and 90 min. Assuming a constant deposition rate, the nominal thickness should follow a linear path with respect to deposition time. The theoretically calculated nominal thickness for the 30 sec and 45 sec Pt deposition was included

in the linear fit as spherical growth of the Pt NPs was predicted by Ramalingam et al [16]. The fitted linear curve of the data is displayed in Figure 5. From the plot, the fitted data yielded the following linear equation –

$$Y = (\mathbf{m} \pm 1.64em)\, X + (\mathbf{c} \pm 1.64ec) \text{ (for 90\% confidence interval)} \quad (6)$$

where X is the deposition time in sec, Y is the nominal thickness in nm, **m** is the slope, *em* is the standard deviation of the slope, **c** is the Y intercept and *ec* is the standard deviation of the Y intercept. Here, the slope is 7.85×10^{-3} nm s^{-1}, the standard deviation of the slope is 2.1×10^{-4} nm s^{-1}. Also, the Y intercept is -0.193 nm and the standard deviation on the Y intercept is 0.061 nm. Combined, the ranges for the 90% confidence interval can be calculated to be: 7.502×10^{-3} nm s^{-1} < $\mathbf{m} \pm em$ < 8.198×10^{-3} nm s^{-1} and -0.2927 nm < $\mathbf{c} \pm ec$ < -0.0927 nm. Considering these ranges for the slope and the intercept, the nominal thickness range for any deposition times can be predicted within a 90 % confidence interval.

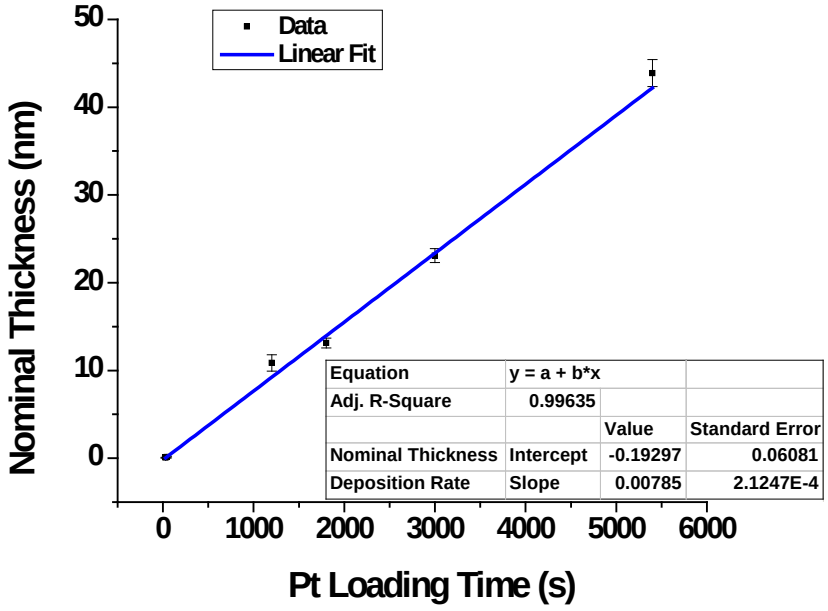


Figure 5: Linear fit of the experimental nominal thicknesses

1.2 Applications of sub-2nm Pt NPs in Electrochemical/Electrical systems

In order to realize the applicability of the fabricated Pt NPs in the sub-2nm range, their stability on different surfaces in harsh environments is a pressing issue. The stability of these sub-2nm Pt NPs was explored to better understand the role of NP size and surface adhesive forces governing the issue of active surface area loss. Typically, Pt NPs immobilized on a support tend to undergo the phenomena of dissolution and coarsening leading to loss in effective surface area which undermines the long-term applicability of these supported NPs. Electron beam-induced coarsening and potentiodynamic cycling in acidic solutions was utilized to study the size-dependent and support-dependent stability of these Pt NPs. Here, a direct evidence of a correlation between Pt NP coarsening on supporting surfaces and their different surface energies was observed

under prolonged e-beam exposure through HRTEM imaging. Utilizing potentiodynamic cycling, it was also observed that crystalline Pt NPs above a mean size of 1.5 nm diameter shows exceptional stability regardless of supporting surface, meanwhile, sub-nm Pt NPs on few layer graphene (FLG) support show better stability properties compared to those deposited on fluorine-doped tin oxide (FTO) support.

From an applications standpoint, Pt NP coated FTO electrodes were utilized at the counter electrodes of DSSCs with the goal of optimizing Pt loading. As part of this study analysing the effect of charge transfer characteristics and crystallinity of sub-2nm Pt NPs in driving reaction kinetics, these Pt NPs were utilized in order to efficiently realize the triiodide reduction reaction which occurs at the DSSC counter electrode. Combination of cyclic voltammetry (CV) and impedance spectroscopy analysis confirmed the higher electrocatalytic activities of sputter-deposited crystalline Pt NPs (1–2 nm) compared with either sub-nanometre Pt clusters or a continuous Pt thin films. While the low catalytic activity and DSSC performance of Pt clusters smaller in size than 1 nm was believed to arise from their non-crystalline nature and charge-trapping attributes, the high catalytic performance of larger Pt NPs in the 1–2 nm regime was attributed to their well-defined crystallinity and fast electron transfer kinetics.

While exploring the stability of these sub-2nm Pt NPs in acidic environments, evidence of size-dependent hydrogen spillover was also observed for these NPs and a correlation between NP size, crystallinity, support characteristics, and hydrogen spillover was also studied. Hydrogen generation and storage is an essential component in the increasingly important field of energy storage. Electrochemical generation of Hydrogen atoms at the surface of Pt like metals at select potentials is a widely accepted phenomenon. However, moving these adsorbed Hydrogen atoms to high surface area support systems for storage is an issue. This study reported spillover of these

adsorbed Hydrogen atoms to the supporting structure for sub-2 nm Pt NPs sputtered on Fluorine Doped Tin Oxide (FTO) and on few layer graphene (FLG) supports. Evidence of C-H bonds formed on the FLG surface due to H spillover from 0.9 nm Pt NPs was also confirmed through XPS analysis.

To explore the electronic properties of TTS deposited sub-2nm Pt NPs for device applications, these Pt NPs were electrically probed while embedded within a dielectric film. These Pt NP embedded dielectrics (Al_2O_3 in this study) were studied with intended application in non-volatile memory devices and the role of traps at the Pt NP/dielectric interface in determining the resultant device characteristics was also explored.

1.3 Overview of primary methods utilized to probe representative Pt nanoparticle signatures

1.3.1 High Resolution Transmission Electron Microscopy

All structural and morphological investigations of Pt NPs in this work were carried out with high-resolution transmission electron microscope (HRTEM). A TEM is a special kind of electron microscope specifically designed for imaging of nanoscale objects.

The Rayleigh criterion defines the resolution of light microscope (δ) as:

$$\delta = \frac{0.61\lambda}{\mu \sin \beta} \qquad (7)$$

where λ is the wavelength of the radiation, μ is the refractive index of the view medium and β is the semi-angle of collection of the magnifying lens. The variable of refractive index and semi-angle is small, thus the resolution of light microscopes is mainly decided by the wavelength of the radiation source (photons). In contrast to other microscopes the electrons in TEM pass through and interact with atoms of the sample. Based on wave-particle duality, similar to the photon, the electron has some wave-like properties. In a TEM, If an electron (mass m_o) is accelerated by an electrostatic potential drop eU, the electron wavelength can be described as:

$$\lambda = \frac{h}{\sqrt{2m_0 eU(1+\frac{eU}{2m_0c^2})}} \qquad (8)$$

For high energy electron beams, the resolution of electron microscope is much better than that of light microscope. For example, for 100keV potential, the wavelength of the electron can be calculated to be 0.0037nm, which is much smaller than that for photons utilized in light microscopes. Due to interaction with the sample being imaged, the incident electrons are scattered. The final image is very complicated interference pattern of incident and diffracted beams. With state-of-the-art TEM microscopes it is possible to achieve resolution as small as 0.08 – 0.05 nm.

The principal setup of TEM is similar to one of light microscope. The image of the sample is then magnified by means of projection lenses and represented on a screen. In TEM, electromagnetic lenses are used instead of glass lenses to guide the electron beam through the microscope. The projection system of microscope consists of intermediate lens and projection lenses. The HRTEM system utilized in this study and a comparison between the components and workings of a light based and electron based microscope can be seen in Figure 6. In a TEM, by changing the strength (i.e. the focal distance) of the intermediate lens it's possible to switch

between diffraction and imaging modes. In case of HRTEM the highest magnification can be as high as 10^6 or even higher, where the final image is recorded with a charged coupled device (CCD).

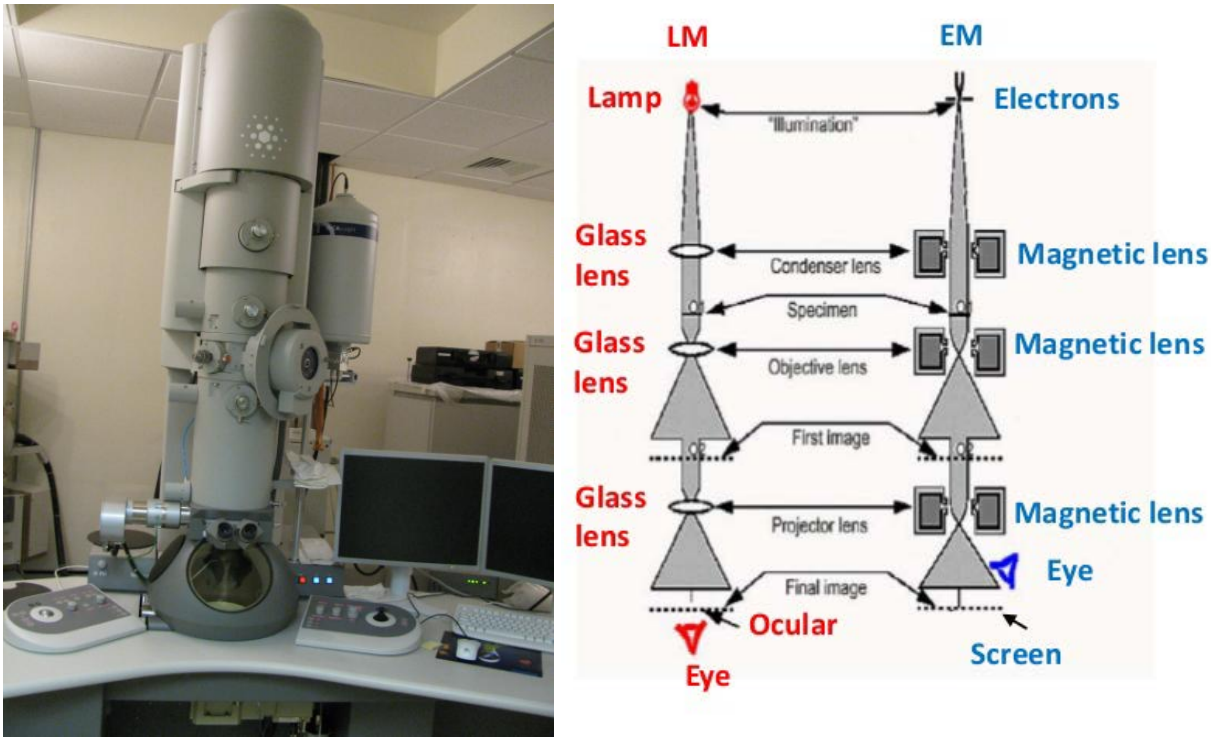


Figure 6: Left – Image of the FEI Tecnai F20 is a 200kV field emission gun (FEG) high resolution TEM utilized in this work (Source: http://amcl.mst.edu/electron/tecnaif20stemtem/) ; Right - Schematics comparing the internal workings of a light microscope (LM) and a transmission electron microscope (EM) setup (Source - http://www.slideshare.net/DiegoRamos5/microscopy-15336091)

1.3.2 Cyclic Voltammetry

Cyclic Voltammetry (CV) is an electrochemical technique which measures the current that develops in an electrochemical cell under conditions where voltage is in excess of that predicted by the Nernst equation. The Nernst equation predicting the cell potential (E) at 298 K is formulated as -

$$E = E^0 + \frac{0.05916}{z} \log_{10} \frac{a_{\mathrm{Ox}}}{a_{\mathrm{Red}}}. \qquad (9)$$

where E^o is the cell potential at standard-state conditions, z is the number of moles of electrons transferred in the cell reaction or half-reaction a is the chemical activity for the relevant species (where a_{Red} is the reducing agent and a_{Ox} is the oxidizing agent). CV is performed by cycling the potential of a working electrode and measuring the resulting current. The rate of voltage change over time during each of these phases is known as the experiment's scan rate (reported in units of V/s). The potential is applied between the working electrode and the reference electrode while the current is measured between the working electrode and the counter electrode. The obtained data is plotted as the measured current vs. applied potential. The utility of cyclic voltammetry is highly dependent on the analyte being studied. Most importantly, the analyte has to be redox active within the potential window being scanned. It is also highly desirable for the analyte to display a reversible CV wave, which is observed when all of the initial analyte can be recovered after a forward and reverse scan cycle.

A standard CV experiment uses a reference electrode, working electrode, and counter electrode. This combination is sometimes referred to as a three-electrode setup. An electrolyte is usually added to the sample solution to ensure sufficient conductivity. The solvent, electrolyte, and material composition of the working electrode will determine the potential range that can be accessed during the experiment. A schematic of the electrochemical setup utilized to probe Pt NP decorated electrodes reported in this dissertation can be seen in Figure 7.

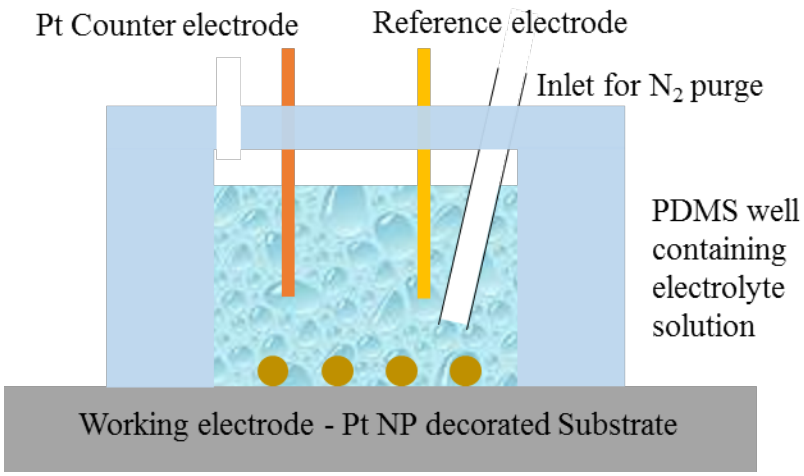


Figure 7: schematic of the electrochemical setup utilized to probe Pt NP decorated electrodes in this study. The working electrodes in this setup are Pt NP decorated substrates, the counter electrode consists of a Pt wire or gauze and the reference electrode choice is made based on the electrolyte composition

CV is an analysis technique with multiple applications where it can be used to study qualitative information about electrochemical processes under various conditions, such as the presence of intermediates in oxidation-reduction reactions, the reversibility of a reaction. Apart from qualitative information, CV can also be used to quantitatively determine the electron stoichiometry of a system, the diffusion coefficient of an analyte, and its formal reduction potential, which can further be used as an identification tool. For a redox process, the voltage separation between the oxidation and reduction current peaks is indicative of the redox reaction kinetics on the working electrode surface and this voltage separation analysis has been utilized multiple times in this dissertation to acquire an understanding of the Pt NP decorated electrodes' electrochemical activity.

1.3.3 Electrochemical Impedance Spectroscopy

Electrochemical impedance spectroscopy (EIS) is a powerful tool typically applied to the characterization of electrode processes and complex interfaces. The usefulness of EIS lies in its

ability to distinguish the dielectric and electric properties of individual contributions of components under investigation in an electrochemical system. Electrochemical impedance is the essentially the response of an electrochemical system or cell to an applied potential. The frequency dependence of this impedance signal can reveal multiple attributes of the underlying chemical processes. In a typical electrochemical cell, slow electrode kinetics, slow preceding chemical reactions, and diffusion can all impede electron flow, and can be considered analogous to resistors, capacitors, and inductors that impede the flow of electrons in an ac circuit. EIS experiments on electrochemical systems at each measured frequency result in raw data which consists of the real and imaginary components of voltage and current. From this obtained raw data one can compute the phase shift and the total impedance for each applied frequency. These can be then fitted to an appropriate model electrical circuit for the electrochemical system under exploration and the obtained resistance and capacitance values help interpret the underlying reaction kinetics. One significant advantage of impedance spectroscopy is that it is a non-destructive technique and thereby can provide time dependent information about the properties of the electrochemical system under exploration and ongoing processes.

1.3.4 Raman characterization of few layered graphene films

Raman spectroscopy is a spectroscopic technique based on inelastic scattering of monochromatic light, typically originating from a laser source. Inelastic scattering means that the frequency of photons in monochromatic light changes upon interaction with a sample. Photons of the laser light are absorbed by the sample and then reemitted. The frequency of the reemitted photons is shifted up or down in comparison with original monochromatic frequency, which is referred to as the Raman effect. This shift in frequency of the reemitted photons provides information about vibrational, rotational and other low frequency transitions in the sample under exploration. The

Raman effect is based on molecular deformations in electric field determined by molecular polarizability. The laser beam can be considered as an oscillating electromagnetic wave with a corresponding electrical vector. Upon interaction with the sample, it induces electric dipole moment which deforms the molecules in the sample of interest. Because of periodical deformation, molecules start vibrating with a characteristic frequency.

When a molecule with no Raman-active modes absorbs a photon with a particular frequency, the excited molecule returns back to the same basic vibrational state and emits light with the same frequency as an excitation source. This type of interaction is called an elastic Rayleigh scattering. For a Raman active molecule, a photon absorbed and part of the photon's energy is transferred to the Raman-active mode and the resulting frequency of scattered light is reduced compared to the incident photon frequency. This Raman frequency is called Stokes frequency. For a Raman-active molecule already in the excited vibrational state, after interaction with the incident photon, the excess energy of excited Raman active mode is released, where the molecule returns to the basic vibrational state and the resulting frequency of scattered light goes up. This Raman frequency is called Anti-Stokes frequency. Figure 8 displays the Jablonski diagram representing quantum energy transitions for Rayleigh and Raman scattering. Every band in the experimentally obtained Raman spectrum corresponds directly to a specific vibrational frequency of a bond within the molecule. The vibrational frequency and hence the position of the Raman band is very sensitive to the orientation of the bands and weight of the atoms at either end of the bond.

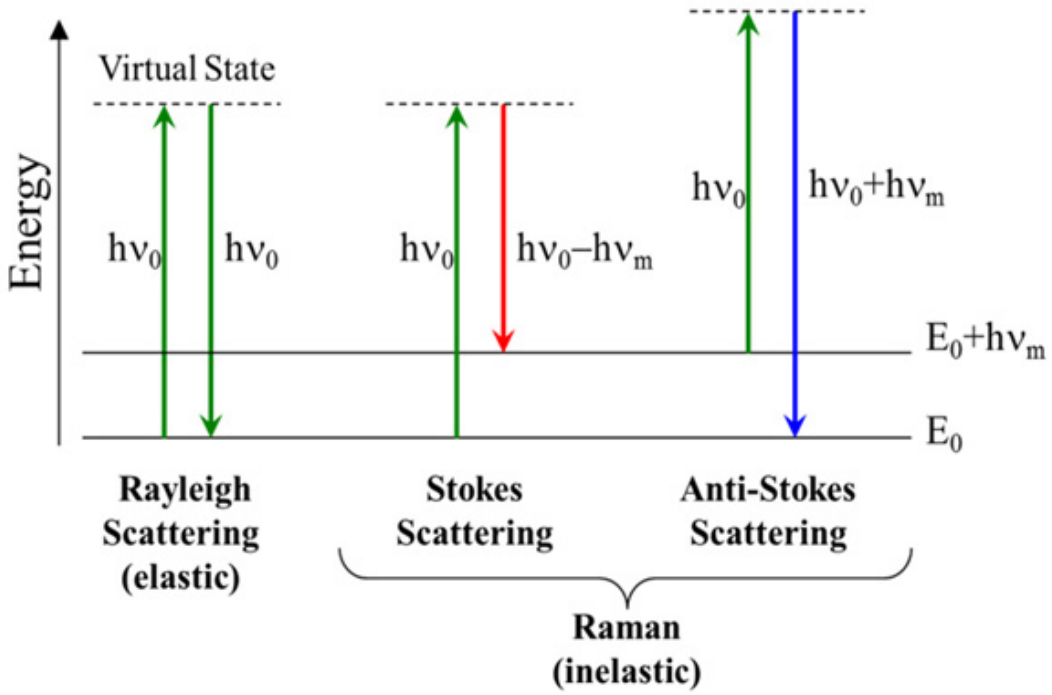


Figure 8: Jablonski diagram representing quantum energy transitions for Rayleigh and Raman scattering (Source- http://bwtek.com/raman-theory-of-raman-scattering/)

Raman spectroscopy is particularly well suited to molecular morphology characterization of carbon materials. In this dissertation, Raman spectroscopy was utilized to characterize Pt NP decorated few layered graphene (FLG) films.

1.3.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface analysis technique capable of providing elemental and chemical state information from the outer 5 to 10 nm of a solid surface. XPS, with its ability to quantify elements and determine chemical states, is used in many branches of materials science, electronics, thin film chemistry, corrosion science, polymer modification, adhesion science, coating chemistry, catalysis, mineral processing chemistry, as well as in exploring fundamental aspects of the chemistry and physics of atoms and molecules. In XPS the sample is illuminated with soft (~1.5kV) x-ray radiation in an ultrahigh vacuum environment. The

photoelectric effect caused by the x-rays leads to the production of photoelectrons, the energy spectrum of which can be determined in a beta-ray spectrometer. This energy spectrum permits one to determine the composition of the sample. The kinetic energies of the emitted photoelectrons, (E_K) can be experimentally obtained. Knowing the photon energy hν one can plot the binding energies of the photoelectrons E_B on a spectrum using the Einstein equation: $E_K = h\nu - E_B$. Because the binding energies of the electron orbitals in atoms are known, the positions of the peaks in the spectrum allows one to identify the atomic composition of the sample surface. Measurement of the relative areas of the photoelectron peaks allows the composition of the sample to be determined quantitatively. Because the photoelectrons are strongly attenuated by passage through the sample material itself, the information obtained comes from the sample surface, with a sampling depth on the order of 5-10 nm. Chemical bonding has an effect on the binding energy of the electron orbital and gives rise to an observable chemical shift in the kinetic energy of the photoelectron. These binding energy shifts can be used to extract information of a chemical nature (e.g. the atomic oxidation state) from the sample surface. In this dissertation, XPS is utilized to observe the sp^2 to sp^3 conversion of C-C bonds induced on Pt NP decorated FLG surfaces by hydrogen spillover from Pt NP to the supporting surface.

1.3.6 Capacitance-Voltage measurements of MOS capacitor structures

The metal oxide semiconductor (MOS) capacitor is essentially the stack forming the gate in a MOSFET. It comprises of a metal (or heavily doped polysilicon) top contact and a semiconductor substrate separated by the field oxide. The MOS capacitor itself is a two-terminal device where bias applied to the metal contact sweeps the MOS structure through accumulation, depletion, and inversion by controlling the buildup of majority and minority carriers in the semiconductor near the oxide through the field effect. In accumulation mode, a sufficiently negative charge applied to

the gate for a p-type semiconductor (as utilized in this chapter 5 in this dissertation) results in the attraction of majority carriers to the region directly beneath the field oxide. As the bias becomes increasingly more positive, the majority carriers are repelled away from the surface resulting in the establishment of a depletion region underneath the oxide. As a result of band bending, the intrinsic Fermi level of the semiconductor moves toward the actual Fermi level. When the bias is strongly positive, minority carriers from the semiconductor bulk enters the region just below the oxide and establishes an inversion region – essentially an electron rich region for a p-type Si substrate.

The capacitance–voltage (C–V) measurement of a MOS capacitor is a powerful and commonly used method of determining the gate oxide dielectric constant, substrate doping concentration, threshold voltage, and flat-band voltage. The C–V curve is usually measured with a C–V meter which applies a DC gate bias voltage, and a small sinusoidal signal (typically in the range of 1 kHz–10 MHz) to the MOS capacitor and measures the capacitive current with an AC ammeter. In the accumulation region, the MOS capacitor is just a simple capacitor with the measured capacitance equaling the capacitance of the oxide (C_{OX}). In the depletion region, the MOS capacitor consists of two capacitors in series: the oxide capacitor, C_{OX}, and the depletion-layer capacitor, C_{DEP}. C_{DEP} is inversely proportional to the depletion width (W_{DEP}) of the space charge region formed at the Si surface and as the applied gate bias increases beyond the flat band voltage (V_{FB}), W_{DEP} expands, and therefore the measured capacitance decreases. This decreasing capacitance value eventually saturates (C_{MIN})upon increasing the gate voltage to the threshold bias and stays constant at high frequencies (larger than 10 KHz – as employed in the C-V measurements in this dissertation) for increasing applied gate biases.

Deviations from the ideal C-V curve can be utilized to extract information about different charges within the oxide and at the semiconductor/oxide interface. Traditionally, Oxide charges have been characterized into three major categories: fixed oxide charges, trapped oxide charges and mobile ions. Fixed charges (Q_f) are independent of oxide thickness and are typically located very near the oxide-semiconductor interface. A positive Q_f results in a negative V_{FB} shift and a negative Qf results in a positive V_{FB} shift. This is because if a negative bias is applied at the gate, then this charge must be compensated by positive charge somewhere along the MOS stack. Ideally, when Q_f is negligible, this charge is compensated entirely by donors in the semiconductor. However if a positive fixed charge is present, then they partially compensate some of the negative gate charge. This reduces the number of donors in the semiconductor that are required to compensate the charge at the gate and thus reduces W_{DEP}. A narrower depletion region raises overall MOS capacitance, producing a positive capacitance-voltage (C-V) shift. The opposite is the case of negative fixed charges. Trapped charges, (Q_t) are electrically neutral sites distributed throughout the oxide that can be charged with the introduction of electrons or holes. This charge is most commonly due to electrons and/or holes injected during device operation and originate due to defects in the oxide bulk and cause a voltage shift similar to the previously mentioned fixed oxide charges. Mobile charges in dielectric (Q_m) are attributed to the presence of ionic impurities with Sodium ions being the dominant contaminant in most reported studies. Unlike the trapped and fixed charges, which are located at a single site, mobile ions can move about within the oxide and lead to bias dependent and bias sweep direction dependent voltage shifts or hysteresis. The total flat band voltage shift observed in the C-V characteristics is due to these oxide charges is the sum of the representative individual voltage shifts and can be stated as –

$$\Delta V_{FB} = (Q_f + Q_t + Q_m)/C_{OX} \tag{10}$$

CHAPTER 2: STABILITY OF SUB—2 NM PT NANOPARTICLES ON DIFFERENT SUPPORT SURFACES

2.1 BACKGROUND

Nanocatalysis is a rapidly growing field involving the use of NPs as catalysts for a variety of organic and inorganic reactions. Transition metal NPs are especially attractive as catalysts due to their high surface-to-volume ratio and high surface energy, which make the surface atoms particularly active. However, active surface atoms may also result in NP instability over the course of their catalytic function. This raises important questions concerning the recyclability of transition metal NPs that have been deposited on a solid support. Loss of effective surface area resulting from changes in particle size and shape represents a fundamental challenge to the long-term stability of systems utilizing these NPs for catalytic applications. A clear understanding of electrode degradation mechanisms is needed to mitigate surface area loss and meet the present Department of Energy (DOE) lifetime goal of 5000 h [41]. In essence, two mechanisms are expected to control surface area loss: Pt dissolution and subsequent redeposition on the conducting support (mass loss mechanism) and Pt particle electrochemical Ostwald ripening (coarsening mechanism) [41, 42]. It has been proposed that these mechanisms are strongly influenced by the particle areal density on the support, which represents the number of particles of a given diameter per unit area of the supporting surface [41]. Dissolution rates are generally faster for NPs with smaller sizes since smaller particles are destabilized by their greater specific surface energy (i.e. smaller NPs are more likely to undergo faster dissolution/coarsening kinetics owing to their higher surface to bulk atom ratio) [43]. Coarsening usually requires dissolution to allow transport of Pt species between particles, but is additionally driven by different particle surface-to-volume ratios

and is therefore highly sensitive to the width of the particle size distribution [41]. However, when NPs are in contact with each other, surface coarsening can be explained by agglomeration rather than Pt dissolution–redeposition [44].

Understanding the size dependence of the dissolution rate is essential to gain a perspective on how the NP size distribution and areal density affects surface area loss, since Pt dissolution is at the root of both off-support deposition and coarsening. Basic thermodynamic analysis suggests that stability decreases with particle size: assuming that bonding in a spherical NP of radius r is the same as in bulk, the additional surface energy (γ) increases the energy per atom by an amount $\Delta\mu = 2\gamma\Omega/r$, where Ω is the atomic volume. This Gibbs-Thomson (GT) analysis predicts a downward shift in the dissolution potential of a particle by an amount $\Delta E = -\Delta\mu/n$, where n is the number of electrons transferred on forming the dissolved metal cation and $\Delta\mu$ is expressed in appropriate units. The GT picture of dissolution at the nanoscale can be questioned on multiple fundamental grounds. The analysis neglects passivation effects on the surface of NPs, which are considerably more reactive than their bulk equivalent [45]. Hence, NPs may compensate for their increased energy by stronger bonding with passivating agents in solution, such as oxygen, protons, or hydroxyl groups [46]. This shift in chemical reactivity may change the nature of the dissolving surface as well as the dissolution mechanism, breaking down the definition and size dependence of the surface energy in the GT analysis. Yet the most important limitation of the analysis may be its use of bulk surface and cohesive energies and the neglect of edge and vertex atoms in NPs. It is also not clear that this assumption holds at the sub-5 nm scale [47] and some researchers have proposed that particles of sufficiently small size are actually stabilized by quantum size effects [48], making the bulk energy term inappropriate to describe bonding at the nanoscale. The lack of direct observations on particles with well-determined size has prevented the development of

quantitative theories to predict stability of NPs in solution. Utilizing TTS technique to fabricate Pt NPs with well-determined size distributions and number densities on support surfaces, this paper aims to provide further evidence of strong correlation between Pt NP-support interactions and Pt NP characteristics with their stability under catalysis.

2.2. METHODS

2.2.1 Few layer graphene (FLG) transfer

FLG was transferred on FTO substrates by rubbing highly ordered pyrolytic graphite (HOPG–SPI2) samples on the intrinsically rough FTO surface and subsequent removal of debris using Scotch tape. This process yields FLG layers with fairly reproducible quality. The I_D/I_G ratio for the FLG samples were ~1 and based on the shape, position, and profile of the G' Raman peak, 3-4 layers of graphene were transferred to the rough FTO surface (for further details, please refer to section 3.3.1). It is worth noting that the FLG samples showed negligible effects of plasma damage after deposition of Pt NPs. Detailed explanation of the lack of plasma damage on tilted-target sputtering (TTS) samples is provided elsewhere [49]. Henceforth, FLG-covered FTO substrates will be referred to as FLG.

2.2.2 Pt NP fabrication and characterization

An AJA International ATC 2000 magnetron sputtering system was used to deposit Pt NPs on FTO and FLG supports. Detailed information of Pt NP sputtering using the TTS method are provided elsewhere [4-8, 16, 50-52]. Exhaustive TEM analysis of Pt NPs was performed using a 5 nm Al_2O_3-coated carbon grid. No significant changes in size distribution or areal density were seen for equivalent Pt depositions on Al_2O_3, FTO, or FLG surfaces[50]. Details of Pt NP characterization are provided in [16]. Exhaustive TEM analysis of Pt NPs was performed using a 5 nm Al_2O_3-coated carbon grid. For graphene films, approximately 100 particles were used in generating the histograms reported in Figure 10. For OTS and Al_2O_3 films, this number stands at 200. Because of the discontinuous nature of graphene flakes on the TEM support grids, lower number of Pt NPs on graphene could be imaged and analyzed. No significant changes in size distribution or areal density were seen for equivalent Pt depositions on Al_2O_3, FTO, or FLG surfaces [49]. Beam induced coalescence during Pt NP characterization under 200kV HRTEM was avoided using a technique described elsewhere in [16].

2.2.3 Cyclic voltammetry (CV) experiments

For the CV setup, the working electrodes were Pt-sputtered FTO and FLG substrates, the counter electrode was a Pt wire gauze electrode, and the reference electrode was a reversible hydrogen electrode (RHE). It is well known that a Pt counter electrode has the propensity to act as a sink if placed in close proximity to the working electrode. As reported by Holby et al., with a Pt sink distance similar to that experienced in in-situ conditions for PEM fuel cells, around 10 mm, it is observed that dissolution dominates the electrochemical surface area loss mechanism [53]. As the

sink distance is moved farther out, this loss is decreased and the less aggressive loss mechanism of coarsening begins to dominate. In all CV experiments, the Pt counter electrode was further than 1 cm from the working electrode to avoid the electrochemical surface area losses due to Pt counter electrode acting as a sink. The electrolyte used in the CV runs was 0.5 M H_2SO_4. The exposed area of the working electrode was controlled using molded PDMS wells. All electrochemical measurements were done at 500 mV/s scan rate. 500 scans (250 cycles) were performed to test electrochemical stability of Pt NPs as the majority of supported Pt mass loss occurs within the first 250 cycles [41].

2.3. RESULTS AND DISCUSSIONS

This chapter discusses stability of these sub-2nm Pt NPs on different supporting surfaces. This was explored to better understand the role of NP size and surface adhesive forces governing the issue of active surface area loss.

2.3.1 Raman characterization of FLG substrates

Raman spectroscopy using a 514 nm laser was done at 3 marked spots on each Pt sputtered FTO-FLG sample (total 18 samples) to determine the quality of the FLG film and the uniformity of the ID/IG ratio at different spots across varying samples. The Raman was done at standard confocality because, given the high surface roughness of FTO, weak signals were attained at high confocality. The Raman curves and the mean and standard deviations of the I_D/I_G ratios are listed below in Table 2. The obtained normalized Raman curves for each Pt varying sputtered-HOPG-FTO sample are listed below in Figure 9. It can be seen that even after prolonged sputtering time, there is minimal plasma damage to the FLG film surface as the ID/IG ratio remains consistent. For all the Raman curves, the I_D/I_G ratio seems quite similar. The 2D band for all the samples is around 2705

cm^{-1} which is characteristic of approx. 3-4 graphene layers [54]. The slight peak noticeable around 2940 cm^{-1} in each sample is generally attributed to a two-phonon excitation. The energy corresponds to the sum of the 1355 and 1590 cm^{-1}. This indicates that these two modes occur in the same region of the sample [55, 56]. Table 2 lists the I_D/I_G ratio for each sample at 3 different spots with the mean and standard deviation for each sample. The overall mean of the I_D/I_G ratio for all 18 samples was 1.02 and the standard deviation was 0.09 revealing a < 10% error bar. Based on the Raman data, the HOPG-FTO composite films look uniform enough to analyze the Pt NP size dependent stability on these supporting structures.

Pt deposition time on HOPG-FTO substrate (sec)	I_D/I_G Spot 1	I_D/I_G Spot 2	I_D/I_G Spot 3	I_D/I_G mean	I_D/I_G Std. Dev
10	0.93	1.02	1.12	1.02	0.09
20	0.85	1.09	1.01	0.98	0.12
30	0.99	0.93	1.20	1.04	0.14
45	0.96	1.02	1.19	1.06	0.11
60	1	0.88	1.06	0.98	0.09
120	1.02	1.02	0.99	1.01	0.02

Table 2: I_D/I_G ratio for each sample at 3 different marked spots with the mean and standard deviation for each sample

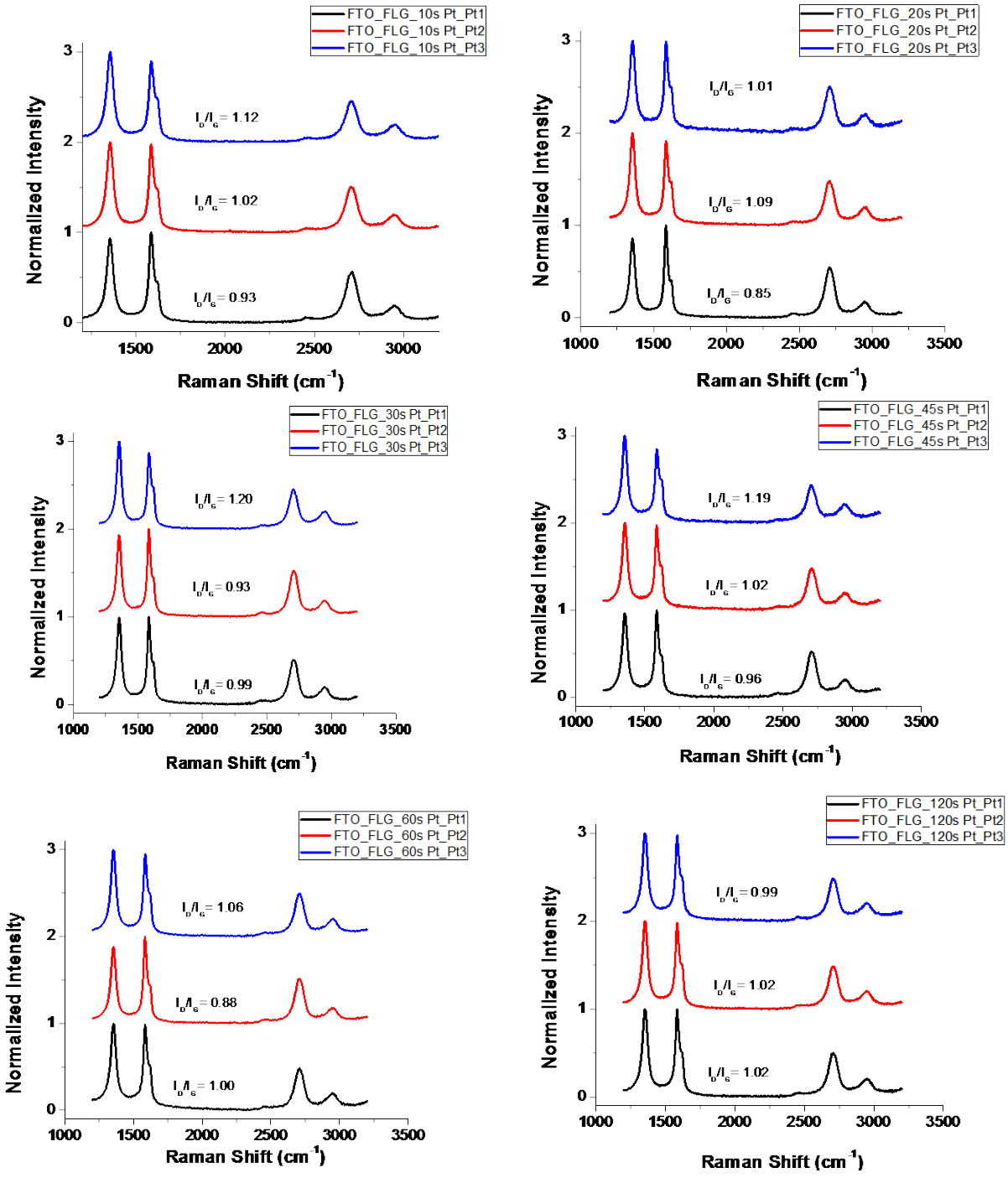


Figure 9: Normalized Raman curves at 3 marked spots for Pt varying sputtered-FLG-FTO sample - (a) 10 sec Pt, (b) 20 sec Pt, (c) 30 sec Pt, (d) 45 sec Pt, (e) 60 sec Pt, (f) 120 sec Pt

2.3.2 Pt NP stability on various surfaces

The Gibbs–Thomson (or Kelvin) equation [43] yields an estimate for the size dependence of particle stability and is generally stated as the chemical potential (partial molar free energy) of a metal atom in a particle of diameter *d*. *U(d)* differs from that in the bulk *U(∞)* by:

$$U(d) - U(\infty) = \frac{4\,\gamma\,\Omega}{d} = E_{GT} \qquad (11)$$

Here, γ is the particle surface free energy, and Ω is the molar volume of the particle. The Gibbs–Thomson energy (E_{GT}) for Pt is 0.18 eV/atom at d = 5 nm, and as large as 0.91 eV/atom for d = 1 nm. It is important to note that the surface free energy term can get more complicated in electrochemical systems due to the presence of electrochemically active species and potential dependent surface oxides [53]. If one assumes that dissolution is dominated by terms of an exponential nature in the particle stability equation (dissolution rate proportional to exp((1-β_1)E_{GT}/kT – (2)), where β_1 is the transfer coefficient with a value of 0.5), then this increase in E_{GT} equates to an increase versus the bulk in the dissolution rate by an order of magnitude for a 5 nm particle, 3 orders of magnitude for a 2 nm particle, and 6 orders of magnitude for a 1 nm particle [41]. The impact of Gibbs–Thomson on the stability is, therefore, far more important for particles below 5 nm than above it and provides a powerful driving force for dissolution and coarsening by 2 nm. The size dependence of dissolution rates shows that the NP size distribution should play an important role in both mass loss and coarsening mechanisms of surface area loss, particularly for particles in the commercially relevant range of a few nanometers. The contribution of size distribution to surface area loss is difficult to determine because surface area loss is potentially influenced by many factors, including temperature, electrochemical potential, presence of hydrogen, Pt loading and dispersion, particle morphology, and carbon support. For example,

Kinoshita et al. [57] demonstrated that the surface area loss with potential cycling was much faster for Pt NPs on carbon than unsupported Pt black (with micron particle sizes). The additional differences of particle dispersion, support, and morphology between catalysts make it almost impossible to establish the direct impact of the changing particle size distribution on surface area loss. In order to ascertain the true effect of sub–2 nm Pt NP size distribution and substrate characteristics on NP stability, it is essential to vary one of the two aforementioned parameters while keeping the other one relatively constant. While changing the type of substrate supporting the Pt NPs is relatively straightforward, controlling NP size distribution on supporting structures is a much more arduous task. Traditionally, a chemical synthesis route (bottom-up process) has been utilized for the preparation of such metal NPs with controlled sizes and size distributions [58, 59]. However, immobilization of these NPs to a supporting structure while maintaining homogeneous size distribution and ensuring good adhesion of the particles to the supporting structure is not an easy task. Another major drawback of the chemical synthesis route is the presence of undesirable side-products (e.g. impurities and capping agents), which may lead to surface poisoning, adversely affecting sustained catalysis [60]. To address these issues, small NPs have been synthesized on supporting structures using top-down techniques such as physical vapour deposition (PVD) and chemical vapour deposition (CVD). However, the large variation in NP size and areal density observed in these studies is undesirable for applications focusing on size-dependent behaviour [16, 50, 61-67] . Top-down approaches such as de-wetting [16, 68, 69] or direct deposition [61, 63, 70, 71] have also been used to create NPs by PVD. The most common of these, the de-wetting technique, produces high-density metallic NPs, but provides limited control over particle size, distribution, and areal density due to random ripening at nucleation sites. Recently, sub-2 nm Pt NPs with narrow size distribution and high areal density have been produced

by tilted target sputtering (TTS) on different substrates, which have been utilized in fields ranging from single electron memory devices to catalysing triiodide reduction at counter electrodes of dye-sensitized solar cells (DSSC) [16, 49, 72-76]. The size tunability and homogeneity in the sub-2 nm regime makes the TTS process ideal for fabrication of supported Pt NPs for the purpose of studying electrochemical stability.

2.3.3 Pt NP stability under e-beam exposure on different substrates

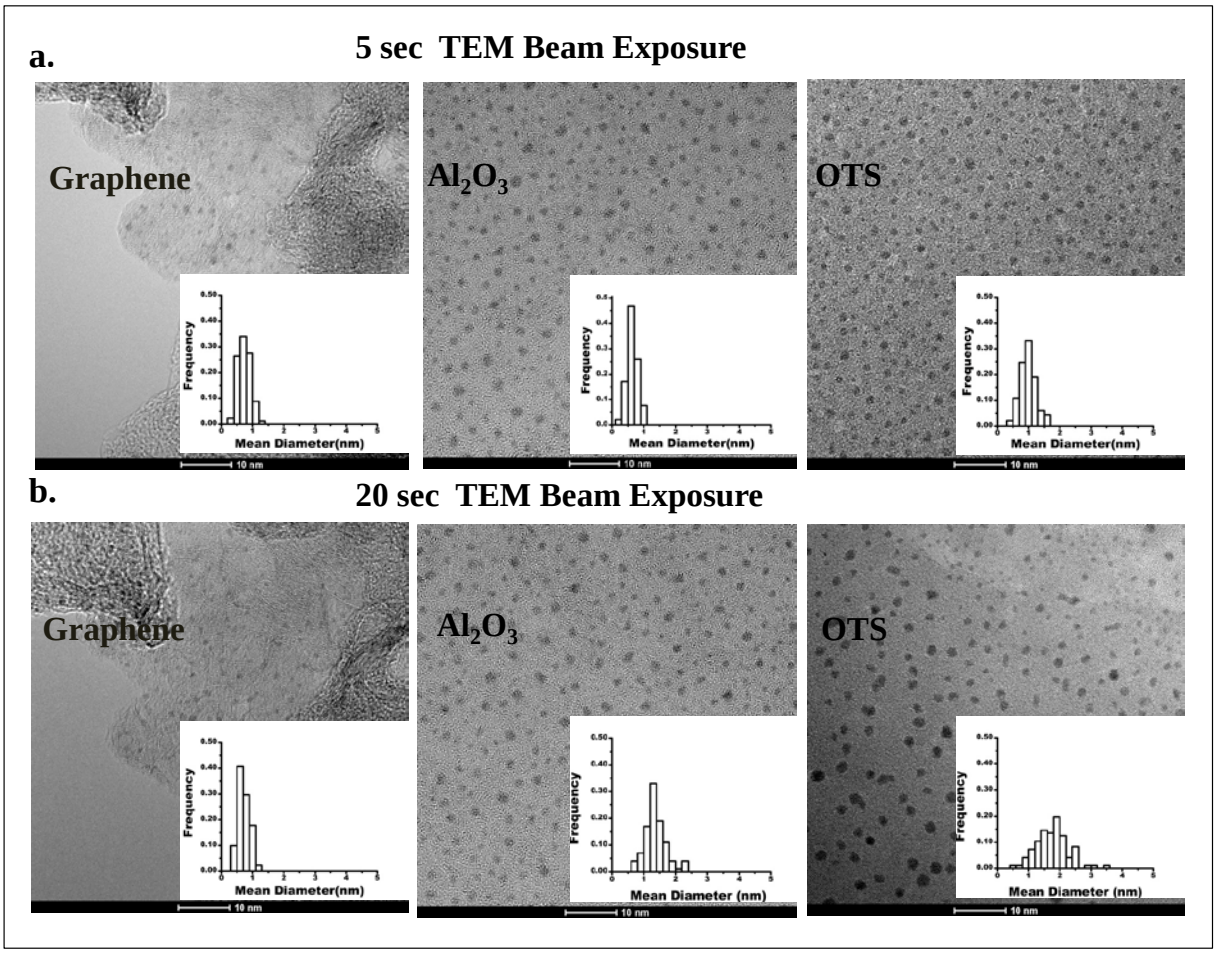


Figure 10: HRTEM of Pt NPs on graphene, Al2O3, and OTS surfaces with (a) less than 5 s beam exposure and (b) with around 20 s beam exposure; sputtering was done at 30 W RF power, 38.3º target angle and for 20 sec sputter time; inset - Pt NP size distribution

Different substrate surfaces were examined to explore the effect of the support surface energy on e-beam-induced coalescence. For comparison, Figure 10 shows the HRTEM images of time-varied beam-induced coalescence for Pt NPs on different substrate surfaces. From Figure 10 a and b, it is evident that beam-induced coalescence was more rapid for Al_2O_3 grids treated with 0.5 mM octadecyltrichlorosilane (OTS) SAM layer (i.e. low surface energy) than for untreated Al_2O_3 or graphene. Whereas the size distribution of Pt NPs on graphene (0.73 ± 0.19 nm) remains relatively unchanged upon longer e-beam exposure, the size distribution of Pt NPs on Al_2O_3 increases from 0.73 ± 0.19 nm to 1.36 ± 0.32 nm. OTS treated Al_2O_3 surface shows the most prominent effect of surface diffusion aided by prolonged e-beam exposure as the Pt NP size distribution increases from 0.99 ± 0.25 nm to 1.75 ± 0.52 nm. It should be noted that the NP growth is dependent on both -the energy of the arriving atom and the energy of the substrate surface. Typically, in theory – for ideal surfaces, the surface energy is a dominating factor for material growth on the substrate. In practical applications, the surface roughness with kinks, edges and step edges supersede this effect disturbing the ideal theoretical assumptions of thin film growth. During sputtering process, when metal atoms arrive at the surface, they bond (chemically) with the substrate surface, releasing energy. Sometimes, this energy is enough to overcome the potential barrier for surface migration. This bonding energy is highly characteristic of the surface and can be controlled by controlling surface properties. Typically a low surface energy substrate will have lower bonding energy and vice-versa. Thus energy from the arriving clusters or thermal energy, greater than this bonding energy can lead to lateral migration of deposited clusters at the substrate. .Surfaces coated with amorphous films (Al_2O_3 in this case) present a wide distribution of kinks, ledges and defects. These defects influence the binding of individual atoms to the substrate, which, in turn, affects surface diffusion and particle nucleation [20]. The most common process on amorphous surfaces is growth

on surface terraces, where the nucleation takes place at particular surface sites with open –Al or –O bonds [77, 78]. Treating the surface with OTS leads to complete, orderly coverage of the oxide layer with the terminal $–CH_3$ bonds of the OTS, thereby eliminating these nucleation sites. Consequently, Pt NP binding to these moieties is comparatively weaker and, thus, the substrate-Pt NP binding energy is easily overcome with electron beam exposure, resulting in accelerated beam-induced coalescence during HRTEM imaging. It should be noted that there is an overestimation of actual size and underestimation of actual particle areal density (in case of OTS treated Al_2O_3surface) even for the NPs seen in Figure 10 a as the particles move and coalesce instantaneously on the low-energy substrate due to the poor substrate–particle adhesion energy.

Graphene proved to be a more stable surface for NP formation. The stability of ultrafine Pt nanoclusters on graphene is in line with that observed in [79], where a strong interaction between graphene nanosheets (GNS) and platinum atoms was observed. In that work, no platinum aggregation was observed even after heat treatment at 400 °C in Ar/H_2 (4:1 v/v) [79]. This strong Pt atom – GNS interaction was explained by a high level of carbon vacancies and defects on GNS due to its preparation through the chemical reduction of graphene oxide. In the present study, the graphene used was prepared by a gas phase route that is considered superior (fewer defects) to graphene fabricated through chemical reduction [80]. Although the defects and carbon vacancies of this graphene are lower than that used in [79], the Pt NPs show remarkable stability. This stability hints towards a strong Pt atom–graphene interaction, which warrants further exploration. This strong Pt-graphene interaction anchors Pt NPs to the substrate, thereby stabilizing the particle areal density [81]. In terms of the GT equation (Eq. 1), a higher substrate surface energy leads to reduction in the particle surface free energy (γ) due to stronger particle-substrate interfacial interaction. As γ decreases, the value of E_{GT} also decreases as well as the dissolution rate since it

is exponentially related to E_{GT} (Eq. 2). Thus, the higher NP stability under prolonged beam exposure on higher surface energy graphene when compared to lower surface energy OTS corresponds well with the aforementioned GT model. It is worth noting that the coalescence of Pt NPs on different surfaces is primarily driven by localized heating due to inelastic collision of the high energy electrons during HRTEM imaging. While comparing Pt NPs on 5 nm Al_2O_3 thin films, OTS treated 5 nm Al_2O_3 thin films, and graphene film (all on holey carbon grids), one might question if the differing specimen thickness would cause appreciable difference in localized heating among the studied samples due to e-beam exposure. It has been previously reported by Egerton et al. that in such cases, the temperature change upon e-beam exposure is independent of specimen thickness [82]. Thus, the localized heating effect should be similar for all studied surfaces and based on the observation of changing NP characteristics over time due to prolonged e-beam exposure, the true nature of NP-substrate interaction can be studied.

2.3.4 Pt NP stability after potentiodynamic cycling

While analyzing stability of Pt NPs on different supports using potentiodynamic sweeping, it is essential to understand the fundamental CV characteristics of Pt in acidic environments. Although HRTEM analysis before and after CV cycling could help determine Pt NP degradation mechanisms, for sub-2 nm Pt NPs, beam exposure can significantly alter Pt NP characteristics (as mentioned in section 3.3.3) and it would be erroneous to draw conclusion from HRTEM image analysis before and after potentiodynamic cycling. As reported in multiple previous studies, the CV of a polycrystalline Pt thin film in an acidic medium can be described in three broad regions:(1) underpotentially deposited hydrogen region (0–0.4 V), (2) electrochemical double layer region (0.4–0.7 V), and the Pt/PtO_2 redox region (0.7–1.2 V). As depicted in Figure 11, the peaks in the underpotentially deposited hydrogen (H_{UPD}) region can be associated with different (110) and

(100) facets [83, 84]. The (111) facet has a weak H adsorption/desorption current density profile, which can be attributed to a lower availability of (111) facets on the polycrystalline Pt surface [83, 85]. Pt NP stability on the supporting surface is a major factor that can be ascertained through multiple CV cycling. As mentioned before, decay of Pt NP catalysts in the 2-6 nm range is usually attributed to the following two reasons: a) NPs inherently show a strong tendency to agglomerate due to their high specific surface energy and b) at higher potentials with respect to the RHE, irreversible Pt oxides form leading to surface degradation and loss of catalytic activity [86]. Thus, all these factors need to be accounted for while explaining stability and other characteristics while analyzing CV plots.

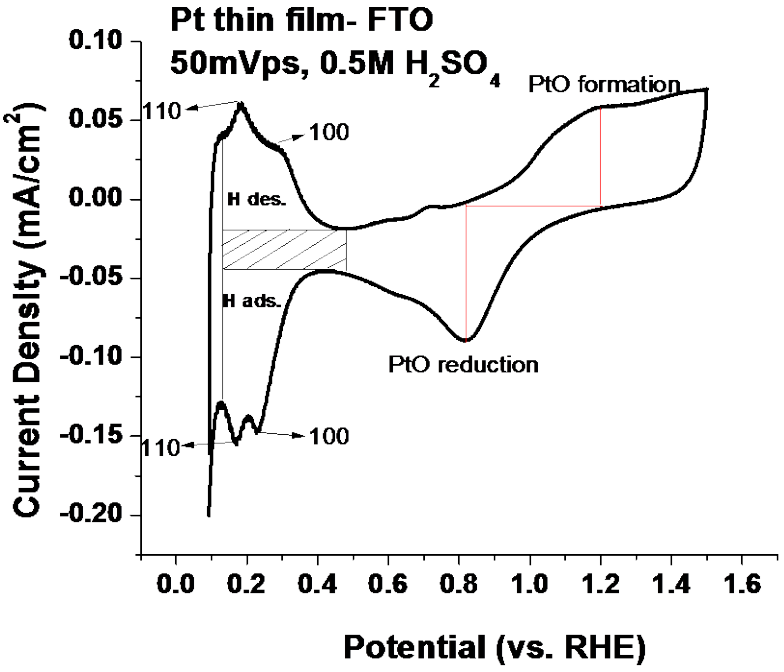


Figure 11: CV of sputtered continuous 50 nm Pt thin film on FTO in 0.5 M H2SO4

All CVs were done between 0 – 1.2 V vs. RHE and although support corrosion could occur at the higher potential ranges, for voltages below 1.2 V, Pt NP dissolution and coalescence have been known to play a more dominant role towards NP degradation [53]. Additionally, only 250 scans were performed at 500 mV/s scan rate to understand the sub-nm Pt stability dependence on support surface-Pt cluster interactions and minimize support corrosion. Also, FTO and graphitized carbon supports are known to be more resistant to support corrosion compared to traditional porous Vulcan carbon morphologies studied in a majority of NP stability tests [87].The potentiodynamic scans of sub-nm (0.9 nm) and sub-2 nm (1.5 nm) particles are displayed in Figure 12. It can be seen from Figure 12 that there are signatures of dissolved oxygen in the system. Although N_2 was bubbled through the system for 10 minutes before starting the experiments, the low Pt loadings make the presence of oxygen signatures more prominent. This should not have significant effects on the results in this study.

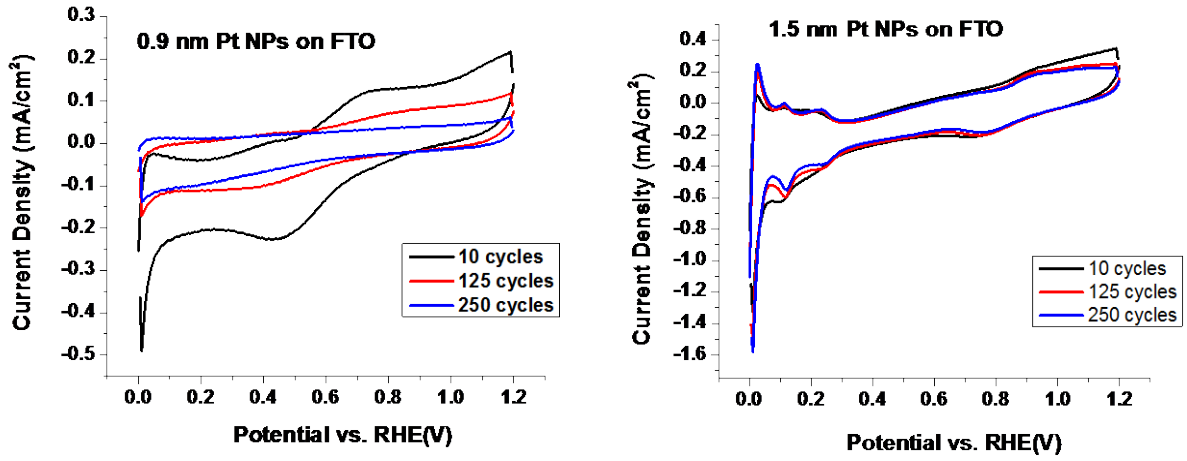


Figure 12: CVs of (a) 0.9 nm Pt NPs and (b) 1.5 nm Pt NPs on FTO in 0.5 M H2SO4

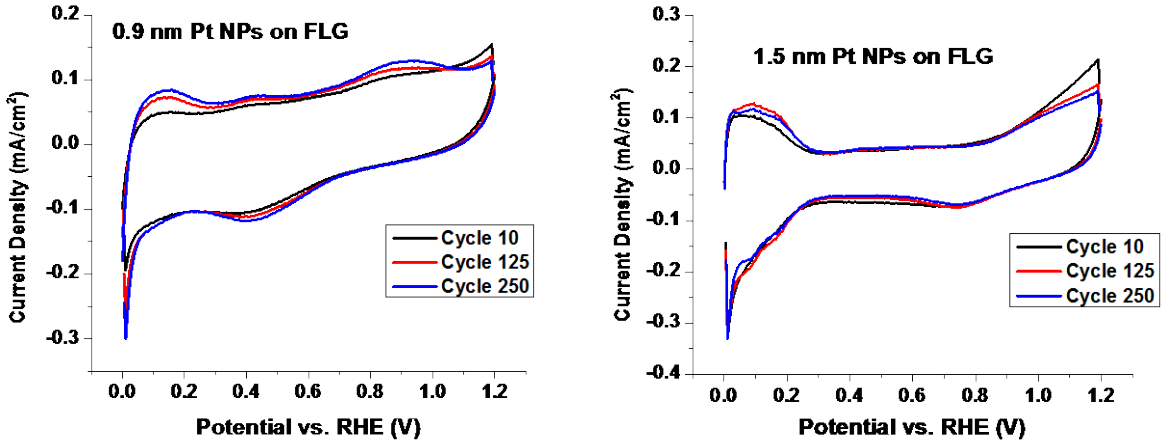


Figure 13: CVs of (a) 0.9 nm Pt NPs and (b) 1.5 nm Pt NPs on FLG in 0.5 M H2SO4

One major difference between these two types on Pt NPs, besides their mean size, is their crystallinity. The 0.9 nm Pt NPs are not crystalline in nature, whereas, the 1.5 nm Pt NPs show single crystalline domains in HRTEM images [16, 49]. Based on the GT model (which does not explicitly take into account the crystalline properties of NPs), the 0.9 nm particles should have a higher E_{GT} value compared to the 1.5 nm particles (since E_{GT} is inversely proportional to the particle diameter) and thus higher dissolution rate. This prediction complies well with the experimental results displayed in Figure 12, where non-crystalline 0.9 nm particles show evidence of Pt mass loss upon multiple cycling. The 1.5 nm crystalline Pt NPs are relatively stable and yield similar current density profiles after 10, 125, and 250 potentiodynamic cycles. The crystalline nature of the 1.5 nm Pt NPs can be further evidenced in Figure 12b by the crystalline facet-dependent peaks in the underpotentially deposited hydrogen (UPD) region as mentioned previously in this section. Apart from size-dependent reduction of E_{GT}, the crystalline nature of these particles could further decrease the γ value of these particles resulting in further lowering of E_{GT} value and thereby the dissolution rate. It is worth noting that the sub-nm Pt NPs show very weak Pt signature characteristics as these are non-crystalline clusters, whose CV signatures are yet

to be reported in published literature. The double layer capacitance of a plain FTO surface is ~9 $\mu f/cm^2$. In cases of Pt NP supported FTO and FTO-FLG supports, the capacitance is typically larger than 20 $\mu F/cm^2$ and not particularly dominated by support capacitance. Pt loading is controlled by manipulating tilted target angle sputtering parameters and size distributions and surface number densities are fairly reproducible over multiple runs [16]. It should also be noted that although quantifying electrochemically active surface area using integration of the hydrogen adsorption/desorption peaks would help strengthen this study, the low Pt loadings and lack of traditionally recognizable Pt signature peaks in CV (especially for sub-nm non-crystalline Pt clusters) make this method to attain quantitative analysis of surface area loss unreliable. Due to this, it is hard to accurately pin down the double layer region in the CV curves leading to erroneous electrochemical surface area values (obtained using the integration technique utilizing the hydrogen adsorption/desorption peaks) that fail to accurately represent involved NP degradation mechanisms. Further effects of the supporting surface, apart from NP size-dependent electrochemical stability, were explored using FLG as the supporting structure. While the calculated surface energy of the FLG films used in this experiment was ~56 dynes/cm [49], the surface energy of pristine monolayer graphene is ~46.7 dynes/cm and that of pristine graphite is ~54.8 dynes/cm [88]. In this case, the high defect ration (n) of the FLG layer (I_D/I_G ~1) must be taken into account. Pristine FLG should have a surface energy closer to pristine graphite, but the high defect count tends to increase the surface energy [89]. Increase in surface energy leads to better NP adhesion to the supporting structure and, thus, reduces γ and increases stability, which was confirmed by CV (Figure 13). Higher stability of NPs on graphene sheets have been reported previously [90, 91]. However, to our knowledge, no detailed analysis of NP characteristics and its effect on stability has been reported. In Figure 13, it can be seen that even non-crystalline 0.9 nm

Pt NPs on FLG support show excellent stability over 250 potentiodynamic cycles when compared to those on FTO electrodes (Figure 13). In general, there are four processes that have been considered relevant to the loss of electrochemically active surface area of Pt in fuel cell applications [47] – First, Ostwald ripening based coarsening of individual Pt NPs on the support, which may involve dissolution of Pt from small particles, diffusion of soluble Pt species from small to large particles in the ionomer phase and redeposition/reduction of soluble Pt species onto large particles on the nanometer-scale. Based on the potential range employed in this study, this mechanism could be the leading cause for electrochemical surface area loss as seen in Figure 12 a. The second mechanism involves Pt crystal migration and coalescence, which further involves motion of Pt particles and coalescence where they meet on the support. Although Pt crystal migration at room temperature in electrolyte-less conditions is less likely, in the presence of an electrolyte, this becomes a complicated mechanism and has been reported to be theoretically possible [47, 53]. The third mechanism involves detachment of Pt NPs from the carbon support and agglomeration of Pt NPs, generally induced by carbon corrosion. As mentioned previously in this section, in the case of this particular study, this is not believed to be the dominant mechanism for electrochemical surface area loss. In the fourth mechanism, dissolution and re-precipitation of Pt single crystals at a Pt sink can result in loss of Pt from the carbon support and loss of electrode activity. This mechanism requires the presence of a Pt sink in close proximity, which is not the case in this particular study. Potential dependent oxide formation on the Pt NP surface could also have major say in Pt dissolution kinetics [53]. Although oxide formation on the surface would affect Pt NP surface tension and thereby the NP free energy, for the studied potential range, this effect should contribute similarly in all studied NP based systems and the Pt NP-support interactions should be considered as an independent quantity in the Gibbs-Thomson model and

would thus independently help determine the Gibbs-Thomson energy. In a previously reported study by Holby et al., the authors discuss how surface free energy changes as a function of applied potential, oxide surface coverage, and relative contribution of particle surface energy due to the support. Here, they indicate that the Pt-support interaction has a rather minor role in determining change in surface free energy and thereby the NP degradation kinetics. With this in mind, it is important to ask if Pt-support interactions likely to play a dominant role in stability for dissolution mediated mechanisms. Although for bigger Pt NPs, Pt-support interactions might play a minor role in determining NP stability mechanics, for sub-nm Pt clusters, the authors believe that Pt-support interactions start playing a more dominant role. This is because these nanoclusters comprise of a few monolayers of Pt atoms and after the first few monolayers are dissolved at higher potentials, the Pt-support interactions would have a major role in determining whether the final Pt layer (in contact with the support) would be available as a nucleation center for dissolved Pt ions. In case of FTO supported particles, due to the weaker interaction energy, potentiodynamic scans are more likely to dissolve the Pt atoms in direct contact with the support (after the first few monolayers have been dissolved in previous scans) thereby eliminating nucleation centers for dissolved Pt ions to nucleate on and thereby leading to electrochemical surface area loss. Counter intuitively, stronger Pt-support interactions (in case of Pt NPs on FLG) would help sustain the final Pt monolayer longer thereby protecting nucleation centers for dissolved Pt ions to nucleate on and thereby preventing significant electrochemical surface area loss. Better Pt NP adhesion at conducting tin oxide (ITO in this case) coated functionalized graphene surfaces has also been previously reported by Kou et al [92]. In that study, based on experimental work and periodic density functional theory (DFT), the authors show that the supported Pt NPs are more stable at the Pt-ITO-graphene junctions.

CHAPTER 3: UTILIZING SUB-2NM PT NANOPARTICLES FOR TRIIODIDE REDUCTION IN DYE-SENSITIZED SOLAR CELLS - IMPACT OF NP SIZE, CRYSTALLINITY AND SURFACE COVERAGE ON CATALYTIC ACTIVITY

3.1 BACKGROUND

This study presents the catalytic and charge transfer activities of sub-2 nm Pt NPs for triiodide reduction (at DSSC counter electrodes). The particles were deposited on planar substrates by tilt target sputtering (TTS) at room temperature. This TTS configuration utilizes an angled deposition sputter process and low-density/low-energy metal atoms in the dissipated deposition flux, thus enabling generation of Pt NPs with a narrow size distribution and high surface areal density (~5×10^{12} cm^{-2}) [16]. Introduced over two decades ago, dye-sensitized solar cells (DSSCs) have emerged as competent alternatives to traditional solid-state solar cells since they possess attractive techno-economic advantages, such as their construction from inexpensive raw materials without requiring large-scale equipment for their manufacture [93-95]. Moreover, their improved performance under diffuse light conditions and/or at higher temperatures, and their negligible dependence on the incident light angle are additional advantages over traditional photovoltaic cells. Efficiencies as high as 12% for small cells and about 9% for mini-modules have been achieved, and means of energy-efficient production methods have been accomplished [94].

Traditionally, the DSSC anatomy consists of these three main components: a photosensitizer (dye) coated nanocrystalline TiO_2 layer on a transparent conducting oxide (TCO) coated glass substrate that serves as the anode, an iodide/triiodide redox couple in an organic solvent, and a triiodide-reducing platinized TCO-coated glass substrate. The conducting TCOs used as cathodes

in the DSSC are extremely poor catalysts for triiodide reduction. In other words, TCO electrodes have a very high charge transfer resistance, generally on the order of 10^6 Ω cm^2. It is essential to shrink the charge transfer resistance significantly, ideally to <10 Ω cm^2, for DSSCs to function efficiently [37]. This is generally achieved by introducing a layer of catalyst on top of the TCO, typically in the form of a 2–50 nm thin film of platinum (Pt) [96].

In the majority of published DSSC studies, Pt thin films prepared by physical vapour deposition such as sputtering, resistive heating, or electron beam heating techniques were used as the catalyst for counter electrodes [37, 93, 94, 97]. There are relatively few reports on the application of Pt NPs on DSSC counter electrodes. It is well known that Pt NPs, which have been employed for a wide variety of catalytic processes, display catalytic activity which depends on both the size and the crystal structure of the NPs [98-101]. In the bulk of these studies, Pt NPs were synthesized via bottom-up wet chemical routes and the size of the particles falls within the 4–10 nm window. One major drawback of chemical synthesis of Pt NPs is the presence of undesirable side-products which may lead to catalytic poisoning, adversely affecting sustained catalysis [102]. Regarding metal NPs prepared via physical vapour deposition processes, these are usually grown on substrates through a thermal dewetting technique [10, 12, 14, 72, 103-105]. It is worth noting that, among the NP characteristics obtained using this thermal dewetting approach, particle density is quite low and the size distribution is wider than expected for controlled optimal Pt loading on substrates. Moreover, the high temperatures required to prepare Pt NPs by thermal dewetting (in excess of 400 ^{o}C) [72, 105, 106] cannot be applied to some substrates, polymer-based flexible counter electrodes, for instance. Recently, highly catalytic Pt NPs on TCO, prepared by a chemical route, were tested as DSSC counter electrodes [106]. In this study, Calogero et al. transferred nominally 4–5 nm Pt NPs generated via wet chemistry onto FTO substrates, followed

by calcination up to 350 ^{o}C which resulted in the growth of some much larger NPs (~15 nm), making deconvolution of the catalytic activities of the residual small Pt NPs difficult. Likewise, no analysis on the crystallinity of these NPs and their role in catalytic activity was reported [106].

To the best of our knowledge, no systematic study on the effect of Pt NP size—particularly for sub-1 nm particles—on DSSC performance has been performed. Gaining an understanding of the lower size limit of Pt NPs viable for efficient catalysis is indeed essential for optimizing Pt usage in a multitude of catalytic reactions. In the case of DSSCs, determining the lower size limit of Pt NPs utilized at the counter electrodes and the NP characteristics dictating this size limitation will help answer some fundamental questions related to curtailing the quantity of Pt required for achieving efficient DSSCs, a crucial step towards attaining real world financial viability for DSSCs.

3.2 METHODS

The catalytic properties of Pt-decorated FTO electrodes were evaluated using electrochemical impedance spectroscopy (EIS) and cyclic voltammetry. The FTO electrodes are also used as counter electrodes in DSSC to determine solar cell efficiency. The experiments involving DSSC included fabrication of its different parts (photoelectrode, electrolyte, and counter electrode), DSSC assembly and photovoltaic efficiency measurement. TEM (transmission electron microscope) analysis was done to observe the Pt NPs used at the DSSC counter electrodes. Cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) were done to characterize the charge transfer properties and hence the catalytic activity of the aforementioned sputtered Pt NPs. Since Pt NP formation is the most novel aspect of this study, it is discussed below. Please see the appendix for more information for more standardized experimental details on photoelectrode

preparation, DSSC preparation and electrical characterization, impedance spectroscopy and cyclic voltammetry.

3.2.1 Size Dependent Pt NP Deposition

Pt was deposited on FTO coated glass substrates utilizing TTS parameters (30 W power, 23.8^{o} target angle) discussed previously in section 1.1 for different sputter durations spanning from 5 s to 120 min.

3.2.2 TEM and HRTEM Characterization of Pt NPs on FTO

To compare the areal density and size distribution of Pt NPs deposited on Al_2O_3 coated carbon grids with that on FTO, macroscopic shavings of the Pt coated FTO were obtained using a diamond-tip scribe. These shavings were then dispersed in DI water and placed on a 200# mesh copper grid for TEM analysis. Particular care was taken so that the TEM electron density was sufficiently low to avoid any beam-induced artefacts such as sintering and coalescence [107, 108]. For Pt NPs deposited for 5 sec, particle size and distribution were not reliable due to the poor image quality. The Pt NP size and distribution on FTO films were observed to be similar to the ones on Al_2O_3 coated carbon grids. HRTEM (high resolution TEM) was done to analyse the crystalline nature of the Pt NPs sputtered on the Al_2O_3 films. A 200 keV Technai HRTEM system was used to attain the HRTEM Pt NP images. Although analysing crystal properties of Pt NPs on FTO shavings would be ideal, this was not a practical option as due to rough FTO shaving surface and FTO nanocrystalline domains, correct observation of Pt NP crystals was hard and required prolonged exposure to the incident beam which could have led to beam induced NP diffusion and growth and henceforth improper analysis of the resultant Pt NP crystal structure.

3.2.3 Experimental details of DSSC fabrication

The experiments involving DSSC included fabrication of different parts of the DSSC (photoelectrode, electrolyte, and counter electrode), DSSC assembly and photovoltaic efficiency

measurement. TEM analysis was done to observe the Pt NPs used at the DSSC counter electrodes. Cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) were done to characterize the charge transfer properties and hence the catalytic activity of the aforementioned sputtered Pt NPs.

3.2.3.1 Photoelectrode Preparation

TiO_2 layers for the photoelectrode were prepared using doctor blading technique.[94] The TiO_2 paste (DSL 18NR-T) was purchased from Dyesol (Queanbeyan, NSW, Australia) with average TiO_2 particle size of ~20 nm. Fluorine doped tin oxide (FTO) (with a sheet resistance of 8 Ω sq^{-1}) was purchased from Hartford Glass Company (Hartford City, IN) and was used as the TCO substrate. A Kurt J. Lesker AXXIS electron beam evaporator was used to deposit ~20 nm compact layer of TiO_2 on the FTO substrate. This blocking layer is more important in case of organic dye sensitized solar cells.[109] Although the sensitization of the photoelectrode with the Ru-N719 reduces the electrolyte – FTO interactions at the photoelectrode (given the specific adsorption of Ru-N719 on the FTO surface [110]), the blocking layer was seen to further reduce the electrolyte – FTO interaction at the photoelectrode. This layer prevents the direct interaction of the electrolyte with the TCO and thereby reduces the open circuit voltage loss due to back transfer of electrons to the electrolyte from the TCO.[110-113] Also, according to Cameron et al., more reproducible results are obtained with the presence of a compact layer compared to the absence of it.[112] A 10 μm TiO_2 layer was doctor bladed on top of the TiO_2 compact layer coated FTO substrates and sintered at 500 °C for 30 min.[114] The resultant photoelectrode was soaked in 0.3 mM di-tetrabutylammonium *cis*-bis (isothiocyanato) bis (2,2′-bipyridyl-4,4′-dicarboxylato) ruthenium(II) (Ru-N719 dye photosensitizer) in ethanol for ~18 h.

3.2.3.2 Electrolyte preparation

The electrolyte solution consisted of a mixture of LiI (0.3 M), iodine (15 mM), 4-*tert*-butylpyridine (0.2 M) and ethanol (15 %, v/v) in acetonitrile.[115] Acetonitrile was chosen as the solvent because the iodide/triiodide kinetics are more facile in acetonitrile compared to other solvents.[96] Additionally, Hauch et al. showed the best charge transfer kinetics at the counter electrode while using acetonitrile as the solvent.[116]

3.2.3.3 DSSC Assembly

The TiO_2 photoelectrode was rinsed in ethanol to remove excess dye and after drying, the counter electrode (FTO with sputtered Pt) was sandwiched on top, with 70-μm double-sided Kapton tape as the spacer. Two 1-mm diameter holes were drilled in the counter electrode for the purpose of electrolyte delivery.

3.2.3.4 DSSC Efficiency Measurements

Current-voltage (I–V) measurements were conducted on the finished DSSCs to measure the maximum output power and cell efficiencies. I–V measurements on the DSSC were conducted using a Keithley 2400 Sourcemeter under AM 1.5 (100 mW cm^{-2}) illumination provided by a 150 W Xenon lamp. Eight (8) μL of the electrolyte was introduced into the cell through the drilled holes and a 0.25 cm^2 mask was used to control the cell illumination area. All efficiency measurements were carried out at ambient temperature (~300 K).

3.2.4 Electrochemical Impedance Spectroscopy (EIS) analysis

EIS studies were conducted to analyze the charge transfer characteristics at the electrolyte-counter electrode interface. A symmetric electrode sandwich cell was employed for characterizing the electrochemical impedance properties of the Pt sputtered counter electrodes. The setup used was designed to be as similar as possible to "real world" DSSCs. This electrochemical cell consists of two identical Pt-sputtered FTO coated glass substrates sealed with a double sided Kapton tape, which served as a spacer. The cell was filled with an electrolyte consisting of 0.5 M LiI and 0.05 M I_2 in acetonitrile. These concentrations are typical for DSSCs.[93-95] The distance between the two electrodes was about 70 μm - the thickness of the Kapton tape. All measurements were carried out at room temperature (~300 K). This type of setup has the following advantages: the electric field on the surface of the two identical electrodes is homogeneous, diffusion is the only transport mechanism in the electrolyte as convection does not occur because the cell is very thin, and migration is negligible because the electric field in the inner cell is shielded due to the high ionic concentration in the electrolyte.[116] Thus, the reproducibility of measurements in this sealed device is much better than open configurations.

The cell created in the manner described above was connected to an Agilent 4294A Precision Impedance Analyzer, via a 16047E test fixture. The impedance of the system was recorded at 20 frequencies between 100 Hz to 100 kHz using a 10 mV (p-p) source voltage without bias. The experiments were repeated for 3 sets of electrodes for each electrode type (that differ in the duration of sputtering).

3.2.5 Cyclic voltammetry (CV) analysis

CV was done on some of the DSSC counter electrodes under contention in an electrolyte containing the iodide/triiodide redox specie. The triiodide oxidation/reduction peak positions and peak current densities were analyzed for FTO electrodes with different Pt coverage sputtered using the TTS system. A continuous Pt thin film deposited by sputtering was studied as the control substrate. The aforementioned Pt sputtered FTO electrodes and the continuous Pt thin film were applied as working electrodes in the CV experiments. The counter electrode used was Pt wire gauze and a Pt wire dipped in the electrolyte solution was chosen as the pseudo reference electrode. Ferrocene was used as the internal standard for all measurements as ferrocene is known to maintain a constant redox potential in organic solvents such as acetonitrile.[117] This addition of the internal standard overrides the need of having a reference electrode with a fixed potential as all potentials can be recorded w.r.t the ferrocene reduction potential.[118] The reversibility of the redox potential ferrocene is compromised at potentials exceeding 1V/s, therefore a much lower potential scan rate of 30 mV/s was used for each experiment.[117] The electrolyte used was 5 mM LiI + 5 mM I_2 in a 0.1 M solution of $LiClO_4$ in acetonitrile. The $LiClO_4$ was used as the supporting salt enhancing the conductivity of the electrolyte solution in acetonitrile.[40, 119-122] LiI was added to the acetonitrile in the N_2 saturated glove box to prevent its oxidation in ambient conditions and formation of –OH bonds at the salt surface reducing the solubility of the salt in acetonitrile. A 5-10 min N_2 purge was done for each sample before doing the CV measurements.

3.2.6 UV-Vis transmission analysis of Pt sputtered counter electrodes

Apart from high catalytic activity, the Pt NP decorated FTO electrodes also depict relatively high transmittance which is an ideal feature for back illuminated DSSC counter electrodes. Back

illumination is the generally preferred method for DSSCs which use TiO_2 nanowires grown on Ti foils or other low transmittance materials as the photo-anode [38-40, 123-126]. In such DSSCs, transmittance of the counter electrode is an essential factor affecting the amount of light entering the solar cell and thereby affecting the cell efficiency. Regular FTO coated glass, the base TCO utilized for most DSSCs, has a transmittance ~70-80 % in the visual range (Figure 14). Lin et al. [38] studied the transmittance drop on Pt sputtered ITO electrodes. Their sputter current used was 20 mA , and they reported a drop in transmittance starting at their 10 sec Pt deposition (~2 % loss for 10sec deposition, ~10 % loss for 20 sec deposition and so on) done on an indium tin oxide (ITO) electrode [38]. Although their optimum DSSC performance was recorded at 30 sec Pt deposition, the recorded transmittance drop was ~ 30 %. This would be considered a significant loss in the incoming light intensity for back illuminated DSSCs. A transmittance Figure 14 shows the UV-vis spectra of Pt sputtered FTO and ITO substrates. In the UV-Vis spectra of FTO-Pt deposited slide, it was observed that the transmittance values for the Pt sputtered FTO samples were slightly higher compared to the FTO transmittance (Figure 14). This was concluded to be within the 90 % confidence interval of the average transmittance value of the FTO film coated glass slides (transmittance values averaged for 10 different slides). This relatively large error bar can be attributed to the highly scattering nature of the FTO films. In essence, this study reports negligible change in transmittance for FTO films with low Pt deposition durations. This negligible drop in transmittance can be attributed to sub-2 nm grain size of the Pt NPs at Pt deposition times < 45 sec leading to negligible scattering from the low deposition time sputtered Pt. Transmittance values remained practically unchanged up to the 45 sec Pt deposition. A recent publication by Calogero et al reports optical transmittance values of a Pt NP decorated counter electrode fabricated by bottom up approach and chemical reduction [106]. The Pt NP distribution is

relatively broad with majority of Pt NPs ranging between the diameters of 2-4 nm. The reported transmittance drop on FTO is ~ 10% which is significantly high compared to the negligible drop in optical transmittance reported in this paper.

Sputtering under similar conditions was also done on ITO substrates to effectively see the role of Pt deposition duration in determining the transmittance of ITO films, which have negligible scattering characteristics. Comparing the transmittance loss reported by Lin et al. for sputter depositions of Pt on ITO films, it can be seen from Figure S3 that there is a ~2 % transmittance loss for the 45 sec Pt deposition – our reported optimum Pt loading compared to 30 % loss at Lin et al.'s optimum Pt loading (30 sec deposition at 10 mA sputter current). Also, the UV-Vis spectra on Pt sputtered FTO samples do not show any discernible drop in transmittance up to 45 sec Pt deposition (avg. particle diameter ~ 1.56 nm) (Figure 14). After the 45 sec Pt deposition, a steady decrease in transmittance can be seen starting at the 120 sec deposition and the transmittance drops by 94 % for the 50 nm Pt film. It can be seen that negligible transmittance loss at our fabricated counter electrodes makes them ideal for use in back illuminated DSSCs.

Thus, it can be seen that these low Pt loading FTO substrates provide good transmittance; an essential feature for back illuminated DSSCs and are especially advantageous as optimum transmittance counter electrodes.

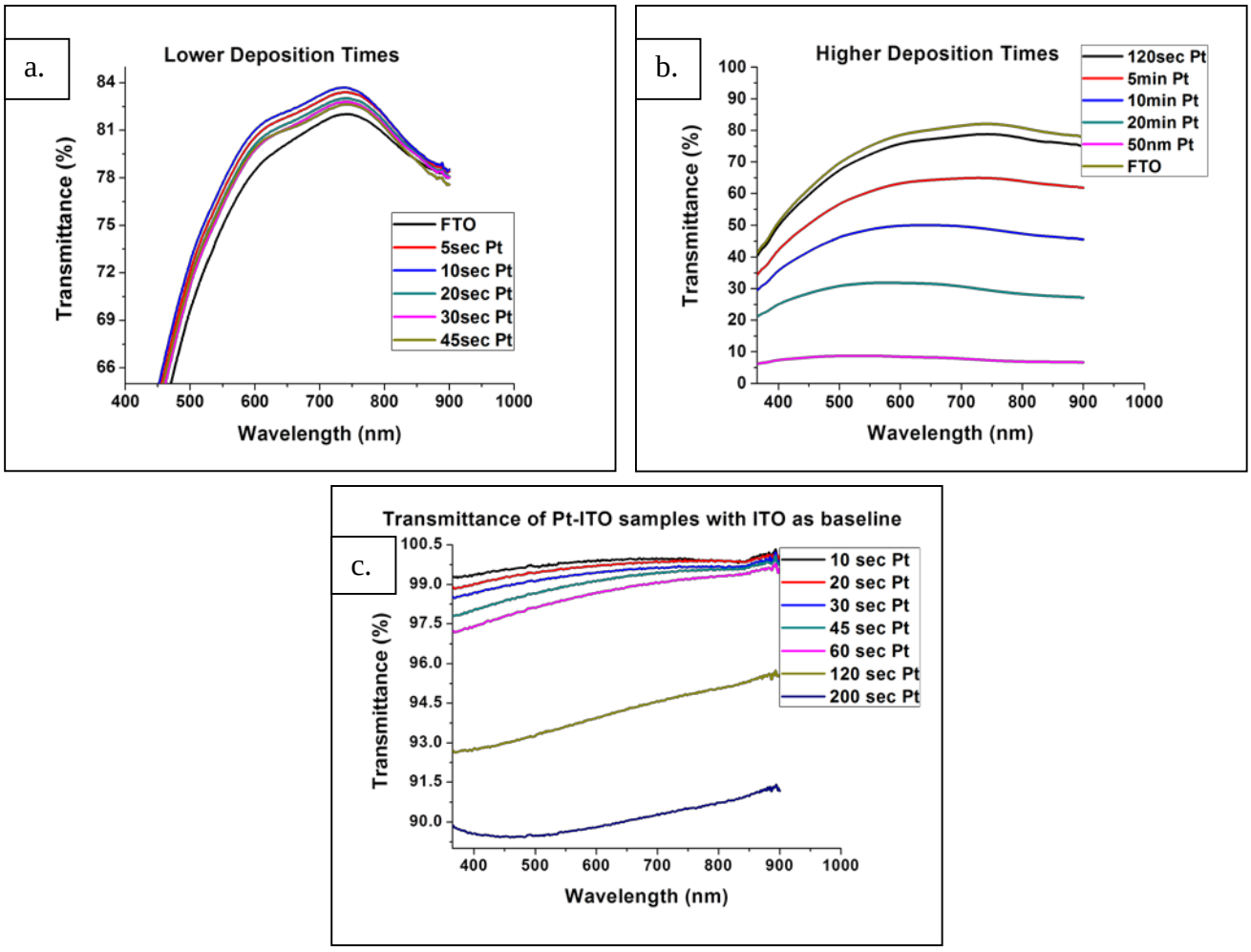


Figure 14: Absorption spectra of the different time Pt sputtered FTO substrates- a) Lower deposition times; b) higher deposition times; c) absorption spectra of Pt sputtered ITO substrates with ITO as baseline

3.3 RESULTS AND DISCUSSIONS

This work investigates the effects of size, distribution, and crystalline characteristics of ultra-fine (sub-2 nm) Pt NPs (fabricated by sputtering Pt on FTO surfaces) on the overall charge transfer resistance and I3– reduction mechanism. In particular, it was examined how the catalytic activity (the I3– reduction rate and the charge transfer characteristics) of the Pt NPs vary as functions of the NP size (a characteristic that was reproducibly controllable in the sub-2 nm size regime) and the NP crystalline structure (which also happens to be strongly related to the NP size in the regime

examined). This allows us to study the efficiency-boost provided to the DSSC as a function of the Pt loading. This section presents the growth mechanism and physical characteristics (size, distribution, crystalline nature) of the sputtered Pt NPs based on the acquired TEM and HRTEM images. Electrical impedance measurements were taken on the fabricated Pt-FTO counter electrodes to study the charge transfer characteristics followed by an examination of the photovoltaic efficiency of the DSSCs which is presented next. Finally, cyclic voltammetry was performed on selected electrodes to understand the role of size and crystallinity on catalytic activity and DSSC efficiency of the crystalline Pt NP based electrodes compared to a continuous Pt thin film.

3.3.1 Pt NP growth on FTO surface

In order to ascertain whether the Pt NP characteristics on FTO substrates were similar to those deposited on Al_2O_3 substrates, TEM analysis was done on a 45 s Pt sputtered FTO shavings (acquisition method discussed in experimental section). The TEM image of the 45 s Pt sputtered FTO shaving is displayed in Figure 15. The NP size distribution on FTO substrate (1.45 ± 0.39 nm) is very similar to the size distribution on Al_2O_3 substrate (1.56 ± 0.42 nm). Thus, all the calculations done above can be safely used in further calculations to predict Pt NP characteristics on FTO.

As listed in Table 3 the amount of platinum present for the 30 s and 45 s Pt depositions are ~10^{-3} times that of a 50-nm platinum film. An intuitive way of conveying the platinum loading is to calculate the "nominal thickness" of the platinum "layer." For such a calculation, one assumes all the platinum present is in the form of isolated spheres distributed evenly over the FTO surface. This value is provided in Table 3. Also provided in Table 4 are predicted values of the nominal thicknesses at low-time intervals based on measured thicknesses of uniform Pt films (10–45 nm) obtained with long sputtering times (20-90 min). The extrapolation to low time intervals is justifiable as long as the sputtering rate (number of Pt atoms deposited

per unit time) is uniform throughout the process. The credibility of our spherical model was verified by the fact that the Pt loadings (nominal thicknesses) obtained by using this model fell within the range of values predicted by extrapolation of measured thicknesses of uniform layers to low time intervals.

Pt Deposition Time (s)	Nominal Thickness (nm)	Estimated number of Pt atoms in each particle (Assuming FCC structure)	Avg. Pt surface area (m^2 g^{-1})	Avg. Pt loading (g cm^{-2})	Pt loading relative to 50 nm Pt film[a]
30	0.0565	63.47	228.16	1.210×10^{-7}	9.865×10^{-4}
45	0.1186	131.77	178.84	2.543×10^{-7}	2.371×10^{-3}

[a] The Pt loading at a given deposition time divided by the Pt loading for a 50-nm continuous Pt film.

Table 3: Pt loading at different sputtering times

Pt Deposition time (s)	Nominal Thickness Range as Obtained from the linear Fit (nm)	Mean Nominal Thickness as Obtained from the linear Fit (nm)	Mean Nominal Thickness as calculated by the spherical particle growth model (nm)
30	(–0.0676[a], 0.1527)	0.0426	0.0565
45	(–0.0449[a], 0.2757)	0.1154	0.1186
120	(0.6075, 0.8905)	0.7490	–

[a] The improbable negative value for the nominal thickness was obtained as a lower range for the mean nominal thickness within a 90% confidence interval.

Table 4: Experimentally predicted and theoretically calculated nominal thicknesses

It is important to note that Pt NP crystal growth is governed by the growth process of sputtered Pt NPs. The NP growth process is governed by surface energy difference between the incoming Pt atom (surface energy > 2500 dynes/cm) and the substrate [9, 14, 17]. Since Pt growth on FTO is not epitaxial in nature, the Pt NP crystal growth is likely governed by the surface energy difference rather than the crystalline

structure of the FTO surface. The measured surface energy for Al_2O_3 used for HRTEM analysis was ~30 dynes/cm and that for the cleaned FTO substrates was ~56 dynes/cm. Both these surface energy values are significantly less than that of the incoming Pt atom and thus the size dependent Pt NP crystal growth on these surfaces should be similar.

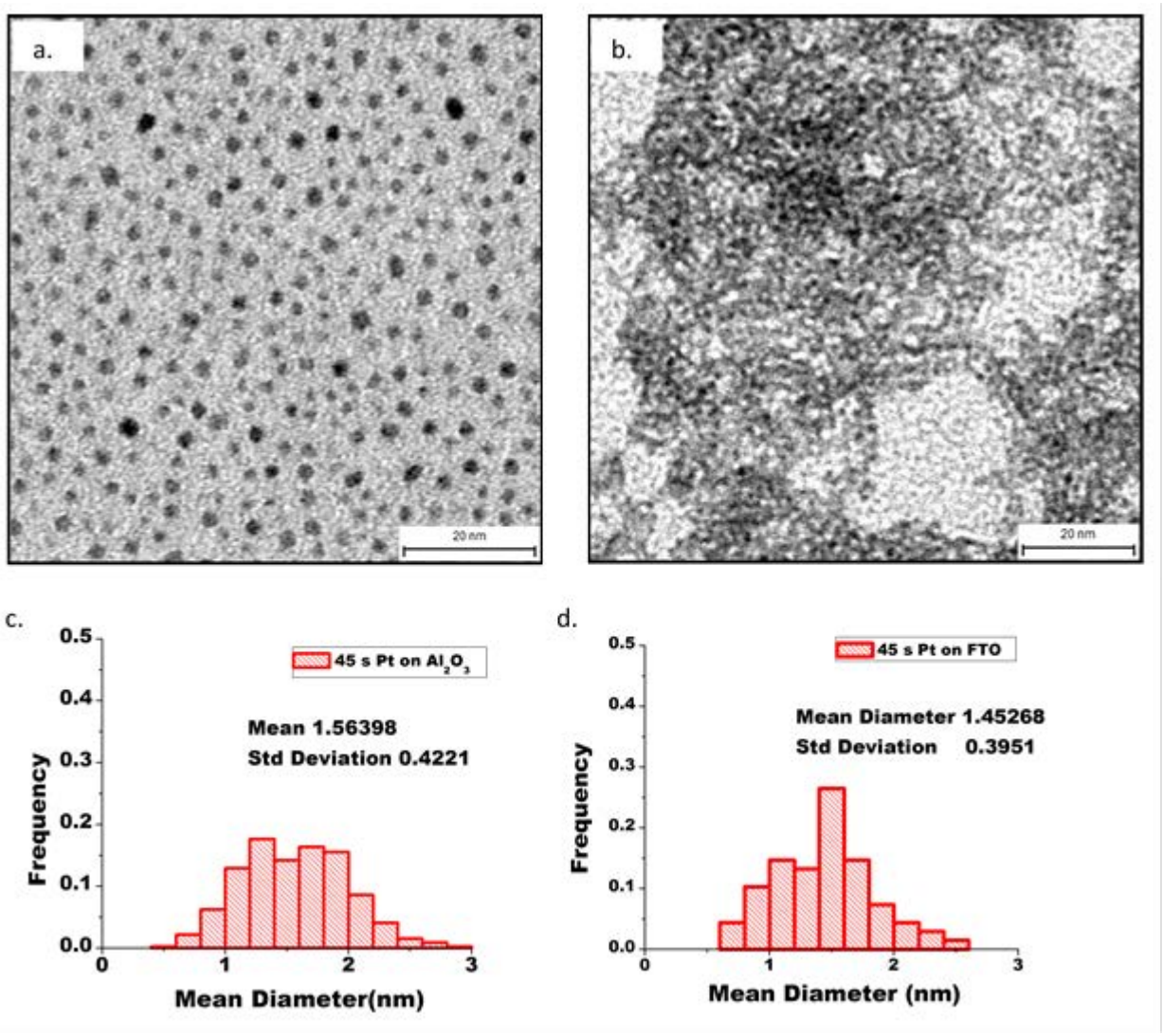


Figure 15 TEM images of (a) 45 s sputtering of Pt on Al2O3 and (b) 45 s sputtered Pt-FTO shavings and the corresponding particle size histograms (c) and (d), respectively.

Analysing the crystalline nature of these sputtered NPs is especially important since to our knowledge, no extensive study on triiodide reaction kinetics at various crystalline facets or its dependence on crystalline nature of Pt NPs is available in literature. Hsieh et al. suggest the <100> and <110> facets of Pt could possess better electrocatalytic ability to triiodide reduction [127]. However, the adsorption of Iodide anion on different Pt facets from the electrolyte also plays a role in determining the triiodide reduction rate [128]. Further discussion of particle size and crystallinity dependent catalytic activity of Pt NPs is discussed in this chapter.

It is also worth noting that formation of defects on transparent conducting oxides (TCO) due to plasma exposure is a well-documented issue and needs to be addressed while sputtering Pt NPs in the presence of Ar plasma. These defects can lead to formation of surface traps and lower the Fermi-level of the FTO surface making electron transfer to Pt (5.65 eV) not a thermodynamically favourable process. However, based on studies by Kim et al. on ITO substrates in the presence of plasma [129], plasma damage was only observed on the ITO surface when a 20 W bias was applied to the substrate and the ITO substrate without bias did not show any signs of damage. In our sputtering process, the substrate is grounded and the particles hitting the substrate are essentially Pt atoms. Also, a tilted target magnetron sputtering system was used which helps strike an Ar plasma at mere 30 W (compared to 100 - 200 W where most metal sputtering is done) and the strong magnetic field near the target keeps the plasma and generated electrons near the target surface. Damage free ITO films were fabricated by Kim et al. after confining the plasma near the target surface [130]. Also, these Pt NPs deposited on Al2O3 have previously been used under similar conditions for single electron memory devices and no device performance deterioration due to oxide surface damage was observed [4-7]. Thus, there should be minimum damage on the FTO substrate as a result of this deposition process.

3.3.2 Electrochemical Impedance Spectroscopy (EIS) analysis

Electrochemical impedance spectroscopy (EIS) was used to analyse the charge transfer characteristics at the electrolyte-counter electrode interface. Lower charge transfer resistance obtained from EIS is indicative of faster charge transfer kinetics of the electrode under consideration and thus helps determine its catalytic activity. The electrical behavior of the measurement cell, assembled as described in the experimental section, can be described by the circuit shown in Figure 16. Here, R_{C1} and R_{C2} are the charge transfer resistances at the two individual electrodes; R_S is dominated by the Ohmic resistance of the TCO layer [116] Also present are two constant phase elements (CPEs), one at each electrode, that arise due to the "ionic double layer" at the electrodes. The ionic double layer is often modeled as an ideal capacitor [131]. However, due to the roughness of the TCO substrate surface, the electrical behavior of the electrolyte - counter electrode deviates slightly from that of an ideal capacitor, [116] hence it was chosen to model it as a CPE instead.

The CPE is a non-intuitive circuit element that replaces a capacitor in a circuit when there is some type of non-homogeneity in the system, delaying or impeding the movement of charge carriers [132]. Mathematically, a CPE is an element whose impedance (Z) is given by the equation

$$Z = 0 - j\,(1 / (\omega Q)^{n}) \qquad (12)$$

where j is the square root of -1, ω is the frequency, and Q and n are the magnitude and "phase angle" of the CPE, respectively. One may also note that if n=1 then the impedance of the element

is identical to that of an ideal capacitor with the same magnitude. If one assumes the two electrodes used are identical, then the circuit may be simplified to the one shown in Figure 16 (b).

As described in the experimental section, an impedance analyzer was used to measure both components of the impedance (Z) (the in-phase resistance (R) and the out-of-phase reactance (X)) at 20 different frequencies (ω) between 100 Hz to 100 KHz. The geometrically equi-spaced frequencies are selected by the instrument itself. The Z vs. ω data obtained from the impedance analyzer is then fit to the equivalent circuit shown in Figure 16 (b), using the software Z-View. It accepts as input, the measured values of R and X at multiple frequencies, allows the user to propose an equivalent circuit for the material being investigated, and provides an estimate of the values of the individual elements in the equivalent circuit (R_C, R_S, magnitude the CPE (Q) and its phase angle (n) in our case), along with an "error" of the estimate.

The effective charge transfer resistance (R_{Ct}) is calculated as

$$R_{Ct} = A\,(R_c / 2) \qquad (13)$$

where R_c is the value of the resistor provided by the Z-view fit, and A is the surface area of the electrode. Similarly, the double layer capacitance is given by

$$C_{dl} = 2\,Q / A \qquad (14)$$

where Q is the magnitude of the CPE, as provided by the Z-view fit to the impedance data. The phase angle of the CPE was, in all cases, ≥ 0.95, showing that the double layer, while not exactly ideal, was still largely capacitive.

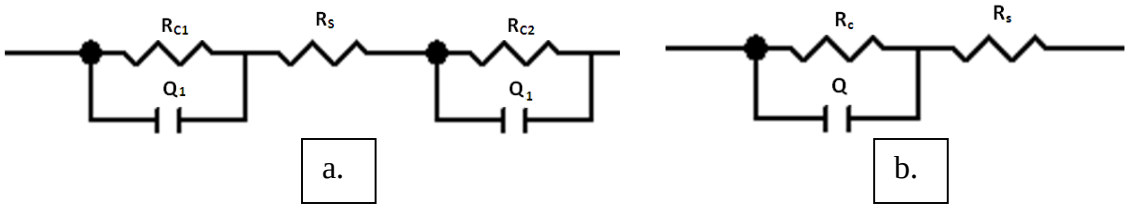


Figure 16: Equivalent circuits for the impedance analysis: (a) equivalent circuit for the individual electrodes; (b) combined equivalent circuit

R_{Ct} represents the charge transfer resistance for the reduction of triiodide at the electrodes, and C_{dl} represents the double layer capacitance. The average (and standard deviation) of the R_{Ct} and C_{dl} values obtained for three separate sets of electrodes (for each sputtering duration) are listed in Table 5 and plotted as a function of the duration of sputtering in Figure 17.

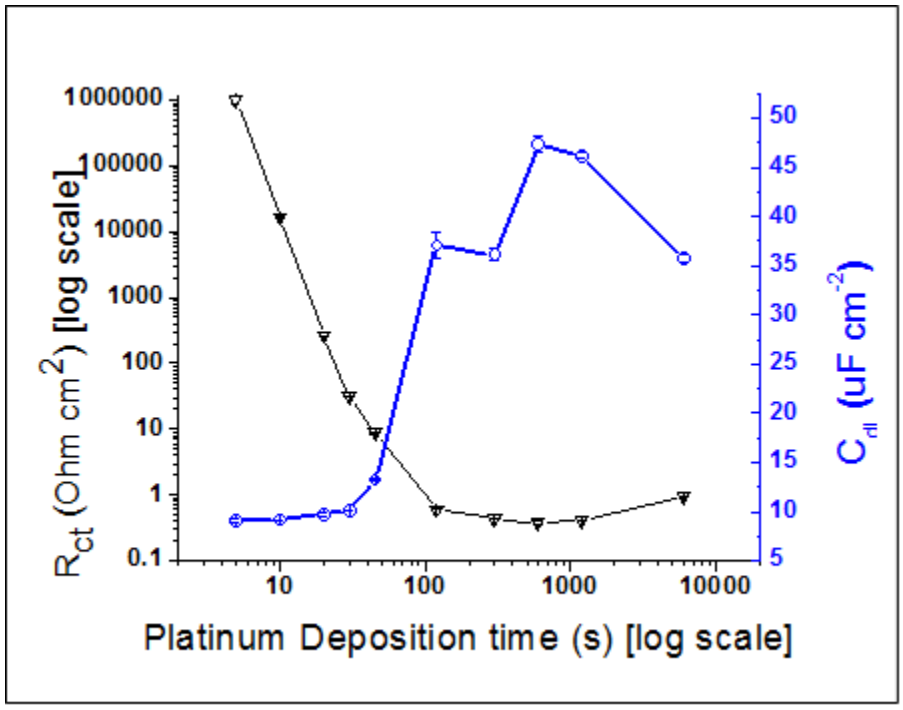


Figure 17: Plots of charge transfer resistance (R_{Ct}) and double layer capacitance (C_{dl}) for counter electrodes versus Pt deposition time.

As is evident from Figure 17, R_{Ct} decreases with increasing duration of Pt sputtering. Lower R_{Ct} values essentially imply higher exchange current densities at the electrolyte – counter electrode interface, thereby signifying higher catalytic activity. Even with just 10 s of Pt sputtering (when the Pt clusters are very small, i.e., 0.76 nm mean diameter, and their areal density is relatively low (4.71×10^{12} cm^{-2}), the R_{Ct} of the counter electrode decreases by about 2 orders of magnitude. The lowest charge transfer resistance value was 0.379 Ω cm^2 which corresponded to the 600 s Pt sputtered-FTO electrodes and implied a relatively high exchange current density of ~34 mA cm^{-2} [4].

The continued exponential drop in the charge transfer resistance resulting from the controlled increase in the size of the Pt NPs indicates the enhanced catalytic activity of Pt at the nanoscale. This increase in catalytic activity can be attributed to faster electron transfer within the NP crystalline structure. Low surface coverage of the counter electrodes prepared at lower Pt sputtering durations (as is demonstrated by their low Pt loading – see Table 3 for 5–20 s deposition), and their non-crystalline nature are believed to inhibit efficient electron transfer at the electrolyte/counter electrode interface, thereby contributing to high R_{Ct}. This high charge transfer resistance can represent a combination of two phenomena. Firstly, for the lower time depositions, Pt coverage of FTO is very low. Since FTO itself is a poor candidate for triiodide reduction, low coverage of Pt contributes towards sluggish charge transfer from the electrode surface. Secondly, for the sub-nanometre sizes of Pt NPs obtained for lower Pt deposition times, electron trapping and collapse of crystal structure are known phenomena and further contribute towards increasing the charge transfer resistance [7, 8, 133]. The relation between Pt NP crystallinity at the FTO counter electrode and DSSC efficiency is discussed in detail in section 2.3.3. Hauch et al. report an R_{Ct} value less than 10 Ω cm^2 should result in good DSSC performance [116]. Here, a 45 s Pt

deposition with a mean NP diameter of 1.56 nm has an R_{Ct} value of 8.78 Ω cm^2 (table 3), thus fulfilling this requirement for fabricating counter electrodes for high performance DSSCs.

3.3.3 DSSC Efficiency Measurements

Impedance spectroscopy results discussed in the previous section show remarkable enhancement in catalytic activity upon introducing extremely low Pt loadings to the FTO counter electrode. These Pt NP-decorated counter electrodes were incorporated into a finished DSSC to analyse the effect of Pt NP loading on the DSSC counter electrode. To date, little work has been done to study the effect of sub-2 nm Pt NPs at the counter electrode on DSSC efficiency. Fang et al. reported consistent efficiencies of 4.9% for a Pt film (2 nm thickness minimum) on FTO, no focused study on the use of sub-2 nm Pt NPs at the DSSC counter electrode has been reported [37]. Although researchers have used Pt NPs at counter electrodes of DSSCs before, the size distributions are broad, and the Pt NPs studied are usually larger than 2 nm in diameter [134-137]. The IV characteristics, efficiency, and fill factor of DSSCs with varying Pt loadings at the counter electrode were studied to correlate the high catalytic activity at low Pt loadings with DSSC performance. The obtained efficiencies and fill factor values are plotted in Figure 18 and the corresponding typical IV curves for representative DSSCs are plotted in Figure 19. The 50 nm sputtered Pt film on FTO was used as the control counter electrode for this study. As noted from Figure 18 and Table 5, the DSSC efficiencies and fill factors rise with increasing Pt sputtering times, and after a certain Pt loading (1.21×10^{-7} g cm^{-2}, 30 s Pt sputtering, ~1.2 nm average particle diameter), reach a maximum and start to plateau.

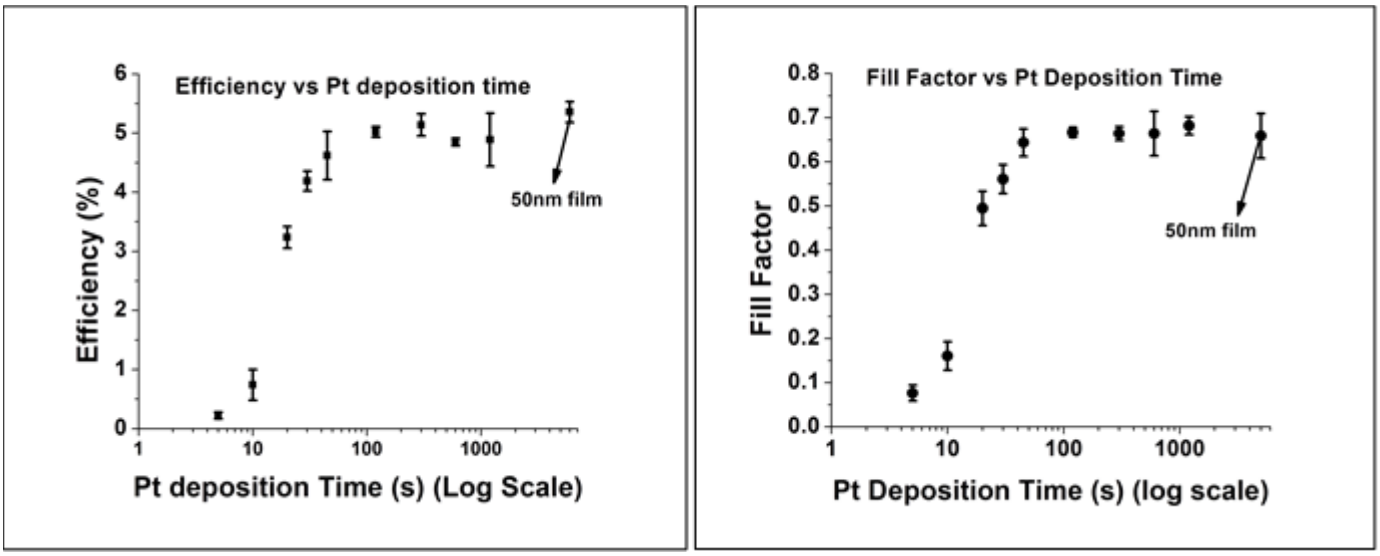


Figure 18: (a) DSSC efficiency at the CE and (b) DSSC fill factor as a function of Pt deposition time.

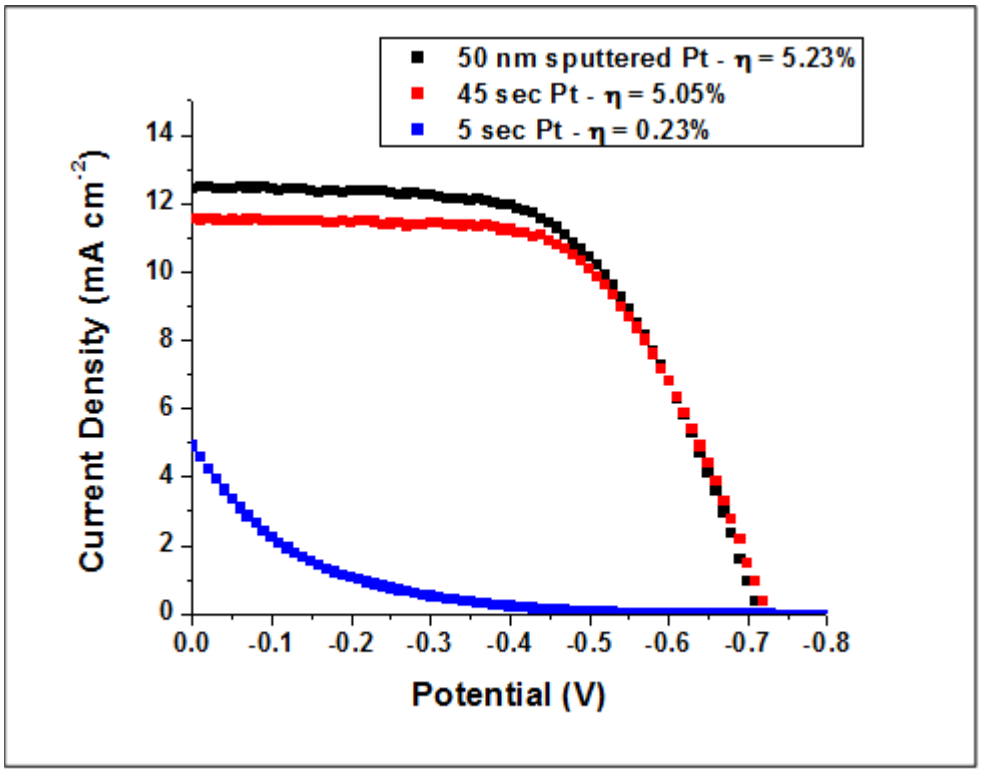


Figure 19: Typical I–V curves of DSSCs with counter electrodes based on Pt deposition times of 5 s and 45 s compared to that of a DSSC with a 50-nm sputtered Pt counter electrode.

This behaviour can be attributed to the charge transfer resistances reducing to ~30 Ω cm^2 after just 30 s of Pt deposition and to less than 10 Ω cm^2 for the 45 s Pt deposition onto FTO as compared to ~10^6 Ω cm^2 resistance for a neat FTO substrate (table 4). The enhanced catalytic activity for sub-2 nm Pt NPs (30 s and 45 s depositions, specifically) is also confirmed by their respectable DSSC performance (comparable to a 50-nm thin film) regardless of low surface coverage of Pt (low surface area available for the triiodide reduction at these counter electrodes). The Pt surface area available for triiodide reduction (A_{Pt}) per unit area at the DSSC counter electrode can be expressed by the following equation:

A_{Pt} = (Pt NP specific surface area (m^2/g)) **X** (Pt loading(g/m^2))

(11)

For a continuous 50-nm sputtered Pt film on FTO, A_{Pt} is essentially unity. However, based on the Pt NP specific surface area and Pt loading values listed in Table 3, the A_{Pt} values are 0.28 for the 30 s sputtered Pt NPs and 0.45 for the 45 s sputtered Pt NPs. Since comparable DSSC performance to a 50 nm sputtered Pt film can be seen starting at a 30 s Pt deposition (table 5), and given their relatively low overall Pt counter electrode coverage, it can be determined that the crystalline Pt NPs have a higher catalytic activity as compared to bulk Pt. Counter intuitively, the low fill factors at lower Pt loadings (Pt NPs under 1 nm in diameter) can be attributed to high charge transfer resistances as seen in Table 5. Sun et al. reported a Pt NP lower size limit of 1 nm for their use as efficient catalysis [133]. This size limitation is attributed to the collapse in crystalline structure observed using theoretical simulations for unsupported spherical Pt NPs under 1 nm in diameter. The extremely low Pt loaded counter electrodes in this case ($t \leq 20$ s) are under 1 nm average size (table 1), and based on the aforementioned Pt NP growth characteristics and HRTEM analysis, are not crystalline in nature. Even though there is a significant rise in efficiency (from less than 1% to

3.24 ± 0.18 %) and a drop in charge transfer resistance (from greater than 10 MΩ cm^2 to 260.8 ± 1.2 Ω cm^2) at 20 s Pt sputtered counter electrodes, this was attributed to a higher Pt concentration at the counter electrode. The DSSC fill factor for the shorter time (t ≤ 20s) Pt sputtered is still low (0.495 ± 0.038), and the catalytic activity is poor due to inefficient charge transfer at the Pt NPs. For further discussion of inefficient charge transfer at short Pt deposition times, see Section 2.3.4. The role of parasitic resistances hampering solar cell fill factors is well known, and the R_{Ct} at the electrolyte/counter electrode interface imparts a similar effect. The drastic drop in R_{Ct} starting at 45 s Pt (avg. diameter 1.56 nm) deposition is mirrored in a rise in the efficiency and fill factor for DSSCs with 45 s Pt–FTO as their counter electrodes. There is little deviance in efficiencies and fill factors for the higher Pt loading counter electrodes beyond the 45 s Pt deposition time. The open circuit voltage was consistent at ~0.7 V for all counter electrodes.

Counter electrode[a]	R_{ct} **(Ω cm^2)**	C_{dl} **(μF cm^{-2})**
5 s Pt	$>1 \times 10^6$	9.12 ± 0.12
10 s Pt	1.641 (± 0.016) × 10^4	9.17 ± 0.01
20 s Pt	(2.608±0.012) × 10^2	9.74 ± 0.21
30 s Pt	30.65 ± 0.21	10.10 ± 0.06
45 s Pt	8.780 ± 0.242	13.23 ± 0.02
120 s Pt	0.607 ± 0.005	37.06 ± 1.33
5 min Pt	0.435 ± 0.007	36.11 ± 0.64
10 min Pt	0.379 ± 0.019	47.32 ± 0.83
20 min Pt	0.404 ± 0.010	46.18 ± 0.27
50 nm Pt	0.922 ± 0.019	35.77 ± 0.46

[a] All counter electrodes were based on Pt deposited on FTO.

Table 5: Charge transfer resistance (Rct) and double layer capacitance (Cdl) for different time Pt sputtered counter electrodes

Counter Electrode[a]	Avg. Pt NP diameter (nm)	Avg. Pt loading (g cm^{-2})	Efficiency (%)	Fill Factor (FF)
5 s Pt	Below 0.5	–	0.22 ± 0.06	0.076 ± 0.018
10 s Pt	0.76	–	0.74 ± 0.26	0.161 ± 0.032
20 s Pt	0.93	–	3.24 ± 0.18	0.495 ± 0.038
30 s Pt	1.23	1.210×10^{-7}	4.19 ± 0.17	0.561 ± 0.032
45 s Pt	1.56	2.543×10^{-7}	4.62 ± 0.41	0.644 ± 0.031
120 s Pt	Particle coalescence	–	5.02 ± 0.09	0.667 ± 0.011
5 min Pt	Particle coalescence	–	5.14 ± 0.18	0.664 ± 0.016
10 min Pt	Film formation	–	4.85 ± 0.06	0.665 ± 0.051
20 min Pt	Film formation	2.325×10^{-5}	4.89 ± 0.45	0.682 ± 0.020
50 nm Pt	Film formation	1.073×10^{-4}	5.36 ± 0.18	0.659 ± 0.051

[a] All counter electrodes were based on Pt was deposited on FTO.

Table 6: Performance characteristics of DSSCs fabricated with different Pt loadings at the counter electrodes

Thus, based on the DSSC efficiency data, the optimum Pt loading is approximated to around 2.54 x 10^{-7} g cm^{-2} (45 s Pt deposition time, Table 6) which contains approximately 420 times less Pt as compared to a 50-nm Pt film and 17 times less as compared to a 2-nm Pt film. To the best of our knowledge, this optimized Pt loading is the lowest reported in the literature (see listed optimized Pt loading values from published literature in [138] and those reported in [96, 135, 137, 139]). Also, comparable efficiencies were generated with 30 s deposition time Pt–FTO counter-electrodes which has a Pt loading of ~1000 times less than the 50-nm Pt film. As explained in the previous section, it is understood that the DSSC efficiency is a function of Pt catalytic activity as well as surface coverage. Thus, maximizing Pt surface coverage and maintaining crystalline NPs (reducing inter-NP distance) should provide a further boost in DSSC efficiency.

3.3.4 Cyclic Voltammetry Analysis

To understand the true catalytic activity of the Pt sputtered FTO electrodes, cyclic voltammetry (CV) analysis was done in an electrolyte containing the triiodide/iodide redox species. Ferrocene was added as an internal standard in these CV measurements [117, 118]. A typical CV curve stating the reactions indicative of the iodide/triiodide complex redox peaks and the ferrocene redox peaks at a continuous sputtered Pt film is depicted in Figure 20. For the purpose of DSSCs, peak 2 provides major information as it involves reduction of triiodide to iodide, the reaction that occurs at the counter electrodes of DSSCs [40, 119-121, 140-142]. A cathodic shift in this triiodide reduction potential is desirable for more efficient counter electrodes as it indicates that the electron transfer required to reduce triiodide requires lower energy and is more efficient [142]. CV curves which represent the I^-/I_3^- redox couple containing electrolyte after ferrocene addition at FTO for 10 s Pt, 20s Pt, 45 s Pt and Pt thin film-coated electrodes are displayed in Figure 22.

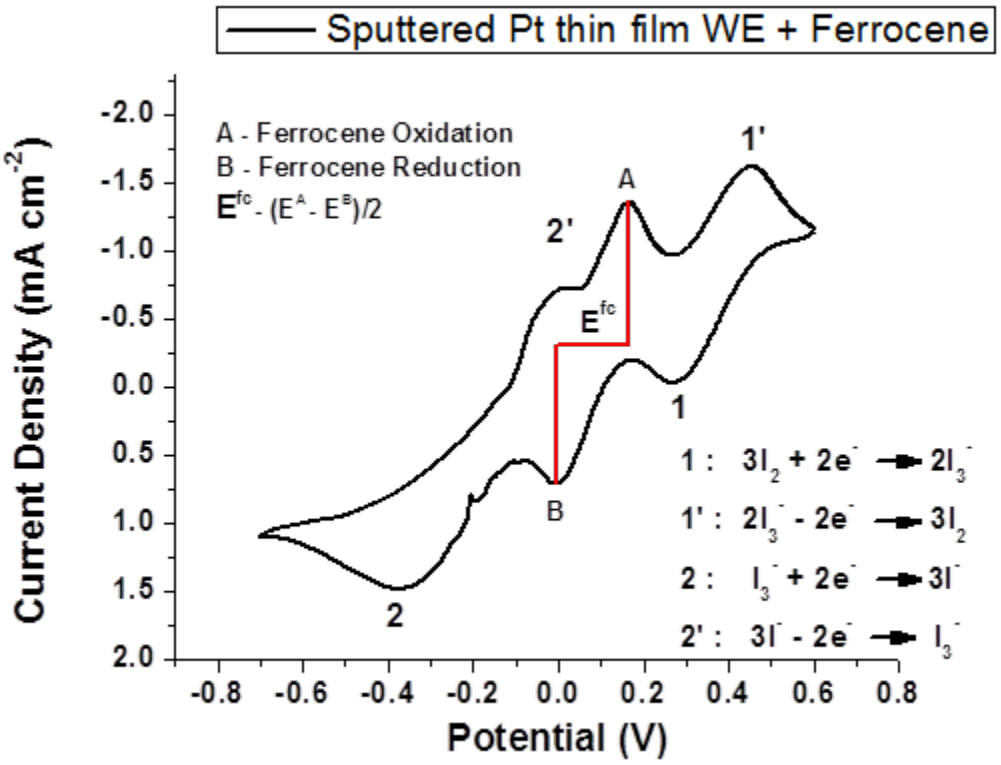


Figure 20: A typical CV curve listing the redox reactions and the corresponding iodide/triiodide and the ferrocene redox peaks. All potentials are referenced to a Pt wire pseudo-reference electrode.

Additional CV curves listing the different redox peaks for all studied Pt sputtered electrodes are provided in Figure 21.

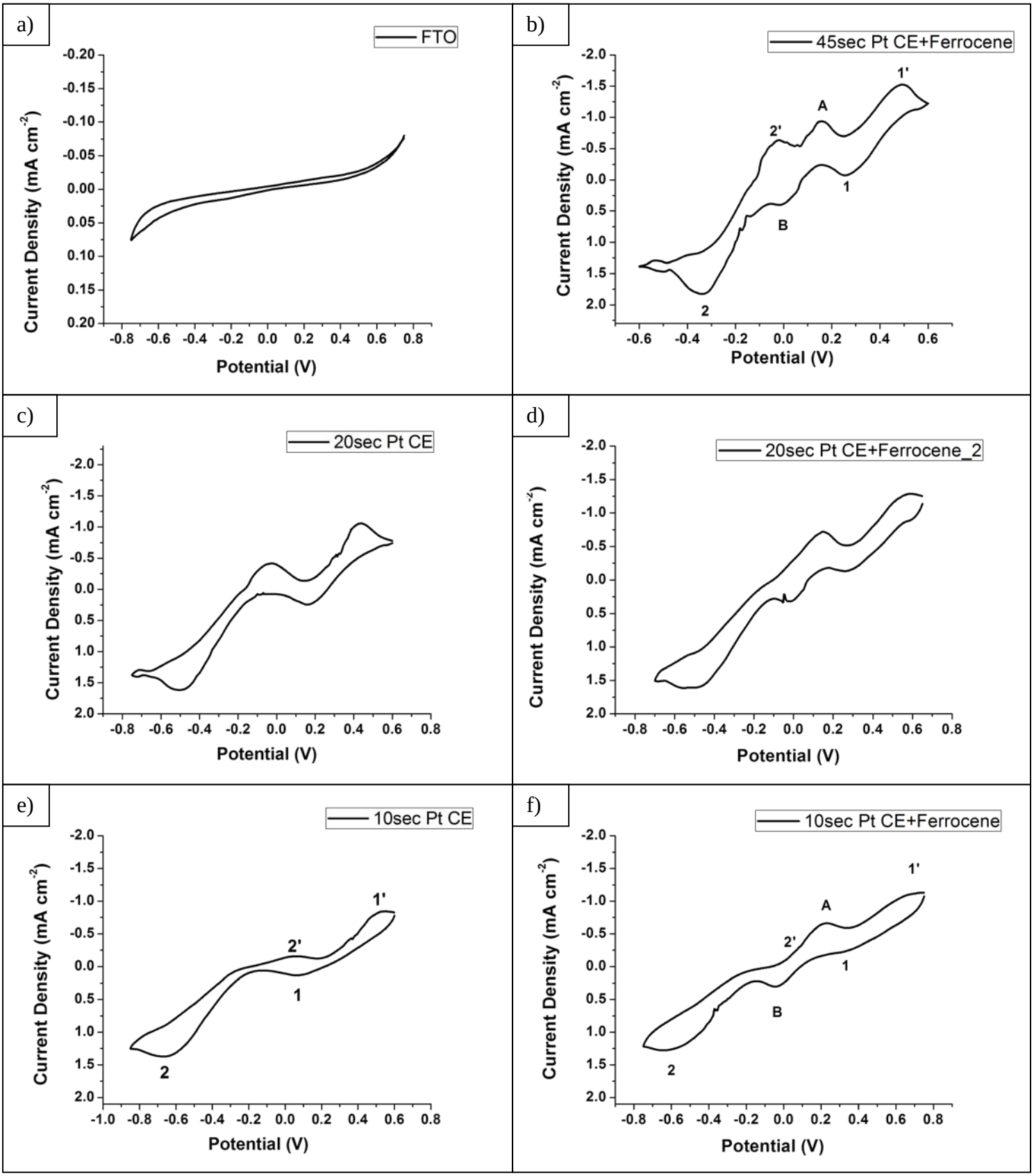


Figure 21: CV curves in the electrolyte containing the triiodide/iodide specie – a)FTO – no discernable iodide/triiodide redox peaks signaling the extremely low catalytic activity of FTO by itself; b) 45 s Pt – FTO working electrode + Ferrocene; c) 20 s Pt – FTO

The working electrodes studied were blank FTO, ~50-nm-thick sputtered Pt film, 10 s Pt sputtered on FTO, 20 s Pt sputtered on FTO, and 45 s Pt sputtered on FTO. Figure 23 plots the standardized peak potentials keeping the ferrocene redox potential set at 0.4 V vs. a saturated calomel electrode (SCE) [117]. As can be seen from the redox peak potentials plotted in Figure 23, the ferrocene corrected peak potential (peak potential vs. SCE) for I_3^- reduction (2) is the most cathodically shifted for the 45 s Pt NP decorated FTO working electrode (–0.026 V) followed by the sputtered Pt thin film (-0.06 V), 20 s Pt NP decorated FTO (–0.194) and 10 s Pt NP decorated FTO (-0.414) working electrodes; hinting at the superior triiodide reduction catalytic activity of 45 s Pt deposition. Also, from Figure 23, the peak difference between the triiodide/iodide redox peaks ($\Delta E_p 2$ value) is minimum for the 45 s sputtered Pt on FTO working electrode (0.317 V) followed in similar order as before by the sputtered Pt thin film (0.395 V), 20 s Pt NP decorated FTO (0.480 V) and 10 s Pt NP decorated FTO working electrodes (0.732 V) confirming lower overpotential required to reduce triiodide which suggests faster electron transfer kinetics and thus enhanced catalytic activity at the 45 s Pt NP electrode compared to 50 nm-thick Pt film and Pt nanoclusters (10 and 20 s Pt) . Another indication of high catalytic activity of the 45 s Pt sputtered FTO working electrode is the higher current density at the triiodide reduction peak (peak 2) compared to the Pt thin film. All these factors depicting enhancement in catalytic activity are seen for the 45 s Pt sputtered FTO electrode even though the Pt surface area available for catalysis is only 45% of a continuous Pt thin film, as mentioned above in section 2.3.3. It is believed that the representative peak positions in the CV curves are inherently related to the Pt size/crystallinity characteristics and have negligible dependence on the Pt surface coverage. However, DSSC performance characteristics (fill factors and efficiencies - section 2.3.3), are determined by a combination of the inherent Pt catalytic activity, which is a function of Pt NP size and crystallinity, and Pt surface

coverage. Thus, based on the redox peak positions and $\Delta E_p 2$ values displayed in Figure 23, the triiodide reduction catalytic properties are poor in case of the 20 s and 10 s Pt sputtered FTO electrodes and strong in case of the 45 s Pt NPs.

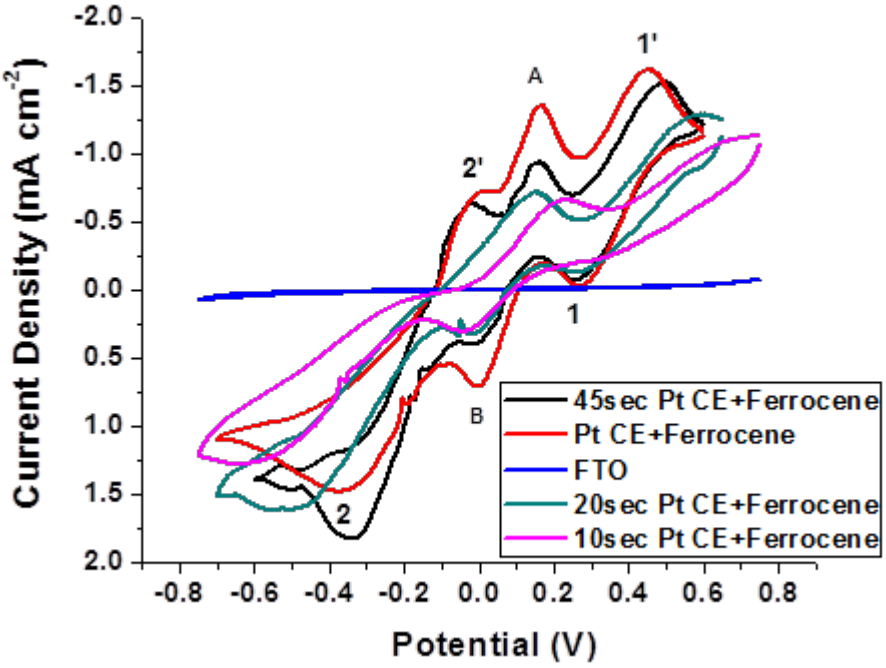


Figure 22: CV curves measured in electrolyte containing the triiodide/iodide couple comparing a 45 s Pt–FTO working electrode, a sputtered Pt thin film, and naked FTO. Potentials are referenced to a Pt pseudo-reference electrode.

The enhancement of catalytic activities in case of the 45 s Pt sputtered FTO electrode over the 20 s and 10 s sputtered samples can be attributed to the high crystallinity of the 45 s Pt NP surface, as discussed in section 2.3.1, and faster electron transfer kinetics as displayed in a schematic in Figure 24. This faster charge transfer can be attributed to faster electron mobility within crystalline structures compared to non-crystalline structures obtained at lower sputter times. The Pt nanoclusters formed at low sputter times (avg. size < 1nm) possess charge trapping characteristics and thus lead to far less efficient electron transfers and thus increase the overpotential required to

undergo certain reactions. [7, 8] Figure 24 compares the charge transfer process between non crystalline clusters, crystalline Pt NPs and Pt thin films. Charge trapping at these Pt NPs (sputtering time $\leq$ 20 s, avg. size < 1 nm) has been proposed in previous papers [7, 8]. In these cases, the lower electron transfer efficiency of these ultra-small Pt NPs play a beneficial role as they reduce recombination in TiO_2 based photocatalytic systems. The higher catalytic activity for 45 s Pt NPs compared to thin films as depicted by CV analysis could arise as a result of two phenomena. Firstly, charge transfer from FTO to the electrolyte is much more efficient in the case of ultrafine crystalline Pt NPs when compared to charge trapping sub-nanometre Pt clusters or relatively thick sputtered polycrystalline Pt thin film that has internal defects due to grain boundaries that leads to the generation of electron loss pathways, as depicted in Figure 24. Secondly, the higher catalytic activity of crystalline Pt NPs compared to the thin film could be due to the faster desorption of I^- from the Pt NPs surface since desorption of I^- from Pt has been described as the rate determining step of the triiodide reduction reaction at low iodide concentrations [128]. Pt is known to readily adsorb iodide anion [143-145] which is reduced from the triiodide ion adsorbed on the Pt surface through a two electron transfer process and the slow iodide ion desorption from the Pt surface hampers fresh triiodide reduction. Iodide adsorption on crystalline Pt surfaces is known to create well defined stable adlayers [146-148] which hinders iodide desorption and henceforth slows down the triiodide reduction reaction. The absence of well-defined facets in Pt NPs used in this study might be favourable for faster iodide desorption due to formation of defective adlayers. In fact, halide poisoning is a prevalent issue in the PEM fuel cell field where iodide ions have been shown to adsorb strongly on crystalline facets of Pt NPs (adsorption on <100> greater than <111> facet) and on steps and kinks formed the intersection of these facets [149]. A spherical stable surface should have minimal surface energy and be relatively free of the aforementioned steps and kinks.

Therefore, in the overall reaction at the counter electrode, electron is received through the FTO surface and, owing to the crystalline Pt NPs, undergoes fast charge transfer to the NP surface where it reduced triiodide into iodide and the faster desorption of iodide from the NP surface enable another triiodide ion to undergo reduction. This phenomenon might be another reason for higher catalytic activity of the spherical 45 s Pt NPs when compared to a polycrystalline thin film.

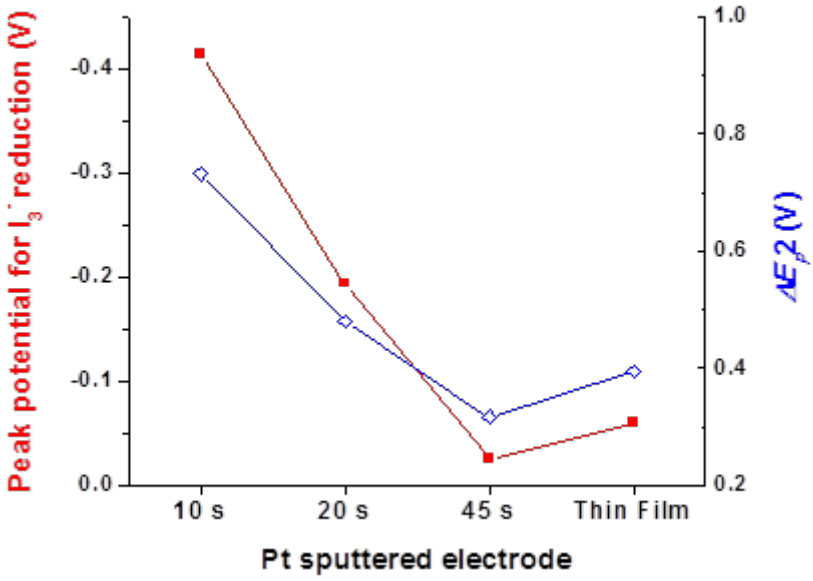


Figure 23: Peak potential for triiodide reduction and the ΔEP value for the triiodide/iodide redox reaction plotted for different studied electrodes

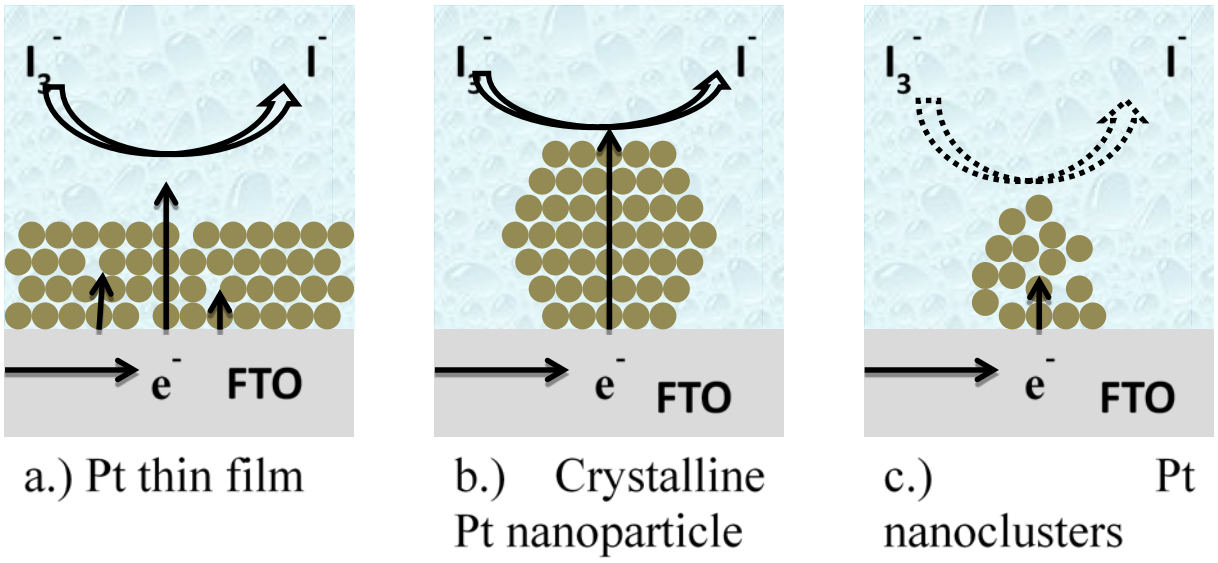


Figure 24: Electron transfer process for various Pt sputtered FTO electrodes. Mismatches in terms of atom alignment in (a.) are meant to represent defects due to grain boundaries within sputtered polycrystalline thin films. The crystalline Pt NP in (b.)

CHAPTER 4: HYDROGEN SPILLOVER AT SUB-2 NM PT NANOPARTICLES BY ELECTROCHEMICAL HYDROGEN LOADING

This chapter discusses the indirect observation of hydrogen spillover observed during electrochemical loading of sub-2nm Pt NPs. In this work, a correlation between NP size, crystallinity, support characteristics, and hydrogen spillover was also studied.

4.1 BACKGROUND

Hydrogen spillover is a phenomenon observed typically at transition metal NP-support interfaces. Hydrogen spillover is a well-recognized phenomenon defined as the transport of adsorbed dissociated hydrogen from one surface to another by surface diffusion. The first surface is typically a metal capable of dissociating H_2 and the second surface is typically the support on which the metal is doped[150]. The uptake of hydrogen by platinized carbon was first interpreted successfully in terms of surface diffusion by Boudart et al. back in the 1960s[151, 152]. The majority of experiments involving spillover utilize either platinum or palladium as these metals are known to dissociate H_2 and promote spillover[153]. So far, the best experimental evidence of the spillover phenomenon was shown by Tsao et al., who used inelastic neutron scattering (INS) to monitor the change of molecular hydrogen in Pt-doped activated carbon (Pt/AC) samples directly and provide conclusive evidence that hydrogen atoms can diffuse to the carbon surface at room temperature[154]. Recently, Lykhach et al.[155] demonstrated by way of resonant photoemission spectroscopy that hydrogen spillover on Pt/CeO2/Cu(111) involves a net transfer of neutral hydrogen, either by atomic hydrogen transfer, as proposed by Hattori and Shishido [76], or by a multistep process. Apart from the aforementioned reports, experimental evidence of

primary spillover is almost nonexistent, with a plethora of reports tracking reactions involving the already spilled over hydrogen atom. For example, the evolution of a peak in the double layer region (where the current density observed during potentiodynamic scanning is dominated by double layer capacitance of the sample). of Pt during cyclic voltammetry has suggested that spillover occurs at nanoscale Pt electrodes encapsulated in glass sheathing[74]. The observed irreversible peak was attributed to hydrogen desorption at the Pt/glass interface with the hydrogen atom spilling over at the interface and hydrogen desorption from the interface occurring at a higher potential. The spillover of atomic hydrogen formed on a Pt surface to the supporting SiO_2 surface and its subsequent desorption from the SiO_2 surface in the form of H_2 was also reported recently during photoelectric water splitting experiments using a metal-insulator-semiconductor system[156]. In yet another example, reduction of metal NP (Pt and Ni)-decorated graphene oxide (GO) flakes through spilled over hydrogen employed spilled over hydrogen from an application standpoint towards facile synthesis of reduced graphene oxide (RGO) [64, 69]. The most comprehensive work on the mechanism of hydrogen spillover from Pt metal NPs to the support was provided by Psofogiannakis and Froudakis, who reported that the dissociation of hydrogen molecules on the Pt cluster is energy barrier-less while the migration of atomic hydrogen from the Pt clusters to the supporting oxide surface is favorable due to the low energy barrier[153]. The density functional theory (DFT) calculation was used to demonstrate that the process of atomic hydrogen diffusion to GO could happen in a manner similar to the hydrogen spillover mechanism on metal oxide surfaces[153]. Li and Lueking further claimed the presence of oxide groups or water molecules at the surface of supporting structure to be advantageous towards capturing the spilled over hydrogen[58].

As mentioned before, the role of the Pt NPs in the spillover phenomenon is to dissociate hydrogen molecules and inject dissociated H atoms to the supporting structure. It is well known that Pt dissociates H_2 molecule readily and the resultant H atoms bind strongly to the Pt surface. Also, it has been shown previously that the H atom binding energy on the Pt NP surface is dependent on H coverage. Theoretical calculations on small Pt clusters indicate that the binding energy of the H atoms at full saturation is 2.44 eV, whereas the same energy is 3.2 eV at zero H coverage[59]. Given such high energy barriers (even in the case of full saturation) for the bound H atom to overcome for spillover from the Pt NP surface, it is hard to conceptualize the H atom spilling over to the supporting structure. Indeed, a large activation energy is required for the H atom to migrate from the strongly bound state on the Pt surface to a less strongly bound immobile state, such as by forming a C–H bond on graphite with a binding energy ~0.8 eV[60]. Based on theoretical simulations of H_2 molecules approaching Pt/Ce2O, Pt/γ-alumina systems, a pathway for the spillover phenomenon has been proposed by Miyamoto et al[61, 62]. After a hydrogen molecule dissociates on kink sites of the Pt NP, one of the two dissociated H atoms was immediately ejected from the Pt to the gas-phase, while the other H atom remained bound on the Pt surface. This ejected H atom was reported to gain kinetic energy due to the dissociation of the H–H bond. Currently, parameters that can affect this process of gas-phase H atom generation are not very well understood. It is likely that its rate is determined by the temperature, the H_2 pressure and the nature, shape and size of the NPs. Detailed understanding of desorption of H atom from the Pt NP in such cases and it effect on the overall spillover schematics is still lacking and this study aims to shed light on it by controlling the physical characteristics of the supported Pt NPs.

So far, the general consensus regarding the NP size dependence of spillover efficiency is that a greater degree of spillover (as deduced by secondary reactions) occurs as the NP/cluster size

reduces. Pt catalyst size has been identified as a crucial factor determining whether significant storage enhancement can be achieved in hydrogen spillover at ambient temperature[63]. Pt NPs of increasing size (2.2, 3.9, and 9.1 nm) were produced by chemical vapor deposition (CVD) onto a metal oxide framework. The hydrogen storage properties of these systems were investigated by high pressure isotherm analysis and showed that smaller sizes were needed for efficient spillover. To our knowledge, there is no reported study on the effect of sub-2 nm Pt NPs in the field of hydrogen spillover. Studying the properties of Pt NPs of sizes in this critical size domain where the NP crystal structure evolves should help further our understanding of the fundamental kinetics of hydrogen spillover.

4.2 METHODS

4.2.1 Few layer graphene (FLG) deposition

FLG was deposited on fluorine doped tin oxide (FTO) substrates by rubbing highly ordered pyrolytic graphite (HOPG–SPI2) samples on the intrinsically rough FTO surface and subsequent removal of debris using Scotch tape. More information on FLG transfer process and its subsequent Raman analysis is provided in section 3.3.1. It is worth noting that the FLG samples showed negligible effects of plasma damage after deposition of Pt NPs. Detailed explanation of the lack of plasma damage on tilted-target sputtering (TTS) samples is provided elsewhere[50]. Henceforth, FLG-covered FTO substrates will be referred to as FLG.

4.2.2 Pt NP fabrication and characterization

An AJA International ATC 2000 magnetron sputtering system was used to deposit Pt NPs on FTO and FLG supports. Detailed information of Pt NP sputtering using the TTS method are provided elsewhere [4-8, 16, 50-52]. Exhaustive TEM analysis of Pt NPs was performed using a 5 nm Al_2O_3-coated carbon grid. No significant changes in size distribution or areal density were seen for equivalent Pt depositions on Al_2O_3, FTO, or FLG surfaces[50]. Details of Pt NP characterization are provided in[16].

4.2.3 Cyclic voltammetry (CV) experiments

For the CV setup, the working electrodes were Pt-sputtered FTO and FLG substrates, the counter electrode was a Pt wire gauze electrode, and the reference electrode was a reversible hydrogen electrode (RHE). The electrolyte used in the CV runs was 0.5 M H_2SO_4. The exposed area of the working electrode was controlled using molded PDMS wells. All electrochemical measurements were done at 500 mV/s scan rate. For H_2 exposure/H loading and XPS analysis, the Pt NP decorated FLG samples were cycled 250 times at 250mV/s scan rate in the underpotentially deposited hydrogen regime (0.05 – 0.4 V vs. RHE).

4.2.4 XPS analysis

X-ray photoelectron spectroscopy (XPS) was conducted using a Kratos Axis 165 spectrometer and vacuum level within the chamber remained near 1.0×10^{-8} Torr during acquisition. A 150 W Al X-ray source was used for the XPS measurements and any effects of sample charging were accounted for by fixing the oxygen peak.

4.3 RESULTS AND DISCUSSION

4.3.1 Evidence of hydrogen spillover from sub-2 nm Pt NPs to FTO

Direct evidence of hydrogen spillover from Pt NPs onto the supporting surface (Figure 25) is difficult to obtain and most literature focuses on secondary phenomena (e.g. hydrogen storage on the supporting surface) to ascertain the efficiency of hydrogen spillover. To the best of our knowledge, all Pt NPs employed in literature for spillover purposes have been above 1.5 nm in diameter[65]. Pt NPs greater than 1 nm in size are usually crystalline in nature[50] and are likely to have stronger chemisorption of H atoms after dissociation of H_2 molecule on the Pt surface. For such crystalline Pt NPs, the ejected H atom from the NP surface after spillover is less likely to have enough energy to form stable C-H bond on the carbon surface near heterogeneous interfaces. This is especially the case in this present study where spillover is reported near interfaces consisting of aqueous electrolyte solutions, which could lead to strong interactions with the spilled over H atom. Bringing down the Pt NP size smaller than 1 nm (non-crystalline clusters) could lead to increased H atom energy and stable C-H bonds heterogeneous interfaces. While analyzing the presence of the spillover indicative peak observed during CV scanning in the double layer region, awareness of the anion adsorption peak around 0.65 V due to SO_4^{2-} anion adsorption is especially important as it competes with the support-mediated hydrogen desorption peak[49, 66, 73, 74, 157]. Figure 26 shows the CV done on a plain FTO substrate. It is important to note that there is no intermediate hydrogen adsorption/desorption regime as is evident in case of the Pt thin film, but a direct hydrogen evolution stage. In Figure 27, a distinctive peak in the double layer region can be seen for the 0.9 nm Pt NPs on FTO during linear voltammetry (LV). The peak positions,

characteristics, and inability of FTO alone to successfully dissociate hydrogen molecules into atomic hydrogen are similar to the effects of SiO_2 reported by Zhan et al[74].

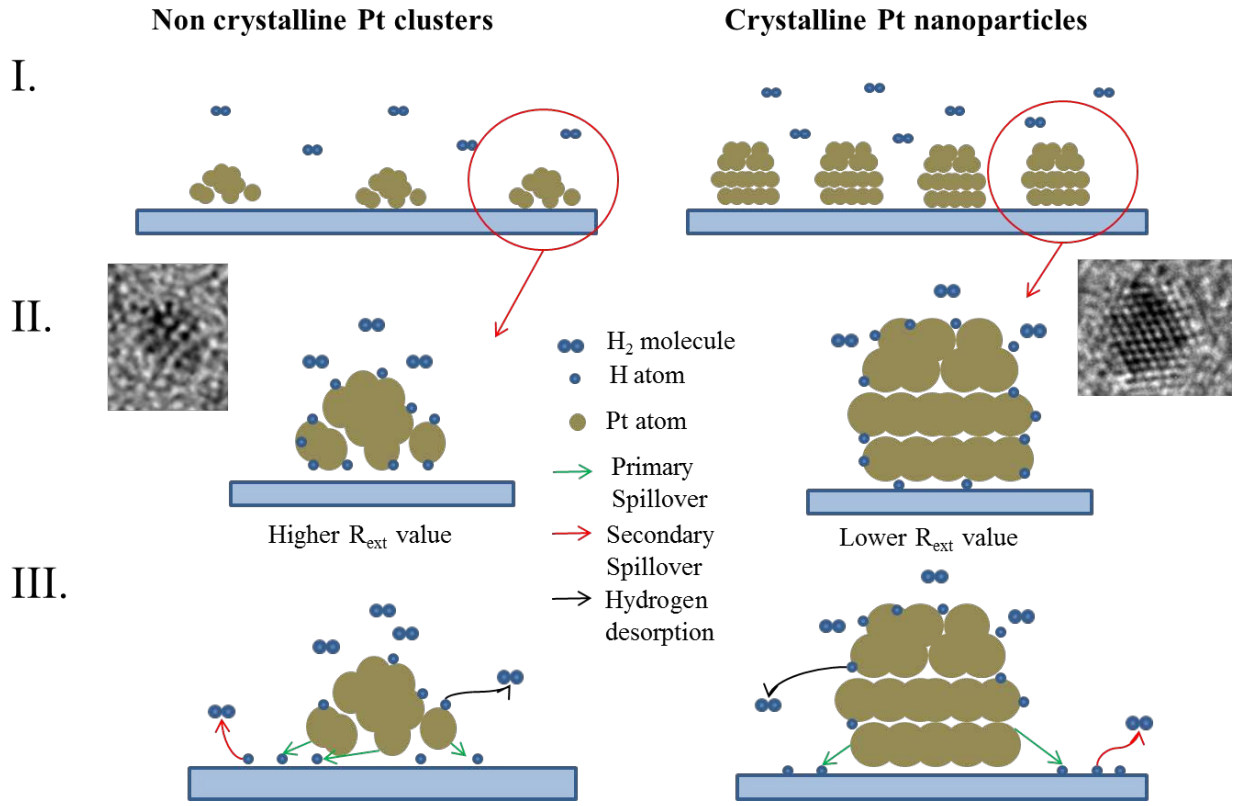


Figure 25: Schematic of hydrogen dissociation and spillover to the supporting surface. I – In-situ electrochemically generated hydrogen molecules in the acidic medium surround the Pt NP surface; II – Hydrogen molecules dissociate to form hydrogen atoms at Pt cluster/NP surface and are adsorbed at the Pt NP surface and Pt NP – support bridged bonds. R_{ext} represents the ratio of Pt NP – support bridged bonds to Pt-Pt bonds at the NP/cluster extremities (R_{ext} = Pt-substrate bonds / Pt-Pt bonds). Inset are the HRTEM images for a non-crystalline Pt cluster and s crystalline Pt NP; III – The dissociated H atoms migrate to the support surface from the Pt cluster/NP surface (primary spillover) and subsequently recombine at the support surface to release H2 molecule (secondary spillover), whose potentiometric signature is seen in the double layer region. The H atoms which remain adsorbed on the Pt NP/cluster surface desorb at potentials < 0.35 V vs. RHE and can lead to characteristic potentiometric hydrogen desorption signatures.

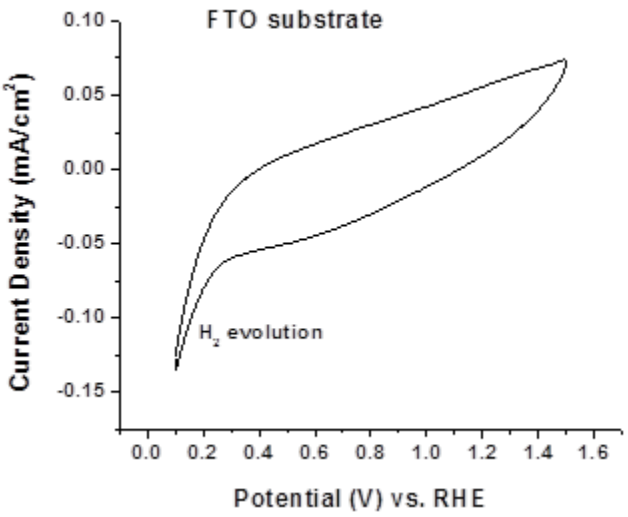


Figure 26: Cyclic voltammogram obtained in 0.5 M H_2SO_4 solution at FTO electrode. Scan rate – 100mV/s

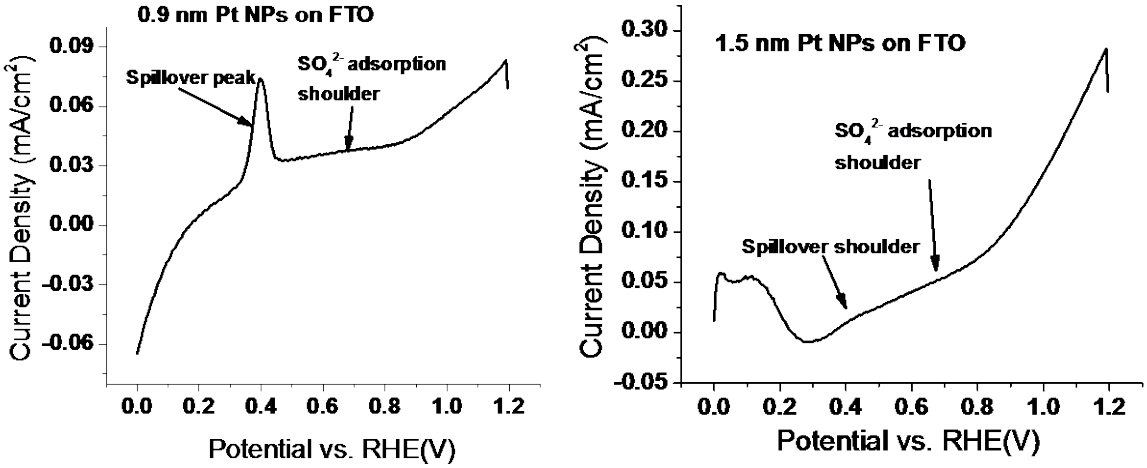


Figure 27: Linear voltammetry profiles for (a) 0.9 nm Pt NPs and (b) 1.5 nm Pt NPs on FTO substrates

Based on previous observations reported by Zhan et al.[74], this sharp peak in the double layer region can be attributed to hydrogen desorption from the FTO surface, which is observable only because hydrogen desorption occurs at a higher potential than desorption on the Pt surface.

However, it should be stated that possibility of charge transfer mechanism involving the spilled over H atom and its role in defining "spillover" peak might exist and due to lack of overwhelming evidence stating otherwise, cannot be ignored. Meanwhile, the 1.5 nm Pt NP-covered FTO sample shows an apparent shoulder in the spillover-mediated hydrogen desorption at the support potential regime (Figure 27 b), but the peak profile is not as sharp as in the case of 0.9 nm Pt NPs. This can be explained by the fact that the molecular hydrogen dissociation property of Pt seems to be inherent to the element rather than its crystalline phase. Therefore, one should expect a larger ratio of spilled over hydrogen to hydrogen desorbed at the Pt surface at lower potentials for the smaller, non-crystalline 0.9 nm Pt NP. The larger, crystalline 1.5 nm Pt particle should be more catalytically active towards hydrogen desorption at potentials near 0.3 V with respect to RHE. Thus a lower ratio of spilled over hydrogen to hydrogen desorbed at the Pt surface was expected. The appearance of a stronger spillover-indicative signal for the non-crystalline 0.9 nm Pt particles is supported by recent reports on atomic Pt catalysis. Guo et al. recently used ab-initio density functional calculations to study the hydrogen spillover mechanism, including the H atom chemisorption, diffusion, H_2 associative desorption on the surface of covalent organic frameworks (COFs), and H atom migration from metal catalysts to COFs[158]. They reported that the spillover process is more likely to occur at the Pt atom–support bridged bond than the Pt-Pt bonds at the surface of the Pt particle. Owing to its smaller size and 2-D growth dynamics, the sub-nm Pt clusters have a higher number of Pt atom-support surface bonds compared to Pt-Pt bonds on the particle surface, increasing the ratio of hydrogen spillover to hydrogen desorption with respect to 1.5 nm particles[16]. An inverse relation between Pt NP size and spillover efficiency has also been reported by Wang et al[63].

There is a consistent peak (or shoulder) around 0.65 V with respect to RHE, which represents SO_4^{2-} anion adsorption on Pt surfaces. The spillover peak and the anion adsorption peak in the double layer region were distinguishable for a majority of the characterized samples. Recall that the origin of the "spillover peak" is a secondary spillover phenomenon where the spilled over hydrogen atom adsorbs on the FTO electrode surface (oxide groups are considered ideal for hydrogen adsorption) and are subsequently desorbed at a potential typically in the double layer region of a characteristic Pt linear voltammetry (LV) plot (~0.4-0.5 V with respect to RHE). It is interesting to note that whereas a small "spillover" bump was evident for almost all 0.9 nm NP-covered FTO samples, around 33% of all samples showed significant peaks in the double layer region. It is also worth noting that the sample showing the most distinguished spillover peak (Figure 27 A) showed the least Pt-like characteristics (i.e. clear, well-defined regions) in its CV plot. This could be due to the lack of crystalline particles for this particular sample compared to others and hints at the spillover effect being enhanced at facet-less, non-crystalline Pt clusters compared to crystalline particles.

4.3.2 Formation of C-H bonds on FLG surface analyzed by XPS

As mentioned before, in case of Pt decorated FTO electrodes, the desorption of spilled over H atoms from the FTO surface leads to the rise of the signature peak in LV plots (secondary spillover) and helps identify the optimum Pt NP size required for spillover at an heterogeneous interface. Although this technique helps identify the Pt NP size required for efficient spillover, for practical hydrogen storage applications, the technique needs to be tested on a supporting structure that has a strong affinity towards H adsorption. Pt NP decorated FLG support was judged as the ideal system to study H storage due to spillover phenomenon as Pt NP show remarkable stability on graphene/FLG support[79]. No secondary spillover peak was observed in the case of Pt-FLG

system during potential cycling before as compared to FTO, because H atom affinity on sp^2 carbon substrates is fairly high and a hydrogen desorption peak would arise at lower potentials, possibly overlapped with Pt indicative peaks in the underpotentially deposited hydrogen (H_{UPD}) region. The different time sputtered Pt - FLG samples were cycled in the H_{UPD} region for 250 cycles each and XPS analysis was performed on the substrate surface before and after potentiometric cycling to study the possibility of change in sp^2 C-C to sp^3 C-H bonds on the FLG surface. XPS analysis confirming the utilization of spilled over H atoms from the Pt NP surface to supporting SWCNT structure to convert sp^2 C-C carbon bonds to sp^3 C-H carbon bonds has been reported before by Bhowmick et al[65]. Figure 28 (a) shows the XPS spectra of Pt-FLG sample before and after electrochemical H loading. The full width half-max (FWHM) of the XPS spectra are also reported within the plot. It can be see that, in the case of FLG sample decorated with 0.9 nm Pt NPs before and after electrochemical H loading, significant change in FWHM can be seen. The FWHM increases from 2.16 eV to 2.49 eV after H loading which corresponds to additional carbon bonding in the C-1s region[65]. Figure 28 (b) depicts the XPS data of the Pt-FLG film on fluorine doped tin oxide (FTO) electrodes before potentiometric cycling in the H_{UPD} region and a deconvolution of the peak into other carbon related peaks using a Gaussian-Lorenztian fit. For the analysis of the XPS spectra in terms of contributions from individual components representing different species, the experimental spectra were fitted by a combination of components by minimizing the total squared-error of the fit. Individual components were represented by a convolution of Lorenztian function, representing the life-time broadening, and a Gaussian function to account for the instrumental resolution [159]. The Gaussian broadening was kept the same for different components. A Shirley background function was also considered to account for the inelastic background in the XPS spectra. In the C-1s region, the C-C peak position was fixed at 284.7 ($\pm$

0.1 eV) and the FWHM was fitted within a (± 0.05 eV range). XPS analysis of graphene and reduced graphene oxide samples has been performed before in published literature [68, 70, 71, 160-166]. Surface contamination in ambient conditions on graphene substrates due to various carbon-oxide groups has been observed in these cases too. Although sample surface sputtering in order to remove surface impurities is a common norm in most XPS data acquisition, this was not performed as it could create irreparable plasma damage on the surface. In Figure 28 (b), the tail broadening in higher binding energy region of the c-1s region in the XPS spectra is indicative of C-O contamination and peaks indicative of these contaminants can be fitted around 286.1 (C-OH), 287.5 (C=O) and 288.9 eV (O=C-OH) and the resultant fit yields an r^2 values around 0.998. The C-C peak was fixed at 284.8 eV and the FWHM was fixed at 1.75 eV during the deconvolution procedure. The FWHM of this C-C peak is slightly broader than that reported in most literature, but this could be explained by the high defect concentration within the FLG film and influence of Pt NPs deposited on the FLG support. C-C peak broadening due to incorporation of metal NPs has been observed before in [167]. This has been attributed to the influence of metal-carbon interaction which disrupts the C-C binding energy and broadens the lineshape of the C-C peak. Figure 28 (c) displays the XPS spectra of 0.9 nm Pt- FLG with its deconvoluted peaks. Keeping the rest of the components (C-C, C-OH, C=O and O=C-OH) at similar peak positions and by mimicking the lineshape of the C-C peak to that in case of the aforementioned 0.9 nm Pt NP decorated sample before electrochemical H loading (Figure 28 (b)), the best fitting was obtained by adding an additional peak at 285.3 eV. All the XPS peak fitting parameters, i.e., peak position, FWHM and percentage composition to overall fit are listed in Table 7. It must be noted that there is a slight C-C peak broadening upon incorporation of bigger Pt NPs (45s Pt and 120s Pt). This peak can be attributed to the binding energy of the C-H bond. The peak position of the C-H bond has been

reported to be ~0.65 eV greater than the C-C bond [162, 168]. Only in the 0.9 nm Pt decorated FLG sample, the need to incorporate an additional peak at 285.3 eV was realized. This can be interpreted as successful partial hydrogenation of the C-C on the FLG surface. The intensity ratio of sp^3 and sp^2 hybridized carbon components is ~0.66 which corresponds to H coverage of ~ 40% (0.66/1.66). This is very close to the saturation H coverage percentage (50%) reported earlier [60, 77, 165]. While studying 1.5 nm Pt NP decorated FLG and Pt nano-island decorated (higher Pt sputtering time – 120s) samples, no significant FWHM increase in the C-1s spectra after electrochemical H loading was observed. During deconvolution, incorporation of an additional peak at 285.3 eV was not required to fit the XPS data (**Figure 29**). Thus, in these cases, the lack of significant C-H bonding suggests a lower degree of H spillover compared to the case of 0.9 nm Pt NP decorated FLG. Thus, based on previously performed electrochemical characterization and XPS analysis, it can be concluded that among the studied samples, only for 0.9 nm Pt NPs, there is a high enough degree of spillover (as characterized by the relative intensity of the secondary spillover indicative peak) and the spilled over H atoms have enough energy to overcome the activation energy barrier to form C-H bonds.

Sample	C-C	C-H	C-OH	C=O	O=C-OH
20sPt_Before (FWHM = 2.16 eV)	284.8‖1.75‖59.7%	-	286‖1.97‖26.4%	287.4‖1.96‖5.5%	288.8‖1.97‖8.3%
20sPt_After (FWHM = 2.49 eV)	284.6‖1.75‖34.7%	285.3‖1.86‖24.6%	286.1‖2.02‖24.9%	287.5‖1.82‖7.4%	289.0‖2.15‖8.4%
45sPt_After (FWHM = 2.12 eV)	284.7‖1.80‖63%	-	286‖2.17‖24.8%	287.5‖2.74‖5.3%	289.2‖2.36‖6.4%
120sPt_After (FWHM = 2.10 eV)	284.7‖1.81‖64.8%	-	285.9‖2.11‖24.7%	287.6‖2.22‖4.1%	289.2‖1.86‖6.5%

Table 7: XPS fitting parameters of various peaks used to for the XPS spectra

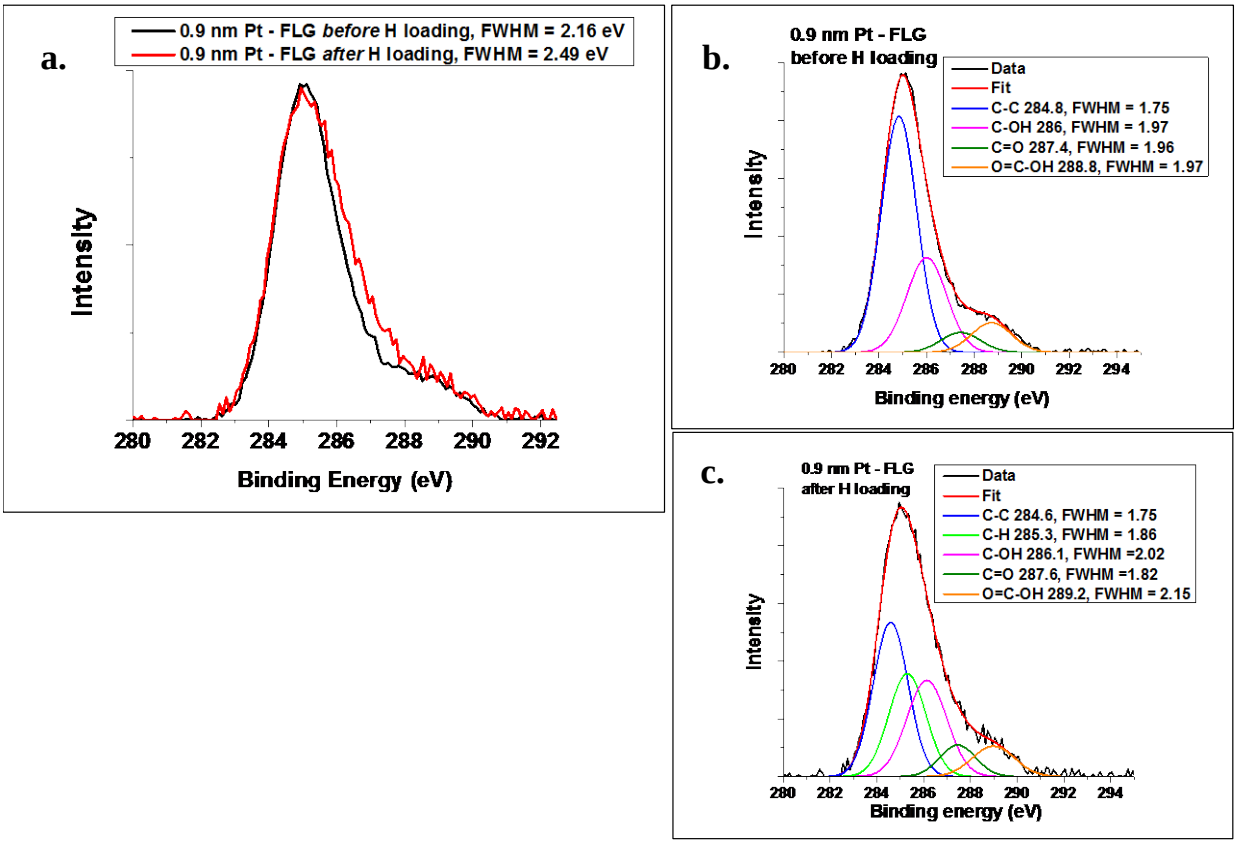


Figure 28: a) XPS spectra of 0. 9 nm Pt decorated FLG substrate before and after electrochemical H loading. The FWHM of the overall C-1s region is also reported in the curve; b) Deconvoluted XPS spectra of 0.9 nm Pt decorated FLG substrate before electrochemical H loading and c) after electrochemical H loading

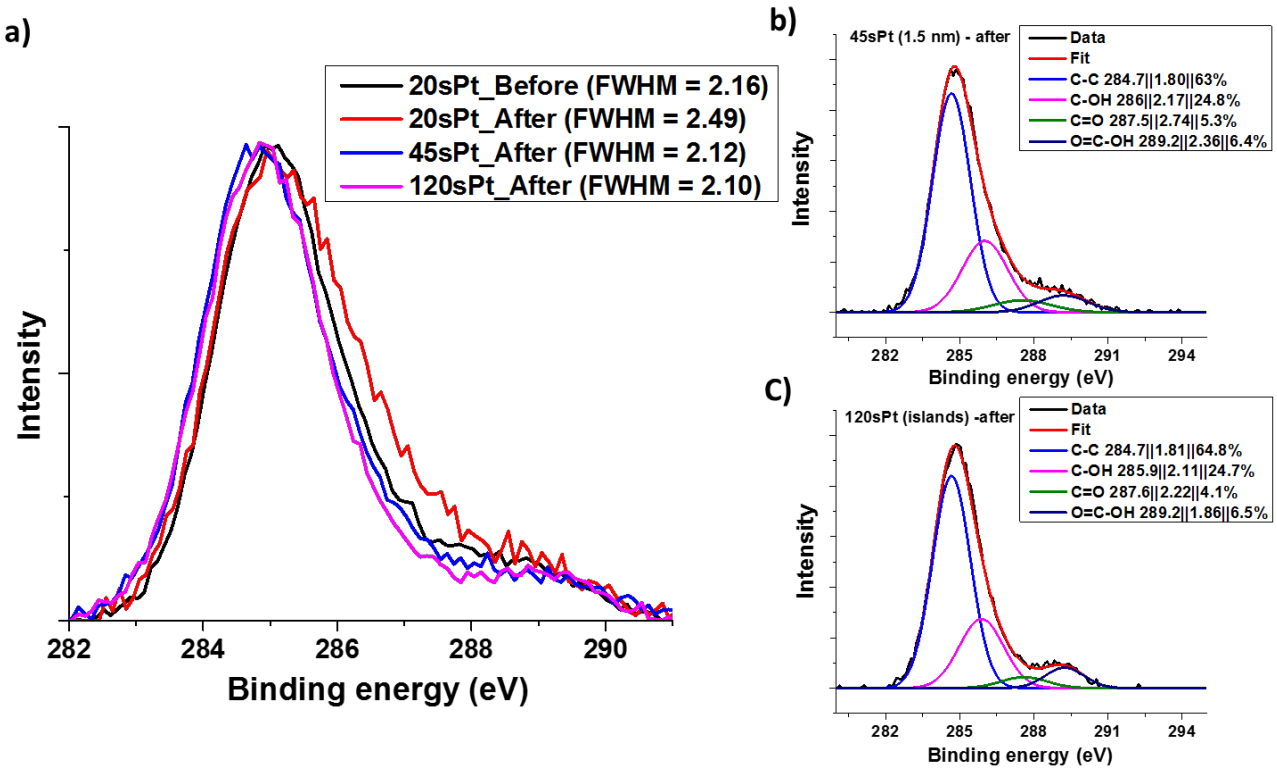


Figure 29: a) XPS spectra of various Pt NP (different sputtering times 20s – 0.9 nm, 45s – 1.5 nm, 120s - agglomerates) decorated FLG substrate before and after electrochemical H loading. The FWHM of the overall C-1s region is also reported in the curve; b) Deconvoluted XPS spectra of 45 s Pt (1.5 nm sized Pt NP) decorated FLG substrate after electrochemical H loading; c) Deconvoluted XPS spectra of 120 s Pt (Pt nano-islands) decorated FLG substrate after electrochemical H loading. The peak position || FWHM || percentage area contribution of the peak towards the overall fit, are reported in b) and c)

Based on this study, it can be surmised that smaller, non-crystalline sub-nm Pt clusters can be efficient centers for hydrogen molecule dissociation and H atom spillover. In this particular study, Pt NPs bigger than 1.5 nm did not show substantial spillover activity, either via monitoring the electrochemical secondary spillover peak at FTO supports or in the C-H bond formation case through direct spillover for the FLG support. It is worth noting that for smaller Pt NPs, the hydrogen molecule dissociation would occur at the non-crystalline, high surface energy Pt NP surface. Based on a proposed spillover pathway reported by Ahmed et al [61, 62], After a hydrogen

molecule dissociates on kink sites of a Pt NP, one of the two dissociated H atoms is immediately ejected from the Pt to the gas-phase, while the other H atom remains bound on the Pt surface. This ejected H atom was reported to gain kinetic energy due to the dissociation of the H–H bond. Based on this spillover pathway, the strong attraction of one dissociated H atom on the Pt surface could aid spillover of the other H atom on the support surface with enough energy to make a stable C-H bond. It should be noted that parameters that can affect this process of gas-phase H atom generation are still not very well understood. Based on theoretical study, Ahmed et al. claim that it is likely that its rate is determined by the temperature, the H_2 pressure and the nature, shape and size of the NPs[61, 62]. This observation is slightly contrary to previously reported results where spillover was observed at Pt NPs larger than 2 nm [63, 65]. It is important to note that in these studies, the degree of spillover was explored by introducing high pressure H_2 gas at the Pt NP/support interface, contrary to electrochemical H loading in aqueous solutions used in this study. It has been acknowledged that minimizing the H atom adsorption energy at the Pt NP surface would increase the degree of spillover[153]. In aqueous surroundings, the H atoms ejected at kink sites of the Pt NPs have to overcome an additional energy barrier due to the polar molecules at the interface and this could lead to suppression of spillover indicative characteristics for Pt NPs larger than 2 nm. Also, it is important to note that the ejected H atoms are short lived [61, 62] and the interactions with H^+ donating species in the low pH aqueous electrolyte could severely diminish the number of H atoms approaching the supporting structure. In case of 0.9 nm non-crystalline Pt NPs, the larger surface energy (due to ultrafine size and non-crystalline structure) [169, 170] might lead to a larger relative proportion of dissociated H atoms being ejected from the Pt NP surface and combined with a shorter migration distance to the supporting structure (owing to smaller NP size), the probability of a larger number of spilled over H atoms with enough energy to form stable C-H

bonds near the supporting structure increases. Thus, the effects of spillover are more evident for 0.9 nm non crystalline Pt NPs in low pH aqueous solutions compared to NPs bigger than 2 nm in size.

An advantage of the technique used in this study to study H storage through spillover is the absence of a hydrogen gas source (which is required in most gas loading based hydrogen storage systems) as the hydrogen is generated electrochemically near the support-NP interface. Although potentiometric voltammetry can be used to analyze size-dependent spillover behavior through evidence of secondary spillover and C-H bond formation on the support, using this method might still underestimate the spillover efficiency. This is because polar water molecules and H^+ species present near the Pt NP interface could reduce the hydrogen atom migration probability and storage in the support (i.e. increase the activation barrier for hydrogen storage in the support). Plus, the harsh acidic environment is likely to functionalize the supporting structure and the probability of irreversible damage to the support in the long run might be a distinct possibility. For example, while monitoring graphene oxide (GO) reduction by passing molecular hydrogen through a solution of Pt NP-incorporated GO flakes as a result of hydrogen spillover from incorporated Pt NPs, post-treatment of the GO flakes with hydrogen gas outside the liquid phase was necessary to achieve the desired reduction [64]. This was explained by the fact that the presence of a liquid phase interferes with the spillover of atomic hydrogen from the Pt NPs to the GO surface, which in turn limits the radius of migration of atomic hydrogen[50]. Thus, to study the true effect of hydrogen spillover efficiency on hydrogen storage for the sub-2 nm Pt NPs, hydrogen gas loading experiments need to be performed in the future.

CHAPTER 5: SIZE/AREAL DENSITY DEPENDENT ASYMMETRIC CHARGING OF SUB-2NM PT NANOPARTICLE EMBEDDED MOS CAPACITORS WITH ULTRATHIN TUNNELING OXIDE

5.1 BACKGROUND

Over the last couple of decades, non-volatile memory-cell structures employing discrete traps as the charge storage media have attracted a lot of attention as the promising candidates to replace conventional dynamic random-access memory (DRAM) or Flash memories [105]. Discretization of the charge storage centers is considered a significant advantage over conventional floating gate (FG) nonvolatile memory architectures employing a dielectric embedded conductive FG, as the continual miniaturization of the tunneling oxide thickness increases the probability of all charge being lost if a leakage path appears in the tunneling oxide [171]. Discretization also helps overcome other limitations induced by the miniaturization of these conventional FG architectures such as increasing cell-to-cell interference, decreasing coupling ratio, decreasing tolerance for charge loss, etc. [172]. All these limitations surrounding conventional FG architectures results in serious reliability issues for memory applications. The discrete charge storage elements utilized in non-volatile memory-cell structures employing discrete traps as the charge storage media are usually traps in a dielectric embedded nitride film or nanocrystal memories which typically incorporate isolated semiconducting or metal nanocrystals fabricated by a myriad of techniques including chemical vapor deposition, low energy ion implantation, annealing of silicon rich oxide, self-assembly of solution processed micelles, thin film dewetting and aerosol based nanocrystal formation [105, 171, 172]. In the case of employing discrete traps in a dielectric embedded nitride film, it has been reported that the trap levels and trap sites in

silicon nitride are not very controllable since the charges can be trapped in between conduction and valence bands of silicon nitride [172]. Meanwhile NC memory devices using semiconducting or metallic NCs as a charge storage layer have an advantage over the silicon-oxide-nitride-oxide-silicon (SONOS) devices when it comes to controlling the trap density and distribution. This is because the density and location of the NCs can be controlled by adjusting the process parameters. Thus, among these two charge discretization techniques, utilizing dielectric embedded nanocrystals is considered a promising candidate for future nonvolatile, high density, and low-voltage memory applications, owing to their inherent immunity to the local oxide defect by discrete charge storage, which allows more aggressive scaling of the tunneling oxide thickness [173]. Among the efforts to further improve the performance of NC memories, metal NC was proposed above its semiconductor counterpart due to large density of states, three-dimensional electric field enhancement, and selectable work function [5-7, 105, 171, 172, 174, 175]. The application of metal NCs over the semiconducting NCs can be justified considering the desired goal for this device is to simultaneously achieve fast DRAM program/erase speeds and long flash memory retention times. For this purpose, creating an asymmetry in charge transport through the gate dielectric to maximize the program/erase charge retention ratio is desirable [176]. One approach for achieving this goal is to engineer the depth of the potential well at the storage nodes, thus creating a large energy band offset between the Si substrate and the storage nodes for programming and retention operations. This can be achieved if the storage nodes are made of metal NCs. As outlined succinctly by Chang et al., the major advantages of metal nanocrystals over semiconductor nanocrystals include: (i) higher density of states around the Fermi level (ii) controllable scalability of the nanocrystal size (iii) a wide range of available work functions and (iv) Smaller energy perturbations due to carrier confinement [171]. In addition, Lee et al. have demonstrated through

electrostatic modeling and analytical formulation that metal NCs significantly enhance the electric field between the nanocrystal and the sensing channel set up by the control gate bias, and hence such a system can achieve a much higher efficiency in low-voltage program/erase operations [176].

Considerable work has focused on the controlled synthesis of metallic NCs for use in non-volatile memory (NVM) devices. Although a wide range of metal nanocrystals have been utilized to realize functioning NVM, the lack of control over the embedded NP size, interparticle distance (areal density) makes it difficult to investigate the electron/hole charging characteristics as a function of embedded nanocrystal properties. To achieve the desired metal NP embedded layer for NVM applications, a CMOS compatible tilted target sputtering (TTS) technique has been previously developed [16]and is employed in this study to achieve NPs with controllable sizes, areal densities, and narrow size distributions. Using the TTS technique, the average size of the NPs can be effectively controlled by varying the deposition time with constant pressure, power, and gas flow rate at room temperature [16, 50]. This technique has been shown to produce uniformly distributed spherical Pt NPs with mean diameters between 0.5 and 2 nm, and for certain process parameters, high areal densities as large as 10^{13} cm^{-2}. Although embedding these Pt NPs in Al_2O_3 have resulted in NVM devices displaying large memory windows and good retention characteristics [5-7, 175], a systematic study analyzing the effect of the deposited Pt NP size, areal density and surface coverage on the quality/magnitude of introduced trap within the surrounding dielectric has not been reported yet. In this study, the influence of TTS sputtered Pt NP size, areal density and surface coverage on the charging/discharging characteristics of Pt NP embedded NVM MOS capacitors has been explored. Three different Pt Np size domains (0.7 nm, 0.9 nm and 1.6 nm) and two different areal density domains (~5 E 12 cm^{-2} and ~10 E 12 cm^{-2}) were explored

under the realms of this study utilizing variable frequency and scan rate dependent capacitance voltage (C-V) and conductance voltage (G-V) measurements. The observed experimental anomalous features within the C-V and G-V signatures has been correlated to the influence of different types and density of traps near the Pt NP/dielectric and dielectric/Silicon interfaces. While a similar device displaying enhanced memory effects due to controllable charging and discharging of the embedded Pt NPs [5] has been reported before, the NVM device structure discussed in this chapter employs a thinner tunneling oxide (Al_2O_3). This leads to a shorter distance between the Si surface and the traps near the incorporated Pt NP layer-dielectric layer, where they act more as “border traps” as compared to “Fixed oxide traps” [177]. This shorter distance in turn leads to a larger influence of the Pt NP induced traps in determining the C-V G-V features and thereby the types and density of these traps can be explored.

Fermi level pinning of the Pt NP layer effective work-function by Pt NP induced traps within the dielectric has been ascertained as one of the mechanisms afffecting the experimental C-V, G-V characterisitcs of the nanocrystal embedded NVM MOS capacitors explored in this study. Fermi-level pinning of the nanocrystal memories induced by high density of dielectric dangling bonds near the metal nanocrystal surface has been shown to complicate the expected charging/discharging characteristics [178]. This is especially the case with noble metal nanocrystal embedded NVM devices due to their negligible chemical interaction at the metal nanocrystal/dielectric interface [179, 180]. For a dielectric in contact with a metal, there are dangling bond states at the interface which are dispersed across the band gap of the dielectric. Depending on the magnitude of the density of these dangling bonds at the interface, the effective metal work unction can shift towards (i.e. its fermi level is “pinned”) the charge neutrality level (CNL) of the dielectric it is in contact with. The CNL of the dielectric can be thought of as a local

Fermi level of its interface states [180]. Application of high dielectric constant (high-k) dielectrics within metal nanocrystal embedded NVM devices can further enhance the degree of fermi-level pinning as high-κ dielectrics are generally known to have substantially higher density of interface states with metals than thermally grown SiO_2 [178]. For example, in this study, Al_2O_3 is used as the dielectric surrounding the Pt NPs and since its experimentally determined CNL (-5.2 eV [181]) is close to the silicon valence band edge, interface dipoles can form by transferring electrons from interface states into the Pt NPs at equilibrium pinning its effective work-function close to the Al_2O_3 CNL near Si valence band edge. More discussion on the Pt NP induced traps within the dielectric and resultant fermi level pinning of the Pt NP layer effective workfunction has been discussed with the obtained experimental data in section 5.3.2.

Since the electronic signatures of the Pt NP embedded NVM MOS capaitors would be discussed in the following results and discussion section (section 5.3), an introduction on metal nanocrystal embedded NVM device operation has also been included in section 5.1.1. In order to familiarize the readers with the advantages/disdvantages of high-k alumina incorporation within NVM devices and issues associated with atomic layer deposition (ALD) synthesized alumina on noble metal nanoclusters, an introductory discussion on high-k alumina incorporation has been included in section 5.1.2.

5.1.1 Metal NC embedded NVM device structure and operation

The metal NC embedded NVM devices explored in this study operate essentially based on similar principles of a floating gate embedded MOS device. It is important to note that the MOS capacitor is a two-terminal device and is essentially the the stack forming the gate in a metal-oxide semiconductor field effect transistor (MOSFET) and the changes in flat band voltage (due to

controlled programming/erasing operation) explored in MOS capacitor architectures can be translated to the shift in threshold voltage in a MOSFET [182].

In the NC embedded MOS capacitor structure, a discretized charge storage node floats within the oxide, separated from the substrate by a thin insulating layer known as the tunneling oxide and from the metal gate by a thicker blocking oxide. Bias applied to the gate metal contact sweeps the MOS structure through accumulation, depletion, and inversion by controlling the buildup of majority and minority carriers in the semiconductor near the oxide through the field effect. A schematic of the NC embedded MOS capacitor structure can be seen in Figure 30.

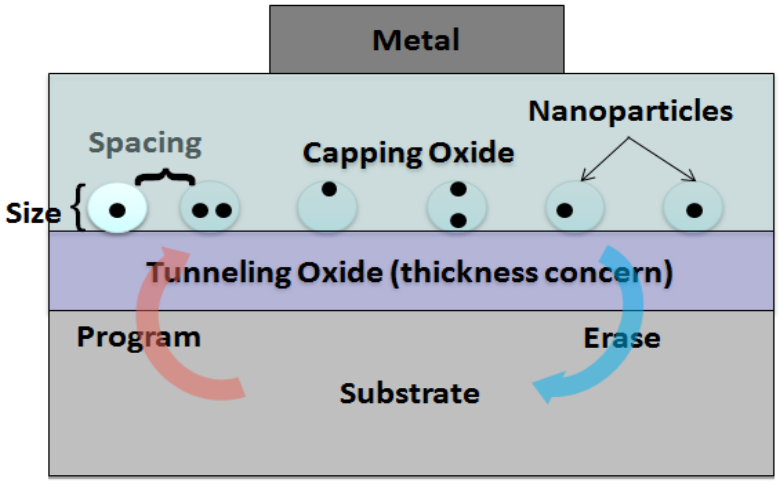


Figure 30: Schematic of the NC embedded MOS capacitor structure outlining the essential NC characteristics that can play a role in determining its charge storage properties (Source: [183])

For programing the NC embedded MOS capacitor, charge is injected from the inverted p-Si substrate into the discretized NC layer. The bias required to inject a charge into the Pt NP layer is a function of the total capacitance coupled to the NP. This is dependent on particle size and inter-particle distance between neighboring Pt NPs. Precise control of the charging energy of

discrete islands depends on optimization of these properties for a layer of NPs sandwiched between dielectric layers. This charge injection could occur through a channel hot-electron injection (CHE) mechanism for thicker tunneling oxides, F-N tunneling for thinner oxides (~10 nm) to direct tunneling for ultrathin oxides (< 3 nm) [174, 184, 185]. The fundamental mechanism of CHE is relatively straightforward in the sense that one just needs to provide enough energy to the channel electrons (making them hot) to overcome the oxide barrier. The hot electrons are injected from the substrate into the floating gate or the charge-trapping layer, due to the vertical electric field applied from the gate. F-N tunneling refers to quantum-mechanical tunneling through a thin potential barrier which is induced by an electric field. The oxide band bends under the application of an electric field, and presents a triangular shaped barrier to the charge-trapping layer. Larger the electric field, thinner the tunneling barrier. Compared to CHE, F-N tunneling is considered a more efficient charge injection mechanism[186]. Direct and F-N tunneling are similar in nature, with the basic difference being that direct tunneling occurs through the trapezoidal barrier and F-N tunneling occurs through the upper triangular barrier of the dielectric. Considering the ultrathin nature of the tunneling oxide utilized in this study (1.7 nm Al_2O_3 + 1.1 nm SiO_2), direct tunneling would be the charge injection (programming) mechanism in this case. In order to erase the injected charge from the embedded NC layer, a sufficiently large negative voltage is applied at the control gate. This applied gate bias is typically larger than the programming bias – given the asymmetry in the blocking and tunneling oxide thicknesses leading to disproportionate potential drops across the dielectrics. Upon application of this erasing bias voltage, the stored charges leave the discretized floating gate (NC layer) through a F-N tunneling mechanism. The representative band diagram for a relevant MOS structure (device structure utilized in this study - Ti – Gate metal →16.1 nm Al_2O_3 blocking oxide → embedded Pt NP later → 1.7 nm Al_2O_3 + 1.1 nm SiO_2

tunneling oxide → p-Si substrate), upon application of a gate bias within the programming, retention and erasing regimes are displayed in Figure 31, Figure 32 and Figure 33 respectively.

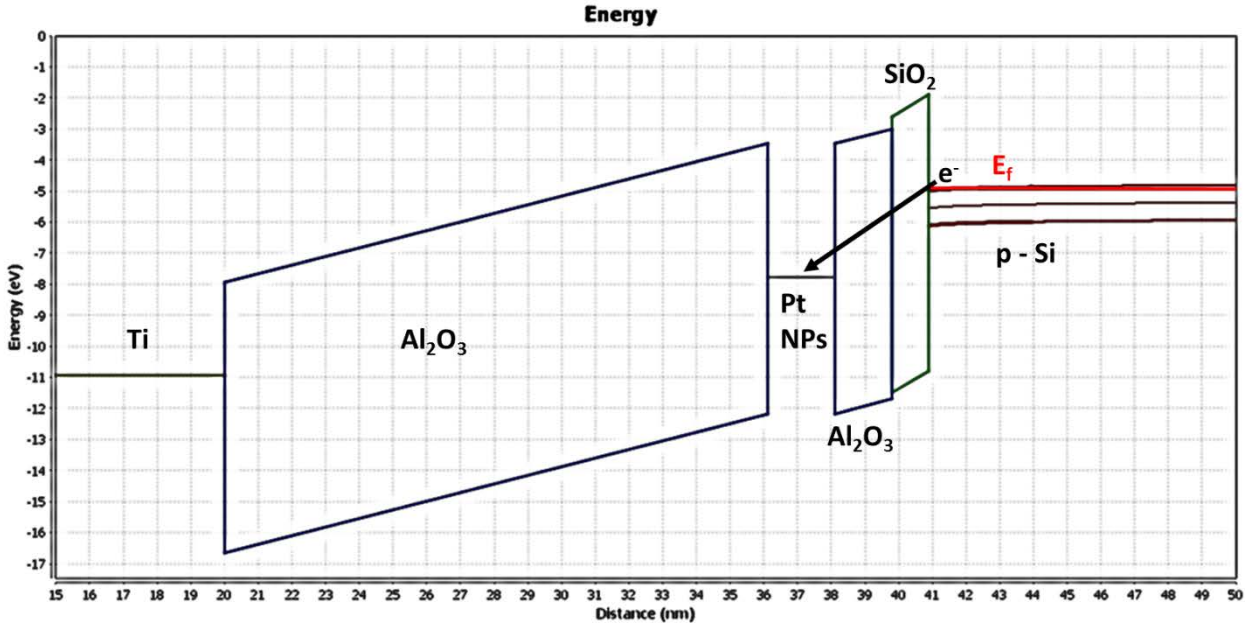


Figure 31: Simulated Band diagram of the MOS capacitor device utilized in this study at a "programming" gate bias of 6V. Simulated using "Stacked dual-oxide MOS energy band diagram visual representation program" [187].

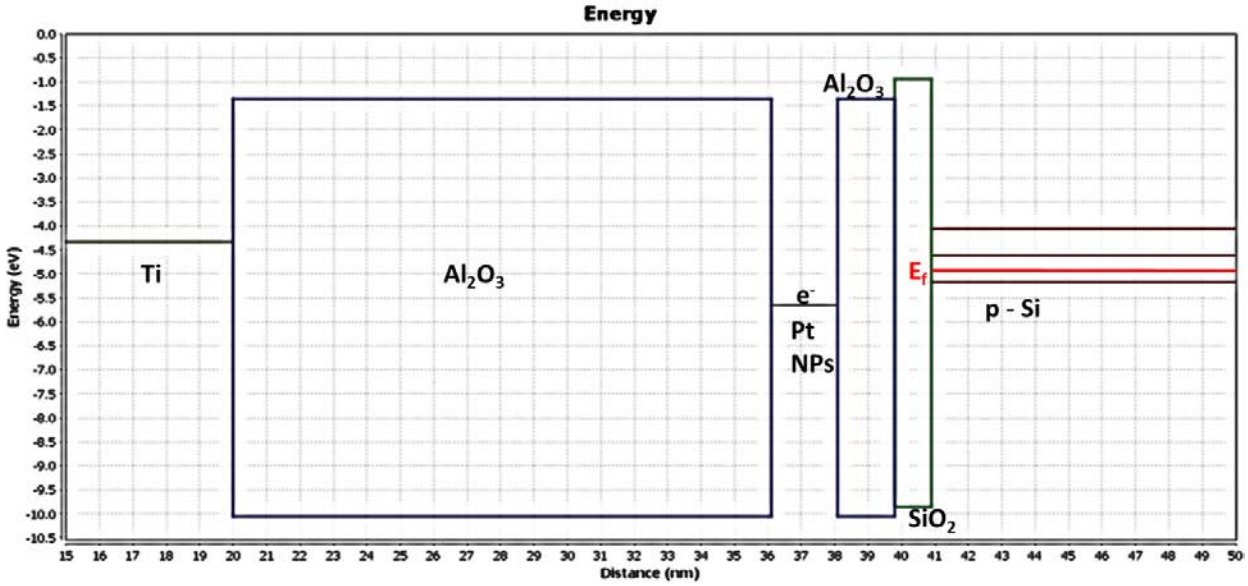


Figure 32: Simulated Band diagram of the MOS capacitor device utilized in this study at the theoretical flat band bias (-0.6 V). Simulated using "Stacked dual-oxide MOS energy band diagram visual representation program" [187].

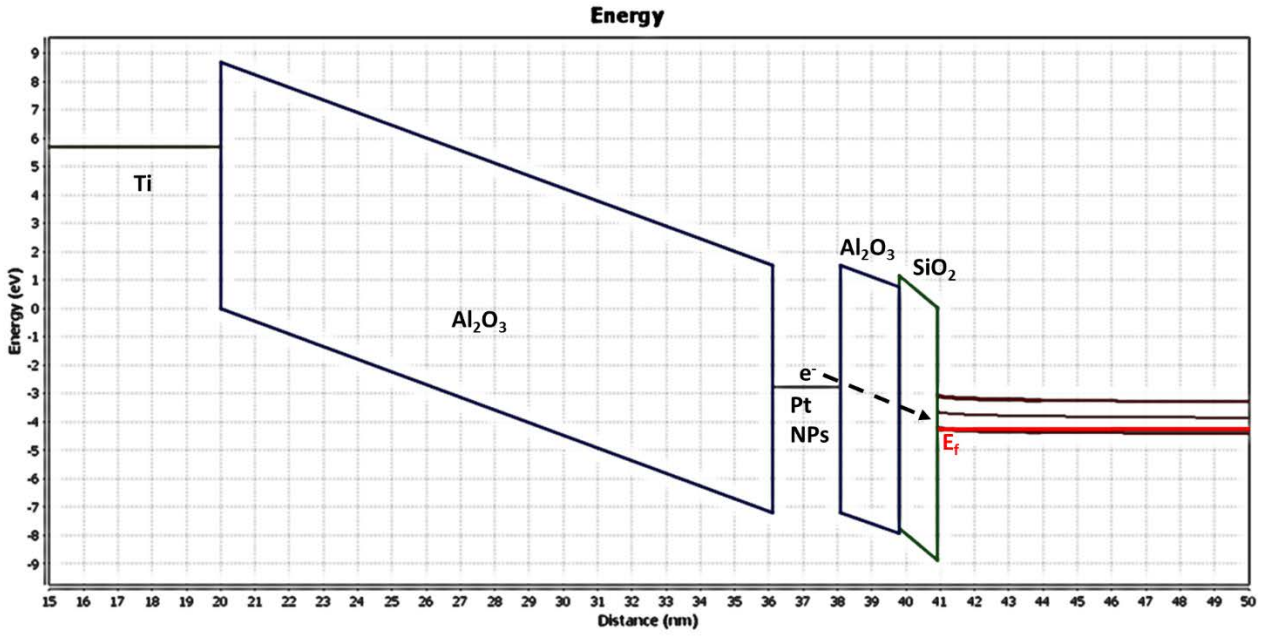


Figure 33: Simulated Band diagram of the MOS capacitor device utilized in this study at an "erasing" gate bias of -10 V. Simulated using "Stacked dual-oxide MOS energy band diagram visual representation program" [187].

5.1.2 Application of High-k dielectrics and influence of post metallization H_2 annealing

Driven by the continuous miniaturization of MOSFETs and thereby memory cells utilizing them, high – k dielectrics have been developed as a viable alternative to SiO_2 within the gate stacks. The advantage of using high-k dielectrics is that for the same equivalent oxide thickness (EOT), the employed high-k dielectrics can have a larger physical thickness than SiO_2, enabling much better control on the gate leakage current [186, 188]. In the drive to find a replacement for SiO_2 in CMOS devices, oxides of hafnium and aluminum emerged as leading candidates [186]. Regarding its usefulness as an alternate dielectric employed within the gate stacks of an NVM with floating gate structure, Al_2O_3 has many favorable properties which include a high band gap, thermodynamic stability on Si up to high temperatures, higher dielectric constant ($k \sim 9$) than SiO_2 ($k \sim 3.9$), and its amorphous nature under the conditions of interest [186]. There are significant advantages in using amorphous dielectrics as they have no grain boundaries or surface facets, which, if present, could result in issues such as higher leakage currents or low local permittivity. They also avoid problems with grain sizes, which can lead to reproducibility related concerns when employed in large scale devices [180]. Also, Robertson has previously reported that aluminum oxide (Al_2O_3) has excellent conduction and valance band offsets when compared to HfO_2 on contact with Si, making Al_2O_3 ideally suited for use with n and p-type Si over a range of doping levels [180]. The concept of a multilayer tunnel barrier concept consisting of a two-layer dielectrics stack with a low- k/high- combination resulting in lower operational voltage or higher speed programming due to the increased current–voltage slope have been proposed over the past decade [189] and is the tunnel barrier employed in this particular study (SiO_2 – low k/ Al_2O_3 – high k).

Since the device structure explored in this study employs a Si-SiO_2 interface, understanding its properties and its effects in governing device performance is essential. Defects at the Si-$Si0_2$ interface, such as fixed oxide charge, oxide trapped charge, and interface traps, continue to be limiting factors in the performance of MOS structures. Interface defects typically arise from the abrupt termination of the crystalline Si lattice. The most widely accepted model for these interface traps is a trivalently bonded silicon atom at the Si-$Si0_2$ interface, denoted by $Si_3 \equiv Si^*$ [190]. In this notation, the three horizontal lines represent the three bonds to bulk silicon atoms, and the * represents the fourth, unpaired valence electron of the silicon atom, which is also referred to as the "dangling bond" in literature. Interfacial charges especially have serious deleterious effects on the flat-band and thereby the threshold voltage, subthreshold slope, and surface carrier mobility [182, 190, 191]. Minimization of interface defects is thus a critical step in fabricating reliable MOS devices. Annealing these MOS structures in an ambient containing hydrogen at relatively low temperatures (typically $250^oC \sim 450^oC$) is considered an effective way of reducing the density of interfacial traps [192]. This annealing step is typically employed after the deposition of the gate metal contact and is referred to as post metallization annealing. Post metallization annealing is employed in this study to minimize the interface defects and more on its effects would be discussed in section 5.3.1.

Also, in the device dielectric stack explored in this study, the high-k Al_2O_3 (as both the tunneling and blocking dielectric layer) is deposited utilizing ALD. It is essential to note that while quality of the ALD deposited tunneling Al_2O_3 layer depends on the surface properties of the SiO_2 layer on the Si surface, the quality of the ALD deposited blocking Al_2O_3 layer on the Pt NP coated tunneling oxide surface is a function of the Pt NP surface coverage. ALD deposited Al_2O_3 on noble metal NP covered surfaces has been previously reported to be substantially porous in nature, where

the high degree of porosity results in a high density of broken or "dangling" bonds near the metal NP surface [193, 194]. Previously, Lu et al reported that the ALD deposited Al_2O_3 overcoating on Pd NPs is porous in nature and grows as a discontinuous film rather than a continuous, pinhole-free coating typically obtained with ALD [194]. Later in this chapter, the porous nature of the ALD deposited Al_2O_3 layer (a function of Pt NP surface coverage) surrounding Pt NPs and exploration of the associated traps based on obtained C-V, G-V characteristics would be discussed in section 5.3.2. Further confirmation of the Pt NP induced porosity for the surrounding ALD alumina overcoating was attained through electrochemical ion penetration studies of the Pt NP embedded Al_2O_3 thin films on n++ Si substrates in section 5.3.3.

5.2 METHODS

5.2.1 Device preparation and electrical characterization

P-doped Si substrates (1-10 Ω cm resistivity range) were first cleaned using the modified Shiraki treatment without removal of the final chemical oxide [195]. This method of Si cleaning was employed in order to introduce a large number of hydroxyl species on the surface, which has been found to aid high quality ultrathin ALD alumina growth [196]. Having surface hydroxyl groups on Si substrates typically results in the initial ALD film growth to be more homogenous when compared to initial film growth on H terminated Si surfaces (where island growth has been reported to be initially prevailing) [197]. The chemical oxide was adjudged to be 1.1 nm based on ellipsometry data. On top of the chemically grown Silicon dioxide, 1.7 nm of Al_2O_3 was deposited using ALD at a process temperature of 300^{o}C using water and Trimethylaluminum (TMA) precursors with a deposition rate of 0.9 Å/cycle. Since hydroxyl-terminated surfaces are desired for complete TMA reaction coverage and defect-free Al_2O_3 formation [198], water was pulsed for

twenty cycles (0.02 s pulses with 8 s purge interval) prior to flowing any TMA vapor. This was followed by repetitive cycles of 0.015 s TMA and 0.02 s H_2O with 8 s purge interval. For the purpose of this study, Pt NPs at different sputtering conditions (sputtering time - 10s, 20s at 23.8 degree target angle and 20s at 38 degree target angle) were sputtered on top of the ALD grown alumina layer. A capping Al_2O_3 layer of 16.1 nm was deposited using similar ALD process parameters as the tunneling layer albeit at a lower temperature of 150^oC on top of the NP layer using ALD giving the total dielectric thickness of 18.9 nm confirmed using ellipsometry. A lower process temperature was utilized for the blocking dielectric layer deposition compared to the tunneling dielectric distribution to minimize temperature induced coalescence of the uncapped Pt NPs. 100 nm Ti and 50 nm Au were subsequently deposited on top of the dielectric using a shadow mask in an e-beam deposition system. A control sample without embedded Pt NPs was also prepared by exactly the same process to verify that the observed capacitance and conductance signatures are solely from the influence of trapped charges at the Pt NP layer, and not from defects within Al_2O_3 [199]. For the post metallization hydrogen anneal, high purity hydrogen was introduced at a rate of ~30 SCCM within the e-beam system chamber under high vacuum conditions (~3 E -8 Torr) at 260^oC for one hour. The dots were imaged under the microscope to gauge their true areas before each measurement. Capacitance-Voltage (C-V – not to be confused by the abbreviation CV used before to denote cyclic voltammetry experiments) characterization of the samples was done under nitrogen flow in a dark confined environment and to optimize device degradation, samples were stored in vacuum in between measurements. High frequency C-V measurements were performed at room temperature using a Keithley 4200-SCS equipped with the 4200-CVU integrated C-V option and pulse generator. Data was taken with a voltage steps ranging from 0.1 V to 0.005V and 30 mV AC signal at a frequency range 10 KHz - 1 MHz. It should be

noted that all C-V, G-V (conductance-voltage) profiles reported in this study were corrected for the possible presence of series resistance [200]. All measurements were taken at room temperature. A schematic of the device structure can be seen in Figure 34.

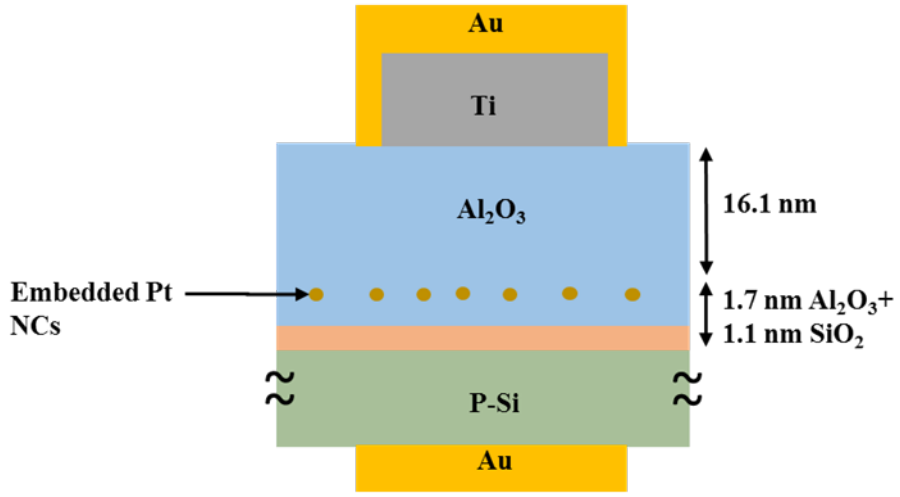


Figure 34: Schematic of MOSCAP device structure with embedded Pt NPs

5.2.2 Pt NP deposition

Details of the sputtering configuration (TTS) utilized in this study is previously discussed in section 1.1. An RF power (13.56 MHz) of 30 W was used to sputter Pt NPs for different deposition times (10s, 20s) and target angles (23.8^o, 38.1^o). Although the Pt NPs embedded in most samples included in this study were deposited at a target angle of 23.8^o, one particular deposition was done at 38.1^o target angle for 20s to attain sub-nm sized ultrafine Pt NPs with a ~ 2 times larger areal density compared to the lower target angle. Pt NP size and areal density obtained from HRTEM images [16] are listed in Table 1**Error! Reference source not found.**. Since the Pt depositions done at 10s, 20s and 45 s sputter times at target angle of 23.8^o have similar areal densities, throughout this chapter, the mean diameters of these Pt NPs (0.76 nm, 0.93 nm and 1.56

nm respectively) would be utilized to refer to the obtained device characteristics. Meanwhile, the device where 20s Pt deposition done at 38.8^{o} target angle has a small embedded Pt NP mean size (0.73 nm), but significantly higher areal density (~2 times) compared to the 23.8^{o} target angle depositions and to avoid confusion this sample would be referred to using the notation 0.73 nm (HD) within this chapter.

5.2.3 Cyclic Voltammetry to ascertain uniformity of ultrathin ALD – Al_2O_3 dielectric

Ion penetration analysis of the Pt NP embedded Al_2O_3 thin films on n++ Si substrates was performed in order to evaluate the uniformity of the dielectric film. Using cyclic voltammetry (CV), the resultant faradaic signals were analyzed to ascertain the degree of ion penetration through the ALD deposited alumina thin film. For all electrochemical experiments, the counter electrode and pseudo reference electrodes were cleaned Pt wires and the electrolyte used was 0.1mM ferrocene in 0.1 M Tetrabutylammonium hexafluorophosphate (TBAHP) in Acetonitrile. The TBAHP was dried in a vacuum oven at 150^{o}C for 24 hrs before making the electrolyte solution in order to get rid of any adsorbed water molecules. The working electrode consisted of Pt NP embedded Al_2O_3 thin films (prepared using ALD) on top of highly doped (n type) Si substrates. First, after modified shiraki cleaning (leaving 1.1 nm chemical SiO_2 layer), 1.7 nm Al_2O_3 was deposited at 300^{o} C using identical ALD process parameters as discussed previously in section 5.2.1. This was followed by Pt NP deposition (different sputtering times at 30 W power and 23.8^{o} Target angle – 10s, 20s and 45s yielding Pt NPs with mean sizes of 0.76 nm, 1.11 nm and 1.56 nm respectively) and subsequent capping by another ALD grown 2 nm Al_2O_3 thin film at 150^{o} C. For comparison, samples with a thicker capping alumina layer (3.8 nm instead of 2 nm) were also prepared in order to analyze the faradaic signatures resultant from ion penetration through these thin dielectrics. Another sample set was added to the second set of the ion penetration experiments

(30 W, 20s, 38.8^{o} target angle) to evaluate the porosity of the thicker capping dielectric. The schematic of the experimental setup evaluating the thinner (2 nm) and thicker (3.8 nm) capping Al_2O_3 layer can be seen in Figure 35 (a) and (b) respectively.

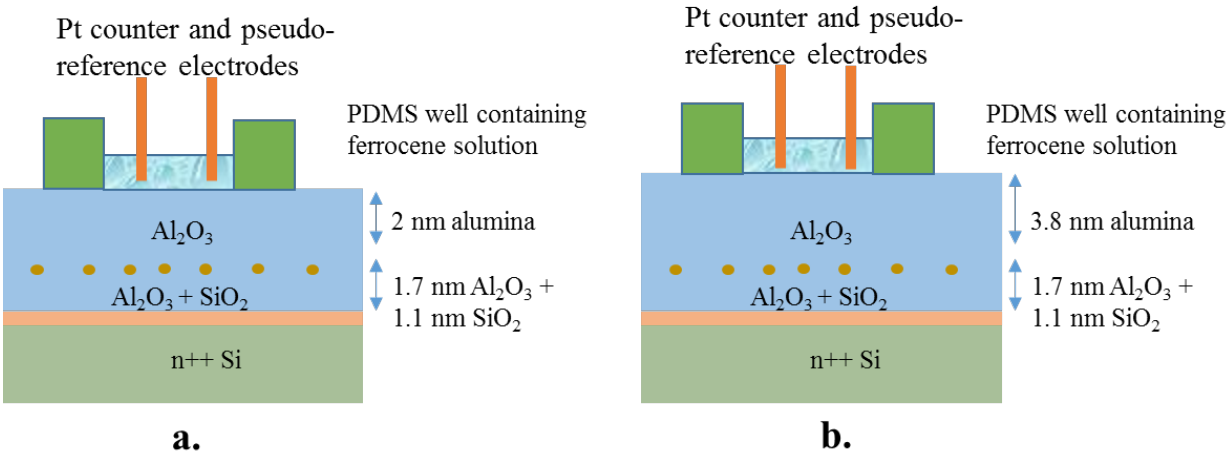


Figure 35: schematic of the electrochemical experimental setup evaluating the – a. thinner (2 nm) and b. thicker (3.8 nm) capping Al_2O_3 layer

5.3 RESULTS AND DISCUSSIONS

In order to ascertain the device characteristics and the effect of embedded Pt NPs, C-V/G-V characterization was done for each sample at multiple dots. C-V sweeps are performed with voltage sweeps from accumulation to inversion, i.e., from negative to positive bias applied on the gate electrode, and back to inversion. A control device (without any embedded Pt NPs) was also prepared on the same p-Si wafer utilizing similar process parameters to the Pt NP embedded devices in order to analyze the dielectric properties. Section 5.3.1 discusses the extracted dielectric characteristics from representative C-V/G-V data and discusses the role of post metallization annealing, which was performed for all devices explored in this study.

5.3.1 Dielectric characterization – Role of Post Metallization Hydrogen Annealing

To understand the impact of Pt NP incorporation within the ALD generated dielectric from representative C-V curves, understanding the quality of the deposited Al_2O_3 is essential. This is due to the fact that the presence of fixed/trapped or mobile charges within the dielectric can lead to shift in the C-V curves and can introduce non-ideality features which can make understanding the role of embedded Pt NP in determining the device's memory retention characteristics challenging. In this section, the C-V characteristics of a MOS capacitor structure without embedded Pt NPs and the role of 260°C post metallization hydrogen annealing is discussed. The C-V measurement of the control sample without any embedded Pt NPs displaying hysteresis at low bias conditions can be seen in

Figure 36. It is interesting to note that under low bias testing conditions (probed within 2 V gate bias window) the hysteresis at the flat band voltage reduces by almost an order of magnitude (0.03 V to 0.004 V) after post-metallization annealing. This reduction in hysteresis is accompanied by significant (~30 times) reduction of the frequency normalized series resistance adjusted conductance (G/ω) peak for the sample after post-metallization H_2 annealing at 1 Mhz (

Figure 37). A conductance peak is typically observed because of the ac loss due to capture and emission of carriers near the Si surface [200]. Although comparing the exact density of interface states (D_{it}), which can be extracted from the equivalent parallel conductance (G_p /ω) peak [201], would be ideal, this calculation was difficult due to two major measurement system limitations. First, there existed a severe reduction in low frequency series resistance adjusted G/ω signal magnitude (close to the system noise level) for the sample after post metallization annealing making accurate determination of G_p /ω challenging. Secondly, the control samples' equivalent parallel conductance (G_p /ω) peak could not be probed within the measurable frequency window (the Keithley 4200 has the minimum measurable frequency limitation at 10 KHz), thereby making location of the exact value at which the conductance peaks for a given value of gate bias uncertain. Despite this limitation, one can qualitatively ascertain the relative magnitude of the density of interface states as it is proportional to the G/ω magnitude [182, 201]).

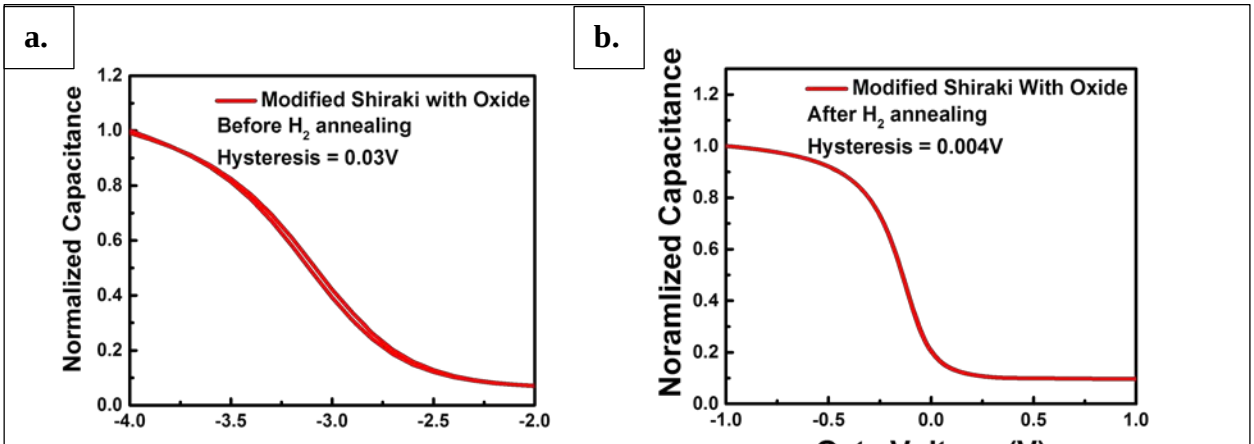


Figure 36: Small window (2 V gate bias) hysteresis for the samples before (a) and after (b) H_2 annealing at 1 MHz

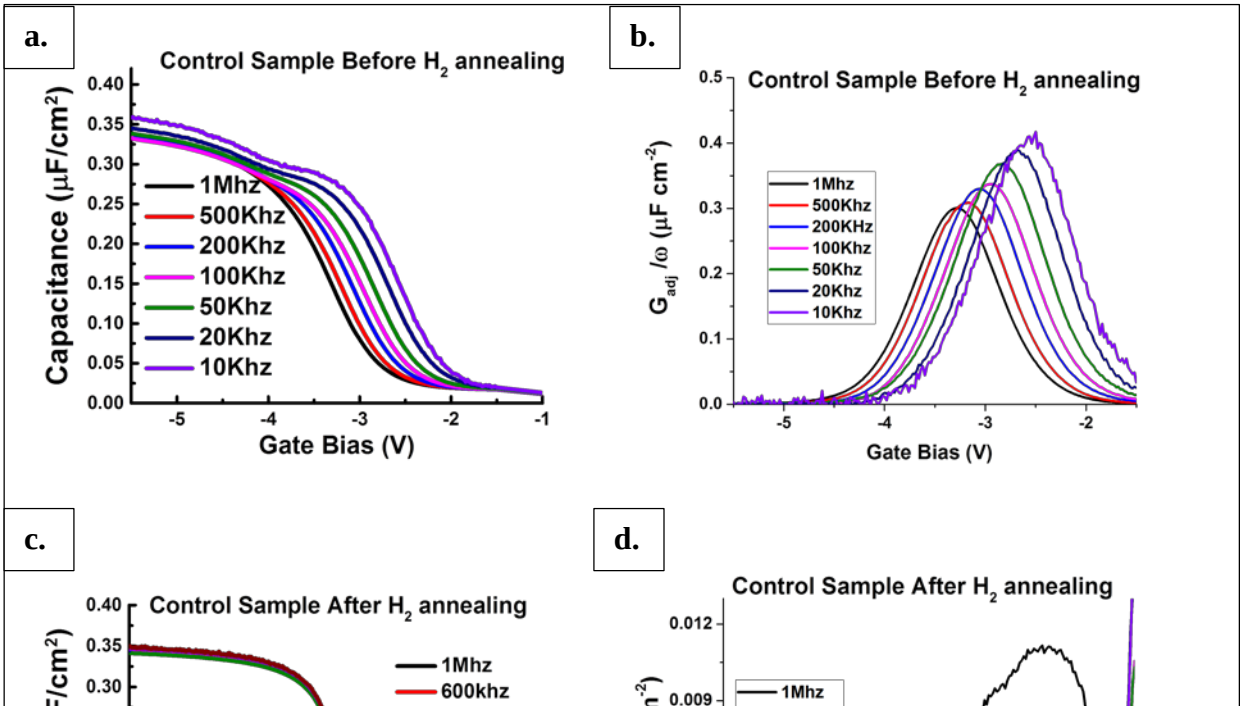


Figure 37: Frequency dispersion in the capacitance and series resistance adjusted conductance for the control sample before ((a) and (b)) and after ((c) and (d)) 260º C post metallization H_2 annealing. The adjusted conductance data for 20 KHz and 10 KHz have not been included in (d) as the conductance signal is close to the measurement system limitation leading to overcorrection and negative conductance values.

The reduction in extracted hysteresis and conductance characteristics indicate significant reduction in the density of interface states at the Si/SiO_2 interface after post metallization H_2 annealing. The dielectric constant of the control oxide (17.8 nm Al_2O_3 + 1.1 nm SiO_2) was calculated based on the capacitance value at the accumulation regime (C_{OX}) of the MOSCAP and found to be 7.73. It can be safely assumed that in the two terminal MOS capacitor structure employed in this study, the 17.8 nm Al_2O_3 and 1.1 nm SiO_2 thin films would act in series and the actual dielectric constant of ALD Al_2O_3 film was calculated to be 7.82. The flat band voltage (V_{FB}) was derived from the C-V plot utilizing the comparative technique (comparing the experimental C-V plot with a simulated ideal C-V plot) for the control sample after H_2 annealing and was found to be -0.07 V [202]. The absence of any significant hysteresis (0.004 V in the -1 to 1 V gate bias range) further points to the substantial reduction of interface trap density for the samples after post-metallization annealing.

The chemistry behind the passivation of Si/SiO_2 interface states due to post metallization H_2 annealing has been explored in numerous past studies [190, 192, 203]. These interface states have energy levels distributed throughout the silicon band gap and originate from a trivalently bonded silicon atom with an unpaired electron, which are also referred to

as P_b centers in most published literature [190]. Although low temperature H_2 post oxide deposition annealing (pre metallization) also helps reducing the Si/SiO_2 interface trap density [192], there is an enhancement in the degree of passivation in the presence of a metal gate. The pronounced effectiveness of interface trap passivation for annealing under metal gates compared to polysilicon gates is suggestive of two species of hydrogen being involved in the process. In polysilicon gated devices, molecular hydrogen from the ambient or the polysilicon grain boundaries has been proposed to diffuse through the oxide and passivate the Si dangling bonds at the Si/SiO_2 interface. Whereas for metal gated devices, atomic hydrogen is held responsible for passivating these traps. In case of post metallization anneal with Al gates electrodes, presence of atomic hydrogen was deemed responsible by Johnson et al. for passivating the interface traps [204]. It has been proposed that atomic hydrogen is produced at the $Al\text{-}Si0_2$ interface, which then diffuses to the $Si/Si0_2$ interface and reacts with the interface traps, subsequently passivating them [190]. Hydrogen is postulated to be produced by aluminum reacting with trace amounts of water at the interface, producing a thin layer of aluminum oxide as well as atomic hydrogen. In the case of the NVM MOS capacitor structure employed in this study, Au coated Ti is the gate metal deposited on top of Al_2O_3 blocking layer. The hydrogen dissociation properties of Ti are well documented in literature and previous DFT studies have indicated a lack of H_2 dissociation barrier on Ti surface [205]. The effectiveness of post metallization H_2 annealing induced passivation of interface traps for the aforementioned control device (

Figure 37) indicates a large presence of atomic hydrogen within the dielectric. Due to the negligible dissociation barrier of H_2 on Ti, it is likely H_2 molecule dissociates on the Ti gate metal and enters the Al_2O_3 from the Ti/Al_2O_3 interface. Once inside the ALD deposited Al_2O_3 film, the hydrogen atom migrates down to the Si/SiO_2 interface, subsequently passivating the Si dangling bonds responsible for the interface traps. High level of Si/SiO_2 interface state passivation induced by hydrogen migration through Al_2O_3 capping layer on SiO_2 at relatively low annealing temperatures have been previously reported by Dingemans et al [206]. The reported high degree of passivation was attributed in part to the effective transport of hydrogen from the Al_2O_3 capping dielectric toward the Si interface during annealing.

Since post metallization hydrogen annealing significantly reduces the interface trap density contribution to the experimentally obtained capacitance values, the shift in V_{FB} (-0.07 V) from the theoretical value of -0.6 V can be attributed to the presence of a net negative fixed charge density of 1.15 E 12 cm^{-2} at the ALD alumina/ SiO_2 interface. The presence of negative fixed charges at Al_2O_3/SiO_2 for ALD deposited alumina has been reported before and has proven beneficial in passivation of p-type silicon surfaces and heavily doped p+ regions for fabricating solar cells with low surface recombination velocities [207]. The origin of these fixed charges at the interface of the ALD grown Al_2O_3 and chemically grown SiO_2 have been attributed to Al vacancies resulting from a preferential tetrahedral coordination of Al in the region close to the interfacial SiO_2 layer [208]. Similar to the 0.53 V V_{FB} shift observed in this study, for ALD deposited Al_2O_3 films on Si, Wilk et al. also report a measured flatband voltage shift of about 300 to 800 mV, when compared to the expected value for the electrode and substrate types used [209]. The hysteresis of the control sample at larger applied gate biases can be seen in **Figure 38**. It's interesting to note that although there is minimum observable hysteresis for the -5 V to 5 V bias regime (under 0.1 V), an increase in hysteresis for the -6V to 6V sweep was observed (0.4 V). This increased shift in the flat band voltage observed during the reverse sweep (6V to -6V) leading to the increased hysteresis is consistent with a build-up of negative charge with increasing gate bias within the dual layer employed in this study. The 400 mV hysteresis observed in the -6 to 6 V gate bias cycling corresponds to a charge density of 8.65 E 11 cm^{-2} and was accounted for in all the memory window calculations discussed later in section 5.3.3.2 of this chapter. The absence of any substantial hysteresis for the control sample within the low applied gate bias regime and the reduction in frequency dispersion and magnitude of G/ω (

Figure 37) shows that the resultant control oxide is of good quality (after post metallization annealing) and the presence of any anomalous features within the C-V, GV characteristics for the Pt NP embedded samples can be safely attributed to the sole influence of Pt NP induced phenomena within the dielectric, more on which would be discussed in the next section of this chapter.

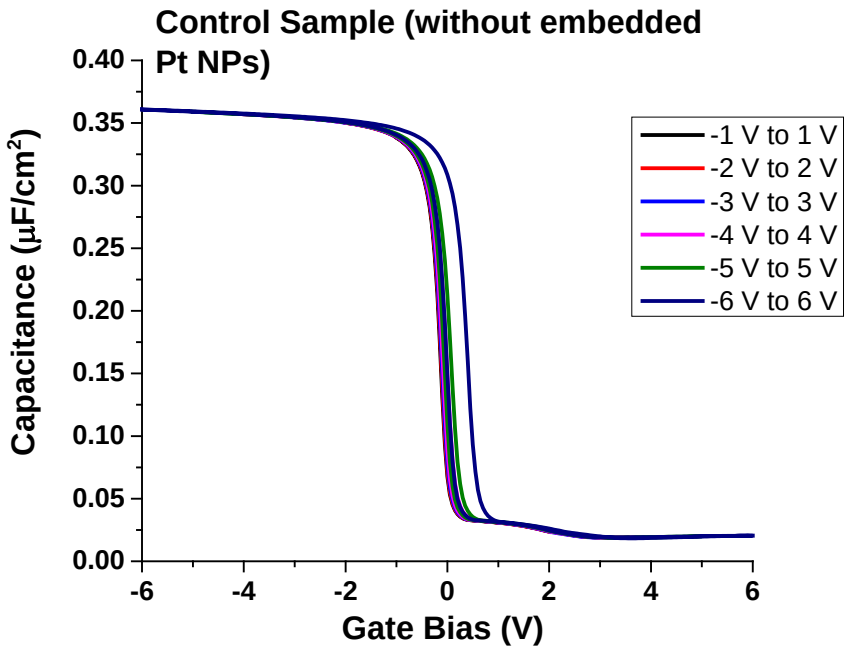


Figure 38: Observed hysteresis within the control sample at larger gate biases

5.3.2 C-V, G-V characteristics of different Pt NP embedded NVM MOS capacitors

Before discussing the obtained C-V, G-V characteristics of the different sized Pt NP embedded NVM MOS capacitors, it is essential to gain an understanding of the gate bias required to program devices. The following section discusses the contribution of Pt NP size dependent charging energies in determine the programming gate bias.

5.3.2.1 Pt NP size/areal density dependent charging

In order to calculate the gate bias required to charge the embedded Pt layer, the NP size and areal density dependent charging energy needs to be taken into consideration. Charging a NP with electrons are often associated with two kinds of energies: Coulomb charging energy (CCE) and quantum confinement energy (QCE), where the Coulomb charging energy arises from the self-capacitance of the NP and the Quantum confinement is linked to the spatial confinement of electrons [210]. CCE is based on electrostatic capacitive charging energy, where for every addition charge *dq* transported to a conductor, work has to be done against the field of already present charges. Thus charging a capacitor with a charge q requires and energy -

$$E = {(q)^2}/{2C} \tag{16}$$

Where C is the total capacitance coupled to the NP. The total capacitance value changes as a function of the Pt NP size, density, tunneling and blocking dielectric thickness in the embedded nanocrystal memory system.

The capacitance for a metal NP embedded in a dielectric is given by -

$$C = 4\pi\varepsilon_{medium} a[1 + \frac{a}{2d} + \frac{\left(\frac{a}{2d}\right)^2}{1-\left(\frac{a}{2d}\right)^2}] \tag{17}$$

Where '*a*' is the radius of the NP and '*d*' is the distance from the surface of the electrode to the center of the NP. Using these, equations for C_{BO} (capacitance contribution of blocking oxide) and C_{TO} (capacitance contribution of blocking oxide) can be calculated. The total capacitance

associated with the NP (C_{tot}) is an addition of its self-capacitance from the tunneling (C_{TO}) as well as the blocking oxide (C_{BO}) layers

$$C_{tot} = C_{TO} + C_{BO} \quad (18)$$

Also, the electric potential of the embedded NP can be given by -

$$V_{NP} = V_b C_{BO}/C_{tot} \quad (19)$$

Where V_{NP} is the voltage build up at the NP and V_b is the bias voltage. In order to derive the voltage required to tunnel in the first electron, the work done by injecting the first electron U_N (N) should equal or be greater than the change in the energy at the NP.

$$U_N(\mathrm{N}) = \mathrm{QCE} + \mathrm{CCE} = \mathrm{e}V_b C_{BO}/C_{tot} \quad (20)$$

It should be noted that for decreasing NP size the energy level spacing of electron states increases indirectly proportional to the square of the dot size. In this case, assuming an infinite potential well, the quantum confinement energies can be calculated using –

$$\mathrm{QCE} = 2/3\ E_F / N \quad (21)$$

where E_F is the Fermi energy of Pt (8.79 eV) [211] and N is the number of atoms in the NP. It should be noted though that for NPs less than 1 nm in size, the obtained QCE values are a mere approximation and one would have to apply cluster theory to calculate the energy levels more precisely. The calculated values of V_b, QCE and CCE for different NP sizes employed in this study are listed in Table 8. It can be seen that while the 0.76 nm Pt NP embedded devices require a ~1V gate bias (*Vb*) to program the NP layer with one electron per NP, for larger 0.93 nm Pt NP embedded devices, the *Vb* values drops to 0.64V for 0.93 nm and 0.22V for 1.56 nm sized NPs.

For the case of 0.73 nm sized Pt NPs with high areal density, the calculated *Vb* value (1.17V) is similar to the 0.76 nm Pt NP case as the *Vb* calculation employed here does not take areal density into account. The areal density is taken into account while calculating the tunneling matrix element (T_{NP}) which can be calculated using

$$T_{NP} = \hbar / (m^* D^2) \quad (22)$$

where *D* is an average distance between NPs and $m*$ is an effective mass of electrons in Pt [212]. The magnitude of T_{NP} is essentially an indication of the degree of lateral coupling between neighboring Pt NPs in the embedded layer. Here, *D* is a function of both the Pt NP size and areal density ($D = \frac{10}{areal\ density^{0.5}} - (NP\ radius)$) and the calculated values of T_{NP} for different sputtering conditions employed in this study are listed in Table 8. As T_{NP} increases and becomes comparable to single electron addition energy (QCE+CCE) for the system employed in this study, coupling between neighboring Pt NPs also increases, which could subsequently result in poor charge retention characteristics of the embedded Pt NP layer in the NVM device. The T_{NP}/(QCE+CCE) fraction listed in Table 8 gives an indication of the relative effect of nearest neighbor Pt NP coupling w.r.t its single electron addition energy. While this fraction is lowest (0.03) for the case 0. 76 nm sized Pt NP, it's approximately more than twice for the 0.93 nm and 0.73 nm (high areal density) case, with 1.56 nm Pt NPs resulting in the highest obtained values (0.35). Thus, the nearest Pt NP neighbor coupling is predicted to increase in the following sequence - 1.56 nm → 0.93 nm, 0.73 nm (HD) → 0.76 nm. This prediction is in line with the charging/discharging behavior observed in the C-V characteristics with the representative Pt NP incorporation. This would be discussed later in the next section discusses the C-V/G-V characteristics of the different Pt NP incorporated NVM MOS capacitors.

Sputter conditions (P = 30 W, varying time, target angle)	**Mean Pt NP size (nm)**	**Mean Pt NP areal density (X 10 ^{12} cm^{-2})**	**Effective Self-Capacitance (aF)**	**Coulomb Charging energy (CCE) (meV)**	**Quantum Confinement Energy (QCE)* (meV)**	**Gate bias required to Program NP (V_b)**	**Tunneling matrix element (T_{NP}) (meV)**	**Tunnel matrix element (T_{NP}) / electron addition energy (CCE+QCE)**
10s, 23.8^o	0.76	4.71	0.69	116.22	386.76	1.04	15.65	0.03
20s, 23.8^o	0.93	5.90	0.85	94.07	214.87	0.64	22.82	0.07
20s, 38.8^o	0.73	10.90	0.66	121.21	446.26	1.17	43.85	0.08
45s, 23.8^o	1.56	5.92	2.19	57.19	44.63	0.22	35.64	0.35

Table 8: Theoretical V_b, QCE and coulomb charging energy for different NP sizes studied in the paper

5.3.2.2 C-V, GV characteristics of different Pt NP embedded NVM MOS capacitors under low gate bias

Before delving further into the Pt NP size/areal density dependent C-V characteristics discussed in this section, it should be noted that in typical memory devices, charges are injected through the tunnel oxide when the bias value becomes sufficient (as discussed previously in section 5.3.2.3). If a sufficient programming/erasing gate bias is applied to the device, a positive flat band voltage shift extracted from the C-V plots is attributed to electron trapping (programming) and negative flat-band shift is due to electron de-trapping (erasing) [72]. However, it should be also noted that in case where insufficient bias voltage is applied to program the Pt NPs, the shift in flat band voltage would be an indication of the dielectric and interface characteristics, with net positive fixed/interface states leading to a negative flat band voltage shift and vice-versa.

Figure 39 displays the C-V characteristics for the control and different sized Pt NP embedded NVM MOS capacitors at an AC probe frequency of 1 MHz within a small 2 V gate bias window. While sweeping the gate bias from accumulation to inversion (forward sweep), a positive shift in flat band voltage (ΔV_{FB} - relative to the control sample with no embedded Pt NPs) is observed for all Pt NP embedded devices. It is interesting to observe that this ΔV_{FB} value increases w.r.t the percentage surface coverage of Pt deposited on the tunneling Al_2O_3 layer. The percentage surface coverage is a function of both the Pt NP size and areal density and is directly proportional to the product of mean Pt NP area (its 2D projection – essentially area of a circle) and the areal density. It is important to note that the ΔV_{FB} observed in the forward sweep is not representative

of the Pt NP layer charging characteristics, but are representative of the of the defects/traps in the dielectric and at the interfaces in close proximity to the p-Si surface. The programming (charging with e^-) properties of the Pt NP layer are represented by the positive C-V plot shifts and degree of hysteresis observed for the Pt NP embedded devices over the reverse sweep (from inversion to accumulation).

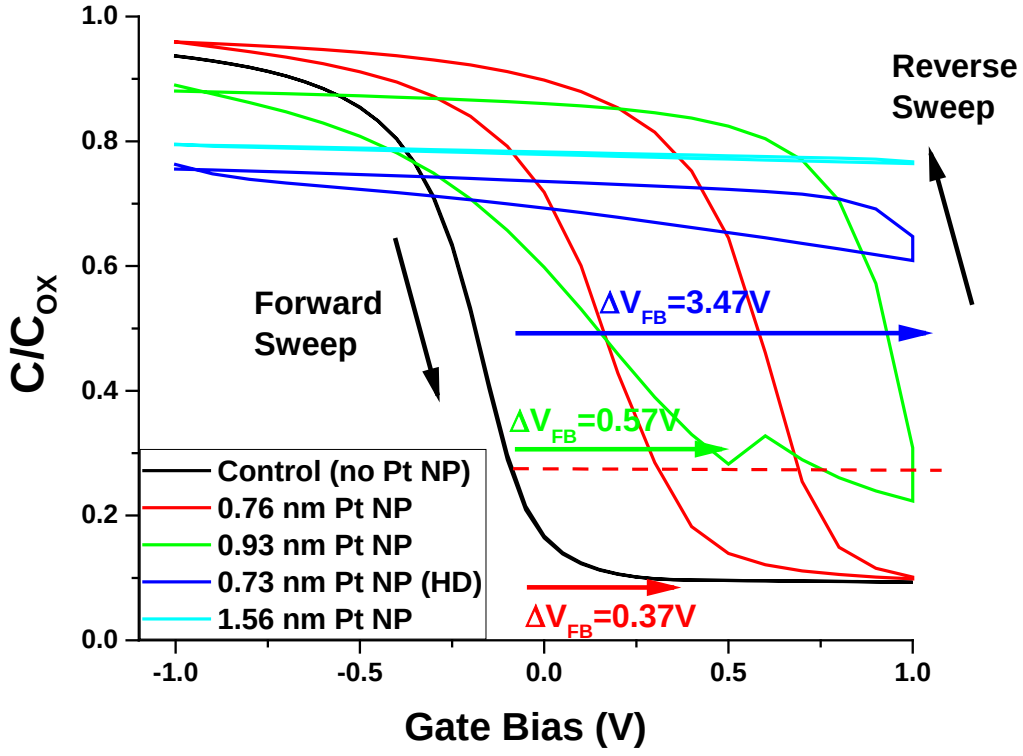


Figure 39: Normalized C-V characteristics for the control and different sized Pt NP embedded NVM MOS capacitors at 1 MHz within a small 2 V gate bias window. The shift in V_{FB} (ΔV_{FB} relative to V_{FB} of the control sample) calculated for the forward sweep has been highlighted using the colored arrows (ΔV_{FB} - 0.76 nm Pt (red) ~ 0.37 V, 0.93 nm Pt (green) ~ 0.57 V, 0.73 nm Pt (HD) (blue) ~ 3.47V)

The ΔV_{FB} observed for the Pt NP embedded devices displayed in Figure 39 were calculated based on the flat-band capacitance matching method [202] and are indicative of both fixed and

interface charges. This cumulative charge density (Q_{Fixed} + Q_{In}) can be calculated from the experimentally obtained ΔV_{FB} value (for forward sweep) using –

$$Q_{Fixed} + Q_{In} = C_{OX}\ \Delta V_{FB} \quad (23)$$

Where C_{OX} is the oxide capacitance of the representative sample extracted from its accumulation regime. The calculated values of the flat-band shifts and corresponding charge densities for different Pt NP embedded MOS capacitors can be seen in Table 9. For 0.76 nm Pt NPs with surface coverage of 2.13%, ΔV_{FB} = 0.37 V, for 0.93 nm Pt NPs with surface coverage of 3.66%, ΔV_{FB} = 0.57 V, for 0.73 nm Pt NPs (high areal density) with surface coverage of 4.56%, ΔV_{FB} = 3.47 V, whereas for 1.56 nm Pt NPs with surface coverage of 11.31%, ΔV_{FB} could not be determined as the sample never reached inversion within the studied gate bias regime.

Sputter conditions (P = 30 W, varying time, target angle)	**Mean Pt NP size [nm]**	**Mean Areal Density (X 10^{12}) [cm^{-2}]**	**Pt Surface Coverage [%]**	**ΔV_{FB} (Forward Sweep) [V]**	**$Q_{fixed} + Q_{In}$ (X 10^{12}) [C/cm^2]**	**$\Delta V_{FB\ INJ}$ (Reverse Sweep) [V]**	**Q_{INJ} (X 10^{12}) [$C\ cm^{-2}$]**	**Number of injected charge per NP**
10s, 23.8^o	0.76	4.71	2.13	0.37	0.80	5.00	9.94	2.11
20s, 23.8^o	0.93	5.90	3.66	0.57	1.09	5.20	9.14	1.55
20s, 38.8^o	0.73	10.90	4.56	3.47	5.96	2.55	3.51	0.32
45s, 23.8^o	1.56	5.92	11.31	-	-	-	-	-

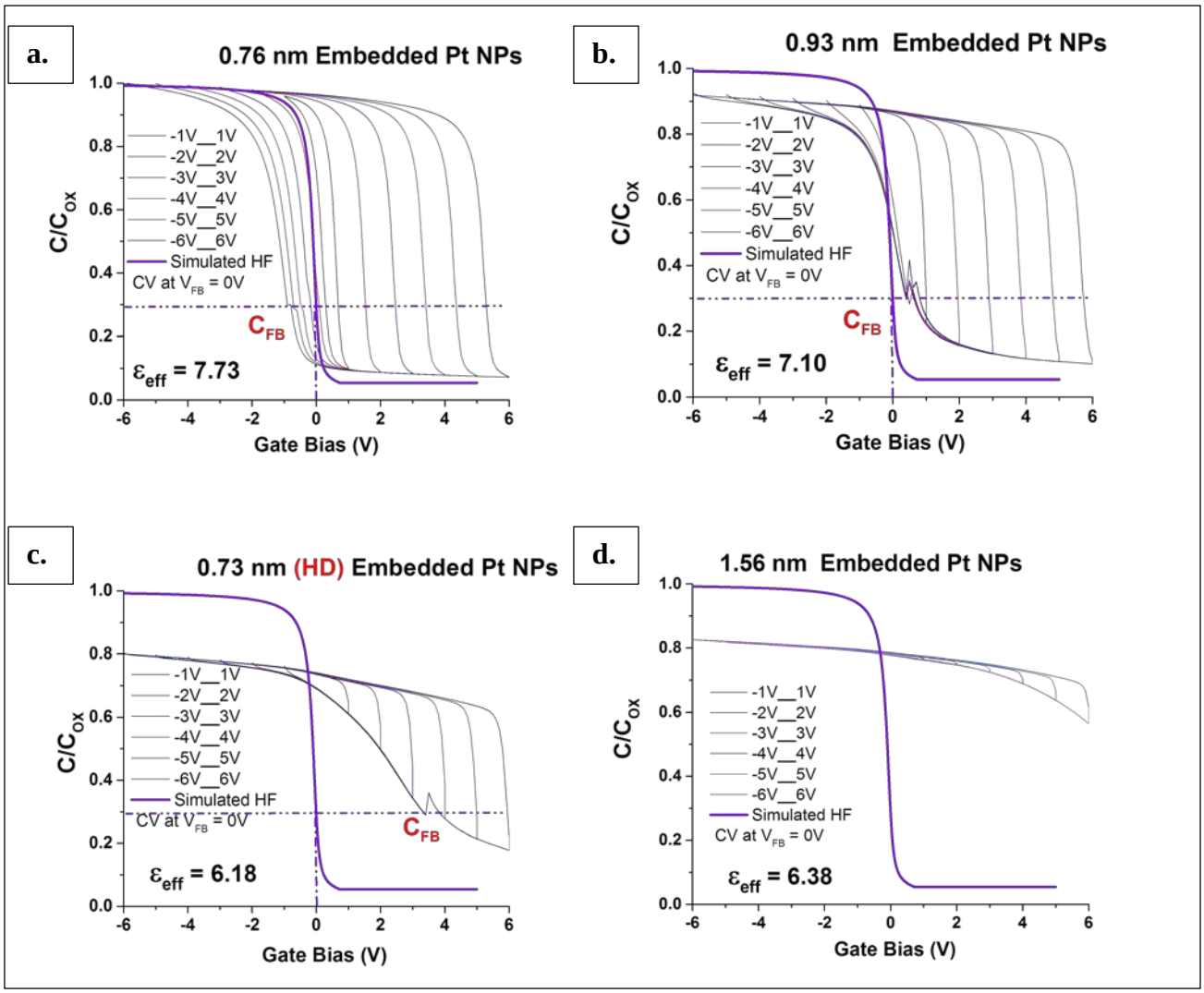
Table 9: Calculated values of the flat-band shifts and corresponding charge densities for different Pt NP embedded MOS capacitors. ΔV_{FB} is obtained from the forward sweep in the low bias probing regime (-1 V to 1V) corresponds to the combined density of fixed and interface traps (Q_{fixed} + Q_{In}) and $\Delta V_{FB\ INJ}$ is obtained from the reverse sweep after programming the MOS capacitor at 6V gate bias and corresponds to the density of injected charges (Q_{INJ}). The number of injected charges per NP are also included. Note that for the 1.56 nm embedded device never reached the flat band capacitance value within the -6 to 6 V gate bias window and thus the corresponding flat-band shifts and charge densities could not be calculated

Since ΔV_{FB} calculated over the forward sweep increases with Pt NP surface coverage, and is indicative of defects within the dielectric, it can be surmised that these defects are a direct result of Pt NP incorporation. Apart from increasing flat band shift with increasing Pt NP surface coverage, the effective dielectric constant (ε_{eff} - which in this case is directly proportional to the dielectric capacitance and given similar dielectric thicknesses should only varies with the C_{OX} value) also decreases with increase in Pt NP surface coverage (Figure 40). For 0.76 nm Pt NPs with surface coverage of 2.13%, ε_{eff} = 7.73 (similar to the control samples), for 0.93 nm Pt NPs with surface coverage of 3.66%, ε_{eff} = 7.10 and for 0.73 nm Pt NPs (high areal density) with surface coverage of 4.56%, ε_{eff} = 6.18. It is worth mentioning that due to the leaky nature of the 1.56 nm Pt NP embedded device and their inability of achieve inversion within the studied gate bias regime, all future discussions would focus primarily on the C-V/G-V signatures obtained from 0.76 nm , 0.93 nm and 1.56 nm embedded devices. The decrease in ε_{eff} values with increasing Pt NP surface coverage can be explained based on the increase in porosity of ALD deposited Al_2O_3 surrounding the Pt NPs. As discussed previously in section 5.1.2, ALD deposited Al_2O_3 on noble metal NP covered surfaces has been previously reported to be substantially porous in nature, where the high degree of porosity results in a high density of broken or “dangling” bonds near the metal NP surface [193, 194]. Thus, based on the increasing extracted defect density within the dielectric and increasing porosity (decreasing ε_{eff}) being a function of increasing Pt NP surface coverage, it can

be surmised that incorporation of Pt NPs introduce defects (due to Al_2O_3 dangling bonds near the Pt NPs) which in turn affect the device performance. The increase in thin (<5 nm) ALD Al_2O_3 porosity with increasing Pt NP surface coverage was also explored using electrochemical ion penetration studies and is discussed later in section 5.3.3.

Figure 40 displays the C-V characteristics for the different sized Pt NP embedded NVM MOS capacitors with mean NP sizes of (a) 0.76 nm, (b) 0.93 nm (c) 0.73 nm (high areal density) and (d) 1.56 nm within a gate bias window of -6 V to 6 V. It is interesting to note that the C-V curve obtained in the reverse sweep (after e^- programming) for all Pt NP incorporated NVM MOS capacitor devices is similar in shape to the ideal simulated CV plot (albeit shifted in the positive direction due to e^- programming) and depicts negligible effects due to defect states close to the Si surface with their energy level within the Si band gap (which typically leads to a C-V stretch-out [177, 182]). Based on the e^- programming induced flat-band shift for the reverse sweep C-V plots ($\Delta V_{FB\ INJ}$), the injected charge density (Q_{INJ}) can be calculated using a similar calculation used previously to obtain $Q_{Fixed} + Q_{In}$. Q_{INJ} divided by the areal density essentially gives an estimate of the number of injected charge per NP, which is typically an overestimation since the experimentally obtained areal density values are an underestimation as Pt NPs smaller than 0.5 nm are challenging to observe in HRTEM images and have not been accounted for in the reported mean areal density and NP size distribution. The calculated values of the flat-band shifts and corresponding charge densities for different Pt NP embedded MOS capacitors has been included in Table 9. While ΔV_{FB} obtained from the forward sweep in the low bias probing regime (-1 V to 1V) corresponds to the combined density of fixed and interface traps ($Q_{fixed} + Q_{In}$) and $\Delta V_{FB\ INJ}$ is obtained from the reverse sweep after programming the MOS capacitor at 6V gate bias and corresponds to the density of injected charges (Q_{INJ}). The 400 mV hysteresis observed for the

control sample during the -6 to 6 V sweep (Figure 38) was accounted for in the Q_{INJ} values reported in Table 9. The number of injected charges per NP is also included in Table 9. The 1.56 nm embedded device never reaches the flat band capacitance value within the -6 to 6 V gate bias window and thus the corresponding flat-band shifts and charge densities could not be calculated. The "ideal C-V shape" observed during the reverse weeps is in contrast with the forward sweep, where C-V plots show substantially more "stretch-out" (Figure 39, Figure 40), with a substantial increase in the degree of this "stretch-out" with increasing Pt NP surface coverage. To understand this dependence of this "stretch-out" phenomenon on Pt NP surface coverage, understanding the location of the Pt NP introduced defects within the dielectric, their proximity to the Si surface and the degree of their interactions with the Si surface governing the p-Si surface potential is paramount.



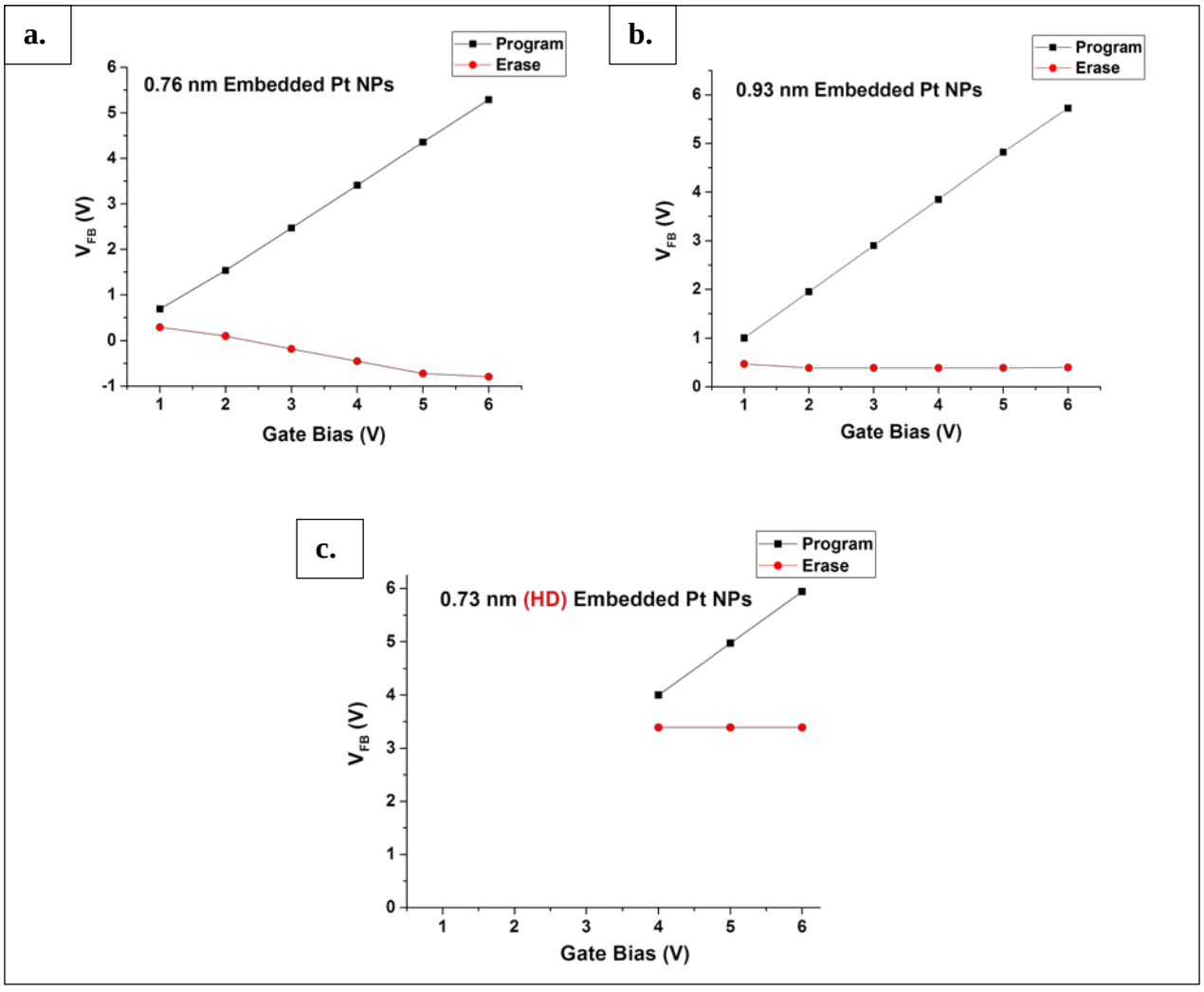


Figure 41: Extracted Flat band voltage (V_{FB}) vs. gate bias for electron programming and erasing for (a) 0.76 nm, (b) 0.93 nm (c) 0.73 nm (high areal density) Pt NP embedded MOS capacitors

Due to the incorporation of an ultrathin tunneling layer (Figure 34), the Pt NP-Al_2O_3 interface dangling bonds are close enough to the Si surface (2.8 nm) where they can be treated as "Border Traps", which are essentially defects at or near the SiO_2/Si interface are distributed in space and energy and communicate with the Si over a wide range of time scales [177]. While for interface traps, the communication of substrate electrons/holes with interface traps is predominantly by capture/emission, for border traps it is mainly by tunneling from the semiconductor to the traps and back. Based on how these "border traps" interact with the Si surface, they can display the signatures of a fixed charge (flat band shift - no C-V "stretch-out") as well as interface traps (flat band shift + C-V "stretch out") depending on two major factors - distance of the Pt NPs from the Si surface and the dielectric constant of the tunneling layer. As can be seen in Figure 39 and Figure 40, in the case of 0.76 nm embedded Pt NPs, there is a minimal CV stretch-out (only a positive V_{FB} shift corresponding to negative fixed charges), whereas for the 0.93 nm Pt NP and 0.73 nm Pt (HD) (~2 times areal density compared to other Pt NP depositions) incorporated samples, there is a significant C-V stretch-out observed in the forward sweep. All the Pt NP embedded devices show asymmetric electron program/erase characteristics which is evident from the CV characteristics in Figure 40 and the plotted extracted Flat band voltage (V_{FB}) vs. gate bias for electron programming and erasing for (a) 0.76 nm, (b) 0.93 nm (c) 0.73 nm (high areal density) Pt NP embedded MOS capacitors in Figure 41. While the distance of Pt NPs from the p-Si surface is essentially the same for all cases, the effective dielectric constant of the tunneling dielectric varies and as discussed previously in this section shows a decreasing trend with increasing Pt NP surface coverage. Thus, for 0.93 nm Pt NP and 0.73 nm Pt (HD) incorporated devices, for the same distance between the "border traps" and the Si surface, the devices with lower effective tunneling dielectric constant allow these "border traps" to play a bigger role in interacting with the Si surface and thereby

affecting the resultant CV plots. More discussion on the timescales and location of the energy level of these "border trap'" w.r.t the Si band gap and the potential fermi-level pinning of the incorporated Pt NP work-function by these "border traps" is discussed in the next section of this chapter.

5.3.2.3 Sweep rate and frequency dependent C-V, GV characteristics of different Pt NP embedded NVM MOS capacitors

To gain a qualitative understanding of the type and time-scales of the "border-traps" introduced upon Pt NP incorporation, forward and reverse sweeps at difference scan rates (ranging from 0.1 to 2 V/s) and frequencies (ranging from 10 KHz to1 MHz) were performed on the NVM MOS capacitors. Fleetwood et al. have previously reported that the effective density of "border traps" depends on the time scale and bias conditions of the measurements [213]. To comprehend the position of the "border traps" within the p-Si bandgap, it is important to understand the change in surface potential with applied gate bias for the MOS capacitor structure employed in this study. Figure 42 displays the surface potential (ϕ_s) variation for an ideal MOS capacitor on a p-doped (doping concentration of 3 E 15 cm^{-3}) Si surface with and 18.9 nm dielectric with a dielectric constant of 7.73 with 0V flat-band voltage. As the gate bias is swept in the forward direction, the surface potential moves from the conduction band edge of Si to the valence band edge and vice versa.

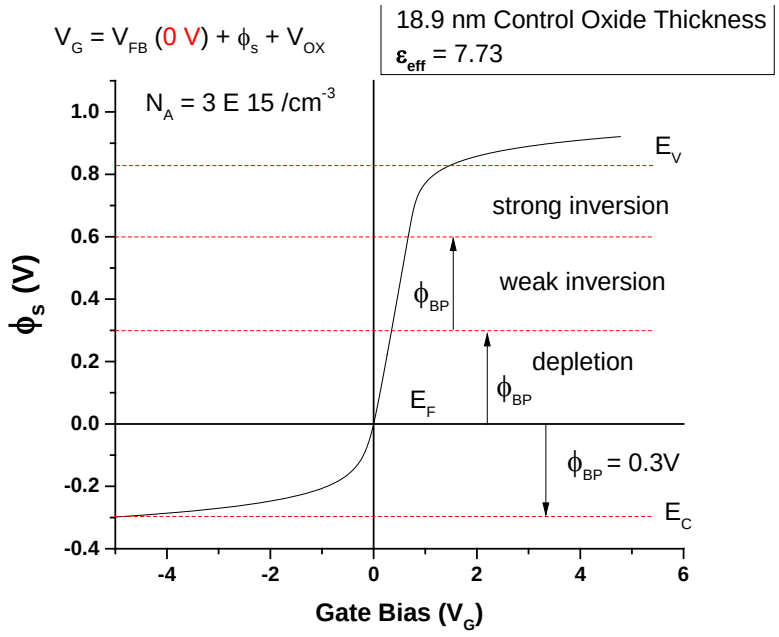


Figure 42: Gate Bias vs Surface potential for the MOS capacitor configuration (calculated at V_{FB} = 0 V) used in this study

Figure 43 (a) and (b) displays the C-V and G-V characteristics of the 0.76 nm Pt NP embedded device obtained during the forward sweep whereas Figure 43 (c) and (d) displays the devices C-V and G-V characteristics in the reverse sweep. It is interesting to note that an anomalous spike is seen in the C-V plots obtained for the forward sweeps near the flat-band condition and with decreasing sweep rates, the flat-band voltage shifts towards more positive gate biases. The anomalous C-V spike is mirrored by a conductance peak near the sweep rate dependent flat-band bias which becomes broader with decreasing scan rate.

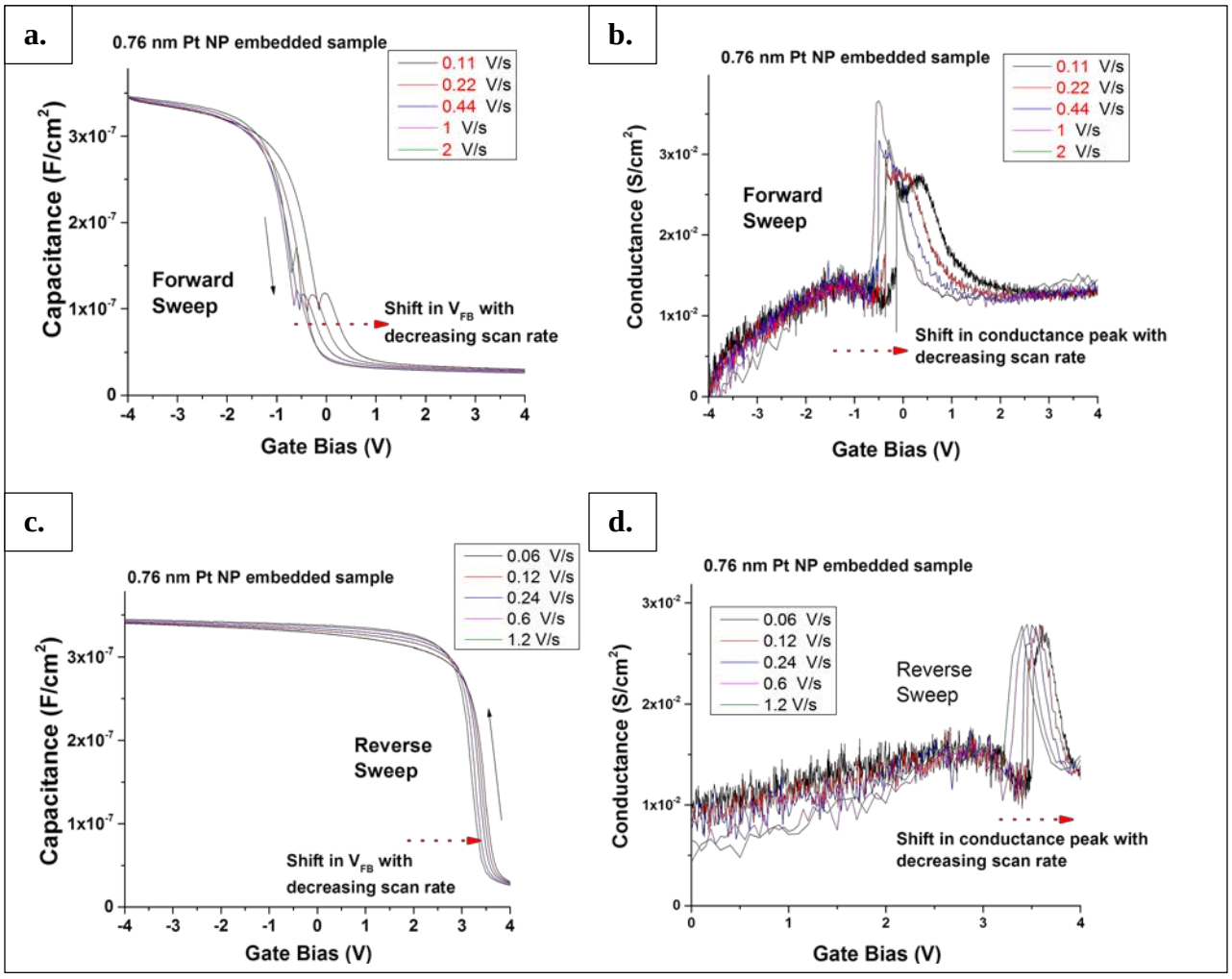


Figure 43: Scan rate dependent C-V and conductance characteristics at 1 MHz for the 0.76 nm Pt NP embedded NVM MOS capacitor for the (a), (b) forward and (c), (d) reverse sweeps respectively

Meanwhile for the reverse sweep condition, no anomalous C-V spikes were observed and while there was a small positive shift in flat-band voltage with decreasing scan rate, contrariwise to the forward sweep case, the change in the width of the associated conductance peak was insignificant. Figure 44 (a) and (b) displays the C-V and G-V characteristics of the 0.93 nm Pt NP embedded device obtained during the forward sweep whereas Figure 44 (c) and (d) displays the devices C-V and G-V characteristics in the reverse sweep. While just one anomalous C-V spike was seen in the previously discussed 0.76 nm Pt NP case, multiple anomalous spikes were observed for the 0.93

nm Pt NP case, where the number of these spikes increased with decreasing sweep rate (from 3 spikes at 0.11 V/s to 7 spikes at 2 V/s). These C-V spikes were accompanied by multiple conductance peaks where the existence between two distinct regimes of conductance peaks becomes more recognizable with decreasing scan rate. While multiple spikes/peaks could be seen in the forward sweep C-V/G-V plots, similar to the case of 0.76 nm embedded Pt NPs, no anomalous C-V spikes were observed and the change in the width of the associated conductance peak with decreasing scan rate was insignificant. The 0.73 nm Pt NP (with ~2X higher areal density) embedded sample displayed similar C-V/G-V characteristics as the 0.93 nm Pt NP embedded device, albeit the flat-band voltage is shifted to a larger gate bias (as observed previously in Figure 39). The presence of multiple C-V spikes and two distinct conductance peak regimes can be seen in the forward sweep (Figure 45 (a) and (b) respectively) accompanied by the lack of any anomalous C-V/G-V features in the reverse sweep (Figure 45 (c) and (d) respectively). The C-V/G-V characteristics obtained for all Pt NP embedded devices during the reverse sweep are indicative of their successful electron charging during the programming operation. As the p-Si surface reaches inversion, driven by the favorable energy difference, the electrons tunnel from the inversion region into the embedded Pt NPs. The stored electrons contribute towards the large positive flat band shifts observed in the reverse C-V plots. The conductance peak observed in the G-V measurements is also representative of this electron tunneling event. It's important to realize the occurrence of the narrow conductance peak observed in the reverse sweep should be associated with the ac loss due to capture and emission of electrons by the Pt NPs but not to the Si substrate/tunnel oxide interface states. The lack of stretch-out of the C-V curves (as seen for the control oxide sample with high density of interface before post metallization annealing – discussed previously in section 5.3.1) is another indication that the observed conductance peak in the reverse

sweep is due to the capture and emission of electrons by the Pt NPs. Huang et al. reported a similar phenomenon while studying NVM MOS capacitors with embedded Si nanocrystals where the origin of the observed conductance peak was associated with the ac loss due to capture and emission of electrons by the embedded Si quantum dots but not to the Si substrate/tunnel oxide interface states [214].

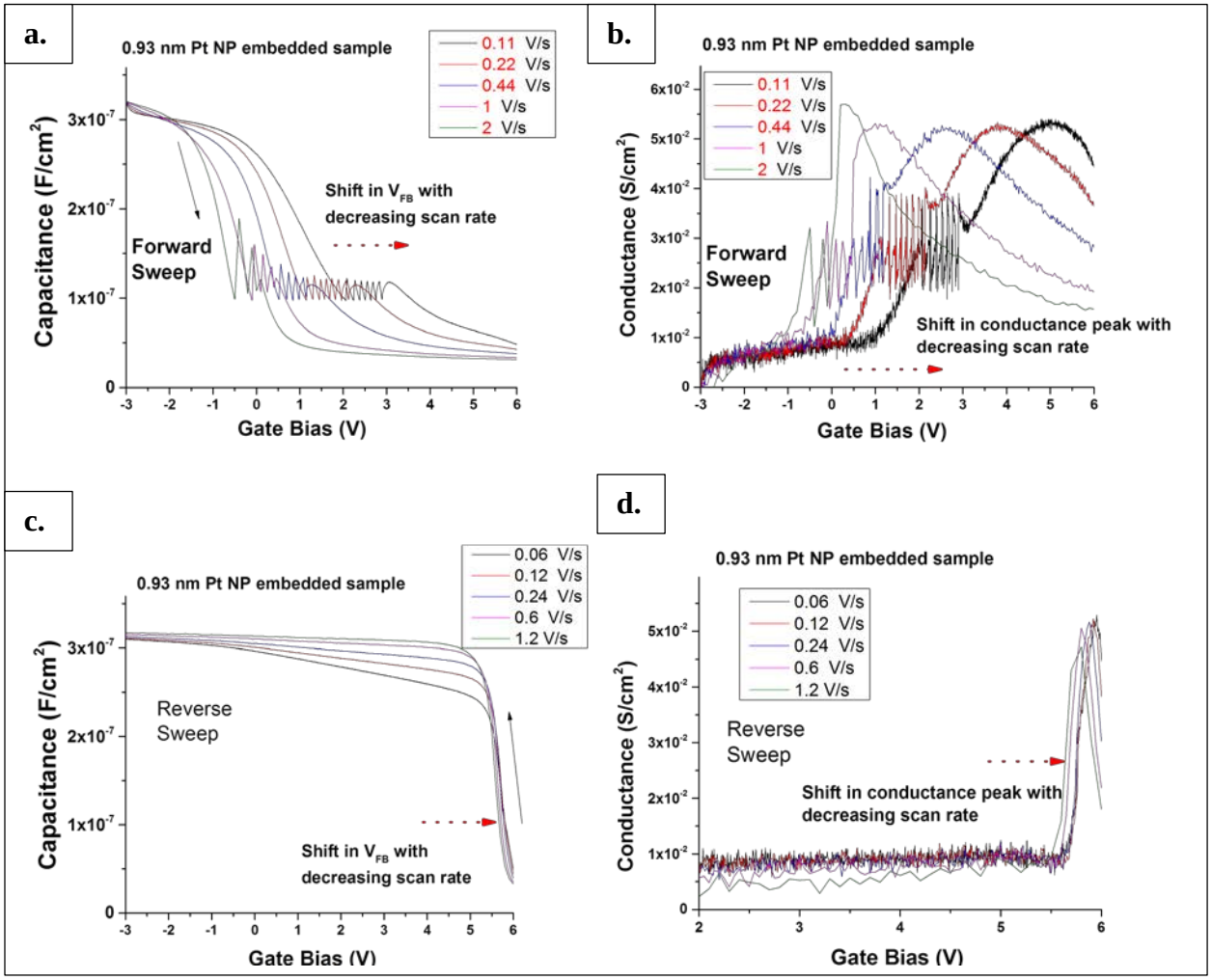


Figure 44: Scan rate dependent C-V and conductance characteristics at 1 MHz for the 0.93 nm Pt NP embedded NVM MOS capacitor for the (a), (b) forward and (c), (d) reverse sweeps

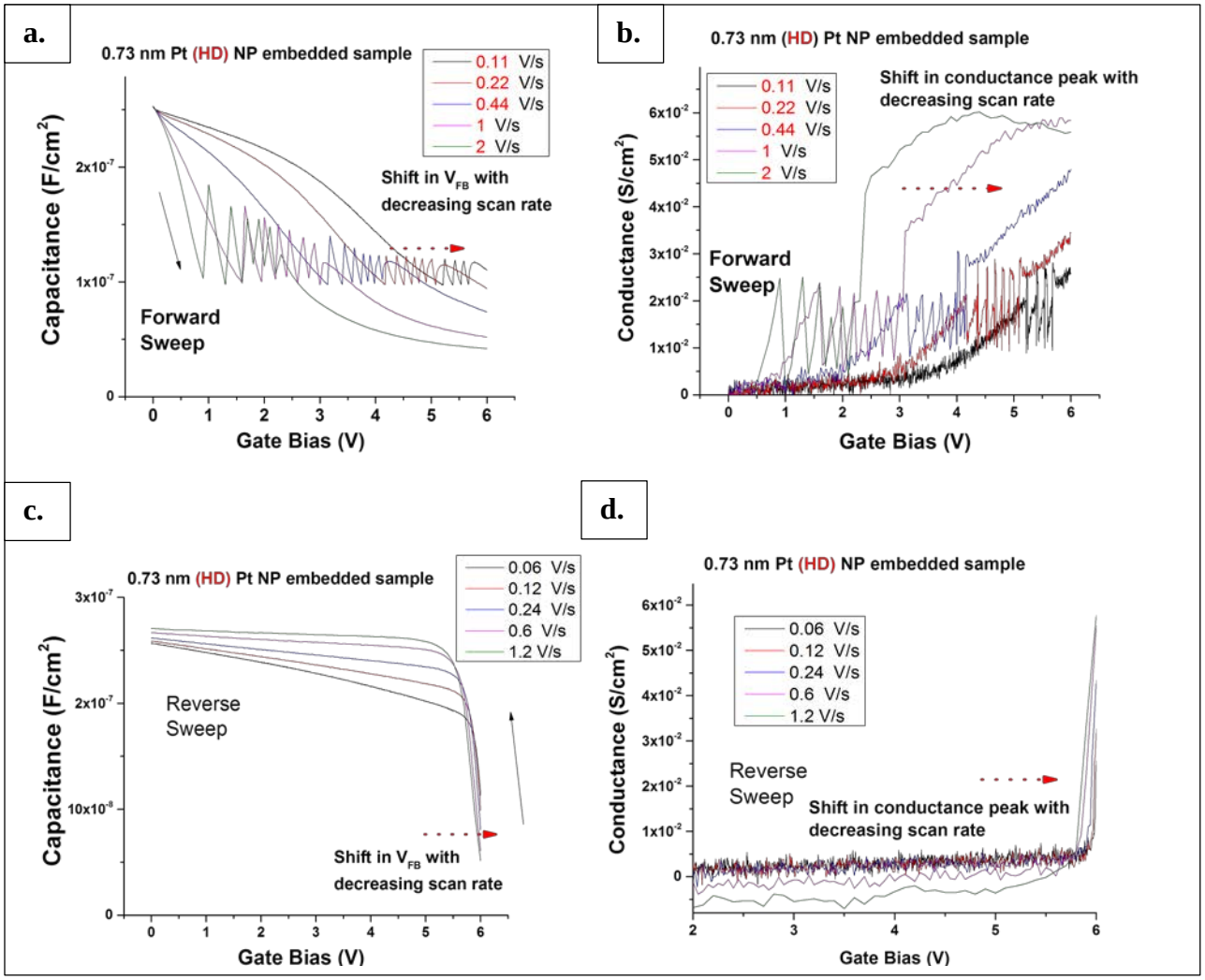


Figure 45: Scan rate dependent C-V and conductance characteristics at 1 MHz for the 0.73 nm Pt NP (with high areal density) embedded NVM MOS capacitor for the (a), (b) forward and (c), (d) reverse sweeps respectively

While the C-V characteristics and the conductance peak seen in the reverse sweep is expected and indicates good electron programming features, the origin of anamalous CV/GV features observed for all Pt NP embedded samples during the forward sweep is more complicated. The sweep rate dependent C-V spikes seen during the forward sweeps in the case of embedded 0.76 nm, 0.93 nm and 0.73 nm (HD) Pt NPs and the corresponding conductance peaks are indicative of charge transfer events with two distinct timescales. While the narrow conductance peaks associated with the C-V spikes near the flat band voltage respond to the fastest employed

sweep rate are indicative of a fast charge transfer event, the broader conductance peak and the corresponding 'hump' seen at larger gate biases are probed at lower scan rates and is indicative of a slower charge transfer event. Based on the surface potential – gate bias plot displayed in Figure 42, and their sweep rate dependent probe at larger gate biases, it can be approximated that the slower traps are located near the valence band edge of Si. Since post metallization H_2 annealing was employed for all the Pt NP embedded devices, and is shown to substantially reduce the density of traps at the Si/SiO_2 interface, the probed slower traps are not at the Si/SiO_2 interface. One might argue that the effectiveness of post metallization H_2 annealing might be reduced for these due to incorporation of Pt NPs within the dielectric (as Pt is known to strongly dissociate H_2 molecule and bind H atom – as discussed previously in chapter 4 – section 4.1) and the slow traps could be due to the unpassified Si dangling bonds at the interface. However, given the low surface coverage percentage of Pt NPs explored in this study (Table 1), it is highly unlikely the effectiveness of post metallization annealing would be substantially compromised. The fixed charge at the Al_2O_3/SiO_2 interface merely causes a V_{FB} shift (as seen in the case of the post metallization anneal control sample in

Figure 36(b)) without distorting the CV shape. This is because this defect level originates due to the *Oi* defect at the oxygen rich intitial Al_2O_3 layer on SiO_2 with its reported thermodynamic transition level at 2.77 eV above the Al_2O_3 valence band minimum [215]. This defect level is located deep witin the valence band of p-Si and hence would not result in "stretch-out" of the CV curves. above. Shin et al. report that for ALD grown amorphous Al_2O_3 thin films, the intial few layers are oxygen rich with the oxygen content decreasing with increassing film thickness [216]. In the case of Al_2O_3 films imployed in this study, Al deficiency at the $Al_2O_3/SiO2$ interface manifests itself in the form of oxygen dangling bonds and the *Oi* defect level deep inside the p-Si

valence band. Apart from the unpassivated dangling bonds at the Si/SiO_2 interface and fixed charge at the Al_2O_3/SiO_2 interface the Al_2O_3 dangling bonds (border traps) surrounding the Pt NPs could be the only other possible physical explanation for the slow traps observed during the forward sweeps. The location of these slow traps near the valence band edge of Si is another factor indicative of their origin from Al_2O_3 dangling bonds. It has been reported previously that for an inert metal (Pt in this case) with negligible chemical interaction at the interface, the density of interface states and the charge neutrality level (CNL) can be calculated directly from the dielectric band structure [179, 180]. The CNL can essentially be thought of as a local Fermi level of the Pt NP/Al_2O_3interface states. The experimentally determined CNL of ALD Al_2O_3 is known at −5.2 eV [181], which is near the valence band edge of Si. E_{CNL} denotes the local Fermi level of the Al_2O_3/Pt NP interface states. A schematic showing the Band alignment of the studied MOSCAP architecture before contact is displayed in Figure 46. Here, E_f denotes the Fermi level of p-Si, E_{In} denotes the average position of the Si/SiO_2 interface states (located at 0.3 eV above the valence band edge [217]), E_{Fix} denotes the transition level of the fixed charges at the SiO_2/Al_2O_3 interface and E_{CNL} denotes the local Fermi level of the Al_2O_3/Pt NP interface states. In order to effectively display the position of the Si/SiO_2 interface states and the Pt NP/Al_2O_3 border traps within the device structure and within the Si band-gap, the inverted device schematic of the Pt NP embedded NVM MOS capacitor structure highlighting the correlation between the position of the dangling bonds within the device to their resultant trap energy levels within the Si band gap is displayed in Figure 47.

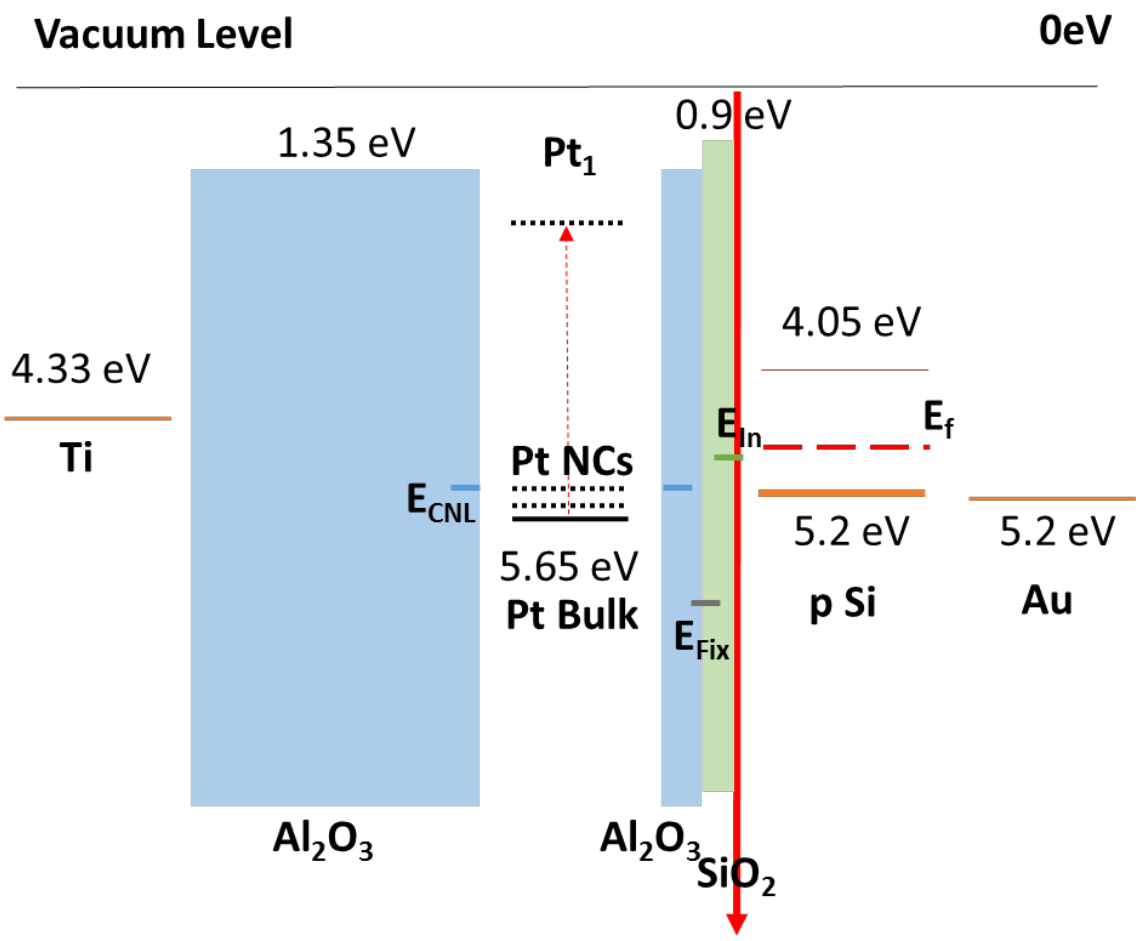


Figure 46: Band alignment of the studied MOSCAP architecture before contact. Here, E_f denotes the Fermi level of p-Si, E_{In} denotes the average position of the Si/SiO_2 interface states, E_{Fix} denotes the transition level of the fixed charges at the SiO_2/Al_2O_3 interface and E_{CNL} denotes the local Fermi level of the Al_2O_3/Pt NP interface states

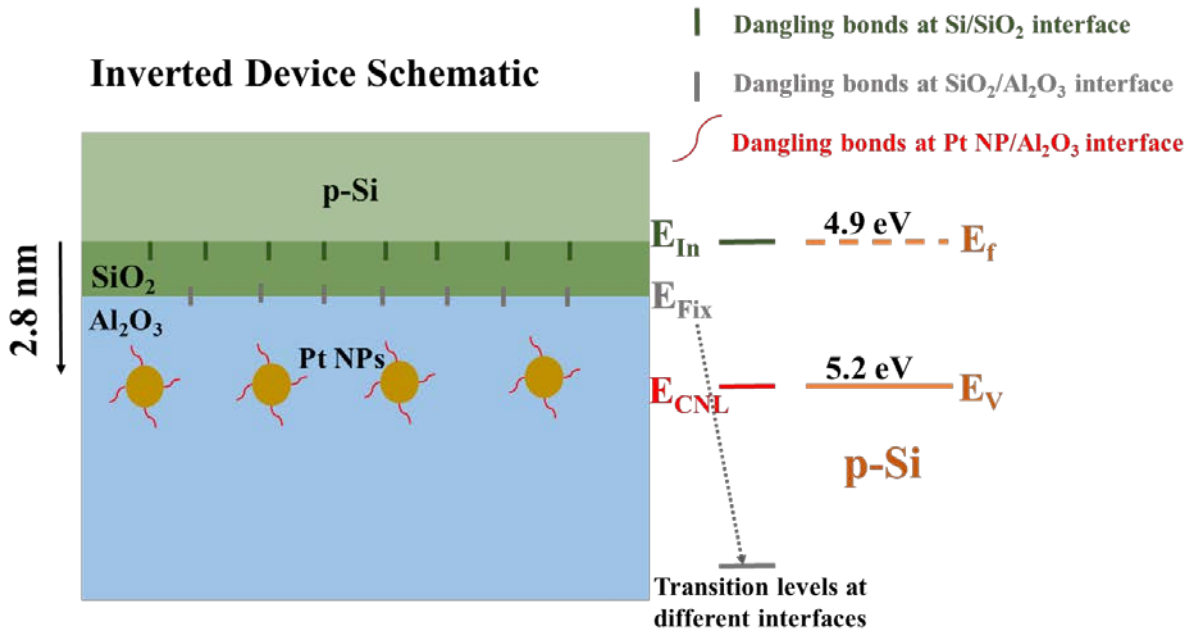


Figure 47: Inverted device schematic of the Pt NP embedded NVM MOS capacitor structure highlighting the correlation between the position of the dangling bonds within the device (present at the Si/SiO_2 and Pt/Al_2O_3 interfaces). Here, E_f denotes the Fermi level of p-Si, E_{In} denotes the average position of the Si/SiO_2 interface states, E_{Fix} denotes the transition level of the fixed charges at the SiO_2/Al_2O_3 interface and E_{CNL} denotes the local Fermi level of the Al_2O_3/Pt NP interface states

While the origin of the slower traps has been identified, to resolve the origin of the fast traps and the C-V spikes observed in the forward sweeps, the role of the aforementioned border traps located at the Pt/Al_2O_3 interface in "pinning" the embedded Pt NP layer effective work-function needs to be discussed. As mentioned previously in section 5.1, fermi-level pinning of the nanocrystal memories induced by high density of dielectric dangling bonds near the metal nanocrystal surface has been shown to complicate the expected charging/discharging characteristics [178]. Depending on the magnitude of the density of these dangling bonds at the interface, the effective metal work unction can shift towards (i.e. its fermi level is "pinned") CNL of the dielectric it is in contact with. In this study, the effective Pt NP layer work-function is pinned by the Al_2O_3 CNL near the valence band edge of Si. The degree of this fermi-level pinning would

essentially be dependent on the density of Al_2O_3 dangling bonds near the Pt NP. Conceptually, this interface trap density should be dependent on the Pt NP surface coverage, increasing in the following order – 0.76 nm Pt NP → 0.93 nm Pt NP → 0.73 nm (HD) Pt NP. This is corroborated by analyzing the frequency dispersion of the experimentally obtained C-V/G-V characteristics. The frequency dependent C-V/G-V characteristics for the 0.76 nm Pt NP, 0.93 nm Pt NP and 0.73 nm (HD) Pt NP incorporated NVM MOS capacitors are shown in Figure 48, Figure 49 and Figure 50 respectively. At a given frequency, all traps with time constants shorter than the reciprocal of the frequency respond to the measuring signal and the flatband voltage will be reached at a particular value of applied gate bias. For the forward sweep of all Pt NP incorporated devices, the slower traps at the Al_2O_3/Pt interface predictably respond at lower frequencies and by comparing the magnitude of their frequency normalized conductance peaks (G/ω), a comparative study of the density of the Al_2O_3/Pt interface states with varying Pt NP incorporation can be conducted. For example, at 20 KHz frequency, the forward sweep G/ω peak for the 0.93 nm Pt NP case is approximately 2 X in magnitude compared to the 0.76 nm Pt NP case. Similarly, at 20 KHz frequency, the forward sweep G/ω peak for the 0.73 nm (HD) Pt NP case is approximately 1.5 X in magnitude compared to the 0.76 nm Pt NP case. Based on these results, it can be surmised that the density of interface states is substantially larger for the 0.93 nm Pt NP and 0.73 nm Pt (HD) NP cases compared with the 0.76 nm Pt NP case. This corroborates well with the trend in Pt NP surface coverage and effective dielectric constant (an indication of dielectric porosity – more on which would be discussed in section 5.3.3).

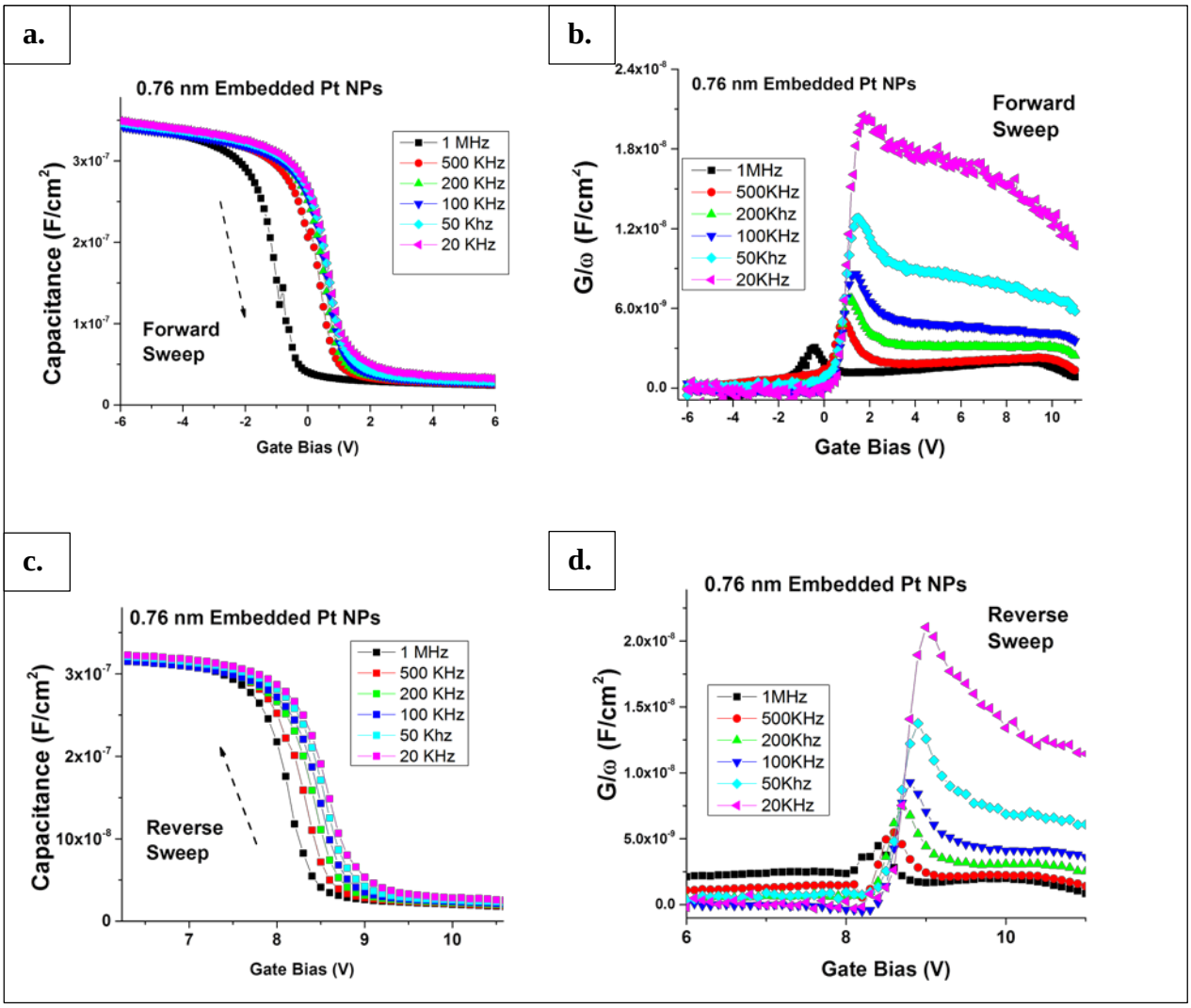


Figure 48: Frequency dependent C-V and conductance characteristics for the 0.76 nm Pt NP embedded NVM MOS capacitor for the (a), (b) forward and (c), (d) reverse sweeps respectively

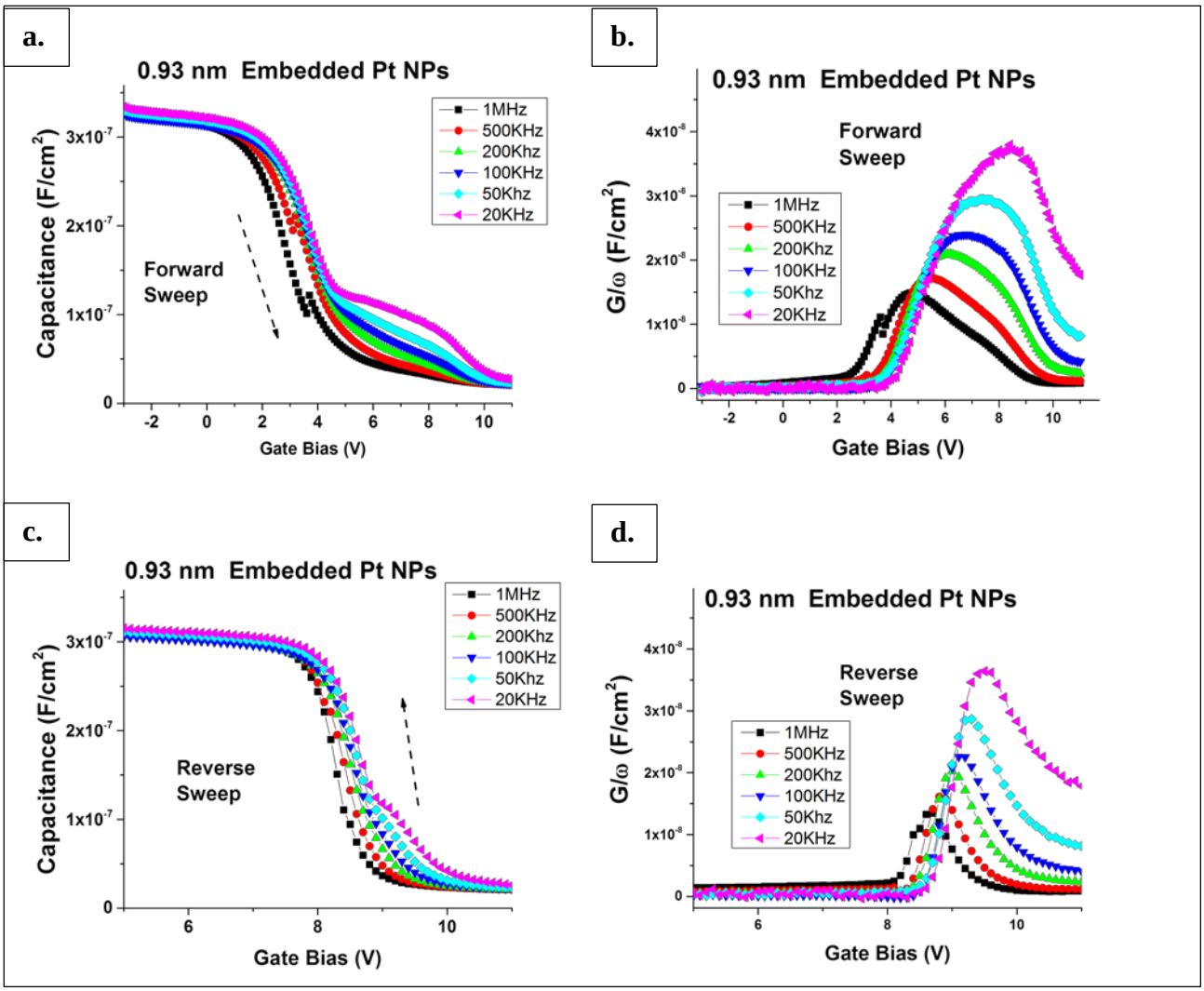


Figure 49: Frequency dependent C-V and conductance characteristics for the 0.93 nm Pt NP embedded NVM MOS capacitor for the (a), (b) forward and (c), (d) reverse sweeps respectively

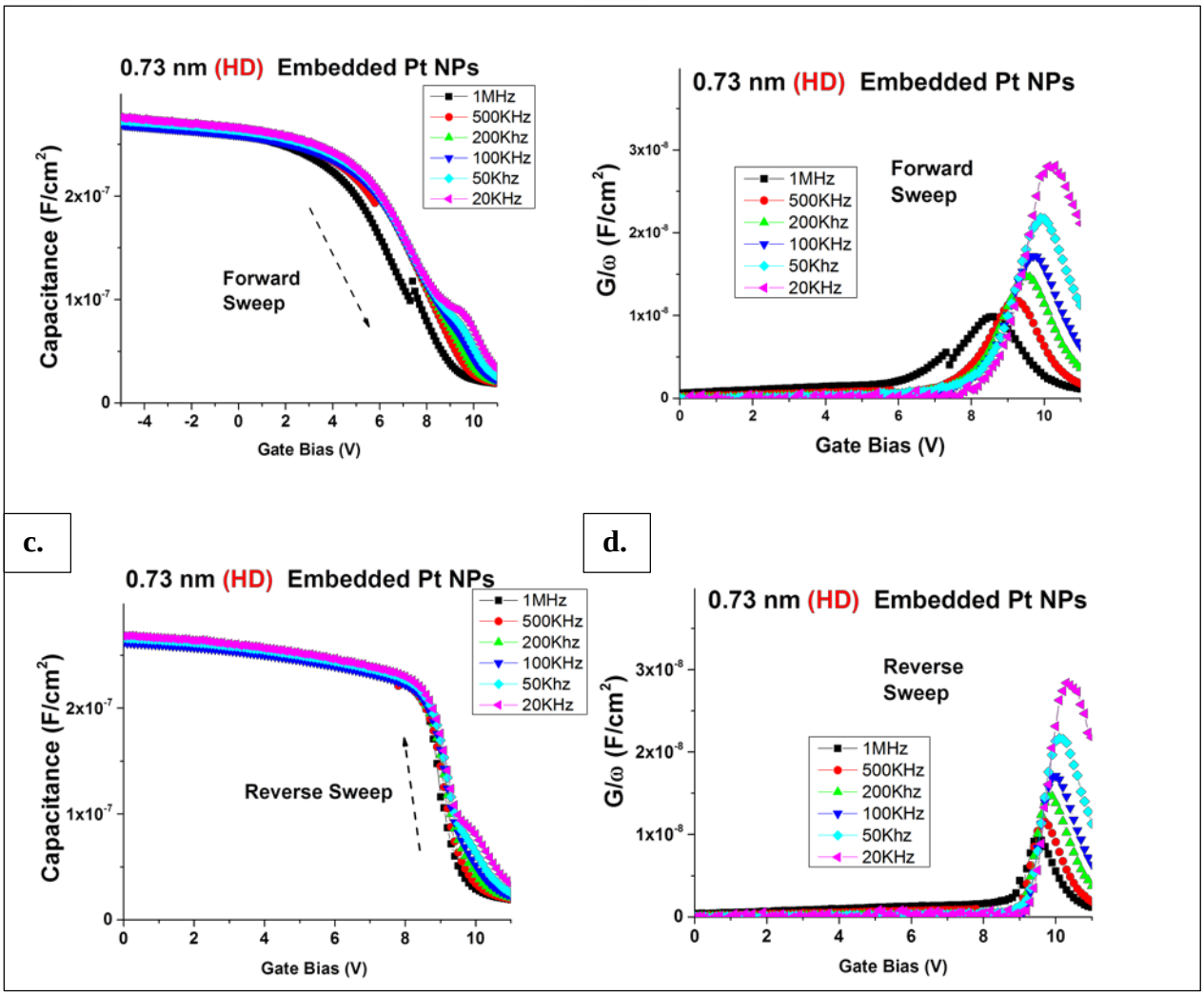


Figure 50: Frequency dependent C-V and conductance characteristics for the 0.73 nm Pt NP (high areal density) embedded NVM MOS capacitor for the (a), (b) forward and (c), (d) reverse sweeps respectively

Now that it is established that the density of traps at the Al_2O_3/Pt interface is a function of Pt surface coverage and can dictate the effective work-function of the embedded Pt NP layer, we can explain the anomalous C-V spikes seen during the forward sweeps.

Figure 51 displays the schematic band diagram explaining the origin of the C-V spikes for the device embedded with 0.93 nm Pt NPs observed during high frequency C-V forward sweeps seem before in Figure 43, Figure 44 and Figure 45. At V(1) gate bias, hole charging (can be conversely thought of as electron discharging) of the Pt NPs occurs. As the gate bias is swept in from accumulation (V(1)) towards flat band voltage (V(2)), the Si surface is depleted of holes and due to the presence of the Al_2O_3/Pt dangling bonds and their alignment with Si valence band edge the holes stored in the Pt NPs repopulate the Si surface through trap assisted tunneling. This repopoluation of holes at the Si surface is seen as a spike in capacitance value at V(3) gate bias. It is interesting to note that the 0.76 nm Pt NP embedded device shows only one capacitance spike, which might be due the lower density of dangling bonds at the Al_2O_3/Pt with the Pt effective work-function getting "de-pinned" at larger gate biases. Meanwhile, for the 0.93 nm Pt NP embedded sample, the aforementioned process of hole depletion and repopulation at the Si surface continues at V(4), V(5) and so on resulting in multiple spikes observed near the flat-band bias. Eventually, as the Pt effective work-function is "de-pinned" at larger gate biases, no more C-V spikes are observed and the device successfully goes into inversion. The 0.73 nm (HD) Pt NP embedded device also follows similar depletion → repopulation → depletion … → eventual "de-pinning" process flow with increasing gate bias, albeit the "de-pinning" occurs at a much larger gate bias and the sample never goes into inversion within the studied gate bias regime.

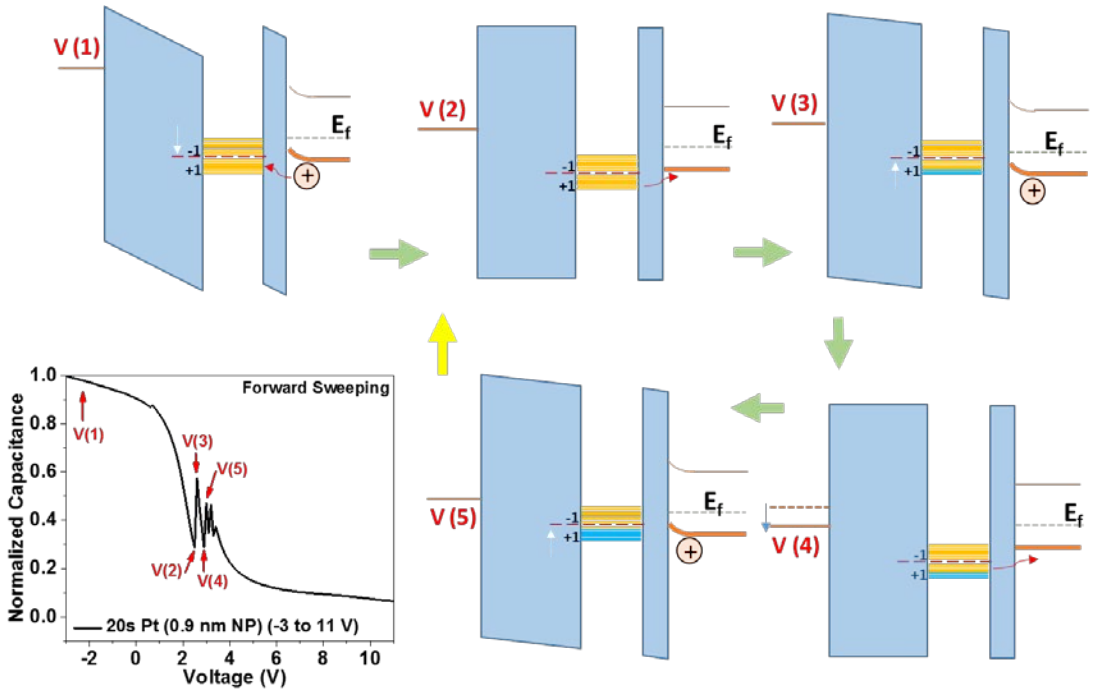


Figure 51: Schematic band diagram explaining the origin of the C-V spikes for the device embedded with 0.93 nm Pt NPs observed during high frequency C-V forward sweeps (V(1) → V(5) – accumulation to inversion).

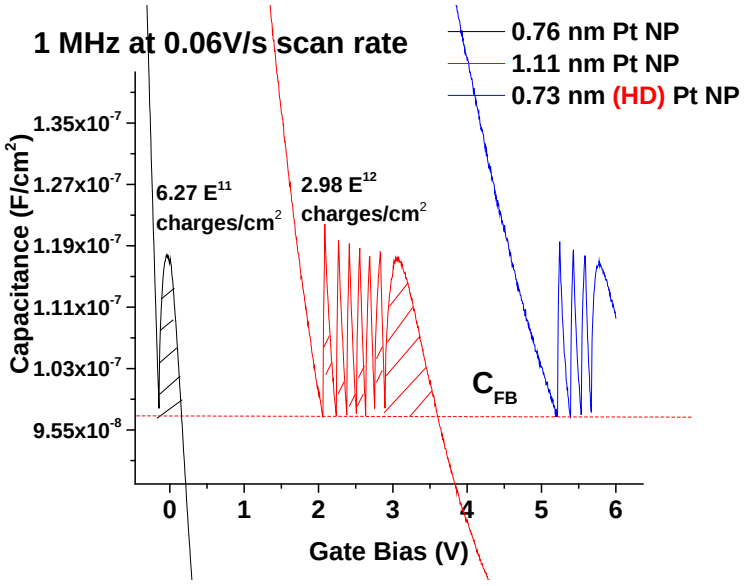


Figure 52: Forward sweep C-V plots for the Pt NP embedded MOS capacitors with calculated density of charges representing the C-V spike induced flat-band shift. The calculation could not be done for the 0.73 nm (HD) case as the device did not reach the eventual flat band value within the studied gate bias regime.

A good approximation of the net number of trapped The trap assisted tunneling discussed in this case leading to repopulation of holes on the Si surface is a fast charge transfer process and is only seen at AC probe frequencies larger than 500 KHz. Considering that at a given frequency, all traps with time constants shorter than the reciprocal of the frequency respond to the measuring signal, the timescale of this trap assisted tunneling process can be predicted to be smaller than 2 μs. Also, based on the flat-band shift encountered after the anomalous C-V spikes, the charge density (which would be a rough estimation of the density of traps at the Pt/Al_2O_3 interface) can be calculated (Table 9) and follows the aforementioned trend of increasing interface charge density with increasing Pt NP surface coverage. The slow traps at the Pt/Al_2O_3 interface also influences the low frequency CV-GV characteristics obtained during the reverse sweep for the Pt NP emebedded NVM MOS capacitors. However, due to the location of the trap energy near the valence band edge of Si and subsequent pinning of the Pt NP effective workfunction by these traps, the injected electrons are highly unlikely to tunnel back to the Si surface. Thus, unlike the forward sweep case, no anamalous C-V spikes were observed in the reverse sweeps for the studied devices. In other words, it can be stated that the Pt NP incorporated NVM MOS capacitors in this study display features indicative of favorable electron storage and poor hole storage, which results in the assymetric memory windows observed in Figure 40. The following section corroborates the aforementioned increase in thin ALD Al_2O_3 porosity with increasing Pt NP surface coverage when probed on the basis of electroehemical ion penetration signatures.

5.3.3 Ion penetration studies of Pt nanoparticle embedded Al_2O_3 thin films

The purpose of the electrochemical ion penetration analysis employed in this study was to ascertain at what thickness of the ALD deposited capping dielectric does the dielectric film become pinhole free. To check the possibility for the use of ALD–Al_2O_3 layers as a pinhole-free dielectric layer, the electron transfer rates of the electroactive species (ferrocene in this case) that undergo fast outer sphere reactions at electrodes were investigated. Typically, if a fully insulating layer exists between the electrode and the electrolyte solution, the electron-transfer rates depend on electron-tunneling across the layer. In this case, the rates significantly decrease with increasing layer thickness. However, if large pinholes exist in the ALD–Al_2O_3 layer, the redox currents of Ferrocene can be readily observed despite the thick layer [218]. Figure 53 displays the cyclic voltammetry (CV) plot of the control n++ Si substrate with ferrocene. A clear reduction peak can be seen in the anodic scan, however, the oxidation peak is not very clear in the cathodic scan as the PF^{-6} anion can show faradaic signatures at larger positive biases. The ΔE_p value, which is representative of the redox rate of the system (smaller ΔE_p values implying a faster redox rate) was fairly large for the control n++ sample (>1.4 V) and shows that bare n++ Si has a relatively low redox rate for the ferrocene system.

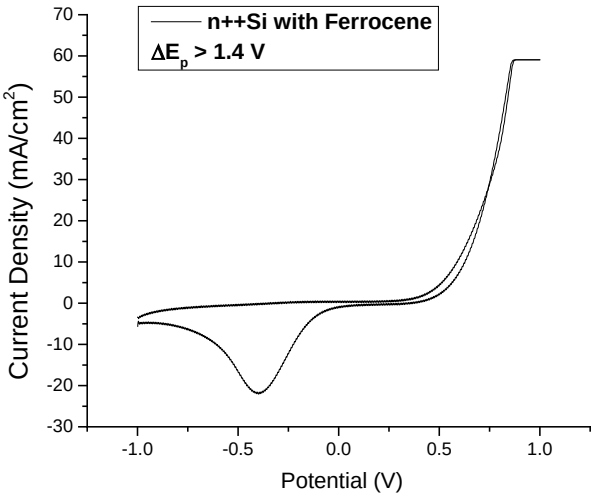


Figure 53: The CV plot of the control n++ Si substrate with ferrocene at a scan rate of 500 mV/s

Figure 54, Figure 55, Figure 56 and Figure 57 display the CV plots of the control n++ Si substrate, with subsequent thinner capping oxide alumina sample, and with the additional Pt NP (10s -0.76 nm, 20s -0.93 nm, and 45s- 1.56 nm) embedded alumina samples respectively.

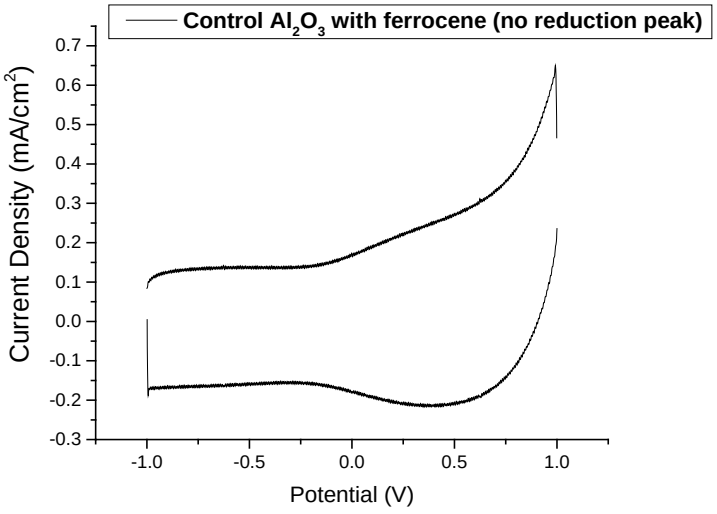


Figure 54: The CV plot of the thinner capping oxide alumina sample with ferrocene at a scan rate of 500 mV/s. Note the absence of any ferrocene indicative redox peak.

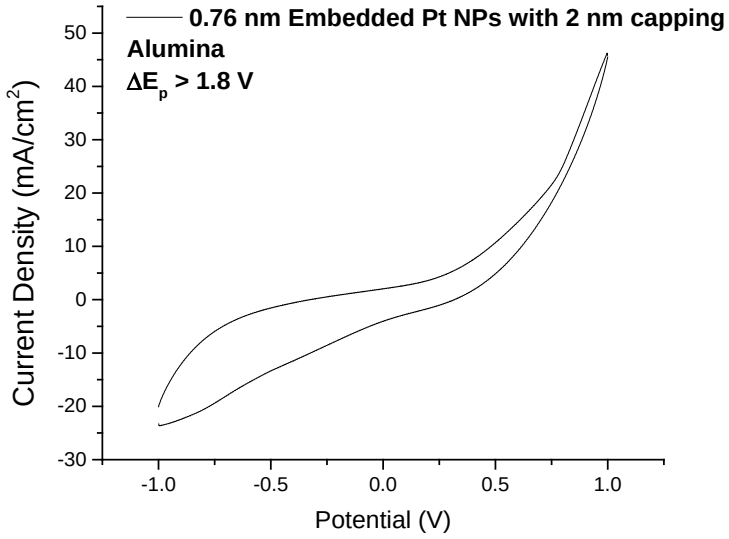


Figure 55: The CV plot of the 0.76 nm Pt NP embedded thinner capping oxide alumina sample with ferrocene at a scan rate of 500 mV/s

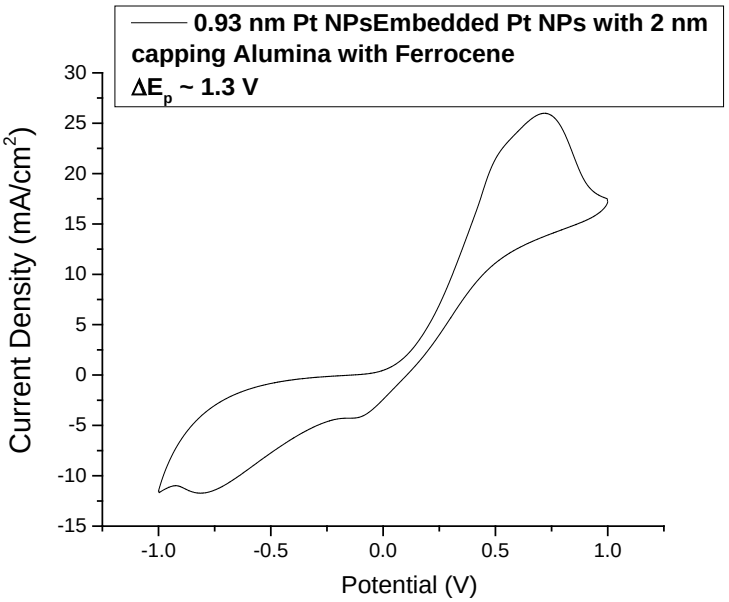


Figure 56: The CV plot of the 0.93 nm Pt NP embedded thinner capping oxide alumina sample with ferrocene at a scan rate of 500 mV/s

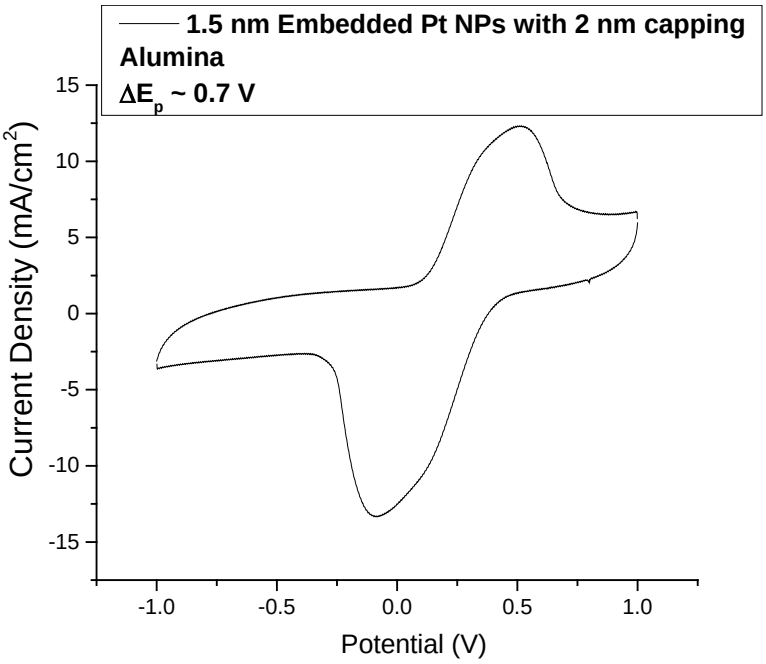


Figure 57: The CV plot of the 1.56 nm Pt NP embedded thinner capping oxide alumina sample with ferrocene at a scan rate of 500 mV/s

Table 10 lists the obtained redox peak potential separation (ΔE_p) values from the resultant CV curves. It can be seen from Figure 54 that the control dielectric film without embedded Pt NPs does not show signs of faradaic currents (indicative of ion penetration to the active surface). However, upon incorporation of Pt NPs within the dielectric, faradaic signatures were observed (Figure 55, Figure 56 and Figure 57). This is because the ultrathin tunneling oxide allows these NPs to be part of the electrochemically active surface area, i.e., ions penetrating the capping oxide and interacting with these embedded Pt NPs would show up as a faradaic signature in the CV measurements. The ΔE_p value here gives an idea about the catalytic activity of these embedded Pt NPs with the ideal ΔE_p value being 0.059 V for the ideal case. The listings in Table 10 are far larger than this theoretical value and it could be attributed to the tunneling resistance of the thin tunneling alumina layer separating the Pt NPs from the conducting n++ Si surface. These ΔE_p are quite predictable as the smaller NPs show sluggish charge transfer behavior due to strong charge storage

characteristics compared to the larger NPs, which depict a less resistive redox pathway and excellent charge transfer features.

Sample	**Pt NP percentage surface coverage (%)**	**ΔE_p (V)**
N++ Si	-	>1.4
N++ Si + Al2O3	-	- (no signatures) -
N++ Si + Al2O3 (0.76 nm Pt)	2.13	1.8
N++ Si + Al2O3 (0.93 nm Pt)	3.66	1.3
N++ Si + Al2O3 (1.56 nm Pt)	11.31	0.7

Table 10: obtained ΔE_p values from the CV curves plotted in Figure 53 – 52.

Since a capping layer of 2 nm ALD alumina, developed on the Pt NP decorated tunneling oxide, allows ferrocene ion permeation, a thicker layer (3.8 nm) was also tested using CV. Figure 58 displays the CV plots of different Pt NP embedded samples with this thicker capping oxide samples. For the thicker capping oxide, the absence of ferrocene indicative faradaic signatures indicates the lack of ion penetration to the embedded Pt NPs. Despite the lack of evidence suggesting ion penetration, a trend of increasing current density with increasing embedded Pt NP surface coverage can also be seen in Figure 58 which suggests lower tunneling resistance for the larger NP embedded dielectrics, allowing better external polarization response with increase in charge transfer efficiency of embedded Pt NPs.

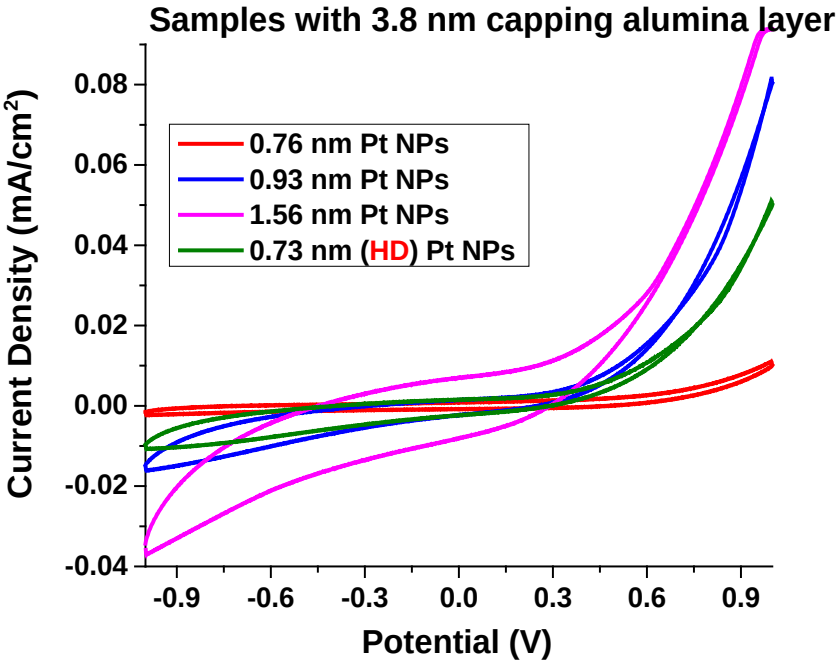


Figure 58: The CV plots of the different Pt NP embedded thicker capping oxide (3.8 nm) samples with ferrocene at a scan rate of 500 mV/s. Note the absence of the anodic peak indicative of ferrocene percolation.

This ion penetration study essentially shows that a 2 nm capping layer is insufficient in obtaining a pinhole free capping layer on top of Pt NPs. Although a 3.8 capping layer was required to obtain a pinhole free surface, the dielectric film is still likely to have a porous structure surrounding the Pt NPs.

CHAPTER 6: CONCLUSIONS

As per the scope of this dissertation, sub-2 nm Pt NPs were successfully deposited using room temperature tilted target sputtering (TTS) process on different supporting structures and their remarkable size distribution homogeneity and controllable areal density helped formulate size dependent characteristics of these Pt NPs in different electrochemical/electrical systems. The second chapter of this dissertation analyzes the stability of sub–2 nm Pt NPs immobilized on different supports (FTO and FLG) as they tend to undergo the phenomena of dissolution and coarsening that leads to loss in effective surface area, which further undermines the long-term applicability of these supported NPs. Gibbs-Thomson energy model was used to predict the stability trends and experimental verification was provided using e-beam-induced coarsening and potentiodynamic cycling in an acidic medium. E-beam-induced coarsening of Pt NPs on OTS and graphene supports was studied to understand the role of surface energy on coarsening/dissolution rate properties. Higher surface energy supports led to lower free energy of supported particles, thereby increasing NP stability. Potentiodynamic cycling in acidic solutions was utilized to study the size-dependent and support-dependent stability of these Pt NPs. Crystalline particles above a mean size of 1.5 nm diameter show exceptional stability regardless of underlying support. Meanwhile, sub-nm Pt NPs on few layer graphene (FLG) showed greater stability compared to those deposited on fluorine doped tin oxide (FTO). Pt NP dissolution and surface corrosion needs for sub-2 nm Pt NPs need to be explored in more detail and since Pt NP degradation can depend on a multitude of factors. This study shows that surface energy engineering of the support is essential toward developing stable Pt NP-based composites for durable catalysis.

The third chapter of this dissertation represents an in-depth study carried out on the triiodide reduction electrocatalytic properties of sub-2 nm Pt particles deposited by time-controlled tilted target sputtering onto FTO-coated glass with validation and exploration of these materials as prospective DSSC counter electrodes. The crystalline nature of these FTO supported Pt NPs is firmly established by HRTEM imaging. These FTO counter electrodes feature well-controlled Pt NPs deposited using TTS deposition and display high catalytic activity, comparable to that of much thicker, uniform films of Pt. In particular, using electrochemical impedance spectroscopy, the role of charge transfer resistance at the electrolyte/counter electrode interface is studied and a direct correlation between charge transfer resistance and DSSC fill factor is established. Further, cyclic voltammetry performed in a triiodide/iodide redox electrolyte confirms the higher catalytic activity of crystalline 1.56 nm particles over that of a continuous thin film. Indeed, a direct relation between NP crystallinity and enhanced catalytic activity—which yields enhanced DSSC performance—is demonstrated in this work. Pt NPs >1 nm were primarily crystalline and showed improved charge transfer characteristics compared to sub-nanometre Pt clusters and even a continuous Pt thin film. This was illustrated by increased triiodide reduction catalytic activity and diminished charge transfer resistance. This enhanced behaviour is believed to be linked to the well-defined nanocrystalline structure and fast charge transfer at the Pt NPs. Meanwhile, sputter-deposited Pt NPs sized below 1 nm in diameter behaved much more akin to classical nanoclusters and showed sluggish charge transfer characteristics exemplified by their poor triiodide reducing catalytic activities and high charge transfer resistances. This was attributed to charge trapping occurring at these sub-nanometre size particles. From an applications standpoint, efficiencies comparable to those of current DSSCs were obtained with Pt NP loadings of just 2.54×10^{-7} g cm^{-2} (obtained by sputtering at TTS configuration for 45 s in the case of this study), which happens to be

approximately 420- and 17-fold less Pt than is required to form continuous thin films of 50 nm and 2 nm thickness, respectively. So, ultimately, this study advocates that optimization of Pt by careful consideration of colloid size and crystallinity (in this case via an elegant controlled sputtering) may lead to efficient catalytic materials for innumerable reactions which result in a reduction in the total need for Pt by one or even multiple orders of magnitude.

The fourth chapter of this dissertation reports the hydrogen spillover properties of the TTS deposited sub-2 nm Pt NPs on FTO and FLG supports. Evidence of Pt NP size dependence on hydrogen spillover was observed for TTS deposited Pt NPs and a correlation between NP size, crystallinity, support characteristics, and hydrogen spillover was established. While a sharp peak in the double layer region indicative of secondary spillover was observed for 0.9 nm Pt NP-coated FTO surfaces during linear voltammetry, a subdued secondary spillover shoulder was observed for crystalline 1.5 nm Pt NP-covered FTO surfaces. Formation of C-H bonds on FLG surface due to H atom spillover from 0.9 nm Pt NPs was also confirmed using XPS. While the more efficient spillover phenomenon was attributed to a lack of crystalline structure and high surface energy of sub-nm particles, further studies need to be performed to provide more concrete evidence of this effect.

The fifth chapter of this dissertation discusses the applicability of sub-2 nm Pt NPs embedded in ALD deposited Al_2O_3 as charge storage nodes in Si based non-volatile memory devices. The role of low temperature (260^oC) post metallization H_2 annealing in significantly improving the Si/SiO_2 interface in the fabricated MOS capacitors by passivating Si dangling bonds is discussed as part of this study. The influence of Pt NP induced border traps within Al_2O_3 near the Si surface and their surface coverage dependent pinning of embedded Pt NP work function is also reported. The pinning of the nanocrystal memories induced by high density of dangling bonds

near the Pt NP surface was observed to complicate the expected charging/discharging characteristics with electron programming favored over hole programming. The degree of this pinning was probed utilizing scan-rate and frequency variant C-V and G-V measurements and was concluded to be dependent on the density of Al_2O_3 dangling bonds near the Pt NP. This density of dangling bonds acting as border traps near the Pt NP surface turns out to be a function of the Pt NP surface coverage, increasing in the following order – 0.76 nm Pt NP with 2.14% surface coverage → 0.93 nm Pt NP with 3.97% surface coverage → 0.73 nm (with ~2X areal density) Pt NP with 4.46% surface coverage. Since ALD deposited high-k dielectrics like Al_2O_3 are extensively utilized in nanocrystal embedded memory structures, and understanding of the role of the nanocrystal induced traps and their influence in determining device performance is paramount. While the best controllable charge storage characteristics were observed for 0.76 nm Pt NP embedded devices, further exhaustive charge retention studies need to be performed to accurately determine their charge retention timescales for their incorporation within commercial memory devices.

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LIST OF PUBLICATIONS

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