IMPROVED CONTACT DESIGN FOR THE SiC PHOTO-SWITCH USED IN HIGH POWER APPLICATIONS

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CHRISTOPHER MICHAEL FESSLER

Dr. William C. Nunnally, Thesis Supervisor

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Dedication

I dedicate this thesis to my brother, Justin. His work ethic and determination has been an inspiration throughout my college career.

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Abstract

Silicon Carbide (SiC) has a bulk dielectric strength of 3000 kV/cm, thermal conductivity of 4.9 W/(cm-K), and high tensile strength. It is considered the most promising photo-switching material that can enable the fielding of the most compact pulse power systems. The SiC photo-switch as an advantage over other high power switches when it is operated at a high blocking electric field. Presently, the field blocking performance of the SiC photo-switch has fallen short of the theoretical expectations. Breakdown occurs prematurely at an applied electric field of ~ 300 kV/cm not at the expected 3000 kV/cm. Breakdown is not due to the SiC bulk material but to electric field enhancement caused by the switch packaging. No packaging method exists to effectively address electric field crowding at the point where the electrode leaves the SiC bulk. At this triple point junction, the induced electric field exceeds the bulk dielectric strength of the SiC. Without an improved package, the potential of the SiC photo-switch may not be realized. Reported in this paper is a novel concept of inserting contoured electrodes into the SiC bulk to minimize field crowding in order to improve the breakdown characteristics. The concept is simulated, a fabrication process is designed, and the first steps to the fabrication process are tested.

Chapter 1: Introduction

1.1. General Description

This paper describes the research and fabrication of the improved SiC package geometry at the University of Missouri-Columbia to produce a SiC photo-conductive switch with more attractive electric field blocking capabilities. The project was sponsored by the Air Force Office of Scientific Research (AFRL) and the Lawrence Livermore National Laboratory (LLNL).

Simulations were initially performed to verify that the electric field in the existing photo-switch is enhanced by its electrode geometry. A fabrication process was then developed to produce an electrode-substrate geometry that lowers the electric field at the electrode-substrate interface. A contoured void in the photo switch substrate was produced by diamond grinding and polishing with a computer-monitored desktop mill.

The experimental results from this research and testing will be presented where the progress of the project allows for presentable results. The design steps, the simulations, and the building of the grinding system will be discussed along with suggestions for improvement. Problems will be addressed and this report will conclude with suggestions for future work.

1.2. Importance of Improving the Photo-switch Field Blocking Capabilities

The SiC photo-switch is unique in many respects and has the potential to enable the fielding of the most compact pulsed power supplies. These switches are important in applications such as photonic radar, tera-hertz RF burst generators, particle accelerators, and electromagnetic launchers. The usefulness of the SiC photo-switch is well

established and the demand for one that can operate near the theoretical limits of SiC is immense. In recent years, however, the interest in fabricating the SiC photo-switch has diminished due to its poor field blocking performance during testing. Theoretically, the large band gap of SiC (3eV) allows a bulk breakdown strength on the order of 3MV/cm. Realistically, the photo-switch has failed prematurely with a pulsed applied field of only 300KV/cm. The discrepancy requires the photo-switch to be 10 times thicker than theoretically necessary to block an electric field. Thus, the overall volume of the system must be increased and compactness is lost. An increase in system inductance accompanies the increase in switch thickness which introduces longer switching rise times. If a power system is to deliver a square pulse, for example, an increase in rise time lowers the system's efficiency. Furthermore, a reduction in compactness reduces the fieldablity of the system. The many positive aspects of using SiC photo-switches, such as sub-nanosecond rise times, long operational lifetimes, isolated triggering, thermal resilience, large dark resistivities, and low optical power requirements, are overshadowed by premature bulk breakdown.

Premature breakdown in general has plagued switches since the beginning of high voltage pulsed power research. The question of how best to improve the electric field blocking capabilities of any switch is without a definite answer. One must first determine the dominating breakdown mechanisms and then find the point where the mechanisms initiate. The two main breakdown mechanisms in the photo-switch are surface flashover and bulk breakdown. Both mechanisms are found to initiate at the triple-point junction in the photo-switch. The triple-point junction is the location of the interface of three materials with different permittivities. In the photo-switch the three materials consist of

the bulk, electrode, and insulating material. Trouble arises at the triple-point due to its tendency to make an applied electric field non-uniform. Abrupt material changes and permittivity mismatch can accumulate charge at the triple-point in ways that result in the crowding of electric field lines. The crowding process is known as the *field enhancement effect*. A non-linear voltage gradient is established throughout the bulk. The induced field at the triple-point can become much higher than the applied electric field. The result is switch breakdown that occurs prematurely; in other words, breakdown happens at a much lower applied electric field than the bulk dielectric strength.

Improving the premature breakdown condition will revive the attractiveness of the SiC photo-switch. The many benefits of using the SiC photo-switch would resonate throughout the pulse power community. The most popular pulse power switches to date are gas discharge devices such as spark gaps and thyratrons. The negative aspects of the gas discharge devices, however, hinder the community's progression to more compact and efficient pulse generation. Not only are gas discharge devices relatively large, but they also experience undesirable jitter, limited power handling capabilities, frequent maintenance, and longer rise times as compared to the SiC photo-switch. The photo-switch operating in linear mode surpasses traditional pulse power switches. The SiC photo-switch touts operation with picosecond jitter, a closure time base solely on the speed at which a light source can deliver the closure energy, higher current densities, controllable conduction times via dopant concentrations, simultaneous parallel closure of large switching arrays, compactness, robustness and low loss conduction. Furthermore, the SiC photo-switch can yield high field blocking capabilities following the improvement of premature breakdown.

1.3. **State of the Art: Previous Photo-switch Work**

The performance of linear Si, GaAs, and 6H-SiC for use as photoconductive semiconductor switch (PCSS) materials has been studied. The physical height of the switch is determined by the dielectric strength of the material,

$$\text{Equation 1.1} \qquad h_s = \frac{V_b}{E_{op}}$$

where h_s is the height of the switch, V_b is the switch blocking voltage, and E_{op} is operating electric field through the bulk [1]. E_{op} values for Si, GaAs, and 6H-SiC obtained experimentally are 90kV/cm, 140kV/cm, 300kV/cm, respectively [2; 3; 4]. The values of E_{op} are much lower than the critical breakdown strength E_{cr} given in Table 2.1 due to the non-uniform electric field at the switch contacts, surface defects, electrode quality, etc.

The semiconductor-wavelength pair determines the optical absorption depth d_o illustrated in Figure 2.1 and graphed versus wavelength in Figure 1.1.

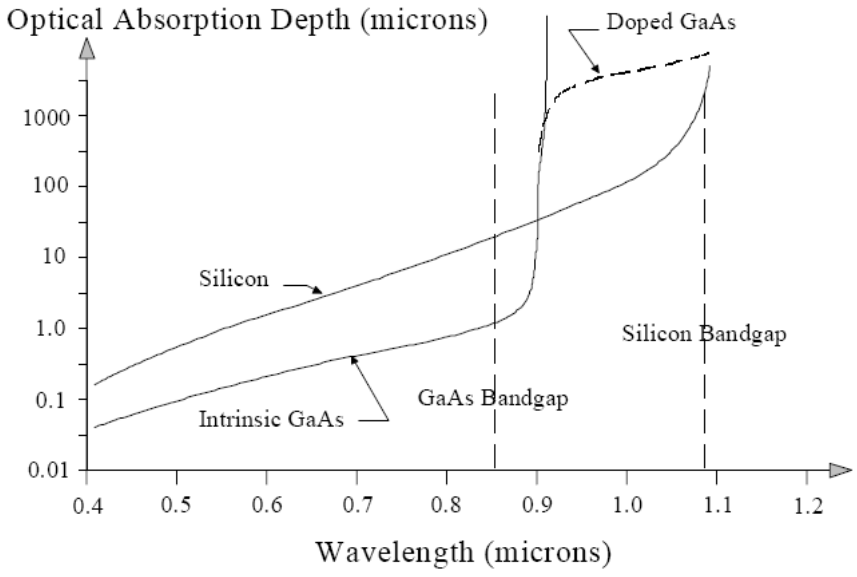


Figure 1.1 Optical absorption depth d_o versus wavelength λ

The wavelength limits for Si and GaAs and the corresponding bandgaps are given in Table 1.1. Previous work on the optical absorption measurement on 6H SiC was examined and few citations were found; thus, a small code was developed at UMC to measure the optical absorption depth in their specific material composition [5]. It was determined that for extrinsic Vanadium-doped 6H-SiC with a maximum allowable trap density of $3x10^{17}/cm^3$, the required energy to ionize all trapped carriers was $5x10^{-4}$ J. The optical absorption depth was 1.2 cm (Figure 1.2). For optimum use of the optical energy, the switch depth d_s should be 4-5 times d_o.

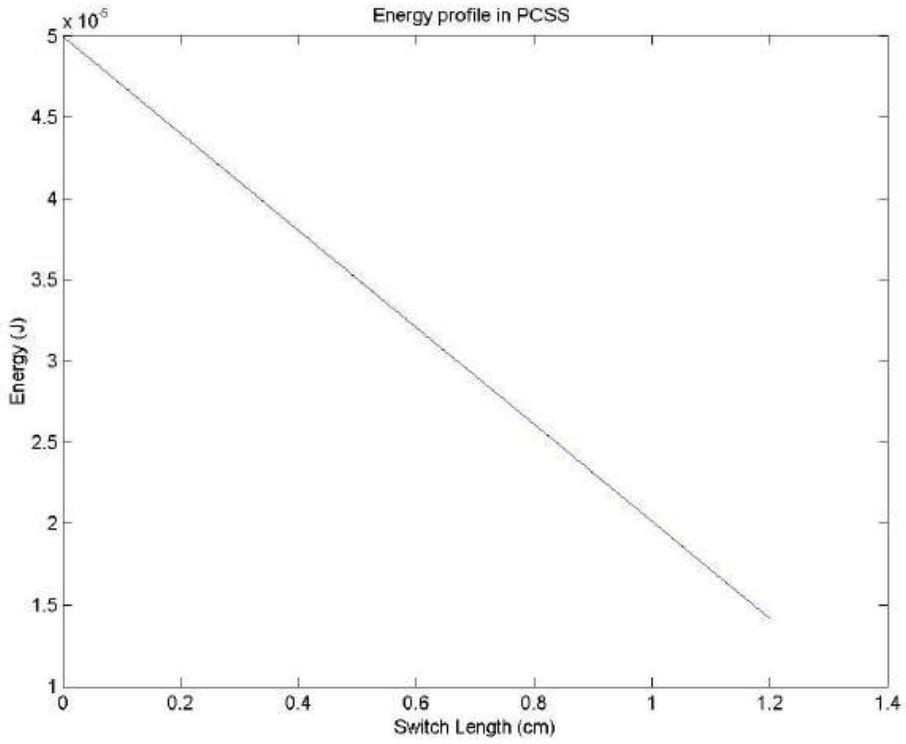


Figure 1.2 UMC absorption depth simulations for 6H V:SiC

Table 1.1 The wavelength limits for Si and GaAs

Material (linear)	Wavelength Limit (μm)	Bandgap (eV)	d_o below bandgap ()	d_o above bandgap
Silicon		1.12		
Intrinsic	1.09		≤1000 μm	a few centimeters
Extrinsic	1.09		≤1000 μm	a few centimeters
GaAs		~1.42		
Intrinsic	0.89		≤1.0 μm	a few centimeters
Extrinsic	0.89		≤1.0 μm	a few millimeters

Several research facilities gathered other photoconductive semiconductor switch (PCSS) information such as Los Alamos Laboratory, UMC, and Sandia Laboratory. The information can be summarized in bulleted points:

- The conducting switch resistance is generally 5-10% of the total circuit resistance to reduce the total optical energy required by a factor of 5 to 10 [6].
- The maximum practical carrier density in Si is ~$5x10^{7}cm^{-3}$ due to thermal runaway, Auger processes, etc. [7].
- A 4 kV/cm conduction field for Si gives a maximum current density of $50kA/cm^2$ [5].
- For GaAs with carrier density similar to Si, the maximum current density is $500kA/cm^2$ [5].
- Based on intrinsic optical absorption, a practical field for Si is 5kA/cm [5].
- Based on intrinsic optical absorption, a practical field for GaAs is 500kA/cm [5].
- Based on intrinsic optical absorption, a practical carrier density for GaAs is ~$10^{16}/cm^3$ [5].

- Based on dopants, recombination time for Si is 100ns to few milliseconds [5].
- Based on dopants, recombination time for GaAs is tens of picoseconds to few milliseconds [5].
- GaAs with bulk resistivity of ~10^7Ω-cm sustains voltage longer than Si with a bulk resistivity of ~10^4 Ω-cm due to off-state power dissipation during charging [5].
- For linear PCSSs, as operational voltage increases, charge time decreases [7].

The University of New Mexico (UNM) discovered a way to improve the voltage performance of their GaAs PCSS shown in Figure 1.3. The material used prematurely broke down at 34kV due to trap filling at the cathode and the inhomogeneous nature of its conduction mechanism [8]. By introducing an n^+ layer at the cathode, they were able operate beyond 34kV (Figure 1.4). The suppression was due to shifting the high field region from the contact to the diffused n^+ layer and blocking electron injection with the resultant p-n depletion region [9; 10].

The University of Missouri has provided rationale for SiC PCSS research, a unique geometry for PCSS, along with a p^+ layer method to improve premature breakdown [5]. The UMC switch geometry is shown in Figure 1.5. The radius of electrode curvature is 1mm. The electrode contact area is circular and measures 0.5cm ^{2}.

The ohmic contact consists of $NiSi_2$/Ti/Pt/Au/Cu layers with respective thicknesses of 200/200/100/100/500 nm. The contacts have a resistivity of 10^{-5} Ω-cm.

The bulk material is of slightly n-type doping. In addition, the switch package has been analyzed and improved [11]. A high permittivity material was used to encapsulate the bulk material to reduce the fringing surface field and theoretically improve package-related, premature breakdown.

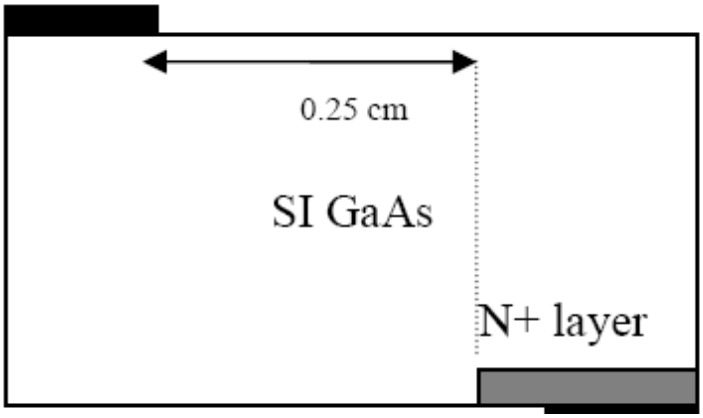


Figure 1.3 SI GaAs with n+ layer at cathode.

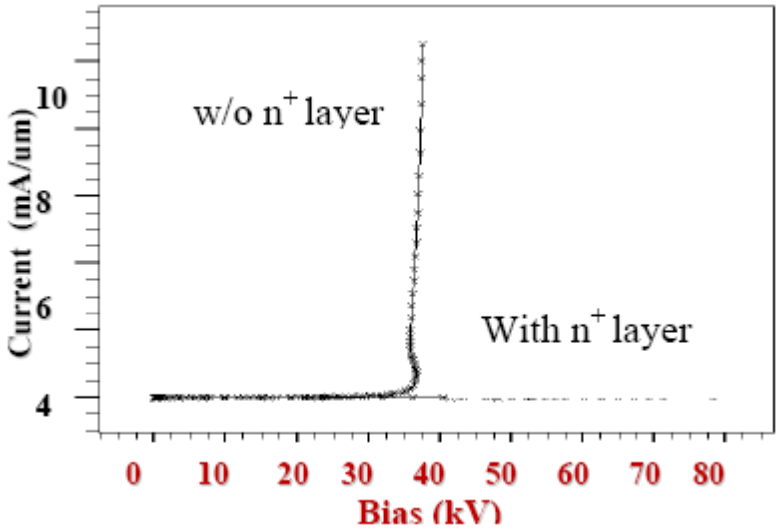


Figure 1.4 IV characteristics with and without the n^+ layer at the cathode

The performance gains from the use of high permitivitty as an encapsulant could not be achieve. Premature breakdown occured at a mean applied electric field of

~300kV/cm, not the projected dielectric strength of 3MV/cm. The premature breakdown results from several problems discovered in continued work [4]:

1) Faulty alignment of the Ohmic contact or the electrode on the opposing sides of the SiC substrate
2) Incomplete encapsulation with the insulating material in the high field region; the point where the high permitivitty encapsulant, SiC, and electrode meet (Figure 2.14).
3) Ragged solder protrusions at the bonding site in the high electric field region
4) Incomplete bonding at the surface interface that results in field enhancement points

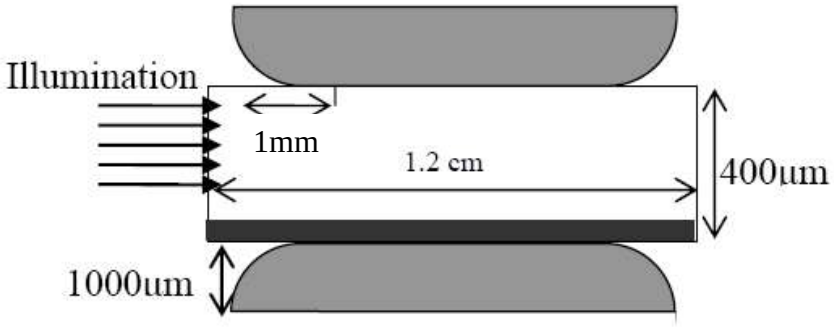
A more viable method to improve breakdown characteristics is to use UMC's p^+ layer [12]. The added p^+ layer is signified by the black line in Figure 1.5 (a). The p^+ layer was deposited at the cathode using ion implantation. The layer is 10μm thickness with a hole concentration of 10^{18} cm^{-1}. The physical mechanism for high bias operation is different for the SiC PCSS than that of UNM's GaAs PCSS. In the SiC PCSS, the interactions of the p-region and n-type bulk result in electron diffusion towards the p^+-region. The positively charged ionized donors in the bulk oppose the anode field, which results in a lowering of the bulk field (Figure 1.6). The linear switching effectiveness is also improved by minimizing surface flashover, filamentary conduction, premature bulk breakdown, and other factors. [12].

1.4. **Limitations of Previous Work**

Most photoconductive pulsed power research at Sandia Laboratories is focused on semi-insulating GaAs as the bulk material. GaAs is preferred over Si due to its

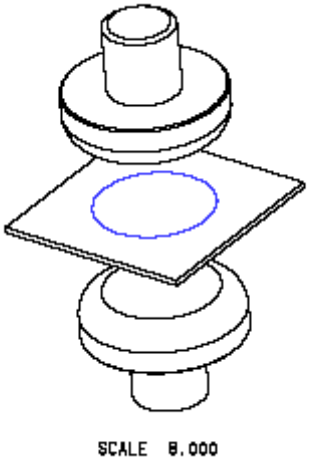
availability, high-gain operation, high electron mobility, and large dark resistivity. In 2000, research at Sandia Laboratories had produced lateral SI-GaAs PCSSs that could withstand over 100 million pulses at ~20A per filament using doped contacts. At 80A per filament, 2 million pulses were achieved without detectable contact damage. A maximum of ~80A per filament was obtained before damage was discovered on the metal portion of the contacts [13]. Today, Sandia is achieving switch lifetimes of 10^8 shots, each 5ns long with 20A per filament—20A being the benchmark for the past 20 years of data accumulation. Rise times of the switches are 350 ps with 100 ps r-m-s jitter. Voltage also affects the lifetime of the switches as the surface breakdown limit of 100kV/cm is approached [14].

The 80A filamentary current capability limits the use of lateral SI-GaAs PCSSs in high power applications. Parallel switching is used to increase current delivery, at the cost of compactness. Firing set applications, for example, require currents from 80 to 3kA for durations of 100s of nanoseconds. At high current levels, doped contacts are no longer effective and light diffusion techniques must be used to reduce contact damage. At the 3kA level, lifetime is reduced to ~20 shots [14].



a

b



c

Figure 1.5 UMC switch geometry (a), prototype switch (b) [5] and AutoCAD isometric view (c).

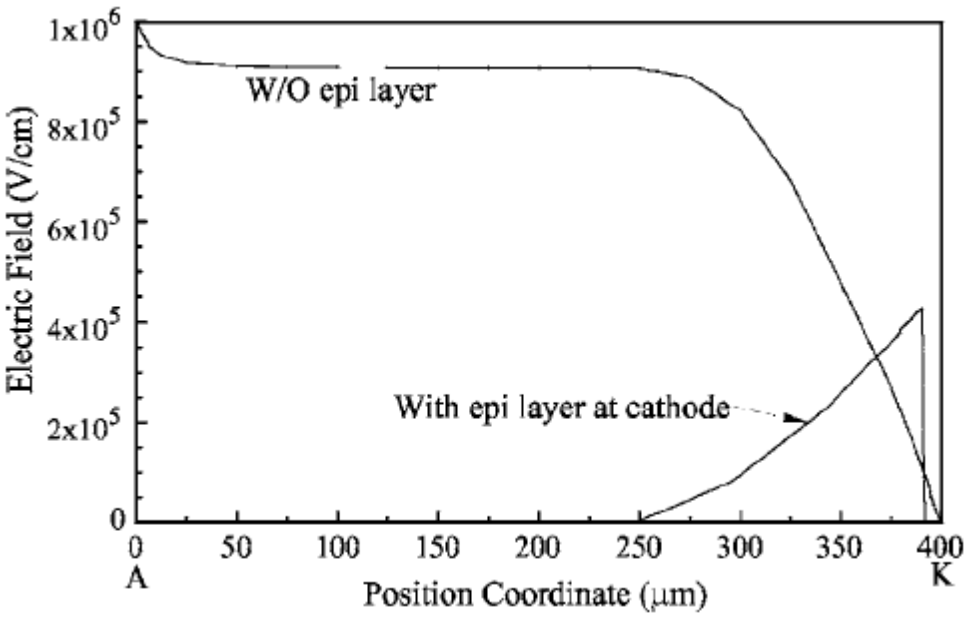


Figure 1.6 A plot of electric field across the PCSS from anode to cathode with and without the p^+ layer as the cathode.

1.5. **Chapter Summaries**

Chapter 2 discusses important concepts and principles needed to understand the field enhancement effect at a triple point. An overview of photoconductive switching is given and existing photo-switch packaging techniques are summarized. Abrasive machining is discussed and valuable insight on an approach to ceramic grinding is also discussed. This chapter also identifies literature relevant to the research presented in this report. The chapter summarizes for the reader past research that helps identify the problem to be examined and the basis for its solution. A brief description and reference is given for the articles found to be most beneficial. The chapter concludes with a statement of the problem to be addressed and a discussion of the rationale for developing SiC as opposed to GaAs for use in photo-switches.

Chapter 3 discusses how the problem is approached with five stages. It presents the methods that were used to analyze the experimental results in each stage. The chapter concludes by defining goals of the overall research initiative and what to expect while striving for the goals.

Chapter 4 discusses the simulations and construction performed in each of the five stages that were used to address the problem. The results from the stages are given. This chapter details the ElecNet simulations performed to aid in design of a novel photo-switch package. Outsourced material removal methods such as lasering and fluid jet etching are also reported. This chapter outlines a procedure that may be used to fabricate the photo-switch package. It also discusses the grinding system designed to grind a contoured void in the SiC substrate as part of the photo-switch package. The custom diamond tooling and data acquisition system are described in detail. The calibration of the grinding system and data acquisition is discussed as well. Instructions on how to operate the grinding system ends the chapter.

Chapter 5 presents the results from experimental grinds. Microscopy examinations of ground and polished SiC substrates are presented. The grinding system required improvements to yield more conclusive data; therefore, the shortcomings of the system and the improvements made are discussed. New grinding results are produced by the improved grinding systems and are reported and analyzed to conclude the chapter.

Chapter 6 provides a summary of this project and outlines the issues and problems which can be addressed in future work.

Summary of Objectives

Three main objectives will be pursued in this research. All objectives will be steps toward improving the UMC SiC PCSS package, specifically its premature breakdown tendency. The SiC PCSS analysis performed by Lawrence Livermore National Laboratories (LLNL) will serve as the building block for this research [4].

The first objective is to take the analysis performed by LLNL a step further. The electrode contact geometry must be examined to determine its contribution to premature bulk breakdown. If the geometry is found to be a significant proponent of the premature breakdown mechanism, there is justification to redesign the PCSS package. Simulations will be performed using existing PCSS dimensions to study the electric field behavior in the PCSS package under an externally applied field.

The second objective is to design an optimal package geometry that minimizes local electric fields. Parameterization simulations will be executed on various geometries to determine the optimal electrode design to implement. The optimal design must not only pacify the field enhancement in the PCSS package significantly, but also be practical to implement. It should also solve the four fabrication problems found in the existing PCSS package in previous work [4].

The third objective is to propose a package fabrication process, to compile the necessary resources needed, and to begin fabrication. This may include outsourcing the fabrication process or building a production machine from the ground up. Proving that the package design is possible to produce is paramount.

Results of the Study

This work has resulted in the design of a novel package geometry for the SiC PCSS. It also produced a fabrication process to produce the geometry. ElecNet simulations showed that inserting the PCSS electrodes with a contour of 100μm or greater into the SiC substrate lowered field enhancement by one order of magnitude. The initial stages of the fabrication process were performed. A grinding machine and diamond tools were designed and constructed to produce the contour. The contoured void was produced by a vertical spindle, eccentric grinding configuration with simple machinery. The best contoured void produced had a radius of 177μm and a depth of 119μm with a roughness projected to be on the sub-micrometer scale. A custom polishing tool was also created out of tin that can prepare the contour surface for the deposition of ohmic contacts.

The grinding system was further improved in such a way that the SiC substrate may be removed, analyzed, and returned for further grinding and polishing without the loss of workpiece and tool positioning. The use of 10μm diamond grit sizes showed the best grinding performance if the sharpness of the tool can be preserved. Analysis was based on SEM images and depth measurements. The use of a 3D optical profiler is suggested for making quantitative comparisons of future SiC substrate grinds. The contour grinding system designed and constructed can produce a SiC PCSS package geometry that is ready for contact deposition and pulse testing.

Chapter 2: Background

2.1. **Photoconductive Switch Theory**

Understanding the operation, composition, and improvement to the SiC PCSS gives insight on its shortcomings. This insight is needed to develop ways to further enhance its performance. Researching the competing PCSS technology, such as the GaAs PCSS, can also uncover ways to improve the SiC PCSS.

Photo-switching

Thermally excited electrons and holes, in a semiconductor experiencing an applied electric field, move to the conduction band and valence band, respectively. The electrons and holes are carriers and provide conduction in the semiconductor. The carriers may also be excited into their respective bands by absorbing photon energy. In this case, the electron flow in the applied field is known as *photoconduction*. The process of *photoconductivity* is defined as the generation of electron and hole carriers by the injection of photons into a semiconductor bulk. The semiconductor may then be referred to as a *photoconductor* [15].

The basic PCSS is shown in Figure 2.1. The bulk photoconductor is sandwiched between two ohmic contacts having height h_s, thickness d_s, and width w_s. The height h_s of the switch is determined by the level of electric field blocking performance desired and is a function of the dielectric strength of the bulk material. The width w_s of the switch is determined by the desired current density during the on-state and should be chosen such that filamentary conduction is avoided. The thickness d_s should be 4-5 times the optical

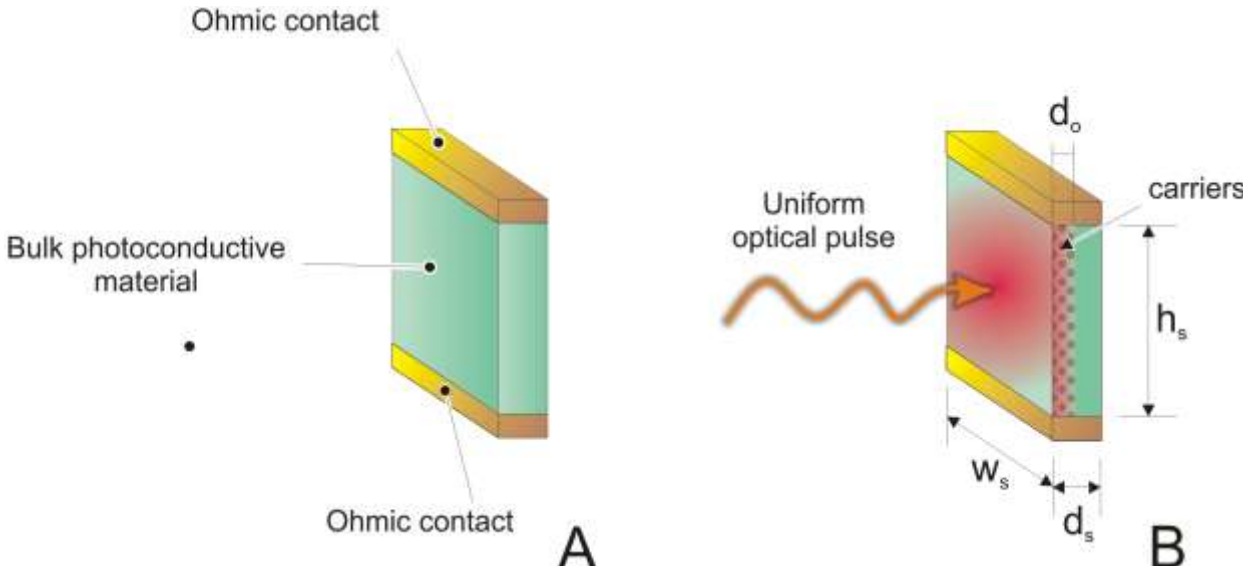


Figure 2.1 Illustration of basic PCSS, A: Unilluminated PCSS, B: Illuminated PCSS

absorption depth d_o for optimal use of the input photons and uniform carrier generation. The electrical skin depth should be equal to the optical absorption depth. The face of the bulk photoconductor is illuminated uniformly with photon energy [7; 3].

One application of the photoconductor is optical switching, or *photo-switching*. Switching, in general, is a means of changing a region of space from an insulator to a conductor. Examples of other high power switches are gas switches, bipolar transistor switches, and field-effect switches. In a gas switch, gas atoms are ionized to create electrons and ions. In a bipolar-transistor switch, electrons or holes are injected from the base to the collector through a depleted region. In a field-effect switch, a conduction channel is formed by the induction of electrons and holes. A photo-switch, commonly referred to as a PCSS, is a bulk insulator when unilluminated, due to the lack of free carriers. This open-switch state is known as the *off-state*. The closed-switch state, or *on-*

state, is when the PCSS is conducting. The on-state occurs during illumination and even following illumination depending on carrier lifetimes and avalanche processes.

Switching Modes

The PCSS has been produced in four traditional geometries [11]. All geometries have a unique aspect of operation. Figure 2.2 A, B, and C shows the lateral geometry PCSSs. In the lateral geometry, illumination direction is normal to the direction of the electric field. The optical energy is fully absorbed within hundreds of micrometers beneath the bulk surface. Linear mode switches in the lateral geometry shown in Figure 2.2 A and B immediately reach full conductivity when illumination is uniform; therefore rise time depends solely on the photon source. Surface flashover is a major concern for switches in Figure 2.2 A and B since maximum electric field is close to the surface. It is also a concern for switch C, however to a lesser degree since the electric field transverses the volume of the bulk material. Therefore, switch C has a slightly slower rise time accompanying the higher field blocking capability. Figure 2.2 D is a vertical geometry PCSS. In the vertical geometry, the illumination direction is parallel to the direction of the electric field. The vertical geometry improves electric field blocking capability by reducing the field near the surface contacts by utilizing the bulk thickness and lengthening the surface flashover path between contacts. Uniform illumination on the vertical geometry is directed through a transparent contact or contact void designated by the trigger port in Figure 2.2 D. Although the illumination is uniform, the carrier density in the conduction path is not since most carrier generation occurs near one contact. An immediate displacement current results which introduces an increase in rise time as the

carriers must propagate through the bulk to the opposing contact to establish an on-state conduction path [5].

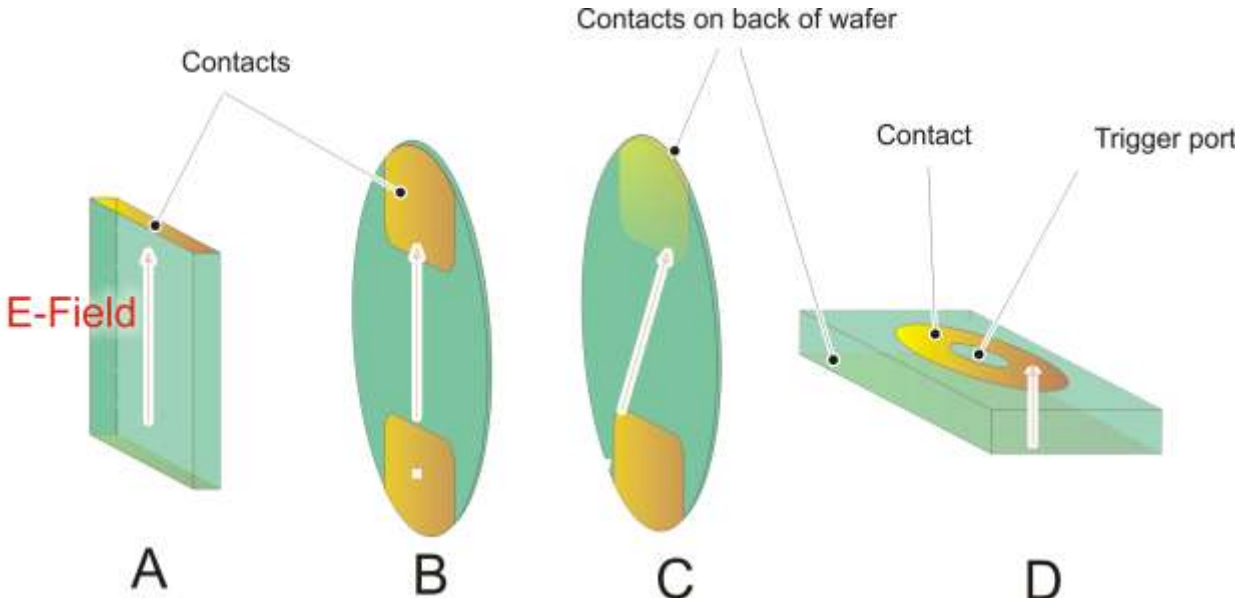


Figure 2.2 Various PCSS Geometries

Four types of photoconductive modes exist: linear intrinsic photoconduction, linear extrinsic photoconduction, non-linear intrinsic photoconduction, and non-linear extrinsic photoconduction [16]. The *linear* descriptor specifies that for each photon injected into the bulk of the photoconductor one electron-hole pair is generated for conduction. Once photon injection is stopped, conductivity diminishes at a rate determined by the recombination time of the carriers. The *non-linear* descriptor specifies that photoconduction is driven by the avalanche process, in which carrier generation is initiated by photon injection but continues via impact ionization. In other words, one injected photon may ultimately generate multiple carriers that establish *lock-on* [17], or a continuing conductivity independent of the photon injection. The *intrinsic* descriptor says that the photon energy used for carrier generation is greater than the

photoconductor's band gap energy--the energy required to move electrons in the valence band to the conduction band. In intrinsic photoconduction, every atom is a potential absorption site; therefore, the absorption depth is very small and can lead to current filamentation at the location of photon entry where carrier generation is dense [16] [5]. The *extrinsic* descriptor, on the other hand, says that the photon energy used for carrier generation is less than the photoconductor's band gap energy. Therefore, the photon energy does not excite electrons in the valence band but excites unionized electrons at the dopant sites. Since the dopant concentration is much less than the atomic concentration, a much larger absorption depth is possible. If absorption, or carrier generation, can be distributed uniformly throughout the bulk then uniform conduction is possible. Bulk current density would be minimized and current filamentation would be avoidable [16].

Switching Materials

Several PCSS materials have been used for high power switching applications. Si and GaAs are two of the most common materials; however, GaAs has surpassed Si in pulse-power generation circuitry due to its superior electrical characteristics [8]. In recent studies, SiC is shown to be potentially an even better PCSS material than GaAs depending on the preferred operation mode [1]. Table 2.1 lists the material properties of the PCSS materials. Silicon has the lowest breakdown field strength out of the three PCSS materials due to its smaller band gap. It is an indirect bandgap photoconductor that absorbs wavelengths λ=1.06 μm. Thus, Si has a large carrier lifetime and can conduct for milliseconds with a nanosecond illumination. Its *dark resistivity*, or unilluminated resistivity, is low therefore current leakage is prevalent. Current leakage easily causes

thermal runaway due to its relatively low thermal conductivity. Thermal runaway damages then Si bulk material. In comparison GaAs has a larger band gap and can therefore block higher fields. GaAs has higher mobility as well due to its direct band gap; therefore, it can photoconduct for picoseconds to nanoseconds in low fields (< 5kV/cm).The GaAs PCSS is commonly switched extrinsically with wavelengths of λ=1.06 μm due to its deep energy states from impurities. Although GaAs thermal conductivity is relatively low, it is less prone to thermal runaway than Si due to its dark resistivity of 10^7-10^8 Ω-cm. Operating GaAs in high fields (~5kV/cm) allows non-linear mode operation. GaAs has the ability to lock-on and thus conduct for microseconds to milliseconds. The optical absorption depth is around 1cm [3]. 6H SiC has the largest bandgap of the three PCSS materials presented. Theoretically, it can block the highest electric field. 6H SiC has an indirect bandgap, thus carrier lifetimes are approximately hundreds of nanoseconds to several microseconds. Similar to GaAs, deep energy states from impurities provide the carriers. Extrinsic photoconduction is possible with wavelengths of λ=1.06μm or λ=532nm. The optical absorption depth is a few centimeters [18].

Table 2.1 Material Properties of Various PCSSs [3] [19]

Properties	Si	GaAs	6H SiC
Band Gap	1.12 eV	1.42 eV	3.02 eV
Critical breakdown field strength	$3x10^5$ V/cm	$4x10^5$ V/cm	$3x10^6$ V/cm
Electron mobility	1500 cm^2/V-s	8500 cm^2/V-s	200-300 cm^2/V-s
Hole mobility	600 cm^2/V-s	400 cm^2/V-s	50 cm^2/V-s
Saturation velocity	$2x10^7$ cm/s	$1x10^7$ cm/s	$2x10^7$ cm/s
Thermal conductivity	1.45 watt/cm°C	0.46 watt/cm°C	5 watt/cm°C
Intrinsic carrier concentration	$1.6x10^{10}$ cm^{-3}	$1.1x10^7$ cm^{-3}	~$1x10^{-6}$ cm^{-3}
Resistivity	10^4 Ω-cm	10^7 Ω-cm	10^{11}-10^{12} Ω-cm
Dielectric constant	11.8	10.9	9.6

Off State Resistance in Linear Mode

When a PCSS is operated in linear mode, its on-state and off-state resistance values are important to the efficiency of the system and the lifetime of the switch. The off-state resistance of any semiconductor, including the photoconductor, is calculated by using the steady-state resistivity ρ_o of the bulk,

Equation 2.1 $$R_s = \frac{\rho_o h_s}{w_s d_s}$$

The resistivity is considered a *dark resistivity* in a photoconductor when the bulk is unilluminated. The bulk material must be intrinsic or compensated to have an effective off-state, or high open switch resistance. Compensation in an extrinsic semiconductor is when its extrinsic Fermi energy is returned to the value close to its intrinsic Fermi energy by the use of a compensator. The compensated bulk behaves intrinsically in the off-state, meaning no free carriers are available for conduction. In the case of n-type (nitrogen

doped), or p-type (boron doped), 6H-SiC photoconductor, the compensating material is Vanadium. The N or B dopant is entirely ionized at room temperature, thus trap sites introduced by the Vanadium trap the ionized carriers at deep energy centers. The Vanadium concentration is generally an order of magnitude higher than the dopant, therefore the Vanadium atoms are partially ionized. The unionized atoms are available to become free carriers when stimulated by photons. The dark resistivity of the SiC PCSS can be described by,

Equation 2.2 $$\rho_o = \rho_{DARK} = \frac{1}{(N_D^+ - N_A^-) q_E \mu_E}$$

where the difference between the ionized donor density N_D^+ and ionized acceptor density N_A^- is quite small. The electron charge is q_E and the electron mobility μ_E are only considered since the hole mobility is much lower. Therefore Equation 2.1 for SiC PCSS becomes

Equation 2.3 $$R_{so} = \frac{h_s}{(N_D^+ - N_A^-) q_E \mu_E w_s d_s}$$

On-State Resistance in Linear Mode

The on-state resistance for a linear photoconductor can be derived using by using the rate of change equation for carrier density [7]. Incident photons create electron-hole pairs (EHP) as carriers; their individual concentrations are equal.

Equation 2.4 $$n_E = n_H = n$$

The general form of the rate of change equation for carrier density, or continuity equation for the photoconductor under illumination is,

Equation 2.5 $$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \mathbf{J} + g_{\mathrm{n}} - \frac{n}{\tau_{nt}} - \frac{(1-n_i)n}{\tau_s}$$

where,

n, carrier concentration
t, time
q, charge
J, current density vector
g_{n}, carrier generation rate
τ_{nt}, carrier lifetime
τ_s, system transit time
n_i, contact injection inefficiency.

The terms in Equation 2.5 are described in words as,

Rate of change of carriers =
+The divergence of the EHP flux vector due to carrier drift and diffusion
+ EHP production rate
- EHP attrition rate from recombination
- EHP loss rate due to contact injection inefficiency

Assuming that there is no electric field applied to the photoconductor and the EHP concentration due to generation is uniform, Equation 2.5 can be rewritten as

Equation 2.6 $$\frac{\partial n}{\partial t} = g_{\mathrm{n}} - \frac{n}{\tau_{nt}} \ ,$$

where g_n is due to illumination. Allowing the quantum efficiency to be unity, meaning that every photon injected creates one EHP, the carrier generation g_n is given by,

Equation 2.7 $$g_n = \frac{\#\ of\ incident\ photons\ into\ the\ photoconductor}{time \times volume\ of\ photoconductor} = \frac{P_L(t)(1-r)}{E_\lambda w_s h_s d_s}$$

where $P_L(t)$ is the time varying incidental laser power, r is the material reflectivity, and E_λ is the photon energy. Assuming that there is perfect photon absorption, or zero material reflectivity, Equation 2.6 can be rewritten as

Equation 2.8 $$\frac{\partial n}{\partial t} = \frac{P_L(t)}{E_\lambda w_s h_s d_s} - \frac{n}{\tau_{nt}} \ .$$

To solve for carrier density in the photoconductor, the carrier rate equation is integrated over time by substituting τ for t,

Equation 2.9 $$n(t) = e^{\frac{-\tau}{\tau_{nt}}} \int_0^t e^{\frac{\tau}{\tau_{nt}}} \frac{P_L(\tau)}{E_\lambda w_s h_s d_s} d\tau \ .$$

For constant optical power $P_L(t)=P_o$ over time $t = t_L$, the carrier density in Equation 2.9 becomes,

Equation 2.10 $$n(t) = \frac{P_o(1-e^{\frac{-t}{\tau_{nt}}})\tau_{nt}}{E_\lambda w_s h_s d_s} \ , \quad 0 < t < t_L \ .$$

If the optical source is switched off instantaneously at $t=t_L$, the carrier density decrease exponentially over time as,

Equation 2.11 $$n(t) = N_o e^{\frac{-t}{\tau_{nt}}}$$

where N_o is the carrier density at $t = t_L$. If the optical pulse length t_L is much less than the carrier recombination time τ_{nt}, then,

Equation 2.12 $$(1 - e^{\frac{-t}{\tau_{nt}}}) \approx \frac{-t}{\tau_{nt}}$$

and at $t=t_L$, Equation 2.10 can be approximated as

Equation 2.13 $$n(t_L) = \frac{E_o}{E_\lambda w_s h_s d_s} = n \ ,$$

where the *total optical energy* $E_o=P_o t_L$. Finally, to arrive at the on-state resistance, the *dark resistivity* ρ_{DARK} substituted in Equation 2.1 is replaced by *light resistivity* ρ_{LIGHT} where

Equation 2.14 $$\rho_o = \rho_{LIGHT} = \frac{1}{nq(\mu_E+\mu_H)} .$$

The on-state resistance at $t=t_L$ for $t_L<<\tau_{nt}$, by combining Equation 2.13, Equation 2.1, and Equation 2.14 is

Equation 2.15 $$R_{SC} = \frac{\rho_{LIGHT} h_s}{w_s d_s} = \frac{E_\lambda h_s^2}{qE_o(\mu_E+\mu_H)} .$$

The SDDA and DDSA SiC PCSS

The two main types of SiC PCSSs are formally introduced. The energy level of the donor Nitrogen resides just below the conduction band energy level E_c rendering the 6H-SiC n-type, prior to compensation. The Vanadium acceptor energy level lies close to the conduction band energy level E_v. The resultant bulk material is termed SI-SDDA 6H-V:SiC, where *SI* means *semi-insulating* and *SDDA* means *shallow donor, deep acceptor.* The energy level of acceptor Boron resides just above the valence band energy level E_v rendering the 6H-SiC p-type, prior to compensation. The situation is now reversed, and the Vanadium donor energy level lies just above mid-bandgap. In this case, the resultant bulk material is termed SI-DDSA 6H-V:SiC, where *DDSA* means *deep donor, shallow acceptor.* The energy levels are depicted in Figure 2.3 along with the wavelength of light with its corresponding energy location, used for carrier generation.

2.2. **Field Enhancement at Material Boundaries**

The large local electric field at the material boundaries in the PCSS is suspected to cause premature bulk breakdown. In order to understand field enhancement and its contribution to bulk breakdown, one must understand the electric field in dielectrics and the effect of boundary relations on field distributions.

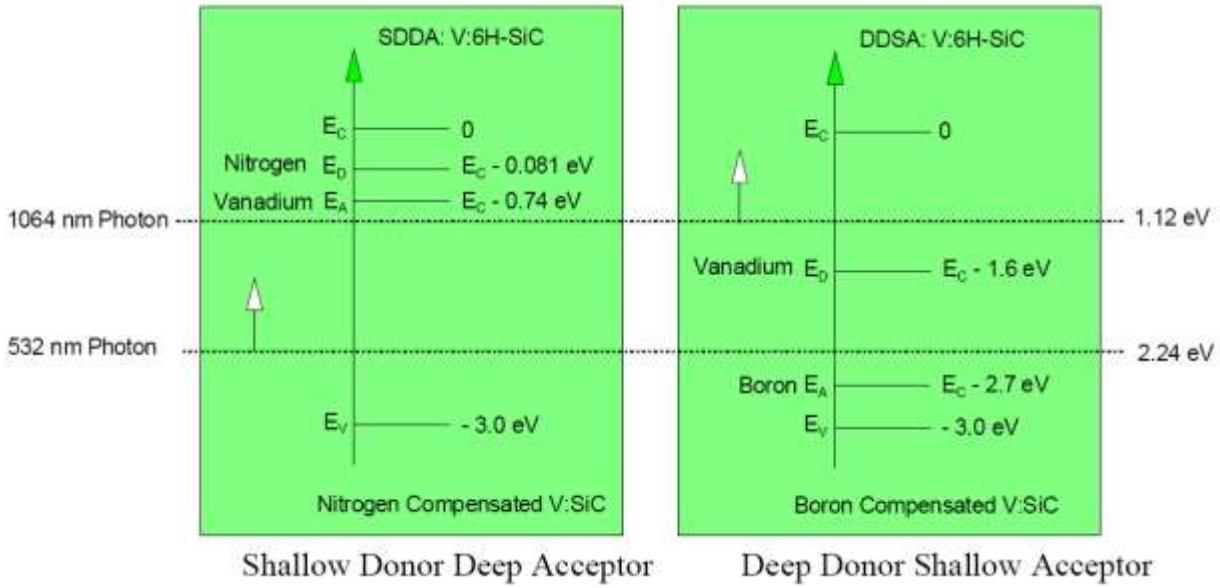


Figure 2.3 Vanadium compensation structures in the SiC PCSS

Consider an isotropic photoconducting substrate as the bulk dielectric. The bulk dielectric is placed in an electrostatic field. The lack of charge migration in a dielectric causes its molecules to behave like dipoles and polarize. Surface charge then appears on the faces of the dielectric. The dipole moment per unit volume, or *polarization P* in a rectangular dielectric slab, for example, is given by,

Equation 2.16 $$P = \frac{QL}{AL} = \frac{Q}{A} = \rho_{sp} \quad (\text{C m}^{-2})$$

where Q is the charge of all dipoles, L is the thickness of the slab, A is the surface area, and ρ_{sp} is the surface charge density. To solve for the electric flux density D though the dielectric slab, the definition of electric flux density in free space must be modified by including the surface charge density

Equation 2.17 $$D = \epsilon_0 E \quad \textbf{(}\text{free space)}$$

Equation 2.18 $D = \in_0 E + \rho_{sp}$ (dielectric) (C m $^{-2}$)

A more general form may be expressed in vector notation,

Equation 2.19 $\boldsymbol{D} = \in_{\mathbf{0}} \boldsymbol{E} + \boldsymbol{P}$ (dielectric) (C m $^{-2}$)

It is the electric flux density ***D*** that is increased by the boundary relations that will increase electric field intensities.

The electric field in a single medium is considered continuous; however, the electric field can abruptly change in magnitude and direction at a boundary between two different media. The electric field may be decomposed into two components with respect to the boundary it may cross. One component is the tangential electric field and the other is the normal electric field. When the boundary is between a conductor and dielectric, as is the case for electrodes bonded to a photoconducting substrate, the tangential electric field across the boundary is zero (assuming the substrate in the off-state is a perfect insulator). Furthermore, according to Gauss's law the normal flux density at the dielectric-conductor boundary is equal to the surface charge density on the conductor.

Equation 2.20 $D_{Normal} = \rho_{sp}$

Therefore it is important to address the arrangement of charge density in photo-switches where electrodes interface with the dielectric bulk material.

The maximum field intensity that a bulk dielectric in the off-state can sustain without breakdown is known as its dielectric strength. Ideally, breakdown would only occur at the point when the applied electric field intensity exceeds the bulk dielectric strength. Actually, breakdown occurs when the induced field exceeds the bulk dielectric

strength. The induced field may become larger than the applied field due to electrode curvature, electrode surface quality, and micro-protrusions for example [20].

A distinction must be drawn between the applied electric field and the induced, or local, electric field. Not always is the electric field intensity that is applied the same intensity found at the material boundaries. According to Equation 2.20, the electric field intensity at the boundary is proportional to the surface charge density on the conductor surface. The charge density tends to be concentrated on surfaces, such as electrodes, with small radii of curvature and less on surfaces with large radii of curvature. Charge density is also higher on surfaces with microprotrusions, such as rough surfaces. This is known as *field enhancement*, since the applied field is actually more intense where charge is concentrated. Field enhancement is also observed at triple point junctions, or locations where three different media with three different permittivities meet (i.e. the cathode-dielectric-vacuum interface).

In an ideal triple point junction the equipotential lines are parallel and uniformly spaced (Figure 2.4 (i)). In the practical case, junctions are mismatched causing a crowding of field lines and highly concentrated equipotential lines, i.e. intensifying the local electric field (Figure 2.4 (ii)) [21]. The degree of equipotential line concentration is a function of the degree of electric field line deflection. The field line deflection depends on the relative permittivity of the dielectric material described by [20],

Equation 2.21 $$\frac{\tan(\alpha_1)}{\tan(\alpha_1)} = \frac{\epsilon_1}{\epsilon_2}$$

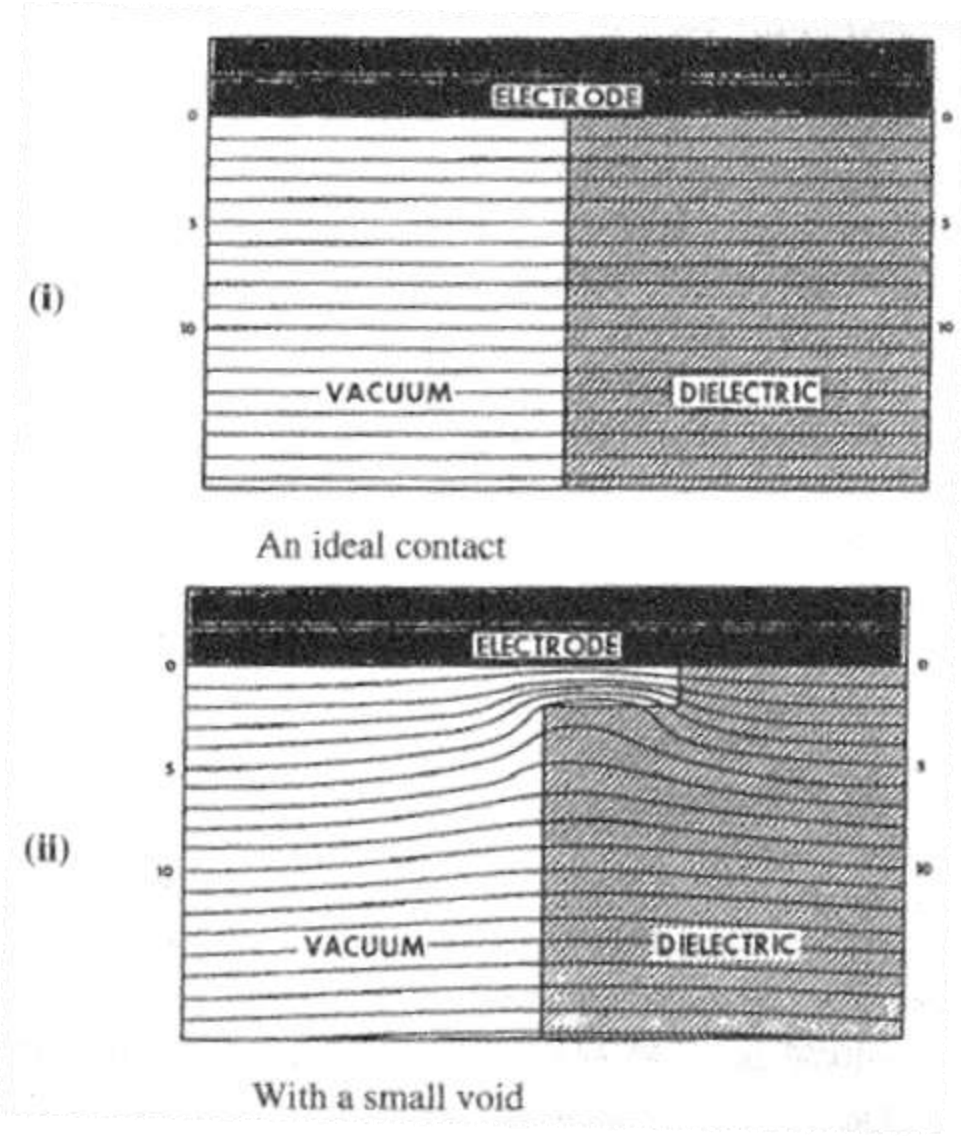


Figure 2.4 (i) Equipotential lines in an ideal triple point junction. (ii) Equipotential lines in a realistic triple point junction [21].

Field enhancement contributes not only to bulk breakdown but to surface flashover as well. Surface flashover is the second mechanism that plagues high voltage dielectrics, and more specifically photo-switches. It is generally accepted that surface flashover initiates with electron emission from the cathode at the triple point junction of a photo-switch. The emitted electrons strike the surface of the dielectric and produce secondary electrons that in turn strike again releasing tertiary electrons. The process

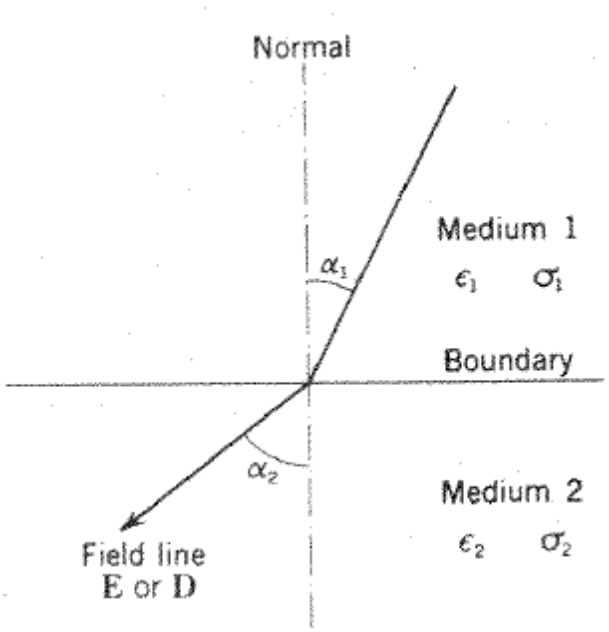


Figure 2.5 A field line bending at the boundary of media with different permittivities.

continues across the surface of the dielectric in an avalanche fashion. The bombarding electrons desorb some of the gas previously absorbed by the surface. The gas cloud is then ionized by the electrons and a conductive path is setup between the anode and cathode. Flashover then occurs. The intermediate steps during flashover, however, are debatable [21]. It is apparent why the triple point junction is a weak point in real photo-switches.

2.3. **Abrasive Machining**

Knowing that in electric fields in the PCSS package are enhanced by abrupt permitivitty changes, rough interfaces, and acute angles, steps can be taken to reduce their enhancement contribution. Material interfaces should be uniform and smooth as possible, acute angles should be relieved by rounding and contouring, and permittivity changes should happen in lower field areas. Abrasive machining, such as grinding, is a common mechanical process that may be used to remove and polish ultra-hard, ceramic

substrate material. Mechanical removal, as opposed to optical or chemical removal, is preferred when substrate curves and contours are required. A precise surface roughness and fine quality can also be achieved using a more accurate form of abrasive machining such as lapping, or more so, polishing.

Abrasive Processes

The mechanical removal of brittle material is complex [22]. It is important to become familiar with tribology, the science and technology of interactive surfaces in relative motion. More simply, one must study friction, lubrication, and wear mechanisms. In the case of brittle materials, such as the ceramic SiC, wear mechanisms have been defined and categorized [23]. Figure 2.6 is shown to give an idea of the complexity of ceramic material removal.

There are several abrasive processes that may be used for ceramic removal: Grinding, Honing, Lapping, Ultrasonic machining, polishing, blasting, etc. This list is by no means exhaustive. Grinding is where hard particles are bonded onto a rotating structure that contacts the workpiece. Honing is the rapid oscillation of an abrasive slab of a workpiece surface. Lapping employs a fine, loose abrasive in a fluid suspension that is scrapped across a workpiece surface in an oscillatory motion. Polishing is where an abrasive is applied to a soft tool surface, dry or wet, then rotated on a workpiece to gently smear the workpiece surface layers. Blasting is where particles are projected with high velocity at the workpiece. The surface quality that grinding can produce compared to machining process of cutting is superior, since the shear deformation mechanism in grinding produces much smaller chips. The chip thickness produced during grinding is

much less than 0.1mm, whereas the chip thickness during cutting is greater than 0.1mm. Grinding is the most easily understood out of the abrasive processes and is applicable for shaping the PCSS package. Therefore it will be described in the following paragraphs.

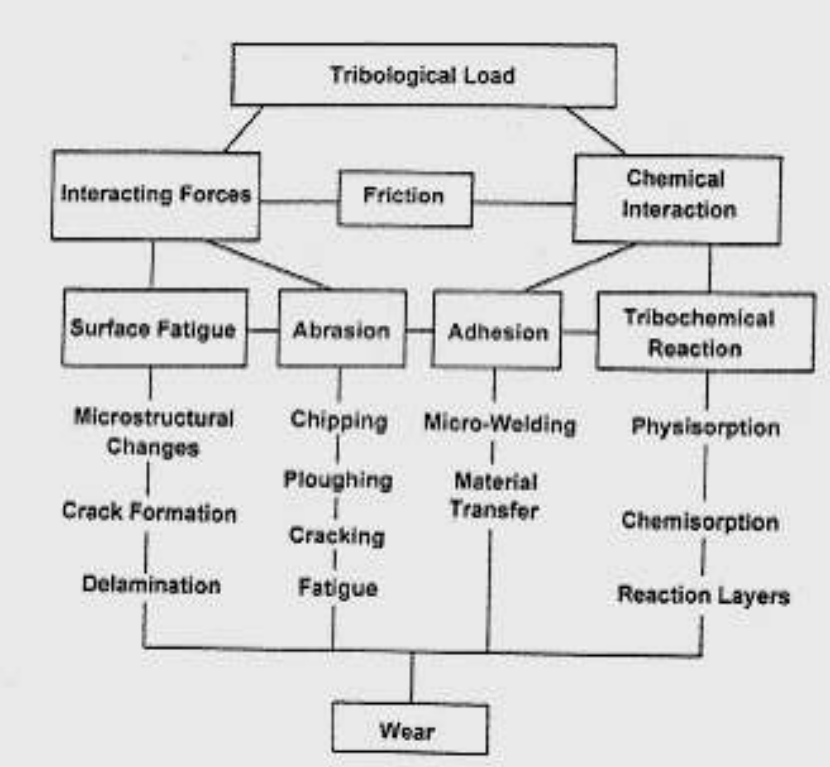


Figure 2.6 Principal Mechanisms and Effects of Wear [23].

Grinding

In the grinding process, abrasive grits are bonded to a wheel that rotates at high speeds. As the wheel makes contact with the workpiece, the relative motion between the wheel and the workpiece constitutes a *friction-pair*. The abrasive grit must have a material hardness greater than that of the workpiece in order to chip, plough, deform, and ultimately remove workpiece material in a predictable and useful fashion (Figure 2.7).

The ratio should not be less than 1.7 to maximize tool life and grinding efficiency. Diamond is the best abrasive grit for the grinding SiC. At room temperature the hardness of diamond is ~8000 kg/mm^2 and the hardness of SiC is ~3000 kg/mm^2. The hardness ratio is acceptable at ~2.6 and remains acceptable for temperatures greater than 1200^{o}C.

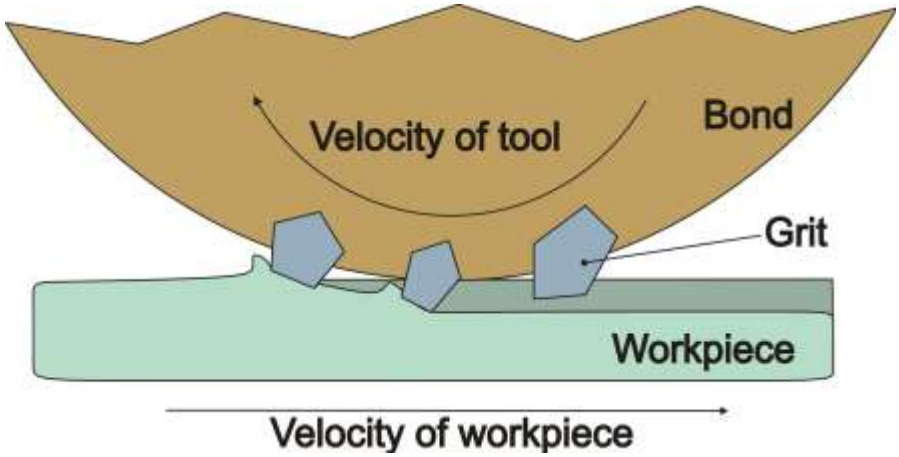


Figure 2.7 The process of grinding

There are various grinding geometries that may be used depending of the shape of the workpiece. For surface grinding, the spindle of the tool can be either horizontal or vertical in relation to the workpiece surface. A horizontal spindle with a straight-fed and cross-fed table is best for uniform surface removal for a large surface area since the cut depth can be set prior to a pass and remain constant throughout the cut (Figure 2.8 (A)). A vertical spindle is best used for varying the depth of cut during a pass, the metal machining equivalent of drilling (Figure 2.8 (B)).

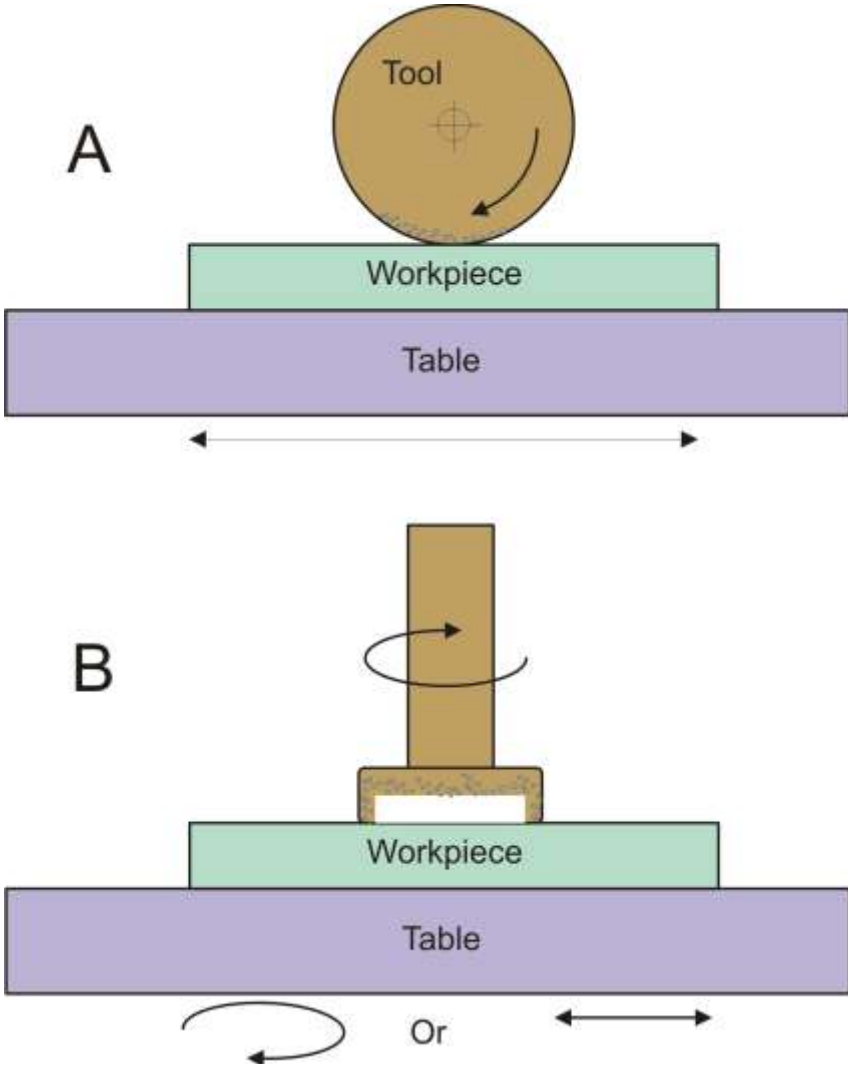


Figure 2.8 (A) Horizontal spindle grinding and (B) vertical spindle grinding.

Parameters of Grinding

In order to produce field reducing contours and fine surface finishes on the SiC substrate in a SiC PCSS, a custom grinder and tools are required. It is important to understand the set-up parameters of the grinding process. Knowing the parameters and how they relate will help guide the design of a custom grinding geometry and tooling.

Table 2.2 names the parameters and their corresponding variables used to formulate fundamental grinding equations. Figure 2.9 depicts the spatial relation of the variables to the grinding set-up for aid in developing the fundamental grinding equations.

Table 2.2 Tribological Parameters

Tribological parameters	Variable	Units
Grinding width	b	m
Removal rate	q	m^3/s
Workpiece speed	v_w	m/s
Depth of cut	a	m
Number of chips per unit time	N	s^{-1}
Number of cutting edges per unit area	C	m^{-2}
Grinding wheel surface speed	v_s	m/s
Chip Volume	V	m^{-3}
Wheel diameter	d_s	m
Chip length	l	m

The average cross-sectional area of chips *A* is derived as follows,

Equation 2.22 $$q = bv_w a$$

Equation 2.23 $$N = Cbv_s \ .$$

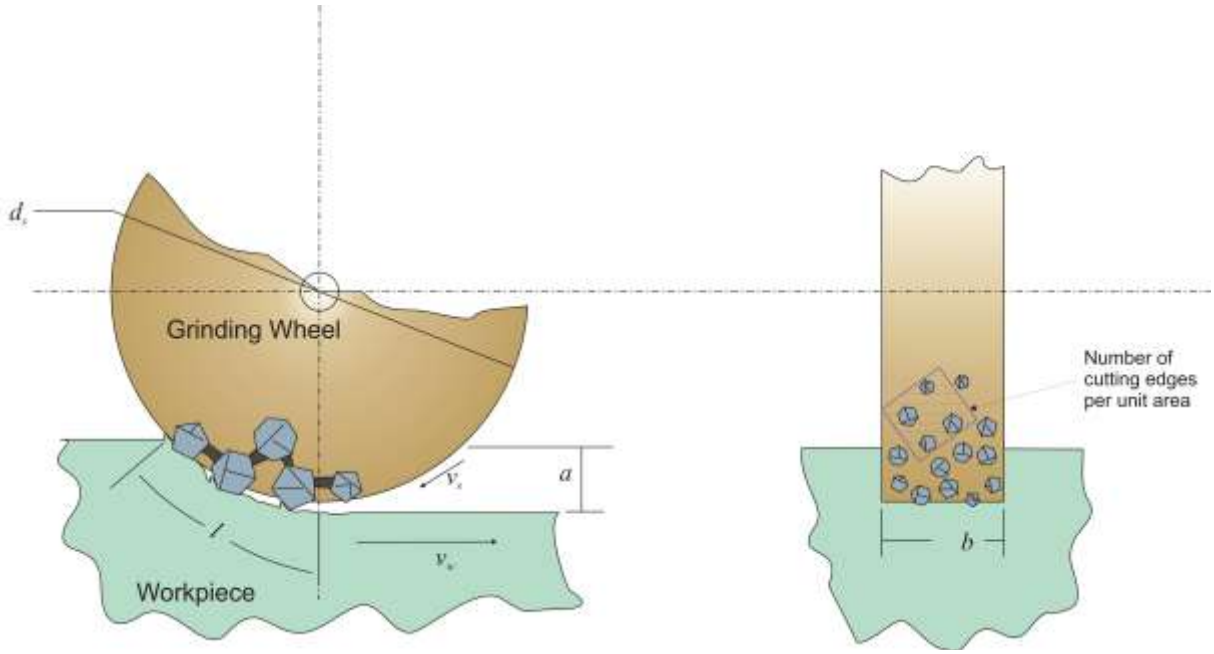


Figure 2.9 Parameters of surface grinding

Therefore the removal rate divided by the number of chips produced per unit time gives the average chip volume,

Equation 2.24 $$V = \frac{q}{N} = \frac{v_w a}{C v_s} .$$

Assuming that the chip length is equal to the contact length, by using trigonomic relations it follows that the chip length is approximately,

Equation 2.25 $$l = \sqrt{d_s a} \ .$$

By combining Equation 2.23, Equation 2.24, and Equation 2.25, the average cross-sectional area of chips is obtained by,

Equation 2.26 $$A = \frac{v_w}{C v_s}\sqrt{\frac{a}{d_s}}\ .$$

Several important points are uncovered with the derivation. Equation 2.26 shows that the average cross-sectional area of chips *A* is decreased by increasing the tool speed or decreasing the depth of cut. When decreasing *A* the cutting force on each cutting edge is decreased. An increase in cutting force can dislodge the abrasives from the binder on the tool. The tool life is shortened dramatically if the force is too great. The dislodging due to an optimal force can also be beneficial by exposing new, sharper cutting edges from binding layers beneath. The exposure of new cutting edges through wear is known as *self- sharpening.* On the other hand, if the average cross-sectional area of chips is decreased below the self-sharpening threshold, the generation of heat becomes a concern and the surface roughness decreases. Therefore, the cutting force must be chosen carefully.

The average cross-sectional area of chips can also be altered by varying the grit concentration, or the number of cutting edges per unit area *C.* An increase in *C* causes an increase in the number of active cutting points and a decrease in the average distance from one cutting edge to another. At some point, a further increase in grit concentration is limited by the grit size. Cutting edges without adequate spacing, or *chip pockets*, cause wheel loading since the swarfs produced become wedged between cutting edges. Thus, a further increase in grit concentration must be accompanied by a decrease in grit size to avoid grinding burn. The grit size-to-concentration relation is known as *mesh size* and is defined as the number of openings per linear inch in the mesh screen that is used to filter abrasive particle sizes. Table 2.3 shows the relation between mesh and particle size. For an optimal removal rate an adequate volume chip pockets must be present.

Table 2.3 Mesh and Particle Size

Particle Size in Microns	US Grit (Mesh)
0.5	12000
1	5000
2	3000
3	2000
6	1200
10	1000
15	800
20	600
25	480
35	320
45	280
60	220
80	180
90	150
110	120
150	100
180	80

An increased grit concentration also results in a decrease in the average chip thickness; a decrease in chip thickness usually correlates to an increase in surface finish quality. In general, individual contact forces on the cutting edges are decreased by an increase in grit concentration, when all other parameters remain constant. In the case of

SiC, chips tend to result from brittle fracture which lowers the thermal load on the tool. A lower thermal load allows for faster tools speeds with finer grit sizes. Wheel wear is also minimized.

Grinding Modes

Ceramic grinding follows the general model for abrasive processes. The general model is composed of five grinding modes. Each mode has uniquely defining qualities. Only two modes are of importance here.

(a) Brittle Fracture Grinding Mode

Due to the brittle nature of ceramic material compared to metallic material very little plastic deformation is seen under the grinding load prior to fracturing. In this mode surface quality is the most rough. Debris produced can be examined by SEM to determine if its consistency is mainly of fragments produced by brittle fracture. A sign of brittle fracture is the occurrence of scratch edges in a ground surface (Figure 2.10).

(b) Ductile-Regime Grinding Mode

To transition from the brittle to ductile grinding regime smaller cutting depths must be used. A smaller depth of cut promotes plastic deformation of the ceramics. The material is removed by a plastic flow mechanism and not fracture.

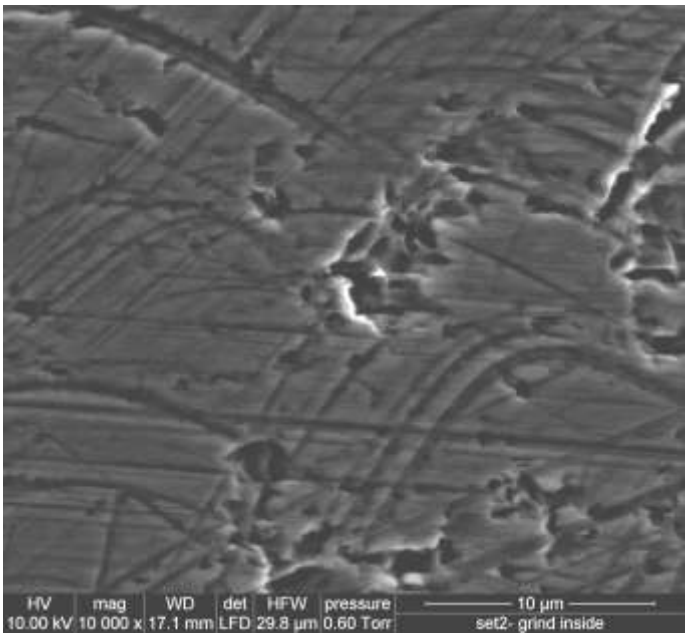


Figure 2.10 Fractures in SiC from surface grinding.

The depth of cut d_c transition point from brittle to ductile grinding, assuming that the depth of cut is equal to the infeed rate, is given by,

Equation 2.27 $$d_c = \beta \left(\frac{E}{H}\right)\left(\frac{K_c}{H}\right)^2$$

where β is a constant, E is Young's modulus, H is the hardness, and K_c is the fracture toughness. The ductile regime limit is based on surface examination. If post-grind examination shows 10 percent surface fracture and 90 percent ductile flow, then the grind is considered to be in the ductile-regime mode.

The ductile-regime mode is the preferred mode for the finishing contours. Also, grinding surface quality can be enhanced at the expense of grinding time. Figure 2.11 shows SiC ground in the ductile-regime mode. The surface is free of fracture lines and appears as if material was torn off.

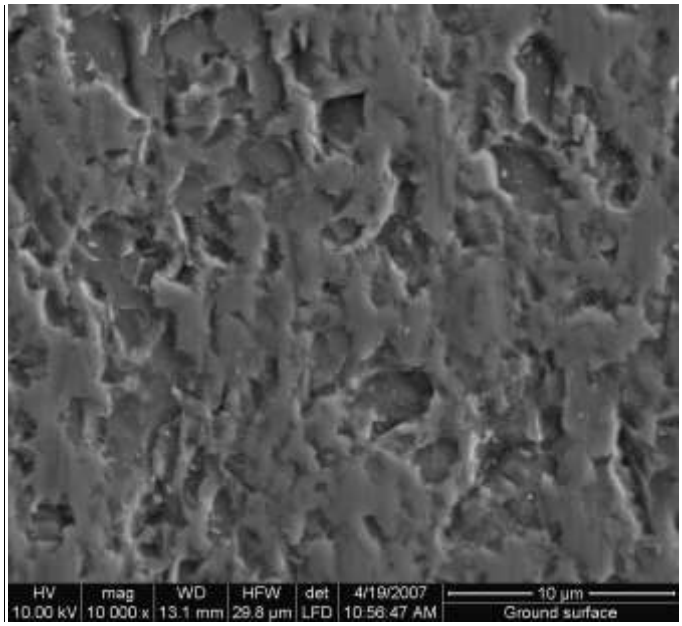


Figure 2.11 Appearance of SiC ground in the ductile-regime grinding mode.

2.4. **Literary Review**

This is a collection of the most useful books and papers that pertaining to the topic of this paper. A brief description of each document accompanies the publication information.

Works Relating to the Problem

The following papers address the issues of SiC when used as a linear optically trigger switch material. To fully utilize the field blocking capabilities of SiC, bulk breakdown mechanisms in photo-switches must be considered. Understanding current photo-switch geometries and electric field enhancement tendencies helps in designing a high electric field switch package.

Photo-switch Applications

Friedrichs, P. et al. "SiC power devices with low on-state resistance for fast switching applications." The 12th International Symposium on Power Semiconductor Devices and ICs. May 2000. 213-216.

This paper addressed the use of SiC for high speed devices with low on state resistance, fast recovery time, and high blocking voltages. Specific on state resistances on the order of 47 mOhm cm^2 were observed with the ability to block 1800 Volts. The recovery times observed were 20ns. These characteristics help verify the expectation of SiC as the semiconductor of choice for up and coming solid state switches.

Loubriel, G.M. et al. "Photoconductive semiconductor switches." Plasma Science, IEEE Transactions on 25.2 (1997): 124-130.

This paper investigated the use of optically triggered GaAs in low impedance, high voltage, high current, compact applications. This paper addressed five specific applications for which the switches are being tested. Munitions firing sets, electro-optic modulators, drivers for laser diode arrays, compact accelerators, and ground penetrating radar are the topics discussed.

Nunnally, W. C. and M. Mazzolla. "Opportunities for employing silicon carbide in high power photo-switches." Pulsed Power Conference, 2003. Digest of Technical Papers. PPC-2003 14th IEEE International. IEEE, June 2003. 823-826.

This paper describes the opportunity for deploying semi-insulating SiC wafers for high power applications. It also discusses the parameters of SiC and the methods of fabricating photo-switches. SiC with a band gap of 3.26eV can withstand fields of 3000 kV/cm before breakdown occurs and handle a current density of 2.4 kA/cm^2 . Its dark

resistivity is 10^{11} Ohm-cm. Furthermore, this paper emphasizes the importance of building high electric field packaging.

Pre-mature switch breakdown

Kelkar, K., et al. "Compact silicon carbide photoconductive switch for high power applications: experiments and simulation." Power Modulator Symposium, 2004 and 2004 High-Voltage Workshop. Conference Record of the IEEE Twenty-Sixth International . 2004. 555-559.

This paper introduces a novel SiC photo-switch design that uses stacked epi-layers to improve switch performance. A test stand was designed and built to measure the pulse charging behavior of the switch. The optical absorption depth of the switch was also measured using light of 532nm and determined to be approximately 1cm. The test stand discussed gives insight on how to build a custom test stand that may be used to compare the DC electric field blocking performance of new switch designs. Knowing the optical absorption depth will be important for fabricating an optimum sized photo-switch. The size of the photo-switch will determine the size of the equipment needed to manipulate the bulk geometry.

Nunnally, W. C., et al. "High electric field, high current packaging of SiC photo-switches." IEEE International Pulsed Power Conference. Monterey, CA, US, 2005.

This paper outlines SiC photo-switch fabrication problems that lead to pre-mature switch failure. These problems include faulty ohmic contact alignment, incomplete insulating encapsulation, solder protrusions in high electric field regions, and incomplete interface bonding. Breakdown is found to occur at the air-SiC-copper contact triple point where high electric field enhancement resides.

Nunnally, W. C. and D. Cooperstock. "Methods and configurations for improving photo-conductive switch performance." Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. Conference Record of the Twenty-Fifth International . July 2002. 183-186.

This paper explores the use of a high dielectric strength and/or a high resistivity material to lower the surrounding electric fields of GaAs photo-switch and minimize sub-surface conduction. One method creates a capacitance between the electrode and the edge bulk material limits the current path and reduces the electric field. The other method fills the high field region with high resistivity material to homogenize the electric field and distribute the switch voltage over a long path to reduce electric field.

Stout, P.J. Kushner, M.J. "Processes leading to filaments in optically switched semiconductors." Proceedings IEEE Pulse Power conference. 1993. 808-813.

This paper reports that high field locations near abrupt contacts cause non-uniform carrier injection into the bulk of the device. Abrupt or rough contacts also provide end points for filaments strike and induce breakdown. It is suggested that graded contacts pull peaks fields away from contacts and into the bulk effectively minimizing field enhancement. Also important is the grounding or ungrounding of the base contact since field enhancement for the grounded case occurs at the anode during the peak of the closing pulse. This implies initial research could focus on the anode design while using a simplified cathode.

Madangarli, V. P., et al. "Influence of contact architecture on the high-field characteristics of planar silicon structures." IEEE Transactions on Electron Devices (May 1996).

This paper discusses the importance of contact geometries on electric field distribution and leakage current in Si wafers. Although this paper analyzes planar photoconductive devices, the information gathered can be applied to a 2-D cross-section of the present axial photo-switch configuration by disregarding the surface flashover tendencies in the planar geometry. It is concluded that an elliptically shaped contact contour is ideal for voltage hold-off in planar structures. This shape could be applied to the cross-section of an axial switch structure.

Works Relating to the Solution

The solution to the premature breakdown of the existing photo-switch package is by no means a simple one. Previous work mostly contributes the breakdown issue to morphology of the electric field throughout the photo-switch package. The solution must therefore focus on manipulating the electric field around and through the package. Many techniques used to improve the electric field are discussed in literature pertaining to high voltage diodes. The overall goal is to use these techniques to design and fabricate a new package geometry, and then compare the breakdown mechanisms to ones in previous photo-switch packages. The publications related to the solution deal with the physical shaping of SiC, electrode configuration, and high voltage DC testing.

High Voltage Devices and Dielectrics

Williams, P F and F E Peterkin. "A mechanism for surface flashover of semiconductors." 7th Pulsed Power Conference. 1989. 890-892.

This paper discusses the flashover tendencies in junction devices with narrow depletion regions. Edge beveling may be used to increase the surface length of the

depletion region to better distribute the tangential electric field at the surface. Distributing the surface field thus limits the voltage hold-off to bulk avalanche breakdown processes. Edge beveling in the case of SiC photo-switches, however, is not directly beneficial since the electric field is uniformly distributed across the bulk material as opposed across a narrow depletion region. Yet, beveling at the electrode-bulk interface may better distribute the normal field around the electrode where the charge in a SiC photo-switch in concentrated.

Mihaila, A. et al. "Buried field rings - novel edge termination method for 4H-SiC high voltage devices." Semiconductor Conference, 2002. CAS 2002 Proceedings. International. 2002. 245-248.

This paper supports the idea that the performance of SiC devices is hampered by the field crowding at the structural edges inducing premature breakdown. The distinction between surface flashover and surface breakdown is important. Voltage breakdown in the SiC devices is reported as a function of the electric field due to interface charge. It reports on benefits of using of buried field rings to smooth the electric field crowding away from the gates thus improving breakdown voltage by 90 percent. Similarly, a buried structure in a photo-switch could help shape the field in a distributed manner and provide flashover prevention.

Cooperstock, David M. "Design, construction, and implementation of a high voltage, pulsed power test bed for the study of GaAs and SiC optically triggered switches." Thesis. University of Missouri-Columbia, 2004.

This thesis provides a good basis on testing SiC photo-switches. ElecNet simulation software proves to be valuable tool for simulating electric fields in and around

the photo-switch package. Different electrode geometries could be simulated in ElecNet, fabricated, and then tested in a test bed similar to the one described.

SiC Composition

Nakajima, A., et al. "Step control of vicinal 6H-SiC(0001) surface by H2 etching." Journal of Applied Physics 97.104919 (2005).

It is important to understand the crystalline structure of 6H-SiC when devising methods to manipulate it. This paper explains the resultant atomic structure and dangle bonds in SiC from performing an etch with a lateral direction component.

SiC Etching

Kim, D. W. et al. "Magnetically enhanced inductively coupled plasma etching of 6H-SiC." IEEE Trans. on Plasma Sci. 32.3 (June 2004): 1362-1367.

This paper reports on using SF_6 plasma to anisotropically etch the SiC substrate up to 100 micrometers. Via holes and large etch depths (100 to 200 micrometers) are achieved by using inductively coupled plasma etching; however, deep voids and via hole have vertical side walls and flat bottoms. Such structures tend to have sharp corners that would lead to field enhancement. Therefore, a combination of plasma etching and other fabrication techniques could produce structures with contoured features.

Lanois, F., et al. "Angle etch control of silicon carbide power devices." Applied Physics Letters 69.2 (1996): 236-238.

Although common in SiC processing, the reactive ion etching of SiC results in mostly vertical patterns. Remote plasma etching can produce isotropic contoured shapes but are often shallow and irregular. This paper reports on the method of using plasma

etching to create voids in SiC substrate that have angled sidewalls. The slope of the sidewall may be selected between 30-80 degrees by varying the bias voltage and O_2 additive in the process. Yet, the angles and depths produced are on the scale of several micrometers which may not be enough structural surface area to minimize charge crowding and field enhancement around an electrode interface in a photo-switch. It is possible however that the angle sidewalls obtained may serve as a stencil for a follow-up isotropic etch process to produce deeper contoured voids in the substrate.

SiC Laser Processing

Henry, M., et al. "Laser Milling - A Practical Industrial Solution for Machining a Wide Variety of Materials." Fifth International Symposium on Laser Precision Microfabrication. SPIE, 2004. 627-632.

This paper summarizes the laser milling process , the types of laser used for milling, removal rates and many other characteristics pertaining to laser milling. Laser milling is an option for SiC substrate processing. It is reported that a XeCl Excimer laser has a wavelength of 308 nanometers. At 308nanometers, the reflectivity of SiC is reduced and the photon energy is easily absorbed by the SiC through the inverse bremmstrahlung. An etch rate of 0.32 micrometers per pulse is possible.

SiC Grinding

Ahearne, E. and G. Byrne. "Ultraprecision grinding technologies in silicon semiconductor processing." Proceedings of the Institue of Mechnical Engineers 1 (2004): 253-267.

This paper details how semiconductors are ground, lapped and polished. Vertical-spindle type machines are reported to be commonly used for grinding silicon. These machines assure surface flatness as long as the eccentric axes of rotation are parallel. Furthermore, it is reported that the benefit of using rotational grinding configuration for processing reduces form errors due to elastic deformations of the machine under load. The grinding process discussed is a viable method for substrate processing.

2.5. **Summary of Literature**

The following information is a translation of the reviewed papers into point of interest for this research.

- SiC has a band gap of 3.26eV and can withstand fields of 3000kV/cm.
- The SiC photo-switch suffers from premature switch failure due to contact alignment, encapsulation issues, solder protrusions, and incomplete bonding.
- High field locations cause non-uniform carrier injection in photo-switches.
- Increasing the area at a depletion region of a semiconductor switch distributes and lowers surfaces fields.
- Etching, lasering, and grinding are methods that can be used to shape a SiC substrate.

The use of previous work helped to direct the studies in the design of a novel SiC photo-switch package and fabrication process. After reviewing and understanding how previous experiments were conducted and results gathered, the components specific to our research were designed, simulated, and constructed.

2.6. **Rationale for Developing the SiC PCSS vs. the GaAs PCSS**

Table 2.4 compares the different parameters of 6H SiC with GaAs [1]. When using UMC's packaging method, linearly operated SiC has the potential to surpass the switch performance of the lateral high-gain GaAs. Furthermore, the issue of filamentary damage can be avoided when operating in linear mode. Consider operating both SiC PCSSs and GaAs PCSSs in linear mode. SiC can support an electric field that is 12 times higher than what GaAs can support. The current density in comparable packing geometries can be similar, even though the mobility of SiC is only $1/20^{th}$ of GaAs. Calculations in previous work show that 16% of the optical energy necessary to achieve a conduction resistance in a GaAs PCSS is needed to produce the same resistance in a SiC PCSS. Furthermore, a SiC PCSS can be operated at a larger conduction electric field than a GaAs PCSS to drop essentially equal conduction voltages across them. Thus, the advantages of the SiC PCSS arise from operating the SiC material as high blocking fields. High blocking field operation justifies focusing on the development of a high electric field package. Also paramount is the order of magnitude larger thermal conductivity of SiC as compared to GaAs. Therefore, SiC can be operated at a higher average power [1].

2.7. **Problems Worthy of Investigation**

Today's extrinsic PCSS geometries suffer from several failure mechanisms from the bulk material current density. For example, the switch geometries shown in Figure 2.12 employ sharp electrode edges that enhance the electric field leading to dielectric strength failure. High field regions are also observed close to the anode increasing the impact ionization rate, which ultimately leads to breakdown [24]. The dielectric failure

may subsequently produce current density damage to the interface of the electrode and bulk.

Table 2.4 Comparison of material properties of GaAs and SiC [5]

Parameter	GaAs	6H-SiC	Unit
Band Type	Direct	Indirect	
Band Gap	1.43	3.02	eV
Electron Mobility @ 3 kV/cm	6000	40	$cm^2/V\text{-}s$
Electron Mobility @ 10 kV/cm	1500	200	$cm^2/V\text{-}s$
Max E-Field	250	3000	kV/cm
Dark Resistivity	10^7	10^9-10^{11}	Ohm-cm
Max Drift Velocity	$2x10^7$	10^7	cm/s
Recombination time	0.5	200-800	ns
Thermal Conductivity	0.55	4.9	W/cm-K

In Figure 2.12 (a) and (b), dielectric failure occurs in the form of surface flashover. In Figure 2.12 (c) and (d), dielectric strength failure occurs through the bulk material due to the formation of high current density filaments. The filaments are formed by non-uniform carrier injection due to field enhancement at either abrupt electrode contacts or rough edges on the electrodes [25]. In every example, large current densities ablate the contacts and bulk material of the PCSSs. In order to eliminate the failure mechanisms, one must implement an electrode geometry that reduces and makes uniform the on-state current densities as well as off-state charge distribution.

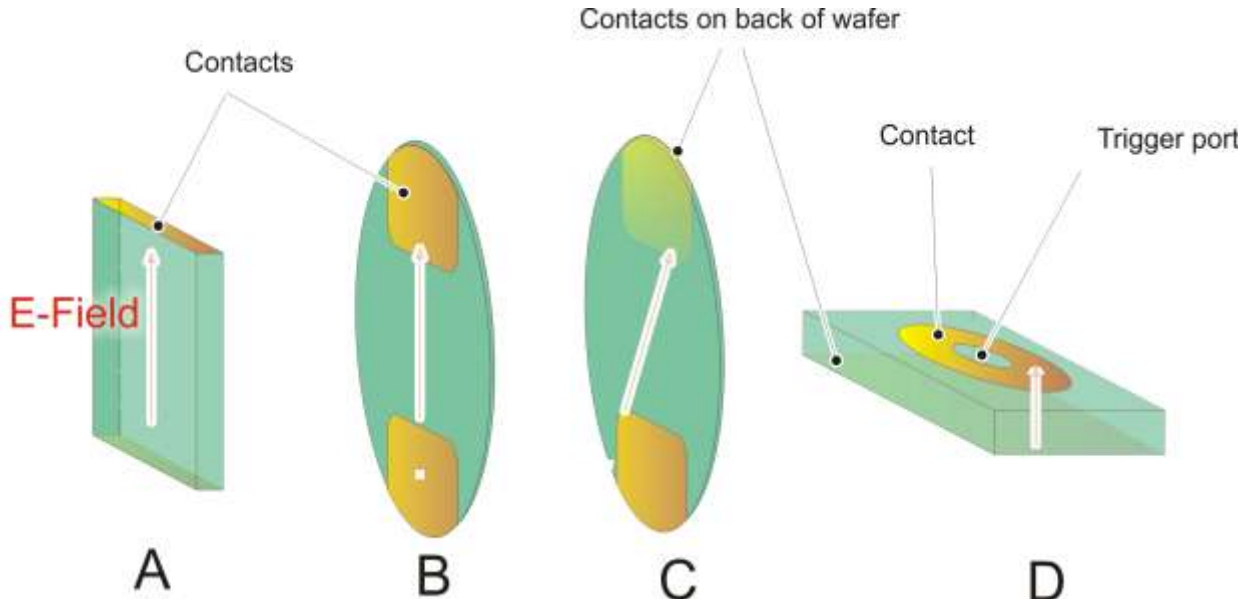


Figure 2.12 Various PCSS geometries. Contacts are deposited onto the bulk semiconductor material. (Figure repeated from previous section for convenience).

The most functional geometry for high power, pulsed power applications implemented in the SiC PCSS is shown in Figure 2.13**.** This geometry, developed by the University of Missouri-Columbia (UMC), has been tested extensively [11]. The switch exhibits an inadequate field blocking performance, however, due to premature breakdown in the bulk; premature breakdown occurs at a mean applied electric field of ~300kV/cm, not the projected 3MV/cm. The premature breakdown results from field enhancement due to several problems discovered in previous work [4]:

1) Faulty alignment of the Ohmic contact or the electrode on the opposing sides of the SiC substrate
2) Incomplete encapsulation with the insulating material in the high field region
3) Ragged solder protrusions at the bonding site in the high electric field region

4) Incomplete bonding at the surface interface that results in field enhancement points

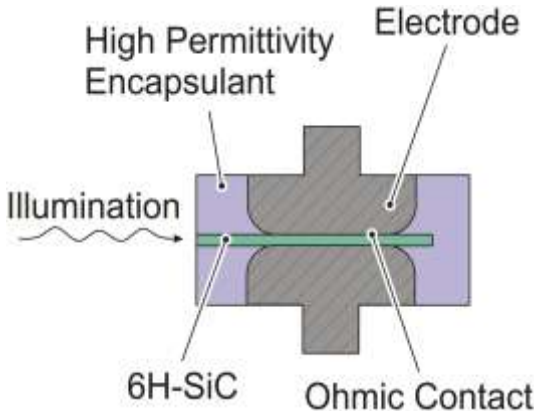


Figure 2.13 UMC PCSS package design. Illustration is shown with encapsulant.

No packaging method exists to effectively address the listed problems. Furthermore, electric field crowding at the location where the copper electrode leaves the SiC substrate possibly contributes to premature breakdown as well (Figure 2.14). These problems are worthy of investigation in order to further SiC PCSS technology. With a systematic approach, the problems can be solved. The ultimate goal is for this research to produce a novel PCSS packaging method that may improve on the problems of the existing SiC PCSS package or even eliminate them.

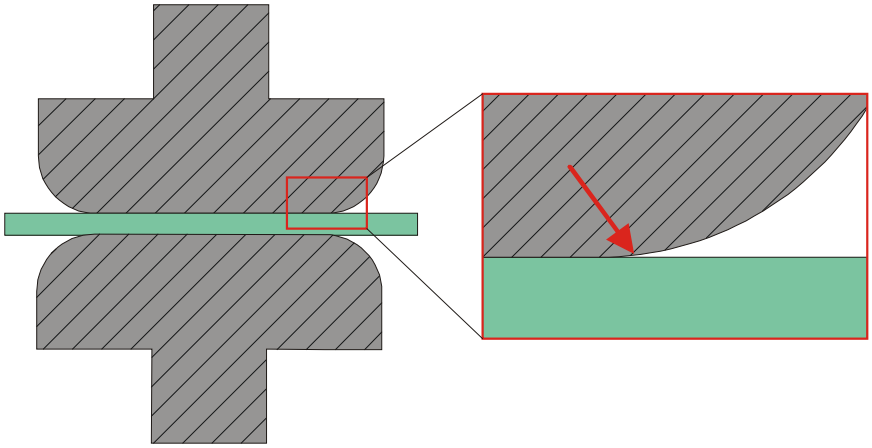


Figure 2.14 The arrow in the zoomed caption shows the high field where the applied electric field may be enhanced. The arrow points to the triple-point junction composed of the electrode radius, the SiC substrate, and encapsulant.

Chapter 3: Research Description and Analysis

3.1. Method of Approach to the Problem

The approach to the problem of improving the SiC PCSS packaging may be divided into five stages. The first stage will be to simulate the existing UMC SiC PCSS switch package to quantify the electric field enhancement produced by the package geometry. The second stage will be to use the information gathered from simulations and the literature to design a more effective package geometry. The third stage will be to select the most feasible process to use to fabricate the switch package. The fourth stage will be to develop a plan of action to produce a novel SiC PCSS package from start to finish. The fifth stage will be to implement the fabrication process (in order to show the package is obtainable by the method selected). Producing an entire package from conception to implementation is desirable; however, given the time constraints and budget of this research, only initial fabrication procedures will be attempted. The following paragraphs will describe each step in more detail.

In stage one, the UMC SiC PCSS package geometry will be mapped two-dimensionally into AutoCAD software. The 2D representation is appropriate since the PCSS is radially symmetric. The 2D model will be imported into Infolytica's ElecNet software. In ElecNet, a DC electric field will be applied across the PCSS package. ElecNet will then be used to map the electric field throughout the PCSS package. The field enhancement characteristics of the existing UMC SiC PCSS package may then be analyzed. Finally, conclusions about the relation of field enhancement to premature breakdown may then be drawn.

In stage two, various conceptual geometries will be laid out in AutoCAD then imported into ElecNet for simulating. Equivalent fields from stage one will be applied to the conceptual PCSS package geometries for comparison purposes. The ElecNet parameterization feature will be used to adjust geometrical aspects of the packages for electric field optimization. By the end of stage two, a package geometry will be assembled that will address the problems described in Section 2.7.

In stage three, different methods of substrate processing will be considered. The processes include laser etching, ion etching, fluid jet etching, and mechanical grinding. To help determine the best process to use, trials may be simulated, outsourced or performed *in situ*. Furthermore, it is possible that a combination of processes may be required. Using multiple processes would add to the production complexity which could be refined for mass production purposes.

In stage four, the research and simulations from previous stages will be evaluated and a plan of action for producing an improved PCSS package will be developed. The package will begin with a photoconductive SiC wafer section. The package should contain a port for illumination and protective insulation to guard against surface flashover. The package should be completed with some type of contacts for electrical connection to the anode and cathode.

In stage five, the method chosen to produce the package will be validated. Again, this may include outsourcing the production, fabricating custom production equipment, or a combination of both. In this stage data will be gathered and analyzed in order to give insight on how effective the production process is and recommendations on how it may be improved.

To gauge the results in each of the five stages, a method of analysis must be set for each stage. The analyses may be quantitative and/or qualitative. The following section will discuss parameters for the analysis of each stage.

3.2. **Methods of Analyzing the Results**

It is clear that the existing UMC SiC PCSS package is flawed, as described in previous work [4]. Not only does its fabrication procedure lead to localized field enhancement points, but presumably its geometry as well.

The analytical purpose of stage one is to verify that the SiC PCSS package geometry, in its purest form (i.e. perfectly aligned, no solder protrusions, perfectly bonded contacts, etc.), causes significant localized electric field enhancement. An external DC electric field, equal in magnitude to the highest field blocked by the existing SiC PCSS, will be applied to the anode-cathode. The equipotential lines will be mapped. The areas of the PCSS that exhibit field crowding will then be analyzed to determine the maximum induced field that results from the externally applied field. The maximum field intensity will be compared to the theoretical breakdown strength of SiC to determine if the breakdown strength has been exceeded. If the condition proves true, then the geometrical contribution to premature bulk breakdown is verified.

The analysis for stage two is straightforward. Conceptual PCSS geometries will endure the same stimulus as the existing PCSS in stage one. The geometries will likely be composed of substrate contours and recesses in troublesome areas to relieve large local fields. The contour and recess dimensions will be parameterized. Parameterization will expose how contour and recess size relates to the magnitude of field enhancement. The resultant trend can be analyzed by finding at what point does change in size and shape no

longer reduce field enhancement. The analysis will give insight on which processing methods may be used for fabrication.

The analysis for stage three will be done by comparing the different processing methods. First, a list of methods used for ceramic processing will be composed. Various sources will be consulted for input on the effectiveness of a method. Next, each method will be tested. The results will be analyzed using SEM microscopy. Finally each method will be ranked based on its ability to produce the geometry. The best method for producing the package geometry will be used in stage five.

Stage four does not require analysis. In this stage, a plan of action is developed for producing the PCSS package.

The analysis in stage five will be qualitative and quantitative. SEM photos will be taken following the fabrication experiments. The photos will be compared to photos of optical polished SiC PCSS substrate to determine relative surface quality. The geometry created in the substrate will be cross-sectioned and compared to the designed geometry to check for form accuracy. Depth measurements will also be performed. The triple-point junction will be examined for perpendicularity.

To analyze how the new package geometry performs, contacts will need to be deposited to form the PCSS. The PCSS will also need to be pulse charged to determine its field blocking ability. A voltage probe would measure the field applied and show at what field breakdown occurs.

3.3. **Definition of Goals**

The main goal of this work is to develop a SiC PCSS package that overcomes the existing SiC PCSS field blocking limitation of 300kV/cm. The main goal can be

disassembled into several sub-goals that this research will help strive towards in order to achieve the main goal. Using sub-goals will help clarify the research approach and lead to an organized checklist to follow. The goals are not to be confused with the three objectives discussed in Section 1.5. To clarify, the goals presented below pertain to the overall research initiative to improve the SiC PCSS. All goals may not be reached in the project presented here. The goals should be a guide for this research and future research.

Main Goal: Develop higher field blocking SiC PCSS package geometry.

Sub-Goal:
- A. Design a substrate geometry that reduces local fields in the SiC PCSS
- B. Determine a feasible method to produce the geometry
- C. Develop a production process that overcomes existing PCSS packaging roadblocks
- D. Produce the geometry with the method chosen
- E. Produce a polished and uniform contact interface
- F. Voltage test the package

3.4. **Results to Expect**

There are expectations tied to each sub-goal in Section 3.3. By noting the expectations of each sub-goal, surprises during the experimental phase that waste valuable time may be avoided. Also outlining expectations can lead to a more thorough preparation prior to experimentation. A thorough preparation not only saves time, but also leads to a more efficient use of the research budget.

In sub-goal A, the localized field in the existing SiC PCSS is expected to occur where the mismatch in permittivity exists at an acute interface angle. Contouring the

substrate at this area is expected to spread out stored charges and thus minimize the local electric field. The contour must be an interface that involves only two permittivities. Anywhere that a triple-point junction occurs should be in an area of relatively lower induced field.

In sub-goal B, it is expected that the ideal method of producing the substrate contour that is mentioned in the previous paragraph will involve plasma etching. It is also expected that the resources and effort needed to accomplish a viable etching protocol exceed what is available for this study. Mechanical processing methods are expected to be more feasible and reasonable to pursue.

In sub-goal C, it is expected that the production process will require specific steps to overcome the problems from Section 2.7. One specific step must involve polishing the interface between the contact and the substrate since the interface is expected to contribute to premature breakdown. It is also expected the production process developed may not be optimal for mass production due to its foreseeable complexity.

Work towards sub-goal D is expected to uncover many unknowns to address. A majority of the research effort and time will be expended on this goal. Producing a substrate geometry that most closely matches the design from sub-goal A is expected to be the most difficult part of the research. Sub-goal E should be easier to reach than D since a variety of polishing methods have been developed for use in optics. Reaching Sub-goal F is the only way to determine if the main goal was achieved. It is expected that improvements will be made to field blocking performance of the SiC PCSS. The degree of improvement is expected to hinge on the level of accuracy and quality in the pursuit of sub-goal D and E.

Chapter 4: Experimental Simulations and Arrangements

4.1. **Stage One: Simulations on the UMC SiC PCSS**

Simulation Setup

Simulations were first performed on the existing SiC PCSS geometry developed by UMC and tested at LLNL. The field enhancement of the package can be determined by simulating the PCSS under an applied field.

The existing SiC PCSS geometry was first mapped into AutoCAD 2000. Since the PCSS is radially symmetric, a two-dimensional representation may be used with the z-axis acting as the axis of symmetry (Figure 4.1). The AutoCAD design was imported into Infolytica's ElecNet electric field simulation package. The UMC electrode has an approximate radius of 1mm and is soldered directly on a flat, unmodified SiC substrate. The SiC substrate has a thickness of 450μm. A voltage of 10.5kV DC was applied to the anode and cathode to create a 300kV/cm electric field through the SiC substrate. Previous studies found that premature breakdown occurred at 300kV/cm in the UMC switch package [4]. Therefore, a 300kV/cm electric field was applied to verify performance limitations due to field enhancement. Two encapsulant materials were simulated. The first encapsulant material simulated was air to demonstrate incomplete encapsulation that results from applying high permittivity material. High permittivity material encapsulation (ε_r=100) was then simulated to determine whether perfect encapsulation helps prevent localized field enhancement at the triple-point junction.

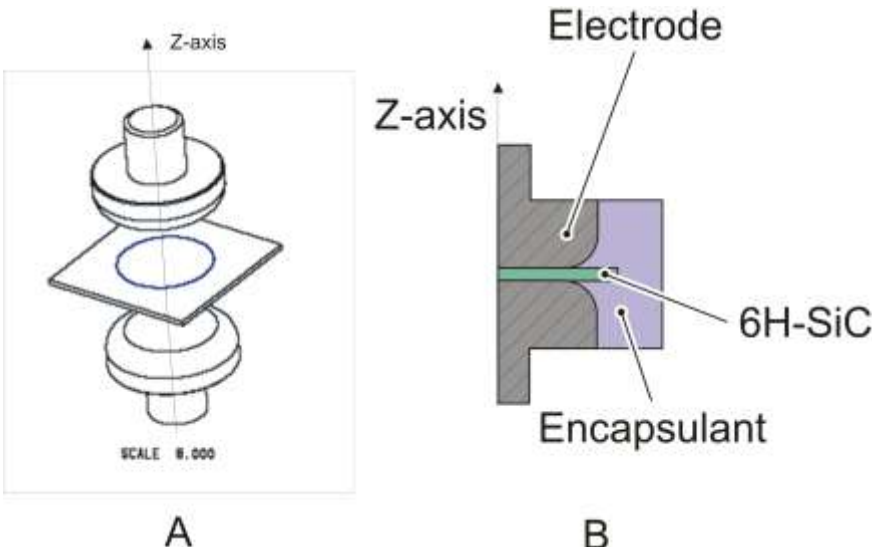


Figure 4.1 3D representation of the SiC PCSS (A). 2D representation produced in AutoCAD for simulation purposes (B).

Simulation Results and Conclusion

The existing SiC PCSS package showed significant field enhancement at the triple-point junction, that is, the point where the electrode the SiC, substrate and encapsulant interface (Figure 4.2). Figure 4.3 illustrates the crowding the equipotential lines at the interface; the electric field is at its maximum intensity at 3.4MV/cm when air is the encapsulant. The maximum intensity when reduce to 1.3MV/cm by using a high permittivity material as the encapsulant, assuming complete encapsulation. Since the applied electric field of 300kV/cm is enhanced to an intensity that exceeds the theoretical breakdown strength of SiC (3MV/cm), bulk breakdown occurs prematurely.

Several conclusions can be made from the simulation results. Premature PCSS bulk break down arises primarily from electric field enhancement at the SiC-electrode-encapsulant interface. The electrode geometry is the main cause of the enhanced field since simulations used perfect contact alignment, complete contact bonding, and no

solder protrusions, and complete encapsulation. The electrode geometry must therefore be modified to improve SiC PCSS performance by making the value of E_{op} approach E_{cr} (See Section 1.3).

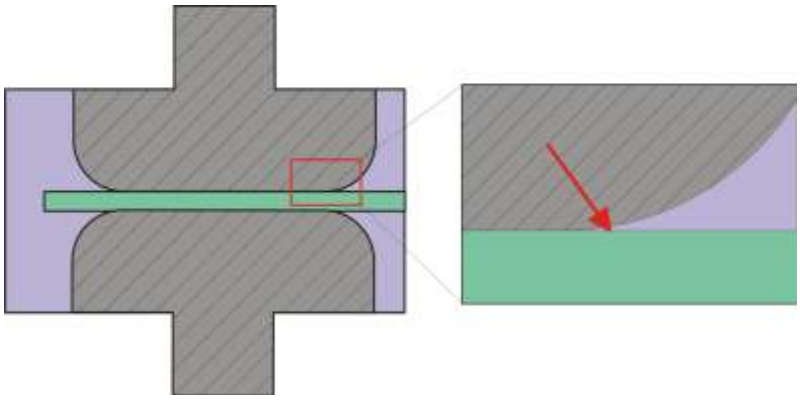


Figure 4.2 The arrow points to the location of maximum field enhancement.

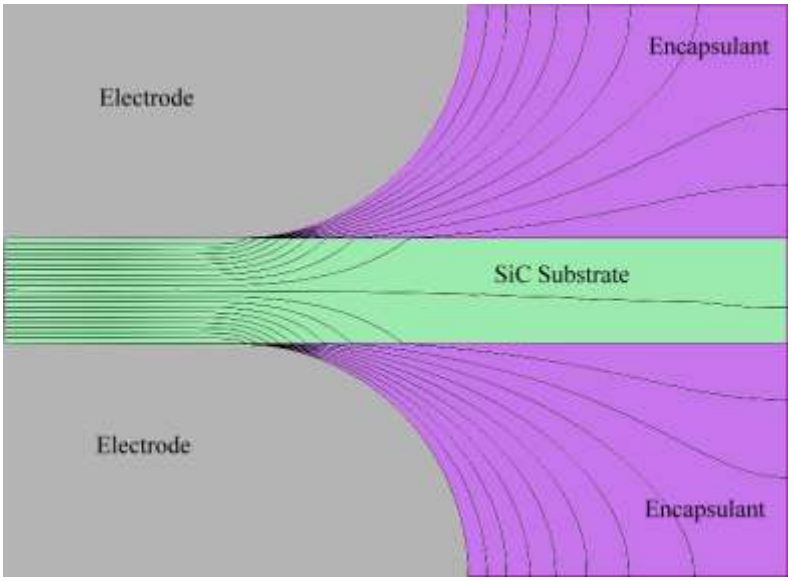


Figure 4.3 The high field enhancement location for UMC SiC PCSS geometry is shown by the crowded equipotential lines. The applied field is 300kV/cm. The electric field enhancement exceeds 3MV/cm at the electrode-SiC interface. (air encapsulant)

4.2. **Stage Two: Novel SiC PCSS Package and Simulations**

Techniques to lower the local electric fields in the package were brainstormed. The overall idea is to separate the triple-point junctions at the anode and cathode with more insulating material since the electric field intensity is inversely proportional to the distance it travels between anode and cathode. This must be done without losing volumetric efficiency, in other words, switch compactness. The best way accomplish this is to begin with a thicker SiC substrate and insert electrodes into the substrate. The photo-switching material serves as part of the encapsulation material. The electrodes should be inserted to a point where the gap between the electrodes is equal to h_s. By surrounding the electrodes with the photo-switching material, the problem with permittivity mismatch and interfaces in a high field location is eliminated. The triple-point junction is moved to a location of lower field intensity; furthermore, the junction can be more easily insulated and made uniform. The inserted electrodes must have a uniform radius of curvature. A curvature, or contour, on the electrode helps to uniformly distribute charges at the electrode-substrate interface, effectively reducing the field around the electrode. The package design is shown in Figure 4.4.

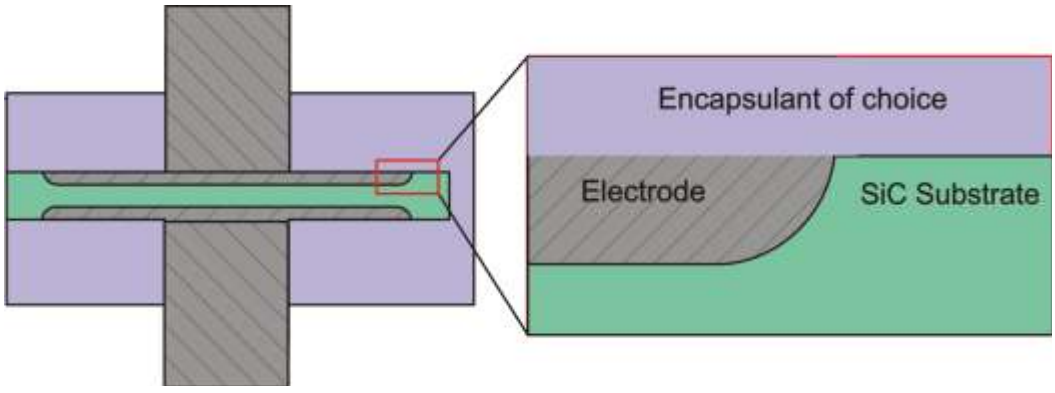


Figure 4.4 The novel SiC PCSS package using and inserted electrode configuration.

Contour Simulation Setup

The inserted electrode package (IEP) was simulated using ElecNet parameterization to determine the size of contour radius on the electrode that is required to reduce field enhancement. The SiC semiconducting substrate is given an initial thickness of 170µm. The top electrode was contoured and inserted into the substrate to a depth equal to the contour radius of the electrode. The initial radius and depth was 10µm. The contour radius was increased by 10µm up to 100µm, then increased by 100µm up to 1.5mm (Figure 4.5). The minimum distance between the electrodes remains at 150µm for every iteration, whereas the substrate thickness that surrounds the electrode is increased each iteration. Increasing the substrate thickness and contour radius together allows the entire electrode contour to remain in contact with the substrate. Furthermore, the encapsulant remains parallel to the electrode and substrate surface. The top electrode was biased each iteration with 4.5kV DC to create an electric field of 300kV/cm across the minimum substrate thickness. The bottom electrode was modeled as a mirror image of the top electrode. Air and high permittivity were used as an encapsulant in separate trials.

Contour Simulation Results and Conclusion

Table 4.1 compares the magnitude of the maximum electric field for an applied field of 300 kV/cm on the existing UMC electrode geometry and the IEP. An encapsulant of air and a material with ε_r=100 were simulated. Only the air encapsulant simulation results are shown in Table 4.1 and Figure 4.6 since the resultant electric field values were virtually the same. The field enhancement for contour

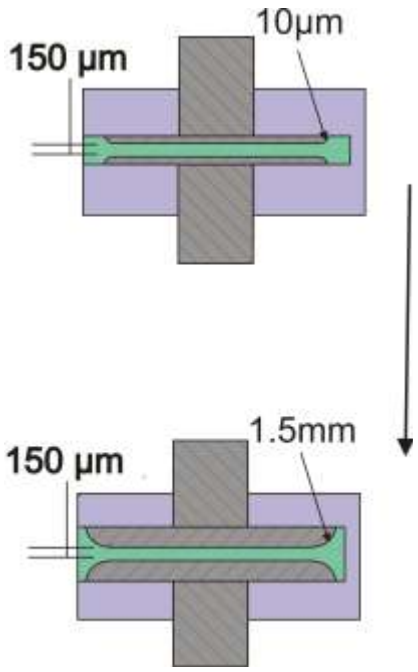


Figure 4.5 An illustration of the simulation iterations for the contour radius parameterization. The minimum distance between the two electrodes and applied field remains constant, where as the overall substrate thickness is increased.

radii greater than 90µm when using air was less than 2 percent improved as compared to the ε_r=100 material.

The electric field in the existing UMC geometry is enhanced to 3.4 kV/cm due to crowding at the triple-point junction of the electrode SiC interface. Figure 4.6 illustrates that electric field enhancement may be reduced significantly by using the IEP with a radius greater than or equal to 100µm. The reduction is less drastic when increasing the contour radius above 400µm. Furthermore, the best field enhancement reduction for any inserted electrode radius is when the triple-point of the electrode and SiC interfaces perpendicularly to the encapsulant. The perpendicular triple point also allows for a better application of high permittivity encapsulant at the junction, as opposed the acute triple-point junction of the exisiting UMC geometry. The application of high permittivity material forces the electric field away from the triple-point junction and back into the

bulk material. Although air performed slightly better for field enhancement reduction, the use of high permittivity material would offer surface flashover protection.

Table 4.1. Results of maximum induced electric fields for varying contour radii

Electrode type		**kV/cm**	**% Change**
Existing UMC geometry		3403	……
IEP (Air encapsulant)			
Radius	10μm	827.0	75.7
	20μm	576.4	30.3
	30μm	483.4	16.2
	40μm	436.0	9.8
	50μm	407.0	6.7
	60μm	388.6	4.5
	70μm	374.0	3.8
	80μm	369.5	1.2
	90 μm	357.6	3.2
	100μm	352.0	1.6
	200μm	325.3	7.6
	300μm	317.3	2.5
	400μm	312.4	1.5
	500μm	310.6	0.6
	600μm	308.9	0.6
	700μm	307.7	0.4
	800μm	306.9	0.3
	900μm	304.8	0.7
	1000μm	303.8	0.3
	1100μm	301.1	0.9
	1200μm	300.8	0.1
	1300μm	300.8	0.0
	1400μm	301.0	0.0
	1500μm	300.7	0.1

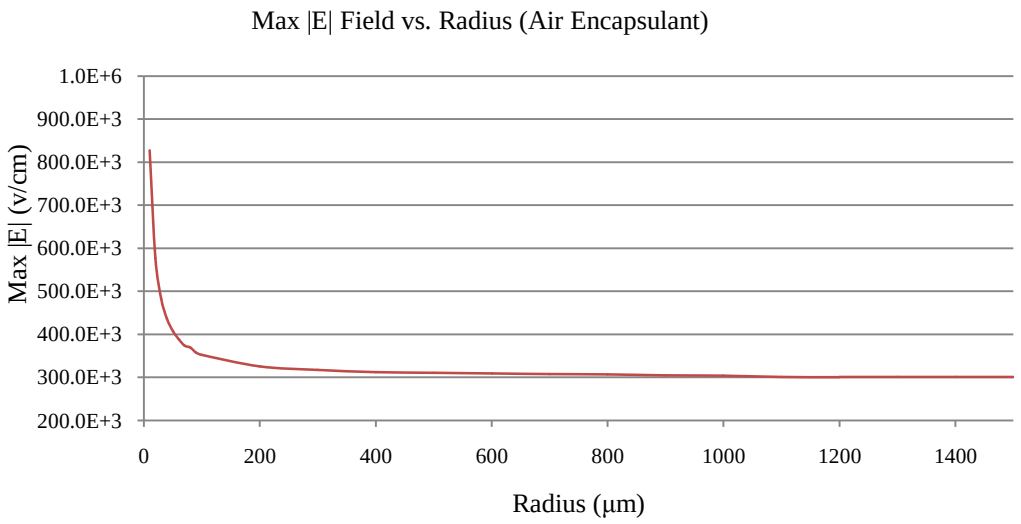


Figure 4.6 The plot shows the reduction in the maximum localized electric field verses electrode radius increase.

Simulations show that the novel package design to addresses previous SiC PCSS packaging issues. Inserting contoured eletrodes into the SiC substrate will alleviate field crowding at the SiC-electrode interface by at least one order of magnitude when employing a contour with a radius greater than 100μm. The design will also allow complete encapsulation since the acute triple-point angles are eliminated. The recessed electrode allows the substrate-ohmic contact interface to be polished and made uniform. At this point the most feasible method to produce contoured SiC substrate structure must be determined.

4.3. **Stage Three: Choosing a Method for Substrate Processing**

Several different processing methods were considered for producing the IEP for the SiC PCSS. The processes of interest include plasma/ion etching, laser milling, fluid jet polishing, and precision grinding.

Many fabrication facilities were contacted about producing our contoured geometry by using plasma, ion, and laser machining techniques [26; 27; 28; 29; 30]; all

responded negatively. Some stated that the technology was unavailable to plasma/ ion etch such a deep void (>100µm) with the 100µm radius contour in a SiC substrate without trenching. Others stated that lasering would be tedious for the required depth and could not give a consistent contour profile.

Plasma etching was investigated since it could easily be used for mass production of the geometry. Further verification of the plasma etching technique was needed, thus etching simulations were performed with collaborative effort using the SILVACO code and employing a variety of parameter configurations and masking patterns [31]. Figure 4.7 shows the etching simulation that most closely resembles the 100µm contour radius; however, without more exhaustive simulation parameterization, plasma etching the contour was not feasible to pursue at this time.

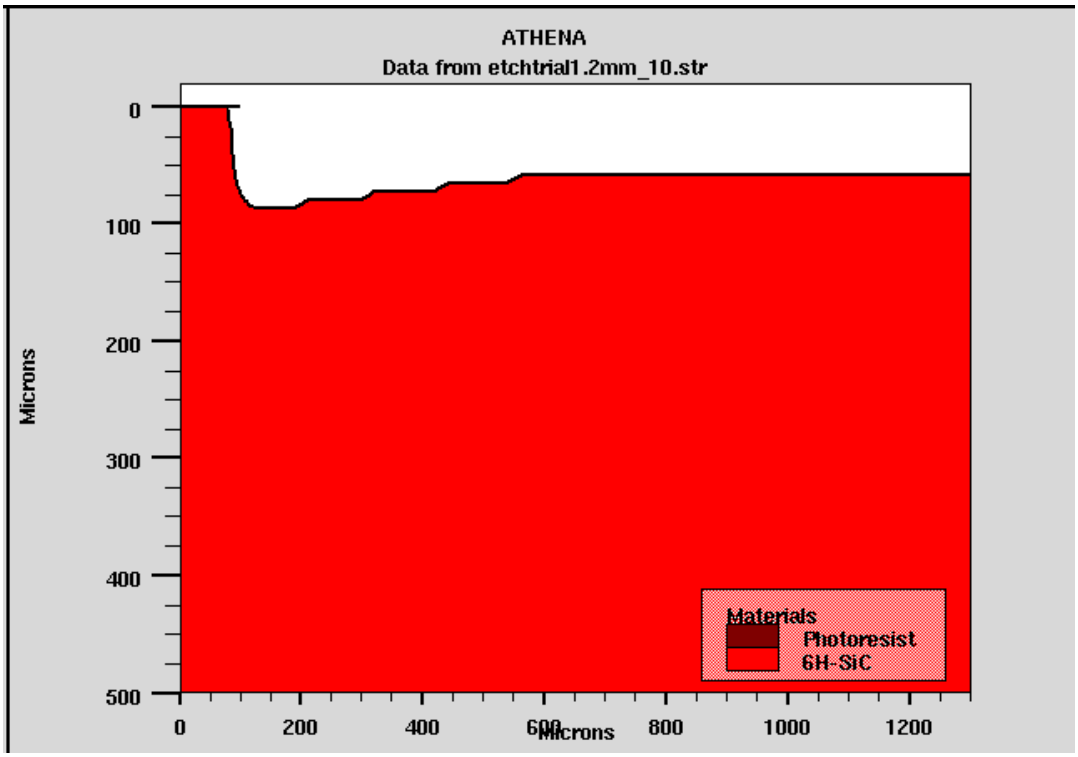
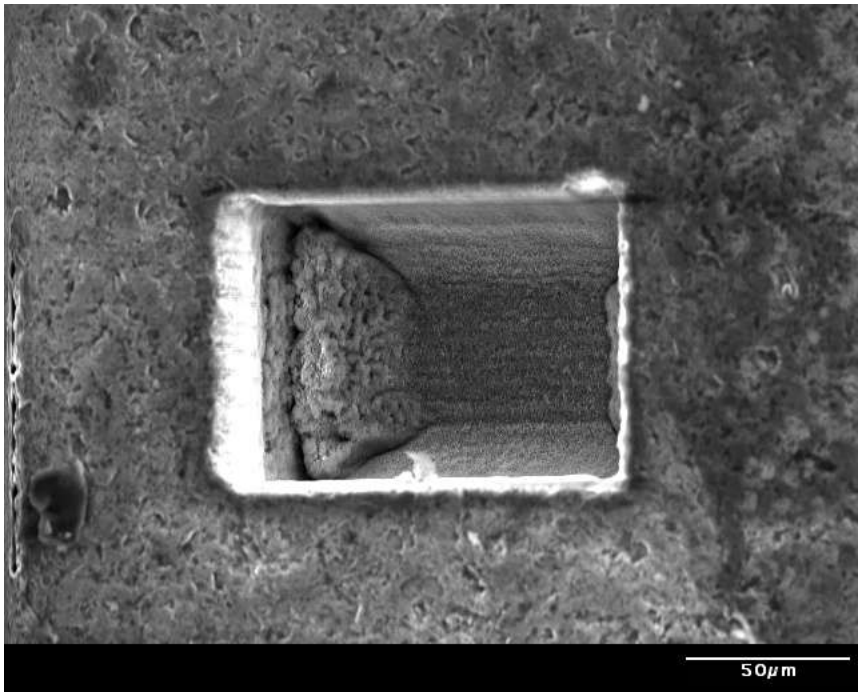


Figure 4.7 The best obtained plasma etch profile using SILVACO.

Laser machining with pulses less than 100ps can produce high precision structures in any material [32]. Machining to micron scale precision is done by removing material faster than heat can be conducted to the bulk. To achieve high accuracy and high quality surface finishes, parameters such as laser wavelength, pulse duration, pulse energy, fluence, repetition rate or scanning velocity must be adapted to the application. Furthermore to obtain controlled processing and high quality surfacing, which is needed for contour production and electric field passivation, material removal has to be monitored on-line and investigated [33]. Laser machining was tested off-site at the University of Missouri-Rolla [34]. Parameterization was therefore at the discretion of the laser operators and the process parameters used are reported in Table 4.2. An observable contour was obtained; however, the aspect ratio of the contour proved difficult to obtain. (Figure 4.8). Uniformity was lost when a circular contact contour was attempted (Figure 4.9). Overall, laser machining is a possible route for contour production and is worthy of future research.



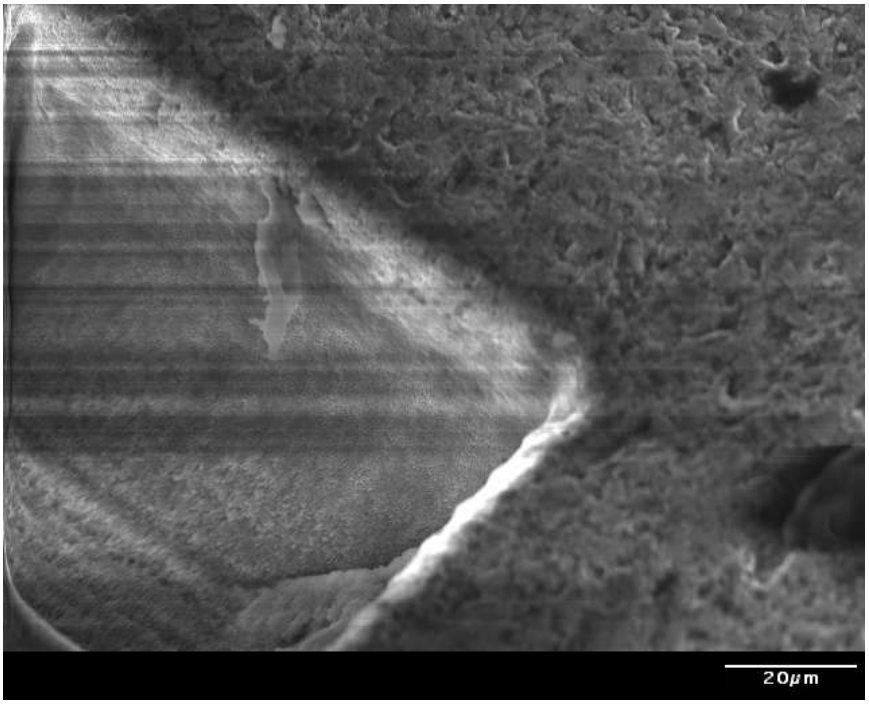


Figure 4.8 SEM images of a laser machined contour in 6H-SiC [34].

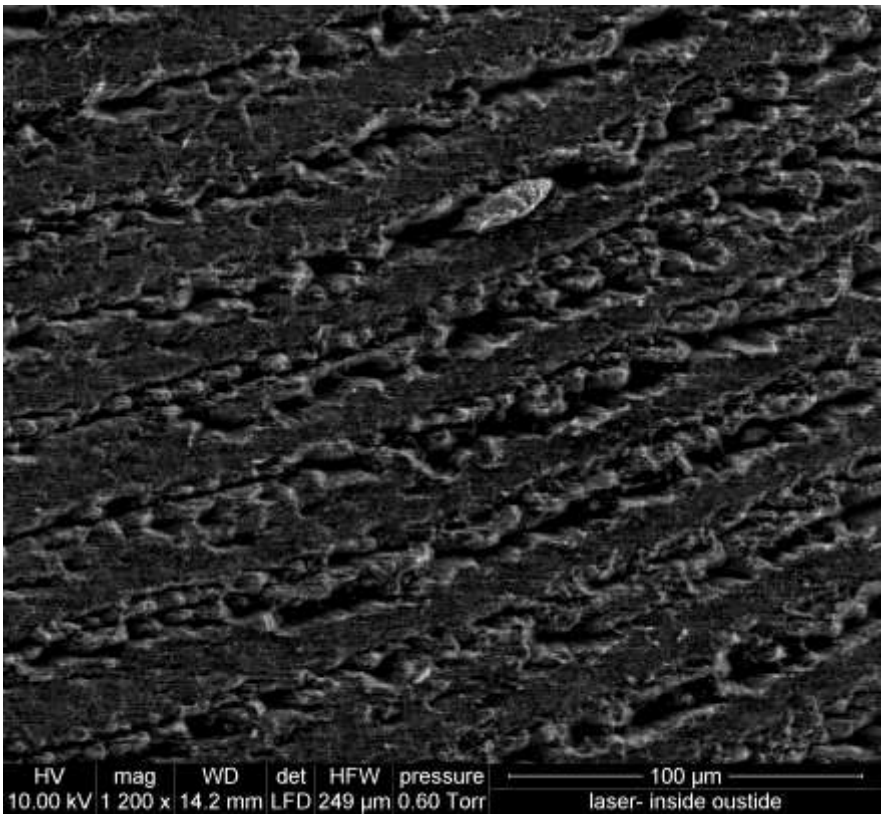


Figure 4.9 SEM images of a laser machined periodic circular void in 6H-SiC [34]

Table 4.2 Laser Machining parameters used for 6H-SiC Contouring

Laser Model	Ti:Sapphire femtosecond laser system
Wavelength	800nm
Pulse duration	120fs
Repetition rate	1 kHz
Pulse Energy	1.4μJ
Machining/processing speed	3mm/min

Table 4.3 Fluid Jet polishing parameters used for 6H-SiC Contouring

Fluid Jet Polisher Model	FJP-1150
Duration	2 hours
Slurry	Cerium oxide fluid

Fluid jet polishing is a novel process that is used for locally shaping and polishing optical surfaces of complex shapes. In fluid jet polishing, a premixed stream of abrasive slurry is projected at a surface at pressures between 0.5 to 6 bars. Fluid jet polishing was consider due to its ability to produce round pits in a glass substrate to a depth of at least 30μm with no indication of removal process degradation. Fluid jet polishing is attractive more so due to zero tool wear and cooling requirements while processing [35]. SiC substrate samples were therefore sent off-site to Lightmachinery for an attempt to produce the contour [36]. Therefore, parameterization was at the discretion of the fluid jet operators and the process parameters used are reported in Table 4.3. A before-and-after comparison is shown in Figure 4.10. The fluid jet polishing showed no contour etching on SiC due to material hardness; however, the result demonstrates that fluid jet polishing may be used for contour polishing as a final preparation step prior to contact deposition.

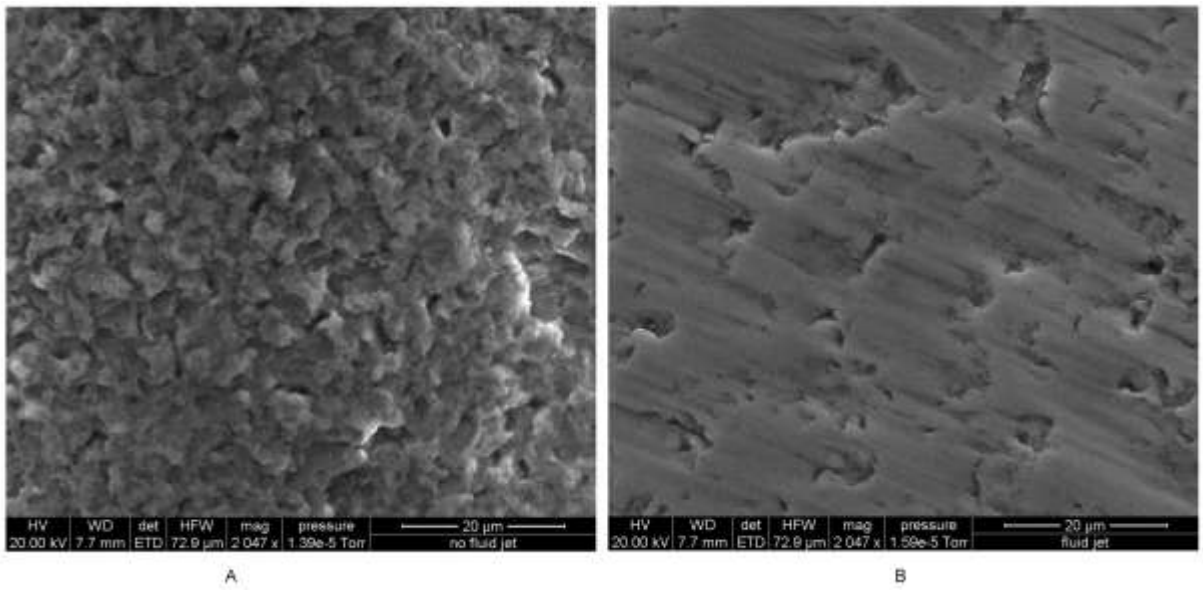


Figure 4.10 SEM images of a fluid jet contour attempt on 6H-SiC [36] (A: before, B: after).

Ceramic grinding may be used to create spherical surfaces in SiC with nanometer surface roughness and submicron form accuracy [37]. A metal-bond diamond tool is used in a rotating vertical spindle configuration. The ceramic workpiece is off set and counter-rotated to produce a consistent contour form and surface integrity. Rapid manufacturing of ceramic contours is possible since there is no need for subsequent lapping and polish with high-precision grinding. Since no off-site collaboration was available and initial grinding tests would be simple to implement and cost-effective, contour production was tested *in situ*. The grinding process was implemented using a rotating spindle, rotary table, and diamond core drill. A generic desktop drill press served as the rotating spindle. A dimple grinder used for thinning SiC substrates was altered to serve as the rotating table. A diamond core drill was designed in AutoCAD, manufactured off-site, and used as the grinding tool.

Figure 4.11 is an illustration of the custom diamond tool fabricated. Figure 4.12 shows the initial grinding setup for conceptual testing. Figure 4.13 is an SEM image of contour produced with the grinding equipment. Initial testing shows that using a grinding method to produce a contour in SiC is a viable option; however, the precision and success of contour grinding would highly depend on the quality of the tooling used.

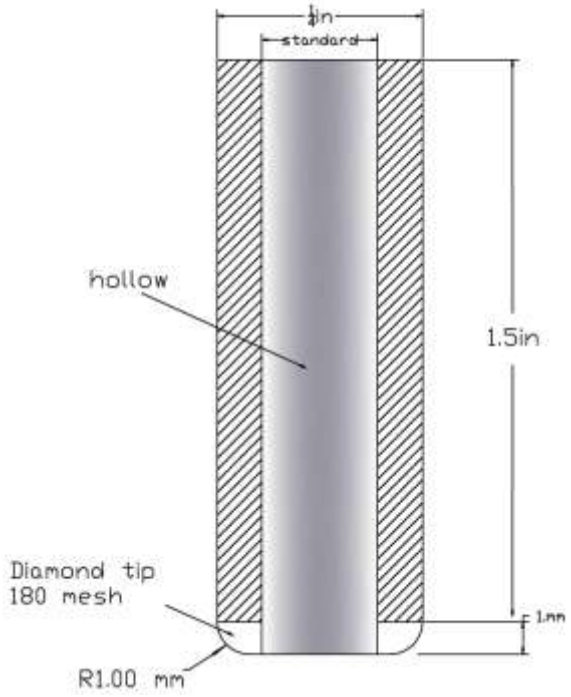


Figure 4.11 An illustration of the custom diamond tool used for contour production via grinding.

Figure 4.12 Initial grinding setup for conceptual testing.

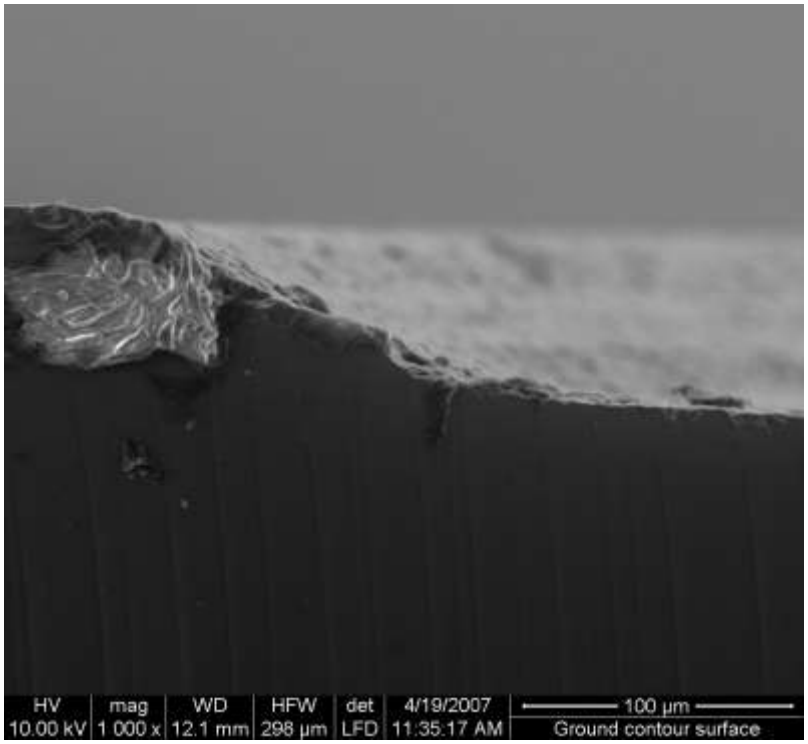


Figure 4.13 Cross-section of the first contour produced in SiC. The substrate was cleaved for examination.

Tests show that the most feasible process for producing the IEP geometry is grinding due in part to its equipment availability, low cost, and controllability. The method of grinding shall be implemented, described, and analyzed in the subsequent sections of this report.

4.4. **Stage Four: Proposed IEP Development Procedure**

A six step procedure was developed to produce the IEP. Figure 4.15 step (A) is rough diamond grinding to achieve the initial contour. It is important that the grind characteristics are of the ductile-regime grinding mode. Ceramics ground in the ductile-regime grinding mode exhibit enhanced strength and surface texture and surface quality [23].

Figure 4.15 step (B) is sub-micron to nanometer wet-type mechano-chemical polishing. A slurry of SiO_2 in a mild alkali solution has been used on Si wafers to produce strain-free, mirror-like surfaces [23]. A similar technique will be used on the SiC substrate contour .

Figure 4.15 step (C) is Electron-Cyclotron Resonance (ECR) plasma etching. ECR etching that uses H_2 or HCl/H_2 can remove polishing damages on the SiC substrate surface and contour.

Figure 4.15 step (D) is electrodepositing ohmic contacts into the contoured void. The ohmic contact consists of a deposited NiSi layer, followed by a Ti layer, a Pt layer, and a Au layer [5].

Figure 4.15 step (E) is lapping/polishing the surface at the interface between the ohmic contact and substrate. It is important that the interface be as smooth and uniform as possible. The triple-point junction should be free of contact protrusions and gaps.

Figure 4.15 step (F) is indium soldering a Cu electrode onto the ohmic contact. The electrode has a diameter which is smaller than the diameter of the ohmic contact in order to avoid solder protrusions at the triple-point junction that can affect the electric field.

The steps in Figure 4.15 show a one-sided packaging procedure; however, the opposing side of the substrate may undergo the same steps in a slightly modified manner. The use of a ground plane was considered in order to eliminate double sided substrate processing. In this case, the ground plane must be larger in diameter than the SiC substrate to account for the fringing electric field and triple-point junction. The SiC substrate edge and corner, however, would again introduce the issue of field enhancement. It is recommended that the IEP be dual sided.

Perfect contact alignment on the UMC SiC PCSS has proven difficult [4]. We have found that alignment tolerance can be increased by decreasing the diameter of one of the two contacts. For UMC's p^+-Si (SDDA) 6H-SiC junction [5], the cathode contact should be slightly smaller in diameter than the anode contact. This will lead to field enhancement around the cathode's contour and its triple-junction. When the increase in field enhancement occurs at the cathode, the p^+-n junction setup by UMC's added epi-layer is more reversed biased. Electron injection is inhibited to a greater degree than if the field enhancement occurred around the anode. Alignment of the contacts is then less critical. Simulations show that for inserted contoured contacts of 100μm radius, separated by 150μm of SiC substrate, an anode to cathode overall diameter difference of 2mm enhances the induced field intensity by 15 percent. As the contour radius is increased, the enhancement factor due to the diameter differential decreases. Simulations

show that for inserted contoured contacts of 400µm radius, separated by 150µm of SiC substrate, an anode to cathode overall diameter difference of 2mm enhances the maximum electric field intensity by only 3 percent (Figure 4.14). The increased enhancement is at the contour.

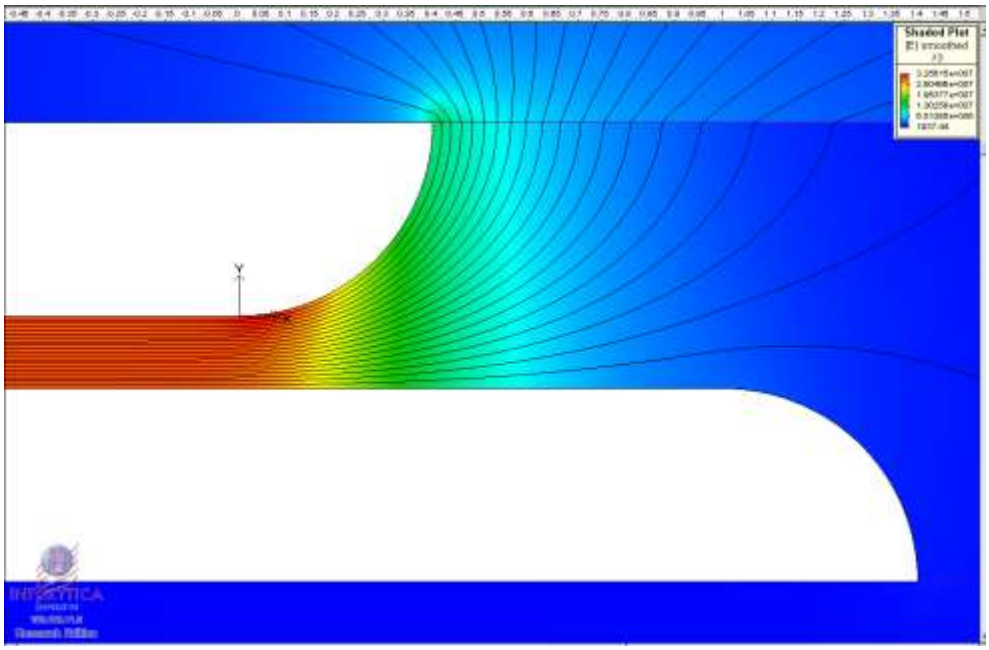


Figure 4.14 Equipotenial contour and E-field plot. 400µm contour radius with 2mm contact diameter differential.

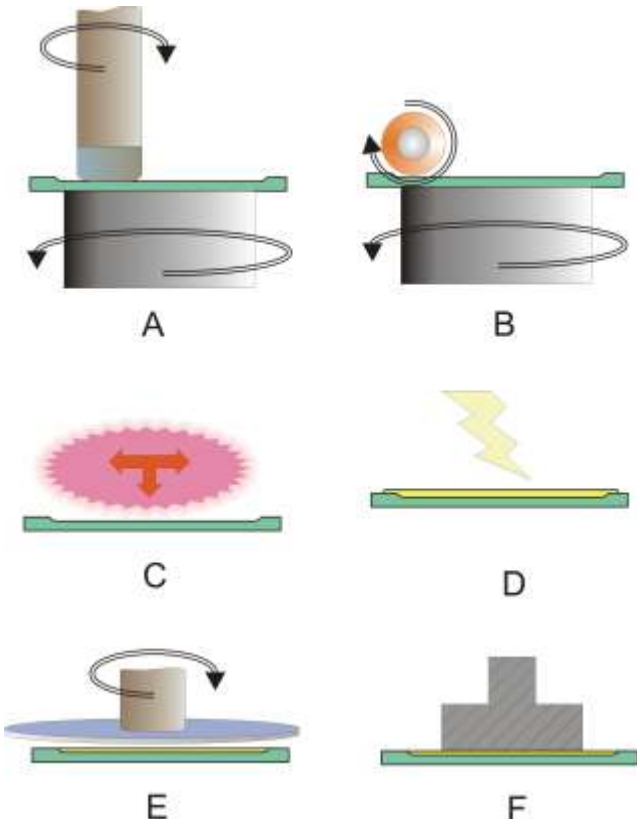


Figure 4.15 Illustration of the IEP development procedure. (A) Diamond grind the contour into the substrate. (B) Polish the ground contour with slurry. (C) Isotropic deep reactive ion etch the substrate. (D) Electrodeposit ohmic contact onto substrate. (E) Lap and polish contact and substrate interface. (F) Solder electrode onto the contact.

4.5. **Stage Five: Contour Grinding Setup**

The contour in the SiC PCSS package geometry will be produced by a ceramic grinding system. The grinding system is composed of three sub-systems: the removal system, the coolant system, and the data acquisition system (Figure 4.16). Each sub-system will be described in detail in the subsequent sections.

Removal Sub-System

The removal sub-system is based on a desktop milling machine. The X-Y positioning table of the milling machine is fitted with a hand-crank rotary table. The

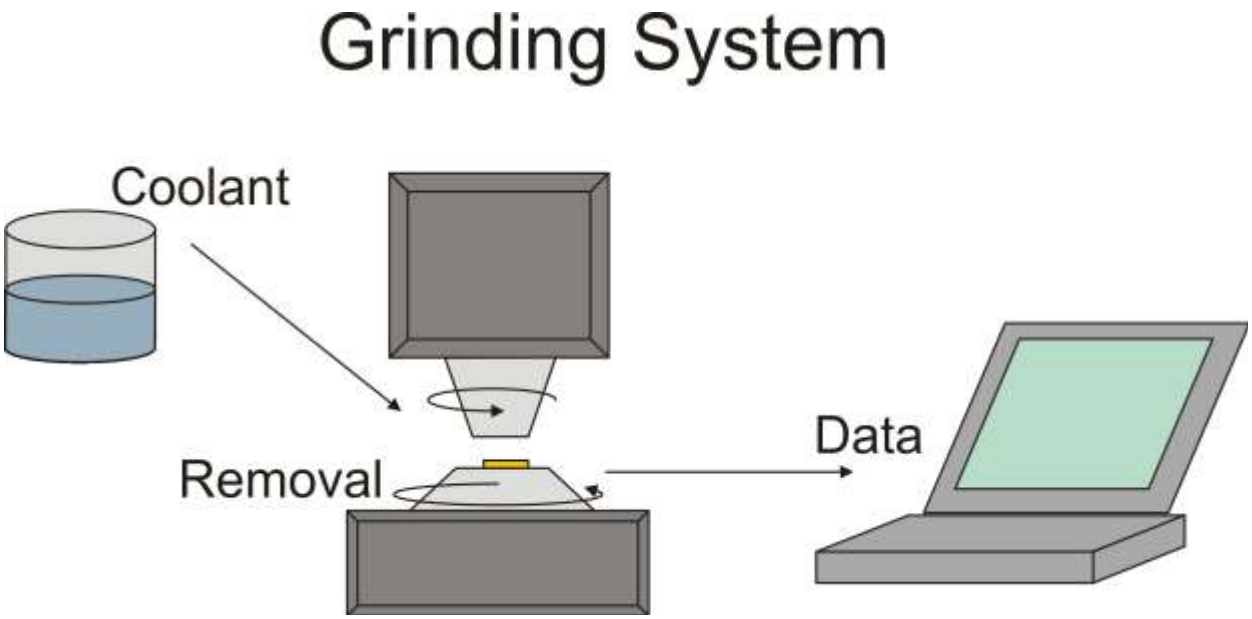


Figure 4.16 Pictorial representation of the grinding system and its sub-systems.

rotary table is made motorized by using a variable speed motor and a drive belt. The workpiece is mounted to the face of a spline shaft that travels concentrically through the center hole of the rotary table. The spline shaft is supported by a linear rotary bearing that is fixed to the rotary table. The linear rotary bearing allows the transfer of torque to the shaft while allowing the shaft to travel linearly. The torque allows the workpiece to be rotated during grinding. Linear travel allows the grinding force to be measured by a load cell placed beneath the shaft. The load cell is coupled to the shaft by a thrust bearing to allow the load cell to remain stationary while the shaft is rotated. The grinding force from the tool may be decomposed into a normal force and tangential force component. The normal force component is provided by gravity via a counter weight. The tangential force component is provided by torque. The workpiece is submerged in a continuous flow coolant bath. The workpiece is rotated counter-clockwise by the spline shaft whereas the tool is rotated clock-wise by the spindle.

The desktop mill required modification to be able to grind with a constant normal force. Prior to modification, a quill was used to adjust the height of the headstock via a toothed track. The quill was spring loaded to counter the weight of the headstock in order hold the headstock in any position along its track. Therefore in order to apply grinding force to the workpiece one must manually apply force to the operating lever of the headstock. To be able to grind using gravitation force alone, the lever was disengaged by removing the toothed track and counter-weight spring. The headstock was counter weighted using a custom pulley system with a bucket filled with lead shot. The downward force of the headstock, and consequently the diamond tool, could be adjusted by adding lead shot to the bucket to decrease grinding force or removing lead shot from the bucket to increase grinding force (Figure 4.18). The gib on the head stock was loosened and lubricated with graphite to reduce friction encountered by the free sliding headstock.

The metal-bond diamond tool was designed to produce a contoured void in SiC. The radius of the contour in the void should be 200μm. The final cut depth of the tool should be 200 μm as well. The contour radius will therefore have a one-to-one aspect ratio. Eccentric grinding will also be used. The axis of rotation of the workpiece and the axis of rotation of the spindle will be offset by 2mm (Figure 4.19). The result is to be a void in the SiC that measures approximately 10.35mm in diameter. The desired void is diagramed in Figure 4.20. Only one side of the substrate will be processed in this research.

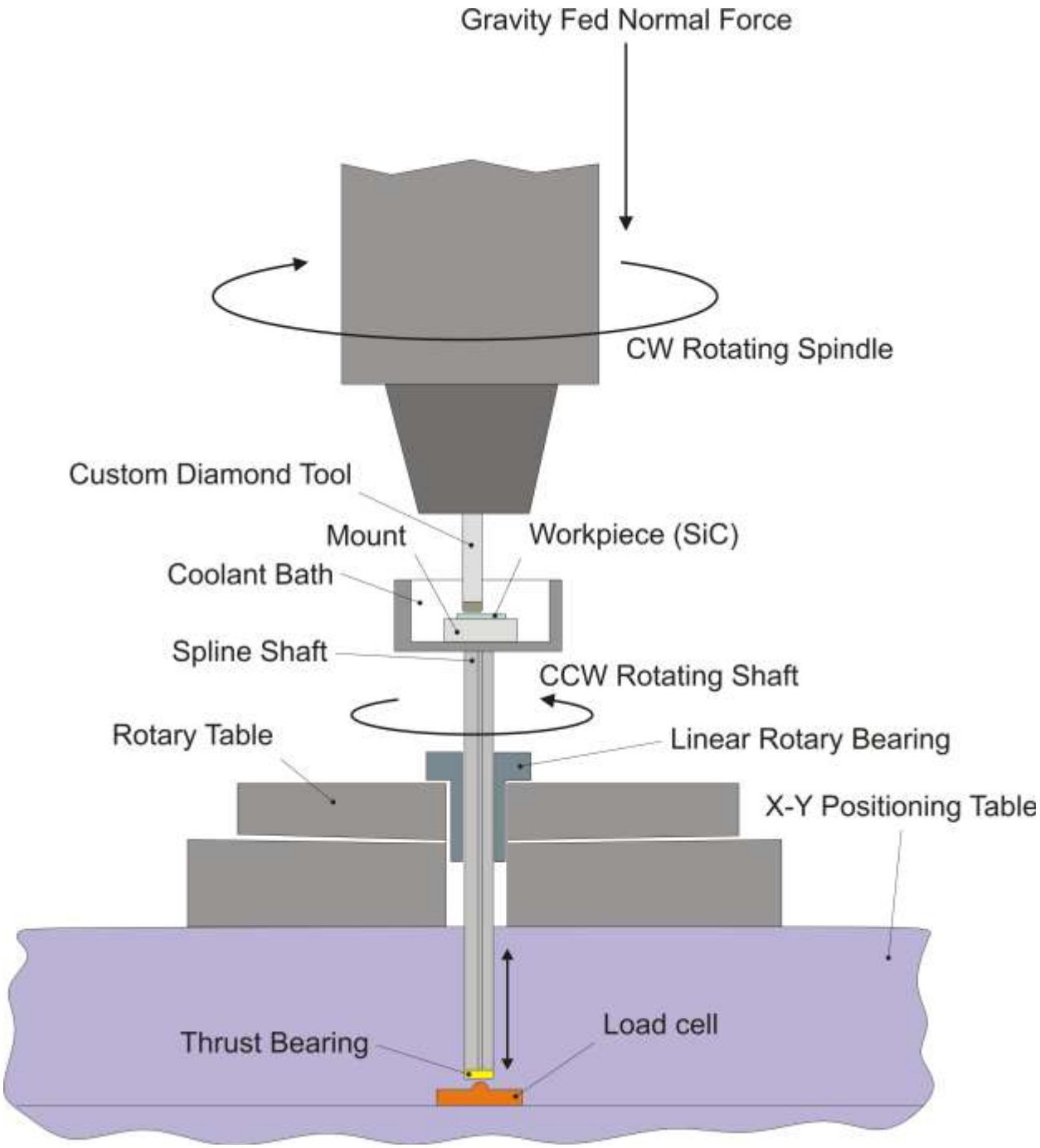


Figure 4.17 A diagram of the removal sub-system.

The tool was designed in AutoCAD and is shown in Figure 4.21. The slot in the tool allows coolant and chips to flow through and away from the tool. Three tools of each diamond grit size were fabricated. The grit sizes are 20µm, 15µm, 10µm, and 5µm. Each

tool was examined using SEM techniques to determine actual dimensions (Figure 4.22). The actual tool radii measurements ranged from approximately 320µm to 450µm; however, the important parameter of the tool is the aspect ratio of the radius contour, not necessarily its size. The aspect ratio, determined by rough SEM measurements, was very close to one-to-one for all the tools fabricated. All tolerances were considered acceptable. The tip of the tool was made hollow to allow for a smaller range of tangential speeds for all diamond contact points. If diamond were located close to the axis of rotation of the tool, their tangential speed would approach zero. A smaller variation of tangential speeds of contact points correlates to a more uniform surface finish. The tool diameter was chosen to be ¼" (6.35mm) to match end-mill standards. A collet will be used to couple the diamond tool to the spindle. Using a collet to seat a tool is more accurate than the 3-jaw chuck that was provided with the desktop-mill.

The SiC PCSS material to be processed was purchased from Intrinsic. The material arrived in wafer form with specifications described in Table 4.5. The 2" wafers were cleaved into 20 square substrates with sides measuring 1.25cm. A substrate will be adhered to the mount shown in Figure 4.17 using melted jewelers wax around the outside edges of the substrate. The outside edges are used for adhesion to allow the substrate to lie flat on the mount.

Table 4.4 Removal Sub-System Specifications

Desktop Milling Machine		
Brand	Micro-Mark Mini Mill	
Spindle Speed	0-2500	RPM
Motor	350	Watt
Voltage	110	VAC
Headstock Travel	7	Inches
X travel	8	Inches
Y travel	4	Inches
Grinding Force	0.5-10	Lbs.
Rotary Table		
Brand	Fuedura	
Diameter	4	Inches
Gear Ratio	1:72	Table:Handwheel
Motor	150, (PWM variable speed)	Watt
Rotary Speed	0-120	RPM

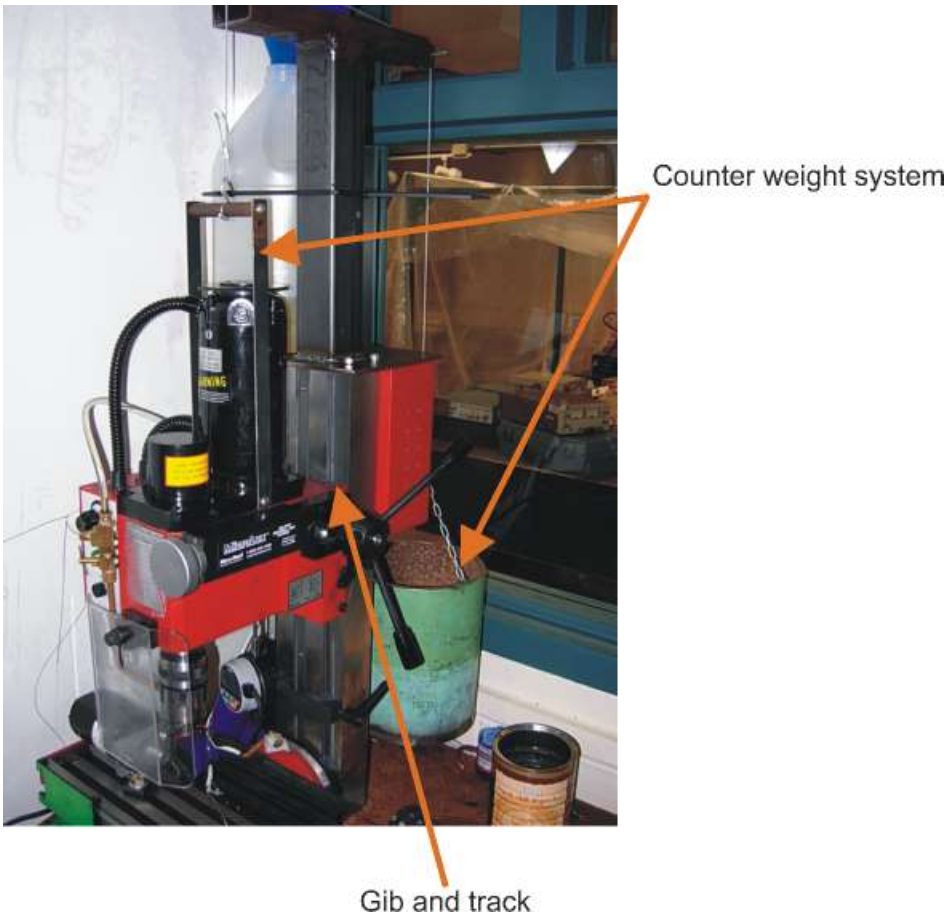


Figure 4.18 Counter weight system and the gib and track lubricated by graphite

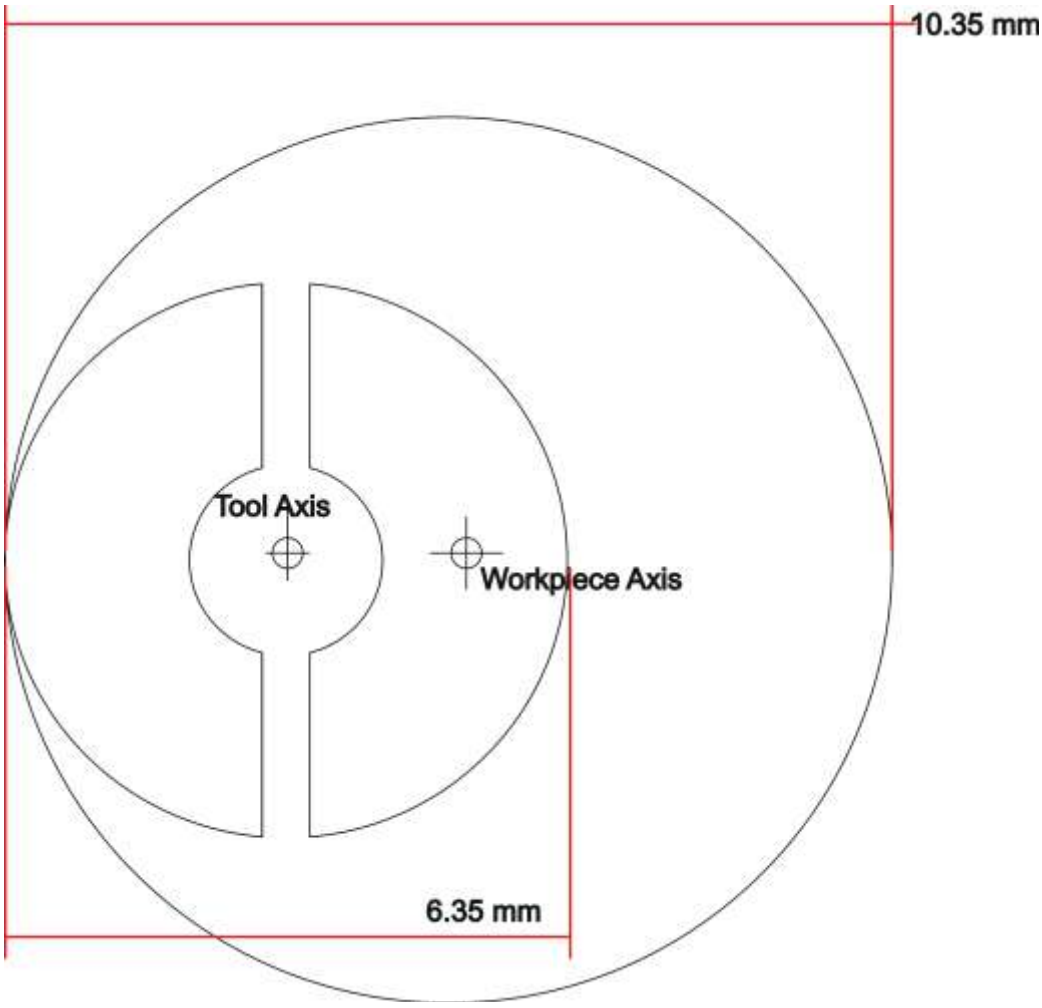


Figure 4.19 Diagram of eccentric grinding

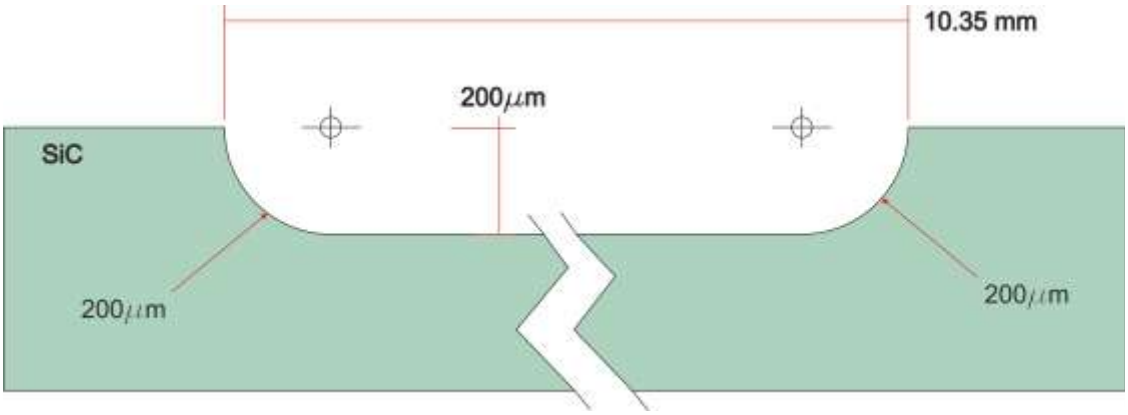


Figure 4.20 Diagram of the post-grind substrate geometry

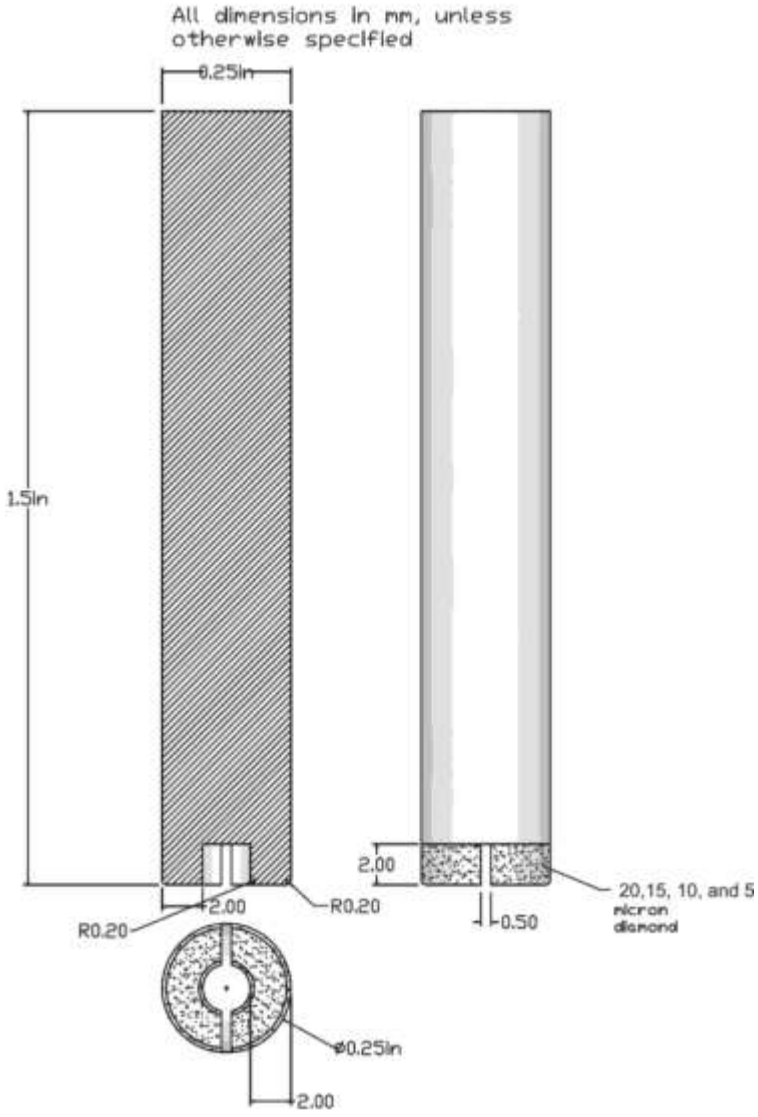


Figure 4.21 Design of custom grinding tool

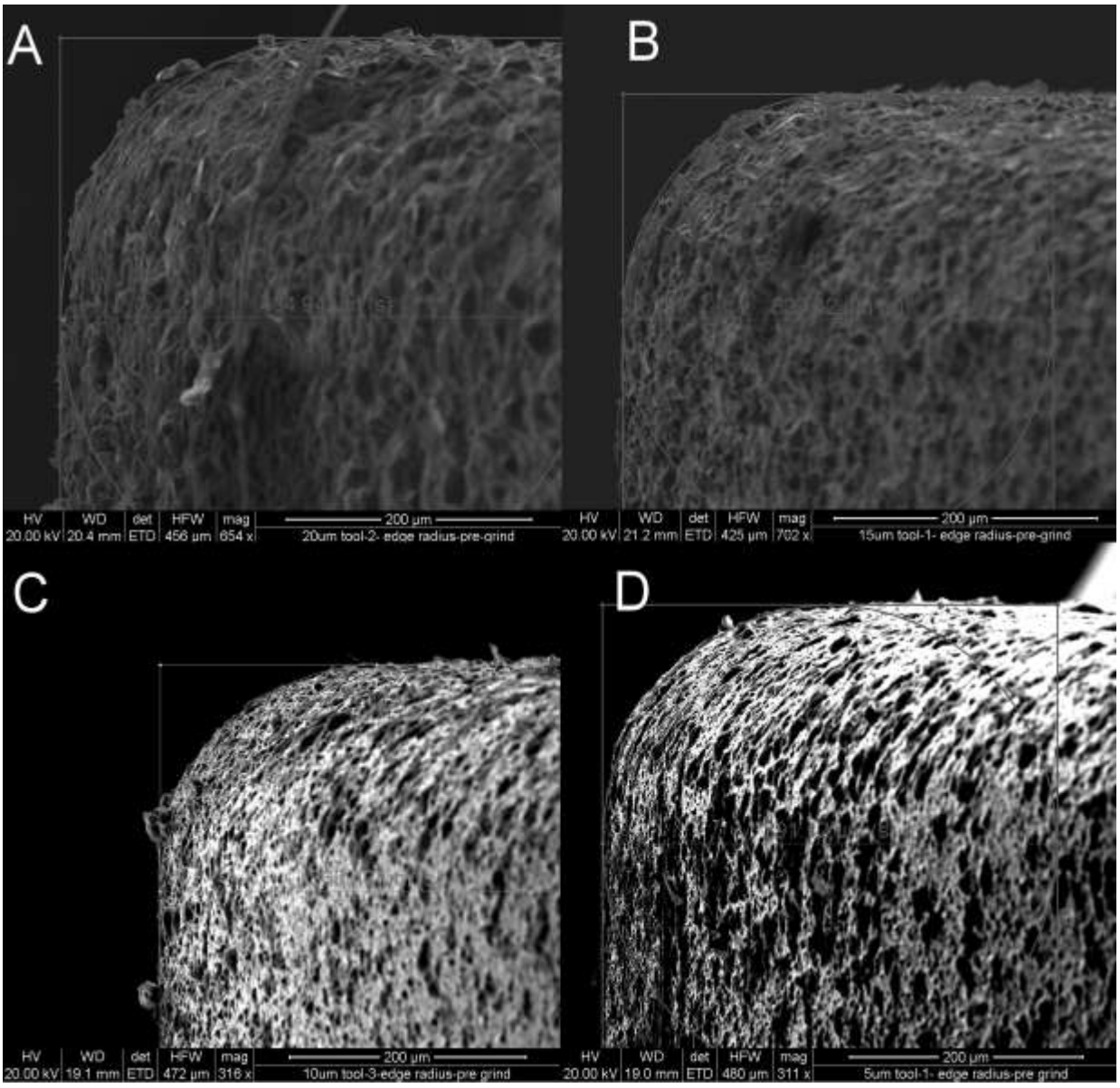


Figure 4.22 SEM images of one tool from each diamond grit category. (A) is 20 micron, (B) is 15 micron, (C) is 10 micron, (D) is 5 micron diamond grit.

Table 4.5 SiC PCSS Material Specifications

Wafer #	Desc.	Grade	Micro Pipe Density	Polytype	Diameter	Resistivity	Orientation	Thickness	Si-Face	C-Face
503088-13AA	V:SiC	B	$<100cm^2$	6H	50.8	>1e9	4.0	450µm	As Cut	As Cut

Coolant Sub-system

The tool-workpiece interface must be cooled to prolong tool life and prevent ceramic glazing. The coolant must be lubricating in nature to maximize surface quality by allowing the tool run at faster speeds without overheating. At faster speeds, tool contact forces are reduced and thus the depth of cut is reduced. Reducing the depth of cut allows material removal to occur in the ductile-grinding regime, the optimal regime for high surface quality.

The coolant used is a mixture of a light oil and kerosene at a 9:1 ratio, according to the tool manufacturer's specifications. The coolant sub-system contains a coolant bath in which the workpiece is submerged. The bath is filled by a gravity fed reservoir that holds one gallon of coolant. One tube to the bath delivers the coolant while a another tube in the bath removes it before overflow occurs. The removal tube uses suction created by an inline 12VDC pump to transport coolant away from the bath. The spent coolant is collected in a one gallon holding tank. The flow rate of the coolant is adjusted by a tee-valve that is in line with the delivery tube. The coolant sub-system is depicted in Figure 4.23. The flow rate of the coolant is not monitored.

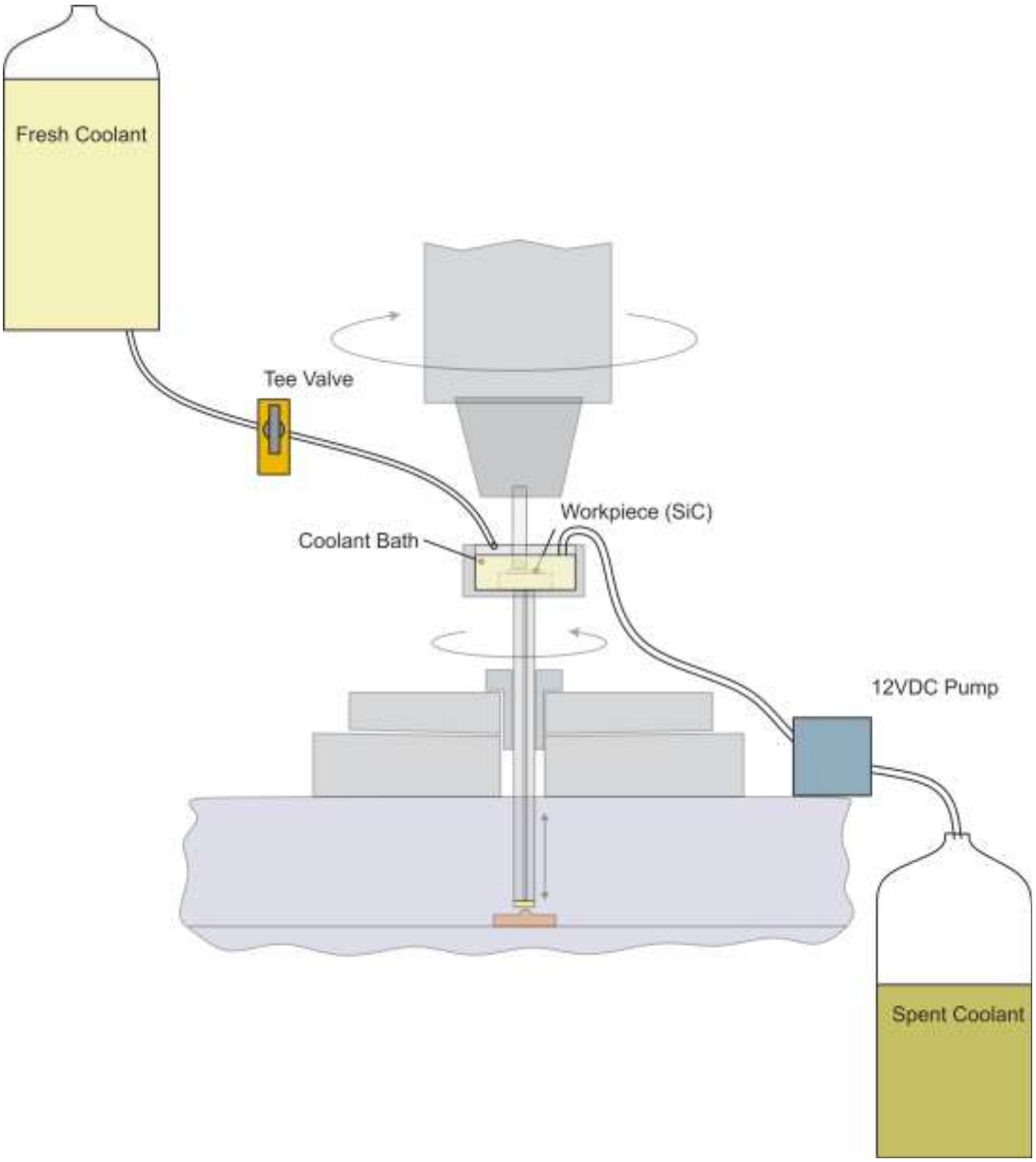
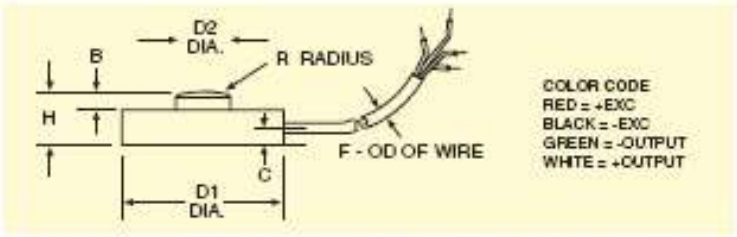


Figure 4.23 The coolant sub-system

Data Acquisition Sub-System

A method to monitor grinding progress in order to make sensible parameter adjustments and to discover trends in contour production techniques is paramount. Parameters to be monitored are normal grinding force, grind depth, spindle RPM, table RPM, and grinding time.

The normal grinding force is measured by the Omega LCKD-10 load cell. The dimensions and specifications are given in Figure 4.24 and Table 4.6. The load cell arrives calibrated but linearity was verified by loading. Due to the weight of the shaft assembly the load cell must be zeroed before use. This is done by applying a voltage on the negative output terminal that is equal and opposite of the voltage at the positive output terminal.



CAPACITY	D1	D2	H	B	C	F	R
1 kg to 50 lb	9.6 (0.38)	2.2 (0.09)	3.0 (0.12)	0.76 (0.03)	1.0 (0.04)	1.3 (0.05)	6.3 (0.25)

Figure 4.24 Load cell dimensions

Table 4.6 Load Cell Specifications

Model	Omega LCKD-10	Units
Excitation	5	V
Output	2	mV/V
Capacity	10	lbs
Full Scale Deflection	0.003	in

The grind depth is measured by a CDI Logic Basic electronic indicator (Figure 4.25). The indicator outputs a continual stream of RS232 serial data allowing a depth rate to be calculated. The indicator is mounted on the stop-bar beneath the headstock and is deflected by the vertical movement of the head stock (Figure 4.26).

Figure 4.25 CDI Logic Basic electronic indicator

Table 4.7 Electronic indicator Specifications

Electronic Indicator Model	CDI Logic Basic BG3110	Units
Range	25.4	mm
Resolution	.001	mm

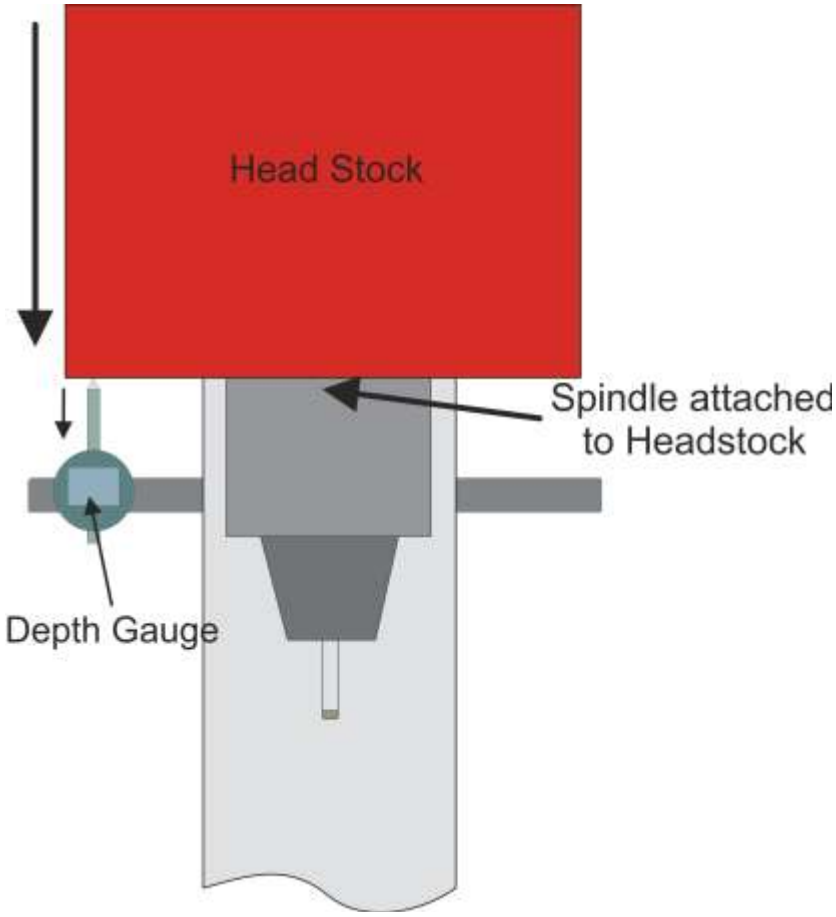


Figure 4.26 Electronic indicator (depth gauge) is deflected by downward motion of the headstock.

The spindle and table RPM are detected using hall-effect sensors (Figure 4.27). Four magnets are adhered to the spindle with a separation of 90º. A hall sensor is placed in proximity to the spinning magnets. Each time a magnet passes the hall effect sensor, the sensors output changes from logic high to logic low. The changes are counted during a known time interval and converted to RPM. The same principle is used for to measure

the rotary table RPM, except that 6 magnets are adhered to the table spaced 60º apart. More magnets allow the RPM to be acquired at a faster interval since the table spins relatively slow compared to the spindle.

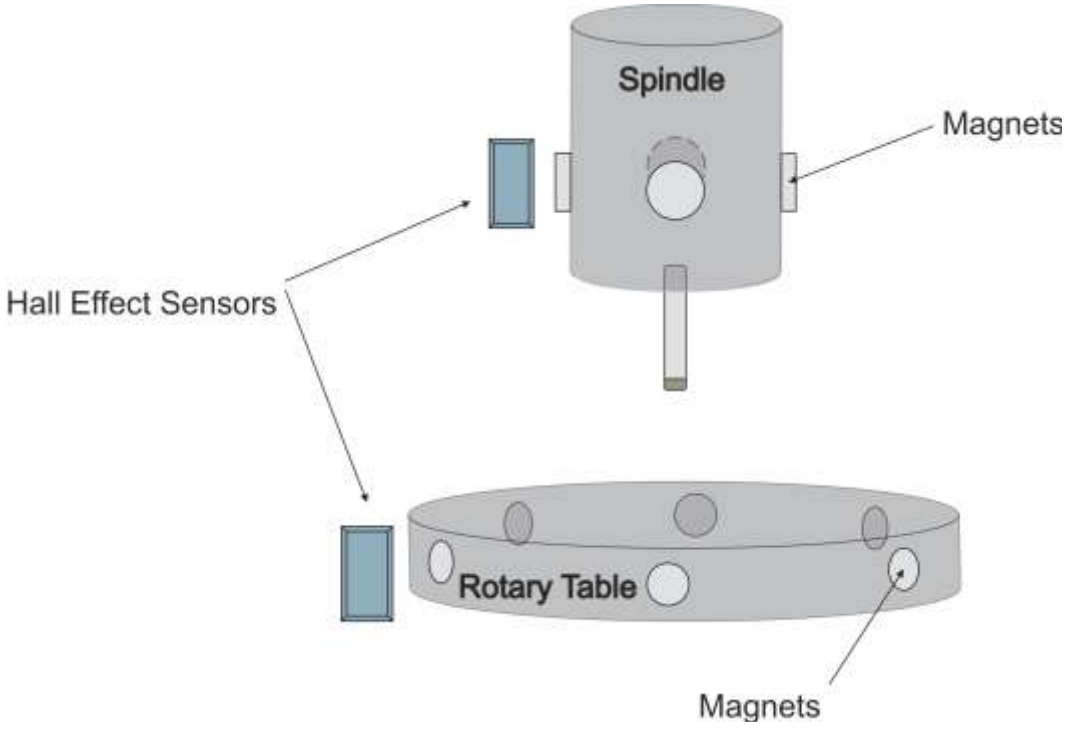


Figure 4.27 Spindle and rotary table RPM measurement diagram

All streaming data from the sensors is collected by a notebook computer running Labview 8.2. A virtual instrument (VI) was written to record sensor data and provide visual feedback of the grinding force, grinding depth, spindle and table RPM, and grinding time (Figure 4.28). Figure 4.29 shows a diagram of how the system is connected. The grind force and grinding depth are sampled at a frequency of 100Hz or every 100ms. The spindle and table RPM are sampled at a frequency of 0.143Hz or every 7 seconds. The VI front panel will be shown and discussed in the next section and an operation overview will be provided.

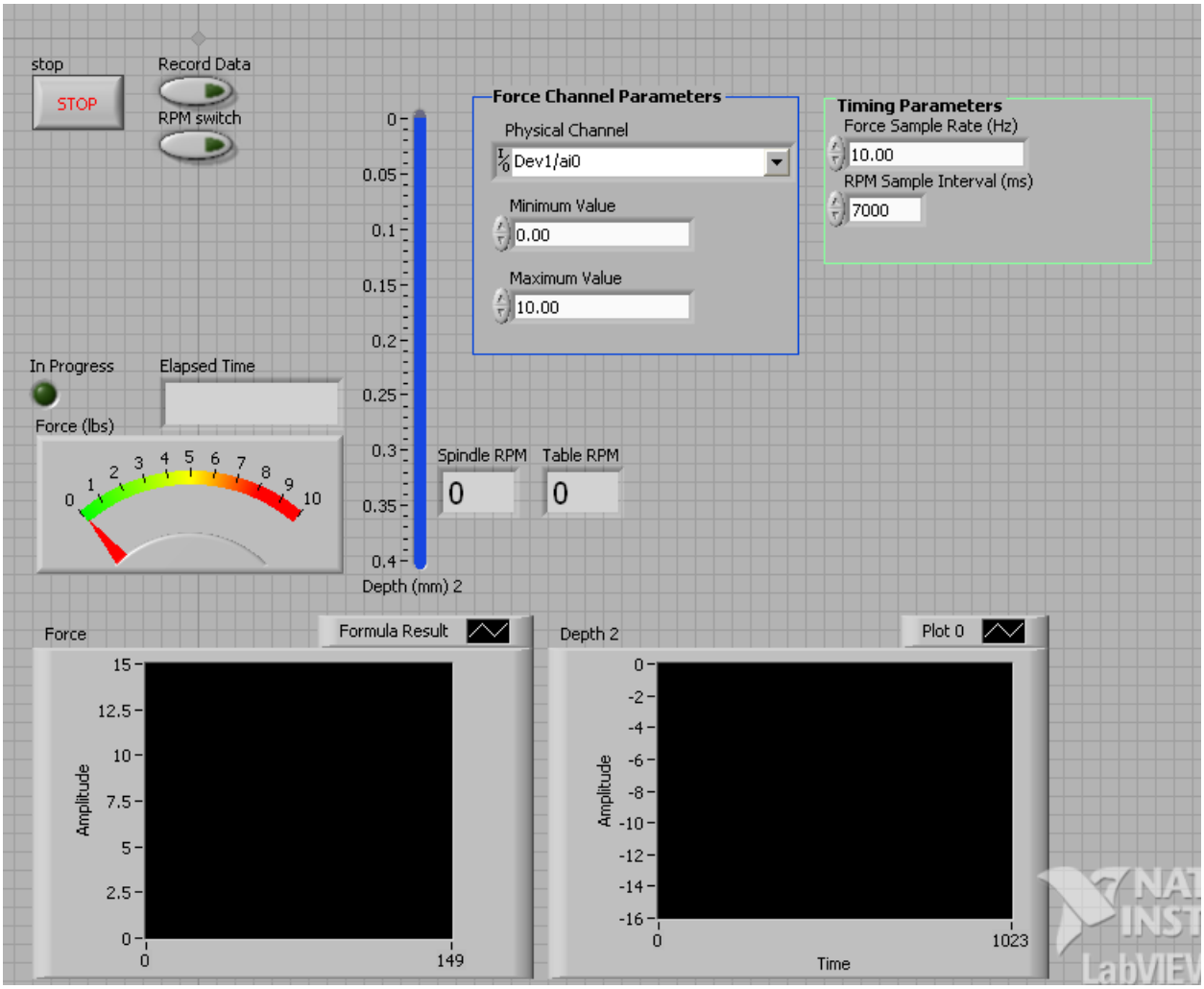


Figure 4.28 Data Acquisition Front Panel

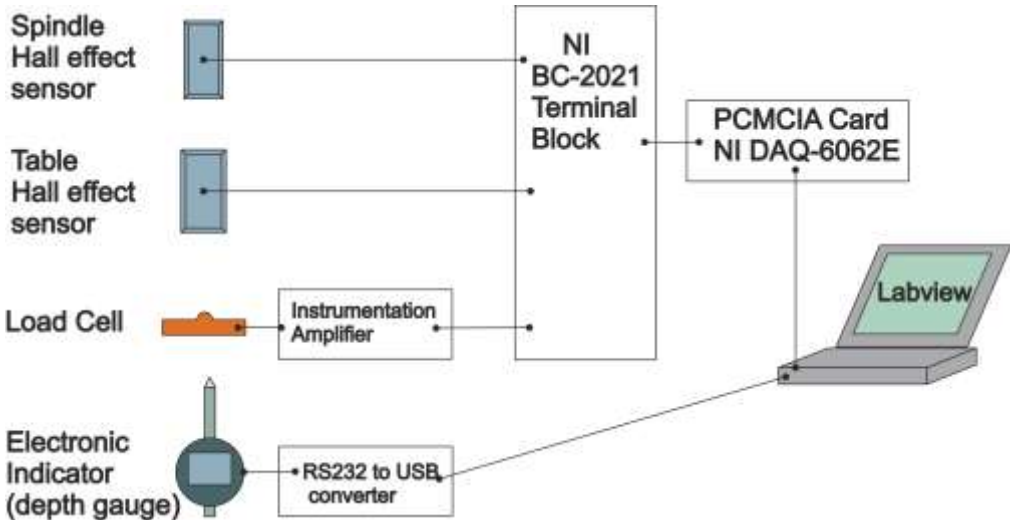


Figure 4.29 A connection diagram of the Data Sub-System.

Operating the System

Several steps must be taken to operate the system. The grind force, RPM, and substrate position are the critical parameters to set. The steps may be divided into four categories: substrate preparation, machine adjustment, code execution, and process termination.

Initially check to verify the headstock is counter-balanced to a point where the headstock has a slight positive (downward) force. This is done manually by unlocking the head stock and lifting it up and down. If no downward force is detected remove lead shot from the rear bucket. Turn on power to the load cell and coolant pump and depth gauge. Return the headstock to the up position and lock it. Clear the depth gauge.

Place the 1.2cm x 1.2cm SiC substrate on to the mount and visually center it with respect to the mount. Then place wax on four corners of the substrate. Heat the mount from below with a heat gun to melt the wax. As the wax cools, the substrate is secured for grinding. With the desired grinding tool chucked, unlock the headstock and lower it down to a position just before the tool touches the substrate and lock the headstock. Use the positioning dials on the X-Y table to center the substrate under the tool. Unlock the head stock and lower the tool onto the substrate. Rotate the table by hand to create grooves in the substrate. Adjust the X-Y table to where the pattern created on the substrate is the same width as the tool. Then, use the X-position dial to offset the tool to 2mm. Leave the tool in contact with the substrate.

Run the VI front panel with the *Record Data* button unselected and the *RPM* button selected. Set the desired grinding force by adding or removing lead shot from the bucket. Then clear the depth gauge. Raise the headstock slightly above the substrate and

lock it. Turn on the spindle and the table and adjust the dials to set the desired RPM. Finally stop the VI.

Now, select turn on the *Record Data* button and the *RPM* button should be on as well. Run the VI front panel. Turn on the coolant using the tee-valve and allow coolant bath to fill. Unlock the headstock and gently lower to down to let the tool contact the substrate. Once the depth gauge shows a positive reading, the data should display on the VI front panel.

When finished grinding, click the *Stop* button on the VI front panel. Turn off the coolant. Return the headstock the top position and lock it. Type the desired file name on the VI front panel and click *Save*.

Chapter 5: Grinding Results and Analysis

Results from simulations and process testing were reported in the previous section. This chapter presents and analyzes the results from contour grinding experimentations.

5.1. **Results**

Data was first collected on the custom diamond tools that were fabricated by UKAM. Laser profilometry used for contour profiling was unavailable during this research. The tools were therefore examined using SEM imaging to determine how closely the fabricator met the design specifications. Approximate edge radius and diamond size measurements were performed on each of the twelve tools. The diamond sizes used were indeed found to be within specification (Table 5.1). The edge radius of the tools measured, on average, to be 190μm. The slot created in the tools was twice as large as specified.

Table 5.1 Diamond tool Measurements

Diamond Size (µm)-Tool#	Edge Radius (+ or - 1µm)	
20-1	211	µm
20-2	218	µm
20-3	197	µm
15-1	170	µm
15-2	182	µm
15-3	177	µm
10-1	194	µm
10-2	198	µm
10-3	183	µm
5-1	196	µm
5-2	191	µm
5-3	175	µm
Range	54	µm
Avg	190	µm

The first grind (Grind 1) was performed with the 20-1 tool and lasted 31 minutes. The acquired data is displayed in Figure 5.1 The average removal rate was 0.04µm/sec for the SiC. The maximum spindle RPM and table RPM possible were used which were 2,438 RPM and 126 RPM, respectively. The depth was initially measured as negative. The final depth measurement detected by the depth gauge was approximately 275µm. The measurement is not only from depth into the substrate but also from diamond height lost on the tool and wax compression. The depth gauge measurements were adjusted for load cell defection. A final grind depth in to the SiC substrate was approximately 81µm (Figure 5.2). Figure 5.3 shows the surface finish in the bottom of the void.

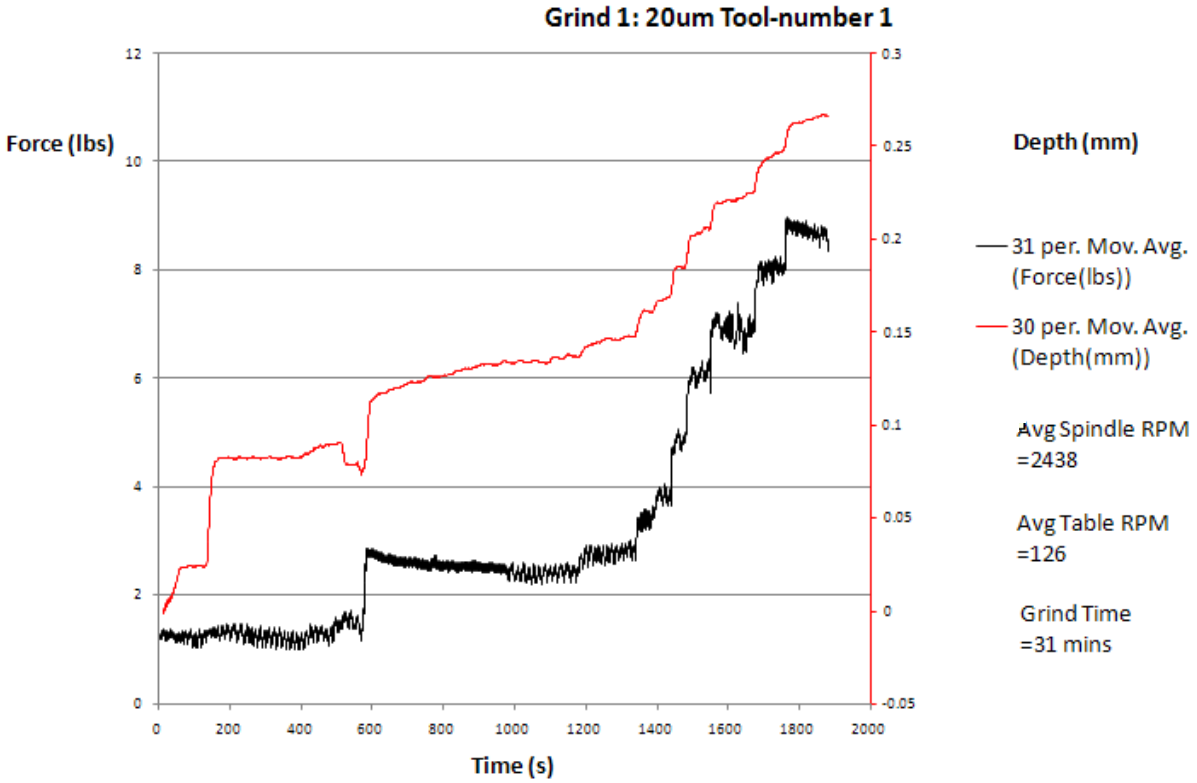


Figure 5.1 The data from Grind 1. The 20 micrometer diamond tool was used.

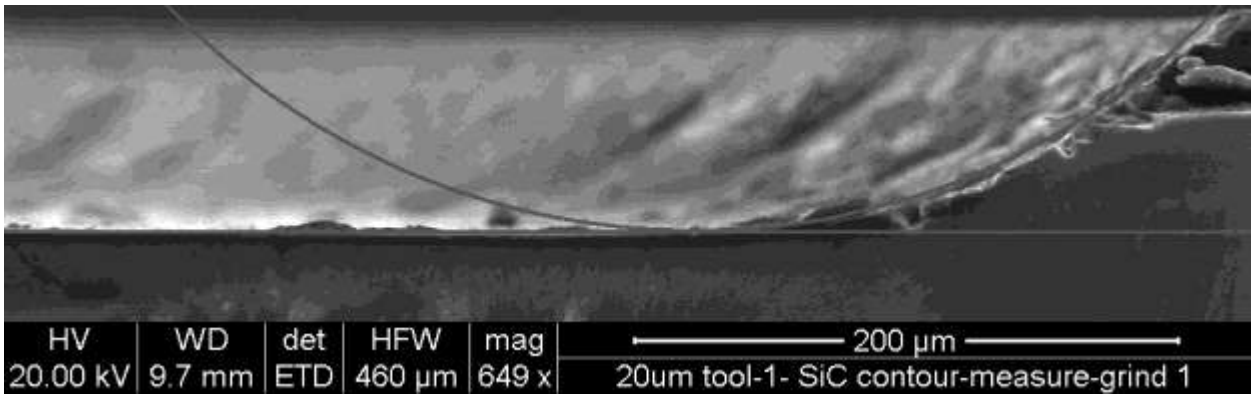


Figure 5.2 An SEM image of the contour produced from Grind 1. The depth of the grind was 81 micrometers.

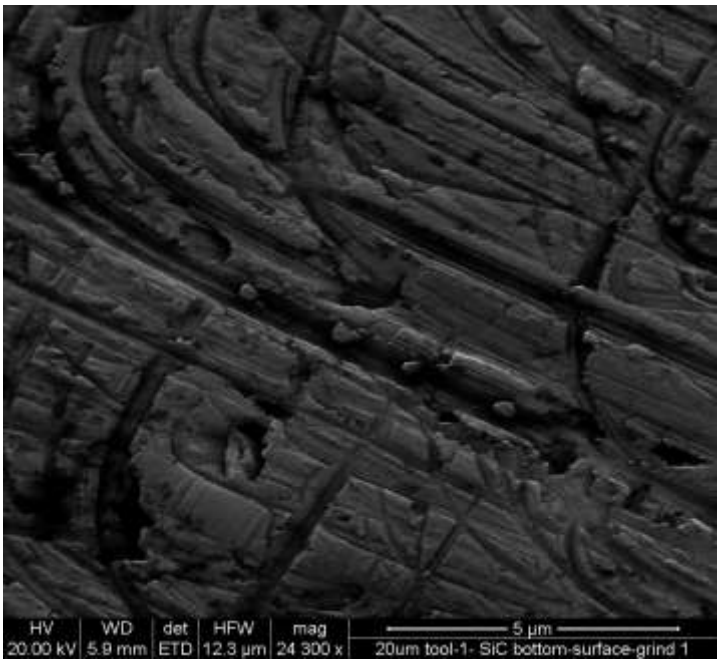


Figure 5.3 The photo shows grinding in the brittle-fracture regime for tool 20-1.

The second grind (Grind 2) was performed with the 5-2 tool and lasted 55 seconds. The acquired data is displayed in Figure 5.4. The average removal rate was 0.145 μm/sec. The maximum possible spindle RPM and table RPM was used which were 2,464 RPM and 118 RPM, respectively. The final depth measurement detected by the depth gauge was approximately 45μm. A final grind depth in to the SiC substrate was approximately 8 μm. A cleaved profile view is not shown to preserve the substrate for further processing. Figure 5.5 shows the top surface of the substrate on the left with a contour transition to the bottom of the void shown on the right.

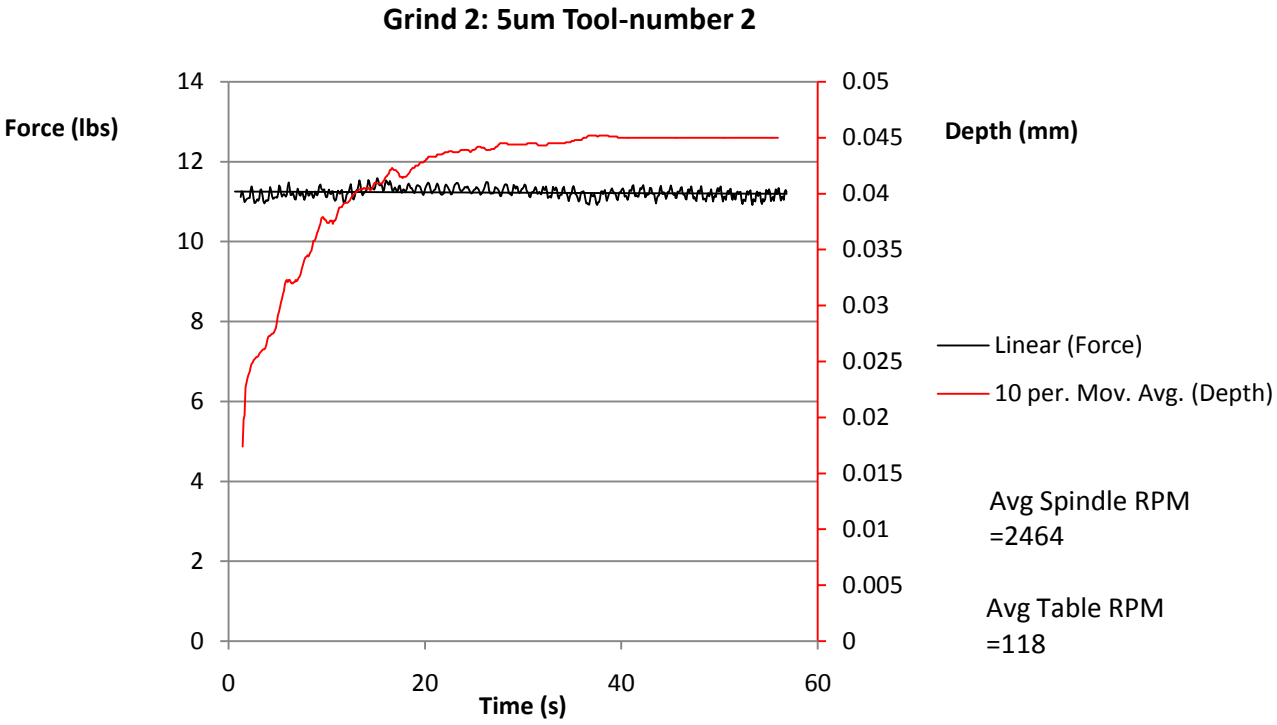


Figure 5.4 The data from Grind 2. The 5 μm tool was used.

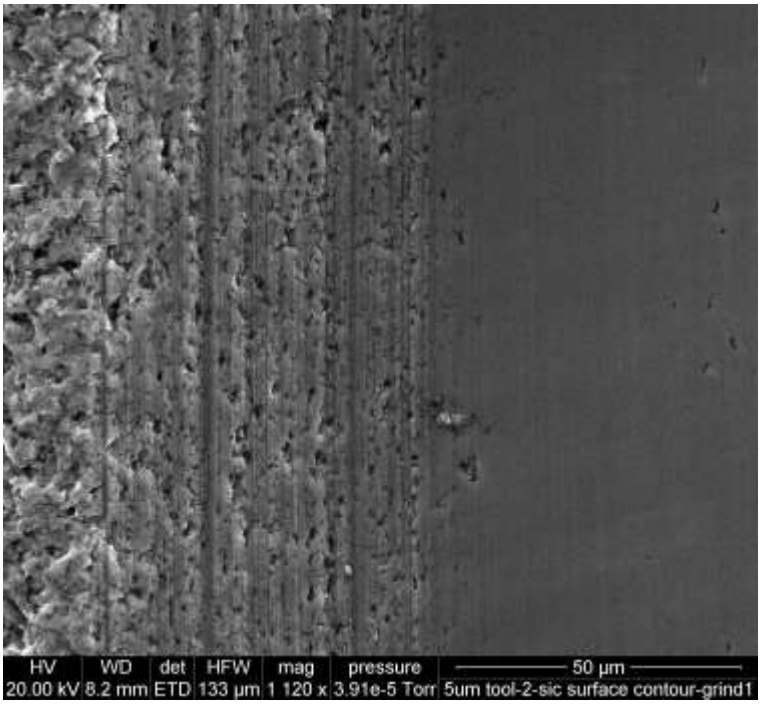


Figure 5.5 Top view of the contour from Grind 2.

The third grind (Grind 3) was performed with the 20-3 tool and lasted 53 minutes. The acquired data is displayed in Figure 5.6. The average removal rate was 0.021 µm/sec. The maximum possible spindle RPM and table RPM was used which were 2,476 RPM and 102 RPM, respectively. The final depth measurement detected by the depth gauge was approximately 180µm. A final grind depth in to the SiC substrate was approximately 69 µm. A cleaved profile view is not shown in order to preserve the substrate for further processing.

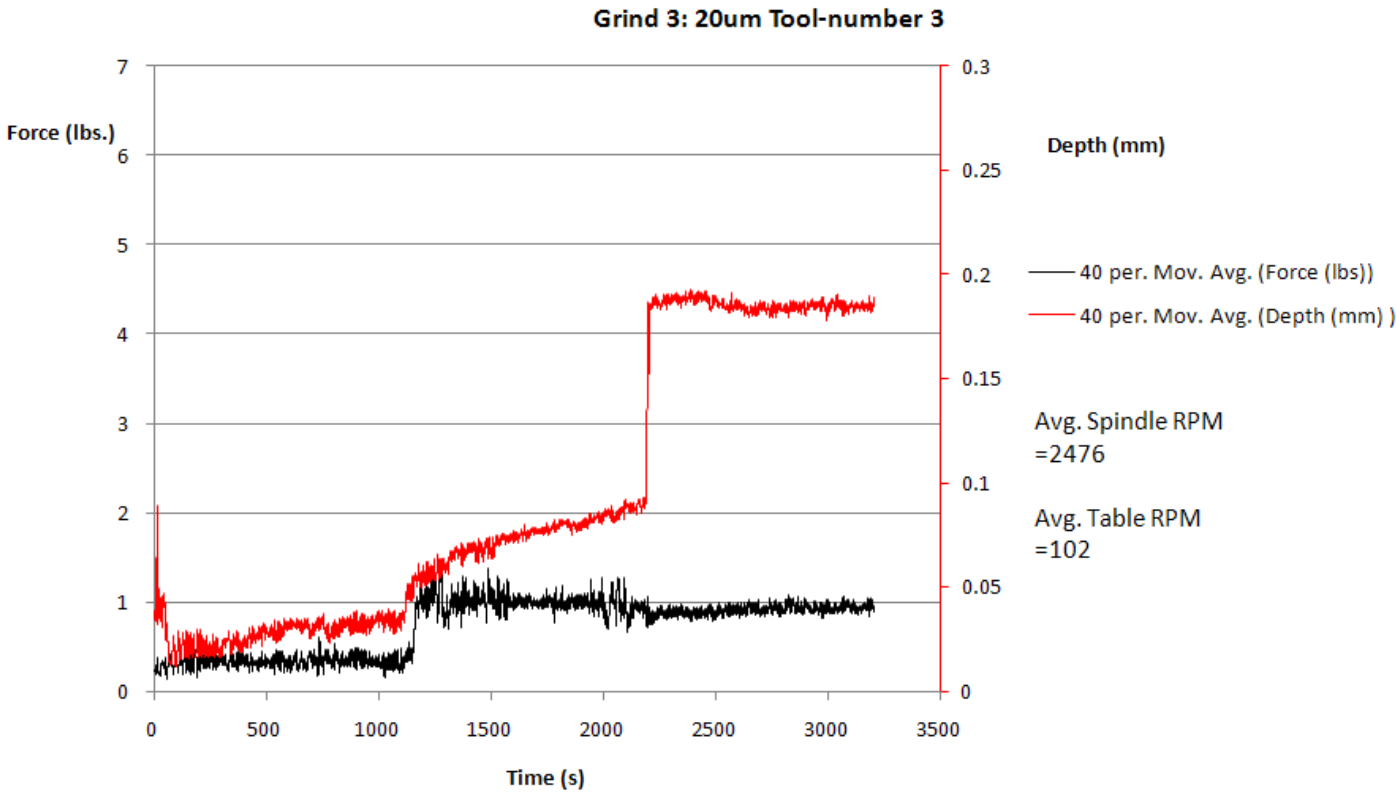


Figure 5.6 The data from Grind 3. The 20 µm tool was used.

The fourth grind (Grind 4) was performed with the 20-2 tool and lasted 24 minutes. The force was ramped up starting at 1 pound and ending at 15 pounds. Then the 5-1 tool was used with a force of 3 pounds to improve the surface and lasted 5 minutes. Approximate force used was 3 lbs. The maximum RPM for both the spindle

and table was used. The data acquisition system crashed during the test thus no Labview data was collected. The sample was cleaved and the profile was examined using SEM (Figure 5.7). The average removal rate was 0.11μm/sec. A final grind depth in to the SiC substrate was approximately 159 μm. Chipping around the contour edge was discovered (Figure 5.8 and Figure 5.9).

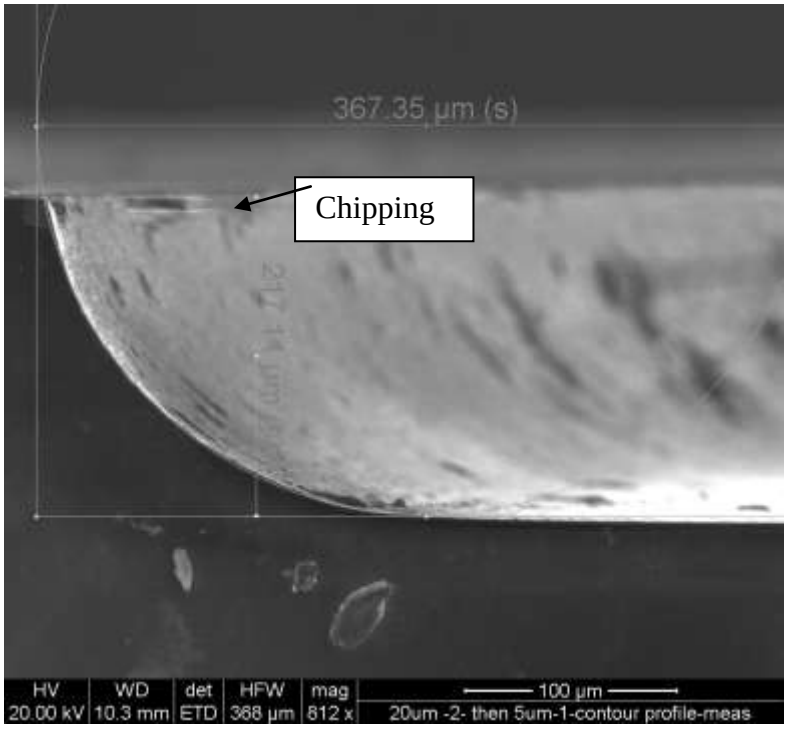


Figure 5.7 An SEM image of the contour produced from Grind 4. The depth of the grind was 159 micrometers.

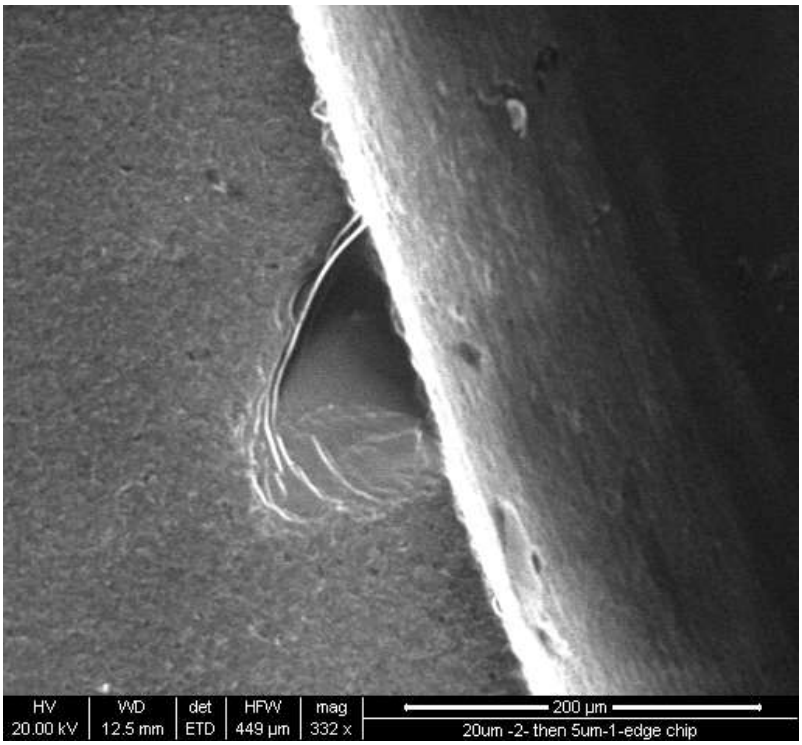


Figure 5.8 Grind 4 shows edge chipping.

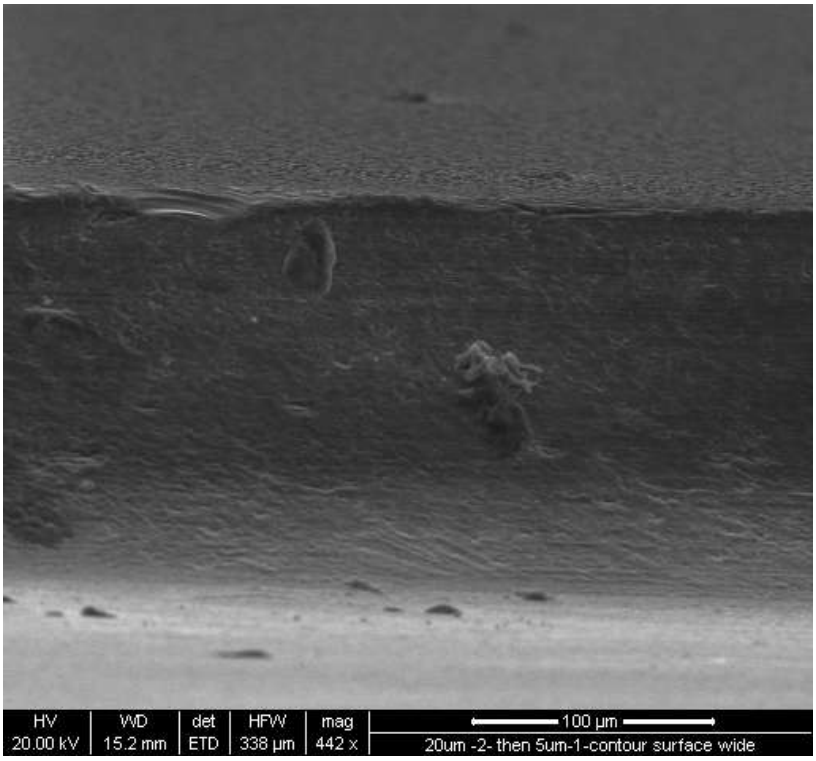


Figure 5.9 An SEM image of the contour wall produced in Grind 4.

5.2. **Analysis**

The every tool edge met the design size specifications with a tolerance of ± 26μm. Therefore, to produce a complete contour in a substrate, the tool must travel into the substrate to an average depth of 190μm. Since the depth required complete contour is well under half of the substrate thickness of 480μm (± 1μm), completing a dual side processing of the PCSS is possible. Furthermore, given that the standard deviation of the edge radii is 14μm, using multiple tools on the same substrate to progress the surface finish would not degrade contour form if the position of the X-Y table could be aligned properly. The desktop mill used was low grade with considerable slop; therefore, accurately realigning the X-Y to account for a tool change during mid-grind was not feasible. It was concluded that one tool should be used per substrate to acquire the initial depth.

The graph from Grind 1 shows a strong relation between depth achieved and force applied (Figure 5.1). At first, travel into the sample appears to be nearly instantaneous and then ceases if a constant grinding force is maintained. More depth could only be achieved if force was increased. The relation is verified in Grind 2 where a constant force of approximately 11 pounds was used (Figure 5.4). The removal rate is shown to approach zero in less than 60 seconds. Tool 5-2 was examined with SEM and the images are shown in Figure 5.10. A depth increase following a force increase signifies tool inefficiency. The inefficiency was attributed to excessive tool wear. As the cutting diamond points flatten their surface area increases lowering the pressure on each cutting diamond; therefore, the grinding force must be increased to obtain a constant pressure and thus a constant removal rate. The cutting diamonds become less effective at cutting

due to their dullness. Furthermore their exposed size increases thus the chip pocket size is decreased. The decrease in chip pocket size causes swarf loading that further impedes material removal.

One advantage of excessive tool wear on the face of the tool is an improved surface finish. Figure 5.5 shows the unaltered surface quality from the manufactured (left) and the surface quality of the bottom of the void created (right). The transition (middle) shows how the surface quality improves as the diamonds are dulled and flattened. The flattening lowers the depth of cut allowing the removal to occur in the ductile grinding regime as verified in a closer examination (Figure 5.11).

The data from Grind 3 shows that a low grinding force produces a constant removal rate. One reason is due to a lower force per grit. The diamonds stay sharper longer so material removal is more consistent. Applying a lower grinding force is necessary since the tool and table speeds are extremely low compared to previous work where spindles speeds used were 10, 12, and 15 m/s and the table speed used was 1000 RPM [38]. Increasing the kinetic energy of the tool and workpiece lowers the force per grit and consequently the depth of cut thus improving surface finish and form accuracy substantially more so than lowering only the normal grinding force [23]. Obtaining 10m/s average speed for the diamonds of the tool would require the desktop mill spindle to run at 44,000 RPM. Revolutions-per-minute at this level would introduce unmanageable vibration and bearing failure if the existing system was modified. Minimizing the normal grinding force was the method used to compensate for the RPM limitation of the existing system. Furthermore, purchasing a system that can handle such

high RPMs with micrometer accuracy, such as the Loh Spheromatic 25-2SL, was outside of the budget for this research.

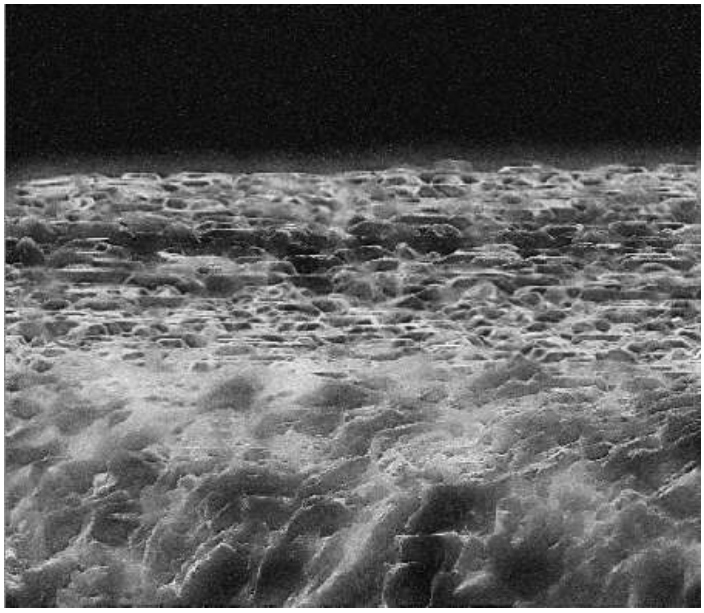


Figure 5.10 An SEM image of excessive tool wear on tool 5-2.

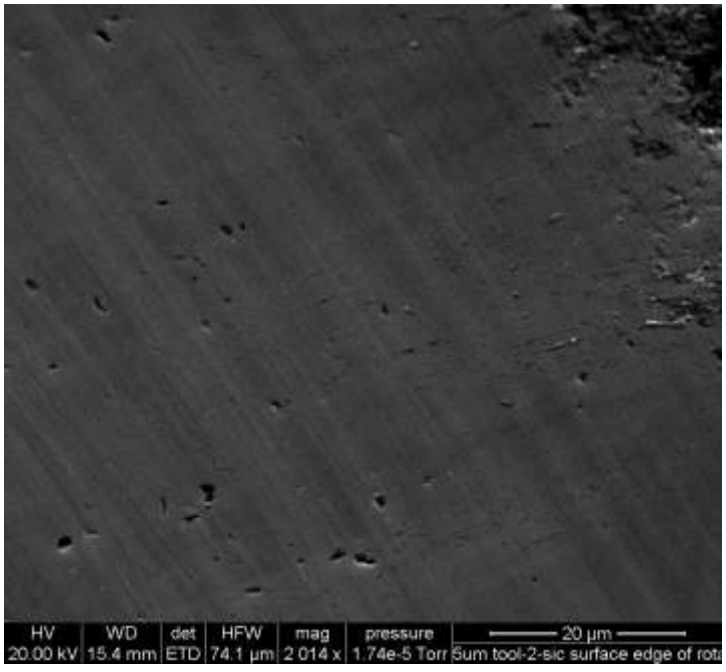


Figure 5.11 An SEM image of ductile regime grinding due to tool wear (5-2 tool).

The inability to maintain the constant removal rate during Grind 3 may also be attributed to the coolant system. Previous work where depths of 150μm into silicon carbide were obtained used a coolant flow rate of 6.6 l/min with pressurized injection [37]. The grinding system in this research used a submerged coolant technique with a maximum coolant flow rate of 0.13 l/min. The submerged coolant technique uses atmospheric pressure, gravity, and viscosity to circulate coolant through and beneath the tool. The interaction of centrifugal force and coolant viscosity due to tool rotation impedes the flow of the coolant through and beneath the tool. The lack of adequate coolant flow allows heat to accumulate in the diamonds thus lowering their hardness and accelerating wear. The accelerated wear is observable in all data plots where the depth gauge reading has low correlation to the depth travel into the SiC substrate. The electronic indicator is found to only monitor a combination of diamond wear and material removal. By using the electronic indicator alone, one can only determine when the diamond tool is no longer effective during a grinding experiment. To improve tool life and allow for higher tool speeds, a hollow tool should be designed and pressurized coolant should be injected through the tool. Through the tool coolant flow allows centrifugal force to aid in coolant flow beneath the tool. It would also decrease tool loading by more effectively clearing swarfs.

The pronounced step in the depth recorded in Figure 5.6 can be explained by considering the slop, or lack of stiffness in the grinding setup. By setting the headstock gib to low friction as required by the counter weight force system, the headstock has detrimental play during grinding. The vibration from headstock play during grinding is obvious when considering the large period for the moving average needed to improve the

readability of the data. The step during the depth measurement is therefore a result of the repositioning of the contact point of the electronic indicator during vibration.

The results shown in the SEM image of Grind 4 were unlike any previous grinds. The contour produced was 83 percent complete. The use of the 5-1 tool effectively improved the surface finish of the contour when comparing the finish of Figure 5.2 to Figure 5.8 and Figure 5.9. The images prove that to achieve the desired depth into the SiC substrate the normal force on the tool must be increased to counter the decrease in the cutting ability of the tool. The positioning of the 5-1 tool could not be performed in a precise manner with the existing setup. The tool was therefore lowered into the void away from the contour and the substrate was repositioned with the Y-axis dial until the tool was spinning against the contour wall. The surface quality of the contour was improved at the expense of the quality of the center of the void. By over-widening the diameter of the void, a center post formed in the middle of the void due to the eccentric grinding arrangement (Figure 5.12). The chipping shown in Figure 5.8 results from vibration due the lack of stiffness in the system and the large removal rate that occurs when abruptly increasing the grind force.

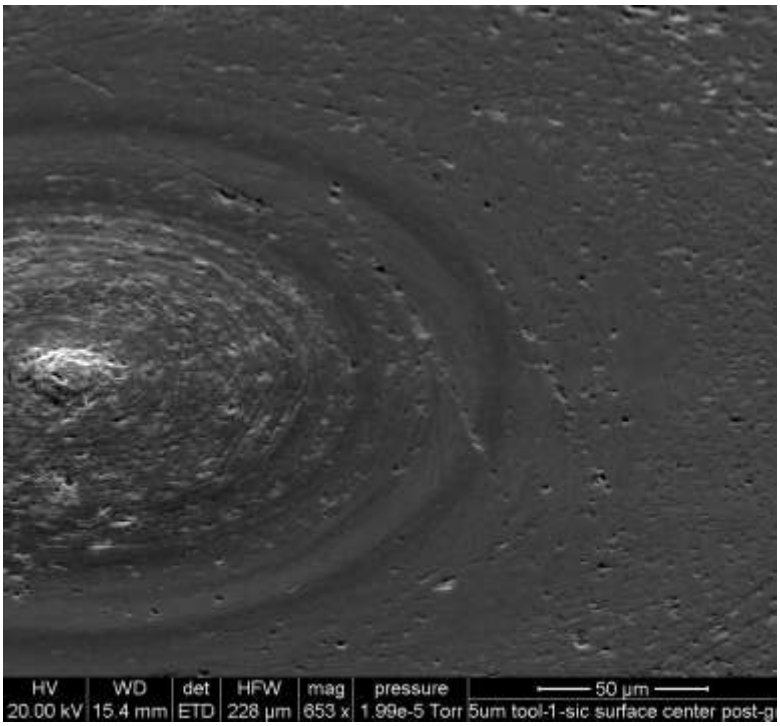


Figure 5.12 An SEM image of the center post produced in Grind 4 due to over-widening the void diameter.

Information on areas of the grinding system that are in need of improvement maybe gathered from Grinds 1 though 4. By redesigning the method using to apply a constant grinding force, slop and vibration can be attenuated and the form accuracy, the surface quality, and the precision of the grind can be enhanced. Grind repeatability with the system is also an issue that should be addressed. By controlling a stiff, accurate grind system so that it has an extremely small scale of material removal, SiC can be ground with a finish comparable to lapping and polishing [39].

The analysis of the results from existing grinding system demonstrates the systems ineffectiveness in producing sensible data. The average removal rates given are of little value since the system does not use a continuous in-feed system but uses constant force feed system. The data plotted is plagued by vibration so large period averaging must be used. Using constant force feed, maximum depth of cut throughout the grind

cannot be determined unless the depth into the substrate is directly measured by a different configuration than what has been used here. The grinding system proves however that eccentric diamond grinding maybe used to produce the IEP for the SiC PCSS. Its weaknesses and possible improvements are compiled in Table 5.2.

Table 5.2 Possible improvements to the grinding system.

Weakness	Effects	Recommendation for Improvement
Vibration	Chipping and surface fractures, poor surface finish	Lock headstock, tighten gibs
Slop and play	Low repeatability, poor form accuracy	Remove counter weight system, use compression grinding force
Depth indicator readout	Reads tool removal, slop, vibration, and SiC removal	Take differential micrometer depth gauge readings on void alone
Load cell	Unable to handle forces over 15 lbs, limits contour depth	Use higher capacity load cell
Low RPM	Low grinding energy, high grit contact forces, extreme tool wear, limits contour depth	Use machine capable of > 44,000RPM spindle speed
Low coolant flow	Extreme tool wear due to overheating, limits contour depth	Use pressurized through-tool coolant

5.3. **Grinding System Improvements**

Several of the improvements were made to the grinding system in order to enhance the quality of data gathered from the grinding process. Sample positioning can be made more accurate, vibration can be minimized, and substrate depth readings can be obtained by implementing the first three recommendations in Table 5.2.

The force producing system was redesigned to allow for the headstock to be locked during the grinding process. The counter weight system was first removed and the gib screws in the headstock were tightened to the point where a large amount of kinetic friction could be felt when moving the operating lever. Since the headstock is no

longer in a frictionless and free-fall state during grinding, its slop, play, and vibration is essentially removed. Furthermore, the small hand wheel, used for fine adjustment of the headstock height, was made operational by replacing the gear rack.

The grinding force that was once produced by the weight of the headstock is now produced by the force resulting from the compression of an elastic material placed between the shaft and the trust bearing (Figure 5.13). The elastic material produces a reaction force that is proportional to the distance it is compressed; therefore, after snugging the gib handle on the headstock, the grinding force of the diamond tool may be precisely dialed in by compressing the elastic material. The headstock remains stationary during grinding due to the static friction force created by the gib. As material is removed from the substrate, the elastic material slightly relaxes and grinding force slightly decreases. The hand wheel maybe used to move the headstock downward to correct the decrease in grinding force.

The new force producing system allows the headstock to be raised to measure substrate depth without losing the tool position. Grinding can therefore be resumed without a decrease in contour form accuracy. The depth is now measured by an electronic micrometer as opposed to an electronic dial indicator. The new measurement method allows the substrate removal depth to be directly monitored without the influence of diamond reduction and vibration. The only downside is the fact that continuous monitoring is not possible; the grinding must be paused to acquire a measurement (Figure 5.14). Table 5.3 shows the specifications of the electronic micrometer that was used as the depth gauge.

Additional grinding experiments were performed following the improvements made to the system. The subsequent sections present and analyze the information gathered. The results are expected to be more conclusive than the results obtained with the initial grinding system due to an improvement in machine stiffness, better isolation from environmental disturbances, and a more precise control of grinding force [39].

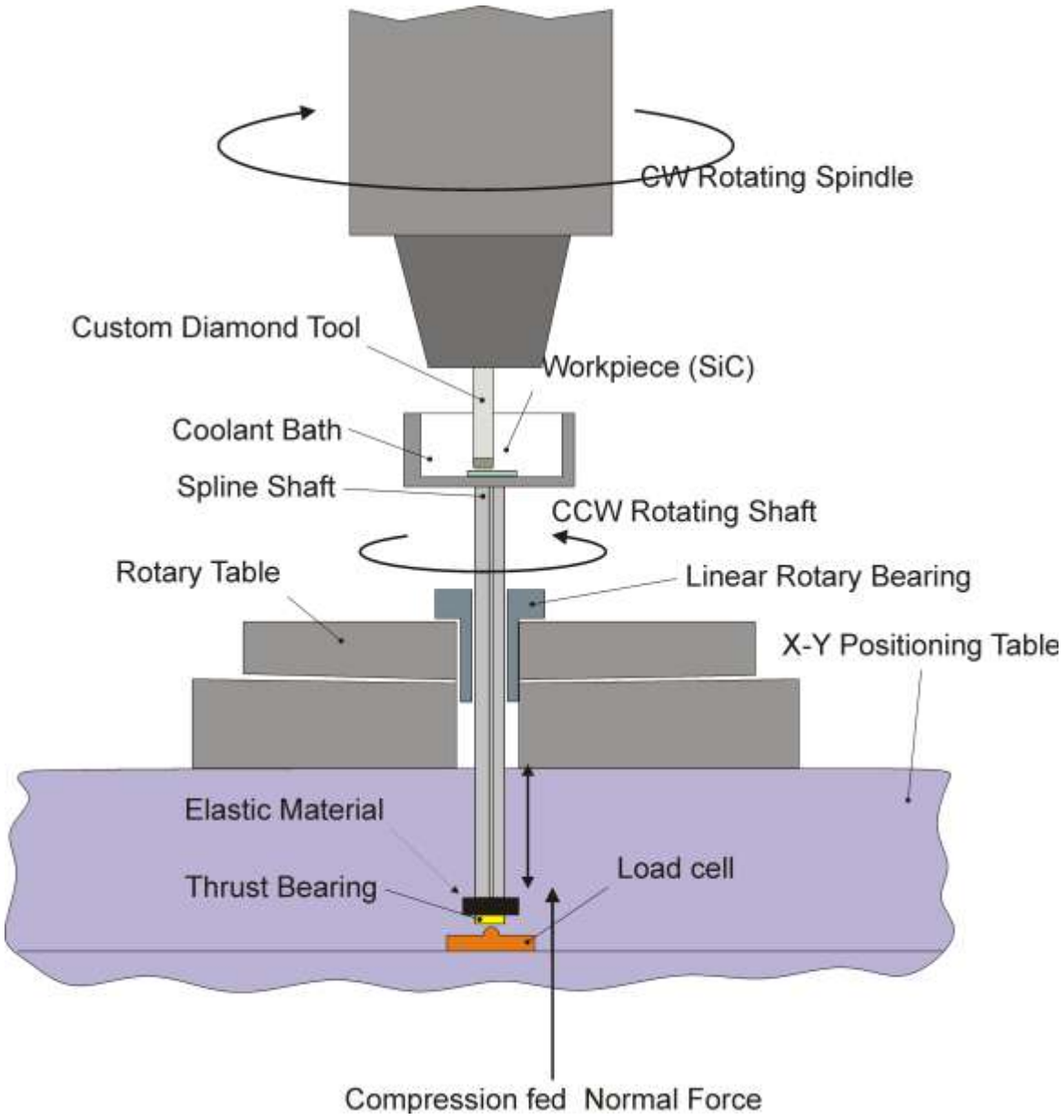


Figure 5.13 The improved removal system produces grinding force through the compression of an elastic material.

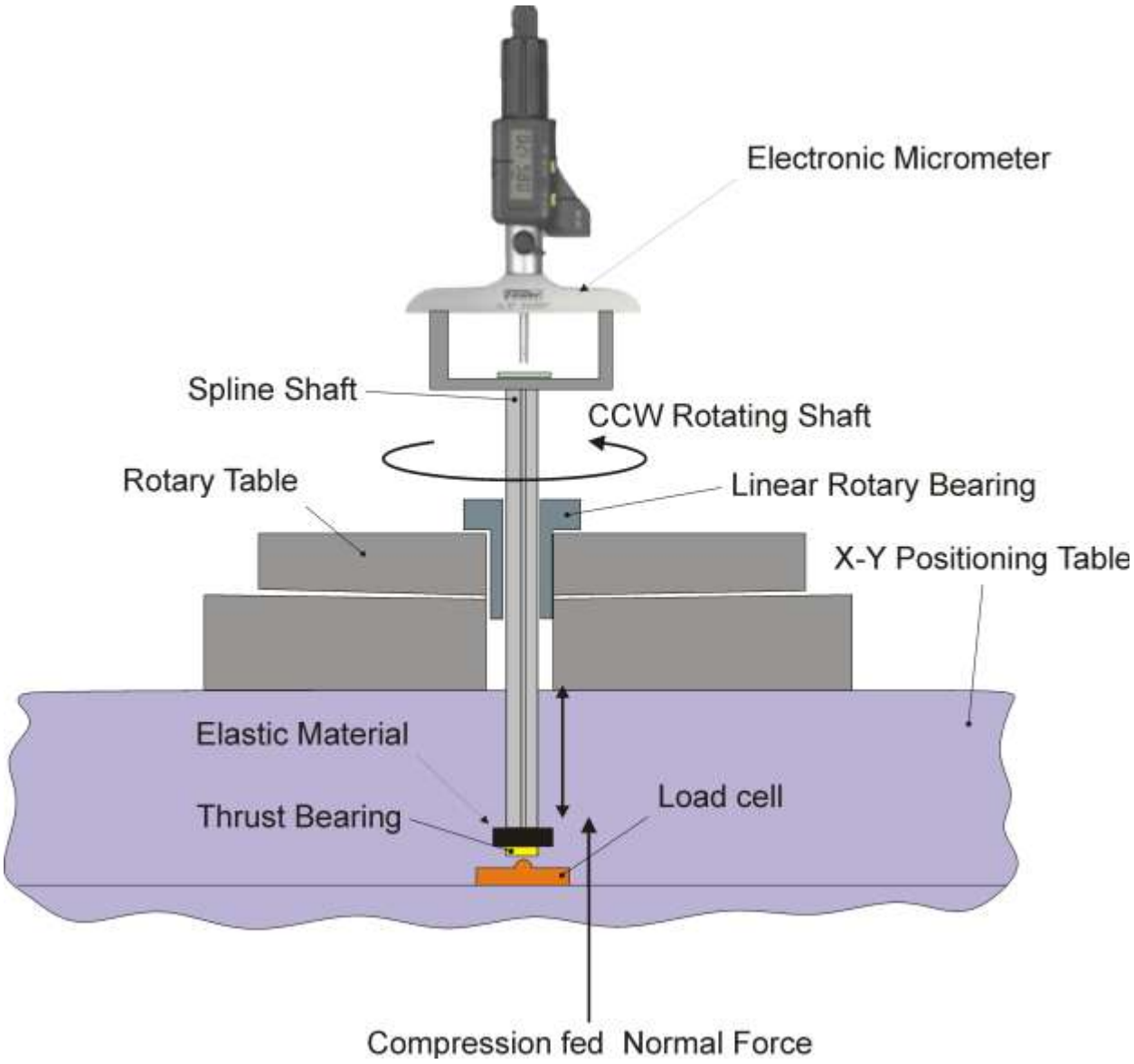


Figure 5.14 The micrometer is used to find the depth of the grind into the substrate.

Table 5.3 Electronic Micrometer Specifications

Electronic Micrometer	Fowler 54-225-456	Units
Range	550	mm
Resolution	.001	mm
Accuracy	± .001	mm

5.4. **Results After System Improvements**

The grinds performed with the grinding system prior to improvement (system 1.0) consumed 5 tools (20-1, 20-1, 20-3 , 5-1, and 5-2) and 5 SiC substrates. Seven unused tools were available (15-1, 15-2, 15-3, 10-1, 10-2, 10-3, and 5-3) and seven unused SiC substrates were available for additional grinding experiments with the improved system (System 1.1). An additional tool to be used for contour polishing was also fabricated.

Mechanical polishing pads are typically made of soft metals such as tin, lead, copper, a pitch, or resin [23].The polishing pads are submerged in abrasive slurry and pressed against the surface to be polished. The individual abrasives embed into the polishing pad. The micro-cutting edges of the abrasive produce fine scratches on the surface of the workpiece creating a high quality finish. By fabricating the pad with a metal that has high malleability and low toughness, it can be formed to a complex contour using pressure. The contour surface can be uniformly polished.

The polishing pad tested in this research was made of 99.9% pure tin and was in the form of a 1/4 inch diameter rod. The tin polishing tool was similar in design to the diamond tools used; however, the tin rod was solid, cut to one inch in length, and faced-off on both ends. The diamond tool could therefore be swapped out for a tin polishing tool following the grinding of a substrate without the need for tool repositioning. The slurry used with the polishing tool contained diamond abrasives having a size range of 2 to 4μm.

The data presented in Figure 5.16, through Figure 5.20 was collected from seven grinds using the seven remaining unused diamond tools and SiC substrates. Each grind was performed using spindle and table speeds of approximately 2500 RPM and 120

RPM, respectively. Each grind was paused periodically to gather substrate depth information. Each grind was cooled using the cooling system detailed in Section 4.5. Force data, RPM data, and grind time was collected with data acquisition system detailed in Section 4.5. The depth data from the dial indicator was disregarded. Grinds produced with the15-1, 15-2, and 15-3 tools had forces of 0.1, 0.4, and 1 lbs. applied, respectively. Grinds produced with the 10-1, 10-2, and 10-3 tools had forces of 0.1, 0.4, and 1 lbs. applied, respectively. Figure 5.15 shows how a depth rate relates to the grind force used for the 10µm and 15µm grit tools.

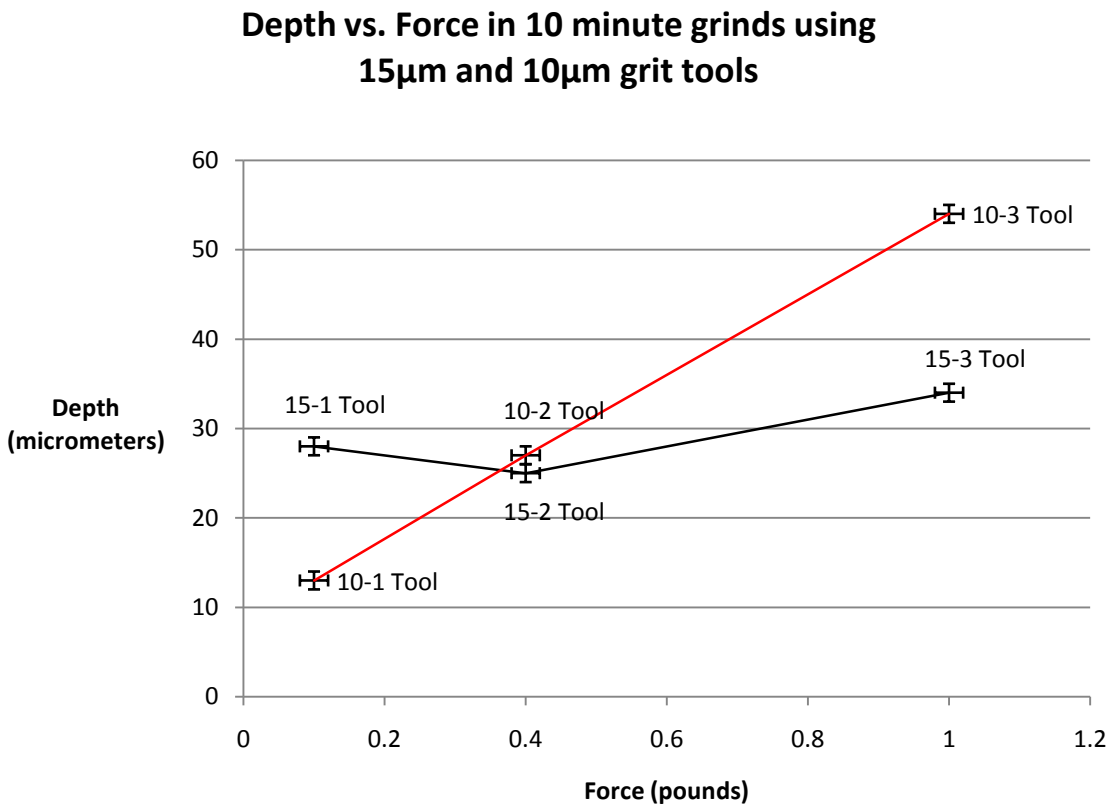


Figure 5.15 A plot of the depth and force relation for grinds performed with 10 and 15 micrometer grit tools.

Figure 5.20 and Figure 5.21 compared slurry polished and unpolished contours and surfaces. The images to the right in Figure 5.20 and Figure 5.21 show the results from a grind with the 15-2 tool. The images to the left in Figure 5.20 and Figure 5.21 show the results from a grind with the 15-3 tool followed by slurry polishing. The polishing tool had an arbitrary force of 4 lbs. applied with the purpose of forming the edge of the tool to the contour. The polishing duration was 15 minutes. The volume of slurry used was 3mL. Figure 5.22 shows how the tin polishing tool formed to the substrate contour.

The results gathered from System 1.1 are analyzed in the subsequent section. By reducing the unknowns through improving the contour grinding setup, the data obtained can be better analyzed to help more clearly map a direction for future research.

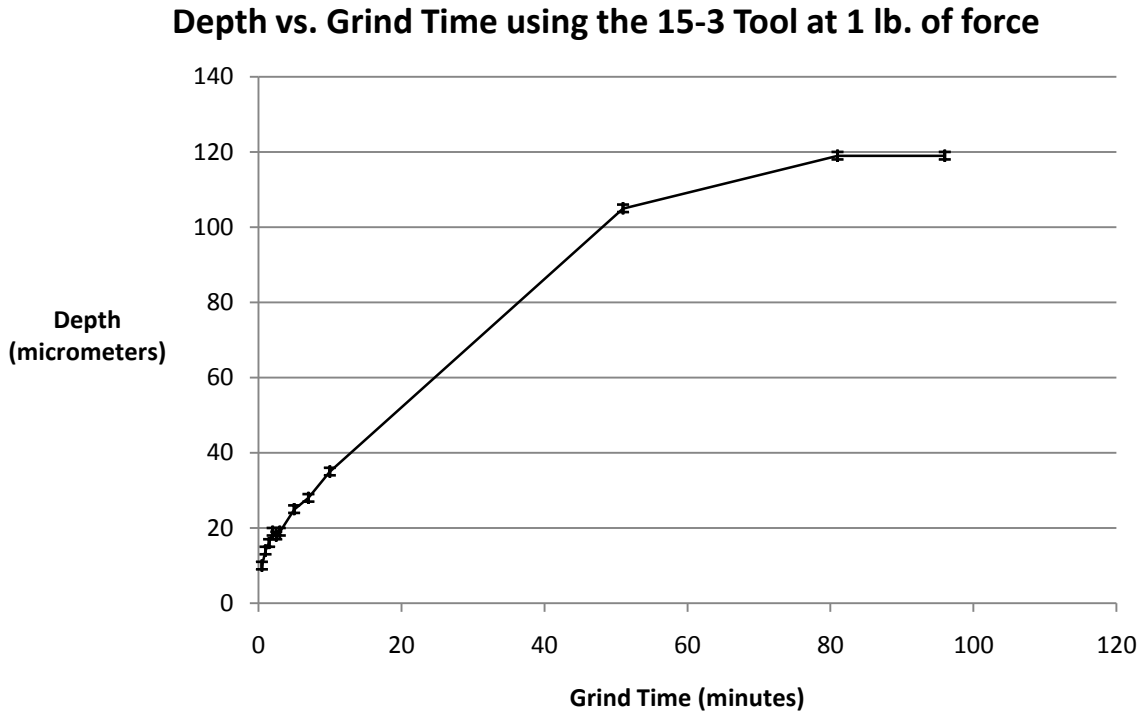


Figure 5.16 This plot shows how material removal decreases with time.

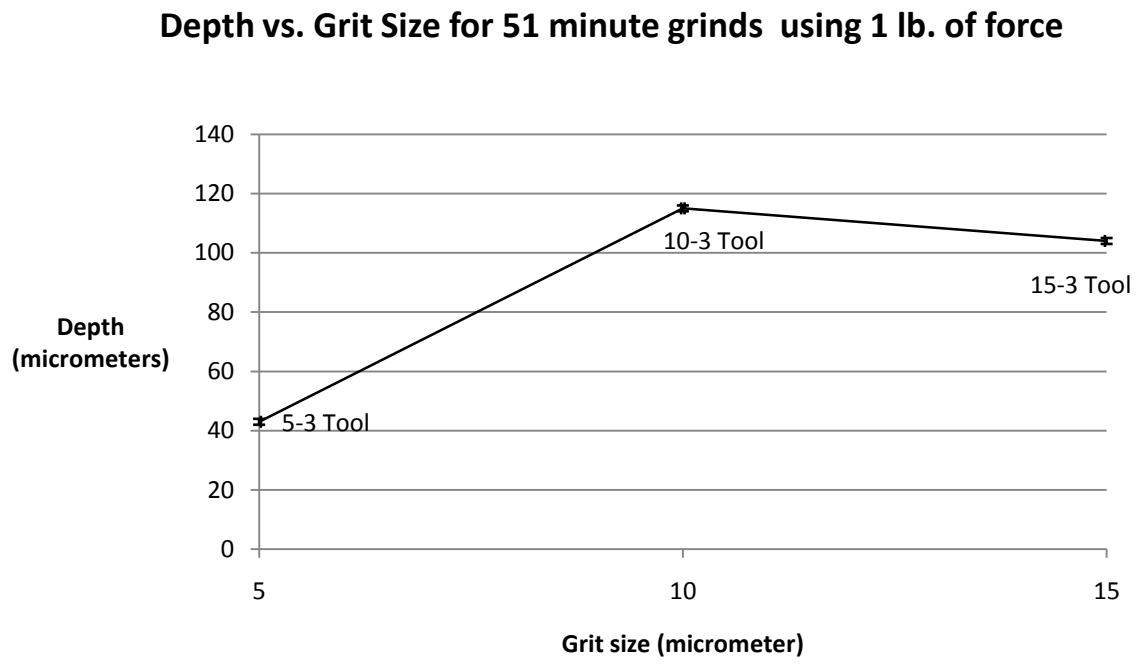


Figure 5.17 This plot shows how the depth into the substrate is related to grit size.

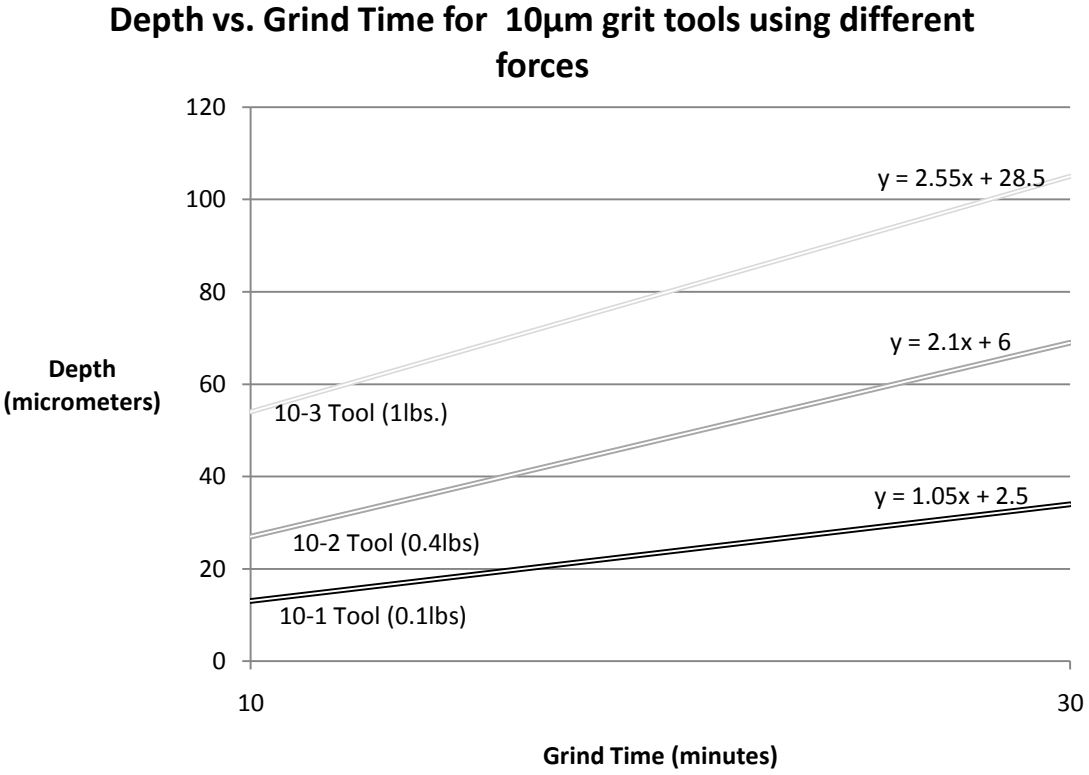


Figure 5.18 This plot shows how the depth rate compares to the grind force used.

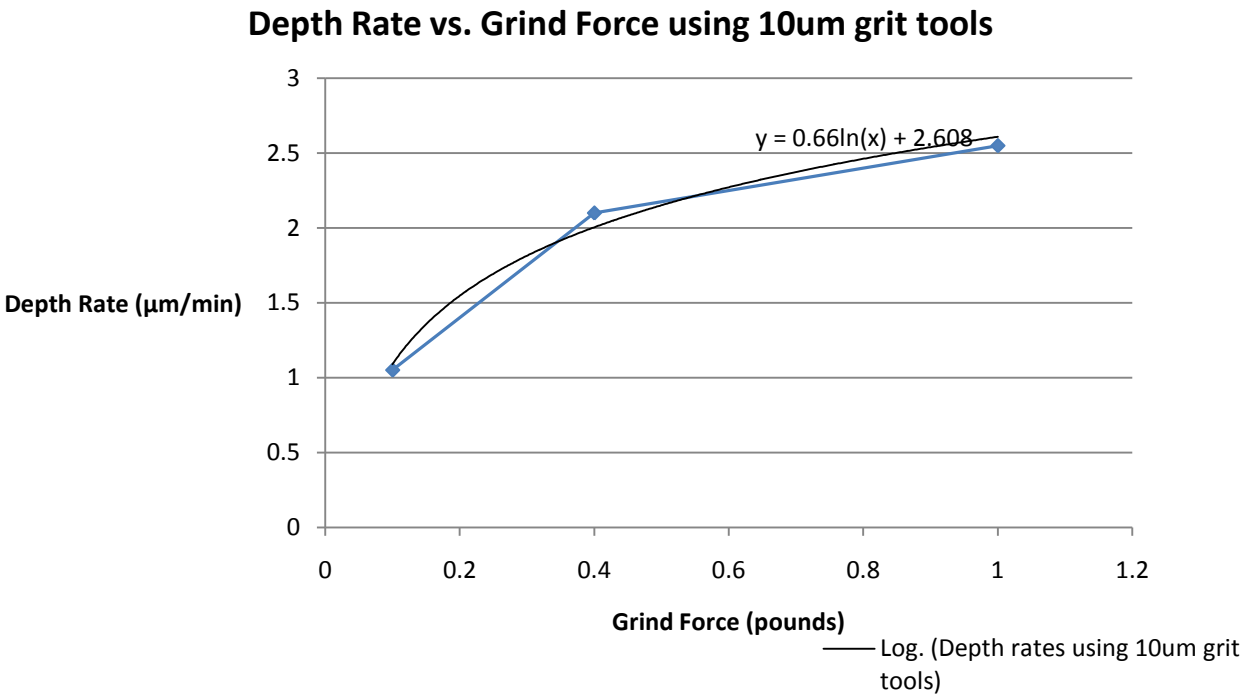


Figure 5.19 This plot shows the trend of the depth rate as the grind force was increased.

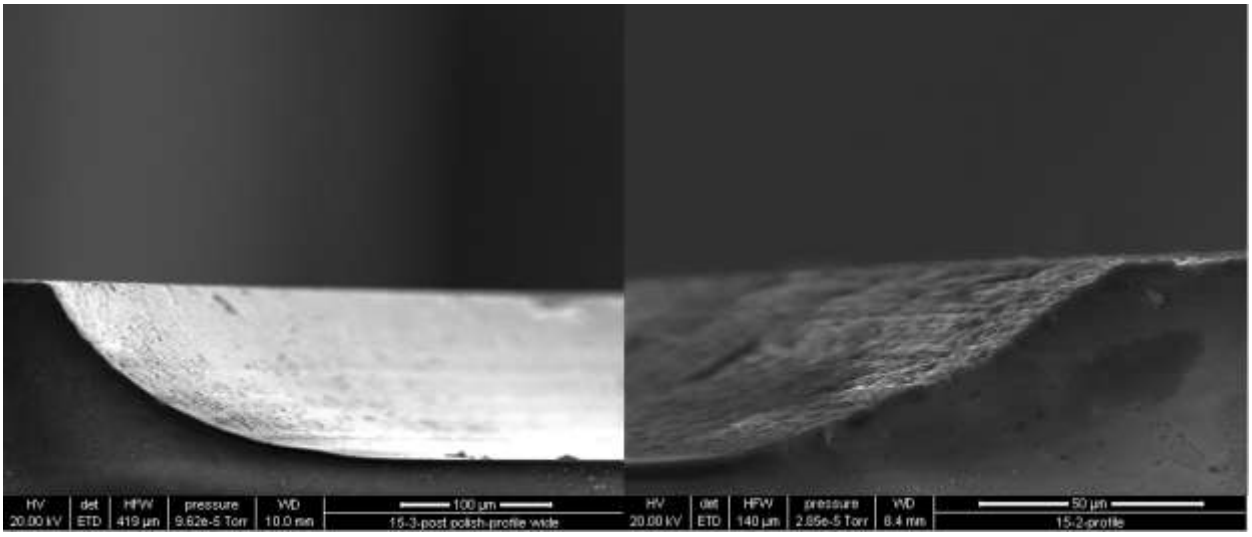


Figure 5.20 An SEM profile comparison image of the grind from 15-3 tool and mechanical polishing (left, 100µm scale) and the grind from 15-2 tool, no polishing (right, 50µm scale).

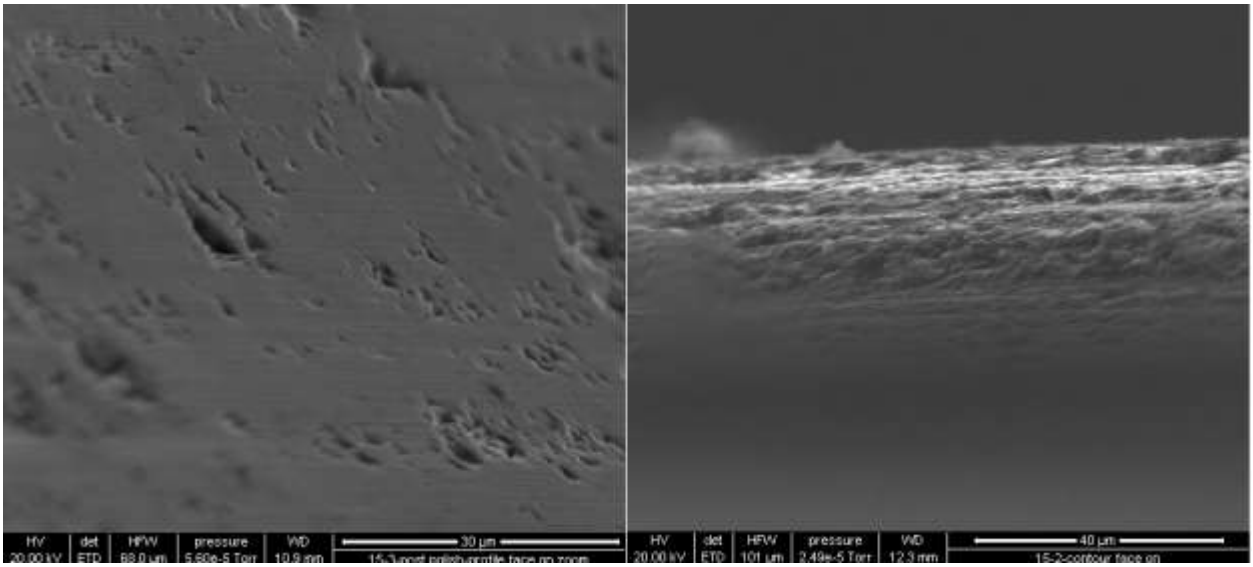


Figure 5.21 An SEM surface comparison image of the grind from 15-3 tool and mechanical polishing (left, 30 µm scale) and the grind from 15-2 tool, no polishing (right, 40 µm scale).

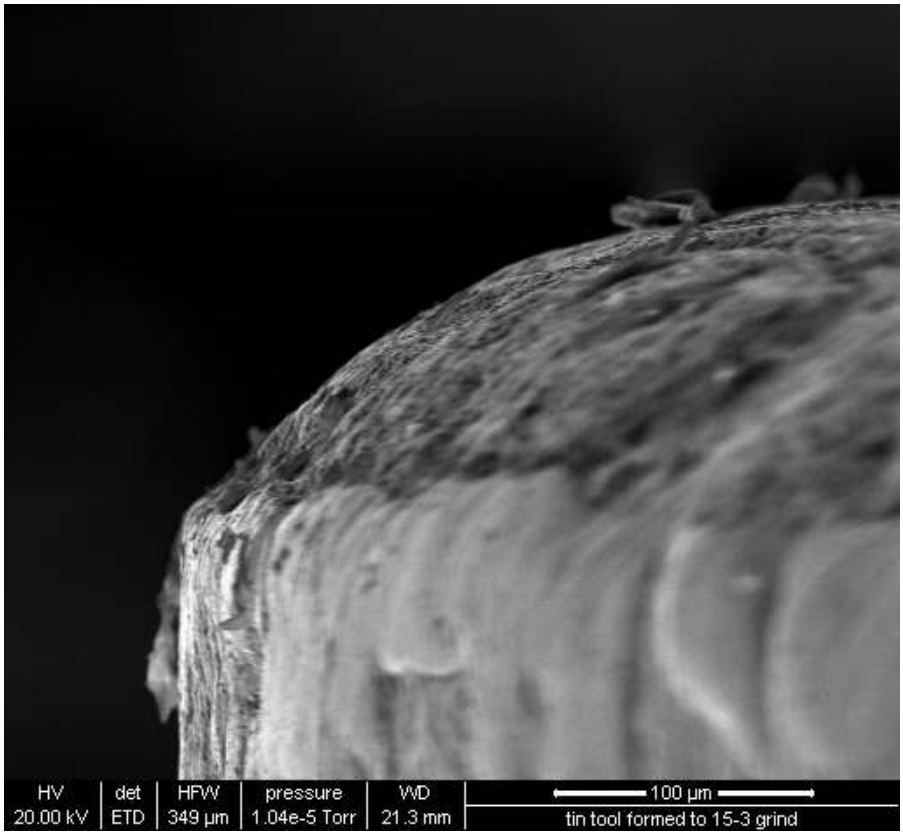


Figure 5.22 An SEM image of the edge of the tin polishing tool formed to the contour produced by the 15-3 tool.

5.5. **Analysis After System Improvements**

Similar in System 1.0, tool wear in the grinding experiments from System 1.1 was still an important issue as seen in Figure 5.16. A final depth of 119µm was achieved with a contour radius of approximately 177µm. The decrease in removal rate is clearly observable from System 1.1 data in Figure 5.16. The decrease is no longer attributed to the lack of system stiffness and vibration but to the low spindle/table speed, the cooling system, and the tool composition. For sintered, poly-crystalline SiC, a depth of cut greater than 65nm would predict material removal to occur in the brittle-facture mode [36]. The single-crystal SiC used in this research is consider to have equal or slighty higher hardness at 30 GPa [40]. The grinding mode transition would occur at an equal or smaller depth of cut according to Equation 2.27. The maximum depth of cut calculated was 384nm and happens during first half-minute of grinding (Equation 5.1). The tool in its sharp state is therefore fracturing the SiC. Fracturing creates large uncut chips that accelerate tool wear in early stages of the grind. Tools must remain sharp for efficient grinding. Fracturing is also a sign of excessive force-per-grit. Ductile mode grinding can be promoted by reducing the uncut chip thickness. Using higher tool speeds reduces the uncut chip thickness which results in a smaller force-per-grit.

Equation 5.1 $$Depth\ of\ Cut = \frac{60}{RPM} \cdot \frac{\Delta D}{\Delta T}$$

The diamond tools were made of an electroplated monolayer of diamond. The best diamond configuration to produce an accurate contour is the monolayer. The contour dimension would change by only about 50 percent of the mean grit size as the individual abrasives wear. It is important to note, however, that the behavior of the monolayer diamond tool changes during grinding. Unlike the multilayer diamond tools that undergo

noticeable dimension change during self-sharpening, monolayer tools require grind force adjustments to maintain a constant feed rate due to the dulling of the abrasives. It is therefore not possible to achieve a steady state removal rate by using a constant grinding force. The wear gradient can be made low and the removal rate made more constant by improving the removal of workpiece chips. Faster diamond wear results from abrasive attack by lingering chips as well as low tool speeds and poor cooling.

Figure 5.15 shows that a sharp 10µm grit is more effective at material removal during, for grinding forces equal to or greater than 0.4lbs, compared to a sharp 15 µm grit. This is a reverse of the general observations in grinding where larger grit leads to more effective material removal. A possible explanation is that the diamond concentration on both tools was so large that chip pockets were too small to relieve chip loading. Smaller chips created by the lower grit size clear out more easily to facilitate material removal. Since increasing the grinding force on both of the grits sizes increases the depth of cut of the tools and the size of the chips produced, the larger grit is more susceptible to chip loading while sharp. Figure 5.17 shows that the removal rates between the 10 µm grit and 15 µm grit tend to equalize as grinding continues. As the diamonds flatten, chip pockets for both grits are further reduced in size to a point where neither size of pocket offers a chip clearing advantage. Furthermore as the diamonds of both grit sizes are flattened, 10µm diamonds likely produce more heat. This can be justified by assuming that the higher diamond concentration in the 10µm tool contributes more to friction. The 15µm grit tool is able to achieve more material removal, i.e. deeper travel into the substrate, due to its abrasives being larger in volume which means longer tool life.

The data plotted in Figure 5.18 is taken from the section of time during grinding that generally showed the most depth activity, the 10 minute to 30 minute period. The slopes of the lines in the plot represent the average depth rate for the specific grind force on each of the 10µm grit tools. By plotting the average depth rates for the different grinding forces, as done in Figure 5.19, a logarithmic trend was discovered. The trendline shows that as the grind force is increased on a tool there is an increase in depth rate; yet, the degree of the increase in depth rate diminishes as force is increased further. The trendline equation may be differentiated and solved to find the grinding force that produces negligible improvement in the depth rate. For example, if a 10 percent improvement in depth rate is considered to be negligible, this corresponds to a grind force of approximately 6.6 lbs for the 10µm grit tool.

A side-by-side SEM image comparison is shown in Figure 5.20 and Figure 5.21. The left image is a 15µm grit grind without post-polishing and the right image is with post-polishing. Since the equipment needed for a quantitative analysis was unavailable, a visual comparison was the only option. It is easy to see from Figure 5.20 that the contour form was maintained. It is estimated that less than 2 micrometers of material was removed during the 15 minutes of polishing. Figure 5.21 is an up-close view of the two surfaces from Figure 5.20. The surface finish is greatly improved and grind damage was reduced without deforming the desired contour. The tin polishing tool proved to be highly effective at forming to the contour to produce a uniform polish (Figure 5.22). Contour polishing with a tin tool and slurry maybe further enhanced by using an alkaline slurry with a pH greater than 10 in elevated temperatures (55ºC) [41].

Chapter 6: Summary and Conclusions

6.1. **Summary of Work**

This work has resulted in the design of a novel package geometry for the SiC PCSS as well as a process to fabricate the package geometry. ElecNet simulations were performed to determine how the existing SiC PCSS package geometry contributed to field enhancement. Electrodes, having a radius of 100μm or greater, inserted into the SiC substrate was found to lower field enhancement by one order of magnitude. ElecNet parameterization was used to develop an optimized package geometry. The main part of the package geometry required a contoured void to be produced in the SiC substrate. The initial stages of the fabrication process were tested. A grinding machine and diamond tools were designed and built to produce the contour. A custom polishing tool was also created out of tin that can prepare the contour surface for the deposition of ohmic contacts.

The contour grinding system was built specifically to demonstrate that the contoured void in the SiC PCSS was possible. The contoured void was produced directly into the substrate by mechanical means with simple machinery. An eccentric, vertical spindle grinding configuration was implemented to produce a circular and uniform void in the SiC substrate. The best contoured void produced had a radius of 177μm and a depth of 119μm with a roughness projected to be on the sub-micrometer scale. The grinding system is capable of turning the diamond tools at speeds ranging from 0.02 to .57 m/s (0 to 2500 RPM) and rotating the workpiece at speeds ranging from 0 to .065 m/s (0 to 120 RPM). The grinding system is also capable of applying a constant grinding force of 0.1lbs to greater than 10 lbs, depending on the capacity of load cell used. A

variety of coolants may be used in the system as well. The grinding system was later improved in such a way that the SiC substrate may be removed, analyzed, and returned for further grinding and polishing without the loss of workpiece and tool positioning. The use of 10μm diamond grit sizes showed the best grinding performance if the sharpness of the tool can be preserved. Monolayer, metal-bonded, diamond tools can produce uniform and accurate contours in SiC substrates on the micrometer scale.

The system constructed yielded useful SiC PCSS packaging results. There are improvements that can made to increase tool life, data acquisition, ease of use, and dual sided processing, but the initial design and construction can produce a SiC substrate that is ready for contact deposition and voltage testing.

6.2. **Future Prospects**

Based on the success of this project and the grinding results the research will be continued to verify that the field blocking performance of the SiC PCSS has been improved by the IEP. To optimize the grinding and polishing processes, a quantitative method of analysis should be established. A 3D optical profiler, such as the Zygo NewView 6000, capable of analyzing contour form accuracy as well as surface quality with sub-nanometer resolution would offer great insight. Also modifying the grinding system to run at much higher spindle speeds (10 m/s) would improve tool life immensely, along with a through-tool, pressurized cooling apparatus. By improving and optimizing the grinding system, a void depth equal to the contour radius of the tool can be achieved and the full potential of IEP can be tested.

The data acquisition system may also be further developed. To accurately monitor the depth of the void being ground into the substrate, the grind experiment must be

stopped and the diamond tool raised. The depth should be measured on the fly for feed rate analysis and adjustment; therefore, a new measurement method should be developed.

A heating apparatus may also be added to the workpiece mount. Adding heat to the mount would ease substrate mounting and removal. Furthermore, the heating apparatus could heat an alkaline slurry that would be used in the polishing process.

Future work should focus on the triple point junction that will result after the deposition of ohmic contacts as well. A lapping method should be developed to smooth any irregularities and mismatch between the contour edge and the deposited metals. This research demonstrated how a uniform contour could be produced and polished; however, fracturing at the edge of the contour was not addressed. The crisp transition between materials at the junction is projected to be the next roadblock.

6.3. **Conclusion**

The SiC photo-switch (SiC PCSS) has the potential to enable the fielding of the most compact pulsed power supplies. These switches can help advance the development of the many pulsed power applications from photonic radar to electromagnetic launchers. The demand for a SiC PCSS that can operate near the theoretical limits of SiC is apparent.

The main goal of this research initiative is to develop a SiC PCSS package that overcomes the existing SiC PCSS field blocking limitation of 300kV/cm. The main goal was divided into six sub-goals, four of which were accomplished in this work. Namely, a substrate geometry was designed that would potentially reduce induced local fields in the SiC PCSS. A production process was developed that will overcome existing SiC PCSS packaging drawbacks. A fabrication method was chosen and implemented that produced

the novel SiC PCSS geometry. Furthermore, steps were taken to give insight on the fifth sub-goal, polishing and interface preparation. The final sub-goal is to assemble and test the novel SiC PCSS package geometry to verify that the field blocking capability was improved beyond 300kV/cm.

References

1. *Opportunities for employing silicon carbide in high power photo-switches.* **Nunnally, W. C. and Mazzolla, M.** s.l. : IEEE, June 2003. Pulsed Power Conference, 2003. Digest of Technical Papers. PPC-2003 14th IEEE International. Vol. 2, pp. 823-826.

2. *Toward pulsed power used for photoconductive switches.* **Loubriel, G. M., O'Malley, M. W. and Zutavern, F. J.** Arlington, VA : s.n., 1987. Proc. 6th IEEE Int. Pulsed Power Conference.

3. *High-Power Microwave Generation Using Optically Activated Semiconductor Switches.* **Nunnally, W. C.** 12, December 1990, IEEE Trans on Elec. Devices, Vol. 37.

4. *High electric field, high current packaging of SiC photo-switches.* **Nunnally, W. C., et al.** Monterey, CA, US : s.n., 2005. IEEE International Pulsed Power Conference.

5. **Kelkar, Kapil.** *Silicon Carbide as a Photo Switch Material for High Power Applications.* Electrical and Computer Engineering, University of Missouri-Columbia. Columbia, MO : s.n., 2006. Disseration.

6. **Druce, R. L. et al.** *Photoconductive Switching in Gallium Arsenide.* National Technical. Information Service. Royal Road, VA : US Dept. of Commerce. UCRL 53868-91.

7. **Nunnally, W.C. and Hammond, R. B.** *Photoconductive power switches.* s.l. : Los Alamos National Laboratory Report LA-9759-MS, April 1993.

8. *Characterization of a semi-insulating GaAs photoconductive semiconductor switch for ultrawide band high power microwave applications.* **Islam, N E, Schamiloglu, E and Fleddermann, C B.** 14, 1998, Applied Physics Letters, Vol. 73.

9. *Electrostatic and current transport properties of n+ /semi-insulating GaAs junctions.* **Darling, R. B.** 1993, Journal of Appl. Physics, Vol. 74, p. 4571.

10. *Analysis of high voltage operation of allium arsenide photoconductive switches.* **Islam, N. E. et al.** 1999, Journal of Appl. Physics Lett., Vol. 86, p. 1754.

11. *Methods and configurations for improving photo-conductive switch performance.* **Nunnally, W. C. and Cooperstock, D.** July 2002. Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. Conference Record of the Twenty-Fifth International . pp. 183-186.

12. *Design and characterization of silicon carbide photoconductive switches for high field applications.* **Kelkar, K. S., et al.** 124905, 2006, Journal of Appl. Phys., Vol. 100.

13. *Doped Contacts for High-Longevity Optically Activated, High-Gain GaAs Photoconductive Semiconductor Switches.* **Mar, A. et al.** 5, October 2000, IEEE Trans. Plasma Sci., Vol. 28, pp. 1507-1511.

14. *PCSS lifetime testing for pulsed power applications.* **Saiz, T.A., et al.** Albuquerque, NM : Pending publication., 2007. IEEE Pulsed Power-Plasma Conference.

15. **Smith, F. Graham and King, Terry A.** *Optics and Photonics.* New York : Wiley and Sons, 2000. 0471489247.

16. *Investigation of Extrinsic, Compensated, Semi-Insulating Silicon Carbide Photo-Conductive Switches for Directed Energy Applications.* **Nunnally, W., et al.** Albuquerque : s.n., 2006. 9th Annual Directed Energy Symposium.

17. *Photoconductive semiconductor switch experiments for pulsed power applications.* **Zutavern, F.J. et al.** 12, Dec. 1990, Electron Devices, IEEE Transactions on, Vol. 37, pp. 2472-2477.

18. *On the Preparation of V-Doped Semi-Insulating SiC Bulk Crystals.* **Bickermann, M, et al.** 2, 2002, American Insitute of Physics, Vol. 22.

19. *Deep Levels in silicon carbide: A review.* **Lebedev, A. A.** 2, Feb 1999, American Institute of Physics, Semiconductors, Vol. 33.

20. **Kraus, John D.** *Electromagnetics.* s.l. : McGraw-Hill, 1984. pp. 56-87. 007035423.

21. **Latham, R V.** *High Vacuum Insulation: Basic Concepts and Tenological Practice.* San Diego : Academic Press, 1995. 0124371752.

22. *Tribo technological aspects of brittle materials grinding.* **Marinescu, I.D. and Webster, J. A.** Ohio : Society of Manufacturing Engineers, 1993, Proc. of the 5th International Grinding Conf.

23. **Marinescu, Ioan D., Tonshoff, H. K. and Inasaki, I.** *Handbook of Ceramic Grinding and Polishing.* Norwich : William Andrew Publishing, 1998. 0815514247.

24. *Silicon carbide photonconductive switch for high-power, linear-mode operations through sub-band-gap triggering.* **Kelkar, K S, et al.** 9, 2005, Journal of Applied Physics, Vol. 98.

25. *Processes leading to filaments in optically switched semiconductors.* **Stout, P.J. Kushner, M.J.** 1993. Proceedings IEEE Pulse Power conference. pp. 808-813.

26. **Wall, Dave.** *Representative.* [Email] [prod.] SiC Laser Machining. s.l. : Resonetics, June 6, 2006.

27. **Tucker, Jeff.** *Representative.* [Email] s.l. : Rohm and Haas, June 6, 2006.

28. **Mittl, Scott, D.** *Sales Engineer.* [Email] [prod.] SiC Grinding. s.l. : Insaco, June 13, 2006.

29. **McNutt, T. R. Ph.D.** *Process Engineer.* [Email] [prod.] SiC Etching. s.l. : Northrop Grumman, Jan. 31, 2007.

30. **Hannan, Phyllis A.** *Representative.* [Email] [prod.] SiC Laser Machining. s.l. : LaserUSA, June 6, 2006.

31. **Kelkar, Kapil, Ph. D.** Simulations of Contour Etching of 6H-SiC. *Unpublished Computer Simulations using SILVACO.* February 2007.

32. *Ultrashort-pulse laser machining of dielectric materials.* **Perry, M. D. et al.** 6803, 1999, Vol. 85.

33. *Microstructuering of SiC by laser ablation with pulse duration from ns to fs range.* **Kreutz, W. E. et al.** 50, s.l. : LAMP 2002, Jan 2003.

34. **Tsai, H and Yukun, H.** *Femtosecond Laser Contouring of 6H-SiC.* MAE Dept., University of Missouri-Rolla. s.l. : Unpublished Results from Laser Machining Experiment, 2007.

35. *Fluid jet polishing of optical surfaces.* **Fahnle, OW.** 28, 1998, Applied Optics, Vol. 37, p. 6771.

36. **Hunter, John.** *Fluid Jet contouring of SiC.* Ottawa, Ontario, Canada : LightMachinery, July 2007.

37. *High-quality grinding of polycrystalline silicon carbide sphereical surfaces.* **Yin, Ling, et al.** 2004, WEAR, Vol. 256, pp. 197-207.

38. *High quality grinding of polycrystalline silicon carbide spherical surfaces.* **Yin, L. et al.** 2004, WEAR, Vol. 256, pp. 197-207.

39. *Ductile-Regime Grinding: A New Techonlogy for Machining Brittle Materials.* **Bifano, T.G.** 1991, Journal of Engineering for Industry, Vol. 113, pp. 184-189.

40. *Hardness of nanocrystalline diamonds.* **Tse, J.S. et al.** 140102, 2006, Phys. Rev., Vol. 73.

41. *Chemomechanical Polishing of Silicon Carbide.* **Zhou, L., et al.** 6, June 1997, J. Electrochem. Soc., Vol. 144.

42. **Sze, S. M.** *Physics of Semiconductor Device, 2nd Ed.* New York : Wiley, 1981.

43. *Surface Flashover of Insulators.* **Miller, H. Craig.** 5, October 1989, IEEE Trans. on Electrical Insulation, Vol. 24, pp. 765-786.