EXPLORING THE CHARGE STORAGE PROPERTIES OF SUB-2 NM METAL NANOPARTICLES －APPLICATIONS IN FIELD EFFECT TRANSISTOR MEMORY AND DETECTION OF TRACE VAPOR MOLECULES

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by

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DEDICATION

I wish to dedicate this work to my loving parents, my brothers and sisters, and my wife Biyan Chen. Their love and company has always been my motivation and support for the exploration of life and science. Thank you.

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS ii

LIST OF FIGURES vii

LIST OF TABLES xiv

Chapter 1. Introduction 1

1.1 Sub-2 nm Metal Nanoparticles for Semiconductor Device and Sensor Applications 2

1.2 Scope of This Dissertation 6

Chapter 2. Theory 7

2.1 Analytical Model for the Metal-Insulator-Metal Tunneling Barrier 7

2.2 Helmholtz's free energy, Coulomb blockade and Quantum confinement 16

2.2.1 Classical SET – Coulomb Blockade vs. SET tunneling 19

2.2.2 Room temperature Classical SET 21

2.2.3 Quantum SET – Quantum Level Spacing 24

2.3 Calculation of Related Capacitance Terms of Nanoparticles 28

2.3.1 Sphere to Plane Model 28

Chapter 3. Sub-1 nm Gold Nanoparticle-based Single-Electron Transistors at Room Temperature 30

3.1 Introduction 31

3.2 Experiment 34

3.3 Discussion 36

3.3.1 Au NP number estimation 36

3.3.2 Role of pentacene layer in electronic properties 37

3.3.3 Electron addition energy and quantum level spacing 40

3.4 Future Work 46

Chapter 4. Barrier Modification of Metal-contact on Silicon by Sub-2 nm Platinum Nanoparticle (Pt NPs) 47

4.1 Introduction 47

4.2 Experiment 50

4.3 Discussion 51

4.3.1 Role of thin dielectric layers (SiO_2 and Al_2O_3) in barrier height reduction 52

4.3.2 Role of different stacking configuration & metal 55

4.3.3 Role of Pt NPs embedded between SiO_2 and Al_2O_3 thin oxide in barrier modification 60

4.4 Future Work 63

Chapter 5. Effect of Sub-1 nm Pt NPs on Doping/Strain of Single-Layer-Graphene Field-Effect Transistor 64

5.1 Introduction 64

5.2 Experiment 67

5.3 Discussion 69

5.3.1 Pt NP size determination and growth mechanism on graphene 69

5.3.2 Electrical characterization of Pt NP-Graphene based FETs 72

5.3.3 Raman Spectroscopy Study 77

Chapter 6. Organic non-volatile memory with embedded sub-nanometer Pt NPs 82

6.1 Introduction 82

6.2 Experiment 83

6.3 Discussion 85

6.3.1 Transistor Characteristics 85

6.3.2 Observation of Size Dependent Effective Work Function of Pt NP Layer in an OFET Architecture 88

6.3.3 Electrically charging and discharging behavior via sub-2 nm Pt NPs 91

Chapter 7. Pentacene OFET-based Detector for Trace Vapor Explosive Detection 97

7.1 Introduction 97

7.2 Experiment 99

7.3 Discussion 104

Chapter 8. Vapor Phase Molecular Imprinting on Pentacene OFET based Vapor Detector 112

8.1 Introduction 112

8.2 Experiment 114

8.2.1 Organic field-effect-transistor fabrication 114

8.2.2 Molecular imprinting method 116

8.2.3 Measurement system 117

8.3 Discussion 119

8.3.1 Transistor characteristics 119

8.3.2 Change in transfer characteristics after molecular imprinting 120

8.3.3 Selective detection of 2, 4-dinitrotoluene 121

8.4 Future Work 124

REFERENCES 125

LIST OF PUBLICATIONS 135

VITA 137

LIST OF FIGURES

Figure 2-1 Schematics of energy band diagram for the metal-insulator (vacuum)-metal tunneling junction with asymmetrical barrier height of nanoelectrodes: (a) $V = 0$; (b) $-\varphi L < V < 0$ for direct tunneling; (c) $V < -\varphi L$ for Fowler-Nordheim tunneling; (d) $0 < V < \varphi R$............ 8

Figure 2-2 I-V characteristics for the metal-insulator (vacuum)-metal nanogap tunneling junction using the same fitting parameters as [26]. 10

Figure 2-3 Simulated I-V characteristics for the metal-insulator (vacuum)-metal nanogap tunneling junction using the same fitting parameters as shown in [26]............ 11

Figure 2-4 Simulated I-V characteristics for the Metal-Insulator (Vacuum)-Metal Nanogap tunneling junction with symmetric barrier heights of 4.5 eV............ 12

Figure 2-5 Equivalent circuit of a single island tunneling device with source, drain and gate electrodes............ 16

Figure 2-6 Comparison of Coulomb Blockade vs. SET tunneling modes for a Classical SET. 19

Figure 2-7 Typical classical three terminal SET stability plot with Coulomb diamond pattern and I_D-$V_{is}(V_g)$ characteristics showing the Coulomb oscillation. (Inset: the corresponding equivalent circuit) 21

Figure 2-8 Effect of temperature to the stability plot of a SET with a 0.98 nm Au NP as an island 22

Figure 2-9 Comparison of simulated stability plot of 0.98 nm Au NP SET with (a) Al_2O_3 (b) SiO_2, and (c) air, at 300 K. 23

Figure 2-10 Schematics showing the size dependent quantum-level spacing. 24

Figure 2-11 Theoretical Coulomb Charging Energy (●), the Quantum Confinement Energy level spacing (■), total electron addition energy (▲), and the estimated numbers of atoms vs. the NP diameter (/). The dotted line indicates the thermal energy at T = 300 K.. 25

Figure 2-12 Comparison of energy band diagram of (a) Classical SET vs. (b) Quantum SET. 26

Figure 2-13 Comparison of simulated stability plot of a (a) classical SET vs. (b) quantum SET with equal QCE vs. (c) quantum SET with unequal QCE at 4.2 K. 27

Figure 2-14 Comparison of I-V characteristics of a (a) classical SET vs. (b) quantum SET with quantum staircase effect. 28

Figure 2-15 Schematics of a sphere-plane capacitor for (left) a gate electrode coupled to a single NP (right), which is an embedded NP coupled to a source or drain electrode. ... 28

Figure 2-16 Calculated bottom-gate-NP capacitance vs. NP size and dielectric thickness (SiO_2 or pentacene). The cyan rectangle is the possible tunneling capacitance range of our SET studied in 2.3. In this region (0.5 nm < NP diameter < 1.5 nm, 5 nm < dielectric thickness < 20 nm), the tunneling capacitance is dependent on the NP size and somewhat independent of the dielectric thickness. 30

Figure 3-1 (a) Schematic of SET device structure; (b) SEM image of the e-beam patterned nanoelectrodes (scale bar 20 μm); inset: nanoelectrode structure with 12 nm gap. The two side gates were not used in this study; (c) Transmission electron microscopy image of 0.86 nm Au NPs with the inset showing the Au NP size distribution. The scale bar is 20 nm; (d) AFM images of Au nanoelectrodes after pentacene deposition. 34

Figure 3-2 (**a**) Drain current vs. gate voltage characteristics of the devices with: (1) 0.86 nm Au NP and pentacene capping layer, (2) pentacene capping layer only, and (3) 0.86 nm Au NP only; (**b**) Energy band diagram for the biased SET. 37

Figure 3-3 (a) Experimental and (b) simulated 2-D stability plot of dI_D/dV_D vs. V_D and V_G for V_G from -14.5 V to -11 V at 300 K; (c) I_D vs. V_G plot with different V_D showing V_G modulation of Coulomb oscillation at 300 K, arrows indicate Coulomb blockade valleys; and (d) I_D vs. V_D plot with V_G = 12.3 V showing quantum confinement staircases. 40

Figure 4-1 TEM image of 1.11 nm TTS-deposited Pt NPs. 51

Figure 4-2 Comparison of Ti-p Si contact with different thicknesses and types of dielectrics (a) Ln (J)-V characteristics. Inset: Schematics of device structures; (b) the Richardson plots; (c) the barrier heights; (d) schematics of energy band diagram showing the barrier reduction of Ti-p Si contact by insertion of thin dielectrics. 55

Figure 4-3 Comparison of ln(J)-V and ln(J)-ln(V) characteristics for (a, b) Ti-Al_2O_3-p Si contact with and without 0.74 nm Pt NPs between the Al_2O_3 and Si surface; (c, d) Ti-SiO_2-p Si contact with and without 0.74 nm Pt NPs between the Ti electrode and SiO2

surface; (e, f) Au-SiO_2-p Si contact with and without 0.74 nm Pt NPs between the Au electrode and SiO2 surface; Inset: Schematics of the device structures. (g) Schematics showing the dipole formation between Ti electrode and Pt NP. (h, i) Schematics of energy band diagram showing the reduction of depletion width with the presence of Pt NPs. 59

Figure 4-4 Comparison of (a) C_D-V, (b) G_P-V, and (c) depletion width Ti-Al_2O_3-p Si contact with and without 0.74 nm Pt NPs (10s). 59

Figure 4-5 Comparison of Ti-p Si contact with different sizes of Pt NPs sandwiched between the 0.98 nm Al_2O_3 and 1.6 nm SiO_2 (a) Ln(J)-V characteristics. Inset: Schematics of device structures; (b) Ln(J)–Ln(|V|) characteristics; (c) the Richardson plots; (d) schematics showing the dipole formation between Ti electrode and Pt NP; (e) Equivalent circuit of the device showing the Coulomb blockade effect; (f, g) schematics of energy band diagram showing the electron wave penetration and the reduction in depletion width with the presence of Pt NPs. 63

Figure 5-1 Device schematics of graphene FET (a) without and (b) with Pt NPs deposited on top of graphene. (c) R-E characteristics of control sample before and after H_2 annealing. 68

Figure 5-2 Comparison of resistance-electric field characteristics for devices with and without conduction channel modification by different sizes of Pt NPs 72

Figure 5-3 Schematic of changes in energy band diagram for graphene-based FET before (a, c) and after (b, d) Pt NP deposition: (a, b) device with 0.5 nm Pt NP layer showing n-

type doping behavior; (c, d) device with 1.1 nm Pt NP layer showing no doping behavior. 75

Figure 5-4 Representative Raman spectra of the control graphene sheet (curve a) and after depositing 0.5 nm Pt NPs (curve b) with 1.1 nm Pt NPs (curve c) on top. 79

Figure 6-1 (a) Schematic illustration of pentacene FET; (b) plane view TEM image of uniformly distributed 1.30 nm Pt NPs with scale bar: 20 nm (Inset: frequency distribution of 1.30 nm Pt NP). 85

Figure 6-2 (a) and (b) Output characteristics of (a) control device and (b) device with embedded 1.3 nm Pt NPs; (c) and (d) Comparison of pentacene FET transfer characteristics without and with Pt NPs measured at -2.5 V drain voltage with gate voltage sweeping from (c) 0.5 V to -1 V and (d) 2 V to -4 V.. 87

Figure 6-3 Energy band diagram of pentacene FET with embedded Pt NPs under flat band condition.. 89

Figure 6-4 (a & b) Memory behavior of pentacene FET (a) without and (b) with 1.3 nm Pt NPs measured at -2.5 V drain voltage and sweeping gate voltage; (c) threshold voltage shift and (d) memory window under different gate bias sweeping for sample with different size Pt NPs.. 93

Figure 7-1 Pentacene-based OFET: (a) Schematic of device structure; (b) actual devices with different width length ratios and sensor within a dual-inline package for sensing; (c) schematics of analyte vapor generation and in situ vapor detection system.................... 99

Figure 7-2 (a) Comparison of sensor response to various concentrations of DNT sensors with different sizes of Pt NPs (0.5, 1.3 and 1.8 nm diameters). The exposure time for DNT and dry air are about 3 min and 5 min separately. The output signal in y-axis is calculated by Id/Id_0, where Id is the drain current measured under -2.5 V of gate voltage and -2.5 V drain voltage. Id_0 is the initial value of the drain current. (b) Percentage change in drain current versus DNT concentration retrieved from the data set of sample with embedded 1.3 nm Pt NPs of **Figure 7-2** (a). 102

Figure 7-3 Schematics of energy band diagram of device with different sizes of Pt NPs under zero gate bias. (EA of Pt NPs with different sizes were adopted from [117]; EA of DNT is adopted from [118]) 107

Figure 7-4 Sensor response to 500 ppb of 2,4-dinitrotoluene for sensors with embedded 1.3 nm Pt NPs: (a) Comparison of change in drain current under different gate voltages (-5, -2, and -1 V); (b) change in mobility (left y-axis) and change in hysteresis (right y-axis); (c) change of threshold voltage under different sweeping direction of gate bias at drain voltage of -2.5 V. (Refer [15] for the mobility and hysteresis determination)...... 109

Figure 8-1 Schematic of pentacene-based OFET: (a) device configuration; (b) device-in-sensor package; and (c) AFM scan of OTS-treated surface (5 × 5 μm area) showing grain morphology of the pentacene layer... 114

Figure 8-2 Illustration of vapor phase molecular imprinting of organic semiconductor. Red dots indicate exposed target-selective functional groups within the imprinted polymer. 116

Figure 8-3 Experimental setup for sensor characterization and in-situ vapor detection.118

Figure 8-4 (a) Output characteristics and (b) transfer characteristics of pentacene-based OFET with 50:1 width: length ratio. 119

Figure 8-5 Changes in OFET transfer characteristics before and after DNT saturation and after 254 nm UV exposure for 15 min and 120 min. 120

Figure 8-6 (a) Comparison of drain current response of the pentacene OFET sensor against various concentrations of DNT vapor before and after vapor phase MIP; (b) drain current response of the imprinted pentacene OFET sensor toward target and interfering analytes (black: 300 ppb DNT [target]; red: 260 ppb DNB; blue: 300 ppb NB, and pink: 300 ppb Nicotine). 123

LIST OF TABLES

Table 2-1 Simulation parameters and characteristic values of **Figure 2-9**. 22

Table 2-2 Simulation parameters and characteristic values of **Figure 2-10**. 23

Table 4-1 Summary of the Pt NP conditions used in this study...................................... 51

Table 5-1 Summary of average G and 2D peaks positions taken at five separate points across the samples and the G and 2D peak shift magnitudes with the uncertainty for each condition (based on the propagation of errors method) in **Figure 5-4**. 79

Table 6-1 Experimentally derived effective work function of different size Pt NPs embedded within the Al_2O_3 dielectric.. 91

Table 6-2 Summary of pentacene NVM device memory characteristics without and with embedded Pt NPs 96

Table 7-1 Summary of Platinum NPs properties with different sizes............................ 107

Table 8-1 Changes of various OFET sensor parameters during molecular imprinting process.. 124

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ABSTRACT

Sub-2 nm size metal nanoparticles are unique compared to their bulk counterparts in semiconductor device and sensor applications due to their size-dependent behaviors, such as Coulomb blockade effect, quantum confinement effect, and the size-dependent work function. In this thesis, the single electron charging behaviors of these nanoparticles are studied through the room temperature operable single charge tunneling devices. Further, by embedding these nanoparticles as discrete charge storage sites in a macroscopic organic field-effect transistor, the electron or hole charging behaviors due to the nanoparticle size-dependent work function are investigated. These memory devices are utilized as sensitive trace vapor detector with the embedded nanoparticles as detection sites. Lastly, the application of these nanoparticles as charge injection hotspots for achieving ideal Ohmic metal-semiconductor contacts, and the doping effects of the nanoparticles to the conduction channel of 2D material-based field effect transistors are studied.

Chapter 1. Introduction

Metal nanoparticles (MNPs) have attracted great interest in different areas due to their unique electrical and physical-chemical properties at the nanoscale [1]–[4]. Bulk electrical phenomena expected of metals (e.g., Ohm's Law) also lose validity as the electron bands become discretized due to quantum confinement [3]. Adding single charges to MNPs costs energy because the energy levels can no longer be considered as continuous, as in the case of bulk metals [3]. The properties that separate MNPs from their conducting bulk metal counterparts are derived from their physical dimensions, including surface-to-volume atom ratio, free electron density, quantized energy level, charging energy, and surface-dipole-enhanced local electric field [5]–[7]. By utilizing the size-dependent behavior of sub-nm MNPs, room temperature operable single charge storage devices can be developed. Because of these excellent charge storage and catalytic properties, MNPs have found roles in integrated electronic/electrochemical device architectures, in which they function as discrete charge storage or catalytic materials [4], [7]–[9]. By embedding MNPs as discrete charge storage sites in a macroscopic field-effect transistor, the program/erase lifetime and retention rate can be improved significantly when compared to traditional floating gate memory.

A large fraction of the atoms in an MNP contain only a few hundred atoms and are located on the surface. These surface atoms are more electrically and electrochemically active due to the fact that they are less coordinately saturated [10]. Charges in a charged MNP also tend to distribute on the outer perimeter of the MNP surface due to the electrostatic interaction and formation of a surface electric dipole with the environmental

charges [11]. The smaller the nanocrystal, the larger the resultant electric field enhancement due to this surface electric dipole and a corresponding change in the MNP work function at their surface, a property that is especially powerful for MNPs in the sub-2 nm diameter regime. The size-dependent work function leads to important applications of MNPs as catalytic molecules and in trace vapor explosive molecule detection since MNPs with dipole-enhanced surface electric field and proper work function facilitate charge transfer between molecules [12]–[14]. MNPs with a large surface electric dipole due to their interaction with other metal or semiconductors also tend to modulate the localized electric field, thus allowing their use for barrier modulation of a macroscopic metal-semiconductor contact or doping 2-D materials such as graphene [15], [16].

1.1 Sub-2 nm Metal Nanoparticles for Semiconductor Device and Sensor Applications

Noble metal nanoparticles (MNPs) have proven advantageous over semiconductor clusters and organic molecules in single-electron transistor (SET) applications due to their higher environmental stability, greater density of states, and mature fabrication techniques [5]–[7]. Theory predicts that MNP dimensions less than 1 nm are required for the quantum confinement energy to surpass the room temperature (RT) thermal noise sufficiently enough to probe single electron quantum excitation states [17]–[19]. Meanwhile, the relatively small electron charging energies of MNP-based SET devices have so far prevented clear RT observation of these Coulomb oscillations and quantum confinement states [17]–[19]. This dissertation is based on the study of controlled deposition of sub-2 nm MNPs by a recently developed tilted target sputtering (TTS) process as well as their applications for single charge storage [5], [7], [12], [20], multi-bit memory [21], metal-

semiconductor contact modification, graphene conduction channel modification [15], [16] and trace explosive vapor detection [13]. MNP sizes and areal densities are controlled by varying the TTS deposition time and deposition (RF) power [22]. Using TTS-deposited MNPs as discrete charge storage nodes, their ultra-small sizes provide the ability to observe and control charge storage and transfer down to the single electron level at ambient temperature (300 K). SET devices incorporating single ~1 nm Au nanoparticles (Au NPs) as a charge transport island were used to study the quantum Coulomb blockade and quantized energy level spacings at room temperature (300 K).

In order to observe the single electron charging behavior of MNPs in macroscopic devices, a device schematic was proposed in which size-tunable sub-2 nm Pt nanoparticles (Pt NPs) were embedded between the tunneling and blocking dielectric layers of a low operation voltage pentacene transistor non-volatile memory (NVM). Controllable work function was observed in the embedded Pt NPs through the size-dependent threshold voltage shift. Non-volatile memory transistors containing embedded Pt NPs exhibited size- and density-dependent memory windows in their transfer characteristics, which was attributed to electron and hole charging and discharging behavior. While devices with small (0.5 nm) Pt NPs demonstrated strong Coulomb blockade and quantum confinement with electron addition energy as large as 1.993 eV, those made with larger (1.8 nm) Pt NPs, allowed for storage of a single charge per NP memory. Pentacene NVM with embedded sub-2 nm Pt NPs were also studied for sensitivity towards trace nitroaromatic explosive vapors. Exploiting the unique electronic properties of Pt NPs, a detection limit of 56.6 parts per billion of 2,4-dinitrotoluene (DNT) vapor was demonstrated while control samples without Pt NPs showed no observable sensitivity to DNT vapor. This remarkable

sensitivity has been attributed to the ability of sub-2 nm Pt NPs to function as discrete nodes participating in charge transfer with adsorbed nitroaromatic molecules. Pentacene-based FET sensor device selectivity was further improved by a vapor phase molecular imprinting (MIP) technique developed and reported below. This OFET-based sensor using pentacene as the molecularly imprinted monomer showed enhanced selectivity to DNT vapor against various interfering analytes. This method can be extended to improve the selectivity of most OFET- and chem-resistor-based sensors without adversely affecting device electronic properties, which is promising for the development of highly selective, low-cost, flexible OFET sensors.

Sub-2 nm MNPs with enhanced localized electric field also find application in barrier modification of the metal-semiconductor contact. One longstanding issue in fabrication of semiconductor devices is Fermi level pinning of the semiconductor at the metal-semiconductor interface. Selecting metals with different work functions provides only limited control over Ohmic contact or Schottky contact barrier height. Extensive studies have demonstrated the benefits of using reduced metal-semiconductor contact resistance using thin insulating tunnel barriers with fixed charges [23], [24]. However, the optimal insulating layer thickness (e.g. ~1 nm for Al_2O_3) is difficult to fabricate and thicker insulator layers increase the contact resistance due to reduction in tunneling probability. Dielectric layers below this thickness are generally unreliable due to surface discontinuities. In this study, the metal-semiconductor contact barrier is controlled by the introduction of sub-2 nm Pt NPs) deposited by TTS. We show the size-dependent Pt NP properties and their role in Fermi level depinning at the metal-silicon interface with a 0.98 nm Al_2O_3 or 1.6 nm SiO_2 dielectric layer. The initial study demonstrated that samples

modified with 0.74 nm Pt NPs show >10^3 times higher current density compared to a Ti-thin oxide-Si contact (control). It also further revealed that the contact can be modulated to be either Schottky or Ohmic using the same contact metal by varying only Pt NP size and areal density.

Another application of MNPs with enhanced localized electric field is in conduction channel modification of 2-D material-based FETs. Graphene's promising electronic properties make graphene-based transistors attractive platforms for future devices. It is well documented that graphene exhibits ballistic transport at the submicron scale and can be doped heavily using a multitude of techniques without significant loss of mobility [25]. Meanwhile, choosing the same metal as the contact electrode for doping is sometimes preferable over using other destructive techniques to minimize contamination. In this report, the doping/strain introduced by ultrafine sputtered Pt NPs of different sizes on single layer graphene has been studied through conduction channel modification of graphene-based FETs and their Raman characterization. For sub-nm (0.5 nm) diameter Pt NPs, a substantial Dirac point shift was observed in the I-V characteristics, suggestive of *n*-type doping of the large area single layer graphene through the process of charge transfer and chemical interaction. Conversely, for larger (1.1 nm) Pt NPs, a minimal Dirac point shift was observed, indicating lack of the charge transfer-induced doping effect. The representative Raman signatures corroborate with the electrical characterization results and indicate that while charge transfer dominates Raman peak shift for the 0.5 nm Pt NP decorated graphene, strain effect dominates in case of the larger 1.1 nm Pt NP.

1.2 Scope of This Dissertation

This dissertation is divided into eight chapters dealing with the different applications of sub-2 nm MNPs in semiconductor device and trace vapor molecule sensor systems. **Chapter 2** starts with discussion of theories and concepts that will be used throughout the dissertation. Subtopic **2.3** discusses the size-dependent charging energy and quantum level spacing of sub-1 nm Au NP and its application in room temperature operable SET devices. **Chapter 4** discusses the barrier modification of metal-silicon contact by sub-2 nm Pt NPs as an alternative to reduce contact resistance and improve current injection in semiconductor devices. While exploring the interaction of MNPs on a metal-semiconductor interface, **Chapter 5** discusses the effects of sub-1 nm Pt NPs on doping/strain of single layer graphene and its role in modulating the conduction properties of a graphene-based FET. **Chapter 6** discusses the utilization of sub-2 nm Pt NPs to achieve low operation voltage pentacene-based NVM by embedding them between the tunneling and blocking dielectric layers. The observation of the controllable effective work function of the Pt NP layer through the size-dependent threshold voltage shift was also discussed. Further exploration of pentacene NVM with embedded Pt NPs for improving the sensitivity of detection toward trace vapor explosives and the NP size-dependent charge interaction with analytic molecules are discussed in **Chapter 7**. **Chapter 8** discusses the development of a vapor-phase molecular imprinting method to further improve the selective detection capability of pentacene FET-based sensors. The terms nanoparticle (NP), island, nanocluster (NC) and quantum dot may be used interchangeably throughout the context of this dissertation when appropriate.

Chapter 2. Theory

2.1 Analytical Model for the Metal-Insulator-Metal Tunneling Barrier

In classical mechanics, if the energy of a particle E is smaller than the maximum height of the potential barrier V of a quantum well, the particle remains in the well forever. Whereas in quantum mechanics, an electron can escape even if its energy E is below the height of the barrier V. Quantum tunneling has no counterpart in classical physics.

For designing a SET device, it is a good practice to have some idea on the tunneling current level of a metal-insulator-metal (MIM) barrier without the charge storage island. Analytical models have been well developed by earlier works and used to estimate the current level. Mangin et al. [26] showed that the tunneling resistance is not only determined by the width of the barrier, but is also due to the strong function of the barrier height of the electrodes on both sides. Namely, one cannot determine the size of the nanogap simply by evaluating the resistance under low bias condition (direct tunneling). However, for determining the tunneling resistance for an SET working in a single electron tunneling region (low bias), we assume that the barrier height is relatively high, and the barrier is in a rectangular shape (direct tunneling).

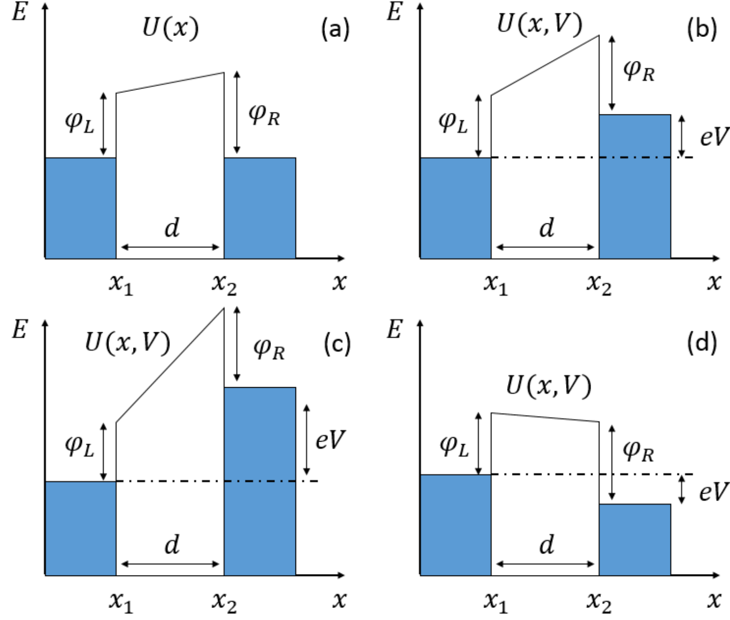


Figure 2-1 Schematics of energy band diagram for the metal-insulator (vacuum)-metal tunneling junction with asymmetrical barrier height of nanoelectrodes: (a) $V = 0$; (b) $-\varphi_L < V < 0$ for direct tunneling; (c) $V < -\varphi_L$ for Fowler-Nordheim tunneling; (d) $0 < V < \varphi_R$.

Figure 2-1 shows the schematics of an energy band diagram for the metal-insulator (vacuum)-metal nanogap tunneling junction with an asymmetrical barrier height of nanoelectrodes under different bias conditions. The potential profile of the insulating gap between the nanoelectrodes under applied voltage V is given by

$$U(x,V) = \varphi_L + \frac{\varphi_R - \varphi_L - eV}{d} * x\,, \qquad x_1 < x < x_1 + d \tag{2-1}$$

The wave function of an electron ψ is determined by the Schrodinger equation [27]

$$\frac{d^2\psi}{dx^2} + \frac{2m^*}{\hbar^2}[E - U(x)]\psi = 0, \tag{2-2}$$

where m^* is the electron mass and $\hbar$ is the Planks constant. By using the Wentzel Kramers Brillouin (WKB) approximation, the electron transmission probability across the nanogap

$T(E,V)$ is given by [26]

$$T(E,V) = \frac{|\psi_R|^2}{|\psi_L|^2} \approx exp\left\{- \int_{x_1}^{x_1+d} \frac{4\pi}{\hbar} \sqrt{2m^*[U(x,V) - E]}\, dx\right\} \quad (2\text{-}3)$$

where E is the total energy of an incoming electron under a bias voltage of V. Assuming the constriction is ballistic with a size comparable to the Fermi wavelength λ_F with a single transmission channel, a one dimensional model is used in this study. Considering the electron tunneling in the nanogap as a scattering problem, the tunneling current is calculated by applying the Landauer-Buttiker formalism, which is determined by

$$I(V) = \frac{2e}{\hbar} \int_0^{+\infty} [F(E) - F(E - eV)] * T(E,V)\, dE \quad (2\text{-}4)$$

where $F(E)\ and\ F(E - eV)$ are the Fermi-Dirac distribution of electrons in the electrodes under thermal equilibrium and an applied voltage V, respectively. $f(E)\ and\ f(E - eV)$ are given, respectively, by [27]

$$F(E) = \frac{1}{1+exp(\frac{E-E_F}{kT})} \quad and \quad F(E - eV) = \frac{1}{1+exp(\frac{E-E_F-eV}{kT})} \quad (2\text{-}5)$$

where E_F is the Fermi level of the electrode (in the case of this work, gold).

A typical I-V characteristics of an MIM nanogap fabricated by performing a controlled electro-migration on an e-beam deposited gold nanobridge, measured and simulated by Mangin et al. can be found in [26]. The parameters used by the paper for fitting are as follows: Gap size: 1.2 nm, barrier height for the two sides: left 0.29 eV and right 0.95 eV, respectively, with a tunneling area of 10 nm^2. Note that the reduced barrier is drastically lower than the usually reported experimental work function of gold (~5.1–5.3 eV). According to the author, this reduced barrier height could be due to surface contamination.

By using the model given in Eq.(2-4) and using the same parameters given above, a simple MATLAB® code was written to obtain the simulated IV characteristics shown in **Figure 2-2**. The results are comparable to what is in [26].

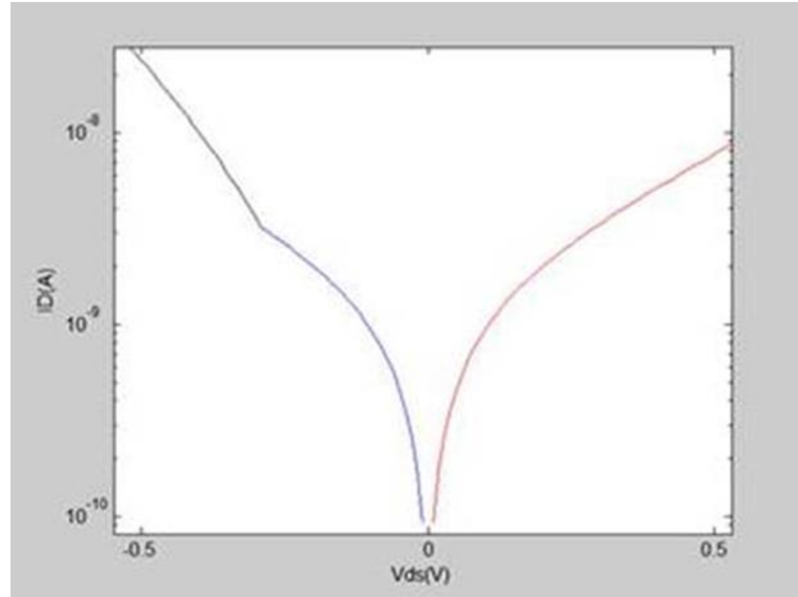


Figure 2-2 I-V characteristics for the metal-insulator (vacuum)-metal nanogap tunneling junction using the same fitting parameters as [26].

If we assume having a similar nanogap to the one in [26] with an asymmetric barrier height of left 0.29 eV and right 0.95 eV, except for ranging the gap size from 1 nm to 10 nm, with a 1 nm step size, the simulation result is found to be the same as that shown in **Figure 2-3**. For a 10 nm gap, 5 to 10 V is expected to give a 1 x 10^{-10} to 1 x 10^{-8} A of current level. In comparison, **Figure 2-4** shows the results for symmetric barrier heights of 4.5 eV for both sides of the electrode. This model is only applicable for a device operating before the avalanche breakdown takes place, in which condition the configuration of the nanogap might change permanently due to electron migration. So in our study, we operated the device within 1 x 10^{-8} A of compliance current.

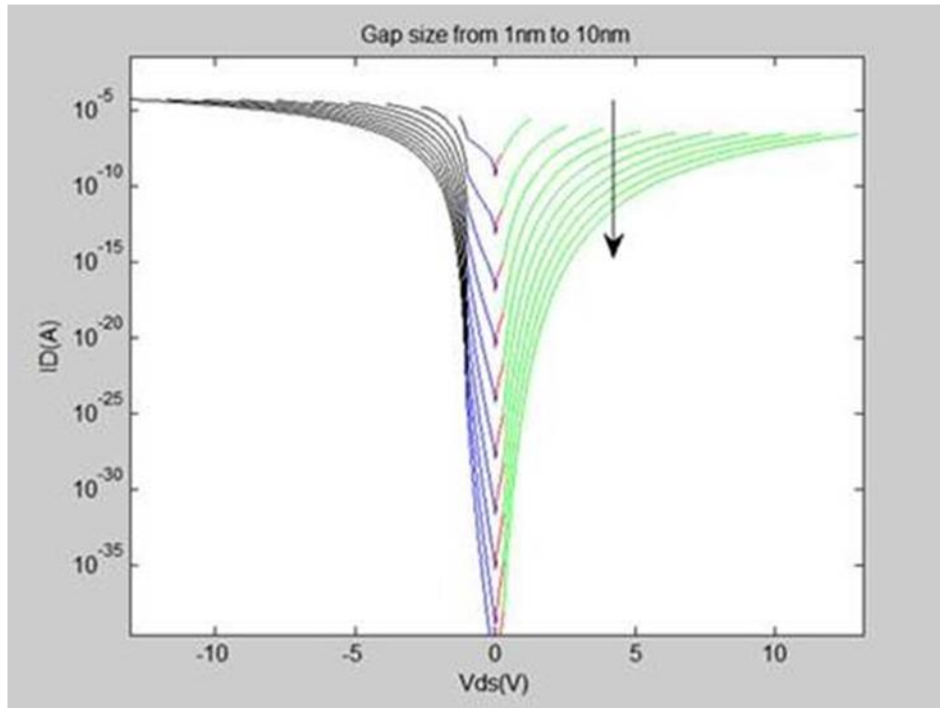


Figure 2-3 Simulated I-V characteristics for the metal-insulator (vacuum)-metal nanogap tunneling junction using the same fitting parameters as shown in [26].

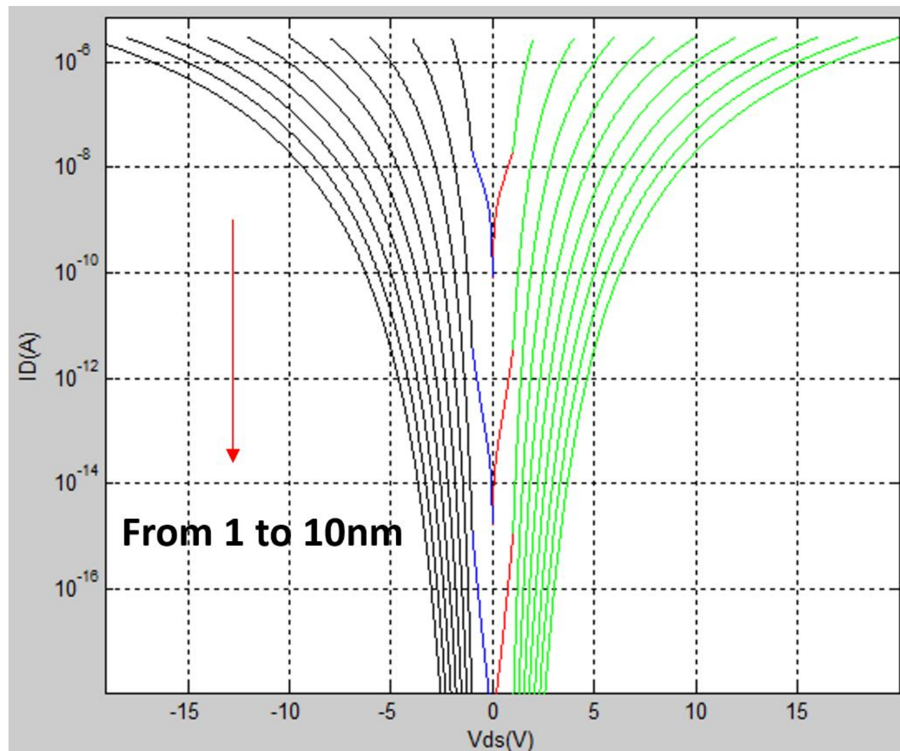


Figure 2-4 Simulated I-V characteristics for the Metal-Insulator (Vacuum)-Metal Nanogap tunneling junction with symmetric barrier heights of 4.5 eV.

The MATLAB code used for the above simulation is given as follows:

```
%% Modeling of MIM nanogap tunneling junction

clear;clc;

%% Defining constants

PI=3.1415926535897932;       %   Pi constant
Q=1.60217733E-19;            %   Electronic charge [C]
TEMP=300;                    %   Temperature [K]
KB1=1.380658E-23;            %   Boltzmann's constant [J/K]
KB2=8.6174E-5;               %   Boltzmann's constant [eV/K]
KT=0.0256;                   %   Thermal energy [eV]
HP1=6.62617E-34;             %   Plank's constant [J*s]
HP2=4.1357E-15;              %   Plank's constant [eV*s]
e=2.7183;
Me=9.1095e-31 *1;            %   Relative Effective electron mass of insulator * free
electron mass [kg]
Me_AL2O3 = Me *0.25;         %   Effective electron mass of al2o3

EP_SIO2=3.9;                 %   Relative permittivity of SiO2
```

```
EP0=8.8542E-12;              %   Vacuum permittivity [F/m]

%% Defining Parameters

%syms Vds;
FIL=4.5;                     %   Barrier height of left electrode [eV]
FIR=4.5;                                                    %   Barrier   height   of   left   ele
ctrode [eV]

V1R=0:0.01:FIR;      %   Define the step size
V1L=-FIL:0.01:0;      %   Define the step size
ramp=0.5;
 VR= FIR:.01:(FIR+FIL)*ramp;              %   Define the step size
 VL=(-FIL-FIR)*ramp:.01:-FIL;              %   Define the step size

FIA1R=(FIR + FIL - V1R)./2;    %   Barrier height of left electrode [eV]
FIA1L=(FIR + FIL + V1L)./2;    %   Barrier height of left electrode [eV]

FIAR= FIL/2;    %   Barrier height of left electrode [eV]
FIAL= FIR/2;    %   Barrier height of left electrode [eV]

GAP=ramp*1e-9;                   %   Length of the gap [m]
GAP_CM=GAP*100;                   %   Length of the gap [m]
```

```
GAPW=3e-9;
GAPH=3e-9;

GAPR = abs((GAP * FIL) ./ (VR - FIR + FIL));
GAPL = abs((GAP * FIR) ./ (-VL + FIR - FIL));

J01 = Q^2/2/PI/HP1./ (GAP).^2;
J0R = Q^2/2/PI/HP1./ (GAPR).^2;
J0L = Q^2/2/PI/HP1./ (GAPL).^2;

C1 = 4* PI * sqrt(2*Me*Q) /HP1 .* (GAP);
CR = 4* PI * sqrt(2*Me*Q) /HP1 .* (GAPR);
CL = 4* PI * sqrt(2*Me*Q) /HP1 .* (GAPL);

T_AREA=GAPW*GAPH;
T_AREA_CM=T_AREA*1e4;
AREA_GAP_BOTTOM=T_AREA;
AREA_PAD=2.5E-7;        % Area of the electrode pad 5e-4m*5e-4m=2.5E-7m^2

CON_QT=2*Q^2/(HP1);         %   Quantum conductance [S]
R_QT=1/CON_QT;              %   Quantum resistance  [R]

%% the low voltage tunneling current
```

```
J1R = J01 .* FIA1R .* exp(-C1.* sqrt(FIA1R))   -   J01 .* (FIA1R+V1R) .* exp(-C1.* sqrt(FIA1R+V1R));

J1L = J01 .* FIA1L .* exp(-C1.* sqrt(FIA1L))   -   J01 .* (FIA1L-V1L) .* exp(-C1.* sqrt(FIA1L-V1L));

JR = J0R .* FIAR .* exp(-CR.* sqrt(FIAR))   -   J0R .* (FIAR+VR) .* exp(-CR.* sqrt(FIAR+VR));

JL = J0L .* FIAL .* exp(-CL.* sqrt(FIAL))   -   J0L .* (FIAL-VL) .* exp(-CL.* sqrt(FIAL-VL));


I1R = T_AREA * J1R;

I1L = T_AREA * J1L;

IR = T_AREA * JR;

IL = T_AREA * JL;


J1R_CM = J1R *1e-4;

J1L_CM = J1L *1e-4;

JR_CM = JR *1e-4 ;

JL_CM = JL *1e-4 ;


%%

figure

semilogy (V1R,I1R,'r-',V1L,I1L,'b-',VR,IR,'G-',VL,IL,'k-');
```

2.2 Helmholtz's free energy, Coulomb blockade and Quantum confinement

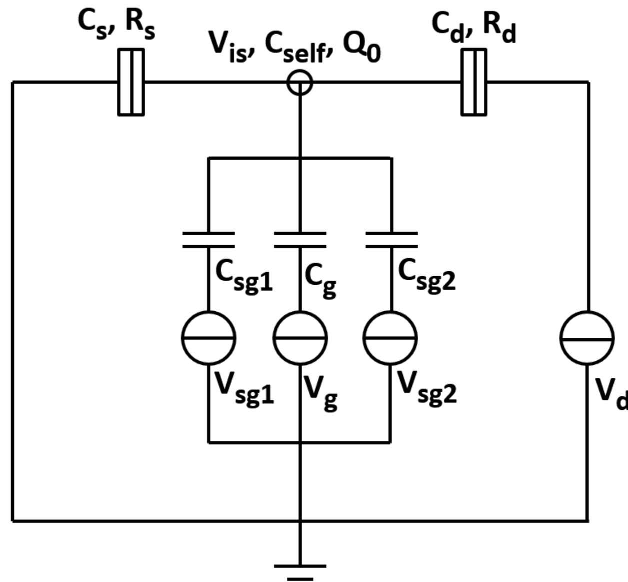


Figure 2-5 Equivalent circuit of a single island tunneling device with source, drain and gate electrodes

For the single island tunneling device discussed in this dissertation, it usually consists of at least one electrode coupled to the island with a tunneling junction consisting of a thin dielectric and either another electrode with a tunneling junction or a gate electrode accompanied by a blocking dielectric. A tunneling junction is usually represented by a junction resistor and a capacitor in parallel. The gate electrode with a blocking dielectric is represented by a gate capacitance. **Figure 2-5** shows the equivalent circuit of a typical single island tunneling device with source and drain electrodes with two tunneling junctions, and a bottom gate electrode and two other side gate electrodes. Two other terminal single electron tunneling devices studied in this dissertation can be simplified from this model.

The energy that determines the charge transport to the SET is described by Helmholtz's

free energy (F) [17]:

$$F = E_{\Sigma} - W \tag{2-6}$$

The total electron additional energy E_{Σ} (EAE) stored in a SET can be written as:

$$E_{\Sigma} = E_C + E_N \tag{2-7}$$

where E_C is the Coulomb charging energy (CCE), and E_N is the quantum confinement energy (QCE). The charge of the island is the sum of the charge induced by each electrode plus an initial offset charge:

$$Q = -Ne = Q_0 + V_{is}(C_s + C_{self}) + (V_{is} - V_d)C_d + (V_{is} - V_g)C_g + (V_{is} - V_{sg1})C_{sg1} + (V_{is} - V_{sg2})C_{sg2} \tag{2-8}$$

The electro static capacitive energy of the island with N excess electrons can be rewritten as:

$$U(N) = \frac{1}{2}C_{tot}V_{is}^2 = \frac{(-Ne - Q_0 + V_dC_d + V_gC_g + V_{sg1}C_{sg1} + V_{sg2}C_{sg2})^2}{2C_{tot}} \tag{2-9}$$

where the total capacitance is given by:

$$C_{tot} = C_s + C_d + C_g + C_{sg1} + C_{sg2} + C_{self} \tag{2-10}$$

The calculation of the capacitance terms will be discussed in the next session. To add the Nth electron to the island with N-1 electron, the energy required would be,

$$U_N(N) = U(N) - U(N-1) + E_N(N) \tag{2-11}$$

$$U_N(N) = \frac{e^2\left(N-\frac{1}{2}\right)}{C_{tot}} + \frac{eQ_0}{C_{tot}} - \frac{eV_dC_d}{C_{tot}} - \frac{eV_gC_g}{C_{tot}} - \frac{eV_{sg1}C_{sg1}}{C_{tot}} - \frac{eV_{sg2}C_{sg2}}{C_{tot}} + E_N(N) \quad (2\text{-}12)$$

By solving $U_N(N) = 0$ and $V_d = 0$, the degeneracy points can be calculated. Assuming one control gate is in use, i.e. V_{sg1} and V_{sg2} to be zero for simplification, the degeneracy points are:

$$V_g(N) = \frac{e\left(N-\frac{1}{2}\right)+Q_0}{C_g} + \frac{C_{tot}*E_N(N)}{C_g} \quad (2\text{-}13)$$

The periodicity of the conductance peaks in the Coulomb diamonds is:

$$T_g(N) = \frac{e}{C_g} + \frac{C_{tot}[E_N(N)-E_N(N-1)]}{C_g} \text{ or just } T_g(N) = \frac{e}{C_G} \quad (2\text{-}14)$$

depending on the filling of the electron shell structure of the quantum dot. For quantum dots with size larger than 100 nm, the CCE is negligible compared to the $\frac{e}{C_g}$ term and thus, $T_g(N)$ can be simplified as:

$$T_g = \frac{e}{C_g} \quad (2\text{-}15)$$

The peak positions of the Coulomb diamonds can then be determined by finding the following:

$$Max(U_N(N)) \quad (2\text{-}16)$$

Assuming a single electron charging condition, the peak energy values are:

$$E_{\Sigma}(N) = Max(U_N\,(N)) = \frac{e^2}{C_{tot}} + \Delta E_N(N) \quad \text{or just} \quad \frac{e^2}{C_{tot}} \tag{2-17}$$

For quantum dots with size larger than 100 nm again, this would become:

$$E_c = E_{\Sigma} = \frac{e^2}{C_{tot}} \tag{2-18}$$

2.2.1 Classical SET – Coulomb Blockade vs. SET tunneling

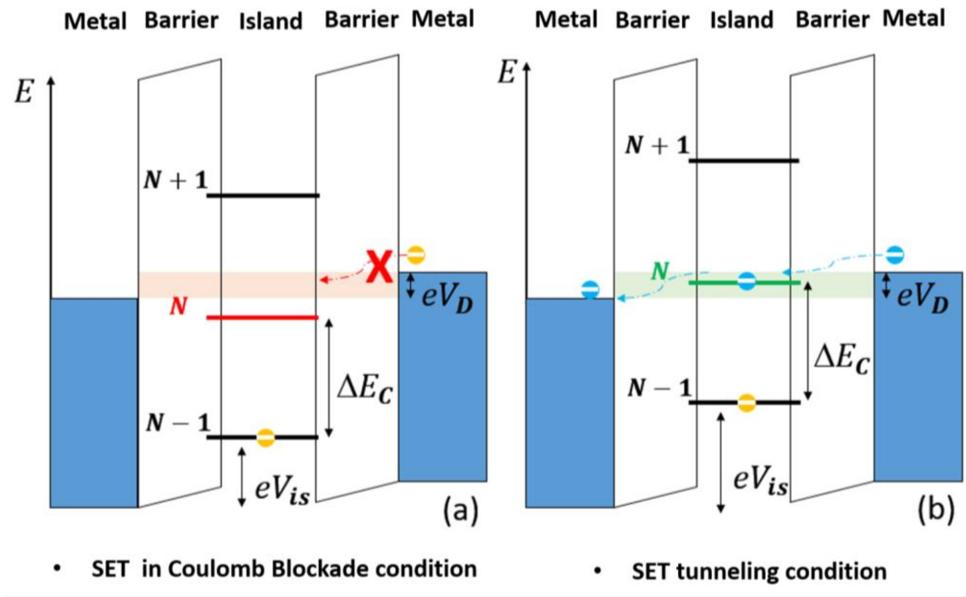
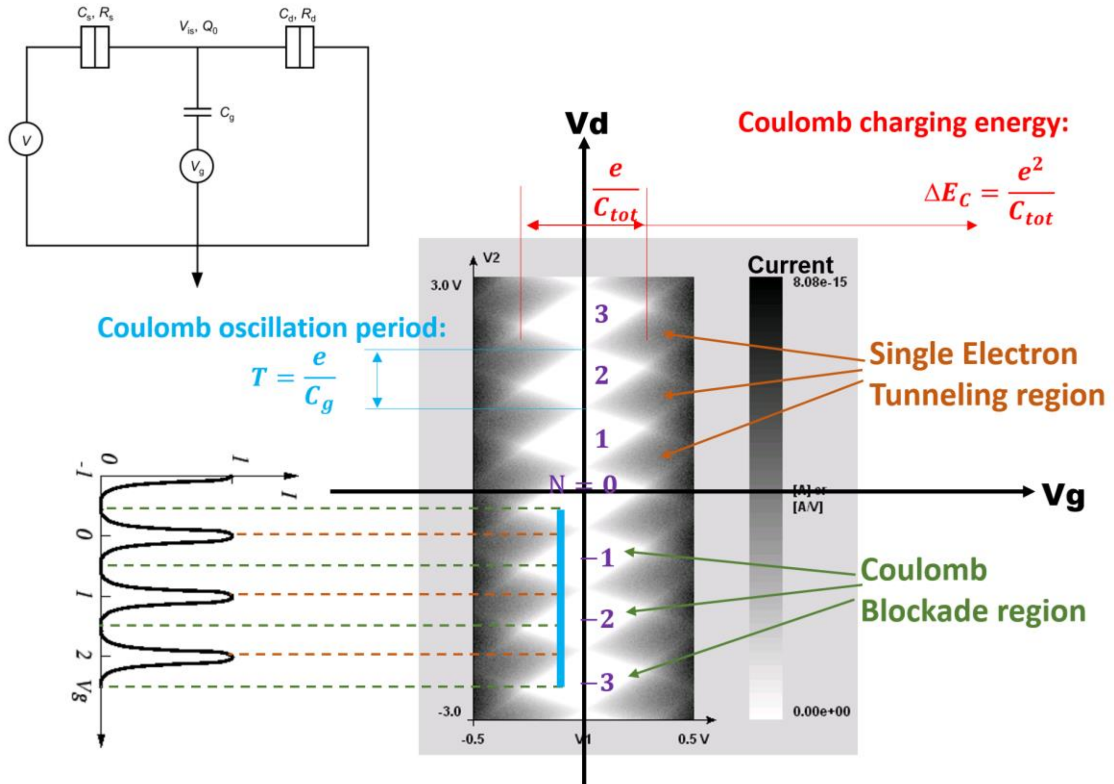


Figure 2-6 Comparison of Coulomb Blockade vs. SET tunneling modes for a Classical SET.

Figure 2-6 shows the energy band diagram comparing the Coulomb Blockade condition vs. SET tunneling condition for a three terminal classical SET where the QCE is ignored. The equivalent circuit is shown in the inset of **Figure 2-7**, which is a simplified condition of the one shown in **Figure 2-5.** The bias of source-drain electrodes V_D sets a window allowing charges to tunnel through the energy levels within, while tunneling through the levels out of the window is forbidden. A gate bias V_{is} offsets the potential of the island

energy levels (…, N+1, N, N-1, …0, …, -(N-1), -N, -(N+1), …). When no energy levels are within the tunneling window, the SET is under the Coulomb Blockade mode; when there is one energy level sitting within the window, the SET is under a single electron tunneling mode, during which one electron can either tunnel onto the island or tunnel out of the island, thus forming a single electron tunneling current. By shifting the gate bias V_{is}, it is possible to observe the periodic change between the two operation modes by measuring the Coulomb oscillation of the tunneling current. By plotting the 2D stability plot (V_D *vs.* V_{is} *vs.* I_D), a diamond like pattern can be observed which is a result of the boundary conditions of change between the two operation modes with respect to V_D and V_{is}. **Figure 2-7** shows a typical classical three terminal SET stability plot with the Coulomb diamond pattern and I_D-$V_{is}(V_g)$ characteristics showing the Coulomb oscillation, which is drastically different from the characteristics of traditional field effect transistors without the SET behavior.



- Conductance oscillates as a function of gate voltage – Coulomb blockade oscillations

Figure 2-7 Typical classical three terminal SET stability plot with Coulomb diamond pattern and I_D-$V_{is}(V_g)$ characteristics showing the Coulomb oscillation. (Inset: the corresponding equivalent circuit)

While it is possible to allow more than one electron to tunnel at a time when having a tunneling window larger than the separation of two energy levels, it is still very difficult to observe these patterns due to the poorer S/N ratio compared to the SET condition. Hence, SET is the preferred mode rather than the multi-electron tunneling for these devices.

2.2.2 Room temperature Classical SET

Although most characterization of the classical SET behaviors have been performed under low temperature (< 100 K), it is possible, to operate these devices at room temperature, given that the CCE is larger than the thermal energy

$$\Delta E_C = \frac{e^2}{C_{tot}} > K_B T = 0.26\ eV\ (T = 300\ K) \tag{2-19}$$

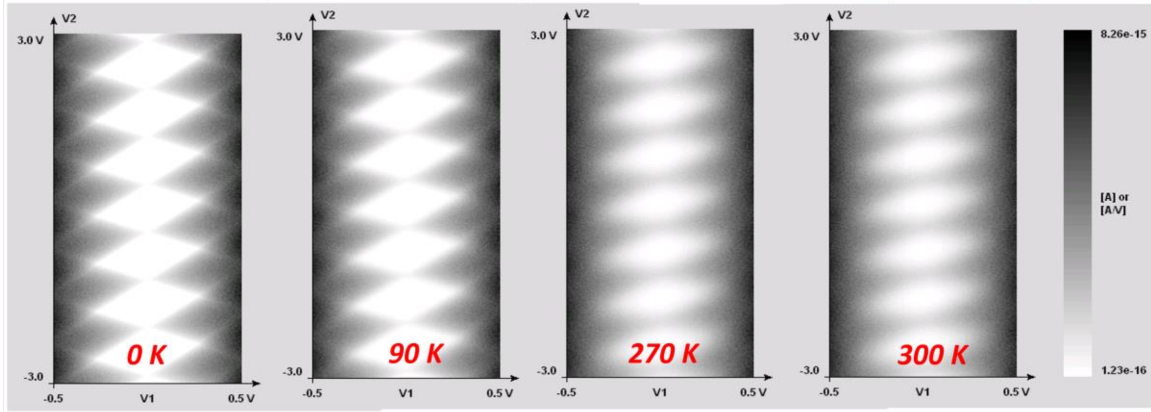


Figure 2-8 Effect of temperature to the stability plot of a SET with a 0.98 nm Au NP as an island

Figure 2-8 shows the effect of temperature to the stability plot of a SET with a 0.98 nm Au NP as an island. The stability plots were simulated by a Monte Carlo based simulator- - SIMON2 developed by C. Wasshuber [28]. The simulation parameters and characteristic values are summarized in **Table 2-1**.

Table 2-1 Simulation parameters and characteristic values of **Figure 2-8**.

Parameters	Units	Values
Gap size	nm	10
Au NP size	nm	0.9
Self-capacitance	C	9.7635E-20
Gate capacitance	C	1.9571E-19
Tunneling capacitance	C	2.0445E-19
Total capacitance	C	6.0440E-19
Gate/total capacitance ratio		0.3234
Temperature	K	0, 90, 270, 300
Tunneling resistance	Ohm	4.20E+13

Characteristic values	Units	Values

Periodicity:	eV	0.8196
Classic Coulomb charging energy	eV	0.2651

It is clear that a high enough thermal energy defined by K_BT can assist the electron tunneling even at the boundary condition of the Coulomb Blockade and smear out the diamond pattern of the Coulomb blockade/SET tunneling. For room temperature operation of the SET, it is, therefore, necessary to reduce the total capacitance coupled to the island, essentially, reducing the size of the island and reducing the dielectric constant. The effect of dielectrics with different dielectric constants in the island is embedded in that which was simulated and shown in **Figure 2-9**. The simulation conditions are summarized in **Table 2-2**. The effect of NP size will be discussed in more detail in the next section.

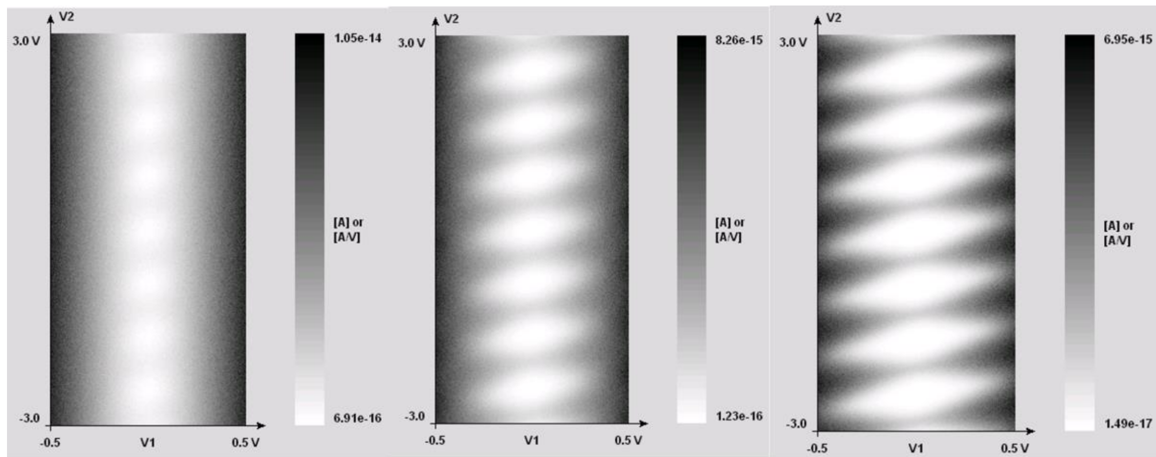


Figure 2-9 Comparison of simulated stability plot of 0.98 nm Au NP SET with (a) Al_2O_3 (b) SiO_2, and (c) air, at 300 K.

Table 2-2 Simulation parameters and characteristic values of **Figure 2-9**.

Parameters	Units	5nm AL2O3	5nm SiO2	no capping
Dielectric constants		9	3.9	1
Tunneling capacitance	C	4.7101E-19	2.0445E-19	1.0490E-19
Gate capacitance	C	1.9571E-19	1.9571E-19	1.9571E-19
Total capacitance	C	1.1410E-18	6.0440E-19	4.0590E-19

Periodicity:	eV	0.8196	0.8196	0.8196
Classic Coulomb charging energy	eV	0.1407	0.2651	0.3954

2.2.3 Quantum SET – Quantum Level Spacing

For the case when the quantum dot size is not negligible, such as the sub-2 nm size nanoparticle used in this study, the $\Delta E_N(N)$ cannot be ignored and can be generally estimated by a 2D growth model from the following:

$$\Delta E_N(N) = \left(\frac{1}{2\pi^2 N}\right)^{1/3} \frac{\hbar^2}{2m^*}\frac{\pi}{d^2} \tag{2-20}$$

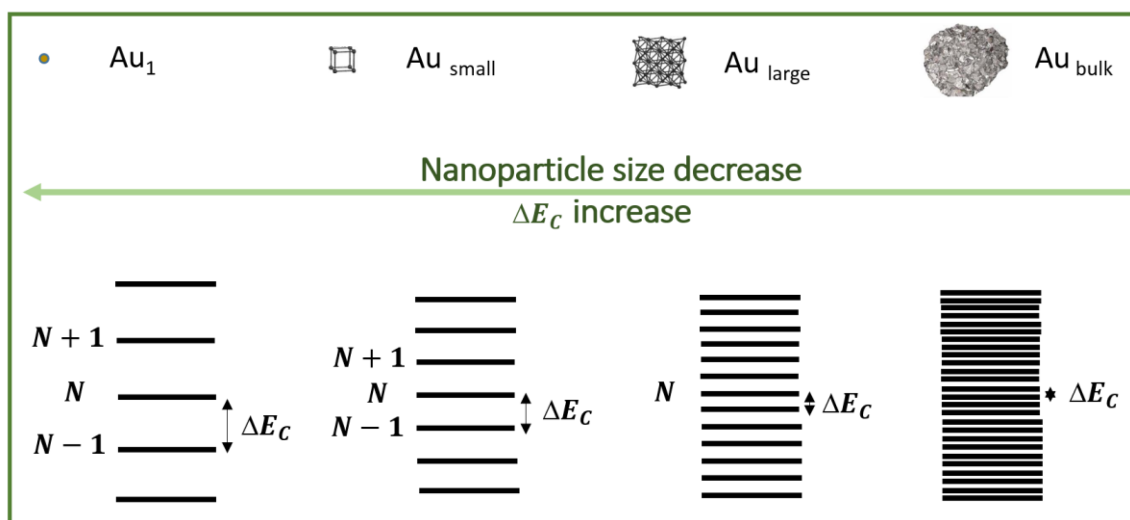


Figure 2-10 Schematics showing the size dependent quantum-level spacing.

As illustrated in **Figure 2-10**, a smaller NP size yields larger quantum level spacing that can be observed more easily during measurements. **Figure 2-11** shows the theoretical CCE, QCE, EAE and the estimated numbers of atoms vs. the NP diameter using the above model

at 300 K. For a room temperature operational SET, an NP size smaller than 4 nm may be required. Note that in an actual case, the exact electron shell structure and QCE of a nanoparticle can be difficult to determine by simply the disk or sphere assumption due to the non-negligible effect of many different cluster structures for clusters with the same number of atoms. In this case, the cluster structure has to be exact and first principle simulation can be used to estimate the exact shell structure.

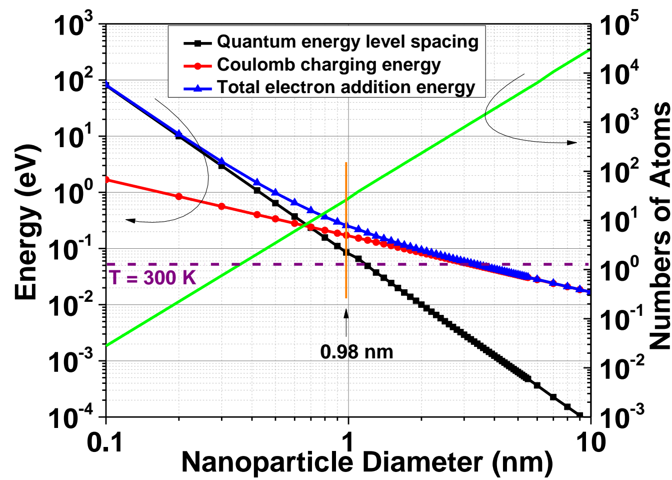


Figure 2-11 Theoretical Coulomb Charging Energy (●), the Quantum Confinement Energy level spacing (■), total electron addition energy (▲), and the estimated numbers of atoms vs. the NP diameter (/). The dotted line indicates the thermal energy at T = 300 K.

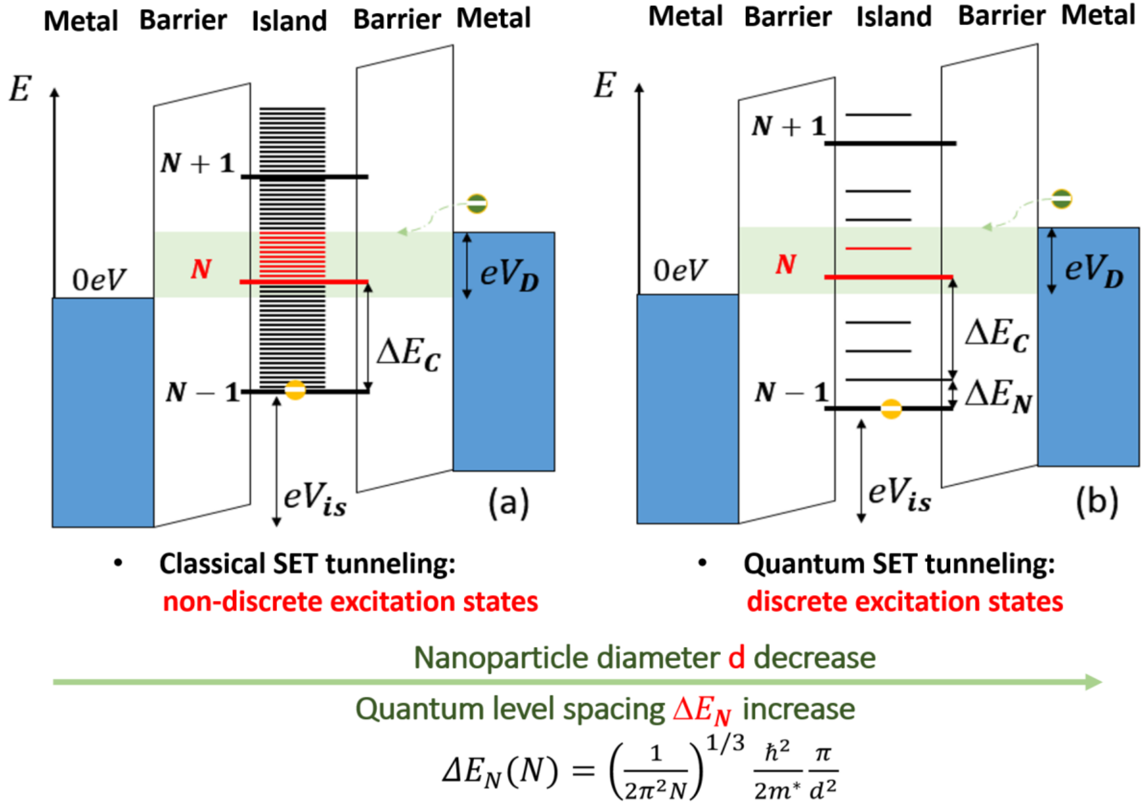


Figure 2-12 Comparison of energy band diagram of (a) Classical SET vs. (b) Quantum SET.

Figure 2-12 compares the energy band diagram of a classical SET vs. a Quantum SET. For the classical SET with a large size island, the quantum-level spacing is much smaller than the thermal energy which can be considered a continuous empty band or excitation states of the ground states (N-1, N, N+1) (not showed in **Figure 2-6** for simplification). Each excitation state and ground state within the tunneling window can be considered as one possible tunneling path to charge or discharge the island. Increasing the tunneling window linearly will result in a linear increase of the tunneling possibility of a charge; hence, a linear increase of tunneling current will occur in the single electron tunneling regime.

For the quantum SET, however, the quantum level spacing is comparable to the thermal

energy, resulting in discrete excitation states. Increasing the tunneling window in this case results in stepwise increase of the tunneling possibility, and hence, a stepwise increase of tunneling current, referred to as the quantum staircase effect. **Figure 2-13** compares the simulated stability plot of a classical SET (a) vs. a quantum SET (b) at 4.2K. Additional fine features (lines and smaller diamonds) due to the quantum staircase effect are observed in the single electron tunneling regime of a quantum SET compared to that of a classical SET. Note that the quantum level spacing is set as constant for **Figure 2-13** (b) which is an idealized case. In reality, these quantum level spacings are dependent on the electron shell structure of the cluster, and the energy level of each electron as illustrated in **Figure 2-13**(c). The staircase effect in the I-V characteristic is illustrated in **Figure 2-14**.

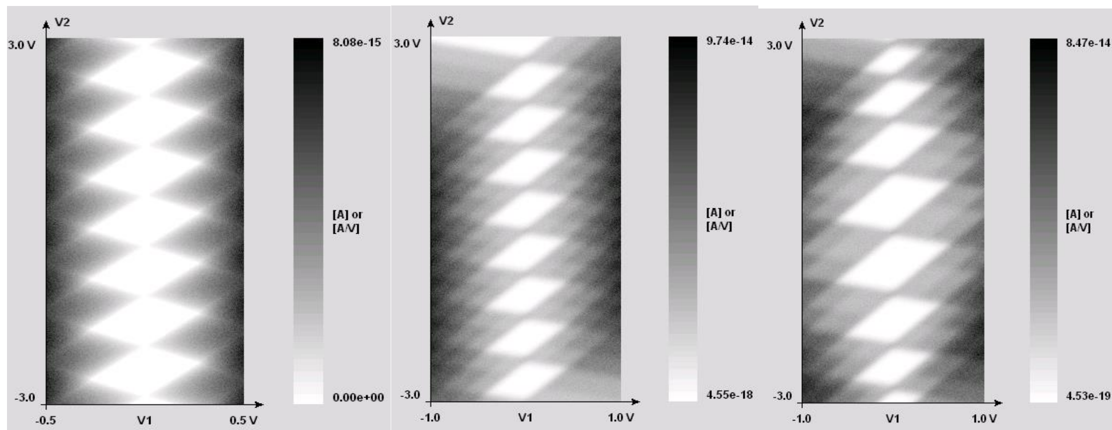


Figure 2-13 Comparison of simulated stability plot of a (a) classical SET vs. (b) quantum SET with equal QCE vs. (c) quantum SET with unequal QCE at 4.2 K.

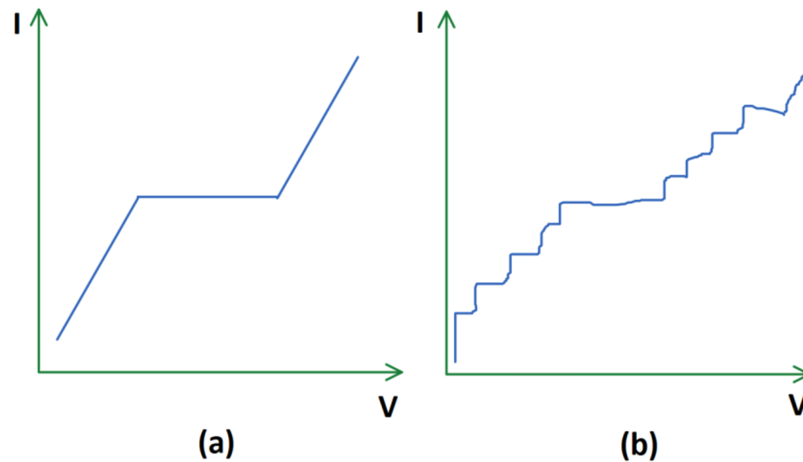


Figure 2-14 Comparison of I-V characteristics of a (a) classical SET vs. (b) quantum SET with quantum staircase effect.

2.3 Calculation of Related Capacitance Terms of Nanoparticles

2.3.1 Sphere to Plane Model

For a more precise estimation of the energy terms, all capacitances coupled to the NP are computed and summed up for the total capacitance. Due to the relatively small dimension of our Au/Pt NPs (0.5–2.5nm) compared to the size of coupling electrodes (> 30 nm) studied in this dissertation, the NP – electrode capacitance can be estimated by a sphere-plane capacitance model [29] as illustrated in **Figure 2-15**.

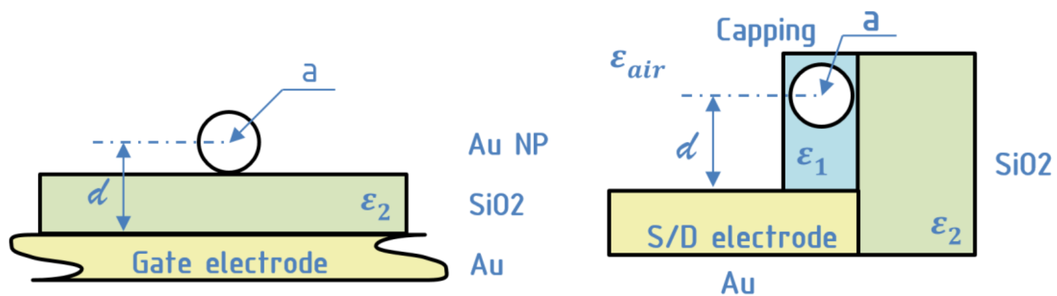


Figure 2-15 Schematics of a sphere-plane capacitor for (left) a gate electrode coupled to a single NP (right), which is an embedded NP coupled to a source or drain electrode.

This capacitance is given by:

$$C = 2\pi\epsilon\sqrt{d^2 - 4a^2}\sum_{j=0}^{\infty}(coth\left[\left(j + \frac{1}{2}\right)arcosh\left(\frac{d}{2a}\right)\right] - 1) \quad (2\text{-}21)$$

where a is the radius of the sphere, d is the distance between the sphere and the plane and ϵ is the permittivity of the dielectric material. For a three terminal SET with source, drain and gate electrode, the three capacitance terms can be represented as

$$C_S = 2\pi\epsilon_{pen}\sqrt{d^2 - 4a^2}\sum_{j=0}^{\infty}(coth\left[\left(j + \frac{1}{2}\right)arcosh\left(\frac{d}{2a}\right)\right] - 1) \quad (2\text{-}22)$$

$$C_D = 2\pi\epsilon_{pen}\sqrt{(g-d)^2 - 4a^2}\sum_{j=0}^{\infty}(coth\left[\left(j + \frac{1}{2}\right)arcosh\left(\frac{g-d}{2a}\right)\right] - 1) \quad (2\text{-}23)$$

$$C_G = 2\pi\epsilon_{SiO2}\sqrt{(t_G + a)^2 - 4a^2}\sum_{j=0}^{\infty}(coth\left[\left(j + \frac{1}{2}\right)arcosh\left(\frac{t_{gate}+a}{2a}\right)\right] - 1) \quad (2\text{-}24)$$

The dielectric constants of SiO_2 and pentacene that are studied in Chapter 2.3 are ~3.9 and 4, respectively. As seen in **Figure 2-16**, the bottom-gate-NP capacitance is a strong function of the NP size when the size is less than 1 nm. The smaller the spherical island, the smaller the electrode to island capacitances, and the larger the CCE. The capacitance is also a strong function of the dielectric thickness when the NP is larger than 1 nm and the dielectric layer thickness is less than 10 nm.

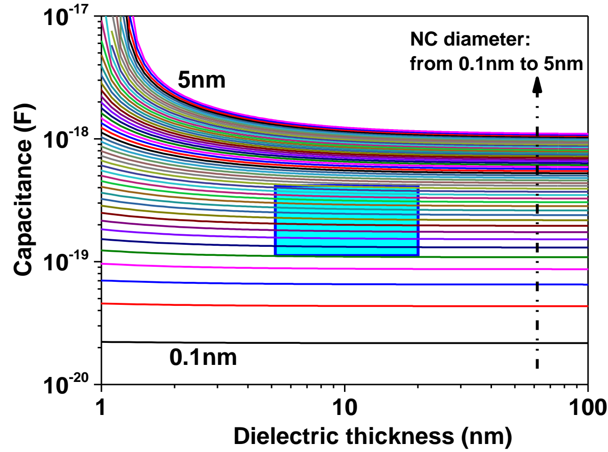


Figure 2-16 Calculated bottom-gate-NP capacitance vs. NP size and dielectric thickness (SiO_2 or pentacene). The cyan rectangle is the possible tunneling capacitance range of our SET studied in 2.3. In this region (0.5 nm < NP diameter < 1.5 nm, 5 nm < dielectric thickness < 20 nm), the tunneling capacitance is dependent on the NP size and somewhat independent of the dielectric thickness.

Chapter 3. Sub-1 nm Gold Nanoparticle-based Single-Electron Transistors at Room Temperature

This chapter discusses the size-dependent charging energy and quantum level spacing of sub-1 nm gold nanoparticles (Au NPs) and their application in room temperature (RT) operable single-electron transistors (SETs). This work is a critical foundation to help explain the effects of sub-nm metal NPs on the macroscopic device structures studied in

the next few chapters. The effects of embedded Au NPs demonstrated here include their utility as discrete charge storage nodes and the ability to control and observe charge storage and transfer down to the single electron levels at ambient temperature. SETs incorporating single ~1 nm Au NPs as charge transport islands are used to study the quantum Coulomb blockade and quantized energy level spacings at RT (300 K). Monodisperse ultra-small (0.86 ± 0.30 nm) Au NPs were deposited by the tilted-target sputtering (TTS) technique into 12 nm nanogaps fabricated by high-resolution e-beam lithography. Tunneling resistance was modulated to ~10^9 Ω by addition of a pentacene layer, allowing clear observation of quantum staircases and Coulomb oscillations with an on/off current modulation ratio of ~100 in room temperature current-voltage (I-V) measurements. Uneven addition energy was also observed and attributed to filling of the AuNC electron shell structure. The maximum electron addition energy and quantized energy level spacing were found to be 350 meV and 172 meV, respectively, which are significantly larger than the thermal energy at 300 K (25.9 meV).

3.1 Introduction

Single-electron transistor (SET) devices are promising candidates for low-power integrated circuits and ultra-high sensitivity detectors of single charges, photons, or molecules due to their operation at the single electron level and high susceptibility to charge interaction. Noble metal nanoparticles (MNPs) have proven advantageous over semiconductor clusters and organic molecules in SET applications due to their greater environmental stability, higher density of states, and mature fabrication techniques [5]–[7]. Theory predicts that MNP dimensions less than 1 nm are required for the quantum

confinement energy to surpass the RT thermal noise enough to probe single electron quantum excitation states [17]–[19]. Meanwhile, the relatively small electron charging energies of MNP-based SET devices have so far prevented clear room temperature (RT) observation of these Coulomb oscillations and quantum confinement states [17]–[19].

Fabrication and integration of monodisperse ~1 nm MNPs in a device configuration has been a major challenge in the progress of SET device technology. Recently, MNP SETs fabricated by thermal evaporation with island sizes mostly in the 5 – 10 nm range and some particles as small as 2 nm demonstrated Coulomb blockade and quantum confinement effects in measurements below 4.2 K [30], [31]. However, Pashkin *et al.* [31] reported an on/off current ratio of Coulomb oscillation of only 1.12 at 300 K, which was observed in only 1 of 56 SETs fabricated, and no quantum confinement states could be resolved. The thermal evaporation technique used for island fabrication in the aforementioned studies suffers from poor control of MNP size and size distribution, resulting in low yield of functional SET architectures and widely varying MNP size-dependent transistor properties [30], [31]. Utilizing the radially dispersed deposition flux in a tilted-target sputtering (TTS) technique, we have demonstrated monodisperse sub-2 nm Pt MNPs and their utility as discrete charge storage nodes [2], [5], [7], [20]. The TTS method demonstrates superior control on MNP size and size distribution (95% of metal islands fall in the range of 0.5–1.5 nm), which is an important step toward improving SET yield and consistency with sub-nm metal islands.

Optimizing the nanogap electrode spacing into which the MNP is deposited is critical to controlling SET tunneling resistance and capacitance. In general, confining charged electrons in the MNP "quantum dot" requires that the tunneling resistance (R_T)

satisfy the condition $R_T \geq \hbar/e^2 \approx 26$ kΩ [17]–[19]. Considering the practical application of direct tunneling through a nanogap, the tunneling current should be sufficiently strong enough to be detected by a commercial low current (fA level) measurement system, which would require $R_T < 10^{14}$ Ω. Assuming vacuum as the dielectric, the resultant required tunneling distance (i.e., distance between electrode and MNP) is less than 2 nm. Many techniques have been developed to fabricate sub-20 nm nanogaps for SET applications within the last decade, including break junction/electron migration [30], [32], [33], scanning tunneling microscopy (STM) [34], [35], and electron beam lithography (EBL) [36]. Break junctions must be fabricated individually, making the method incompatible with traditional large-scale complementary metal-oxide semiconductor (CMOS) fabrication techniques [30], [32], [33]. Liu *et al.* [36] presented e-beam overlap and overexposure EBL techniques to fabricate nanogaps with a 15% success rate for sub-5 nm gaps and with a100% success rate for sub-10 nm gaps. Further improvement in the yield for sub-5 nm gap devices is of crucial importance for sub-1 nm MNPs.

In this work, we have incorporated ~1 nm gold MNPs (Au NPs) into EBL-generated metal nanogaps. Au NPs were deposited using the TTS technique to achieve tunable size and narrow size distributions [2], [4], [5], [7], [13], [20]–[22], [37], [38]. A loosely packed layer of organic semiconductor pentacene was thermally deposited over the whole nanogap-Au NP assembly to reduce the tunneling resistance and obtain measurable current. Clear uneven quantum Coulomb oscillations and quantum level spacings were demonstrated at 300 K. We also report unique features in the charge transport characteristics that may indicate signatures of pentacene vibronic states. More than one-third (37%) of the devices showed SET behavior with consistent characteristic single

electron behavior over the 5-day measurement time frame. To the best of our knowledge, this is the first RT demonstration of MNP quantum-level spacings in a CMOS-compatible SET.

3.2 Experiment

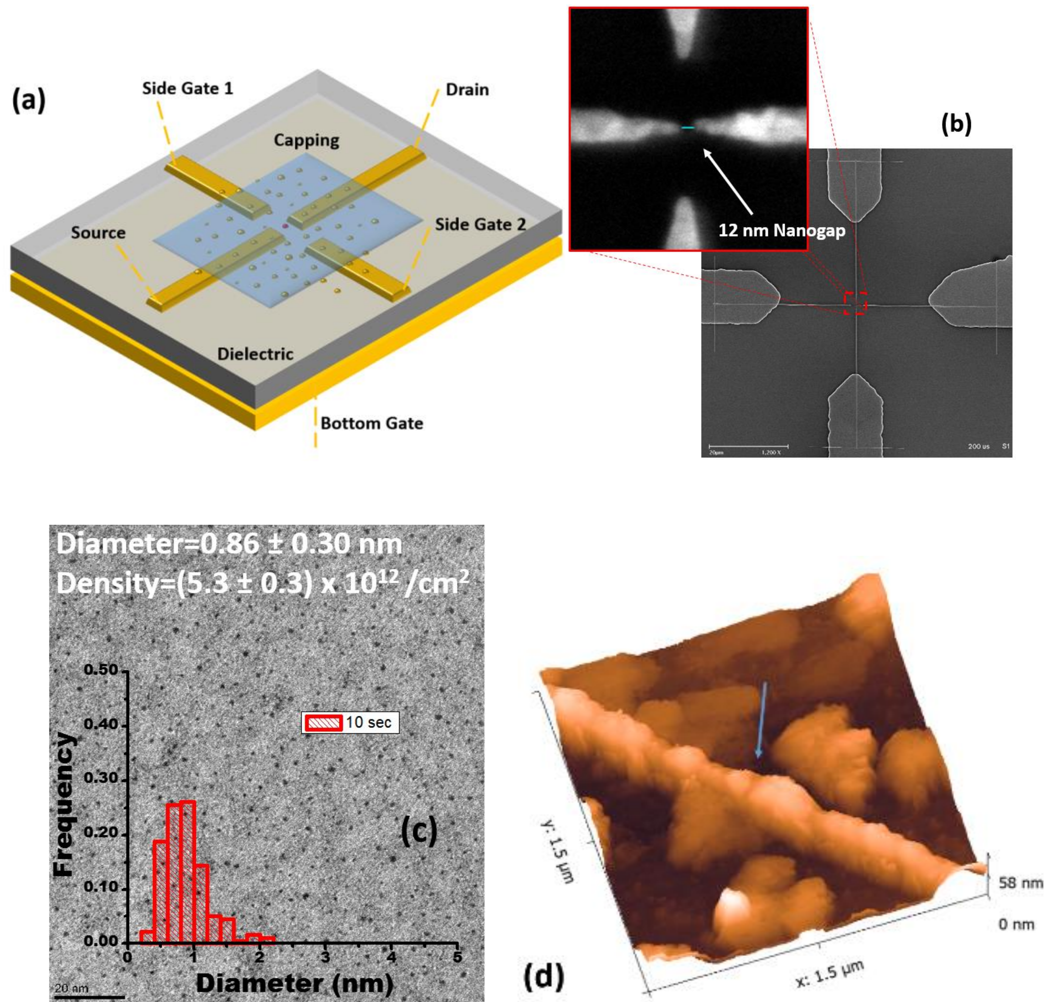


Figure 3-1 (a) Schematic of SET device structure; (b) SEM image of the e-beam patterned nanoelectrodes (scale bar 20 μm); inset: nanoelectrode structure with 12 nm gap. The two side gates were not used in this study; (c) Transmission electron microscopy image of 0.86 nm Au NPs with the inset showing the Au NP size distribution. The scale bar is 20 nm; (d) AFM images of Au nanoelectrodes after pentacene deposition.

The MNP SET device schematic is illustrated in **Figure 3-1** (a). The SET substrate

consisted of heavily doped p-type silicon with Cr-Au bottom gate contacts and a 200 nm thermally grown silicon dioxide (SiO_2) blocking layer. Nanogaps were patterned in a 100 nm poly(methyl methacrylate) (PMMA) resist layer using an Elionix ELS-7000 EBL system operated at 100 kV accelerating voltage and 200 pA beam current. The triangular geometries forming the gap regions were patterned using half the dose of that used for the remainder of the electrodes to enhance the precision and reproducibility of the gaps. The resist was developed in a 1:3 ratio of methyl isobutyl ketone to isopropyl alcohol (1:3 MIBK:IPA) at 0 °C followed by the deposition of 2 nm Cr as an adhesion layer for a 30 nm Au layer [39], [40]. The electrodes were then connected to larger contact pads defined by photolithography to enable electrical measurements. The pads were defined by aligning a second photo mask with the EBL-patterned nanogap electrodes followed by resist development and deposition of 100 nm Au film. The final Au nanogaps varied in length from 8–21 nm with an average gap dimension of 13 nm (**Figure 3-1** (b)). Au NPs with 0.86 ± 0.30 nm diameter (range: 0.5–2.2 nm) and $(5.3 \pm 0.3) \times 10^{12}$ cm^{-2} particle number density were then synthesized by TTS technique using 10 s sputtering time, 18 W power, 38.8° target angle, and 4 m Torr working pressure (**Figure 3-1** (c)) [4], [5], [7], [20], [22], [37], [38], [41]. Pentacene was finally thermally deposited as a capping layer to reduce tunneling resistance over the whole Au nanogap-Au NP assembly (**Figure 3-1** (d)). Pentacene grain sizes obtained through AFM measurements ranged from 200–300 nm with height ranging from 30–80 nm.

Atomic force microscope (AFM, Bruker) was used to image the nanoelectrodes before and after pentacene deposition. Imaging was carried out using an SNL-10-B probe (2 nm nominal radius). Electrical characterizations were carried out in a triaxial guarded

and electromagnetic shielded probe station (Signatone WL-210E) in a dark, nitrogen environment at room temperature (~300 K). The current-voltage (I-V) measurements were taken by a Keithley 4200-SCS semiconductor characterization system with pulse generators and pre-amplifiers. During the measurement, the source was fixed at 0 V while the drain and gate electrodes were biased at different values.

3.3 Discussion

3.3.1 Au NP number estimation

Addressing Au NP formation within the nanogap, the Au NP size distribution and number density would be severely affected in this case of depositing Au within the nanogap. Here, it can be safely assumed the nanogaps have sharp tips, and characteristic SET electronic signatures are determined by Au NPs falling in the direct line of contact between the two tips (12 nm gap length). Thus, the nanogap region has an effective width of 2 nm. Furthermore, after considering the Au NP size distribution/number density and a deposition surface with feature sizes less than 2 nm in height, the number of Au NPs lying within the 12 nm gap can be calculated to be two or three. However, after considering the pronounced aspect ratio of the nanogap (30 nm Au sidewall height to 12 nm gap length), the number of Au atoms/clusters actually reaching the 12 nm SiO_2 surface is severely reduced. The acceptance angle of the cone was determined based on the positioning of the target with respect to the substrate holder [22]. This reduction in number of Au NPs reaching the SiO_2 surface is because a majority of the thermalized Au atoms/clusters outside the acceptance cone would more likely deposit on the Au sidewalls due to better matching between the surface energy of the Au atoms/clusters and polycrystalline Au

sidewall surface, compared to a lower energy SiO_2 surface. Thus, within the acceptance cone, the volume of the thermalized Au atoms clusters is reduced to just 12% of the expected value on a relatively featureless surface. This leads to the conclusion that there might be one or zero Au NPs within the 12 nm nanogap when deposited using the TTS configuration being employed here. This matches well with the observation that, although experimental features were prominently seen in the SET characteristics at room temperature for some devices (with one Au NP in the gap), some devices were found without any experimental SET indicative features, which is further indicative of zero Au NPs existing within the nanogap.

3.3.2 Role of pentacene layer in electronic properties

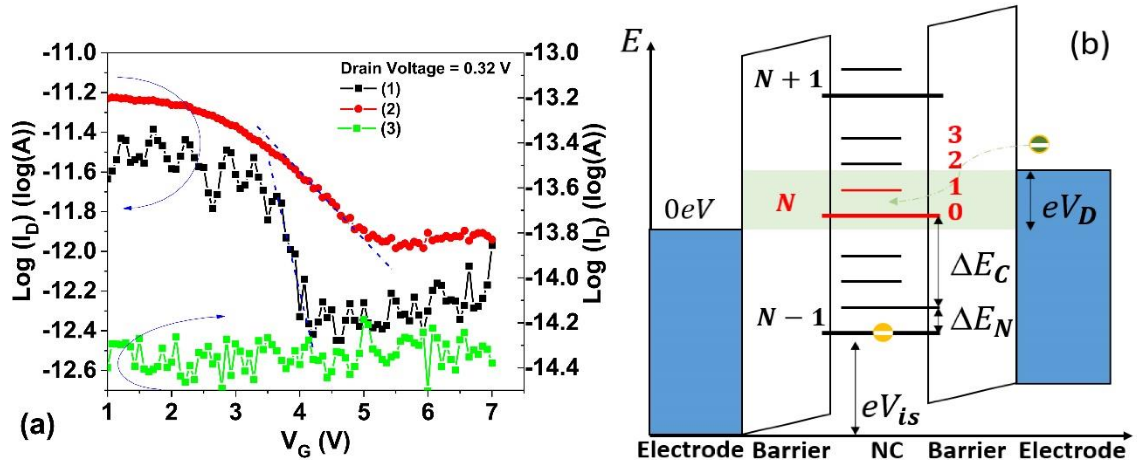


Figure 3-2 (**a**) Drain current vs. gate voltage characteristics of the devices with: (1) 0.86 nm Au NP and pentacene capping layer, (2) pentacene capping layer only, and (3) 0.86 nm Au NP only; (**b**) Energy band diagram for the biased SET.

Figure 3-2 (a) shows the drain current-gate voltage (I-V) characteristics of three device configurations: (1) device with both 0.86 nm Au NP and pentacene capping layer; (2) device with pentacene layer only; and (3) device with 0.86 nm Au NP only. These I-V

curves were measured from different devices out of necessity as the order of Au and pentacene depositions required to fabricate the complete Au NP/pentacene device made it practically impossible to measure the same nanogap in all device configurations. The potential leakage current due to the pentacene conduction channel in devices (1) and (2) is dictated by variations in nanogap size (8–22 nm), pentacene coverage, and molecular arrangement within the nanogaps. The baseline current observed in device (2) is higher than device (1) for this reason. However, the actual contribution of pentacene to the leakage current in SET device (1) is difficult to separate from the contribution of Au NP. The leakage current due to the presence of pentacene may partially offset the measured transport current of the Au NP SET.

Drain current (I_D) was suppressed for devices (1) and (2) when biasing with gate voltage $V_G \gtrsim 5$ V, indicating depletion of the hole-conducting pentacene. Devices operating in this region did not show clear SET peaks due to current suppression by the large tunneling resistance. Device (3) shows no leakage current and remains at ground level ~10^{-14} A, resulting from the impenetrable dielectric barrier created by the lack of pentacene in the nanogap. Meanwhile, clear oscillation peaks were observed from device (1) when biasing with $V_G < 4$ V. This operation clearly demonstrates V_G modulation of the tunneling resistance by changing the carrier density in the pentacene layer, which effectively reduces the tunneling barrier between the Au nanogap electrode and the Au NPs. We attribute these oscillation peaks to the Coulomb oscillation effect resulting from the presence of the Au NPs rather than any effects of pentacene. The charging energy for 200–300 nm pentacene grains is only a few meV [17], which is close to the thermal energy, whereas the charging energy is expected to be much higher for 1 nm Au NPs.

Charge mobility across the nanogap can elucidate further information about the morphology of the pentacene layer. The low mobility (~ 4.23×10^{-5} $cm^2V^{-1}s^{-1}$) observed across the nanogap in our devices suggests a limited number of pentacene molecules in the nanogap. High mobility (~0.1–1 $cm^2V^{-1}s^{-1}$) would suggest highly ordered molecules with significant π-π overlap as seen with pentacene film growth on self-assemble monolayers (SAMs) of octadecyltrichlorosilane (ODTS) [42]. Mobility within the nanogap could be restricted by poor molecular alignment, insufficient fill factor, or a combination of both. Furthermore, any pentacene molecule in the vicinity of an Au NP is likely to attach itself to the Au NP due to the heightened Au NP surface energy resulting from its higher surface area to volume ratio (Supplementary Information S4). One pentacene molecule (1.54 nm length) is likely to cover a 1 nm Au NP due to the tendency of pentacene molecules to lie flat on Au surfaces [43].

The bulk and interface trap states of the pentacene layer will influence the tunneling properties of the SET. Depending on the actual trap site location, these bulk and interface trap states might serve as gated background charges of the SET, shifting the stability plot [17]–[19], or providing additional trap tunneling paths within the dielectric when the device is operating in the sub-threshold region (~3–5 V). When the SET is operated in the negative V_G range, most of the shallow trap states can be filled by holes, minimizing the charge de-trapping effect and facilitating the observation of SET behavior. This is important because the transported charges can be trapped and untrapped by the neighboring trap sites, limiting conduction when operating near the threshold V_G of pentacene (Supplementary Information S4).

3.3.3 Electron addition energy and quantum level spacing

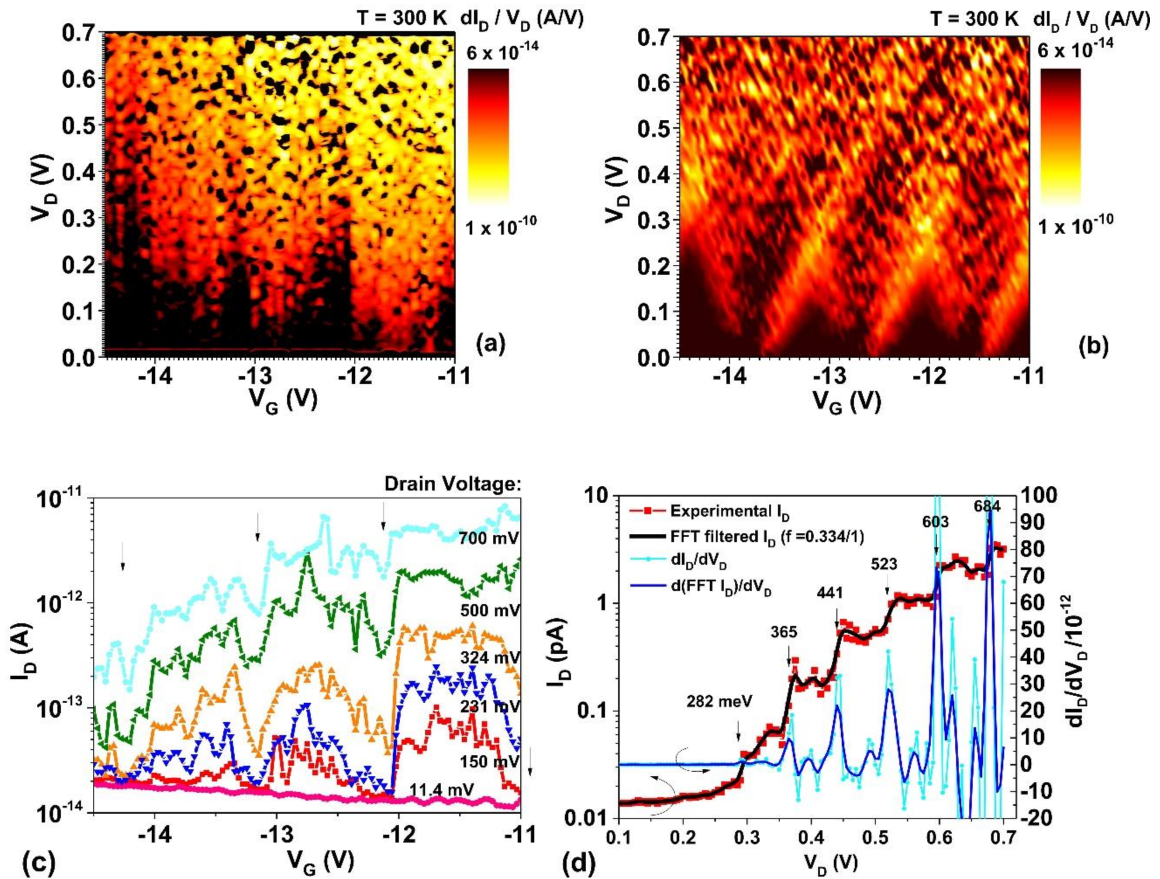


Figure 3-3 (a) Experimental and (b) simulated 2-D stability plot of dI_D/dV_D vs. V_D and V_G for V_G from -14.5 V to -11 V at 300 K; (c) I_D vs. V_G plot with different V_D showing V_G modulation of Coulomb oscillation at 300 K, arrows indicate Coulomb blockade valleys; and (d) I_D vs. V_D plot with V_G = 12.3 V showing quantum confinement staircases.

The current through the Au NP is a strong function of the Au NP energy band structure and system band alignment (**Figure 3-2** (b)), the nature of which can be revealed, in turn, by the current transport characteristics. **Figure 3-3** (a) is a two-dimensional (2-D) stability plot of our 1 nm Au NP SET at 300 K, plotting the first derivative of drain current (dI_D/dV_D) as a function of both V_D and V_G, and **Figure 3-3** (c) contains individual drain current vs. gate voltage (I_D vs. V_G) characteristics extracted from that plot. The

current/conductance stability plot is a powerful tool for studying the addition energy and energy spectrum of a SET [31], [44], [45]. Four periodic dark and bright shaded regions can clearly be seen at V_G = -11, -12.2, -13.3, and -14.5 V, respectively, when sweeping the gate bias from -11 V to -14.5 V with an average periodicity of ~1.1 V. The bright and dark regions correspond to low and high conductance, respectively, and the current on/off ratio between these Coulomb peaks and valleys was found to be ~100, two orders of magnitude higher than Pashkin *et al*. [31]. These bounded regions are referred to as Coulomb diamonds and correspond to the observed conduction peaks and valleys with low drain bias (**Figure 3-3** (c)). The low conductance regions indicate energetically stable regions with different electron numbers on the Au NP. The electron addition energy for each electron number is taken from the height of the Coulomb diamond on the V_D axis or, alternatively, can be calculated from the conductance peak spacing. The electron addition energies for the four stable regions are approximately 0.35, 0.21, 0.28, and 0.18 eV, respectively.

In contrast to the classical Coulomb blockade model [17]–[19], the data here show uneven electron addition energy values. Some electron numbers have particularly large associated electron addition energy, indicating that the corresponding electron number is relatively stable. A similar effect was observed at 50 mK by Tarucha *et al*., where an unusually large addition energy was observed for a symmetric 2-D harmonic potential when the cluster electron number coincided with 2, 6, 12, ...[45]. This is reminiscent of the closed electron shells in atoms, where the three-dimensional spherically symmetric potential gives rise to the shell structure (1s, 2s, 2p, 3s, 3p, ...) and the ionization energy has a large maximum for atomic numbers 2, 10, 18, etc. Small clusters behave like artificial atoms when their size is on the order of the electron wavelength and the continuous energy

bands become quantized shell structures, which has been successfully described by the jellium model [44], [45]. Adding one electron requires the Coulomb energy E_C plus the difference $\Delta E_N(N)$ between two quantum levels. If a second electron is added to the same quantum level (i.e., the same shell in an atom), $\Delta E_N(N)$ vanishes and only the Coulomb energy E_C is needed.

Figure 3-2 (b) shows the energy band diagram of a single Au NP at certain bias conditions before an electron tunnels from the drain electrode to the Nth energy state. Here, N-1, N, and N+1 represent electron addition energy levels with spacing of either E_C or $E_C + \Delta E_N(N)$, where E_C is the Coulomb charging energy given by $E_C = q^2/2\, C_{tot}$ with C_{tot} equal to the total Au NP capacitance. N is the number of charges on the Au NP, and ΔE_N is the quantum level spacing [17]. The numbers 0, 1, 2, and 3 represent the Nth ground level and 1st, 2nd and 3rd excitation states of the Nth ground level with quantum confinement level spacing, respectively. In this configuration, the N-1th ground level, which is occupied by an electron, sits below the tunneling window (set by eV_D) and does not take part in the charge transport. The Nth empty ground level in the tunneling window is a much more energetically favorable position for an electron to tunnel from the Fermi level of the drain electrode. The gate bias coupled to the Au NP with the gate oxide capacitor can move the energy spectrum of the Au NP up or down relative to the neighboring band alignments, where the bias-dependent energy alignment with each ground level in the tunneling window results in a detectable change in the tunneling current. In the absence of a ground level within the tunneling window (e.g., V_G = -12.3 V and V_D = 0.231 V in **Figure 3-3** (c)), the electron tunneling through the Au NP is energetically forbidden, resulting in the well-known Coulomb blockade region or the presence of current oscillation valleys in the I_D vs.

V_G plot.

In addition to the Nth ground level, the quantum confinement excitation states of the ground level within the tunneling window act as alternative tunneling paths (**Figure 3-2** (b)). Consider again the bias condition V_G = -12.3 V and V_D = 0.3 V with the Nth ground level within the tunneling window. By increasing the drain bias, the number of available excitation states of the Nth level can be modulated, resulting in a stepwise change in the tunneling rate, which can be detected as current steps or conductance peaks in the drain current vs. drain voltage (I_D vs. V_D) characteristics (**Figure 3-3** (d)). To further analyze these features, we took the derivative of the I-V curve in **Figure 3-3** (d) and applied a Fast Fourier Transform (FFT) digital low-pass filter to remove noise with equivalent energy less than 25.9 meV (details on noise reduction in Supplementary Information S2). Six current staircases and differential conductance peaks were clearly observed at V_D = 282, 365, 441, 523, 603, and 684 meV, with the first peak at V_D = 282 meV corresponds to the total electron charging energy. The other five peaks with step sizes of 83, 76, 82, 80, and 81 meV are due to the stepwise increase of excitation states available on the island as tunneling paths. A similar Coulomb staircase with step size of $\Delta V_D = e/\max(C_D, C_S)$ can be observed in classical SETs with asymmetric tunneling junctions where C_D and C_S are junction capacitances and $\max(C_D, C_S)$ represents the larger of the two values. However, the classical Coulomb staircase is inadequate to describe our data as $\max(C_D, C_S)$ because a 79 meV step size was found to be ~2.04 aF, which corresponds to a 6.5 nm Au NP with a 29.2 meV Coulomb charging energy. This directly contradicts the Au NP size distribution obtained by TEM (**Figure 3-1** (c)) and the observed total electron charging energy. The staircase phenomenon observed in **Figure 3-3** (d) is, thus, due to alignment of quantum

confinement energy level spacing. Stepwise increase in tunneling rate can result from the change in available excitation states for electron tunneling from one electrode to the Au NP and from the Au NP to the other electrode. Thus, these measured step sizes may not exactly represent the electron shell structure energy spectrum.

The uneven addition energy for different electron numbers can be attributed to the filling of Au NP electron shells, which would be considered direct evidence of quantum Coulomb blockade and quantum confinement states. However, the accuracy of the charging energy and confinement energy may be reduced due to the signal-to-noise ratio at RT. Due to the relatively weak capacitive coupling of the gate electrode to the Au NP, a larger range of gate bias is necessary to reveal the full energy spectrum. The energy levels involved in current transport can also be indicated by lines parallel to the edge of the Coulomb blockade region in the 2-D stability plot, such as those observed by Bolotin *et al.* and Pashkin *et al*. [30], [31]. These lines are not readily apparent from **Figure 3-3** (a), which could be due to the relatively high thermal energy obscuring energy level features comparable to 25.9 meV.

In the case of a single Au NP SET, the mutual capacitance of the Au NP with the source, drain, and gate electrodes in the device were estimated to be 4.09×10^{-20} F, 6.80×10^{-19} F, and 2.13×10^{-19} F, respectively, based on analysis of the edge slope of the Coulomb blockade regions in **Figure 3-3** (a). These values, however, might not be highly accurate due to the blurring of the slope of the diamond edge by the thermal noise at RT. The coupled Au NP size can be estimated by the mutual capacitance obtained above using the sphere-plate model (Supplementary Information S5), which is estimated to be ~ 0.98 – 1 nm, within the range of the Au NP diameters measured by HR-TEM (0.86 ±

0.30 nm). The Coulomb charging energy is then calculated to be 196 meV, close to the smallest addition energy in **Figure 3-3** (a) (180 meV at $V_G = -11$ V). Considering the electron addition energies of all four electron numbers (350, 210, 282, and 180 meV), the level spacings are approximately 172, 30, 104, and 0 meV, respectively. The Au NP diameter, capacitance, and energy terms obtained from the above calculation were used to simulate 2-D stability curves using the SIMON simulator based on the Monte Carlo method [17]. The equivalent circuit used in this study is shown in Supplementary Figure S14. The single Au NP condition was assumed in this case. The source-to-Au NP and drain-to-Au NP tunneling resistances used were 2.79 and 3.12 GΩ, respectively. A ±10% error within the randomized capacitances, resistances, and charges were applied for each tunneling event. The number of tunneling events per bias condition per tunnel junction was 300. The energy level spacings used were 172, 30, 104, and 0 meV. The simulated 2-D differential conductance stability plot at 300 K is given in **Figure 3-3** (b). These results match qualitatively with the experimental data in **Figure 3-3** (a). Although some of the SET signatures are obscured due to thermal noise, appropriate noise reduction allows clear observation of the blockade regions and some of the unique SET features could still be observed.

Matching the oscillation model to the experimental data becomes more difficult when trying to consider more than one Au NP coupling between the nanogaps, as the Au NP diameters, Au NP-to-electrode coupling strength, and inter-Au NP coupling strength will have significant effects on the oscillation pattern of the system [17]–[19], [46], [47]. In particular, the electron wave functions of two strongly coupled Au NPs overlap, causing them to act as a single, large Au NP with reduced Coulomb charging energy and Coulomb

oscillation periodicity. For two weakly coupled Au NPs, additional oscillation peaks can be observed at the degeneracy point when biasing with low drain voltage and the Coulomb charging energy can be highly relative to the case of an SET with only one NP [48].

3.4 Future Work

Future study includes low temperature measurement and incorporation of ultra-dense multi-NP-layers as tunneling matrix in a SET device to achieve high signal-to-noise ratios at room temperature.

Chapter 4. Barrier Modification of Metal-contact on Silicon by Sub-2 nm Platinum Nanoparticle (Pt NPs)

This chapter discusses the application of sub-2 nm platinum nanoparticles (Pt NPs) to address a longstanding issue in the fabrication of semiconductor devices—Fermi level pinning of semiconductor at the metal-semiconductor interface. The control of the metal-semiconductor contact barrier through the introduction of sub-2 nm Pt NPs deposited by tilted target sputtering (TTS) is studied. We show the size-dependent properties of Pt NPs and their role in Fermi level depinning at the metal-semiconductor interface with a 0.98 nm Al_2O_3 and/or 1.6 nm SiO_2 dielectric layer. It was found that the areal density of Pt NPs played a significant role in barrier modification; hence, modified samples with embedded 0.74 nm Pt NPs with areal density of 1.1×10^{13} cm^{-2} have shown ~10^4 times higher current densities compared to a control device [Titanium (Ti) - thin oxide - (Silicon) Si contact] and a device with embedded Pt NPs at ~1.6 × lower areal density. We further demonstrate that the contact can be modulated to be either a Schottky or Ohmic contact by simply varying Pt NP size and areal density.

4.1 Introduction

One of the most interesting properties of the metal-semiconductor (MS) junction is the rectifying barrier for electrical conduction or the Schottky barrier. According to the Schottky-Mott Relationship [49], the energy mismatch between the majority carrier band edge and the Fermi level of the metal determines the barrier height. But the theory received very little corroboration from experimental results. Regardless of the metal work function,

a barrier tends to pin the Fermi level of the semiconductor to a particular value. The term "Fermi level pinning" was introduced to describe this insensitivity of the Schottky barrier height (SBH) to the metal work function. Many groups have tried many different approaches to explain the mechanism of Fermi level pinning. Some of the approaches are: the defect model, the metal induced gap states (MIGS) or interface trap states (ITS), chemical bonding model, or inhomogeneity of Schottky barriers [49]–[53]. As a result of Fermi level pinning, the contribution of contact resistance due to non-ideal Ohmic contact, affects the device characteristics drastically in the nanometer regime [54]. Among various methods to overcome the aforementioned issue, doping the Si heavily (in order to reduce the effective barrier width) is the most common one. However, the doping methods used (e.g. ion implantation, diffusion) do not have a precise control of depth and anisotropy, and, hence, are not applied in case of fine doping of organic semiconductor or 2D material based devices. Numerous studies have also demonstrated reduced metal-semiconductor (MS) contact resistance, using thin insulating tunnel barriers with fixed charges [23], [24]. Incorporation of a thin dielectric layer between the MS contact, reduces the SBH by 'depinning' the Fermi level, but the effective barrier width for tunneling also increases due to the contribution from the dielectric layer. Thus, the oxide thickness must be optimized to achieve a favorable trade-off between the SBH and effective tunneling barrier width. However, the optimal insulating layer thickness (e.g., ~1 nm for Al_2O_3) is difficult to fabricate and thicker insulator layers increase the contact resistance by reducing the tunneling probability. Dielectric layers below this thickness (~1 nm) are generally unreliable due to surface discontinuities. The concept of barrier modification using two metals with different work functions was introduced in the 1990s when Tung [55] reported

the first analytic solution of electron transport in inhomogeneous Schottky barrier heights (ISBH) with the prediction of the potential pinch-off effect. Narayanan [56] introduced the notion of enhanced tunneling at triple interface (ETTI), which was later adopted, theoretically and experimentally, by many researchers to explain the barrier modification due to metal nanoparticles (MNPs) at the MS contact [57]–[62]. Based on the ISBH and ETTI model, it can be predicted that by reducing the size increasing the density of MNPs, and increasing the work function difference between metal electrodes and MNPs the barrier modulation effect can be enhanced. However, MNPs used in previous studies are of relatively larger size, and also the techniques used to deposit had limited control over the size and areal density of the MNPs [60], [61], [63], [64]. The effect on barrier modification of sub-nm diameter MNPs and the combined effect of both thin dielectric and MNPs has not been explored extensively. In this study, we control the metal-semiconductor junction barrier by incorporating sub-2 nm platinum nanoparticles (Pt NPs) deposited by tilted target sputtering (TTS) [65], which has been previously demonstrated for application of non-volatile memory, vapor molecule detection, and so on [7], [12], [13], [15], [16], [21], [66]. Pt was chosen to maximize the work function difference between the metal electrode and the NPs. We report the properties of the size-dependent Pt NPs and their role in Fermi level depinning at the metal-semiconductor interface with 0.98 nm Al_2O_3 and/or 1.6 nm SiO_2 dielectric layer. As the sub-2 nm MNPs are embedded into dielectric layers between the MS contact, the electron addition energy of the MNP matrix, which comprises the Coulomb charging and quantum confinement energy, should also be taken into consideration. Our initial study reveals that samples with 0.74 nm Pt NPs modified samples show >100-fold higher current density compared to a Ti-thin oxide-p Si contact

(control). We further show that the contact can be modulated to be either Schottky or Ohmic using the same metal, by varying only Pt NP size and its areal density.

4.2 Experiment

Metalorganic contaminants were removed from low-doped p-type Si (p-Si) using a modified Shiraki cleaning process [67]. The chemically grown SiO_2 (~1.6 nm) was preserved for some samples by drying off the samples with N_2 after immersing them in $HCl:H_2O:H_2O_2$. TTS was used to deposit Pt NPs onto the substrate with the deposition time and target angle tuned to obtain different Pt NP sizes and areal densities. Deposition times of 10, 20, and 45 s at 23° incidence angle corresponded to Pt NP sizes of 0.74, 1.1, and 1.45 nm, respectively. With larger target angle (38°) and 20 s deposition time, Pt NP size was reduced to 0.72 nm, and their areal density was increased. Details on this methodology and results of others can be found in [7], [13], [21], [65]. **Figure 4-1** shows a TEM image of 1.11 nm TTS-deposited Pt NPs with the insets showing a size distribution analysis. The Pt NP conditions used in this study are summarized in **Table 4-1**. A 0.98 nm Al_2O_3 layer was then deposited by Atomic Layer Deposition (ALD) [13], [65]. 80 nm of Ti and/or Au metal contact was then electron beam deposited atop the samples. The backside of the substrate was then coated with large area Cr/Au to ensure an Ohmic back contact. 2 nm of Cr was deposited prior to the 80 nm Au to improve the adhesion. Samples were then H_2 annealed at 250 °C for 1 hr to improve the oxide quality. The devices were characterized in a Janis ST-500 probe station system which has the capability of achieving vacuum (down to ~ 5 m Torr) and can be cooled down to 80 K. Current-voltage (I-V) and capacitance-voltage (C-V) characteristics were measured by a Keithley 4200 SCS system. About 7-10

devices for each condition were measured and plotted with error bars where applicable.

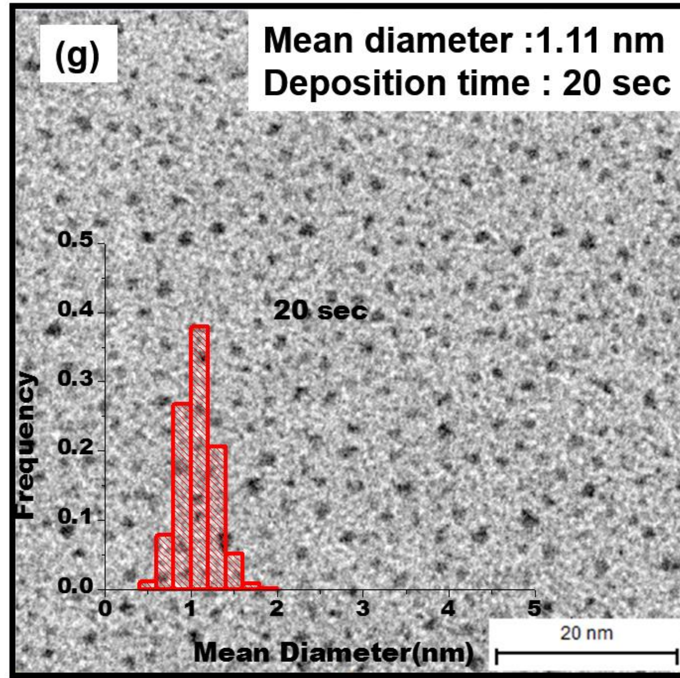


Figure 4-1 TEM image of 1.11 nm TTS-deposited Pt NPs.

Table 4-1 Summary of the Pt NP conditions used in this study

Conditions	**Deposition time** sec	**Target Angle** deg (°)	**NP diameter** nm	**Areal Density** 10^{12} /cm^2
Control	/	/	/	/
1	20	38	0.72	11
2	10	23	0.74	7
3	20	23	1.11	5.4
4	45	23	1.45	7.7

4.3 Discussion

According to thermal-emission (TE) model [49], a y Schottky barrier can be

analyzed through J-V characteristics in the forward bias direction. For moderately doped semiconductors, the J-V characteristics in the forward direction is given by Eq. (4-1).

$$J = \frac{I}{A} = J_s[exp\left(\frac{qV}{\eta kT}\right) - 1]\,,\ J_s = A^{**}T^2 exp[-\frac{q}{kT}(\emptyset_{B0} - \Delta\emptyset)] \qquad (4\text{-}1)$$

$$\eta = \frac{q}{kT}\frac{\partial V}{\partial(lnJ)}\,, \emptyset_{B0} = \frac{kT}{q}ln(\frac{A^{**}T^2}{J_s}) \qquad (4\text{-}2)$$

J_s is the saturation current density. A is the device area, A^{**} is the effective Richardson constant, which was reported to be ~30 for p-Si [49]; T is the temperature in Kelvin; q is the electron charge 1.6×10^{-19} C; k is Boltzmann's constant 1.38×10^{-23} J/K; $\Delta\Phi$ is the image-force lowering, and V is the forward bias voltage. η and Φ_{BO} are the ideality factor and barrier height which can be calculated by Eq. (4-2). The $\partial V/\partial(lnJ)$ term in the ideality factor equation is the reciprocal of the slope in the linear fitting of the J-V characteristic and J_s is the intersection of the linear fit of the J-V characteristic at the y-axis. In other words, after achieving the intercept and the slope by linear fitting the J-V characteristic, Φ_{BO} and η can be calculated. When η=1, the carrier transmission is dominated by TE. Meanwhile, when $\eta > 1$, the main transmission mechanism involves field-emission (FE) or thermal-field-emission (TFE).

4.3.1 Role of thin dielectric layers (SiO_2 and Al_2O_3) in barrier height reduction

The SBH is usually defined as the difference between the conduction band minimum (CBM) of the semiconductor at the interface to the Fermi level of the system. For a "pure" MS Schottky barrier (e.g., excluding the effect of image force lowering, and

interface impurity), if $V_P(z)$ represents the CBM potential reference to the Fermi level, with z being the depth into the MS interface and W being the width of the depletion region, then for $0 < z < W$,

$$V_P(z) = V_{bb}\left(1 - \frac{z}{W}\right) + V_n \quad (4\text{-}3)$$

where $V_{bb} = \phi_{B0} - V_n - V_a - V_o$ is the total band bending at a given applied bias V_a for a SBH of ϕ_{B0}, V_o the SBH lowering due to a thin dielectric layer between the MS interface, and V_n is the difference of the CBM and the Fermi level of bulk semiconductor determined by the doping concentration. The maximum value of $V_P(z)$ yields the SBH (max [$V_P(z)$]). When inserting a dielectric layer, the SBH is lowered due to Fermi level depinning of the oxide; at the same time, the effective barrier width for tunneling is increased when taking into consideration the contribution of the oxide barrier itself. Insertion of a thin dielectric layer lowered the SBH by 'depinning' the Fermi level, but on the other hand also increased the effective barrier width for tunneling. Thus, for the purpose of reducing contact resistance, the oxide thickness must be optimized to obtain a favorable trade-off between the barrier height and effective barrier width. Previous studies have reported that the optimized thickness for Al_2O_3 to reduce the specific contact resistance effectively, is ~1 nm [23], [24]. The Ti-p-Si system is expected to form a Schottky contact with an experimental SBH of ~0.5 eV. A thin dielectric was inserted between Ti and Si to specifically 'depin' the Fermi level formed due to metal induced gap states or interface defect states. Devices with 0.98 nm atomic layer deposited (ALD) Al_2O_3 were used as control and compared with devices comprised of 0.98 nm Al_2O_3 and/or 1.6 nm chemically grown SiO_2. Devices with 0.98 nm Al_2O_3 showed the highest current density at both positive and negative bias (**Figure 4-2** (a)). The lower current injection of other conditions

were due to the increase of tunneling resistance with thicker oxide, which offsets the benefit of SBH reduction. By using Eq. (4-1) and (4-2), the ideality factor of ~1.3–1.6 was obtained, which meant that FE or TFE should to be taken into consideration for the current transport mechanism.

For further analysis of the current transport behavior, the activation energy measurements (J-V-T) were performed. According to [49],

$$ln\left(\frac{I_F}{T^2}\right) = ln(AA^{**}) - \frac{q(\Phi_{B0}-V_F)}{kT} \qquad (4\text{-}4)$$

where $q(\Phi_{B0} - V_F)$ is considered to be the activation energy. Over a limited range of temperatures (typically around room temperature), the value of A^{**} and Φ_{B0} are essentially temperature independent. Thus for a fixed forward bias V_F, the slope of a plot of $In(I_F/T^2)$ versus 1/T yields the barrier height Φ_{B0}, and the ordinate intercept at $1/T = 0$ yields the product of the electrically active area A and the effective Richardson constant A^{**}. The slopes of the curves in the Richardson plots (**Figure 4-2** (b)) were used to calculate the barrier heights (**Figure 4-2** (c)). It was determined that devices with thicker oxides have lower barrier heights (~ 0.18 eV and ~ 0.12 eV), which indicates better Fermi level depinning.

The energy band diagrams for different structures demonstrating this behavior were plotted in **Figure 4-2** (d). The next two sections present a study of the modulation of the contact by embedding different sizes and densities of TTS deposited Pt NPs in these devices.

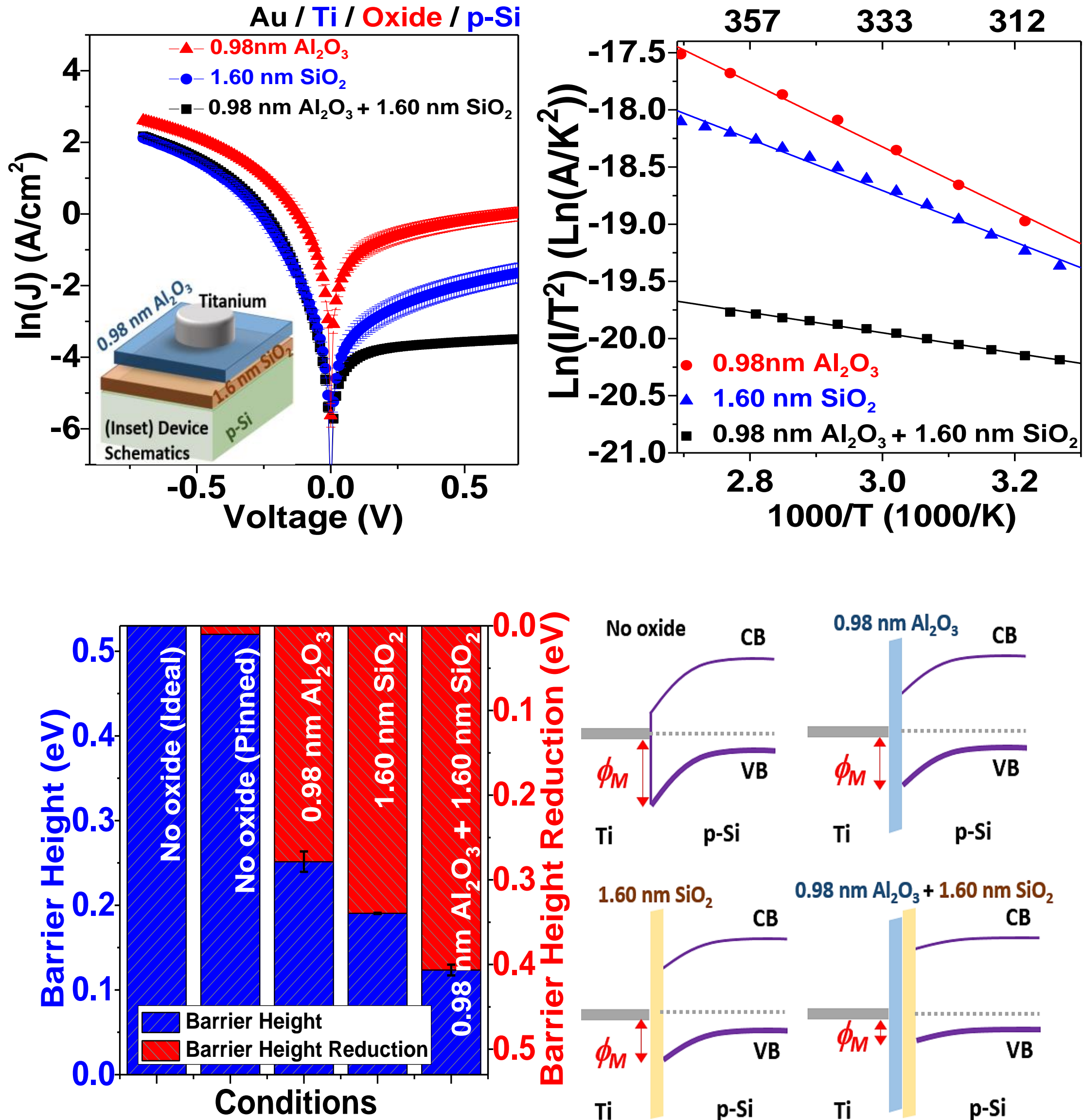


Figure 4-2 Comparison of Ti-p Si contact with different thicknesses and types of dielectrics (a) Ln (J)-V characteristics. Inset: Schematics of device structures; (b) the Richardson plots; (c) the barrier heights; (d) schematics of energy band diagram showing the barrier reduction of Ti-p Si contact by insertion of thin dielectrics.

4.3.2 Role of different stacking configuration & metal

Figure 4-3 (a)-(f) shows the J-V characteristics of a device with and without Pt NPs in combination with different thin dielectric stacking and different macroscopic metal electrodes.

Figure 4-3 (a) compares the ln (J)-V characteristics of the Ti/Al_2O_3/p-Si contact with and without 0.74 nm Pt NPs embedded. Significant enhancement in the current density was observed for both forward and reverse bias for the samples with embedded nanoparticles. In fact, a three order magnitude improvement occurred in the reverse current density. The ln (J)-ln (|V|) curve in **Figure 4-3** (d) further confirmed the good linearity and complete symmetric current conduction for both forward and reverse regions, which caused an ideal Ohmic contact to form with this configuration.

Comparing the J-V characteristics displayed in **Figure 4-3** (a, d) and (b, e) for devices with Ti electrodes, we also found that samples with Pt NPs closer to the p-Si surface have an overall higher current density, especially in a reverse bias region. This can be explained by the partial potential drop within the thin dielectric and the lowering of dipole induced electric field to the semiconductor, weakening the SBH modulation due to the Pt NPs.

By comparing J-V characteristics displayed in **Figure 4-3** (b, e) and (c, f) it was found that the introduction of Pt NPs on top of the thin Al_2O_3 layer converted both Ti-Al_2O_3-p Si contact and Au-Al_2O_3-p Si contact from Schottky barrier contact in to quasi-Ohmic contact with ~10^4 improvement in reverse current density for both cases. In particular, Au-Al_2O_3-Pt NP- p Si contact is showing linear and symmetric Ohmic behavior. With either the top or bottom of the Pt NP in contact with the electrode or Si, the Coulomb blockade effect is negligible in these cases since Pt NPs are not isolated by tunneling junctions. A metal-metal dipole enhanced electric field will be the main cause of the barrier modification and current modulation (**Figure 4-3** (g)). When a combination of different metal patches is brought into contact with a semiconductor in a macroscopic electrode,

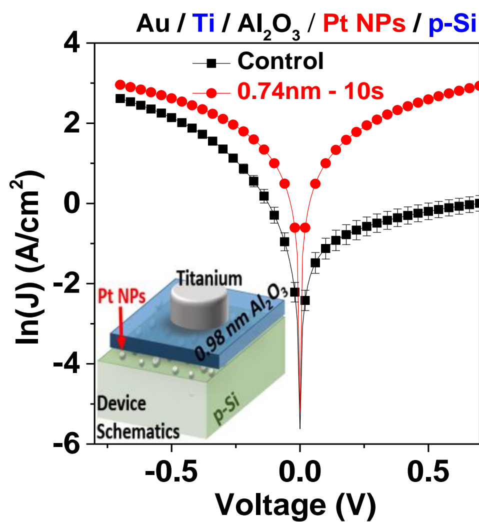
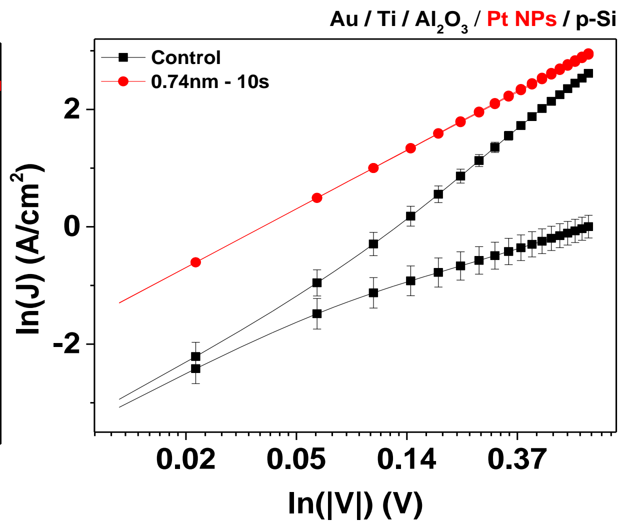
with electrode contact area and semiconductor depletion width much larger than the dimension of those patches, the macroscopic current transport cannot be modeled by a parallel combination of these different SBH MS contacts. Instead, the electric field induced by the interface dipole between metal patches with different work functions tends to modulate the local SB and thus the current transport, which is especially the case when MNPs are incorporated into the MS contact. The schematics of an energy band diagram in **Figure 4-3** (h)–(i) illustrate this effective reduction of SBH and depletion width of a macroscopic MS contact with embedded MNPs. According to Tung's [55] ISBH model, by introducing the potential due to a planar circular metal-metal interface dipole layer with a moment per area of $2\epsilon_s\delta(x,y)$ and radius of R into a MS contact with mean SBH of ϕ_{B0}, Eq. (4-3) can be modified as follows to represent the $V_P(z)$ at the center of the circular patch along the z axis:

$$V_P(0,0,z) = V_{bb}\left(1-\frac{z}{W}\right) + V_n - \Delta\left(1-\frac{z}{(z^2+R^2)^{1/2}}\right) \tag{4-5}$$

with $\Delta = \phi_{B0} - \phi_{B,patch}$ being the SBH difference between the two metals before contact. By differentiating Eq. (4-5) with respect to z, the electric field is given by

$$E(0,0,z) = V_{bb}\left(\frac{2}{W}-\frac{2z}{W^2}\right) - \Delta\left(\frac{1}{(z^2+R^2)^{1/2}}-\frac{z^2}{(z^2+R^2)^{3/2}}\right) \tag{4-6}$$

Eq. (4-6) is qualitatively in good agreement with the result of **Figure 4-3** (a) as for Pt with much higher work function than Ti and hence lower SBH of Pt-Al_2O_3-p Si than Pt-Al_2O_3-p Si yielding large SBH difference of Δ. The Pt NPs with R as small as 0.36 nm are expected to induce a large negative electric field near the MS interface, resulting in reduction of local SBH and hence facilitate the current injection at these hot spots.


Au / Ti / Al$_2$O$_3$ / Pt NPs / p-Si
Control
0.74nm - 10s
Titanium
Pt NPs
0.98 nm Al$_2$O$_3$
Device
Schematics
p-Si
ln(J) (A/cm^2)
Voltage (V)

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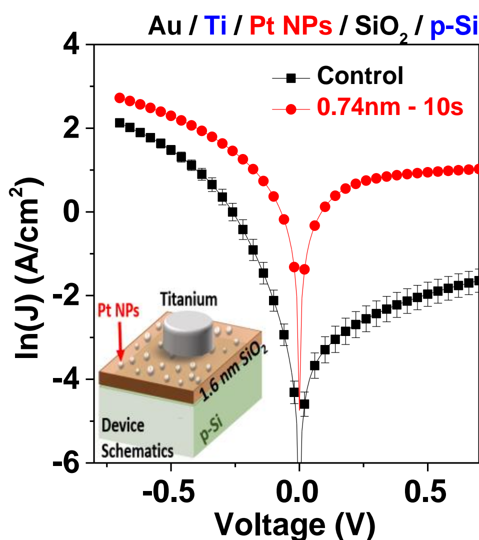
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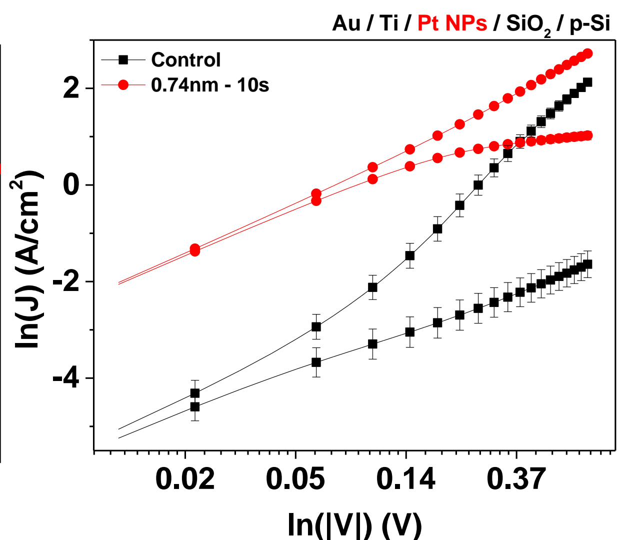
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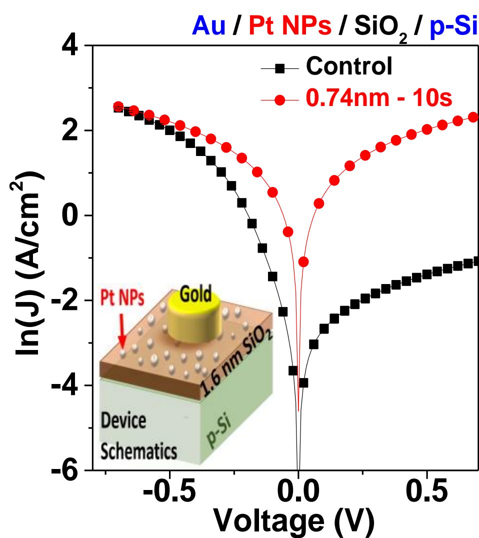
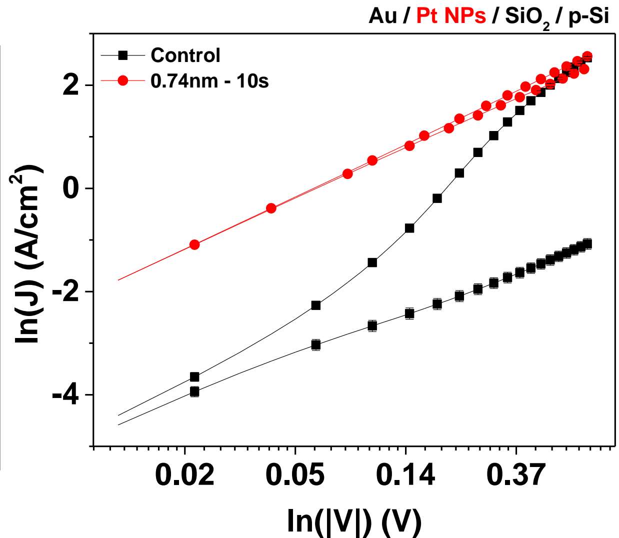

Au / Pt NPs / SiO$_2$ / p-Si
Control
0.74nm - 10s
Gold
Pt NPs
1.6 nm SiO$_2$
Device
Schematics
p-Si
ln(J) (A/cm^2)
Voltage (V)

Au / Pt NPs / SiO$_2$ / p-Si
Control
0.74nm - 10s
ln(J) (A/cm^2)
ln(|V|) (V)

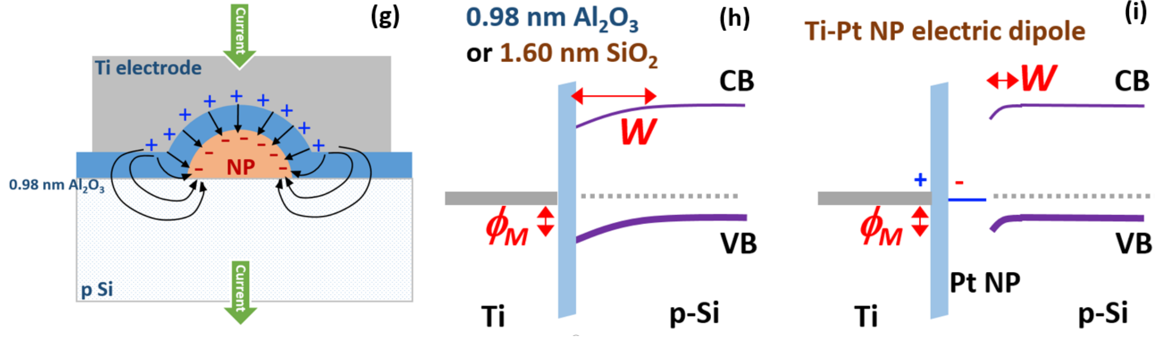


Figure 4-3 Comparison of ln(J)-V and ln(J)-ln(V) characteristics for (a, b) Ti-Al_2O_3-p Si contact with and without 0.74 nm Pt NPs between the Al_2O_3 and Si surface; (c, d) Ti-SiO_2-p Si contact with and without 0.74 nm Pt NPs between the Ti electrode and SiO2 surface; (e, f) Au-SiO_2-p Si contact with and without 0.74 nm Pt NPs between the Au electrode and SiO2 surface; Inset: Schematics of the device structures. (g) Schematics showing the dipole formation between Ti electrode and Pt NP. (h, i) Schematics of energy band diagram showing the reduction of depletion width with the presence of Pt NPs.

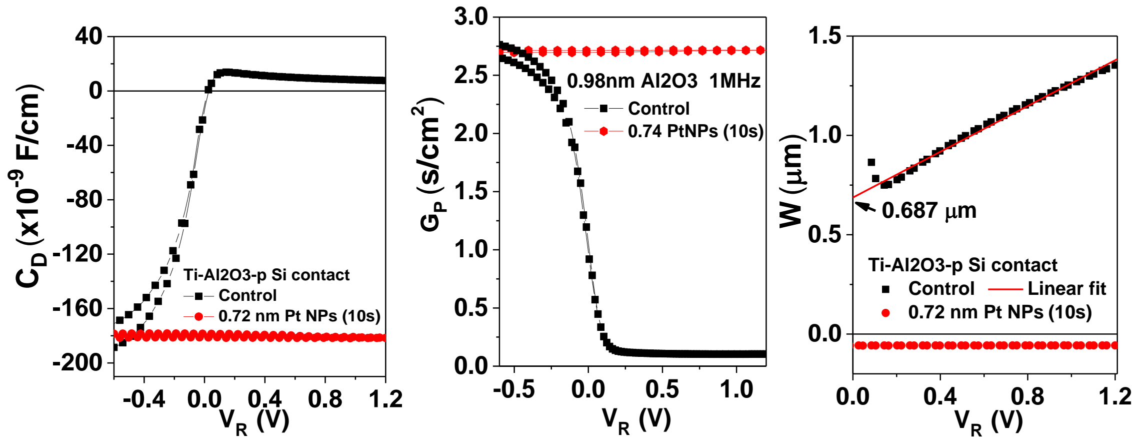


Figure 4-4 Comparison of (a) C_D-V, (b) G_P-V, and (c) depletion width Ti-Al_2O_3-p Si contact with and without 0.74 nm Pt NPs (10s).

Capacitance-voltage (CV) measurements were also performed to study the barrier modification. The depletion width of the semiconductor under reverse bias can be estimated by,

$$W_D = \frac{\varepsilon_S}{C_D} = \sqrt{\frac{2\varepsilon_S}{qN_D}(\psi_{bi} - V_R - \frac{kT}{q})} \tag{4-7}$$

where ε_s is the permittivity of the semiconductor, N_D is the doping concentration, ψ_{bi} is the CBM band bending at zero bias, and V_R is the reverse bias voltage. For Ti - 0.98 nm Al_2O_3 - p Si sample, the depletion width at zero bias is calculated to be ~685 nm. For Ti - 0.98 nm Al_2O_3 - 0.74 nm Pt NPs - p Si sample (**Figure 4-4** (a)). C_D is a negative number, which is an indication of high parallel conductivity (**Figure 4-4** (b)) due to the current injection hotspot of the Pt NPs, which dominated the overall reactance (represented as negative capacitance), resulting in large error in the measured C_D; hence, the depletion region formed at the p Si band edge cannot be determined (**Figure 4-4** (c)). Further circuit analysis correcting the measured C_D is required to make CV analysis useful for our Pt NPs embedded samples with high conductivity.

4.3.3 Role of Pt NPs embedded between SiO_2 and Al_2O_3 thin oxide in barrier modification

The device consisting of embedded NPs between two dielectric layers [Ti/0.98 nm Al_2O_3/Pt NPs/1.6 nm SiO_2/p-Si] was studied in this section. By controlling the deposition time and target angle, different sizes and densities of Pt NPs were deposited (**Table 4-1**).

There are mainly two MNP-related mechanisms responsible for the current modulation in **Figure 4-5** (a) and (b): (1) Enhanced electric field due to Ti-Al_2O_3-Pt NP interface dipole, resulting in the SBH modulation (**Figure 4-5** (d, f, and g)) and the potential pinch-off effect and (2) NP size dependent Coulomb charging energy (CCE) and quantum confinement energy (QCE) [12].

The CCE can be estimated by the equivalent circuit given in **Figure 4-5** (e),

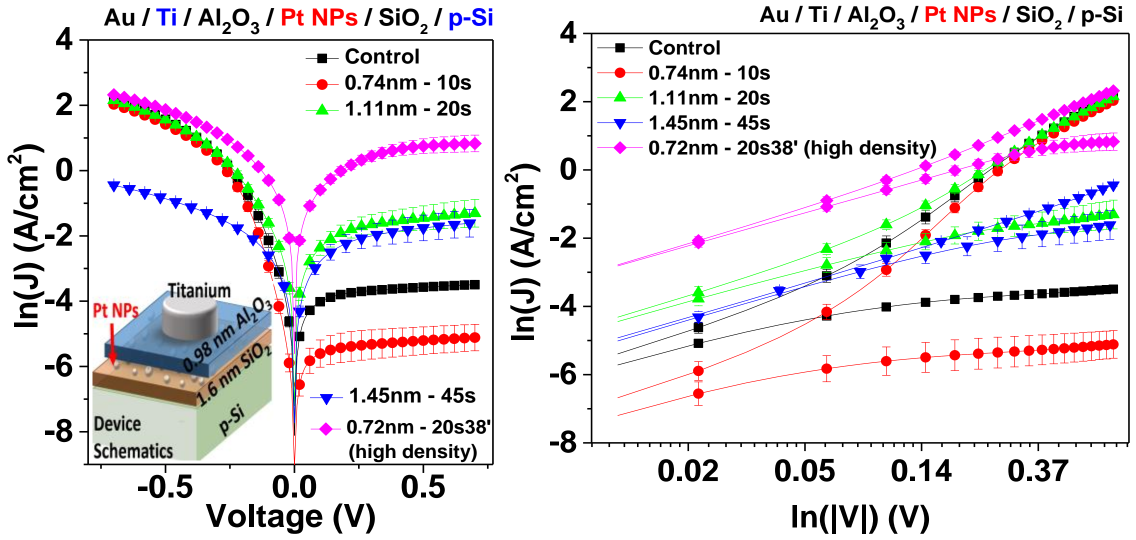
$$CCE = q^2/(C_1 + C_2) \tag{4-8}$$

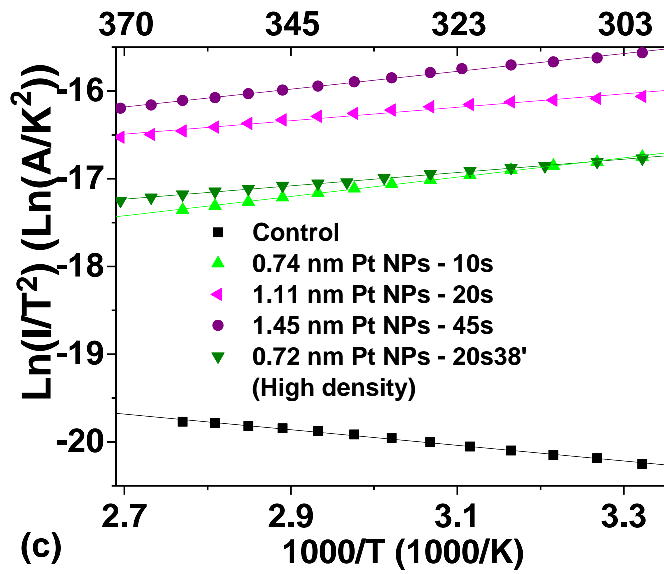
where C_1 and C_2 are the junction capacitance of the Ti/0.98 nm Al_2O_3/Pt NPs and Pt NPs/1.6 nm SiO_2/p-Si, respectively. Note that due to the asymmetric capacitance and resistance of the two tunneling junctions, the voltage required for charging the Pt NPs will also be polarity dependent, with

$$V_1 = \frac{CCE}{q} * \frac{C_1+C_2}{C_2} \text{ and } V_2 = \frac{CCE}{q} * \frac{C_1+C_2}{C_1} \quad (4\text{-}9)$$

For the 0.74 nm (10 s) sample with low areal density (7 x 10^{12} /cm^2), the high charging energy was dominant over other mechanisms hence the current was the lowest. Increasing the density to 1.1 x 10^{13} /cm^2 (0.72 nm – 20 s 38°) resulted in reduction of charging energy due to smaller inter-NP distance and stronger inter-NP coupling, considering the whole Pt NP layer as the tunneling matrix [12]. With the large NP density, the effect of electric field enhancement of Ti-Al_2O_3-Pt NP interface dipole became dominant and yielded the highest current.

For similar NP density, larger size NP samples have a much lower charging energy, which facilitated the charge tunneling, resulting in a higher current injection level. The SBH modulation due to the Ti-Al_2O_3-Pt NP interface dipole induced electric field will be dominant. Note that the radius of the Pt NPs plays an important role in the SBH modulation similar to the case described in Eq. (4-6). Using the Richardson plot provided in the ISBH model, however, usually causes an underestimation compared to experimental results for ultra-small MNP cases due to the fact that it ignores the curvature of the interface dipole layer and treats it as a planar structure. For a more accurate determination, the enhanced tunneling at the metal-metal interface at the edge of the patches also need to be taken into consideration [56].





(c)

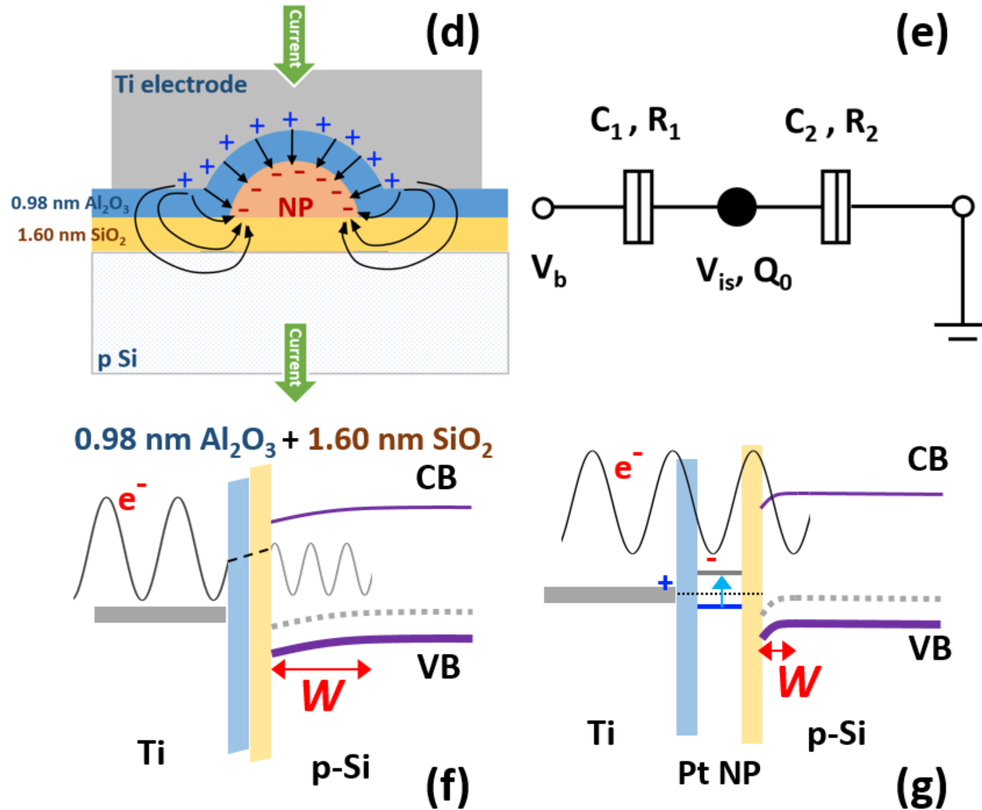


Figure 4-5 Comparison of Ti-p Si contact with different sizes of Pt NPs sandwiched between the 0.98 nm Al_2O_3 and 1.6 nm SiO_2 (a) Ln(J)-V characteristics. Inset: Schematics of device structures; (b) Ln(J)–Ln(|V|) characteristics; (c) the Richardson plots; (d) schematics showing the dipole formation between Ti electrode and Pt NP; (e) Equivalent circuit of the device showing the Coulomb blockade effect; (f, g) schematics of energy band diagram showing the electron wave penetration and the reduction in depletion width with the presence of Pt NPs.

4.4 Future Work

Future work includes the capacitance-voltage (CV) characterization on these M-S contacts and the simulation on the dipole enhance electric field using COMSOL and other tools to further reveal the Pt NP size dependent behavior on the barrier modification.

Chapter 5. Effect of Sub-1 nm Pt NPs on Doping/Strain of Single-Layer-Graphene Field-Effect Transistor

This chapter discusses the doping and strain effects induced by ultrafine sputtered Pt nanoparticles (Pt NPs) of different sizes on a single layer graphene through conduction channel modification of graphene-based FETs and subsequent Raman characterization. For sub-nm (0.5 nm) diameter Pt NPs, a substantial Dirac point shift was observed in the I-V characteristics, suggestive of *n*-type doping of the large area single layer graphene through the process of charge transfer and chemical interaction. Conversely, for larger (1.1 nm) Pt NPs, a minimal Dirac point shift is observed, indicating a lack of charge transfer induced doping effect. The representative Raman signatures corroborate with the electrical characterization results, which shows that while charge transfer dominates Raman peak shifts for the 0.5 nm Pt NP decorated graphene, strain effect dominates in case of the larger 1.1 nm Pt NP.

5.1 Introduction

Graphene's promising electronic properties make graphene-based transistors attractive platforms for future devices. It is well known that graphene exhibits ballistic transport at the submicron scale and can be doped heavily using a multitude of techniques without significant loss of mobility [25]. There are two primary methodologies utilized for doping graphene: first, by replacing carbon atoms with either donor or acceptor dopant atoms destructively [68], [69]; second, by charge transfer or localized electric field induced doping with the presence of either physically or chemically adsorbed dopant molecules on

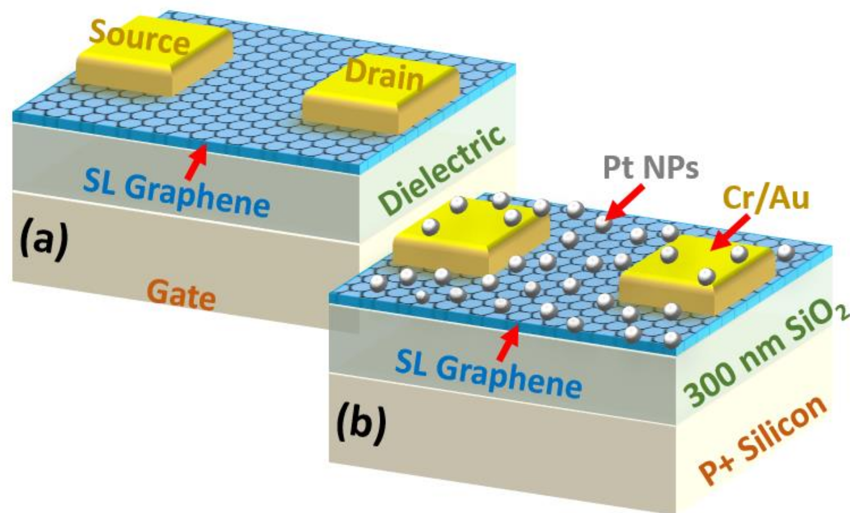
the surface of graphene [70], [71]. Recently, researchers have reported a two-step process as an efficient way to dope graphene with single atoms [68]. This idea involves creating vacancies by high-energy atom and ion bombardment and subsequently filling these vacancies with desired less-energetic dopant atoms. The resulting doping density, while not very high, can theoretically be controlled accurately and result in predictable device characteristics. It must be noted that implementation of these destructive methods towards doping graphene may not be preferable in situations where no significant change in the intrinsic properties of graphene is desired. Meanwhile, choosing the same metal as the contact electrode for doping is sometimes preferable over using different metal configurations to minimize potential contamination issues. Wu et al. previously studied the role of thermally evaporated Au NPs and thin film in doping graphene [70]. Here, the authors report both *n* and *p* type doping characteristics based on the discreteness of the Au nanoparticles (NPs) and thin film with different deposition times, with ~20 nm size NPs leading to *n*-type doping and Au film leading to *p*-type doping in graphene. This experimental observation was supported by DFT calculations where the authors report that graphene has stronger chemical interactions with the Au NPs (leading to a smaller separation between the Au NPs and graphene) compared to the thin film, which eventually leads the two systems to have opposite doping types. It should be noted that the Au NPs were deposited using a thermal evaporator in this case and are larger than 10 nm with broad size variation and low areal density, making precise experimental control of the doping concentration difficult. The experimental study of NP size dependent doping on graphene for ultrafine metal NPs (generated during the initial atom to cluster growth phases) is still unexplored and can shed further light on fundamental metal NP/graphene interactions.

While metal deposition on graphene can end up doping the underlying graphene, significant differences in graphene and deposited metal lattice parameters can also induce strain on the SL graphene layer [72]. It is well known that introduced strain can also help modify the material's electronic properties (as in case of strained Si), thus understanding the role of introduced strain and charge transfer on the electronic characteristics of SL graphene is the key to understanding fundamental SL graphene to metal interactions. Raman spectroscopy is a powerful tool for monitoring the physical properties of graphene related damages to the crystal lattice, doping effects, and mechanical strain. Recently, researchers reported the change in Raman signatures as a function of doping by directly controlling the doping concentration by applying a gate voltage in a top or back-gate configuration, which results in a shift in the Fermi energy from the Dirac point [73]. Here, the characteristic G peak position shifted to higher wave numbers (blue-shifts) for increasing Fermi level (*n*-type) and tended to saturate for high doping concentrations. Other studies have also suggested that representative Raman shifts can be due to a combination of doping and induced strain, and the red/blue shift in the representative peak positions (G and 2D) can help differentiate between the two [72], [74], [75]. It has also been previously reported that the relative strength of the G and 2D peaks' shift can provide information of whether the charge-transfer or strain effect dominates [76], [77]. Typically, if the shift of the G peak is much larger than that of the 2D peak, this peak shift is attributed to charge-carrier density modulation rather than mechanical strain [72]. Contrariwise, if the shift of the Raman peaks is caused by mechanical strain due to metal on graphene, the shift of the 2D peak is observed to be much larger than that of the G peak.

In this chapter, we report the size dependent doping/strain induced by sputtered Pt

NPs on single layer graphene for two different Pt NP sizes (0.5 nm and 1.1 nm) through modification of the conduction channel of graphene-based field-effect transistors (FETs) and subsequent Raman peak shift analysis. Pt NPs were deposited using the tilted-target sputtering (TTS) deposition technique atop a graphene sheet, and the NP sizes were controlled by varying the deposition time [78], [79]. While we have shown the Pt NP work function to be strongly related to its size when embedded in dielectrics [80], the Fermi level of graphene can be modulated by the electric gating effect and any charge transfer between the Pt NP and graphene layer, depending on their work function differences. Electrical and Raman characterization have been carried out to probe the effects of strain/doping on the conduction properties of graphene-based FETs.

5.2 Experiment



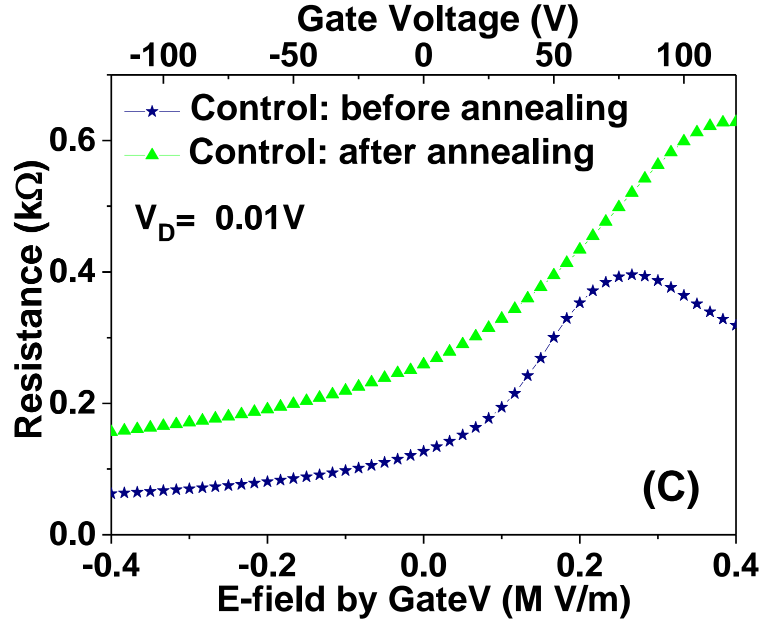


Figure 5-1 Device schematics of graphene FET (a) without and (b) with Pt NPs deposited on top of graphene. (c) R-E characteristics of control sample before and after H_2 annealing.

A schematic diagram of device structures utilized in this study is shown in **Figure 5-1** (a). Chemical vapor deposition (CVD) grown graphene on *p* type heavily doped Si wafer with 300 nm SiO_2 was purchased from ACS Material™. *P*-type heavily doped Si wafers were employed as the substrate with Cr-Au bottom gate contacts. A 2 nm Cr adhesion layer was deposited prior to the 80 nm Au deposition. The 300 nm thermally grown silicon dioxide (SiO_2) on top of the Si substrate was used as the blocking layer. Cr-Au electrodes were thermally deposited atop the graphene layer through a shadow mask with 50 µm channel length and 63:1 width: length ratio, respectively. The samples were then annealed for two hours at 400 °C and 10^{-7} Torr working pressure to remove any PMMA residue, which is typically left behind by the graphene transfer process and is a suspected contaminant that can alter the intrinsic properties of graphene. Pt NPs were sputtered on top of the graphene films using TTS deposition at 30 mW power and 23.8°

target angle for a duration of 5 and 20 seconds [78], [81]. A final 250 ^{o}C H_2 annealing was performed to negate the effect of any sputtering induced plasma damage on the graphene samples and to remove any potential *p* doping effect that had been previously attributed to the presence of residual PMMA [82]. The resistance-gate electric field (R-E) characteristics of the control samples (without sputtered Pt NPs) before and after H_2 annealing are shown in **Figure 5-1** (b). Note that due to the sensitivity of pristine graphene to atmosphere, it is still reasonable to see p-doped behavior after the annealing process, as reported recently in [83].

5.3 Discussion

5.3.1 Pt NP size determination and growth mechanism on graphene

In order to understand the Pt NP/graphene interaction for ultrafine Pt NPs, it is essential to understand their growth mechanism on the underlying graphene support. In this study, we use a complementary metal-oxide semiconductor (CMOS) compatible TTS technique to achieve NPs with controllable sizes, areal densities, and narrow size distributions [5], [7], [37], [38], [41], [78], [81], [84]. These NPs have previously been utilized in Si- and GaAs-based single-layer [5], [84] and multi-layer [7], [21] non-volatile memory (NVM) devices, dye-sensitized solar cells (DSSCs) [81], trace vapor chemical sensors [13], and hydrogen spillover [37] as well as room temperature two-terminal single-electron tunneling devices [41]. Through these studies, the utility of these NPs as discrete charge storage nodes has been demonstrated. Their ultra-small sizes allow observation and controlled charge storage. In addition, they can transfer down to the single electron level at ambient temperature (27 °C) [5], [7], [84]. The Pt NPs used in this study were deposited

using room temperature TTS process on graphene at 30 W power, 23.8 degree target angle for 5 s and 20 s. Since our previous study showed similar Pt NP growth characteristics on Al_2O_3 and graphene during the initial growth phase [79], the Pt NP mean size and areal density were derived from exhaustive TEM studies under similar sputtering conditions on Al_2O_3 films published elsewhere [78] and determined to be 0.5 nm with an areal density of 1.9×10^{12} cm^{-2} for 5 s deposition and 1.1 nm with an areal density of 5.4×10^{12} cm^{-2} for 20 s deposition.

For the aforementioned TTS sputtering conditions employed in this study (30 W power at 23.8^{o} target angle), the incoming metal atoms are less likely to be thermalized and form clusters before hitting the graphene support [78]. As the metal atoms arrive at the surface during the sputtering process, they form a strong bond with the substrate surface, releasing energy. This bond energy is highly characteristic of the defects and kinks on the target surface and can be controlled by controlling the surface properties [78], [81], [85]. For graphene surfaces, the defect sites have been previously shown to have better adhesion and can "pin" the adatoms and control the nucleation phase of the nanoparticle growth process [86]–[88]. The 0.5 nm sized NPs fabricated after 5 s of sputtering are in the nucleation and 2D growth regime [78] where the incoming atoms bond strongly to the defects on the graphene support and are less likely to diffuse on the substrate surface. For a larger deposition time (20 s), the deposition regime switches from 2D to 3D growth where diffusion supersedes nucleation as the dominating growth process. This occurs when all the defect designated nucleation centers are occupied by the "pinned" adatoms and clusters on the graphene surface and additional incoming Pt atoms diffuse on the now "defect-free" surface and eventually migrate to the adatoms and adatom clusters occupying the

nucleation sites. As a result, a larger Pt NP (1.1 nm) is formed. This phenomenon has been previously shown under similar sputtering conditions on amorphous alumina under which the sputtering duration dependent switch from 2D to 3D growth regimes is characterized by an increase in Pt NP size accompanied by a reduction in the mean areal density [78].

Discussion on the initial phases of Pt NP growth on graphene is also important as it may help shed further light on the Pt NP–graphene adhesion energy and subsequent charge transfer process. Previously, Chi et al. performed first principle studies correlating Pt cluster size to binding energy on different carbon surfaces [89]. They reported adsorption characteristics of a single Pt atom and Pt_n (n = 3,7, 13) clusters on a (5, 5) single wall carbon nanotube (SWCNT) where the highest binding energy is found for the Pt_{13} cluster compared to smaller clusters and is considered a function of the number of C atoms adjacent to Pt [89]. However, the cluster size dependent on the binding energy conclusion from the aforementioned study might not be applicable in the Pt NP-graphene system discussed in this paper. This is because, while Chi et al. discuss the adsorption of "preformed clusters" on a curved graphene surface, the Pt NPs employed in this study grow from atoms to clusters on the support surface–starting from nucleation to formation of Pt to C bonds at graphene defect sites, followed by subsequent growth into larger particles through diffusion as the nucleation sites have been filled previously. The 0.5 nm Pt NPs (~4 Pt atoms) generated in the 2D growth regime are more likely to have a larger proportion of the NP's low-coordination number atoms in close contact with graphene, possibly leading to large binding energy, which can lead to a smaller Pt NP to graphene distance that can generate a more efficient charge transfer. Counterintuitively, for the larger Pt NP (1.1 nm – ~47 atoms), generated in the diffusion dominated 3D growth regime, Pt atoms

adjacent to the graphene might exhibit higher coordination numbers, lower binding energy leading to the Pt NP being further away from the graphene support compared to 0.5 nm Pt NP. Thus, based on the growth mechanism of Pt NPs on graphene and the transition from 2D growth (0.5 nm NP) to 3D growth regime (1.1 nm NP), it is likely that the 0.5 nm Pt NPs might exhibit stronger bonding to the graphene support compared to the larger Pt NPs.

5.3.2 Electrical characterization of Pt NP-Graphene based FETs

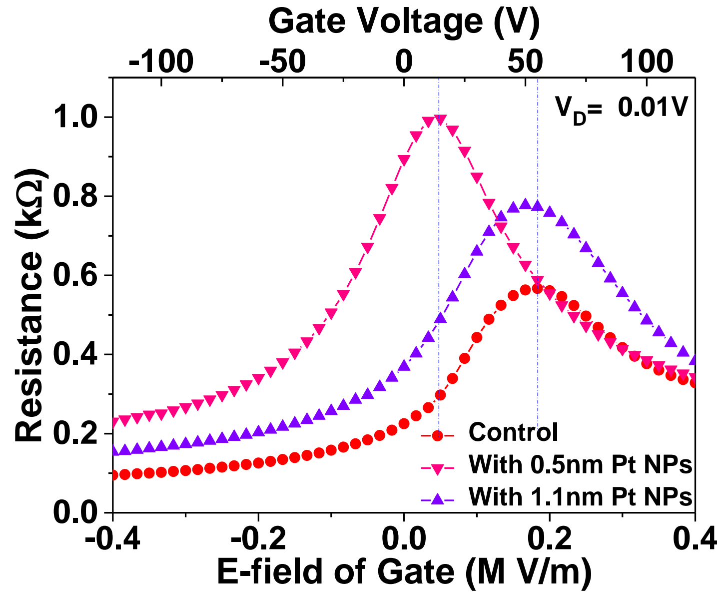


Figure 5-2 Comparison of resistance-electric field characteristics for devices with and without conduction channel modification by different sizes of Pt NPs

All I-V measurements of Pt NP-graphene-based FETs were conducted in a triaxial guarded and electromagnetic shielded Signatone™ probe station in a dark, nitrogen environment at room temperature (~300 K). During the measurements, the source electrode was fixed at 0 V, while the drain and gate electrodes were biased at different values. To ensure that property changes were due to Pt NP deposition rather than sample variation,

samples were first characterized as a control before sputtering Pt NP on the same post characterization control samples. **Figure 5-2** shows a comparison of R-E characteristics for a graphene FET with and without conduction channel modification using different sizes of Pt NPs, with the gate voltage sweeping from -120 V to 120 V at a drain voltage of 0.01 V. The relatively high gate bias is used due to the relatively small gate capacitance of a thick (300 nm) SiO_2 blocking layer. The maximum resistance peak indicates the charge neutralization point, which corresponds to the Dirac point of the graphene layer in a FET structure [70]. In the gate voltage region from -120 V to the Dirac point, the Fermi energy is raised above the Dirac point by the gate voltage, resulting in hole conducting transport; whereas, in the gate voltage range from 120 V to the Dirac point, the Fermi energy is lowered below the Dirac point by the gate voltage, resulting in electron conducting transport. The graphene layer of the control device (without Pt NPs) showed *p*-type behavior, with the Dirac point at ~55 V (0.18 MV/m). We attribute this initial positioning of the Dirac point to the metal electrode in contact with graphene and the resultant band alignment between the work functions of the Cr-Au electrodes and graphene. Song et al. [90] and Park et al. [91] have shown that the work function of graphene does depend on the type of metal used as the contact, with a Dirac point shift of more than 80 V for graphene with Cr-Au electrodes [90]. After a 0.5 nm Pt NP deposition, a Dirac point shift of -40.8 V was observed for the sample, indicating *n*-type doping, whereas minimal change was observed for 1.1 nm Pt NP devices (**Figure 5-2**). Here, the doping concentration N can be estimated by

$$N = \frac{C_{ox} \times \Delta V_{th}}{q} \quad (5\text{-}1)$$

where Cox is the oxide capacitance (~ 11.5 nF/cm^2 for 300 nm SiO^2), q is the elementary charge, and $\Delta V_{th} \approx -40.8$ eV is the Dirac point shift caused by the 0.5 nm Pt NPs. The doping concentration is calculated to be about -2.93×10^{12} cm^{-2}, which is comparable to the mean areal density (1.90×10^{12} cm^{-2}) of the 0.5 nm Pt NPs (see **section 5.3.1** for more details). As the actual areal density is typically larger than the areal density measured in TEM analysis, (due to the fact that NP size smaller than 0.5 nm are difficult to resolve), it can be safely assumed that each of these sub-nm Pt NPs contributes approximately one electron to the graphene conduction channel.

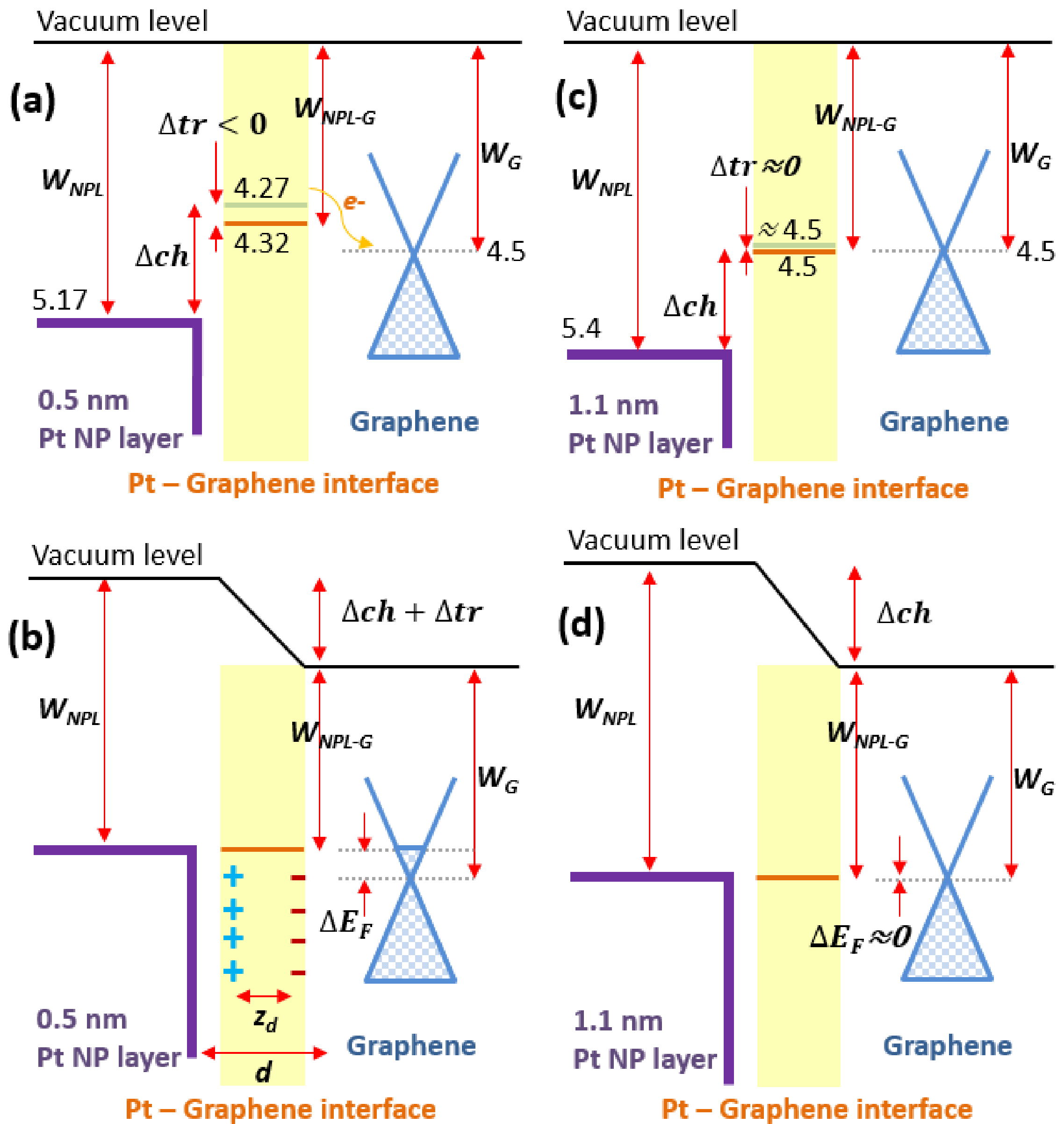


Figure 5-3 Schematic of changes in energy band diagram for graphene-based FET before (a, c) and after (b, d) Pt NP deposition: (a, b) device with 0.5 nm Pt NP layer showing n-type doping behavior; (c, d) device with 1.1 nm Pt NP layer showing no doping behavior.

It should be noted that although the Pt NPs are discrete in nature, it is reasonable to assume an effective Pt NP layer on the conduction channel when studying the macroscopic conduction properties of a FET structure [92]. **Figure 5-3** shows the schematics of an energy band diagram for our graphene FETs with 0.5 nm and 1.1 nm Pt NP layers,

respectively. To study the contribution of charge transfer to the formation of interface charge dipole between the Pt NP layer and the graphene, a plane capacitance model was adopted, where the change in potential energy (Δtr) [93] can be calculated by

$$\Delta tr(d) = e\Delta Q/C = e^2/\varepsilon_0 \cdot N(d) \cdot z_d \quad (5\text{-}2)$$

where d is the Pt NP layer-graphene separation, $z_d \approx d - 2.4$ Å is indicative of the effective distance between the two surface charges, and $N(d)$ is the doping concentration. In addition, the change in potential energy $\Delta ch(d)$ due to chemical interaction between the Pt NP layer and the graphene layer must also be considered [93]. For the optimized bulk Metal-graphene separation of $d_{eq} \approx 3.3$ Å, $\Delta ch(d) \approx 0.9$ eV. It should be noted that the contribution $\Delta ch(d)$ is dependent on d, and can still be larger than 0.9 eV for the case of ultra-small Pt NP due to the likely smaller metal-graphene distance (smaller than 3.3 Å, as previously discussed in **Section 5.3.1**) compared to a larger NP and bulk [70]. The Fermi level shift (ΔE_F) in graphene can be expressed as

$$\Delta E_F(d) = W_{NPL} - W_G - \Delta tr(d) - \Delta ch(d) \quad (5\text{-}3)$$

where W_{NPL} and $W_G \approx 4.5\ eV$ are the effective free air work function of the Pt NP layer and the graphene layer, respectively. The crossover point ($\Delta E_F = 0, \Delta tr = 0$) of metal free air work function from n- to p-type doping of graphene is given by $W_0 = W_G + \Delta ch \approx$ 5.4 eV. Thus, based on these calculations, the graphene layer would be p doped by Pt NPs with a work function larger than 5.4 eV, and n doped with a work function smaller than that. Considering the linear density of state (DOS) of graphene $D(E) = D_0|E|$ with $D_0 \approx 1.737\times10^{14}$ eV cm^{-2} and by taking the integration one can attain

$$\Delta E_F = \pm\sqrt{\frac{2N}{D_0}} \tag{5-4}$$

For experimentally determined $N \approx$ -2.93×10^{12} cm^{-2} of 0.5 nm Pt NP layer, ΔE_F is estimated to be -0.18 eV; while for 1.1 nm Pt NP layer, there is no perceptible shift in the Dirac point and $\Delta E_F \approx 0\ eV$. By combining equations (5-2)–(5-4), the effective free air work function (W_{NPL}) of the Pt NP layer can then be estimated by

$$W_{NPL} = \pm\sqrt{\frac{2N}{D_0}} + W_G + \Delta ch + e^2/\varepsilon_0 \cdot N \cdot z_d, \tag{5-5}$$

where (W_{NPL}) can be calculated as ~5.17 eV for 0.5 nm layer and ~5.40 eV for 1.1 nm Pt NP layer. It should be noted that the actual work function of individual Pt NPs would be smaller than the calculated value which is based on the assumption of an effective Pt NP layer. To determine the work function of individual Pt NPs, a multiple sphere-plane capacitance model has to be used instead to determine the change in potential energy due to charge transfer. Nevertheless, the above calculation is in accordance with previous studies showing that the effective work function of a layer of sub 1 nm Pt NPs can be much smaller than that of bulk material [82], [94]. The NP size dependent work function of Pt NPs is expected to be between 1.5 (single atom) to 6.1 eV (bulk) depending on the actual size, packing and surrounded dielectrics.

5.3.3 Raman Spectroscopy Study

Raman spectroscopy was carried out to further study Pt NP deposition induced doping and mechanical strain on the graphene layer. The relative shifts of the G and 2D peaks can be used to determine the combined effect of Pt NP induced doping and strain to

the graphene layer [72]–[77]. **Figure 5-4** shows a representative Raman spectra comparing the G and 2D peak position of a graphene layer under different sputter durations with the control graphene sample. The average G and 2D peak positions are summarized in **Table 5-1**. For the control graphene sample, the G peak position is at 1,582.9 cm^{-1} and the 2D peak position is at 2,696.5 cm^{-1}. After sputtering 0.5 nm Pt NPs, the G peak positioning blue shifts to 1591.9 cm^{-1}, and the 2D peak remains relatively unchanged (after considering the standard errors) at 2,695.7 cm^{-1}. Meanwhile, after sputtering 1.1 nm Pt NPs on graphene, similar to the 0.5 nm Pt NP case, the G peak position also blue shifts to 1,591.9 cm^{-1} and the 2D peak displays a significant blue shift to 2704 cm^{-1}. These shifts in the characteristic peak positions are indicative of significant changes in the resonant vibrational modes of the underlying graphene structure after Pt NP deposition. As mentioned previously, these shifts could be indicative of graphene doping or mechanical strain on the graphene layer.

While studying mechanical stress induced by Pt NPs on the graphene surface, one must consider the degree of mechanical strain imposed by the sputtered Pt NPs. Based on a recent study, metal thin films with high lattice order mismatch on graphene results in a significant shift in 2D positioning (due to increased strain) [72]. Similar to metals like Au and Ag, a large lattice mismatch exists for Pt on graphene. Other studies also seem to indicate mechanical strain will primarily influence the 2D peak position with G peak splitting encountered at larger strains [74], [75]. While depositing metals with matching lattice indices to the underlying graphene surface (< 2% strain-like Co and Ni) [72], a larger shift appears in the positioning of the G peak compared to the shift in the 2D peak. This representative shift in the relative peak position was attributed to successful

doping. However, for metals with larger lattice mismatches, Raman analysis is typically attributive of mechanical strain induced shifts; hence, doping effects are hard to surmise from Raman analysis.

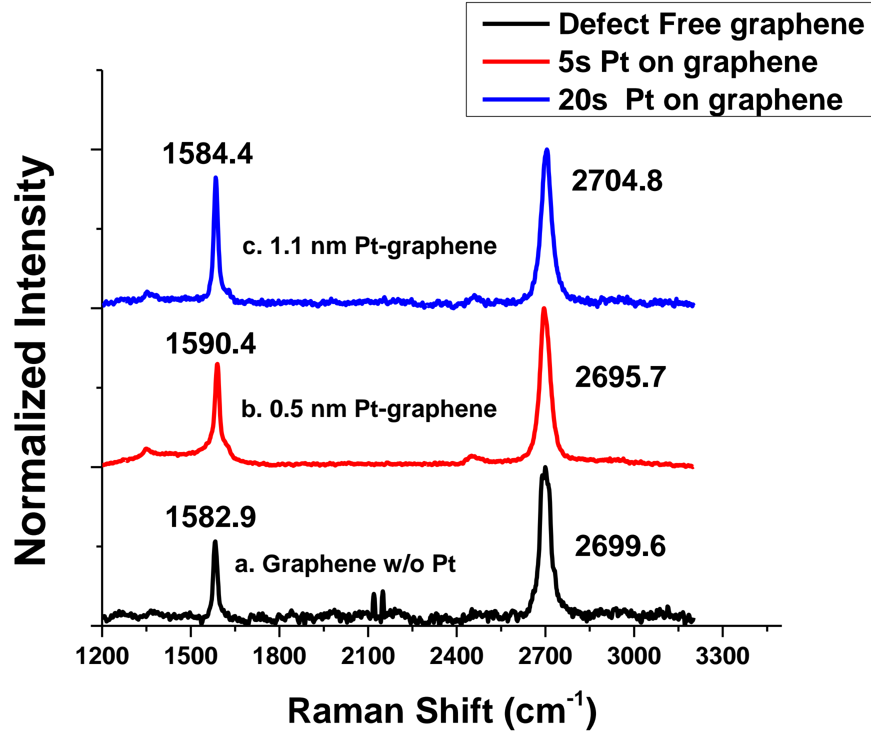


Figure 5-4 Representative Raman spectra of the control graphene sheet (curve a) and after depositing 0.5 nm Pt NPs (curve b) with 1.1 nm Pt NPs (curve c) on top.

Table 5-1 Summary of average G and 2D peaks positions taken at five separate points across the samples and the G and 2D peak shift magnitudes with the uncertainty for each condition (based on the propagation of errors method) in **Figure 5-4**.

Sample	**Mean Pt NP Size (nm)**	**G band (cm^{-1})**	**2D band (cm^{-1})**	**ΔG (cm^{-1})** (uncertainty w.r.t control)	**Δ2D (cm^{-1})** (uncertainty w.r.t control)
Defect-free graphene	-	1583.8±1.8	2696.5±4.9	-	-

Sputtered for **5 s** at 30 W, 23.8° target angle	0.5	1587.8±2.6	2697.1±6.3	**4.0** (3.2)	**0.6** (8.0)
Sputtered for **20 s** at 30 W, 23.8° target angle	1.11	1588.4±3.4	2704.0±0.2	**4.6** (3.8)	**7.5** (4.9)

Based on the shift in representative peak positions (as listed in **Table 5-1**) for the 0.5 nm decorated graphene sample, there are only significant changes in the G peak positioning (4.0 $\pm$ 3.2 cm^{-1}), not the 2D peak (0.6 $\pm$ 8.0) cm^{-1}. This might be counterintuitive. Based on the study by Wang et al. [72] for metals on graphene with a large lattice mismatch, there should be a significant shift in the 2D peak position and no significant changes in the G peak position. However, based on the observed shifts in the Raman peak positions (**Table 5-1**), it appears as if these NPs do not induce discernable mechanical strain on graphene, but rather successfully induce charge density carrier modulation, i.e., the NPs dope the graphene film. The type of doping (*n* or *p*) can be determined by the red/blue shift in the G band positioning [73] and in this case, the blue-shift in the G band location is significantly larger than the error bars and hints towards a successful *n*-type doping of the graphene sample. This is corroborated by the electrical measurements discussed in **Section 5.3.2** where the Dirac point shift also indicates the *n*-type doping of graphene. However, in the case of a 1.1 nm decorated graphene sample, there are significant changes in the G peak and 2D peak positioning. This falls more in line with the observations of Wang et al. [72] as there is a significant shift in the 2D peak position (7.5 $\pm$ 4.9 cm^{-1}) with less significant changes in the G peak position (4.6 $\pm$ 3.8 cm^{-1}) which is indicative of mechanical straining of the graphene lattice. Again, this is corroborated by the electrical measurements discussed in **Section 5.3.2** where there is

minimal Dirac point shift indicative of a lack of doping. As discussed previously in **Section 5.3.1**, the experimental evidence discussed so far hints that for larger (1.1 nm) Pt NPs on graphene, there would be a straining on the graphene surface due to the large lattice mismatch of the deposited Pt NPs, but these Pt NPs could be at a larger distance from the support surface, leading to less efficient doping. Thus, the shifts in characteristic Raman peaks together with the associated Dirac point shifts (or there might not be any charge transfer to the graphene surface at all–as in the case of 1.1 nm Pt NP decorated graphene). This study indicates that 0.5 nm Pt NPs lead to a charge transfer and subsequent *n*-type doping of graphene, whereas in the case of 1.1 nm Pt NPs, the strain effect dominates, and there is little indication of charge transfer to the graphene layer.

Chapter 6. Organic non-volatile memory with embedded sub-nanometer Pt NPs

This chapter discusses the application of the single electron charging behavior of MNPs on macroscopic devices, a low operation voltage pentacene transistor-based non-volatile memory (NVM) device is proposed and studied by embedding size-tunable sub-2 nm Pt NPs between the tunneling and blocking dielectric layers. A controllable work function was observed in the embedded Pt NPs through the size-dependent threshold voltage shift. NVM transistors containing embedded Pt NPs exhibited Pt NP size- and density-dependent memory window behavior in their transfer characteristics, which was attributed to electron and hole charging and discharging behavior by the Pt NPs. While devices with small (0.5 nm) Pt NPs demonstrated a strong Coulomb blockade and quantum confinement with electron addition energy as large as 1.993 eV, those made with larger (1.8 nm) Pt NPs allowed for storage of a single charge per NP memory.

6.1 Introduction

In this chapter, we elucidate the electron/hole injection properties of Pt NPs embedded in the Al_2O_3 dielectric layers of a pentacene-based NVM device by tuning the size-dependent Pt NP work function. The work function of metal NPs is strongly affected by the surrounding dielectric, as explained by the Fermi level pinning theory [95]. As such, the size-dependent work function of embedded metal NPs can differ considerably from unsupported nanoparticles [96]. While photoemission, thermal emission, and Kelvin probe measurements can generally be used for the measurement of work functions of surfaces,

these methods are not readily applicable to NPs embedded within an NVM structure. Taking advantage of the dependence of the threshold voltage on the metal NP work function, we explored the NP size-dependent work function of the NP-embedded samples by probing the shift of threshold voltage of the current voltage characteristics compared to the control device. While smaller (0.5 nm) Pt NPs showed electron charging behavior due to the smaller work function, larger (1.3 nm and 1.8 nm) Pt NPs showed both electron and hole charging behavior due to a better work function alignment with the Fermi level of pentacene. The memory transistor exhibits controllable memory window behavior, which is dependent on the size and density of Pt NPs. Devices with 0.5 nm Pt NPs have small memory windows due to a strong Coulomb blockade effect and quantum confinement, whereas devices with 1.8 nm Pt NPs show storage of a single charge per NP, which may prove advantageous to the further development of nanoscale NVM and sensor applications.

6.2 Experiment

A heavily doped p-Si substrate (0.001–0.005 Ω-cm, Silicon Quest International) with Cr/Au (2.5 nm/80 nm) thermally deposited on the back (unpolished) side was used as the bottom gate electrode. After organic cleaning and subsequent drying with a stream of N_2 gas, an 18 nm Al_2O_3 charge blocking layer was deposited by atomic layer deposition (ALD). ALD-processed substrates were then introduced into a sputtering chamber for Pt NP deposition, which was carried out for 10, 20, or 30 s at 30 W RF power, 4 m Torr working pressure, and a 10 sccm Ar gas flow rate at room temperature. Pt NP-decorated substrates were immediately transferred to the ALD chamber and a 2.5 nm Al_2O_3 tunneling layer was deposited and annealed in H_2 at 260 °C for 45 min to passivate interface states

in the dielectric and improve gate dielectric quality. The Al_2O_3 tunneling layer was then subjected to 40 W O_2 plasma for 5 min and immersed in 0.05 wt% octadecyltrichlorosilane (OTS, Sigma-Aldrich) solution in toluene for 3 h. A 60 nm thick pentacene (Sigma-Aldrich) active film was then deposited at 80 °C with an 0.2 Å/s deposition rate without any purification. Au source and drain electrodes (80 nm) were deposited at room temperature with 1 Å/s deposition rate. Pentacene and Au layers were patterned via shadow mask using a thermal evaporator with a base pressure of 10^{-7} Torr. Device channel lengths (L) and widths (W) were 50 and 1,250 μm, respectively. A control sample was prepared by the same process excluding Pt NP deposition to verify that the observed memory window was due to Pt NPs and not due to charge trapping sites in the dielectric or organic semiconductor layers.

NVM FET devices were characterized immediately after removal from the thermal evaporator chamber. A Signatone WL-210E probe station was operated in the dark, under N_2-purged conditions to minimize degradation by moisture, air, or light. Output and transfer properties were measured at room temperature by a Keithley 4200-SCS semiconductor characterization system with a pulse generator.

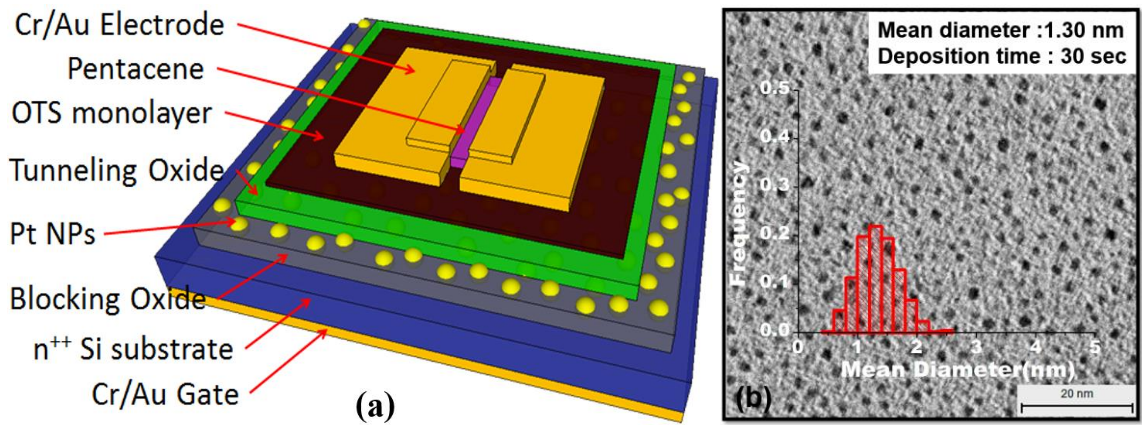


Figure 6-1 (a) Schematic illustration of pentacene FET; (b) plane view TEM image of uniformly distributed 1.30 nm Pt NPs with scale bar: 20 nm (Inset: frequency distribution of 1.30 nm Pt NP).

6.3 Discussion

6.3.1 Transistor Characteristics

Figure 6-1 (a) shows a schematic of the final bottom gate, top contact pentacene NVM FET device with Pt NPs embedded in the gate dielectric layer. Pt NPs were varied in size across the sub-2 nm regime by altering the TTS deposition time. The resultant NPs were spherical in shape with narrow particle size distributions. **Figure 6-1** (b) shows a plane view transmission electron microscopy (TEM) image of uniformly distributed 1.30 nm Pt NPs. From TEM image statistical analysis, sputtering deposition times of 5, 30, and 60 s resulted in Pt NPs with 0.52 ± 0.12 nm, 1.30 ± 0.31, and 1.8 ± 0.65 nm mean particle diameters (hereafter referred to as “0.5 nm,” “1.3 nm” or “1.8 nm”), respectively, and areal densities of 1.7 ± 0.5, 7.5 ± 0.2, and 7.1 ± 0.3 ($\times 10^{12}$ cm^{-2}), respectively. Relatively narrow size distributions were obtained using the TTS deposition technique (**Figure 6-1** (b), inset), which is critical to identifying changes to specific device characteristics based on Pt NP diameter. We believe that the dominant cluster growth mode changes from two-

dimensional to three-dimensional cluster growth for deposition times of 5–20 s and 25–45 s, respectively, showing an increase in NP densities according to different durations of deposition time. Beyond 45 s, the Pt clusters begin coalescing to form larger particles and the NP number based on density starts to decrease. Details of the Pt NPs growth evolution for different TTS deposition times and its effects on the NPs size and density has been reported elsewhere [3], [4], [7], [13], [21], [22], [97].

Figure 6-2 (a) and (b) show the output characteristics of pentacene-based FETs without and with 1.3 nm Pt NP, respectively. Output curves were measured using a 0.1 V drain voltage step after a 0.1 s delay and gate voltage varying from 1 to − 4 V in 1 V steps. Under the influence of a negative bottom gate voltage, holes are injected into the pentacene layer from the top Au source electrode, which creates an accumulation layer. Both devices exhibit typical p-channel behavior with hole accumulation mode at negative gate voltage and hole depletion mode at positive gate voltage. In addition, both devices showed well-defined current modulation with good linear and saturation behaviors at low and high drain voltages, respectively.

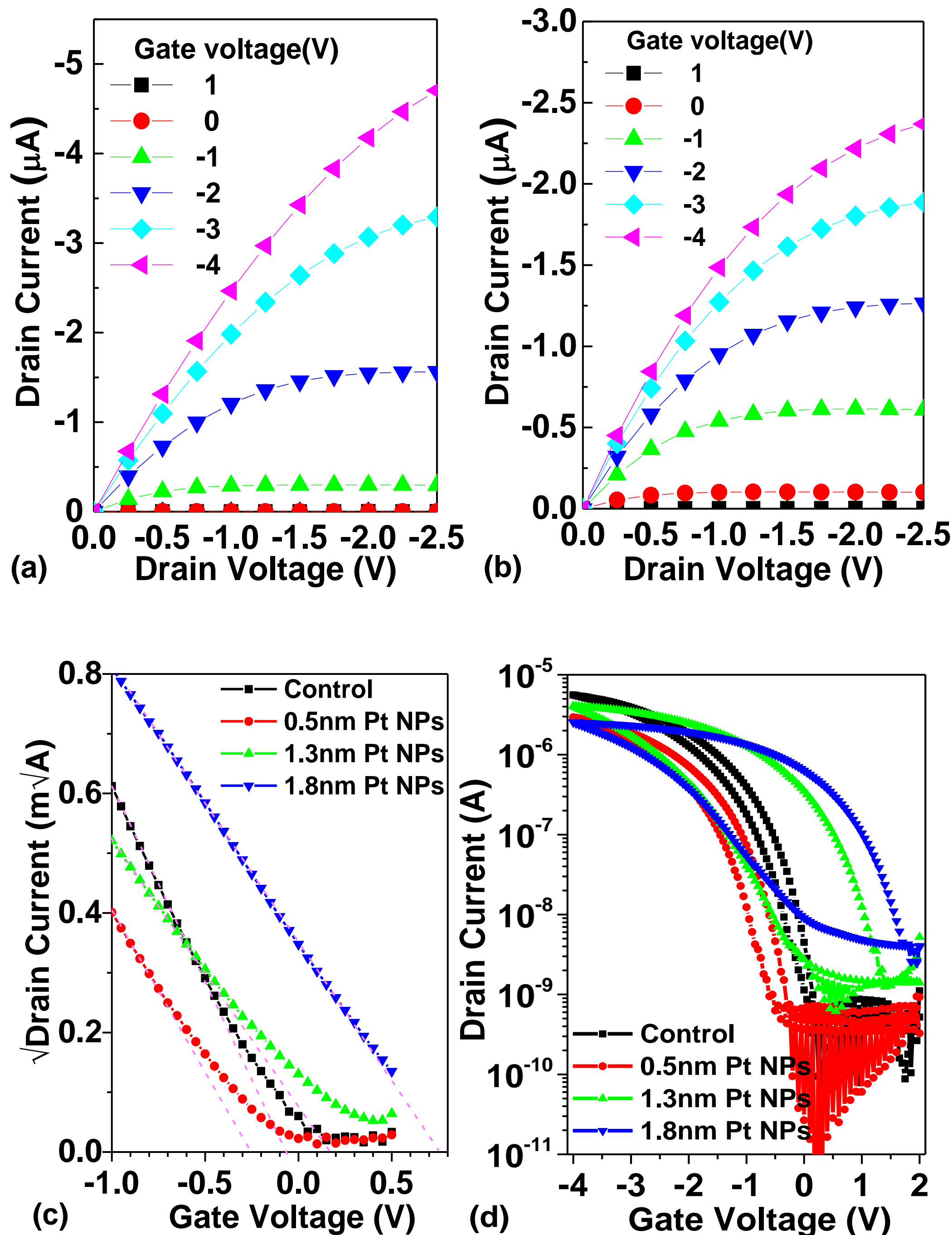


Figure 6-2 (a) and (b) Output characteristics of (a) control device and (b) device with embedded 1.3 nm Pt NPs; (c) and (d) Comparison of pentacene FET transfer characteristics without and with Pt NPs measured at -2.5 V drain voltage with gate voltage sweeping from (c) 0.5 V to -1 V and (d) 2 V to -4 V.

6.3.2 Observation of Size Dependent Effective Work Function of Pt NP Layer in an OFET Architecture

The transfer characteristics of pentacene FETs without and with Pt NPs are shown in **Figure 6-2** (c) and (d). In this experiment, the gate voltage was swept from a positive to negative value and back in 0.5 V increments while the drain voltage was fixed at − 2.5 V. All devices were scanned in a narrow voltage range of 0.5 V to − 1 V (**Figure 6-2** (c)) to find the region with minimum hysteresis, indicating negligible Pt NP charging. The field effect mobility (μ) in the saturation region is calculated using Eq. (1), where W and L are the channel width and length, respectively; C_{OX} is the gate capacitance per unit area; and V_G, V_D and V_{TH} are the source-gate, source-drain, and threshold voltage, respectively.

$$\mu^{Sat} = \frac{2L}{W} \times \frac{1}{C_{OX}} \times \left(\frac{\sqrt{I_D^{Sat}}}{V_G - V_{th}}\right)^2 ,\ for\, |V_G - V_{TH}| < V_D \quad (6\text{-}1)$$

The saturation hole mobility of the control sample was 0.087 ± 0.015 $cm^2/V{\cdot}s$, which is about two times greater than the device with embedded Pt NPs. The mobilities for the 0.5, 1.3, and 1.8 nm Pt NPs devices are 0.0463 ± 0.012, 0.0384 ± 0.017, and 0.0453 ± 0.021 $cm^2/V{\cdot}s$, respectively. No significant NP size dependent mobility for the devices are observed. Note that these values are lower than state-of-the-art high performance OFETs; furthermore, the reported Pt NP size-dependent work function and memory behavior in this study did not rely on mobility. The results are beneficial to different OFETs when embedding small size metal NPs regardless of the mobility of the semiconducting layer.

The threshold voltage (V_{TH}) was estimated from the *x*-intercept of the linear fit of the square root of drain current versus gate voltage. Hysteresis was determined by the

change in threshold voltage at different measurement conditions. The control sample threshold voltage (V_{TH}) was − 65.1 mV, indicating small work function difference between the heavily doped p-Si gate electrode and the Fermi level of the hole conducting pentacene. Size-dependent threshold voltages were observed from the devices with embedded Pt NPs, which are direct evidence of the size-dependent work function of Pt NPs embedded within the Al_2O_3. Threshold voltages were − 255.9 ± 35.2 mV, 173.8 ± 47.6 mV, and 717.8 ± 65.3 mV for 0.5 nm, 1.3 nm, and 1.8 nm Pt NPs, respectively, indicating a relatively small work function for 0.5 nm Pt NPs and relatively large work functions for 1.3 nm and 1.8 nm Pt NPs compared to the Fermi level of pentacene. Thus, Pt NPs with diameter between 0.5 nm and 1.3 nm were expected to have the best band alignment, illustrated in the energy band diagram below (**Figure 6-3**). Future study from first principles will better elucidate the mechanism of Pt NP size dependence on work function when embedded in Al_2O_3.

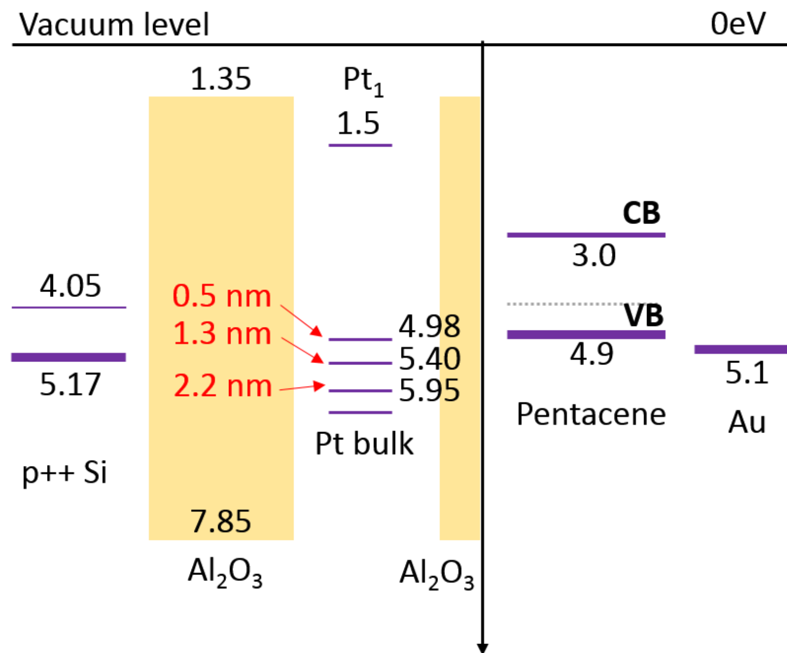


Figure 6-3 Energy band diagram of pentacene FET with embedded Pt NPs under flat band condition

In most crystalline silicon-based field-effect transistors (FETs), the devices are operated in the inversion regime, with the threshold voltage specified as the gate bias at which the Fermi level at the insulator/semiconductor interface crosses the middle of the gap [98]. Meanwhile, organic FETS (OFETs) are generally operated in the accumulation regime, in which the gate voltage is polarized positively (negatively) versus the n-type (p-type) substrate and the "threshold voltage" corresponds to a gate-bias-dependent mobility [99]. This "threshold voltage" was found to be

$$V_{TH} = \pm\frac{qn_0d_s}{C_{OX}} + \phi_{ms} - \frac{Q_f}{C_{OX}} \tag{6-2}$$

where q is the elemental charge, n_0 is the density of free carriers at equilibrium, d_s is the thickness of the semiconductor, C_{OX} is the accumulation capacitance density of the oxide, ϕ_{ms} is the work function difference between the gate electrode and the semiconductor, and Q_f is the density of fix charges within the oxide layer. The first term on the right represents the contribution from the bulk free carriers, whereas the second and third terms are the contributions from the flat band potential. Although it is particularly difficult to derive the work function of individual Pt NPs due to the discontinuous nature of the discrete floating gate, a reasonable estimation is the effective work function ϕ_{NP} of the overall Pt NP layer using

$$\phi_{NP} = \phi_m - q\Delta V_{TH} \tag{6-3}$$

where ϕ_m is the work function of the gate electrode, heavily doped p-type silicon (~5.17 eV) in our case, and ΔV_{TH} is the shift in threshold voltage for a sample with embedded Pt NPs with respect to the control sample. The effective work functions of different size Pt NPs as

floating gates were calculated and summarized in **Table 6-1**. For Pt NPs with diameter of 0.5 nm, the effective work function of 4.98 eV was found to be smaller than that of the bulk Pt, which is 5.3–6.35 eV. Meanwhile, the effective work function (5.95 eV) of 1.8 nm Pt NPs approached the bulk work function. Note that the actual work function of these Pt NPs could be underestimated due to the discrete nature of the NP floating gate. For the relatively lower density of the 0.5 nm Pt NPs sample, the work function could be much lower than 4.98 eV.

Table 6-1 Experimentally derived effective work function of different size Pt NPs embedded within the Al_2O_3 dielectric

Pt NP diameter (nm)	0.5 ± 0.1	1.3 ± 0.3	1.8 ± 0.7
Threshold voltage (mV)	− 255.9 ± 35.2	173.8 ± 47.6	717.8 ± 65.3
Change in threshold voltage, ΔV_{TH} (mV)	− 191.8 ± 50.4	237.9 ± 62.8	782.9 ± 80.5
Effective work function, ϕ_{eff} (eV)	4.98 ± 0.05	5.40 ± 0.06	5.95 ± 0.08

6.3.3 Electrically charging and discharging behavior via sub-2 nm Pt NPs

Sweeping the gate voltage between − 4 V to 2 V yielded a hysteresis of 0.309 V in the control sample, which is due to the presence of bulk traps within the Al_2O_3 layer (**Figure 6-2** (d)) [100]. However, pentacene FETs with embedded 0.5 nm, 1.3 nm, and 1.8 nm Pt NPs exhibited clear memory windows of 0.512 V, 2.09 V, and 2.93 V, respectively. Although there was partial influence of bulk traps and interface states, it can be concluded that Pt NPs play a major role as charge storage nodes. Counterclockwise hysteresis loops were observed for all NVM devices with embedded Pt NPs, indicating hole injection from pentacene to Pt NPs at negative voltages (i.e., program operation) and electron injection at positive voltages (i.e., erase operation). When sufficient negative

voltage is applied to the gate electrode, holes are injected from the pentacene FET channel through the 2.5 nm tunneling layer via Fowler-Nordheim tunneling and are stored in the Pt NPs [101]. This process is reversed in the erasing operation mode. Holes are withdrawn from the Pt NPs through the pentacene layer when a positive gate voltage is applied, resulting in detrapping of the Pt NPs. A relatively thick blocking dielectric layer was used to prevent charge transfer from the gate to the Pt NPs and vice versa during program/erase operation. Injection of holes or electrons into the Pt NP layer will lead to a negative or positive shift in V_{TH}, which represents the memory window of organic NVM FET [102].

Dual sweeping memory behavior was observed for both the control device and device with embedded 1.3 nm Pt NPs at different ranges of sweeping gate voltages (**Figure 6-4** (a) and (b)). We attribute the memory window for the control device to the interface and bulk traps of the oxide layer, which is considerably smaller than devices with embedded Pt NPs. The corresponding Pt NP size-dependent threshold voltages for different sweeping gate voltages are summarized in **Figure 6-4** (c). Due to the abovementioned size-dependent embedded Pt NP work function, size-specific electron/hole charging properties can be seen for each device. A negative shift in threshold voltage was observed for the device with 0.5 nm Pt NPs when the sweeping gate voltage started coming from either direction, indicating hole charging. For 1.3 nm Pt NP devices, the threshold voltage shifted negatively for gate voltage sweeping from the negative direction and positively for sweeping from the positive direction, indicating both electron and hole charging characteristics. Meanwhile, devices with 1.8 nm Pt NPs showed better electron injection efficiency than hole injection.

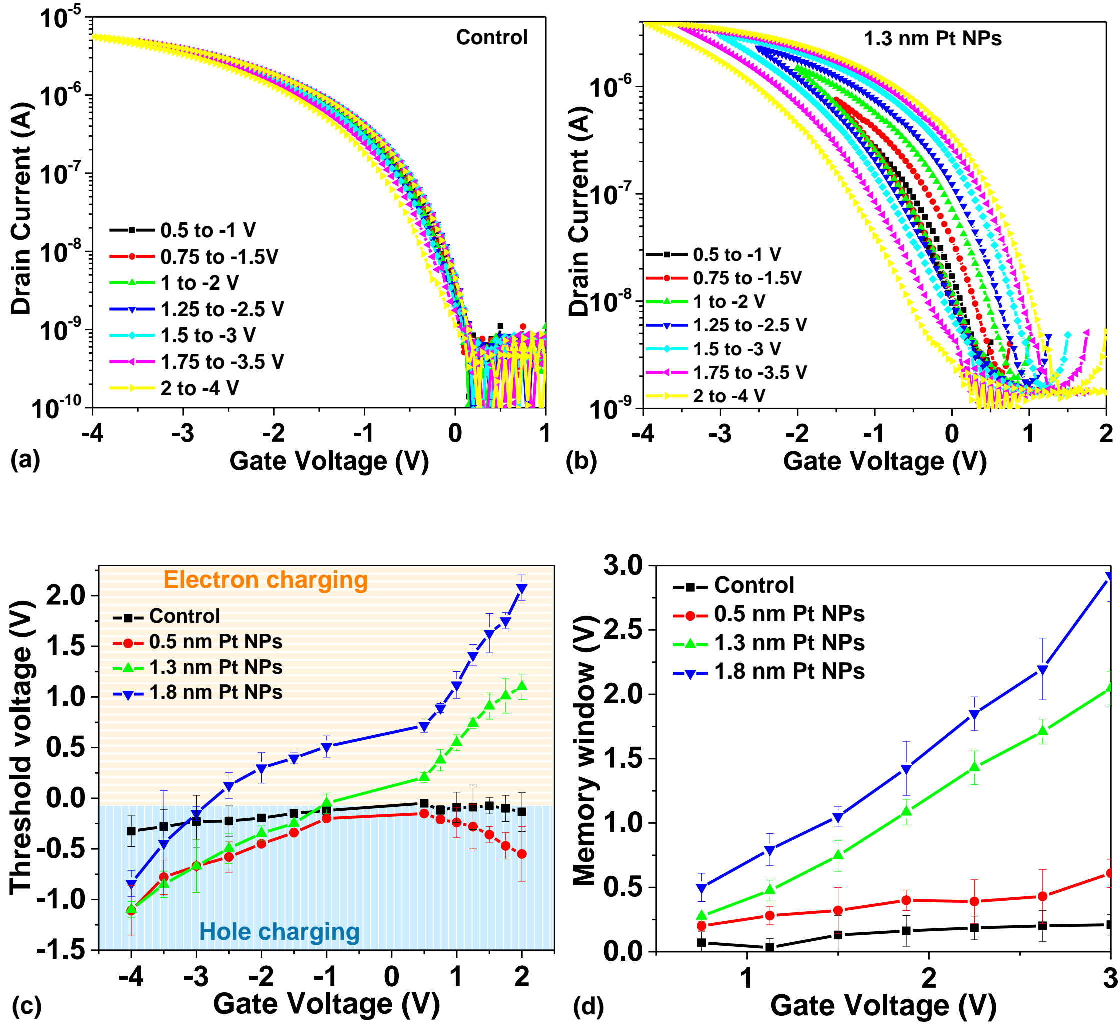


Figure 6-4 (a & b) Memory behavior of pentacene FET (a) without and (b) with 1.3 nm Pt NPs measured at -2.5 V drain voltage and sweeping gate voltage; (c) threshold voltage shift and (d) memory window under different gate bias sweeping for sample with different size Pt NPs.

Pronounced Pt NP size-dependent memory window behavior was observed as a function of sweeping gate voltage (**Figure 6-4** (d)), increasing with Pt NP diameter due to the increase in total Pt NP capacitance. Further, the memory window (ΔV_{TH}) increased monotonically with applied sweeping gate voltages for NVM devices with 1.3 nm and 1.8 nm embedded Pt NPs. The trapped charge densities were calculated using the relationship

$$N_t = \frac{C_{OX}\,\Delta V_{TH}}{q} \tag{6-4}$$

where N_t is the trapped charge density, C_{OX} is the accumulation capacitance density of the oxide, and q the elementary charge. For a gate voltage of ±3 V, the corresponding effective charge densities were 9.8×10^{11} cm^{-2}, 4.6×10^{12} cm^{-2}, and 6.8×10^{12} cm^{-2} for 0.5 nm, 1.3 nm, and 1.8 nm Pt NPs, respectively, (Note: 0.21 V was subtracted from ΔV_{TH} to compensate for trap charges). Considering the respective Pt NP areal densities of 1.7×10^{12} cm^{-2}, 7.5×10^{12} cm^{-2}, and 7.1×10^{12} cm^{-2} for 0.5 nm, 1.3 nm, and 1.8 nm Pt NPs, the charges per NP were found to be 0.58, 0.62 and 0.96, respectively. This suggests approximately ~1 charge per 1.8 nm Pt NP.

Meanwhile, charging efficiency appears to reduce with decreasing Pt NP diameter. While the 0.5 nm Pt NPs samples showed an almost constant memory window throughout 0 to 2.5 V of gate bias, samples with 1.3 and 1.8 nm Pt NPs showed a monotonic increase in memory window as a gate bias increase. We attribute this to be due to the relatively large electron addition energy and the above mentioned lower equivalent work function for the sample with smaller size NPs. The electron addition energy can be estimated by $U_N = E_C + E_N$, where the Coulomb charging energy for a single electron charging event is determined by $E_C = q^2/2C_{tot}$, with q being the unit charge, and $C_{tot} = C_{channel} + C_{gate}$ being the total capacitance coupled to the NPs [17], [41]. Given the relatively small size of the Pt NPs with respect to the channel and the electrodes, the mutual capacitance of the Pt NPs to the conduction channel $C_{channel}$ and the bottom gate electrode C_{gate} can be estimated by a spherical particle to parallel plate model, respectively:

$$C = 2\pi\epsilon\sqrt{d^2 - 4a^2}\sum_{j=0}^{\infty}(coth\left[\left(j + \frac{1}{2}\right)arcosh\left(\frac{d}{2a}\right)\right] - 1) \tag{6-5}$$

where a is the sphere radius, d is the distance between the center of the sphere and the plane, and ε is the permittivity of the dielectric. The dielectric constants of our ALD grown Al_2O_3 is ~7.5. The quantum confinement energy E_N can be estimated by $E_N = 2 * E_F/(3 * N)$, where E_F is the Fermi energy of Pt, and N is the total number of electrons for Pt NPs. The electron addition energy was then estimated to be 1.993 eV for 0.5 nm Pt NPs and decreased to 0.133 eV for 1.8 nm Pt NPs, approaching the thermal energy at 300 K (0.259 eV).

For smaller Pt NPs, a larger gate voltage is required for the charges to overcome the additional required addition energy. One can estimate this required gate bias by using

$$V_b = \frac{U_N}{q} * \frac{C_{tot}}{C_{gate}}. \quad (6\text{-}6)$$

While one need only 0.490 V and 0.288 V to charge the devices with 1.3 nm and 1.8 nm NPs, respectively, a gate bias as large as 4.072 V is needed to charge the 0.5 nm NP samples. Thus, devices with larger embedded Pt NPs can be charged and discharged more efficiently under dual gate bias sweeping, resulting in an increase in the memory window (1.84 V and 2.71 V for 1.3 nm and 1.8 nm Pt NPs, respectively).

The interparticle coupling can also play an important role in the NP specific charging behavior. The main effect is defined as a tunneling matrix element (t) between equivalent single-particle states in nearest-neighboring NPs which is given by [41]

$$t \approx \frac{\hbar^2}{m^* d^2} \quad (6\text{-}7)$$

where d is the average interparticle distance and m^* is the effective electron mass of Pt. For interparticle distance of 7.15 ± 1.11, 2.35 ± 0.35 and 1.95 ± 0.73 nm, t is estimated to be

1.49 ± 0.42, 13.78 ± 0.13, 19.98 ± 0.26 meV, respectively. Since the charging energies due to interparticle coupling for 0.5 and 1.3 nm Pt NPs samples are relatively small compared to the average electron addition energy (1.49 meV vs. 1993 meV and 13.78 meV vs. 231 meV), the leakage current due to lateral tunneling should be lower for smaller size NP samples in this case. The average interparticle coupling for the 1.8 nm Pt NP samples is more comparable to the average electron addition energy (19.98 meV vs. 133 meV), which is a sign of poorer charge retention due to lateral tunneling than samples with smaller size NPs. Part of the charges in the conduction channel may be dissipated by first tunneling onto the NPs then through the lateral tunneling matrix, which can presumably be the reason of the lower on/off current ratio for the larger NP samples. The above discussed pentacene NVM device characteristics without and with embedded Pt NPs are summarized in **Table 6-2**.

Table 6-2 Summary of pentacene NVM device memory characteristics without and with embedded Pt NPs

Pt NP diameter (nm)	**Control**	**0.5 ± 0.12**	**1.3 ± 0.32**	**1.8 ± 0.65**
Deposition time (s)	/	5	30	60
Mobility ($cm^2/V \cdot s$)	0.087 ± 0.015	0.046 ± 0.012	0.0384 ± 0.0017	0.0453 ± 0.021
Maximum memory window (V)	0.21 ± 0.08	0.61 ± 0.11	2.05 ± 0.13	2.92 ± 0.20
Effective charge density ($\times 10^{12}$ cm^{-2})	/	1.0 ± 0.3	4.6 ± 0.3	6.82 ± 0.5
Pt NP density ($\times 10^{12}$ cm^{-2})	/	1.7 ± 0.5	7.5 ± 0.2	7.1 ± 0.3
Inter-NP distance (nm)	/	7.15 ± 1.11	2.35 ± 0.35	1.95 ± 0.73
# of charges per Pt NP	/	0.58	0.62	0.96
Total capacitance (aF)	/	0.426	1.151	1.634
Coulomb charging energy (eV)	/	0.376	0.139	0.098
Quantum confinement energy (eV)	/	1.618	0.092	0.035
Electron addition energy (eV)	/	1.993	0.231	0.133
Required charging voltage (V)	/	4.072	0.490	0.288

Chapter 7. Pentacene OFET-based Detector for Trace Vapor Explosive Detection

The pentacene NVM discussed in the previous chapter has also been studied for enhanced sensitivity towards trace nitroaromatic explosive vapors by embedding Pt NPs. Exploiting the unique electronic properties of Pt NPs, a detection limit of 56.6 parts per billion of 2,4-dinitrotoluene (DNT) vapor was demonstrated while control samples without any embedded NPs showed no observable sensitivity to DNT vapor. We attribute this remarkable enhancement in sensitivity to the ability of these NPs to function as discrete nodes, participating in charge transfer with adsorbed nitroaromatic molecules.

7.1 Introduction

Electronic sensors based on organic semiconducting polymers are rapidly gaining prominence due to the sheer number of organic semiconductor polymer choices and the ability to chemically functionalize them for specific applications. Despite the promise of organic field-effect transistors (OFET) as vapor phase sensors, their applicability towards sensing of explosive vapors is not well established. The typical saturation vapor concentration of 2,4,6-trinitrotoluene (TNT), pentaerythritol tetranitrate (PETN) and cyclotrimethylene-trinitramine (RDX) at standard atmospheric pressure and ambient temperature (297 K) are reported to be 6.2 parts per billion (ppb), 12.4 parts per trillion (ppt), and 3.65 ppt, respectively[103]. Whereas state-of-the art transistor-based sensors are reported to have detection limits in the ppb to ppm (parts per million) range [104]–[106]. Thus, this necessitates a fundamental reengineering of the transistor architectures to

improve their sensitivities while providing potential fingerprinting capabilities.

Platinum (Pt) nanoparticles (NPs) have attracted great interest in many fields due to their unique electrical and physical-chemical properties [1]–[4]. Because of their excellent chemical stability and catalytic properties, Pt NPs have been the preferred materials for integration into electronic and electrochemical device architectures to function as discrete charge storage or catalysts [4], [7]–[9]. We have developed a tilted target sputtering process for achieving sub-2 nm Pt NPs with controlled sizes and density as well as narrow distributions of metal NPs [1], [2], [4], [7], [20], [22]. These sub-2 nm Pt NPs have been utilized in silicon [1] or GaAs -based single-layer [20] and multi-layer[7] non-volatile memory devices, dye-sensitized solar cells [4] as well as room temperature single-electron tunneling devices [2]. In these studies, we have demonstrated their utility as discrete charge storage nodes, their ultra-small sizes affording us the capability to control (and observe) charge storage and transfer down to the single electron levels at ambient temperature (27 ^{o}C) [1], [7], [20].

This dissertation shows that the incorporation of Pt NPs into organic semiconducting polymer-based FET structures can have a dramatic effect on the overall sensitivity of otherwise insensitive OFET sensors to 2,4-dinitrotoluene (DNT) vapor. We adopted pentacene as the model semiconductor material in these studies as it showed no inherent sensitivity to DNT. DNT was chosen as the model analyte for the following reasons [107]: 1) DNT is structurally similar to TNT, sharing most of its electronic properties (strong electron accepting nature), 2) it is relatively safer to handle in a laboratory setting, and 3) it is often produced as a by-product of TNT degradation.

Most reported studies pertaining to OFET-based sensing of explosive vapors rely

on the intrinsic sensitivity of the polymer's electronic properties upon adsorption of the (explosive) analyte molecules. Here, we rely on the synergism between the embedded sub-2 nm Pt NPs and the organic polymer layer for improved performance of the device. Our sensor derives its response from the intrinsic electron-withdrawing nature of the DNT molecules [104] and the manner in which the DNT molecules interact with the semiconducting polymer as well as the embedded Pt NPs of the transistor devices. By real-time monitoring of multiple OFET parameters such as the drain current, change of mobility and hysteresis window, high sensitivity to DNT vapor was observed for sensors with embedded Pt NPs compared to the control devices (sensors without Pt NPs).

7.2 Experiment

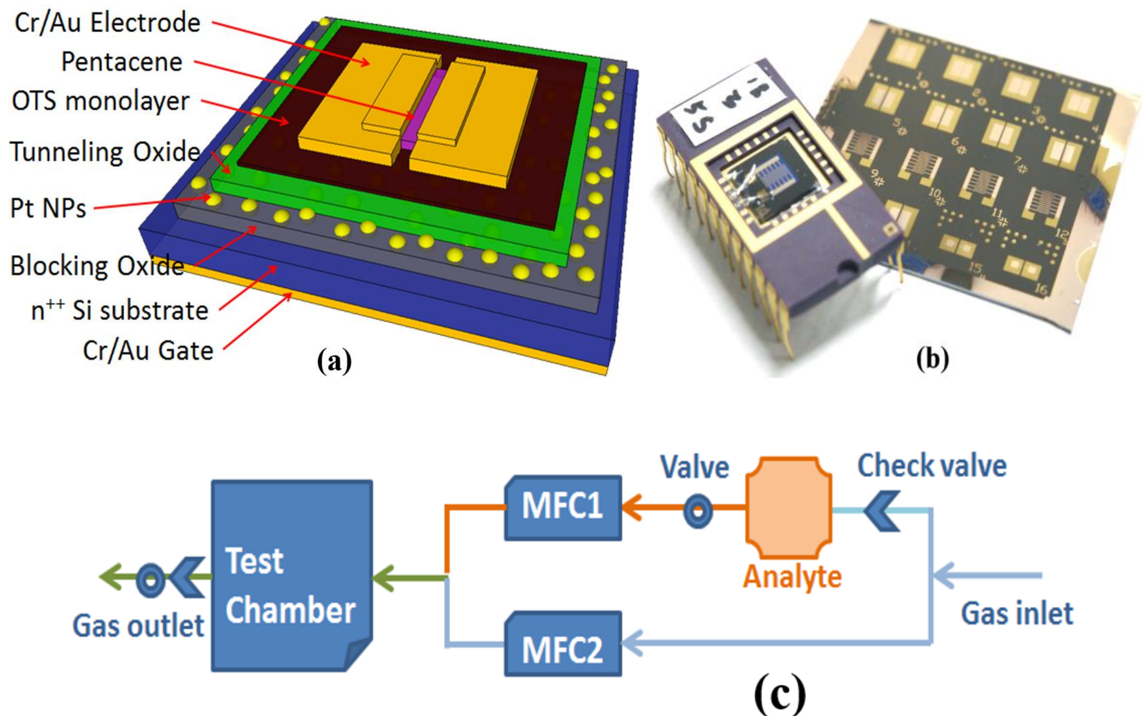
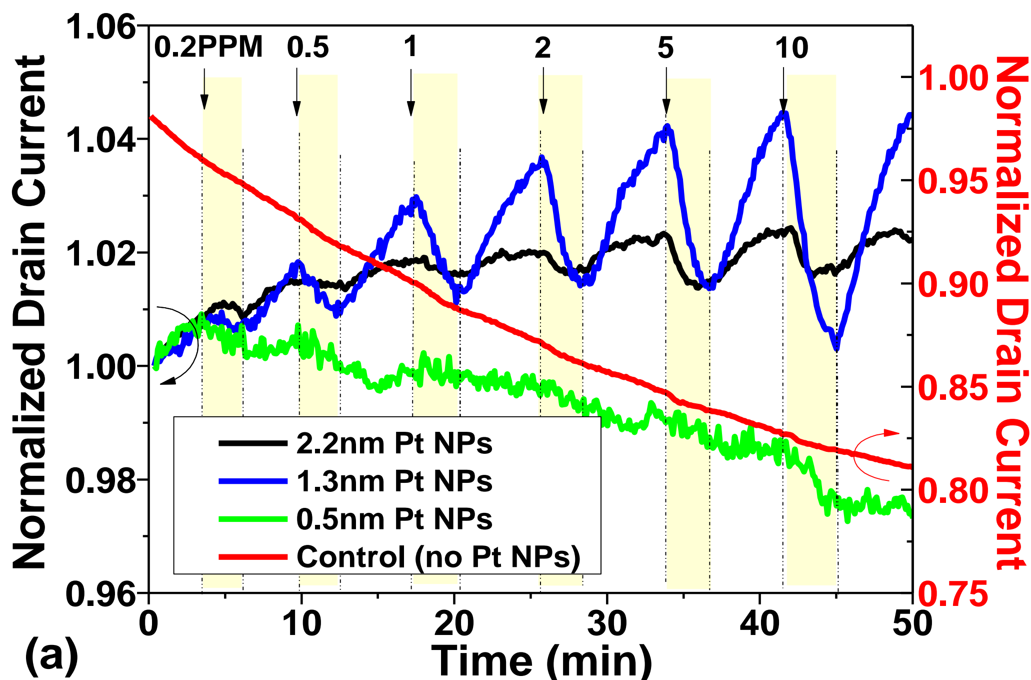


Figure 7-1 Pentacene-based OFET: (a) Schematic of device structure; (b) actual devices with different width length ratios and sensor within a dual-inline package for sensing; (c) schematics of analyte vapor generation and in situ vapor detection system.

Figure 7-1 (a) illustrates our pentacene OFET-based sensor architecture. Here, heavily doped silicon wafers were employed as the sensor substrate with bottom gate electrodes. After organic cleaning and subsequent drying with a stream of nitrogen gas, 20 nm of Al_2O_3 were grown by atomic layer deposition (ALD) [108] to function as the blocking layer. Samples were transferred into the sputtering chamber followed by Pt NPs deposition. Details of the NPs formation and the effect of various processing parameters on the size and number density of the deposited NPs have been discussed in our previous work [1]–[4], [7], [20], [109]. The average size of these NPs can be tuned simply by varying the deposition time. In this paper, sensors without any embedded NPs within the device architecture were used as control samples (referred to as "control"). Sensors embedded with NP sizes of 0.52 ± 0.12 nm, 1.30 ± 0.31 and ~1.8 nm (Referred to as "0.5 nm," "1.3 nm" or "1.8 nm" samples), with NP densities of $1.7 \times 10^{12}/\mathrm{cm}^2$, $7.5 \times 10^{12}/\mathrm{cm}^2$ and $7.6 \times 10^{12}/\mathrm{cm}^2$, respectively, were fabricated and tested. Following the deposition of Pt NPs, a tunneling layer of Al_2O_3 was grown by ALD covering the NPs. For samples with 1.3 nm and 1.8 nm Pt NPs, 3.2 nm of Al_2O_3 was chosen as the tunneling layer thickness. Due to the strong Coulomb blockade effect associated with the 0.5 nm Pt NPs[1], [2], [7], a thickness of 2.5 ± 0.13 nm of Al_2O_3 was chosen as the tunneling layer to facilitate charge transfer. Self-assembled monolayer of octadecyl-trichloro-silane (OTS) was formed on top of this Al_2O_3 tunneling layer to improve the surface for subsequent growth of pentacene [110]. The pentacene film was deposited through thermal evaporation (Kurt Lesker ATC 2000 V) at 80 °C with a deposition rate of 0.2 Å/s. Finally, 80 nm of Au source and drain electrodes were deposited using a thermal evaporator with the substrate maintained at room temperature. Both pentacene and Au films were patterned using specially designed shadow

masks. The schematics of the device structure and final packaged sensor are shown in **Figure 7-1** (a) and (b). Inter-digitated electrodes with channel length (L) of 180 μm and width (W) of 18.7 mm were used for this study.

Transistors were characterized using a Keithley 4200SCS semiconductor characterization system under dark conditions and with nitrogen gas flowing through the chamber in a probe station (Model: Signatone WL-210E). A custom-built vapor-generation and real-time measurement system (**Figure 7-1** (c)) was used for the evaluation of sensor performance. For sensing measurements, the packaged sensors were housed in an airtight, custom built stainless steel enclosed chamber equipped with inlet/outlet ports to allow for external electrical connections and for the flow of test gases. 0.5 g of the DNT solid was placed in an enclosed chamber and allowed to equilibrate until a saturated vapor of the compound was established within the chamber. Dilution of this vapor was then performed by means of a carrier gas to the required concentration by adjusting the flow rate of the carrier gases (using two mass flow controllers (MFC), MFC1 and MFC2), which flowed across the sensor surface. The current-voltage (I-V) curves were obtained in real time, measured in the accumulation mode. Multiple parameters like drain current, threshold voltage, mobility, and hysteresis window were monitored *in situ* as a function of concentration and time. All the characterizations were performed under dark conditions. (Supporting information has the detailed transistor characteristics [108].)



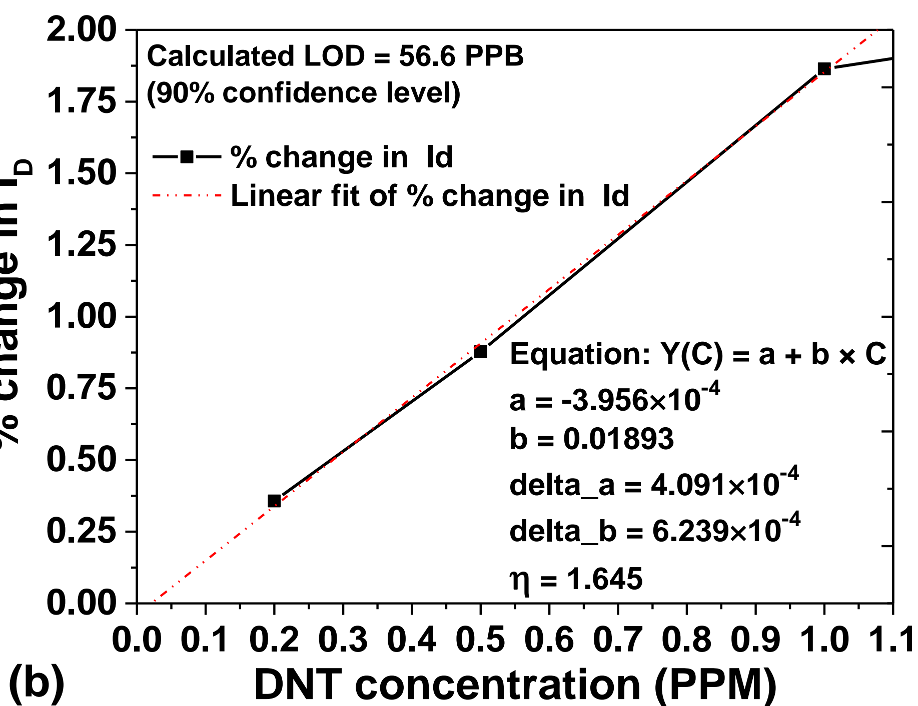


Figure 7-2 (a) Comparison of sensor response to various concentrations of DNT sensors with different sizes of Pt NPs (0.5, 1.3 and 1.8 nm diameters). The exposure time for DNT and dry air are about 3 min and 5 min separately. The output signal in y-axis is calculated by Id/Id_0, where Id is the drain current measured under -2.5 V of gate voltage and -2.5 V drain voltage. Id_0 is the initial value of the drain current. (b) Percentage change in drain current versus DNT concentration retrieved from the data set of sample with embedded 1.3 nm Pt NPs of **Figure 7-2** (a).

For the sensing measurements, the sensors were first exposed to a steady stream of dry air for 10 minutes to establish the baseline prior to DNT exposure. The samples were exposed to different concentrations of DNT for controlled time periods followed by exposure to dry air to refresh the sensor to its original state. The sampling interval (time interval between adjacent data points) was set at seven seconds. The drain current was continuously monitored during each exposure. **Figure 7-2** (a) shows the drain current response of the control sample (without Pt NPs) versus different size Pt NP embedded sensors to various concentrations of the DNT vapor. A constant drift in the drain current was observed for both devices albeit in opposite directions. For the control sample, such behavior is typical and is attributed to the degradation of pentacene under stress bias resulting in the reduction of drain current [111]. The origin for the positive drift in drain current for the Pt NP embedded sample warrants further study. It is evident from **Figure 7-2** (a) that no measurable change in drain current was observed when exposing the control sample to a DNT vapor. A remarkable enhancement in sensitivity for the Pt NPs embedded samples is readily apparent from the plot. The response of a diffusion limited sensor is often defined by a few regions of interest: a concentration region below which there is no distinguishable response, a linear response region (0.2 to 1 ppm in this case), and a non-linear super-saturated region (> 1 ppm in this case) [108]. **Figure 7-2** (b) shows the linear relation of percentage change in drain current versus DNT concentration retrieved from the data set of the sample with embedded 1.3 nm Pt NPs of **Figure 7-2** (a). The limit of detection (LOD) is calculated to be 56.6 ppb, which is determined by

$$Y_{LOD} = \frac{-a\times b+\sqrt{a^2\times b^2-(b^2-\eta^2\times\Delta b^2)(a^2-\eta^2\times\Delta a^2)}}{b^2-\eta^2\times\Delta b^2} \tag{7-1}$$

where $a, b, \triangle a, \triangle b$ are the parameters extracted from the linear fit of **Figure 7-2** (b). For a 90% confidence level, $\eta = 1.645$ is used [108].

7.3 Discussion

The observed responses may be explained by taking into consideration the various ways DNT molecules can interact with the organic semiconducting polymer and the embedded Pt NPs thereby affecting the overall transistor characteristics. The evoked responses are attributed to the combination of DNT induced effects and are summarized as: 1) doping effect [104], [112], 2) dipole effect [104], [112], and 3) charge transfer effect between Pt NPs and DNT molecules: Doping Effects: The electron withdrawing nature of the nitro groups leads to a hole-doping effect when absorbed into the polymer layer. This effect is manifested in positive threshold voltage shifts and increased drain current for the OFET device[113], [114]. Dipole Effect: Molecules with large associated dipole moments such as DNT (4.4 debye [104]) are known to induce strong localized electric fields within the semiconductor polymer. Localization of these molecules close to the conduction channel can influence the charge transport within the conduction channel by trapping or slowing down the charge carriers, reducing the field effect mobility and saturation drain current, and shifting the threshold voltage. These DNT dipoles will reorient, trap or release carriers depending on the bias direction of the dual gate bias sweeping measurement resulting in a change of hysteresis window in the transfer characteristics. Pt NPs enhanced dipole effect and their charge transfer between explosive molecules: Many unique properties of metal nanoparticles with size comparable to 1 nm are originated from their size-dependent electron affinity, ionization energy, band gap and density of states [10]. For

Pt NPs with different numbers of atoms, the electron affinity (EA) could be engineered from 1.5 eV for a single atom to 5.6 eV for the bulk material [115]. Thus, the NP size having the best energy level alignment with that of the DNT molecule (EA of 3.5 eV [116]) facilitates efficient electron transfer between the two. When the explosive molecules are localized close to the NPs, the electron energy difference between the two materials can lead to charge transfer between them through the tunneling Al_2O_3 layer. This charge transfer between Pt NPs and DNT molecules (DNT molecules having the tendency to withdraw electrons from the NP) will positively charge the Pt NPs, thereby producing a negative shift of threshold voltage as well as a reduction in the drain current. With the aid of these interactions, the localized DNT dipoles are also expected to change the hysteresis behavior of the transfer characteristics and show an enhanced dipole effect when compared to devices without Pt NPs.

The devices' overall sensitivity to explosive vapors is determined by the combination of all of these effects. The contradictory nature of the doping and the dipole effect has the potential to lower the sensitivity of the devices, especially for the control samples. Due to the fact that no measurable response was observed for sensors without embedded NPs (**Figure 7-2** (a)), it can be concluded that doping and/or the dipole effect (without the aid of Pt NPs) plays a relatively insignificant role here. We attribute the dominant sensing mechanism for the senor with embedded Pt NPs to be the charge transfer effect between analyte molecules and Pt NPs. Assuming that the deposited particles are spherical with a mean observed diameter of d, the number of Pt atoms N present in a given particle can be estimated by

$$N = f\left(\frac{V_{particle}}{V_{Pt_{atom}}}\right) = f\left(\frac{d}{2\times r}\right)^3 \qquad (7\text{-}2)$$

where r is the atomic radius which is 0.139 nm for platinum, and ƒ is the "packing fraction" which equals to 0.74 for face centered cubic (FCC) structures [4]. Note that the calculated number of atoms might be a slight overestimation since the packing fraction for non-crystalline NPs would be less than 0.74. The numbers of atoms are then calculated to be about 7, 78, and 206 for "0.5 nm", "1.3 nm", and "1.8 nm" size of Pt NPs, respectively. **Figure 7-3** shows the schematics of an energy band diagram of the Pt NPs with Al_2O_3 tunneling layer with an energy band of DNT to understand the charge transfer process between the Pt NPs and DNT molecules. Nie et al. studied the relation between multiple electronic properties and size of the Pt NPs by molecular orbital simulation using the Vienna ab initio simulation package (VASP) [115]. It was found that the electron affinity (EA) for 0.5 nm NPs containing approximately 7 atoms was expected to be about 3 eV [115]. In the case of 1.8 nm Pt NPs, containing ~206 atoms, the EA is close to the bulk Pt value (5.3 eV) [10]. For NPs with size in between 0.5 nm and 1.8 nm, such as 1.3 nm Pt NPs (~78 atoms), the EA value lies in between 3 and 5.3 eV.

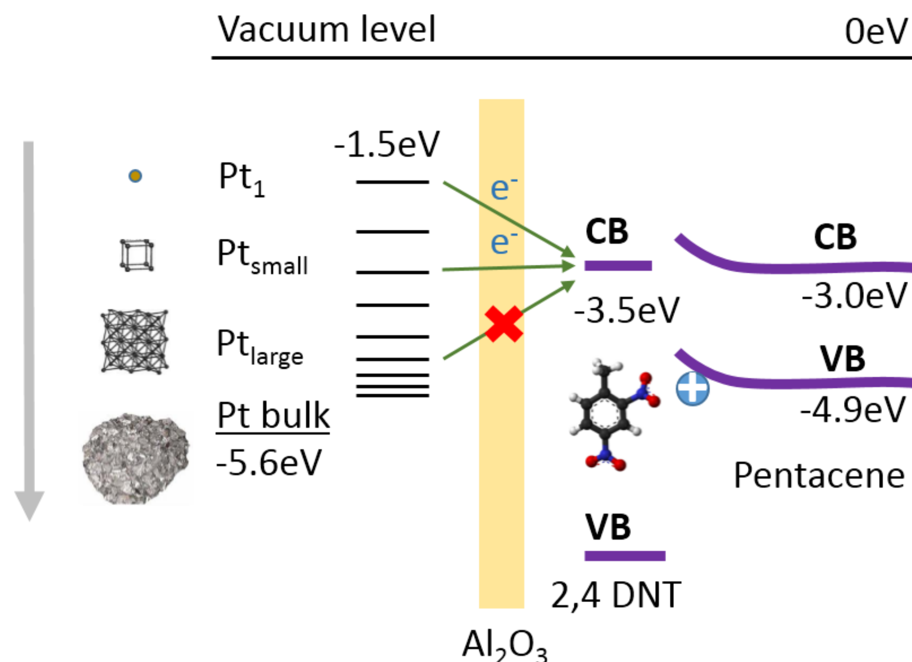


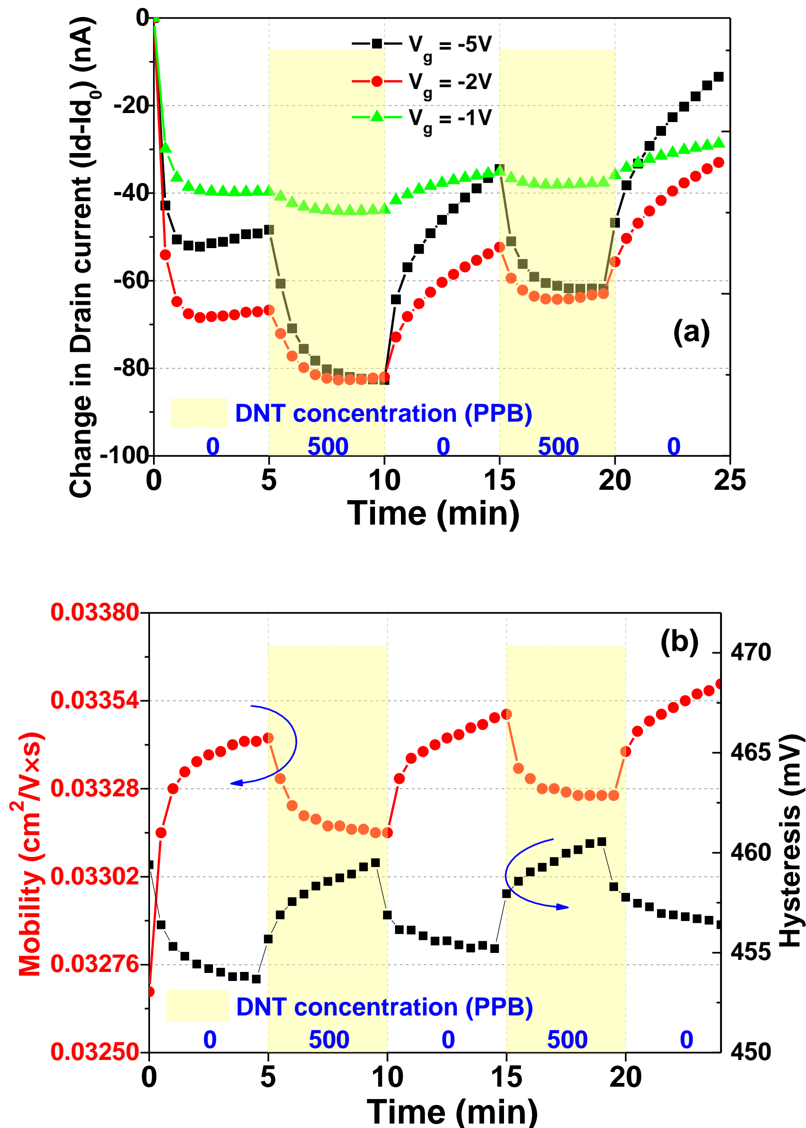
Figure 7-3 Schematics of energy band diagram of device with different sizes of Pt NPs under zero gate bias. (EA of Pt NPs with different sizes were adopted from [115]; EA of DNT is adopted from [116])

Table 7-1 Summary of Platinum NPs properties with different sizes

Diameter (nm)	**0.52±0.12**	**1.30±0.31**	**~1.8**
NPs Density (10^{12} /cm^2)	1.7	7.5	7.6
Number of Atoms	~7	~78	~206
EA (eV) [115]	~3	/	~5.3
Coulomb Charging Energy(meV)[2]	291.7	110.7	76.6

The sensor with embedded 1.3 nm Pt NPs showed the best sensitivity towards DNT vapor whereas the sensor with embedded 0.5 nm Pt NPs showed the least. One possible reason for the reduced sensitivity of the device with 0.5 nm Pt NPs compared to 1.3 nm Pt NPs could be due to the higher Coulomb charging energy (292 meV) of 0.5 nm Pt NPs than that of the 1.3 nm NPs (111 meV) [2]. Also, the NPs density of 0.5 nm NPs (1.8×10^{12} cm^{-2}) is much lower than that of 1.3 nm NPs (7.5×10^{12} cm^{-2}). For 1.8 nm

particle with an EA similar to the bulk Pt, a large mismatch of electron affinity of Pt with respect to that of DNT reduces the probability of electron transfer significantly, giving rise to a poorer sensor response. **Table 7-1** summarizes the electronic properties of Pt NPs with different sizes used in this study. Taking into account all of the above factors, sensors with embedded 1.3 nm Pt NPs with the best matched electron affinity with respect to DNT and high-particle density produced the best response. Further optimization of the type and size of metal NPs and the thickness of tunneling oxide is expected to improve sensor performance.



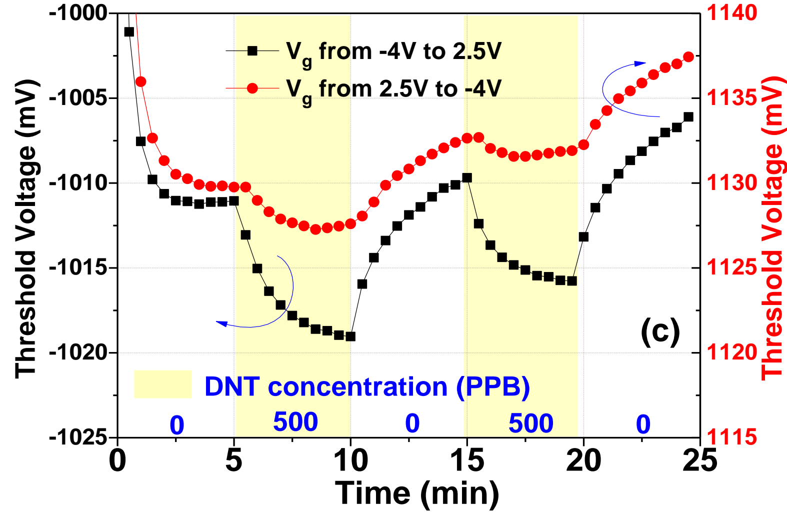


Figure 7-4 Sensor response to 500 ppb of 2,4-dinitrotoluene for sensors with embedded 1.3 nm Pt NPs: (a) Comparison of change in drain current under different gate voltages (-5, -2, and -1 V); (b) change in mobility (left y-axis) and change in hysteresis (right y-axis); (c) change of threshold voltage under different sweeping direction of gate bias at drain voltage of -2.5 V. (Refer [15] for the mobility and hysteresis determination).

To illustrate how the above mechanisms influence the multiple transistor parameters during DNT exposure, another measurement was carried out by exposing the sensor with embedded 1.3 nm Pt NPs to 500 ppb of DNT. **Figure 7-4** (a) compares the change of drain current under different gate voltages upon exposure to DNT. About 10 times and 4 times of amplification in the response was observed for -5 V and -2 V gate voltages respectively, compared to the amplification at -1 V gate voltage. These observations are in accordance with Huang's analysis [112] which states that

$$\Delta I_{sat} = \frac{W}{2L} \times C \times (\mu_{sat} + \Delta\mu) \times \left[V_g - (V_t + \Delta V_t)\right]^2 \tag{7-3}$$

where $\frac{W}{L}$ is the channel width/length ratio, C is the capacitance density, μ_{sat} and $\Delta\mu$ are the mobility and its change when exposed to DNT, V_t and ΔV_t are the threshold voltage and its change, and V_g is the applied gate voltage. As shown in **Figure 7-4** (b) and (c), decreases

in field effect mobility and negative shift in the threshold voltage for the gate voltage sweeping in forward and reverse directions were observed which could be attributed to the enhanced dipole effect due to the localization of the DNT molecules in the conduction channel when interacting with the Pt NPs. The change in threshold voltage from forward and reverse gate voltage sweeping resulted in a change in the hysteresis window (see **Figure 7-4** (b) and (c)), which is a direct evidence of charge transfer between the DNT and the Pt NPs. Thus, all these parameters (e.g. the drain current, on/off current ratio, mobility, threshold voltage, hysteresis window, and sub-threshold swing) can be used as sensor outputs for a more quantitative analysis of the exposure event and possibly to discriminate between different analytes.

In conclusion, we have demonstrated remarkable improvement in sensitivity (many orders of magnitude improvement) of semiconducting polymers towards nitroaromatic explosive vapors through the incorporation of high density, sub-2 nm Pt NPs. A detection limit of 56.6 ppb of DNT vapor was observed, while the control sample without any embedded NPs showed no observable sensitivity to DNT vapor. NPs have been found to play a prominent role in their interaction with vapor phase DNT molecules and the ensuing charge transfer processes are significantly modulating the overall response of the field effect transistor device. Remarkably, control samples did not elicit any observable response even when exposed to DNT concentrations as large as 10 ppm.

It is important to note that the choice of semiconducting polymers in such a trace vapor detection system plays an important role in determining the sensitivity of the device to nitroaromatic vapor. While polymers like poly-3-hexylthiophene (P3HT) have been shown to be intrinsically sensitive to nitroaromatic vapors, there is a dearth of literature on

the use of pentacene polymer for electronic nose applications, possibly due to its low observed sensitivity to the vapor. Under these circumstances, it is noteworthy that with the integration of Pt NPs, we have demonstrated a remarkable boost in sensitivity of the device to DNT vapor. We believe that by incorporating this structure to the device with more sensitive organic materials than pentacene, the detection limit can be further improved.

Chapter 8. Vapor Phase Molecular Imprinting on Pentacene OFET based Vapor Detector

To improve the selective detection capability of the pentacene FET-based sensor discussed in the previous chapter, a vapor phase molecular imprinted polymer (MIP) technique was developed and is presented in this chapter. This OFET-based sensor using pentacene as the molecularly imprinted monomer showed enhanced selectivity to 2, 4-dinitrotoluene (DNT) vapor against various interfering analytes. This method can be extended to improve the selectivity of most OFET- and chem-resistor-based sensors without adversely affecting the device's electronic properties, which is promising for the development of highly selective, low-cost, flexible OFET sensors.

8.1 Introduction

Organic semiconducting material-based sensors are rapidly gaining prominence due to the myriad of chemical functionalities available for enhancing the transduction of physical/chemical signal-to-sensor electric signals. The increased interest in organic field-effect transistors (OFETs) over simple chem-resistor configurations for vapor explosive detection is due to the amplifying properties of a field-effect device and the fact that multiple parameters—threshold voltage, hysteresis window, subthreshold swing and mobility—of the OFETs may be probed to gain information about the explosive vapor interactions with the sensing material [13], [112]. Different approaches, such as morphology engineering, polymer functionalization, and metal nanoparticle assisted

charge interactions have been explored so far with the goal of improving sensitivity of these OFET sensors [13], [112], [117]. The ability to give these sensors molecular recognition capability on a single sensor basis still remains largely unexplored, although preliminary accounts of polymer functionalization to improve recognition capability have been reported [112]. OFET sensor array systems consisting of different organic materials have also proven to show fingerprint response to different types of analyte vapors [118]. These systems are usually bulky, expensive, and not very straightforward from an operational standpoint. In this paper, we demonstrate a novel vapor phase molecularly imprinting (MIP) method for improving the trace vapor detection selectivity of a single pentacene OFET-based sensor.

MIP-based techniques adapted from analyte-selective chromatographic separations [119] hold great promise for sensing applications. The imprinting process is typically performed in the solution phase using the target analyte as a template. A combination of appropriately chosen functional monomers and crosslinking monomers are also used where the functional monomers interact and bind to the target analyte (covalently or through non-covalent interactions), and the crosslinking monomers polymerize around the formed complexes [120], [121]. Subsequent extraction of the template molecules from the cross-linked network results in a polymer with imprinted cavities that are complementary in shape and functionality to the target analyte, leaving the polymer with molecular recognition capability. Translating this technique to impart molecular recognition to organic semiconducting materials without degrading the core electronic properties of an OFET-based sensor is challenging because these fabricated devices are usually susceptible to solvent damage during the templating process. Alternate techniques that minimize

damage to the organic semiconducting materials are greatly needed. In this work, we report a vapor phase MIP technique suitable for an organic semiconducting layer in an OFET-based sensor, enhancing the sensor selectivity towards DNT vapor over other analytes, without significantly degrading the organic layer.

8.2 Experiment

8.2.1 Organic field-effect-transistor fabrication

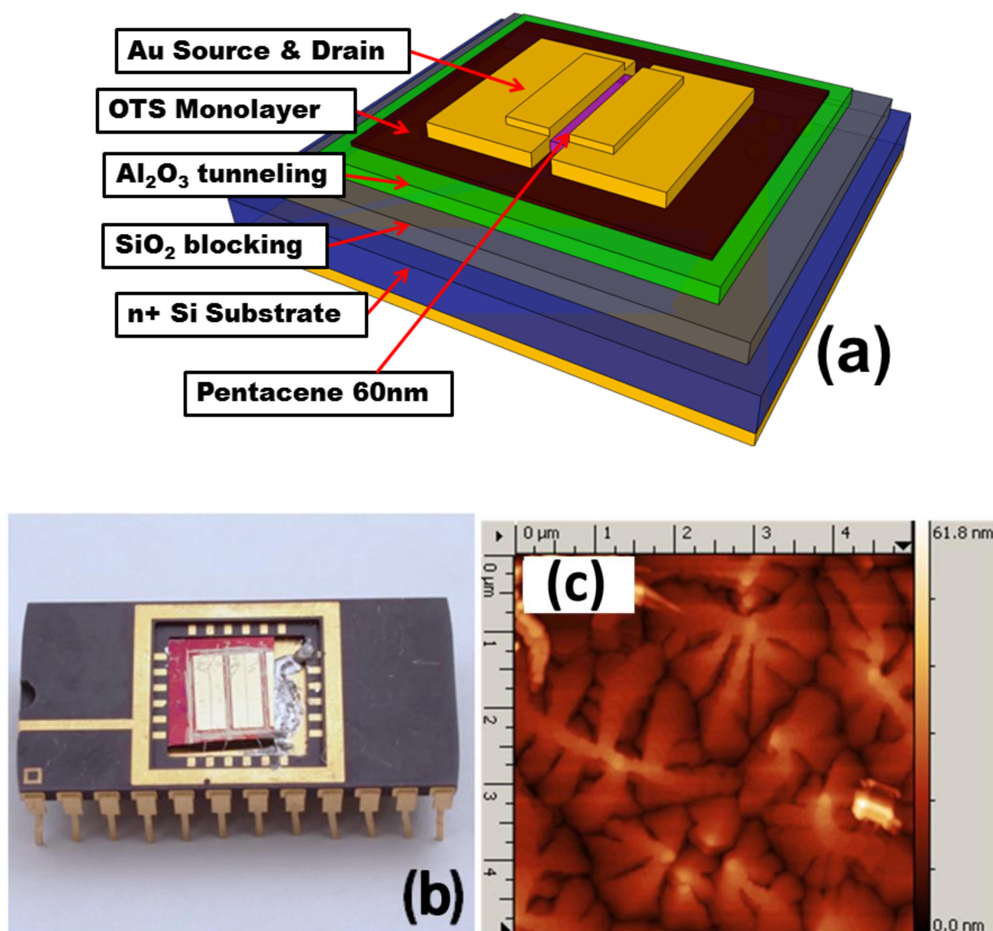


Figure 8-1 Schematic of pentacene-based OFET: (a) device configuration; (b) device-in-sensor package; and (c) AFM scan of OTS-treated surface (5×5 µm area) showing grain morphology of the pentacene layer.

Figure 8-1 (a) and (b) illustrates our pentacene OFET-based sensor architecture and packaging. The bottom gate electrode is a heavily-doped silicon wafer with 200 nm SiO_2 capping. After subsequent sonication in acetone, methanol and deionized water followed by drying with streaming N_2 gas, atomic layer deposition was used to synthesize 3 nm of Al_2O_3. The substrate was exposed to 30 minutes of H_2 annealing at 250 °C in a 10^{-8} Torr vacuum system to improve the oxide quality. The Al_2O_3 surface was modified by low-power O_2 plasma and octadecyltrichlorosilane (OTS) treatment to form a low-energy–CH_3-terminated surface in order to facilitate efficient pentacene grain nucleation. A 60 nm pentacene layer was deposited by thermal evaporation at a deposition rate 0.2Å/s. The substrate temperature was held at 80 °C during the deposition. Pentacene grains were measured with AFM to be ~3 μm (**Figure 8-1** (c)). Finally, 80 nm Au was deposited atop through a shadow mask to form the source and drain electrodes.

8.2.2 Molecular imprinting method

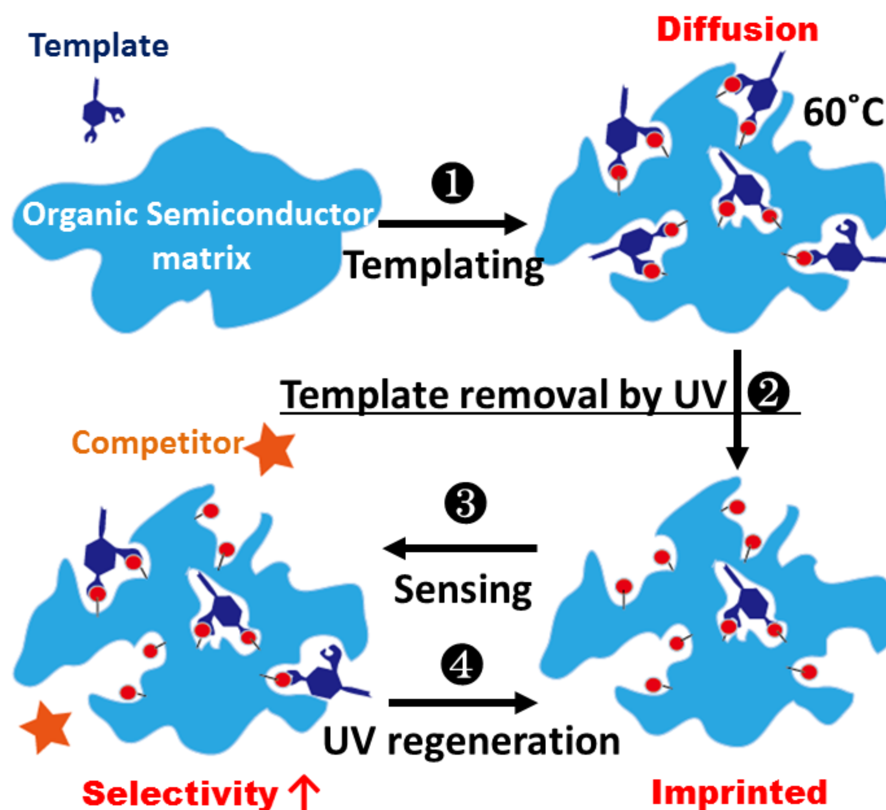


Figure 8-2 Illustration of vapor phase molecular imprinting of organic semiconductor. Red dots indicate exposed target-selective functional groups within the imprinted polymer.

After device fabrication, vapor phase molecular imprinting was performed on the pentacene layer (**Figure 8-2**). The fabricated OFET was placed in a test chamber at 60 °C with saturated vapor of the chemical template species (DNT in this case). This temperature was chosen since it allows relatively high diffusion rates within pentacene, but it is still safely below the sublimation temperature of pentacene (~100 °C [122]). The increased molecule mobility at this temperature allows for pentacene reorganization around the adsorbed template molecules, which is similar to the solution-phase molecular imprinting processes. The devices are then cooled to room temperature in saturated vapor, thereby

trapping the template molecules within the reorganized pentacene layer. Template extraction is then performed through brief UV exposure that degrades the template molecules, leaving behind molecular imprints within the pentacene.

8.2.3 Measurement system

Figure 8-3 shows the in-situ measurement system used for sensor performance evaluation. The sensors were placed in a home-built test chamber and connected to a Keitheley 4200 SCS system for sensor current-voltage (I-V) characterization. 0.5 g of solid or 0.5 mL of a liquid analyte was placed in the analyte chamber to generate a saturated analyte vapor. A mass flow controller (MFC 1) was used to control the carrier gas flow rate passing through the analyte chamber, while another MFC (MFC 2) was used to control the dilution gas flow rate. A trace concentration of the target analyte is passed over the device in the test chamber by controlling the carrier gas flow ratio of MFC 1 and MFC 2. The carrier and dilution gas used in this study was dry N_2. For the in-situ sensing measurement, a 30 s sampling interval with ~1 s of measurement time was used.

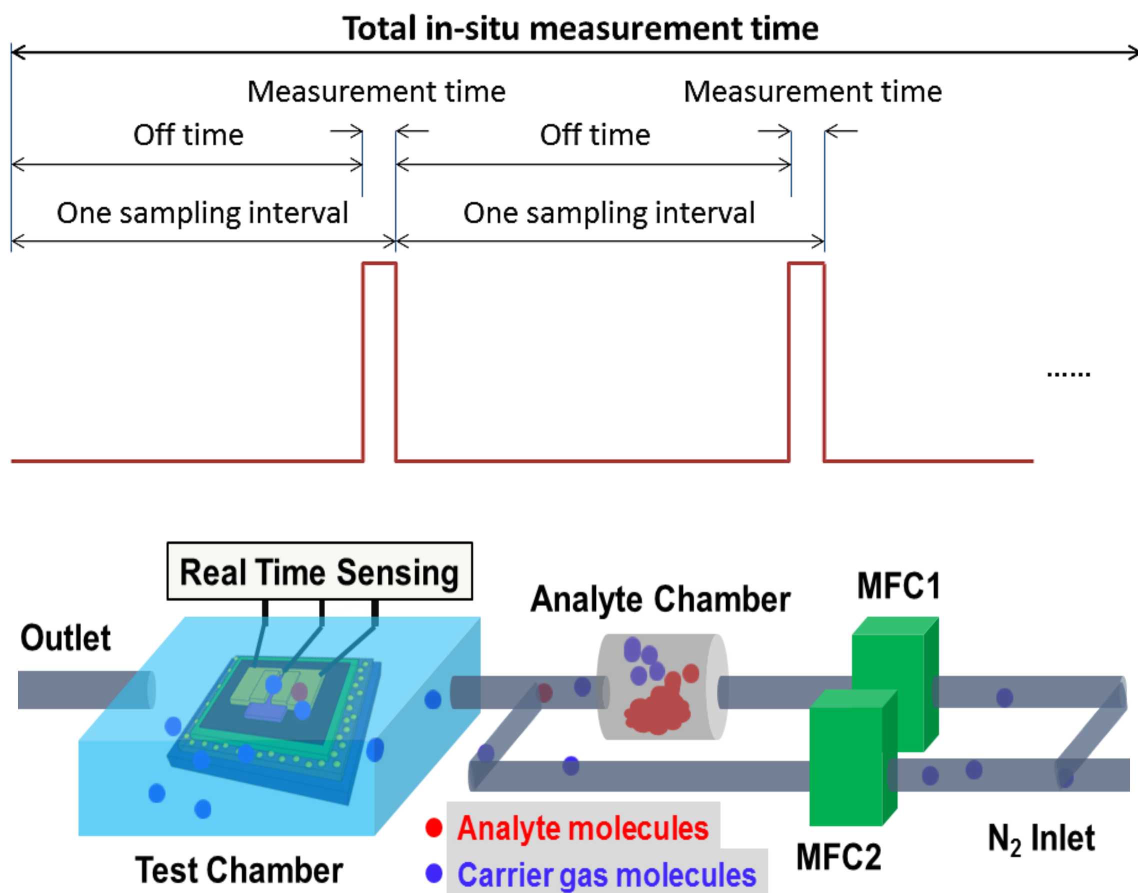


Figure 8-3 Experimental setup for sensor characterization and in-situ vapor detection.

8.3 Discussion

8.3.1 Transistor characteristics

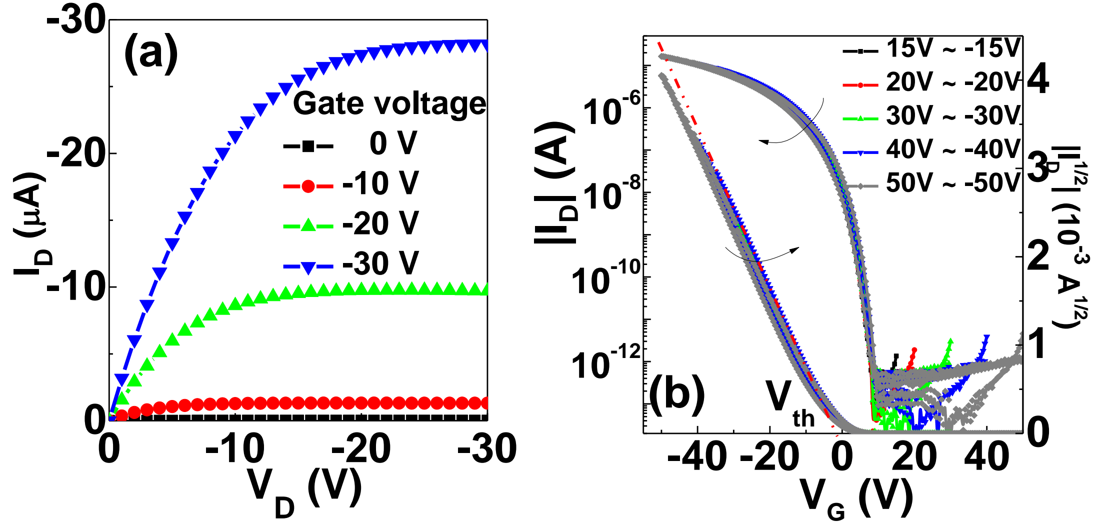


Figure 8-4 (a) Output characteristics and (b) transfer characteristics of pentacene-based OFET with 50:1 width: length ratio.

Device output and transfer characteristics are shown in **Figure 8-4** (a) and (b), respectively. The drain current through the conduction channel of the OFETs can be described by $I_D^{Sat} = \frac{W}{2L}\mu C_{OX}(V_G - V_{TH})^2$ for saturation mode and $I_D^{lin} = \frac{W}{L}\mu C_{OX}[(V_G - V_{TH})V_D - \frac{V_D^2}{2}]$ for linear mode, respectively, where μ is the field effect mobility; W, L are the channel width and length, C_{OX} is the gate capacitance per unit area, V_G, V_D and V_{TH} are the source-gate, source-drain and threshold voltage, respectively. The relatively high on-off ratio and small hysteresis indicates good transistor characteristics, which is promising for sensing applications. The threshold voltage, hysteresis, on/off ratio, and mobility and subthreshold swing of the pentacene OFETs will be calculated and used to characterize the device before and after the MIP process in the next section.

8.3.2 Change in transfer characteristics after molecular imprinting

Figure 8-5 shows the I_D-V_G plots indicative of the transfer characteristics of the pentacene-based FET after each step of the MIP process with DNT as the template. Significant changes in sensor threshold voltage and sub-threshold swing were observed. It is found that more than 2 h of 254 nm UV exposure is necessary for complete extraction of the DNT template molecules.

Table 8-1 summarizes changes in sensor parameters before and after the imprinting process.

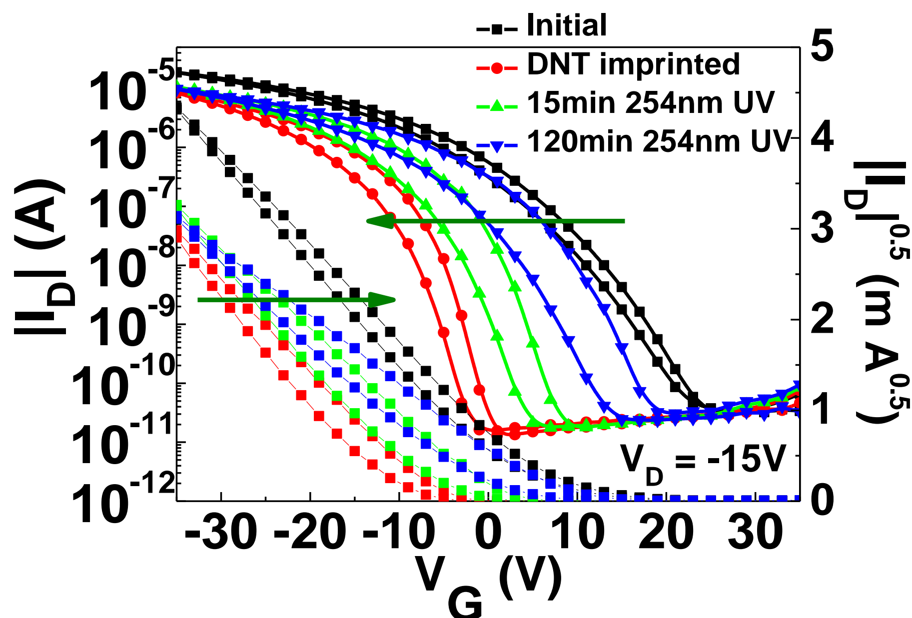


Figure 8-5 Changes in OFET transfer characteristics before and after DNT saturation and after 254 nm UV exposure for 15 min and 120 min.

The predominance of the dipole fields associated with the absorbed DNT molecules close to the conducting channel of the pentacene FET resulted in significant distortion of the electric field within the conduction channel [13], [112]. Thus, an additional potential is

required for the injected charges to overcome this field, effectively resulting in a negative threshold voltage shift for the device upon DNT saturation (see **Figure 8-5**). The threshold voltage returns close to its original value after UV exposure at 254 nm, indicating near-complete removal of the template molecules. A significant reduction in the sub-threshold swing (S) after DNT imprinting is also observed. The density of the pentacene-SiO_2 interface trap states (D_{it}) can be evaluated based on S using the relation [123] $D_{it} = \left(\frac{q}{kT} \cdot \frac{S}{ln10} - 1\right) \cdot \frac{C_i}{q^2} - \frac{C_{del}}{q^2}$ with C_{del} being the depletion capacitance of pentacene, and C_i being the capacitance of the gate dielectrics. With C_{del} and C_i not being changed significantly, a reduction in S indicates a suppression of D_{it}, which could be due to the binding of the DNT molecules with these interface trap states. A partial recovery of S after UV exposure indicates an increase in D_{it} and is indicative of partial extraction of the DNT template molecules from pentacene. Further, a hysteresis in current-voltage curves, as well as change in mobility (as manifested in the transfer characteristics of the device following the imprinting process) are indicative of charge traps created through removal of the template molecules. The device processed under the same condition without DNT imprinting showed negligible change in the transistor characteristics, indicating that changes in threshold voltage, mobility, hysteresis, and hole concentration during the templating process are due to incorporation and removal of the template molecules. This observation suggests a molecular imprinting approach can be developed to achieve fingerprint responses to chemical interactions within the organic semiconductor.

8.3.3 Selective detection of 2, 4-dinitrotoluene

The testing of imprinted devices was performed to evaluate the targeted sensing

characteristics of the imprinted devices towards DNT. OFET sensors were exposed to ~300 parts per billion (PPB) of the target DNT analyte and common interfering analytes (i.e., nitrobenzene/NB, dinitrobenzene/DNB, nicotine). Throughout the exposure, the OFETs drain current was recorded at constant gate and drain voltage. **Figure 8-6** shows the device response (% change in drain current) for imprinted pentacene OFET devices. The imprinted pentacene OFETs response indicates sensitivity to various concentrations of DNT vapor (~1% response to 30 PPB DNT) whereas devices without imprinting show no sensitivity (**Figure 8-6** (a)). We attribute this result to a combination of enhanced pentacene surface areas from cavities created during the imprinting process and improved DNT shape recognition of the imprinted pentacene. The large associated dipole moment of the DNT molecules linked to the molecular cavities created by the imprinting process leads to large induced electric fields in close vicinity to the molecules which are capable of trapping mobile charge carriers. The imprinting process also leads to decreased mobility, and reduced drain current [13], [112]. As evidenced in **Figure 8-6** (b) the imprinted pentacene-FET based detectors are highly selective towards DNT molecules over other nitro group-containing moieties such as dinitrobenzene (DNB), nitrobenzene (NB), and nicotine. Thus, our vapor phase molecular imprinting technique shows promise towards imparting molecular recognition capability to organic semiconducting materials and improving their sensitivity to target analytes. However, additional work needs to be done with regard to improving limit of detection and to further develop this technique to include other analytes of interest (*e.g.,* RDX, PETN).

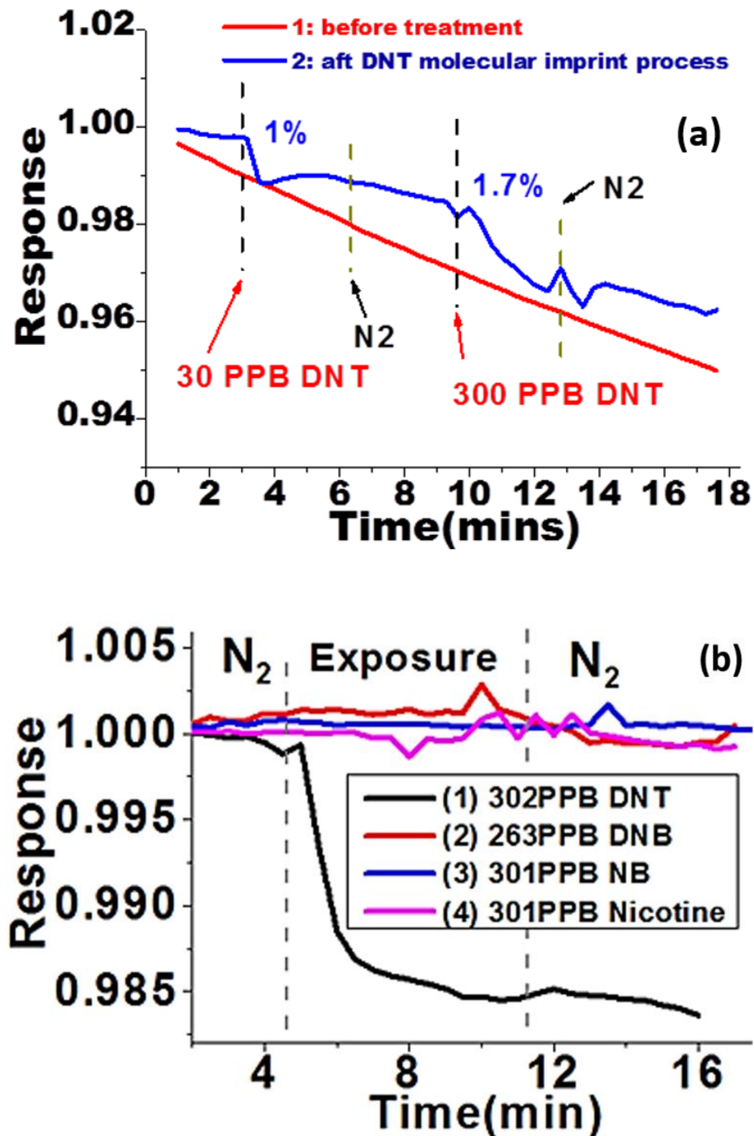


Figure 8-6 (a) Comparison of drain current response of the pentacene OFET sensor against various concentrations of DNT vapor before and after vapor phase MIP; (b) drain current response of the imprinted pentacene OFET sensor toward target and interfering analytes (black: 300 ppb DNT [target]; red: 260 ppb DNB; blue: 300 ppb NB, and pink: 300 ppb Nicotine).

Table 8-1 Changes of various OFET sensor parameters during molecular imprinting process.

	Initial	900 PPB DNT (60 ˚C)	254 nm UV exposure (2h)
Water Contact Angles (˚)	88.77 ± 0.31	95.01±0.56	89.73±0.40
Drain Current (10^{-5}A) (V_g = -15V, V_d = -15V)	1.860	0.843	0.968
Threshold Voltage(V)	7.06	-5.32	5.89
Mobility (cm^2/ V s)	0.0249	0.0224	0.0136
Sub-threshold Swing (V/dec)	4.821	1.671	3.543
Hysteresis (V)	4.68	6.03	7.53

8.4 Future Work

Future work includes applying this vapor phase MIP method for other analytes such as TNT and ammonium nitrate.

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LIST OF PUBLICATIONS

JOURNAL PUBLICATIONS

1. **H. Zheng**, B. K. Mahajan, S. C. Su, S. Mukherjee, K. Gangopadhyay, S. Gangopadhyay. "Barrier Modification of Metal-contact on Silicon by Sub-2 nm Platinum Nanoparticles and Thin Dielectrics" ***Scientific Reports***, vol. 6, p. 25234, Apr. 2016.

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6. **H. Zheng**, Y. Zhou, and S. Gangopadhyay. "Size-Dependent Work Function and Single Electron Memory Behavior of Pentacene Non-Volatile Memory with Embedded Sub-Nanometer Platinum Nanoparticles." ***Journal of Applied Physics***, vol. 117, no. 2, p. 024504, Jan. 14, 2015.

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CONFERENCE PROCEEDINGS

1. **H. Zheng,** and S. Gangopadhyay. “Molecularly Imprinted Organic Transistor Based Sensor for Selective Trace Chemical Vapor Detection.” In *18th International Conference on Sold-State Sensors, Actuators and Microsystems, Transducers*, 2015.

2. **H. Zheng**, S. Mukherjee, K. Gangopadhyay, and S. Gangopadhyay. “Effect of Sub 1-Nm Pt Nanoparticle on the Conduction Properties of Graphene Based Field Effect Transistor.” *ECS Trans., vol.* 61, 39:1–11, Oct. 1, 2014.

VITA

Haisheng Zheng was born in Zhuhai, China on Feb. 06. 1987. Haisheng received his B.S. degree in Electronic Science & Technology (Microelectronics) from South China University of Technology, Guangzhou, China. His studies focused on improving the OLED efficiency based on dendritic material for all-printed colorful OLED displays. In Aug. 2010, he enrolled in the graduate program of the Department of Electrical and Computer Engineering at the University of Missouri, Columbia and joined Dr. Shubhra Gangopadhyay' s research group as a graduate research assistant. During his Ph.D. study, he researched on exploring the charge storage properties of sub -2 nm metal nanoparticles and their applications as semiconductor devices with associated studies on field effect transistor memory, trace vapor molecules detector, neutron detector, Ohmic metal-semiconductor contact, and 2D material based devices. He received his Ph.D. degree in Electrical and Computer Engineering in July 2016.