NEXT-GENERATION FLASH MEMORIES USING TWO-DIMENSIONAL MATERIALS

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By
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ABSTRACT

This thesis presents a model that provides the output characteristics of next-generation flash memories using two-dimensional materials. Multi-Layer Graphene Nanoribbon (MLGNR) and Graphene are used as the channel and floating gate of the device proposed. The current in the channel is calculated using the Poisson-Schrodinger equation; the numerical algorithm is based on the Newton-Raphson (NR) method. A comparative study is done on two different Floating Gate Transistor (FGT) based on the proposed model. Silicon dioxide (SiO_2) and Hafnium dioxide (HfO_2) are the two oxides explored as the top control oxide of the device.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of School of Computing and Engineering have examined a thesis titled “Next-Generation Flash Memories Using Two-Dimensional Materials” presented by Hemanshu Shishupal, candidate for Master of Science degree, and certify that in their opinion it is worthy of acceptance.

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LIST OF SYMBOLS

N+	N-type semiconductor
P+	P-type semiconductor
S/D	Source/ Drain
F	Floating
ρ_{fix}	Fixed Charge
ε	Dielectric constant
N_D^+	Concentration of ionized donor
N_A^-	Concentration of ionized acceptor
ϕ	Electrostatic potential
$\hbar$	Planck's constant
m	Effective mass
Ψ	Eigenfunction
E	Eigenvalues
E_C	Conduction band edge
ε_0	Absolute permittivity
ε_r	Relative permittivity

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CHAPTER 1

INTRODUCTION

The Flash Memory technology has recently gained attention with the growing demand for the non-volatile memories for mobile electronic devices. Conventional flash memory technology composed of Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) structure with floating gate (FG) as the charge trapping/ storage medium. The basic working principle of floating gate flash memory cell is based on the threshold voltage variation because of the injected electrons in the floating gate/ charge storage medium. Higher data retention rate, minimal power consumption, high density and high endurance are the desired features of a flash memory device.

With the continuous scaling down of these devices, the floating gate technology faces serious problems such as lateral charge leakage into the drain and source regions, and complete charge loss because of pinholes and defects in tunnel layer. The charge trapping flash memory structures are proposed to overcome the drawbacks of scaled floating gate cells. In the charge trapping flash memories, charge storage medium comprises of electrically isolated traps. Nanoclusters in Si-nitride, semiconductor nanocrystals (Si, Ge, etc.) and metal nanocrystals (Co, Al, Au, Ni, Ag, etc.) are used as traps. Discrete charge storage nodes prevent lateral charge leakage and allow further scaling of the tunnel oxide. The use of distinct charge trapping medium offers high endurance, low power consumption and fast operation in high-density memory applications.

The leakage current increases exponentially as the gate oxide gets thinner which causes reliability problems in flash memories. Materials with high dielectric constant (high-k) are proposed as tunnel oxides and control oxides in flash memory technologies. The application of

high-k dielectrics, the leakage current is significantly reduced due to increased physical dielectric thickness. This high-k material improves the write/ erase speed without degrading the data retention performance. High-k dielectric flash drives with dense nanocrystals exhibit improved retention performance and faster operation.

This thesis investigates the charge storage property of the graphene in flash memory applications, and effect of multilayer graphene nanoribbon (MLGNR) used as charge storage layer/ floating gate on the memory performance. Our motivation is to improve the performance of the MLGNR flash memory technology with SiO_2 as the tunnel and control oxide and graphene as charge storage medium.

The thesis is organized as follows: Chapter 2 address the material characteristics used in the proposed device. Chapter 3 gives the detail device description. Chapter 4, explains detail flowchart for modeling the device in TCAD. Results for programming, erase and read are discussed in chapter 5. Chapter 6 concludes the thesis by summarizing the results and provides future work in this direction.

CHAPTER 2

GRAPHENE AND MULTI-LAYER GRAPHENE NANORIBBON

2.1 Graphene –

Researchers and scientists come up with new materials with the unique property that captivates the entire semiconductor industry. Graphene is one such material with unusual features such as ballistic electron transportation and half-integer quantum Hall effect [1]. This 2-D material is the parent of all graphitic carbon forms which is strictly expected to consist of a single layer.

Graphene a two-dimensional material constitutes a new Nano-carbon comprising layers of carbon atoms arranged in six-member rings. Its potential was most notably recognized when Novoselov and Geim won the 2010 Nobel prize in physics [2]. Graphene shows quantum Hall effect at room temperature, an ambipolar electric field effect with ballistic conduction of charge carriers, tunable band gap, high elasticity [1], making it a promising candidate for high-speed nanoelectronics.

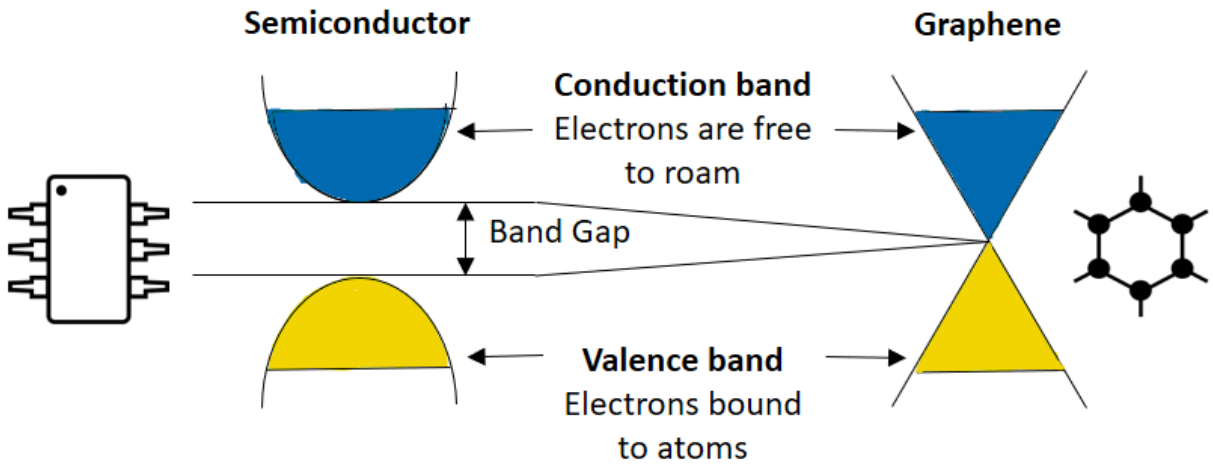


Figure 1: comparison of energy band gap between semiconductor and graphene.

Electrons in the solid are restricted to a certain band of energy (vertical axis). In figure 6 on left-hand side is the energy band gap of the semiconductor where electrons are bound to an atom and can break free or go into the conduction band if they can overcome the band gap by gaining energy by heat or passing photon. But on the right side is the band gap for graphene, which is infinitesimal, which ensures a fast and easy flow of electrons.

2.2 Synthesis –

There are four primary ways to produce pure graphene [3].

2.2.1 Epitaxial Graphene –

This method involves chemical vapor deposition (CVD) growth on the epitaxially matched metal surface.

2.2.2 Micromechanical Exfoliation –

This process produces high quality of graphene that is electrically isolated for fundamental studies of transport physics and other properties, but this approach is not scalable to the large area. Micromechanical Exfoliation, produces graphene in the order of ten to hundreds of micrometers.

2.2.3 Exfoliation of Graphene in Solvents –

Based on the dispersion of graphite in various solutions, typically done by the acquaintance of graphite powers in organic solvents such as DMF or NMP to high-intensity ultrasound.

2.2.4 Substrate –

Free gas-phase synthesis of graphene platelets gives large-scale production of powered graphene of high purity by CVD approach.

2.3 Multi-Layer Graphene Nano-Ribbon (MLGNR) –

The Graphene nanoribbons are the strips of graphene with the width less than 50nm. These ribbons were first introduced as a theoretical model by Mitsutaka Fujita and his team to examine the edge and nanoscale size effect in graphene [4].

2.3.1 Electrical Properties –

The electronic state of GNRs depends mainly on the edge structure (armchair or zigzag). In an armchair edge, each pair of segments is a 120/-120-degree rotation of the previous couple whereas, with zigzag edges, each successive edge segment is at an opposite angle to the previous. The zigzag edges provide edge localized state with non-bonding molecular orbitals near the Fermi energy [4].

The tight binding theory predicts that zigzag GNRs are always metallic by nature, while the armchairs can be either metallic or semiconducting depending on their width. The Density Functional Theory (DFT) calculations show that armchair nanoribbons are semiconducting by nature with energy gap proportional to the inverse of the GNR width [5].

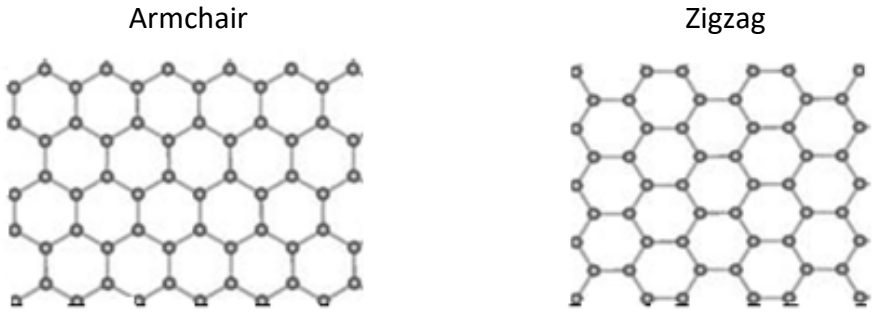


Figure 2: Structure of graphene nanoribbons with armchair edges (armchair nanoribbon) on left and zigzag edges nanoribbons (zigzag nanoribbon) on right [6]

Their two-dimensional structure, high thermal and electrical conductivity and low noise make GNRs a possible alternative to copper for high speed integrated circuits interconnects. Graphene nanoribbons possess semi-conductive properties and are an excellent alternative to the silicon semiconductors capable of sustaining microprocessor clock speed up to 1THz [7].

2.4 Multi-layer Graphene Nanoribbon (MLGNR) Flash Memory –

The explosion of connected devices and digital services is generating a massive amount of new data. This data is only useful if its stored and analyzed quickly, creating challenges for the service providers and system builders who must balance cost, power and performance trade-offs while designing memory and storage solutions. With the conventional Silicon based flash memory technology reaching its limit, concerning to the physical and material characteristics, researchers are looking for new materials and techniques.

Scaling of flash memory devices leads to high data storage capacity and lower program/ erase voltages for these devices. However, scaling also results in increased capacitive coupling between the floating gates of adjacent cells. This parasitic coupling between neighboring cells causes a wide distribution in the threshold voltages of the devices [8]. Reducing the height of the floating gate is one possible solution to reduce the capacitive coupling. Experiments prove that the conventional polycrystalline silicon (poly-Si) floating gate thickness can be reduced to 7nm. However, a significant fraction of an electron injected into such thin poly-Si would be ballistically transported through floating gate, that would result in slower programming. These ballistic can cause impact ionization in the blocking dielectric, degrading dielectric reliability. To improve these issues with thin poly-Si floating gate, use of thin metal layer in place of thin poly-

Silicon is proposed, and 1nm thin metal layer as a floating gate material can suppress the ballistic current component [9].

Since graphene is the thinnest naturally stable sheet having metallic properties, it would be interesting to use graphene in place of poly-Si or metal as charge storage layer in floating gate flash memory. The interlayer spacing between two graphene sheets in MLG is the only 0.34nm, 6-7 layers of MLG sheets would be 2-3nm thick. Thus, use of MLG in flash memory leads to substantial reduction in the vertical dimension of these devices. Also, graphene is thermally stable up to $1500^{O}C$ [10]. Thus, thermal stability issues anticipated with metal floating gate may not be a problem with graphene.

The multilayer graphene (MLG) has several technical advantages over their single layer analogs. A single layer graphene (SLG) has a work function (WF) of 4.2eV. WF of the MLG depends on the number of layers when it is less than 4. For thicker MLG sheets (>4 layers) WF saturates to 4.6eV [11]. Higher WF of MLG is favorable for long-term data retention. Another consideration for using MLG is the higher density of states (DOS) in MLG compared to SLG [12]. Higher the DOS, larger is the memory window. So, MLG based flash memories have larger memory window compared to SLG based flash memories.

CHAPTER 3

DEVICE SPECIFICATIONS

3.1 Device Description –

Figure 8 shows the detail procedure for fabricating the MLGNR flash memory. The flash memory structure is fabricated on silicon dioxide substrate which also acts as a bottom oxide (figure 8(a)). The doped reservoir serves as drain and source of the device is placed over the bottom oxide (figure 8(b)). Multilayer graphene nanoribbon connects these two terminals (figure 8(c)). Tunnel oxide covers the entire channel as well as the drain and source reservoir (figure 8(d)). Storage layer or the graphene floating gate covers the tunnel oxide which is used as a charge trapping layer (figure 8(e)). Upon which the control oxide is placed (figure 8(f)). The top and the bottom control gate are self-aligned with the channel as shown in the figure 8(f).

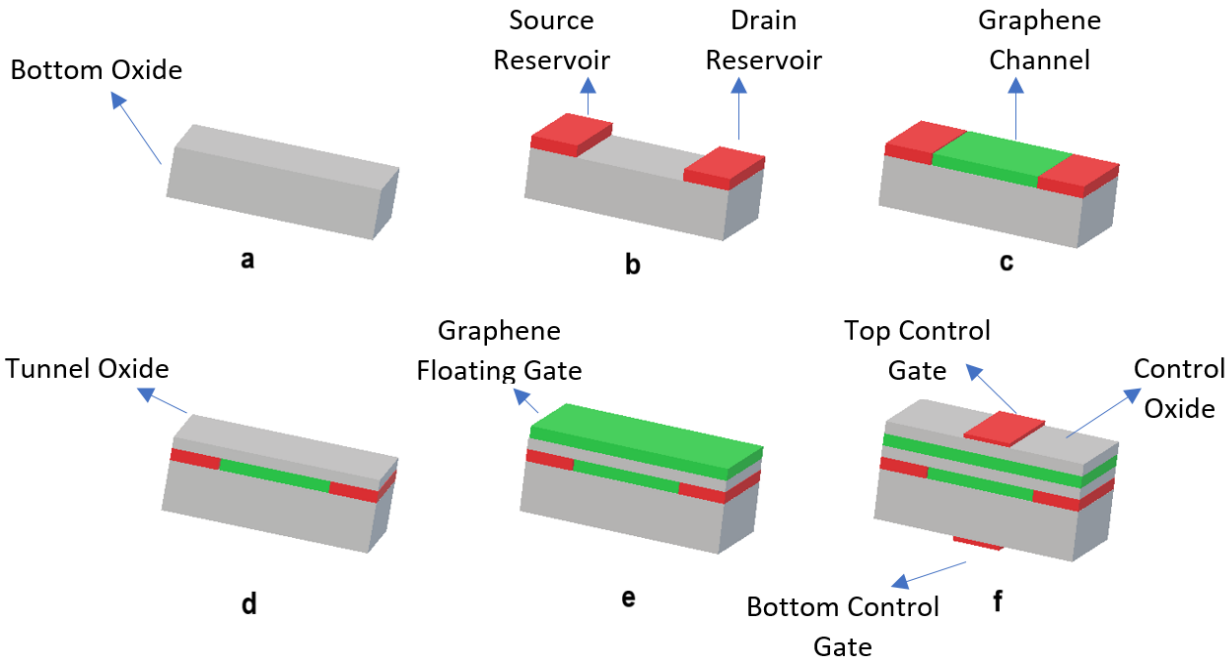


Figure 3: Detail steps for fabricating MLGNR flash memory

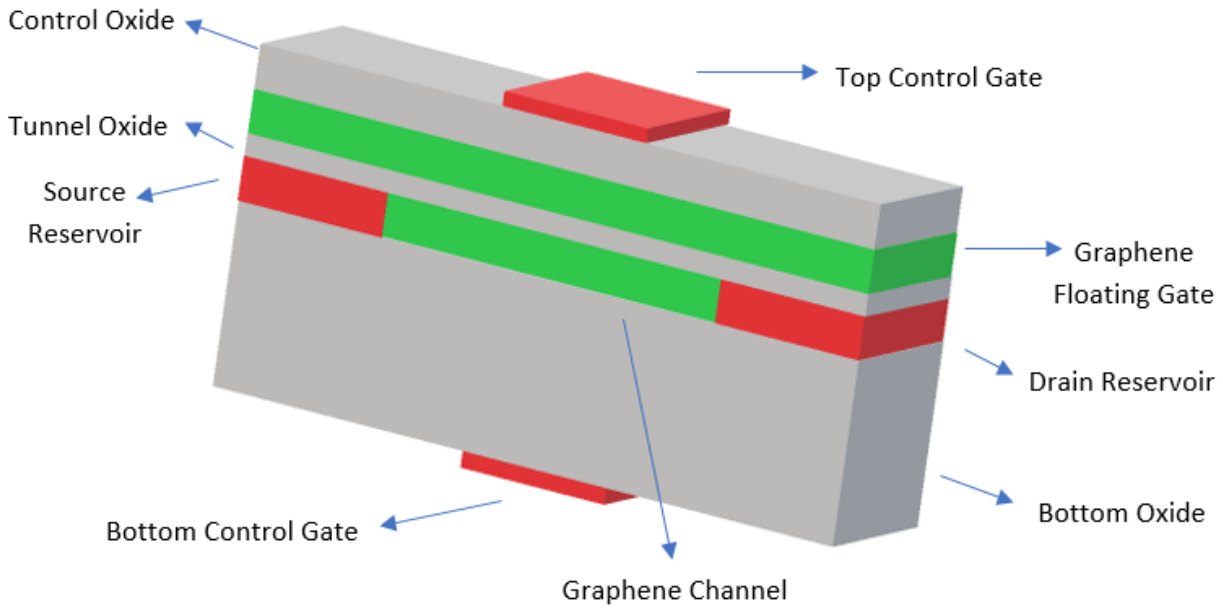


Figure 4: MLGNR flash memory cell

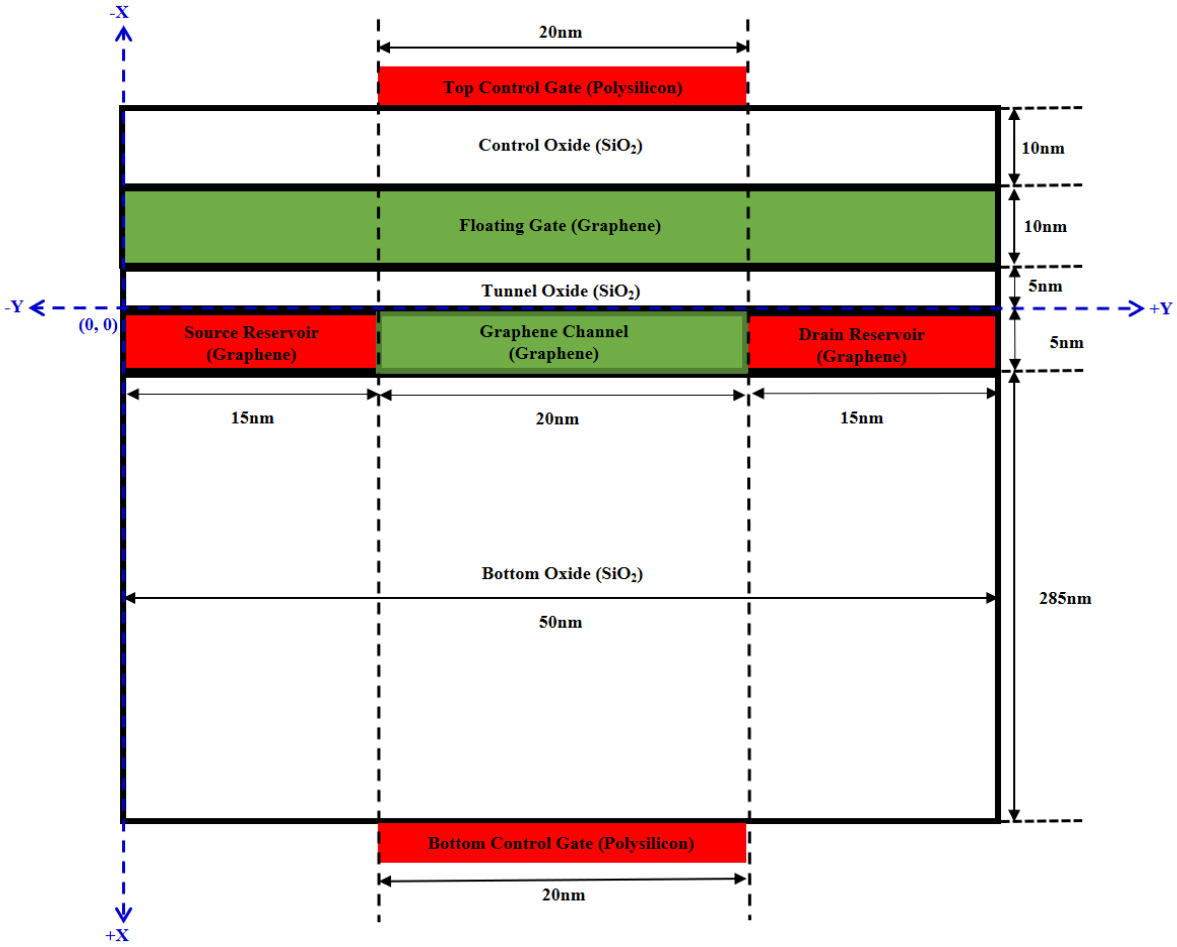


Figure 5: Material and dimensions description of the MLGNR flash memory cell

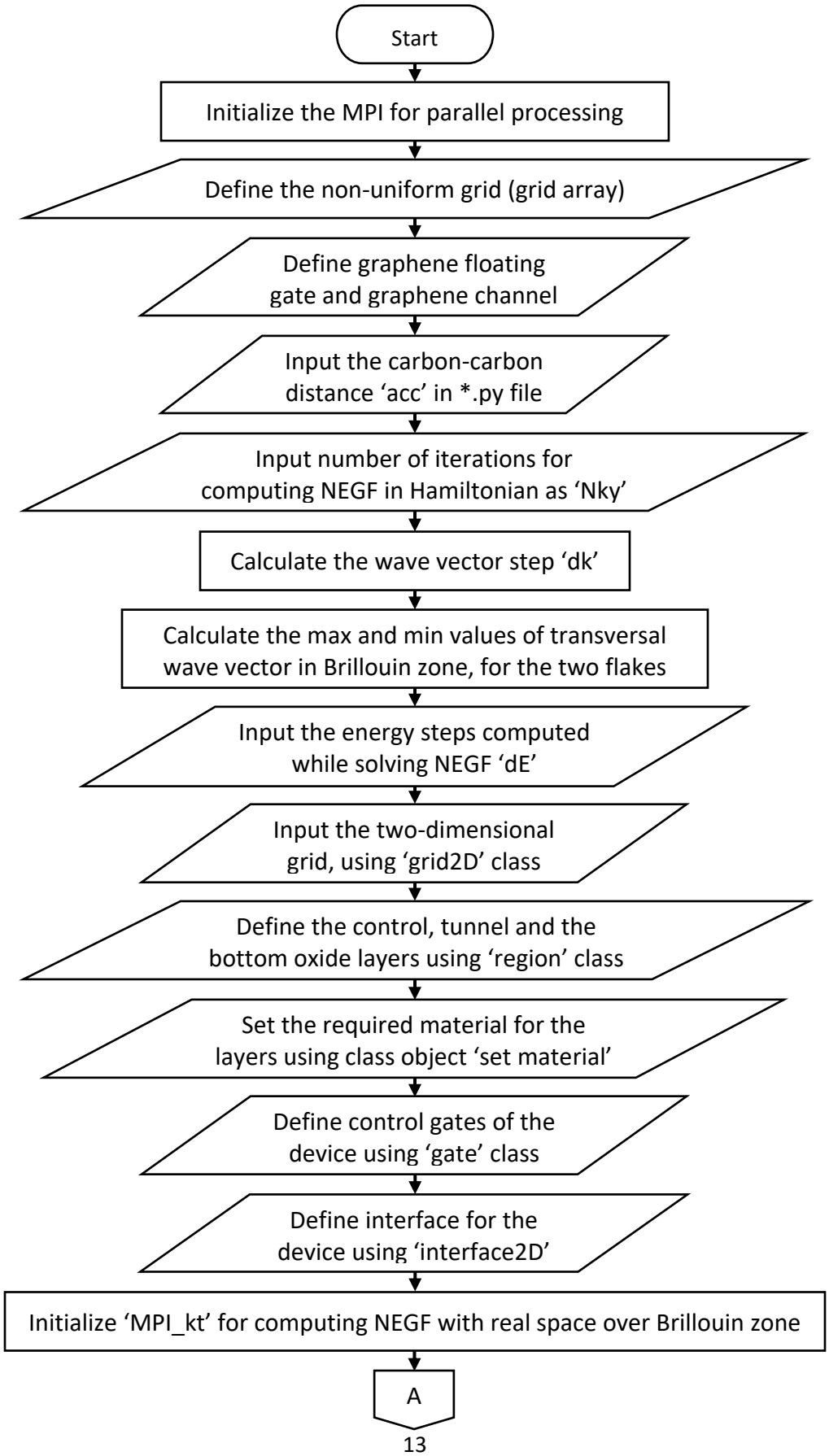
Table 1: Detail description of the MLGNR flash memory cell

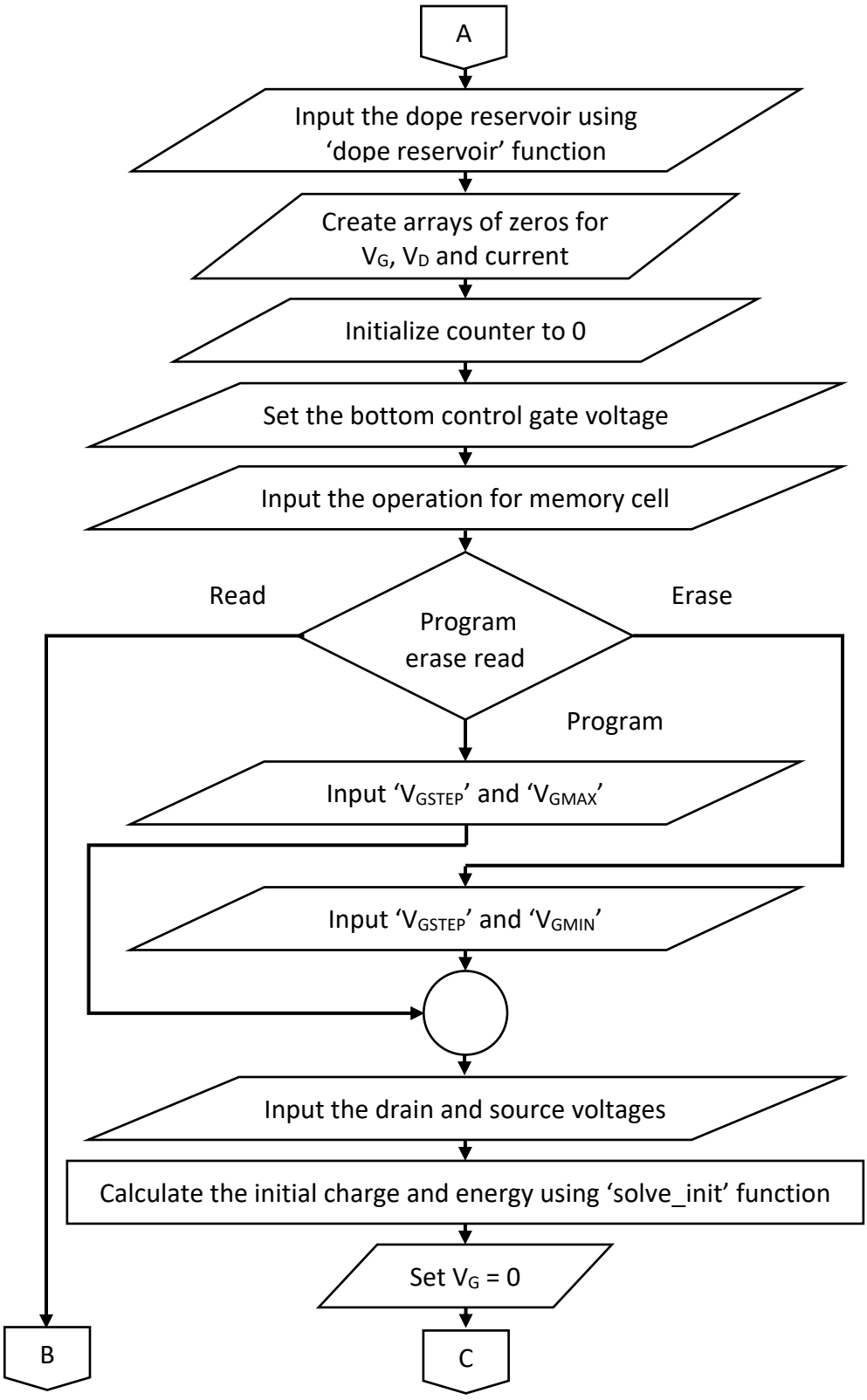
	Proposed Design	
	Material	Dimension
Top Gate Length	Polysilicon	20nm
Control Oxide Thickness	SiO_2	10nm
Control Oxide Length	SiO_2	50nm
Floating Gate Thickness	Graphene	10nm
Floating Gate Length	Graphene	50nm
Tunnel Oxide Thickness	SiO_2	5nm
Tunnel Oxide Length	SiO_2	50nm
Channel Thickness	Graphene	5nm
Channel Length	Graphene	50nm
Source Reservoir Thickness	Graphene	2nm
Source Reservoir length	Graphene	15nm
Drain Reservoir Thickness	Graphene	2nm
Drain Reservoir length	Graphene	15nm
Bottom Oxide Thickness	SiO_2	285nm
Bottom Oxide length	SiO_2	50nm
Bottom Gate Length	Polysilicon	20nm

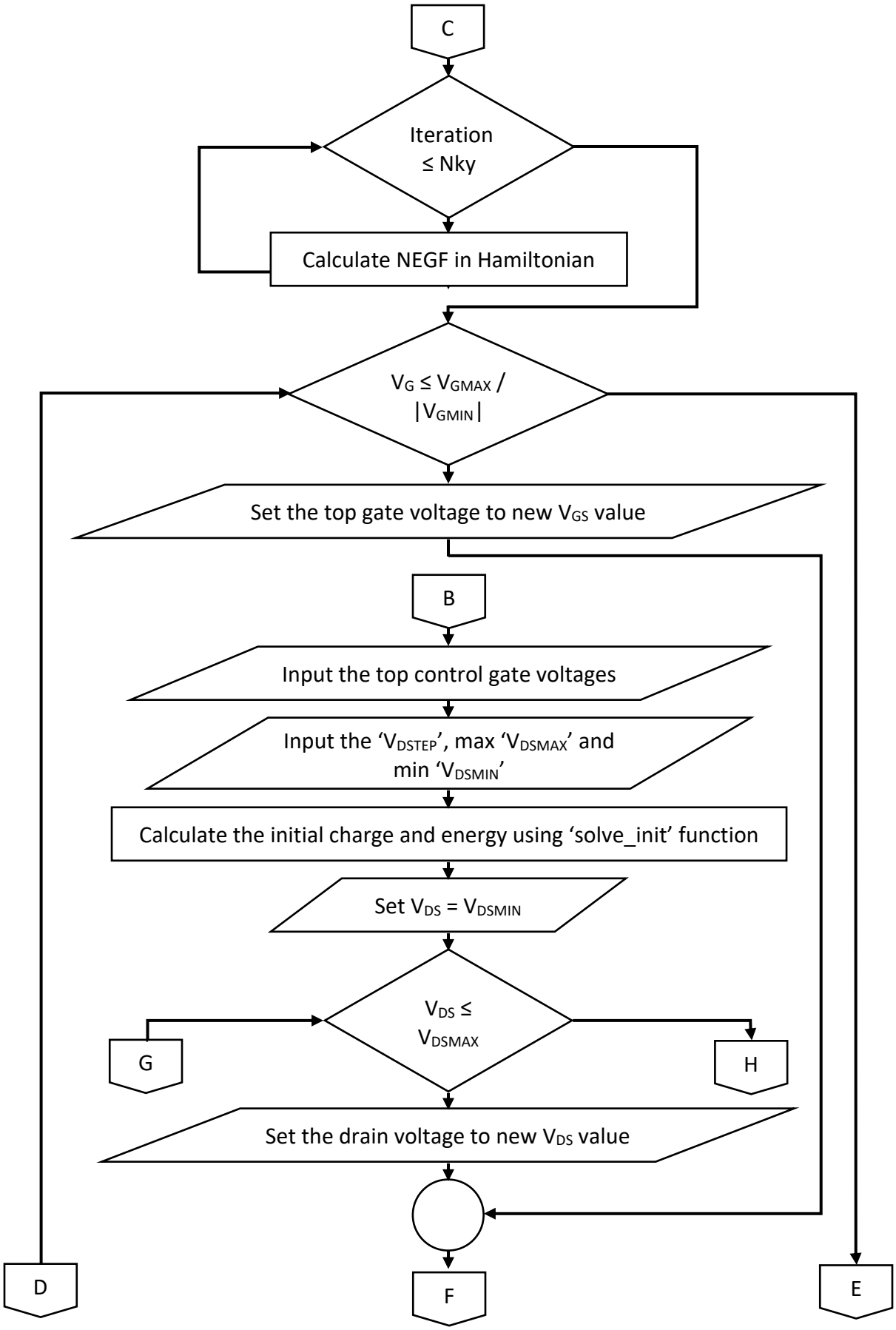
CHAPTER 4

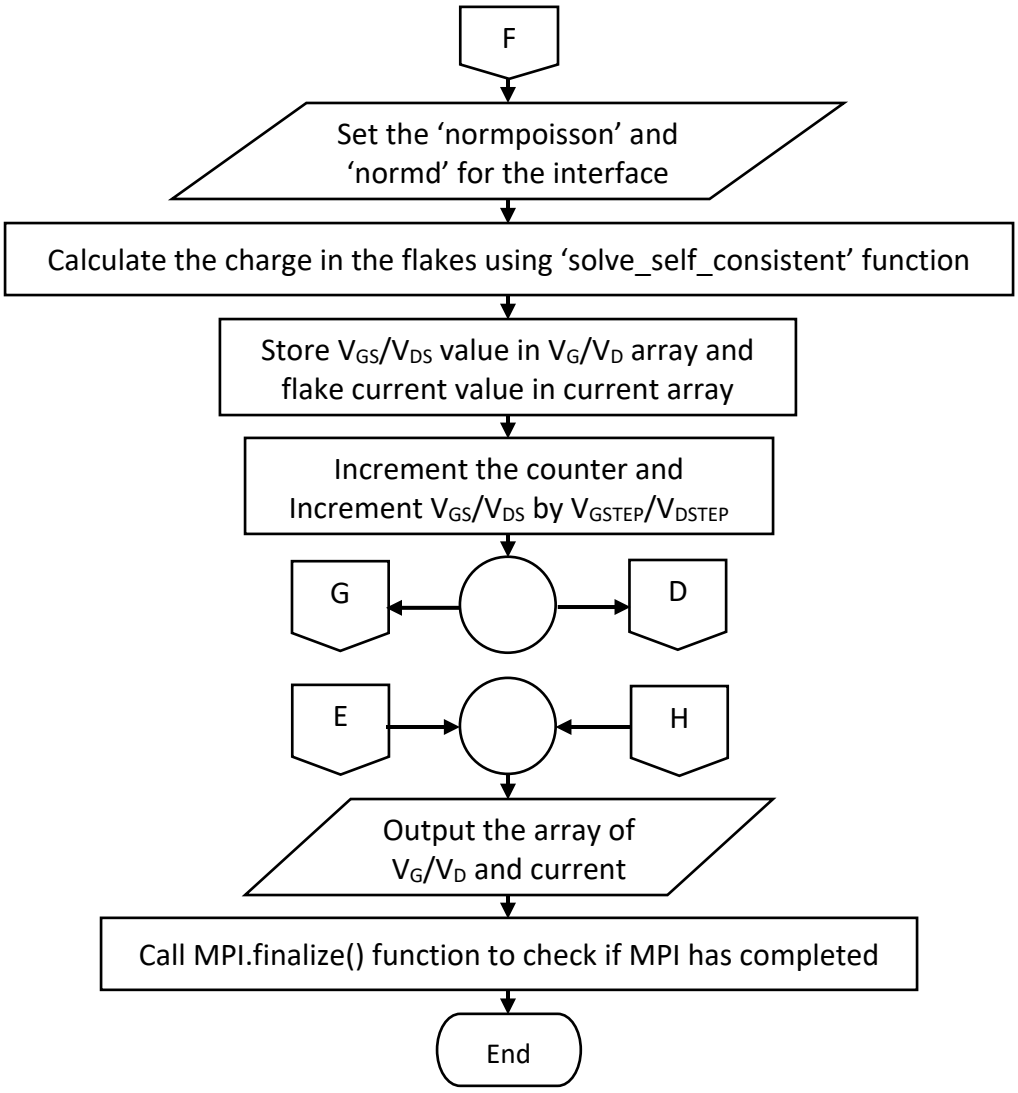
FLOWCHART AND MODULE

4.1 Flowchart –


Start
Initialize the MPI for parallel processing
Define the non-uniform grid (grid array)
Define graphene floating gate and graphene channel
Input the carbon-carbon distance ‘acc’ in *.py file
Input number of iterations for computing NEGF in Hamiltonian as ‘Nky’
Calculate the wave vector step ‘dk’
Calculate the max and min values of transversal wave vector in Brillouin zone, for the two flakes
Input the energy steps computed while solving NEGF ‘dE’
Input the two-dimensional grid, using ‘grid2D’ class
Define the control, tunnel and the bottom oxide layers using ‘region’ class
Set the required material for the layers using class object ‘set material’
Define control gates of the device using ‘gate’ class
Define interface for the device using ‘interface2D’
Initialize ‘MPI_kt’ for computing NEGF with real space over Brillouin zone
A


A
Input the dope reservoir using 'dope reservoir' function
Create arrays of zeros for V_G, V_D and current
Initialize counter to 0
Set the bottom control gate voltage
Input the operation for memory cell
Read
Program erase read
Erase
Program
Input 'V_{GSTEP}' and 'V_{GMAX}'
Input 'V_{GSTEP}' and 'V_{GMIN}'
Input the drain and source voltages
Calculate the initial charge and energy using 'solve_init' function
Set V_G = 0
B
C


C
Iteration
≤ Nky
Calculate NEGF in Hamiltonian
$V_G \leq V_{GMAX}$ /
$|V_{GMIN}|$
Set the top gate voltage to new V_{GS} value
B
Input the top control gate voltages
Input the 'V_{DSTEP}', max 'V_{DSMAX}' and
min 'V_{DSMIN}'
Calculate the initial charge and energy using 'solve_init' function
Set $V_{DS} = V_{DSMIN}$
$V_{DS} \leq$
V_{DSMAX}
G
H
Set the drain voltage to new V_{DS} value
D
F
E


F
Set the ‘normpoisson’ and ‘normd’ for the interface
Calculate the charge in the flakes using ‘solve_self_consistent’ function
Store V_{GS}/V_{DS} value in V_G/V_D array and flake current value in current array
Increment the counter and Increment V_{GS}/V_{DS} by V_{GSTEP}/V_{DSTEP}
G
D
E
H
Output the array of V_G/V_D and current
Call MPI.finalize() function to check if MPI has completed
End

4.2 Module –

4.2.1 vIDEs Class and Function Definitions –

NanoTCAD vIDEs has specific modules developed for the different materials used to build the GFGT. Like the SiO_2 structure, drain and source reservoirs, graphene is used for channel and floating gate, the metal contacts used as top and bottom gate.

4.2.1.1 Non-uniform Grid –

Syntax – nonuniformgrid (numpy_array)

This command allows creating a non-uniform grid along one axis. Numpy array is an array of an even number of elements in the form of X_1, Δ_1, X_2, Δ_2.... X_n, Δ_n, where X_i defines the position of the grid point along the general direction (x, y, z) in nanometer, while Δ_i is the spacing between two user-defined points.

4.2.1.2 Graphene Definition –

Syntax – graphene (L)

Graphene (L) is the NanoTCAD vIDEs class for graphene flake. As the input, it requires the length of the graphene flake in Nano-meter. The actual simulation domain contains a chain of carbon atoms along y-direction and L nanometer long. The flake is then repeated along the y-direction attaching semi-infinite leads through the definition of self-energy $\sum$, while in the transversal direction periodic boundary condition is imposed. Along the x-direction, the flake is periodic with period Δ.

Attributes –

a. acc (double): Carbon to carbon distance expressed in nanometers.

b. E (numpy array): Array of energies for which the transmission coefficient and the free charge is computed in the graphene using NEGF formalism.
c. T (numpy array): Array of transmission coefficient computed in correspondence of the energies stored in the E array.
d. kmax (double): Maximum value of the transversal wave vector in the Brillouin zone, over which the integral for the T and the charge is computed. Default value pi/ Δ.
e. kmin (double): Minimum value of the transversal wave vector in the Brillouin zone, over which the integral for the T and the charge is computed. Default value 0.
f. dk (double): The wave vector step used for the computation of the charge and the T.
g. dE (double): The energy step computed when solving the NEGF.
h. mu1 (double): Fermi level of the left reservoir.
i. mu2 (double): Fermi level of the right reservoir.
j. current (function): Computes the current through the landauer formula, once filled the T vector.

4.2.1.3 Grid2D –

Syntax – grid2D (xg, yg, [xC, yC] ...)

xg and yg are points of the discretized grid along x and y-axis. xC and yC are the x and y-coordinates of the atoms to be included in the 2D domain. Grid2D deals with the non-uniform rectangular grids, with all the relevant quantities required to discretize the 2D Poisson equation within the box-integration method.

Attributes –

a. xmin (double): minimum of the x-coordinate.

b. xmax (double): maximum of the x-coordinate.

c. ymin (double): minimum of the y-coordinate.

d. ymax (double): maximum of the y-coordinate.

4.2.1.4 Oxide definition –

Syntax – region ('region geometry', coordinates)

The oxide can be defined using the region class, which is devoted to defining to which material the points of the grid belong.

Attributes –

a. geometry (string): defines the geometry of the oxide, hexahedron geometry, used to pass six values xmax, xmin, ymax, ymin, zmax, zmin.

b. eps (double): define the relative dielectric constant of the material.

c. set material (string): define the region as Si, SiO_2, HfO_2.

4.2.1.5 Gate definition –

Syntax – gate ('gate geometry', coordinates)

The gate can be defined using the gate class, which is devoted to defining the points of the grid in which Dirichlet boundary conditions must be imposed. All the points of this class maintain their electrostatic potential fixed to the predetermined user-defined value.

Attributes –

a. geometry (string): defines the geometry of the gate, hexahedron geometry, used to pass six values xmax, xmin, ymax, ymin, zmax, zmin.

b. Ef (double): Fermi level of the gate.

Note – Fermi level is the opposite of electrostatic potential.

4.2.1.6 Reservoir definition –

Syntax – dope reservoir (grid, interface, NEGF class, molar fraction, boundary box)

This function imposes a doping equal to the molar fraction in correspondence of the atoms of the NEGF class, that are included in the hexahedron region defined by numpy array boundary box containing its coordinates xmax, xmin, ymax, ymin, zmax, zmin.

4.2.1.7 The Initial Solution –

Syntax – solve init (grid, interface, channel)

The function computes the initial solution of the Poisson equation. It solves the Laplace equation over the whole domain, imposing Dirichlet boundary conditions in correspondence of the gate, and the atoms belonging to the doped reservoirs. The potential E^* to be imposed in the reservoir is calculated assuming complete ionization and solving the following equation

$$\rho_{fix} = N_{1D} \log[1 + \exp(\frac{E^*}{V_T})] \ldots ①$$

Where N_{1D} is the one-dimensional density of the states self-computed by the solve init procedure, while the left-hand term is the fixed charge, equal to the molar fraction of the reservoir [14].

4.2.1.8 Solve Self-Consistent Function –

Syntax – solve self-consistent (grid, interface, NEGF class)

Solve self-consistent function solves self-consistently the Poisson equation and the NEGF on the material specified by NEGF class. The code is based on [13]

$$\nabla \bullet [\varepsilon \nabla \phi] = -q\,[\mathrm{p} - \mathrm{n} + \rho_{fix}] \ldots ②$$

The Schrödinger equations/ NEGF equations are solved at the beginning of each NR cycle, starting from the initial potential ϕ, and the charge density in the NEGF class is kept constant until NR cycle converges. Then the algorithm solve-Poisson is repeated until the norm of the difference between the potential computed at the end of two subsequent NR cycles is smaller than a predetermined value [15].

4.2.1.9 Solve Poisson Function –

Syntax – solve Poisson (grid, interface)

This function is devoted to solving the Poisson equation. Arguments passed are the grid and the interface class. Equation to be solved is

$$\nabla \bullet [\varepsilon \nabla \phi] = -q\,[\mathrm{p} - \mathrm{n} + \rho_{fix}] \ldots ③$$

Where $(\mathrm{p} - \mathrm{n})$ is the free charge, ε is dielectric constant, ϕ is the electrostatic potential and ρ_{fix} is the fixed charge. As the input, it requires a free charge and fixed charge to be passed in the interface, and as output, it returns electrostatic potential stored in the attribute Phi of the class interface [16].

4.3 Calculation –

4.3.1 Initial Calculations –

acc/ a = 0.144 (carbon to carbon distance used for initial calculations)

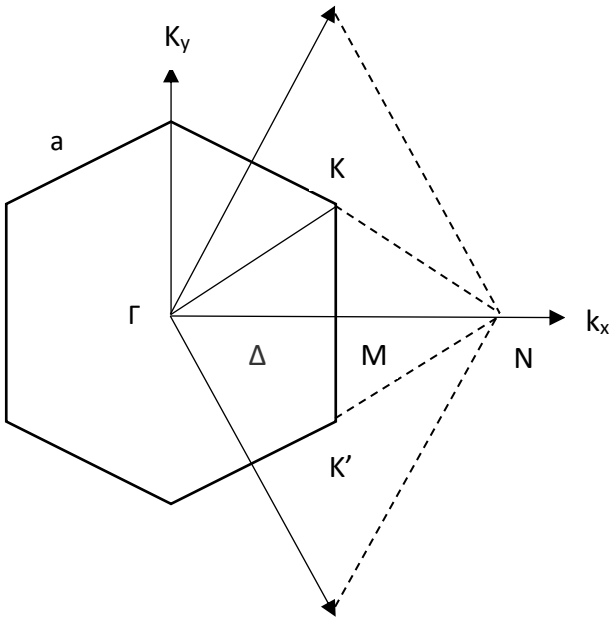


Figure 6: First Brillouin zone of the honeycomb lattice and the Dirac points K and K' at the corners.

The position of the two Dirac points K and K', located at the corners of the Brillouin zone are

$$K = \frac{2\pi}{3a}\left(x' + \sqrt{3}y'\right), K' = \frac{2\pi}{3a}\left(x' - \sqrt{3}y'\right)$$

In the simulation, we are considering only the x-direction,

$kF = \frac{2pi}{3\Delta}$ … ④, in x-direction, where $\Delta = \sqrt{3} \cdot acc$

$$kymax = kF + 2 \text{ … ⑤}$$

$$Nky = 32$$

We are defining the number of such K points, i.e., number of transversal k-points

$$dk = \frac{(kymax - kF)}{Nky * 0.5} \text{ … ⑥}$$

Step/ intervals at which charge and the transmission coefficient.

$$FLAKE.kmax = kF + dk * Nky * 0.5 \ldots ⑦$$

$$FLAKE.kmin = kF - dk * Nky * 0.5 \ldots ⑧$$

kmax and kmin represent the max and min values of wave vector 'k' in the Brillouin zone [17]. (Brillouin zone is a region under which the characteristics of atoms are same.)

4.3.2 Approach –

Calculations are based on the self-consistent solution of many-body Schrodinger equation with density functional theory and the computation of the conductance of tunnel constrictions through the solution of 3D Schrodinger equation with open boundary conditions.

Self-consistent Poisson-Schrodinger equation is solved with density functional theory, the device capacitances are extracted from the dependence of electrochemical potential of the dot on the gate and reservoir voltages, and conductance is computed using 1D transfer Hamiltonian formalism [18].

The Poisson equation is solved over the entire 3D domain, while the Schrodinger equation is limited to confined regions and solved in momentum space. The numerical algorithm is based on Newton-Raphson (NR) method. To compute the single electron transistor (SET) conductance within the 3D treatment of transport, we solve the 3D Schrodinger equation with open boundary conditions for each quantum constriction using the scattering matrix technique. The domain is divided into N slices along the propagation direction, and 2D Schrodinger equation in the transversal plane is solved for each slice. By enforcing mode matching, we then compute the total scattering matrix of the constriction and therefore the conductance.

4.3.3 Numerical Method –

To solve Schrodinger equation with mean field approximation we solve the nonlinear Poisson equation in 3D,

$$\nabla[\varepsilon(\mathrm{r})\nabla\,\phi(\mathrm{r})] = -q\,[\mathrm{p(r)} - \mathrm{n(r)} + N_D^+(r) - N_A^-(r) + \rho_{fix}] \ldots ⑨$$

Where ϕ is electrostatic potential, ε is dielectric constant, p and n are the hole and electron densities. N_D^+ is the concentration of ionized donors, N_A^- is the concentration of ionized acceptors, and ρ_{fix} is fixed charge density [21][22].

Semiclassical approximation is assumed in the whole domain for hole, acceptor, and donor densities, electron densities are strongly confined region is computed by solving the Schrodinger equation with Density Functional Theory (DFT) and Local Density Approximation (LDA). Elsewhere, for electron density, the semiclassical expression is used. The Schrodinger equation for Kohn-Sham single electron is,

$$-\frac{\hbar^2}{2}\,\nabla\,[m^{-1}(r)\nabla\Psi(r)] + V(r)\Psi(r) = E\Psi(r) \ldots ⑩$$

Where $\hbar$ is reduced Planck's constant, m is effective mass and Ψ and E are the eigenfunction and eigenvalues. The potential V in equation ⑩, can be expressed as $V = \mathrm{E}_C + V_{exc}$, where E_C is the conduction band edge, and V_{exc} is exchange-correlation potential.

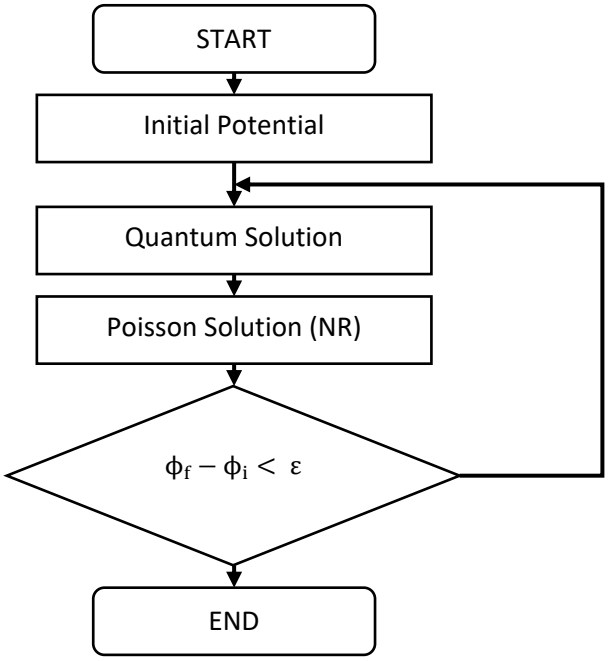
$$V_{exc} = -\frac{q^2}{4\pi^2\varepsilon_0\varepsilon_r}[3\pi^2 n(r)]^{\frac{1}{3}} \ldots ⑪$$

We use the expression valid for the 3D system.

The coupled Poisson and Schrodinger equations are solved using Newton-Raphson method. The Schrodinger equation is resolved at the beginning of each NR cycle. The eigenfunctions are the kept constant until each NR cycle converges, while eigenvalues are adjusted. At the end of NR cycle, the Schrodinger equation is solved again, and a new NR cycle is

performed. The algorithm is ended when the norm-two of the difference between the electrostatic potentials obtained at the end of successive NR cycle is smaller than the given threshold.

Initial potential ϕ_i is used to compute the local density of states by solving Schrodinger equation, the local density of states is then frozen, and non-linear Poisson equation is solved with NR algorithm to obtain potential ϕ_f. If ϕ_f is not close enough to ϕ_i, a new cycle is started by again computing local density of states.



Flowchart of self-consistent 3D Poisson Schrodinger solver

Concerning 3D quantum region, the quantum dot, the number of electrons in the confined region is fixed to N, and electron density is expressed as

$$n(r) = 2\sum_{i=1}^{m}|\varphi_i(r)|^2 + (N-2m)\,|\varphi_m + 1(r)|^2 \ldots ⑫$$

Where φ_i is orbital associated to the ith eigenvalue, and $m = \left[\frac{N}{2}\right]$ is the number of fully occupied single electron levels.

For given N, the electrochemical potential of the dot can be determined simply using Slater formula. The electrochemical potential $\mu(N)$, defined as the energy necessary to add the Nth election to the dot, can be expressed as

$$\mu(N) = E(N) - E(N-1) = \varepsilon\,(\mathrm{N} - 0.5) \ldots ⑬$$

Where E is the total energy of dot, while ε is the energy of half-occupied highest Kohn-Sham orbital of a system with $N - 0.5$ electrons.

Once we have the band and density profiles at quasi-equilibrium, we compute the transport properties of the device. To calculate conductance between two generic sub regions of the device, we solve 3D Schrodinger equation with open boundary conditions along the direction of propagation.

CHAPTER 5

RESULTS

5.1 GFGT using SiO_2 as the control oxide –

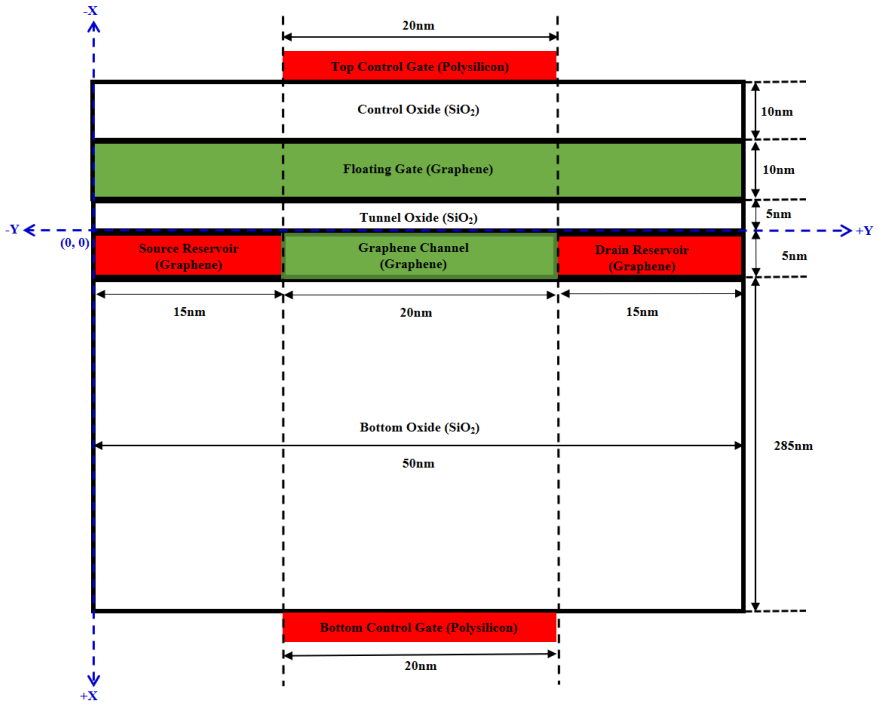


Figure 7: GFGT using SiO_2 as the top control oxide

The Flash memory cell functions by storing charge in the floating gate or storage layer. The presence or the absence of charge in the floating gate determines whether the channel will conduct or not.

5.1.1 Program operation –

The proposed FGT is programmed by applying a positive high voltage pulse to the control gate terminal, at a small V_{DS}, which leads to electron tunneling through tunnel oxide layer by hot electron injection effect. This high voltage at the control gate terminal coupled to the floating gate through the control oxide and invert channel. These inverted channel electrons have high drift velocity and kinetic energy. The collision between these energetic electrons dissipates heat

which increases the temperature. These hot electrons cannot transfer their kinetic energy to the surrounding atoms quickly and spread towards the oxide layer. The reason why these hot electrons move vertically (Floating gate) instead of horizontally (Source) is the high positive voltage at the control gate. These tunneled electrons are injected into the floating gate (Graphene storage layer) from the channel (Graphene). The stored charge in the Graphene storage layer causes an increase in the threshold voltage (V_{TH}) of the proposed FGT. This high V_{TH} is read as a logic "0". Figure 13 shows "Program" operation: I_{DS} versus V_{TG} characteristics and Table 2 simulation conditions.

Table 2: Simulation conditions for program operation using SiO_2 as control oxide

V_{TG}	0 V to +20 V
V_{DS}	0.5 V
V_{BG}	0 V
Temperature	300 K

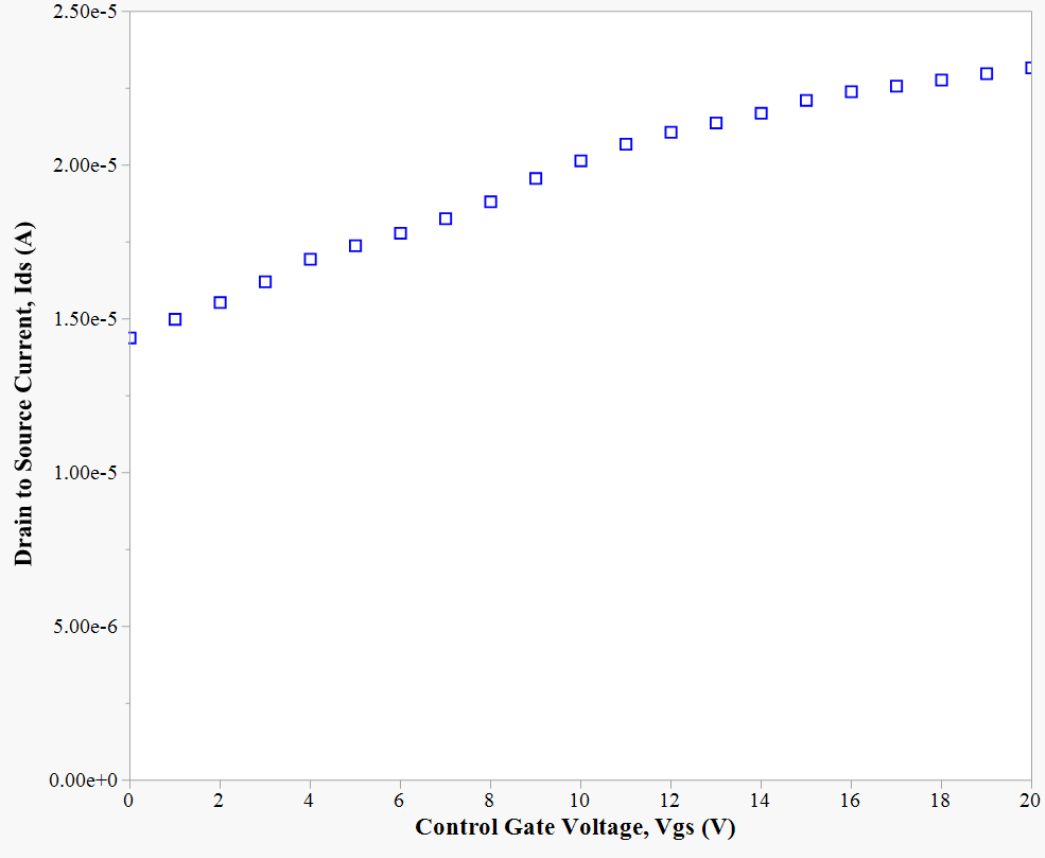


Figure 8: Program operation I_{DS} versus V_{TG} characteristics when V_{DS} = 0.5V is fixed for SiO_2 as control gate

5.1.2 Erase operation –

The memory cell is erased by applying a high negative voltage (-20V) pulse to the control gate terminal of the proposed device, and a small V_{DS} is maintained. The stored electrons in the floating gate (storage layer) are tunneled back to the MLGNR channel through the tunnel oxide. So, the floating gate is discharged by the Erase Operation, which is read as a digital logic "1". Due to this discharge of electrons from the floating gate, V_{TH} drops to the original voltage level. Figure 14 shows the "Erase" operation: I_{DS} vs V_{TG} characteristics and Table 3 tabulated simulation conditions.

Table 3: Simulation conditions for Erase operation using SiO_2 as control oxide

V_{TG}	-20 V to 0 V
V_{DS}	0.5 V
V_{BG}	0 V
Temperature	300 K

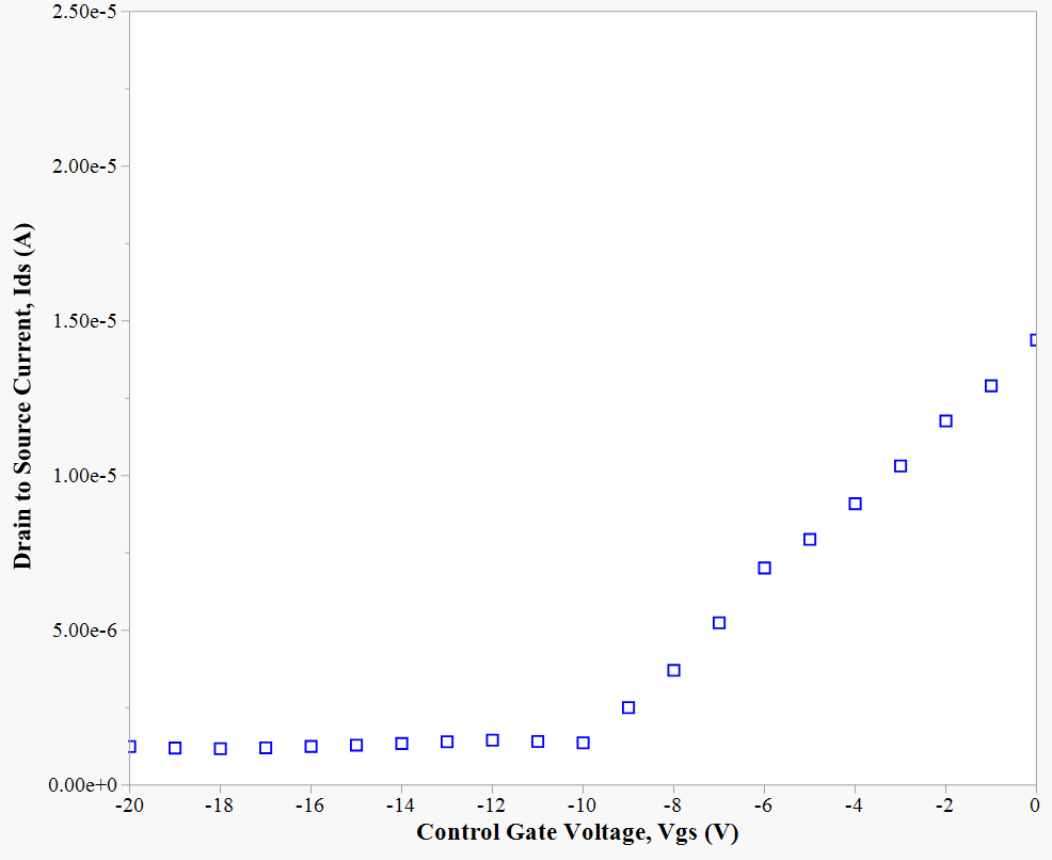


Figure 9: Erase operation I_{DS} versus V_{TG} characteristics when V_{DS} = 0.5V is fixed for SiO_2 as control gate

5.1.3 Program vs Erase Operation –

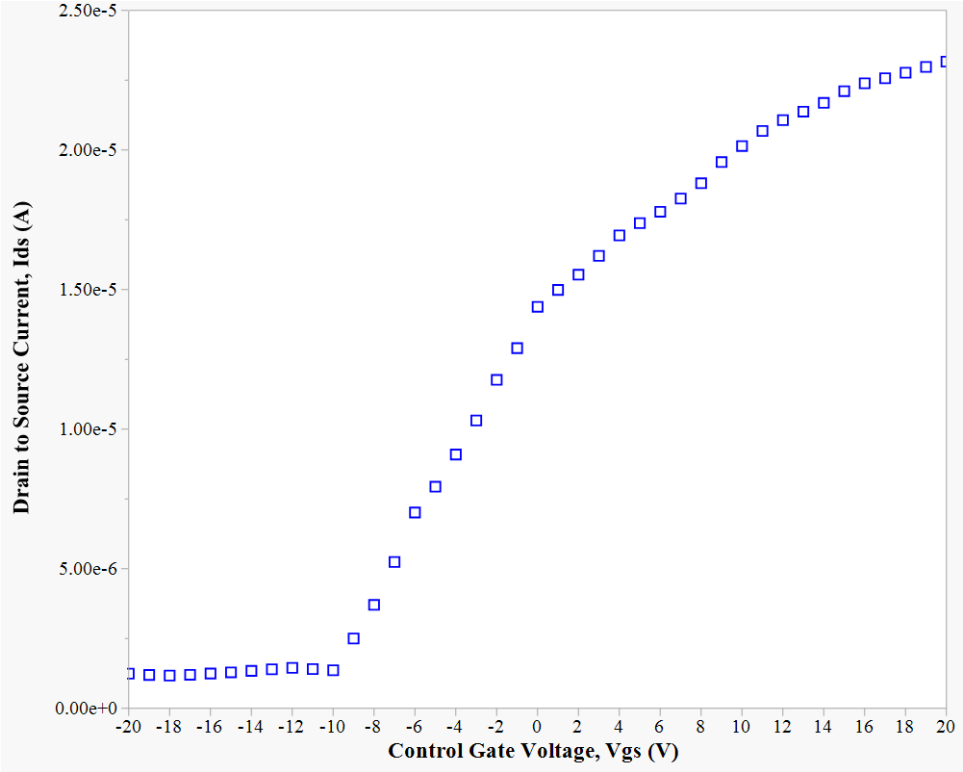


Figure 10: Program and Erase operation I_{DS} versus V_{TG} characteristic when V_{DS} = 0.5V is fixed for SiO_2 as control gate

5.1.4 Read Operation –

The proposed FGT is read by applying an intermediate positive control gate voltage to the memory device while reading the drain current. The intermediate voltage is chosen between the min threshold voltage (erased state) and max threshold voltage (programmed state) of the proposed FGT. This intermediate control gate voltage is such that FGT will maintain its previous state, i.e. Program and Erase. Figure 16 shows the "Read" operation: I_{DS} versus V_{TG} characteristics and Table 4 tabulated simulation conditions.

If the memory cell is programmed (stored “0”), after the “Read” operation FGT will remain off. If FGT is programmed, the Graphene channel remains off and does not conduct current. This lack of current conduction is read as a “Programmed” or logic “0”.

If the memory cell is erased (stored “1”), after the “Read” operation FGT will remain turned on. If FGT is erased, the Graphene channel turns on and starts current conduction. This current conduction is read as an “Erased” or logic “0”.

Table 4: Read Operation simulation conditions using SiO_2 as control oxide

V_{TG}	4.5 V
V_{DS}	0 ~ 1 V
V_{BG}	0 V
Temperature	300 K

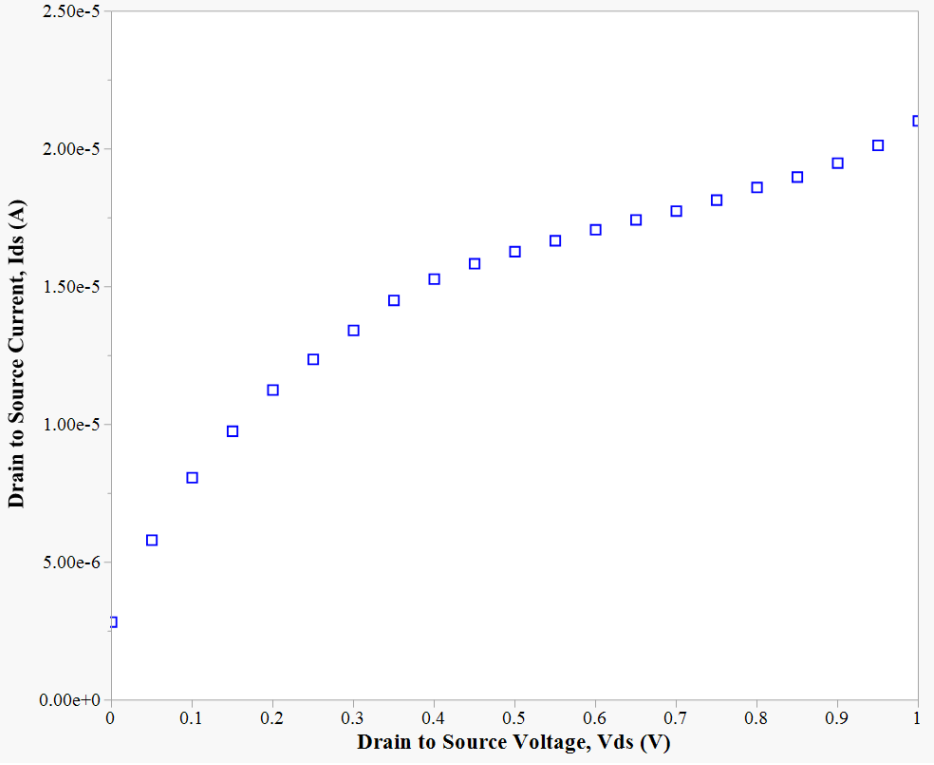


Figure 11: Read operation I_{DS} versus V_{TG} characteristic when V_{TG} = 4.5V is fixed for SiO_2 as control gate

So, if I_{DS} is relatively high, the logic high or "1" is stored in the proposed FGT. If I_{DS} is relatively low, logic low or "0" is stored in the proposed FGT.

5.2 GFGT using HfO_2 as the control oxide –

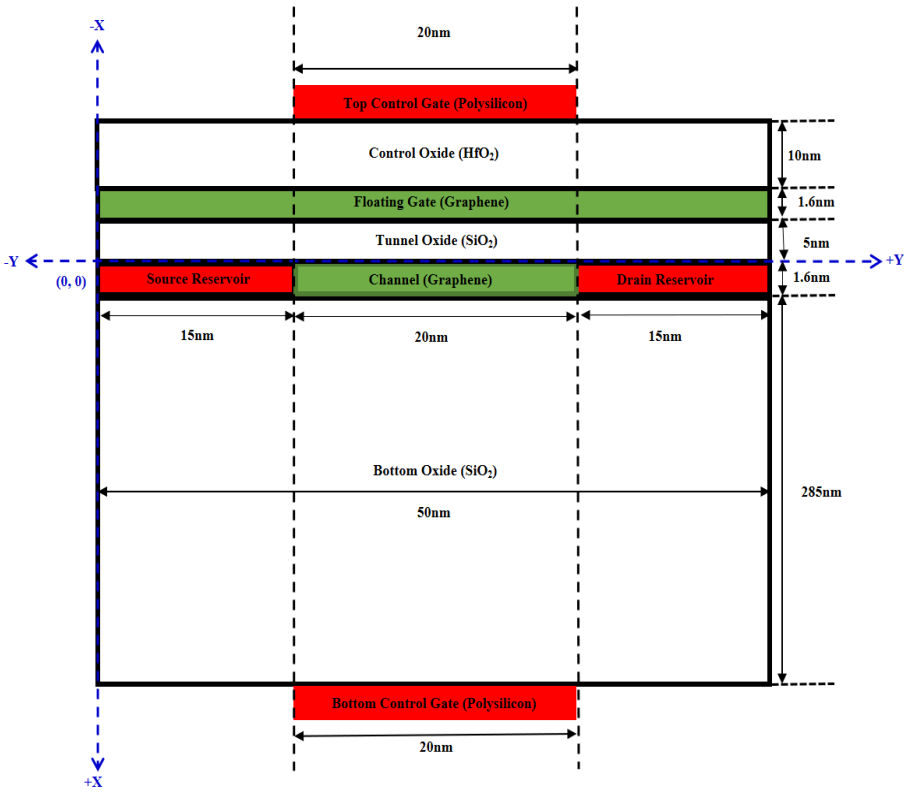


Figure 12: GFGT using HfO_2 as the top control oxide

Table 5: Erase and Program operation simulation conditions using HfO_2 as control oxide

V_{TG}	-20 V to +20 V
V_{DS}	0.5 V
V_{BG}	0 V
Temperature	300 K

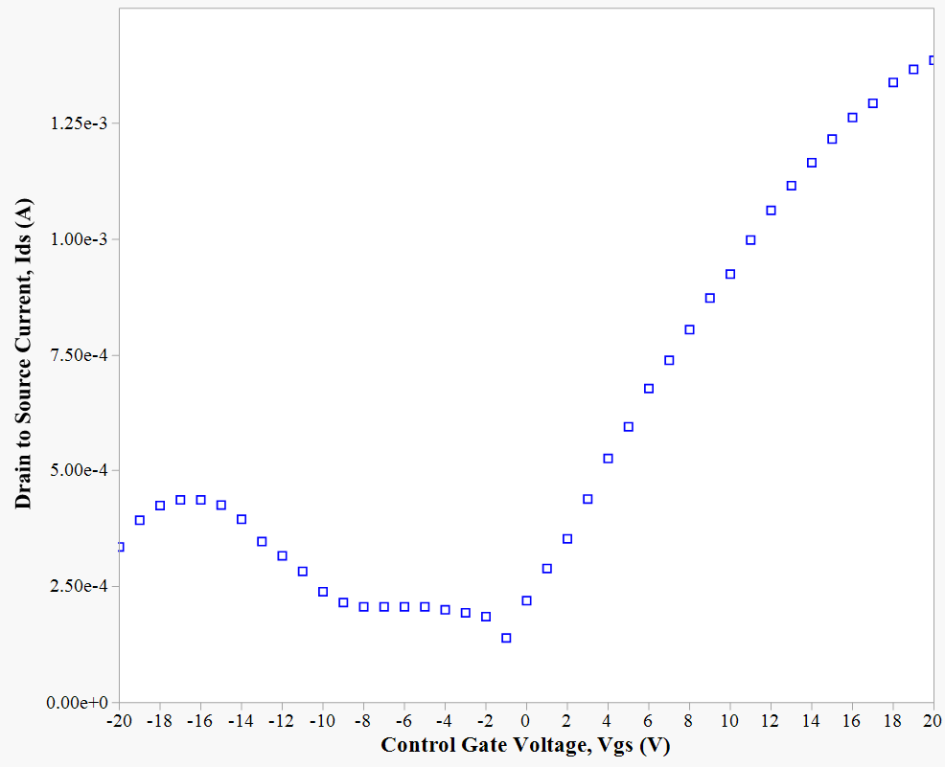


Figure 13: Erase and Program operation I_{DS} versus V_{GS} characteristic when V_{DS} = 0.5V is fixed for HfO_2 as control gate

Table 6: Read Operation simulation conditions using HfO_2 as control oxide

V_{TG}	4.5 V
V_{DS}	0 ~ 1 V
V_{BG}	0 V
Temperature	300 K

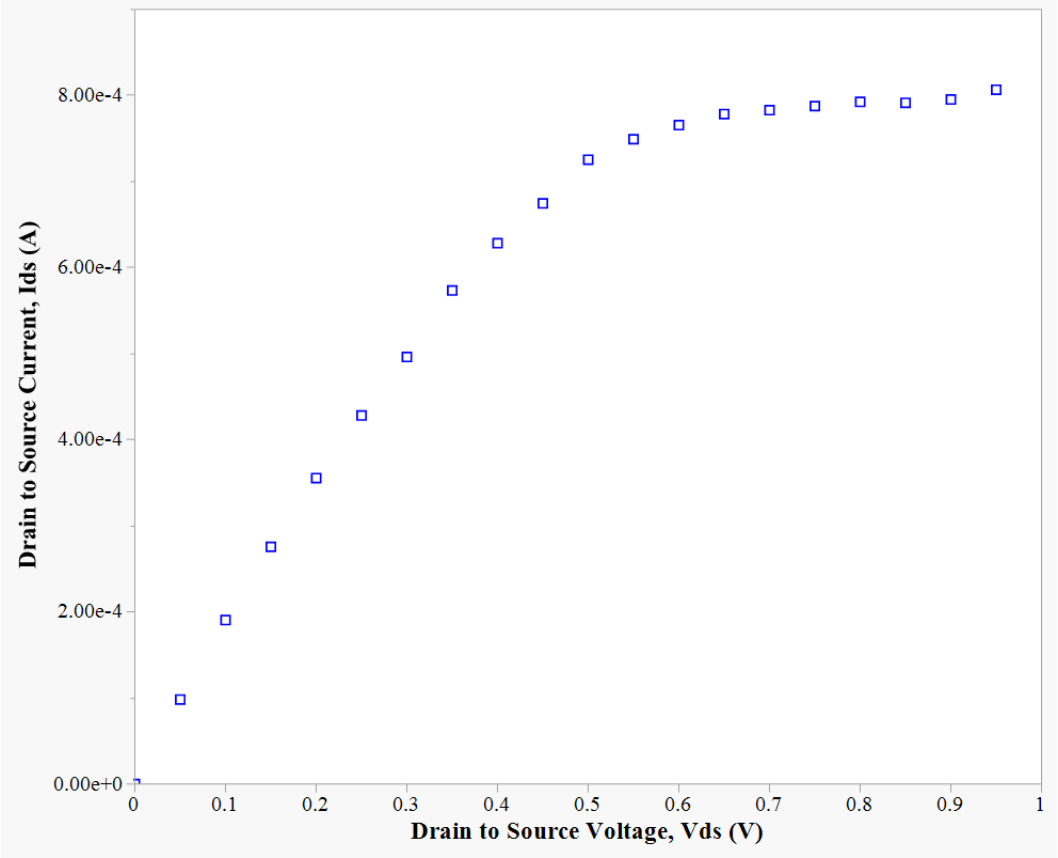


Figure 14: Read operation I_{DS} versus V_{TG} characteristic when V_{TG} = 4.5V is fixed for HfO_2 as control gate

CHAPTER 6

CONCLUSION AND FUTURE WORK

Graphene based Floating gate transistors (FGT) were successfully modeled in the proposition. The two FGT were developed using Silicon dioxide and Hafnium dioxide as the top control oxide. Hafnium dioxide having the higher dielectric constant (4-6 times higher than SiO_2), resulted in better performance compared to the device developed using SiO_2. Thus, HfO_2 is a good substitute for SiO_2, for the sub-nanometer devices.

Further, using the FGT model proposed, devices using different two-dimensional materials (MoS_2, $MoSe_2$, $MoTe_2$, WS_2) as channels for different top control oxides and tunnel oxides can be studied for much smaller, faster and reliable next-generation flash memories. Not only different materials for channel, control and tunnel oxides but, different architectures can be examined using the proposed model, such as FGT using dual control gates. The model can be improved for the top and the bottom control gate for better control over channel resulting in enhanced performance of the device.

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VITA

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List of Publications

1. Nahid Hossain, Hemanshu Shishupal, Masud Chowdhury, "Tunneling Transistor based 6T SRAM Bit Cell Circuit Design in sub-10nm Domain", Proc. of *IEEE MWSCAS, Boston, MA, USA, Aug 2017*
2. Hemanshu Shishupal, Nahid Hossain, Masud H Chowdhury, "TCAD Simulation Methodology of MLGNR Based Floating Gate Transistor Flash Memory" (in submission)