Advanced NanoDielectric Material Development and Scaling for use in Compact Ultra-High Voltage Capacitor Prototypes

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by

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The undersigned, appointed by the Dean of the Graduate School, have examined the thesis entitled:

ADVANCED NANODIELECTRIC MATERIAL DEVELOPMENT AND SCALING FOR USE IN COMPACT ULTRA-HIGH VOLTAGE CAPACITOR PROTOTYPES

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Abstract

ADVANCED NANODIELECTRIC MATERIAL DEVELOPMENT AND SCALING FOR USE IN COMPACT ULTRA-HIGH VOLTAGE CAPACITOR PROTOTYPES

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ABSTRACT

The dielectric material employed in this effort is a proprietary nanocomposite material, MU100. The material was initially developed to shrink high frequency, high voltage, dielectric loaded antennas; however, due to its unique material characteristics, the nanocomposite has shown promise in development of high voltage capacitors. Previous work has shown small-scale samples of the high permittivity nanocomposite material to have an average dielectric strength of 220 kV/cm with peak breakdown fields in excess of 328 kV/cm. When scaling up to realize application specific voltages, failure modes become more pronounced due to volume effects of the nanocomposite and field enhancement factors at the electrode dielectric interfaces. This work describes how the material was increased in volume from small samples up to compact capacitor prototypes capable of repeatable performance at 500 kV to in excess of 1 MV with lifetimes greater than 10,000 shots.

Chapter 1. Introduction

1.1 Previous Work

Capacitors are vital to the energy storage needs of nearly all pulsed power and directed energy systems being fielded today. Capacitors are a large contributor to the size and weight of a system. In order to make these systems more practical for field use, the energy storage systems must become significantly smaller and lighter. High energy density capacitor development is the forefront of this size reduction effort. The University of Missouri's Center for Physical and Power Electronics has demonstrated a significant size reduction to ultra-high voltage pulsed power capacitors using a proprietary nanoceramic, nanodielectric composite material known as MU100B.

The MU100B nanodielectric was developed to reduce the size of high power antennas using dielectric loading [1]. The material was developed to be a fully machinable nanoceramic – polymer composite to allow for fabrication of even the most sophisticated antenna geometries. The name MU100B comes from the material's high permittivity (ε_r), which is approximately 100 at high frequencies (1 GHz). In conjunction with the material's high dielectric constant, the material's dielectric characteristics are very stable with temperature (permittivity +/- 10% across a temperature range from -40 to 140 $^{\circ}$C). Due to MU100B's advantageous material properties, such as high dielectric constant, high dielectric strength, high resistivity, low temperature coefficient, and ease of machinability, the proprietary nanodielectric material has also shown promise as a medium for reducing the size of high frequency, high voltage capacitors [2], [3].

For the past few years the Center for Physical and Power Electronics at the University of Missouri has focused on the development of small scale MU100B capacitors

[4]. That development has yielded small scale capacitors with an active dielectric constant near 200 at relevant frequencies (5 – 15 MHz) with dielectric strengths of 100-250 kV/cm on average. The material, MU100B, is employed as the active dielectric material in this effort to reduce the size and weight of ultra-high voltage pulsed power capacitors.

Capacitor development by the Center for Physical and Power Electronics began with an initial 55 kV, 40 nF capacitor design with electrode radius equal to 6.35 cm [5]. When considering the dielectric properties of the original MU100B dielectric, a capacitor thickness of 0.825 cm was necessary to achieve these parameters. During the first capacitor development effort, the focus was devoted to the processing techniques of the MU100B dielectric, specifically to increase the high-voltage performance and lifetime of small-scale (2.54 cm diameter, 0.15 cm thick) MU100B-based capacitors. The material production was optimized and then evaluated for capacitor lifetime, and capacitor voltage hold-off strength.

The initial research was intended to yield base lifetime data, meaning the acquired data could ultimately be scaled to characterize the expected attributes of capacitors of differing dimensions in the future. The lifetime data tests were carried out on 0.1 – 0.2 cm thick samples of MU100B that were repetitively DC charged, and then discharged into a resistive load within a microsecond to millisecond time frame. The number of shots necessary to cause breakdown of the capacitor were recorded as the lifetime for the small scale samples. The lifetime in many cases exceeded 750,000 pulses.

While striving to increase capacitor performance, it was found the lifetime of the capacitor depends largely on the dielectric-electrode interface. Thus, improving this interface became an important part of the research effort. Initial tests were performed on

flat MU100B capacitors with electrodes fabricated by sputtering platinum through an unseated mask onto the capacitor surface. Silver-loaded epoxy was applied by hand to the platinum electrode. This initial method yielded inconsistent results, for many of the electrode parameters varied.

The second-generation electrode investigation utilized the small-scale capacitor test data to optimize the initial results and reduce the variables. The electrode fabrication process remained the same, except that the platinum layer was sputtered using a seated mask, which resulted in the electrode being centered on the capacitor face consistently.

In the third-generation of electrode fabrication, silver epoxy was sprayed onto the platinum layer. Improvements in the reproducible application of the electrodes onto the capacitors led to an increase in the capacitor lifetime [6]. Analysis of breakdown in the capacitor showed that the breakdown started at the triple point of the dielectric, electrode, and the surrounding material interface with the partial electrode configuration.

In order to eliminate the observed breakdown through the bulk of the MU100B with the partial electrode, a fourth-generation of electrode application was employed. In this generation, the electrode was applied to the entire face of the capacitor. The full electrode model extended the triple point to the edge of the dielectric disk. With this change, a substantial increase in capacitor lifetime was observed. Subsequent generations of electrode fabrication built upon the success of the fourth generation. Moreover, to reduce the cost of production, platinum was replaced with silver for the sputtered electrode material. Even though silver is known to be more reactive than platinum, no degradation in performance was observed with this material substitution [7].

Finally, endeavoring to increase the robustness of the outer electrode layer, the painted silver-loaded epoxy was replaced with electroplated copper. Additional improvements in capacitor performance were obtained with this type of electrode application. The electroplating process was refined in order to apply the copper onto only the sputtered silver electrode and is the method currently used in the small-scale capacitor fabrication process. Additionally, the electroplating process provides precise control of the application of copper, allowing the thickness of the copper electrode to be optimized for varying applications. This electrode development effort resulted in small scale capacitors (2.54 cm in diameter, 0.15 cm thick, and approximately 400 pF in capacitance) with lifetimes of over 800,000 discharges before failure when run at 80% of device maximum threshold breakdown field, which was equal to 225 kV/cm on average [4].

To begin increasing the voltage hold-off of capacitors made of the proprietary material, the thickness of the dielectric layer was increased substantially. 1 cm thick devices were fabricated before focusing on the 2 cm thick devices which were desired for an early program goal of fabricating a 250 kV capacitor.

A single capacitor was manufactured, which held off the desired 250 kV. Additional testing and evaluation of this thicker capacitor also led to further improvements in electrode design. The flat, plated copper on silver method was sufficient for the very high electric fields but did not show the same lifetime as it did with the smaller scale tests described previously. It was determined that the electric fields along the edge of the MU100B needed to be further shaped by the electrode, thus a corona shield top hat assembly was designed to be placed on top of the copper layer of the electrode. The design,

and development of the field shaping electrode is a substantial topic in this report and will be discussed in much more detail in coming chapters.

The second generation of this ultra-high voltage capacitor development effort required the prototype devices under development to have a capacitance of 130 pF and a voltage rating of 500 kV. To realize this requirement, the previously developed thicker MU100B substrate capacitors (2 cm thick) were stacked in series to increase voltage hold off capability. A novel bonding procedure of the stacked substrates was developed, adequately joining MU100B substrates through a solid equipotential layer. The bonding procedure was also applied to the field shaping electrode, which is utilized at the top and bottom of each ultra-high voltage stack. Proper stacking of 2 cm thick MU100B substrates allowed for the voltage rating requirement to be met and combining multiple stacks in parallel allowed for the capacitance rating to be achieved. Specifics of this ultra-high voltage capacitor development effort, as well as full-scale device electrostatic models and physical testing will be discussed at length in the remainder of this report.

1.2 Commercial Capacitor State of the Art

Recently there has been renewed interest in increasing the standard performance characteristics of high energy density, long lifetime, high voltage capacitors. The renewed interest is most likely due to the rapidly growing call for fieldable directed energy systems, primarily driven by the defense market. The energy storage for systems of this type (high power microwave (HPM) and some high energy laser (HEL) systems) of application is crucial for optimal performance. Often times the energy storage system, nearly always high voltage pulse discharge capacitors, are significant contributors to the systems overall size and weight. In an effort to continue making future directed energy systems lighter and more

mobile – therefore more deployable – high voltage capacitor technology is in need of a substantial size reduction. This is the driving cause behind the renewed interest in raising energy density of high voltage pulsed power capacitors.

Energy density in capacitors (U_v), as seen in the following equation, is dependent, linearly, on the relative permittivity (ε_r) of the operational dielectric material, and exponentially on the operational electric field (E).

$$U_v = \frac{1}{2}\varepsilon_0\varepsilon_r E^2 \; [J/m^3] \tag{1.1}$$

That being the case, the density of capacitive energy storage can be increased at a much faster rate with incremental improvements in capacitor operational voltage, opposed to relative permittivity increases. However, when the ultimate energy density is desired, improving the relative permittivity should not be overlooked, as is the case in polymer-ceramic composite material development where the high dielectric strength of a polymer material is coupled with the high relative permittivity of a ceramic in an effort to improve energy density by both means. When developing a novel capacitor with intentions of shrinking the state of the art at very high voltages, using a new proprietary nanoceramic-polymer composite material, it is important to know just where the state of the art lies for the two types of materials employed.

1.2.1 Polymer Film Commercial Capacitor State of the Art

Polymer film capacitors, as their name implies, employ moderate dielectric constant (ε_r ranging from 3-5) polymer materials as the dielectric, most commonly polypropylene, mylar, and polyvinylidene fluoride. In capacitor applications, huge surface areas of the polymer are needed to achieve appreciable capacitance. Further, the dielectric strength of most polymers is exceptionally high, enabling the large surface areas to be

spread as thin films opposed to thick sheets. When fabricating high voltage polymer film capacitors, the general idea is: electrode layers, separated by dielectric film layers which are wound around a mandrel to form a large surface area capacitor with a high form factor. Those wound capacitors can be used individually or joined together in series to achieve higher operating voltages or joined in parallel to increase total capacitance.

The high voltage pulsed discharge capacitor market consists of many companies. Innovations in the commercial sector of the market are made by specialized companies like General Atomics (capacitor group formerly known as Maxwell Laboratories) and Aerovox to name a few. From the High Voltage Capacitor brochure available on the General Atomics website, high voltage polymer film capacitors are currently being manufactured over a wide range of specifications, ranging from 100 mF at 1 kV to 10's of pF at 2 MV [8]. As seen in Figure 1.1, the capacitor line most relevant to this development (very high voltage) is the plastic case series (shown as the yellow points in the figure).

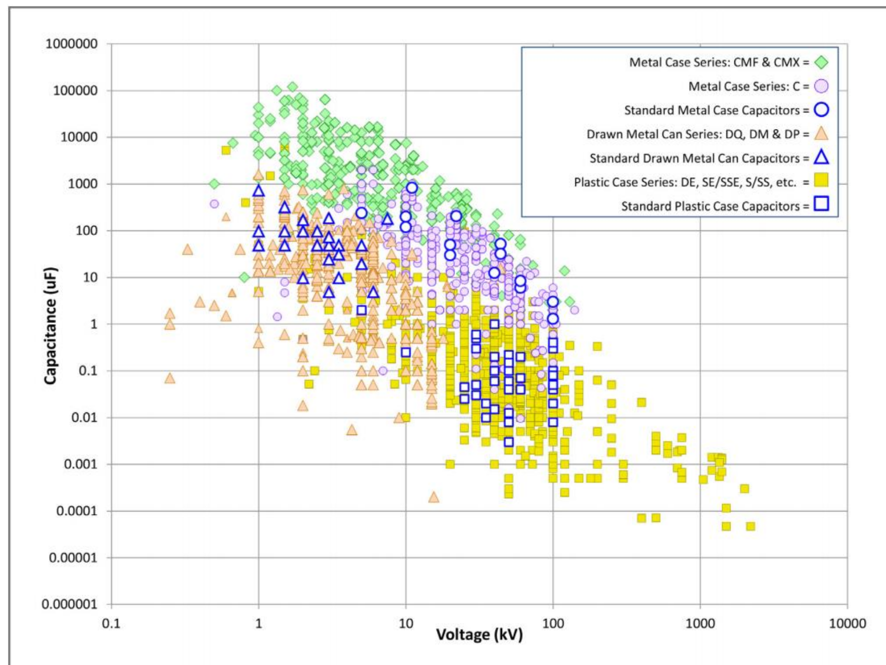

Figure 1.1: Commercially available high voltage polymer film capacitors. Devices capable of operation well above 100 kV are of most relevance to the scope of this report.

The highest voltage capacitors (500 kV plus) in the plastic case series are termed "very high voltage capacitors" by the manufacturer and due to smaller demand and export controls, little information is publicly available on such devices. It is therefore assumed that size, fabrication, and lifetime characteristics will be scaled up versions (more windings in series) of the lower (100 kV max) voltage plastic case series capacitors. The highest voltage rating of an in-stock catalog plastic case series capacitor is 100 kV [9]. This capacitor has a capacitance of 40 nF, and a rated lifetime of $3x10^4$ charge/discharge cycles at 20% voltage reversal.

It is known that polymer film capacitors performance under voltage reversal is less than ideal [10]. Lifetimes of polymer devices drop sharply after a threshold of increasing voltage reversal [11]. The effect of voltage reversal on pulsed discharge capacitors is small below 20%. Increasing voltage reversal induces different failure modes into the dielectric material and capacitor geometry. The multitude of polymer materials and varying geometries employed in polymer capacitor designs makes each device respond to voltage reversal differently. Therefore, a spread in lifetime degradation as percent voltage reversal is increased is seen. The range at which lifetime is affected by voltage reversal is shown in Figure 1.2 [11]. When operation at large voltage reversal is required, polymer film capacitor lifetime is drastically reduced. For example, an application requires long lifetime operation at 60% voltage reversal, the rated lifetime of a polymer capacitor will be reduced to somewhere around 3% (shown in Figure 1.2) of its rated lifetime at rated voltage. Taking that into account, the 30,000 shot lifetime of the aforementioned General Atomics plastic case capacitor would be reduced to approximately 900 discharges.

One could assume that the higher voltage capacitors of the same series would have similar lifetime specifications. Thus, the same effects would be seen in systems desiring high energy density by means of operating at larger voltages. Therefore, the state of the art of polymer film capacitors is that they are very widely manufactured, the most widely manufactured pulsed discharge capacitor by far. Long time fabrication has led to many varying designs allowing a wide specification range to be met, as far as capacitance rating and voltage levels are concerned. The advent of metalized film, self-healing technology, has enabled an increase in device energy densities by being able to run self-healing capacitors much closer to their average dielectric breakdown field at long lifetimes. However, the draw back to polymer film is a limited tolerance for non-ideal pulse shapes and temperatures, limiting viability in specific directed energy applications. In many such cases the self-healing capacitors have lifetimes of less than 1000 pulses, making them not useful for repetitive operation.

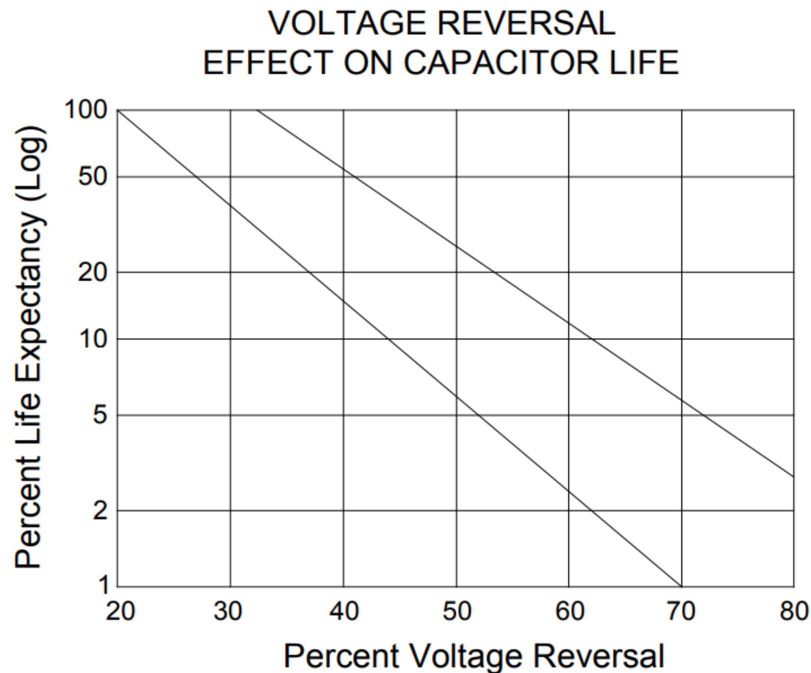

Figure 1.2: Percentage of rated life expectancy of typical polymer film capacitors as affected by percent of voltage reversal subjected to the device.

1.2.2 High Voltage Ceramic Capacitor State of the Art

High voltage ceramic capacitors are a much less mature technology than their polymer-based counterparts. The most common application of ceramic based capacitors is packing large capacitance value in minimal space at low voltages; generally, for integrated circuit type regimes. Ceramic lends itself very well to small packages at low voltages because the high dielectric constant of most perovskite ceramics allows large capacitance values to be attained in much smaller packages than traditional insulators but at lower operating voltages because of the material's inherently lower dielectric strength. Therefore, the maximum operational voltages attainable by commercially available purely ceramic high voltage capacitors is roughly 10-100 times less than that of the highest voltage commercially available polymer film capacitors.

Ceramic capacitors low dielectric strength can be accounted for by understanding how the bulk ceramic is manufactured. A ceramic disk is made by joining various particles, in the form of a powder, by mechanical pressing in a die, resulting in disks of a certain thickness. The disks are then sintered at very high temperatures to get the particles to meld together. After cooling, the disks have electrodes applied to each of the two faces, resulting in a capacitor. Incomplete reconciliation of particle grain boundaries, or insufficient void removal will lead to premature dielectric failure in ceramics, as the boundaries and voids are generally filled with air.

The largest market for ceramic capacitors is for the low voltage, integrated circuit, industry. However, there is a rapidly growing sector of the ceramic capacitor industry focused on high voltage (greater than 1 kV in this case) devices. This is being enabled by further research into particle mixes and manufacturing methods enabling improved dielectric strengths at larger volumes. Commonly, the maximum operational voltage

available in the current market is approximately 50 kV [12]. Operational voltage of current high voltage ceramic capacitors is limited by how large of ceramic disk can be manufactured with high quality. If higher voltages are required out of ceramic dielectrics, stacking of the devices must be employed, which increases cost rapidly.

The large dielectric constants (typically ε_r in the range of 2000 – 5000) at work in ceramic capacitors will generally result in those devices being considerably smaller than those made of polymer film, when capacitance and voltage ratings are equal [13]. Since the size of the device is smaller, the self-inductance of ceramic devices is often times smaller than other capacitors on the market as well. The lower inductance allows for higher frequency operation and faster rise times in a discharge application.

Different than polymer film capacitors, ceramic dielectric performance is degraded less by the voltage reversal of a subjected pulse [14]. However, the dielectric properties of common ceramics are known to vary largely with the magnitude of applied voltage and operational temperature [15] [5]. Therefore, the capacitance of a ceramic capacitor can very up to 30 – 40% according to their service environment, be it applied voltage level or their operational temperature. The market leader in production of the highest voltage ceramic capacitors shows how the permittivity of devices can change with applied voltage and operational temperature, Figure 1.3 [12].

If the voltage level of an application is not exceeding several 10's of kV, and conserving space is of importance the current state of high voltage ceramic capacitors would fit that requirement perfectly. However, if the requirement is to store large amounts of energy at very high voltages, or have very stable capacitance values, regardless of

operational parameters, the commercial state of the art, as it pertains to ceramic capacitors, is not mature yet.

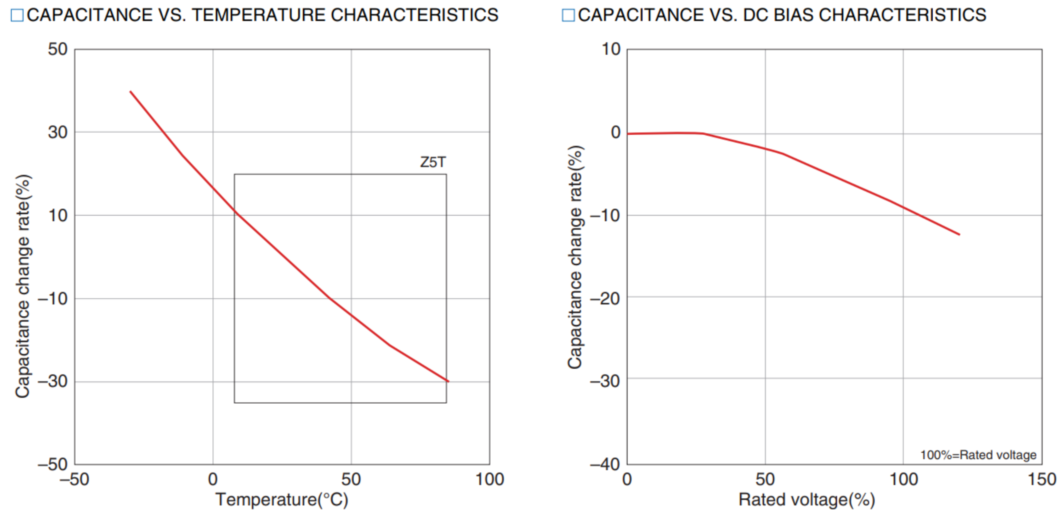

Figure 1.3: The operational dependencies of available commercial high voltage ceramic capacitors are shown. Ceramic's dielectric constant dependence on temperature is substantial and is shown at the left. Whereas the dependence on applied voltage is shown in the right graph.

The pros and cons of each capacitor type have been presented, and it should be obvious that both material types have desirable qualities to the pulsed power and high voltage industries. Commercially available polymer film capacitors can handle very high voltages reliably. They have more constant capacitance values across all operating conditions. Commercially available ceramic capacitors are generally smaller and less inductive than their counterparts, in addition to tolerating voltage reversal marginally better. Thus, if a single dielectric material could harness the qualities of both materials (the voltage handling of the polymer with the space saving high dielectric constant of the ceramic) and employ that into a functional device, the current state of the art could be substantially surpassed. An undertaking such as that will be described in the remainder of this thesis based on our experiments with MU100B.

1.3 Scope and Goals of Research

The primary focus of this research is to use the advanced MU100B ceramic nanocomposite to design, fabricate, and test fully functional ultra-high voltage (voltage ratings 500 kV - >1 MV) capacitor prototypes that are several times smaller than what is available in the commercial state of the art. This was attained through further advancements in the development of the MU100B nanocomposite material, primarily in the stabilization of the material manufacturing processes, generating a more consistent and high-quality final product. Finally, advanced simulation and design methods allowed for engineering of sophisticated capacitor electrode designs as well as assembly methods to realize functional ultra-high voltage capacitor prototypes.

As shown in section 1.2, there has been a renewed interest in the field of high voltage and high energy density capacitors, which has led to advancements in the state of the art. The primary advancements have been in increasing operational voltages while reducing overall size. Smaller high voltage capacitors have great potential for uses in many DC and pulsed power applications such as with, radar, laser, and directed energy systems, as well as smaller applications like defibrillators and medical x-ray machines to name a few [16] [17] [18]. However, the current state-of-the-art technologies for these applications are still rather bulky and environmentally unstable for ideal operation. A specific problem for the pulsed power and directed energy industries is this new generation of capacitors must have low losses and low self-inductances enabling very fast discharge times (picosecond-microseconds), all the while remaining stable across a myriad of environmental conditions as directed energy systems are fielded outside of the laboratory.

The method utilized by the University of Missouri to address this problem is the use of ceramic nanoparticles suspended in a polymer matrix as opposed to the more

traditional use of only polymeric or ceramic dielectrics [19] [20].What makes these nanocomposite materials ideal for high-energy density applications is that, ideally, they can blend the high-dielectric constants of ceramics with the high-dielectric strengths of the polymers into one material.

This project was approached as a balancing act between improving and stabilizing the MU100B material (raising the relative permittivity while maintaining the dielectric strength) and employing advanced capacitor design and fabrication methods to aid in nanocomposite material performance in ultra-high voltage capacitor applications [21]. While materials with high relative permittivity exist, and materials with high dielectric strengths also exist, very few materials display both properties simultaneously [22]. The operational fields required to use these materials in high voltage capacitor applications are so large, advanced electrode topologies (spreading of the electric fields at electrode edges) must be investigated and employed [23]. The research will focus on the aforementioned as summarized by these goals:

1) Continue to develop the high-dielectric constant nanocomposite material, MU100B, with the following focus:
    a) Improve dielectric constant of material by 50% at frequencies of interest (1-15 MHz)
    b) Maintain dielectric strength in thick substrates (~2 cm thick) to a minimum of 100 kV/cm
    c) Stabilize production processes, increasing material production yield to 90%
2) Characterize and inspect the material's and initial prototype capacitor's dielectric properties and performance with the following methods:

a) Dielectric spectroscopy

b) High-voltage capacitive discharge

c) Pulsed dielectric strength testing

d) Scanning electron microscopy

e) 3D electrostatic simulations

3) Design, Fabricate, and Deliver two long lifetime (10^4 pulses) 130 pF, 500 kV capacitors capable of repeatable performance with a 50-80% voltage reversal.

   a) Test material and devices past minimum requirements.

   b) Use test data to reevaluate designs and supply additional, redesigned, test devices if necessary.

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Chapter 2. Theory

2.1 Barium Titanate

2.1.1 Characteristics of Perovskite Materials

Scientists and engineers have known of a class of materials that exhibit extraordinarily high relative permittivity known as perovskite ceramics. These perovskites share the same crystalline structure as calcium titanate ($CaTiO_3$) [1], seen in Figure 2.1. Many common oxides take on this structure and have a chemical formula ABO_3, where A and B represent the cations with oxygen serving as the anion of the oxide. These crystal structures can display several symmetries: hexagonal, cubic, orthorhombic, tetragonal or rhombohedral, all of which have the potential to manifest different physical properties. Some of these symmetries can produce stable electric dipoles resulting in strong ferroelectric effects. While these materials generally display relatively high dielectric constants, their dielectric strength tends to be inadequate for most applications as they are prone to failure along grain boundaries within the ceramic's internal structure.

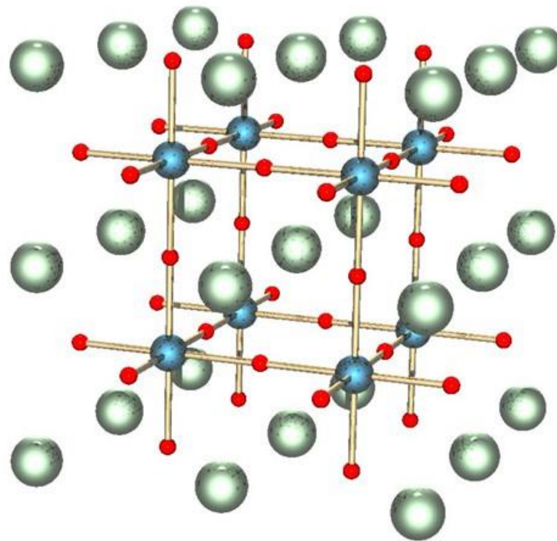

Figure 2.1: Crystalline structure of a general perovskite ceramics. Red represents oxygen atoms, blue represents cations (usually a smaller metal), and green represents the anions (usually a larger group II metal.

Barium titanate ($BaTiO_3$) is a commonly available perovskite material and is an important material in the field of electroceramics due to its good electrical characteristics. Depending on the crystalline structure of the barium titanate, the material can display photorefractive effects as well as piezoelectric properties [2]. It possesses a high dielectric constant and low losses. The values of the dielectric constant depend on the purity, density and grain size of the barium titanate. Dielectric properties also are dependent on temperature, frequency, and dopants. The temperature dependence of the dielectric constant can be seen in Figure 2.2. Many companies, including TDK, utilize doped strontium titanate in the production of capacitors. However, the University of Missouri has been able to develop a nanocomposite material composed principally of chemically pure barium titanate, which will have a higher dielectric constant than its doped counterpart.

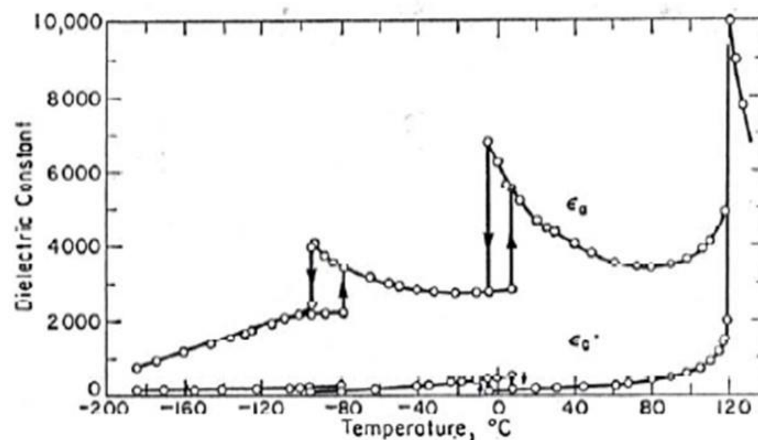

Figure 2.2: Dielectric constants of sintered BaTiO3 crystals as a function of temperature [3].

2.1.2 Dipole Moments and Their Effect on the Electric Properties of Barium Titanate

Barium titanate has been of interest to the scientific community due to its interesting ferroelectric properties. Ferroelectricity is the spontaneous alignment of electric dipoles by their mutual interactions. In 1912 Debye postulated the existence of permanent electric dipoles [4]. It was theorized that these dipoles would occur when atoms of different

electron affinities are formed into molecules. The differing electron affinities of the constituent atoms forming the molecule would cause the electron cloud to congregate near the stronger binding atoms. When these dipoles are placed in an external field, they will experience a torque which will force them to align with the field.

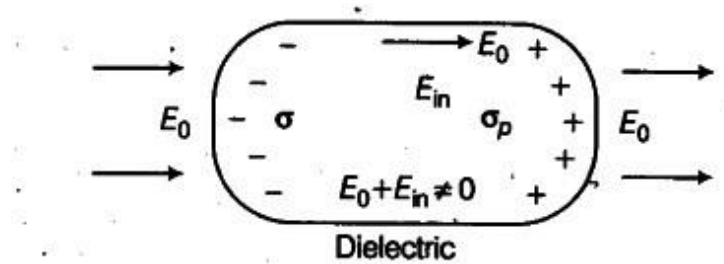

Figure 2.3: Sketch depicting the spontaneous formation of an electric dipole in an external electric field.

Figure 2.3, depicts an intrinsically unpolarized piece of dielectric becoming spontaneously polarized in the presence of an external electric field. The free dipole ends of the outer material wall would then contribute to the orienting field at the center of the dielectric as, $\frac{P}{3\varepsilon_o}$. By neglecting any other contributions from the internals of the dielectric you can arrive at the Mosotti expression, shown below for the local field [5],

$$E' = E + \frac{P}{3\varepsilon_0} \quad [V/m] \tag{2.1}$$

Where E' is the microscopic local field, E is the external electric field, and P is the polarization. This can result in an electric field that increases the polarization of the dipole, and the polarization in turn will increase the microscopic electric field. Thermal agitation keeps this phenomenon from having runaway effects, unless a critical temperature is reached at which point the dipoles electric susceptibility will approach infinity.

A. Von Hippel elaborates why this effect is of interest, especially when considering perovskite materials such as barium titanate [6]. It is the vibrational modes of the titanium

(Ti) against the oxygen (O) ions which allow barium titanate to have such a high dielectric when it is in a single crystalline form. However, barium titanate does not contain any permanent dipole moments, and if it did, they would be effectively locked in the orientation of the overall structure.

The Center for Physical and Power Electronics has cleverly engineered a solution to this problem. By suspending barium titanate particles in a rigid polymer matrix a randomly oriented crystalline structure is produced. Because individual crystalline structures are physically, not electrically, isolated from one another, when an external electric field is applied the domains can react individually rather than as a single structure. This allows polarization to have a greater effect on the entire structure, effectively increasing the local field. This idea of barium titanate nanoparticles aligning with external electric fields to self-organize is corroborated through the work at the Max-Planck-Institute of Colloids and Interfaces in Germany [7].

2.2 Nano Ceramic Dielectrics

2.2.1 Multi-Modal Particle Distributions

By increasing the density of the nanoceramic composite, it is possible to increase the permittivity and dielectric strength of the material. Fiebig shows that the effective permittivity of a composite material is equal to the weighted sum of the logarithm of the permittivity for each separate material comprising the composite [8],

$$\varepsilon_{eff} = \prod_{n=1}^{N} {\varepsilon_n}^{\alpha_n} \quad (2.2)$$

where α_n is the percentage the given material makes up.

However, a simple experiment of putting spherical objects in a volume will show there is a flaw with using one size of particle for this method: the introduction of space

devoid of particles. These regions where the relatively high permittivity particles do not exist will lower the effective permittivity of the composite as a whole. It was then theorized by Furnas [9] [10] that using multiple particle sizes would enable these holes to be adequately filled reducing their effect on the permittivity of the composite, approaching a limit of a solid material. These models were later verified though Andereggs experiments [11]. Through analysis using the mathematical models developed by Furnas, the following graphs were produced showing the volume percentage of voids versus the ratio of particle sizes when the particles have 40%, Figure 2.4, and 30%, Figure 2.5, voids in a 1:1 ratio of large particle size to small particle size respectively [12].

For Figure 2.4 and Figure 2.5, a realistic ratio of the size of the largest particle to the smallest particle is 1000:1. This ratio corresponds with the difference between particles on the size of μm and nm respectively, both particle sizes that are commonly available. Thus, it can be seen that when there are initially 40% voids by volume for a 1:1 mixture, using a ternary mixture the total voids in the composite can be reduced to 10%. For 30% voids by volume for a 1:1 mixture, using a ternary mixture the total voids in the composite can be reduced to slightly above 5% with a 1000:1 size differential between the largest and smallest particle size. This ratio could be increased further; however, the returns start to diminish. For a ternary mixture, the maximum packing density is 95%. This is in comparison to a binary packing distribution that has a theoretical maximum packing density of 86% [13].

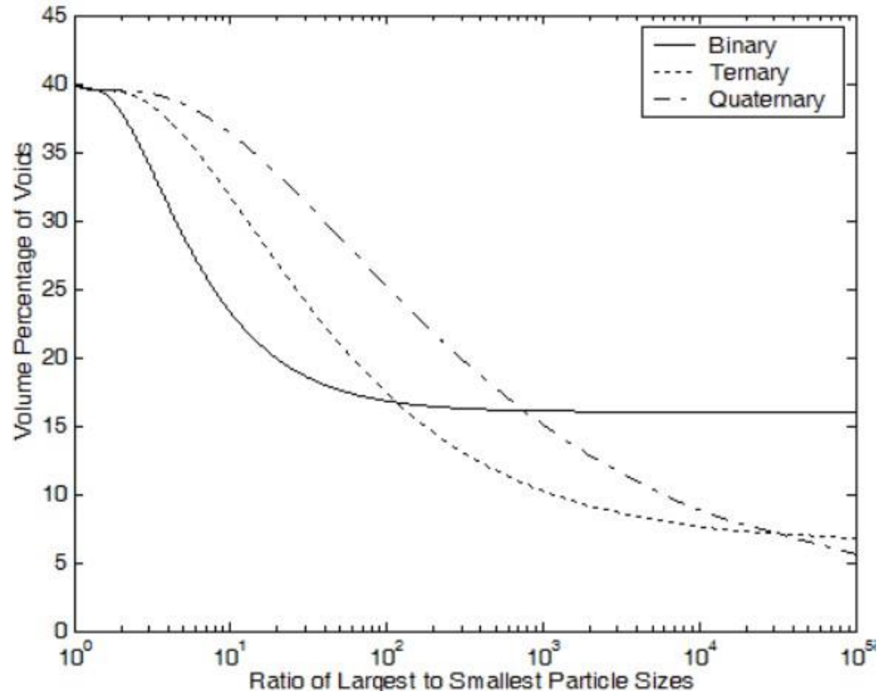

Figure 2.4: Graph depicting the volume percentage of voids versus the ratio of particle sizes for particles with 40% voids in a packed bed of each size for binary, ternary, and quaternary mixtures [12].

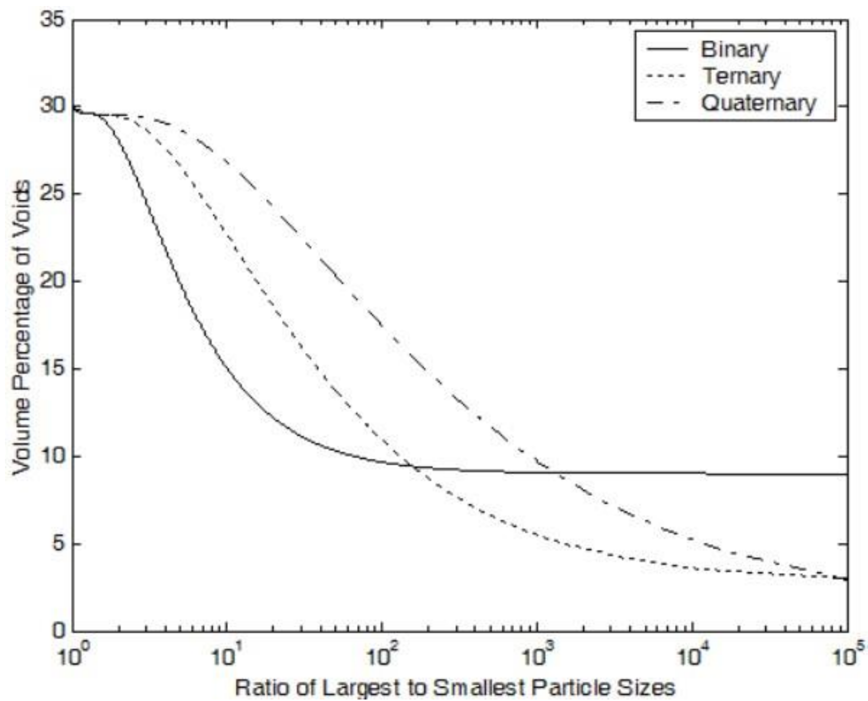

Figure 2.5: Graph depicting the volume percentage of voids versus the ratio of particle sizes for particles with 30% voids in a packed bed of each size for binary, ternary, and quaternary mixtures [12].

2.2.2 Effect of Voids on Electrical Performance

The presence of voids (in this case, areas devoid of nanocomposite materials, or pockets in the encapsulant in which all air was unable to escape) within a composite, or any surrounding material can significantly degrade the performance of the device through the potential for premature dielectric breakdown. Since voids are typically assumed to be filled with air, or other similarly dielectrically weak gasses, the breakdown voltages of voids can be substantially lower than the constituent materials. That issue gets compounded due to the concentration of electric fields in a void. In a simple model of the electric field distribution between a void and the surrounding high dielectric constant material in which a layer made up of the void and a layer consisting of the high dielectric material form the volume of a capacitor, a serial combination of capacitive layers is effectively formed, and can be modeled with the following equivalent circuit from [14].

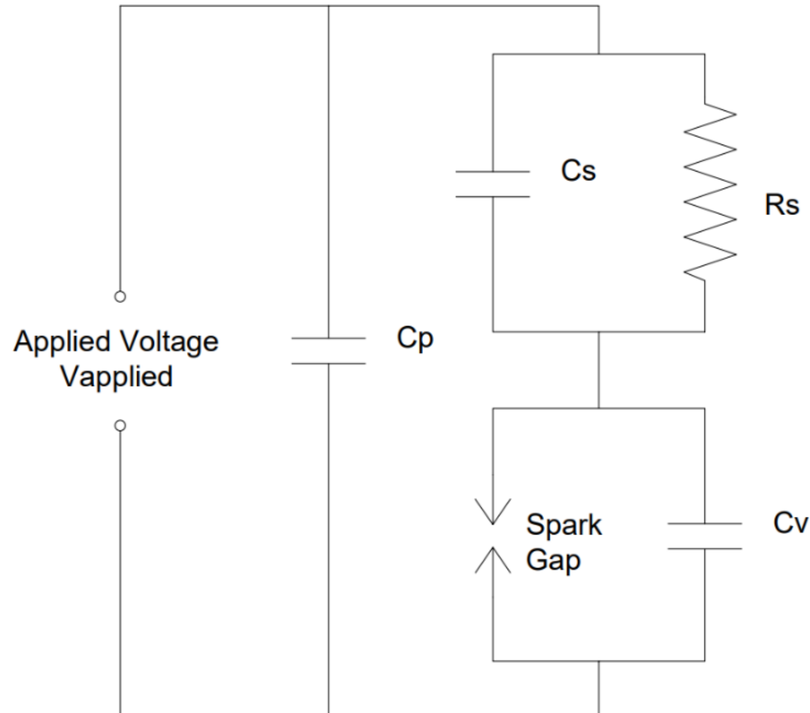

Figure 2.6: Equivalent circuit model of a void in an insulating material matrix. The capacitance formed by the void is shown as Cv and is charged through a series connection of the insulating material above it and in parallel with the rest of the void free material [14].

Where the void is represented by a capacitor, C_v, in parallel with a spark gap which discharges, at least partially, when the voltage across it exceeds the breakdown inception voltage of the void (which depends on material present in the void as well as void shape). The void capacitance must be charged through the insulation in series with it, which is represented in the void equivalent circuit as a parallel combination of capacitor, C_s, and resistor, R_s, as shown in Figure 2.6. The remainder of the void free insulation can be represented by a parallel capacitor, C_p. Usually the size and location of the void forces the values of the three capacitances to behave like this: $C_s \ll C_v \ll C_p$. Thus, the voltage across the void capacitance can be modeled by the following equation:

$$V_v = V_{applied} \frac{C_s}{C_v + C_s} \tag{2.3}$$

Where V_v is the voltage across the void capacitance, and $V_{applied}$ is the voltage across the entire device. Therefore, when V_v exceeds the breakdown voltage of the gaseous material in the void, the void will breakdown according to Paschen's law when the field enhancement factors of the void are accounted for [15]. Since voids are essentially random in formation, shapes can vary widely and, often times, the field enhancement factors present in a void are very high, making even small voltages across the void capacitance susceptible to causing void breakdown. Void breakdowns can trigger surrounding material breakdowns if the void breakdown results in high enough energy electrons to continue the breakdown avalanche into the surrounding material.

The inability to mitigate voids from a nanocomposite dielectric material, or any surrounding material, can greatly perturb dielectric breakdown performance as well as considerably lower the material permittivity, as the material making up the void (usually air) has a very low dielectric constant, ~1. Care must be exercised when manufacturing the

nanocomposite material to ensure void free, or void minimal production, and vacuum outgassing of encapsulant epoxies is crucial for reliable nanocomposite capacitor performance.

2.3 Electrical Breakdown Mechanisms in Solid Insulators

The methods of electrical breakdown in solid insulators are many, and the nature of electrical breakdown in general is statistical in nature, meaning that a number of causes all have a finite probability of causing a breakdown at a given time [16] [17]. However, various materials do have preferred, or higher probabilities of certain methods initiating breakdown in a specific material. Purely electrical breakdown causing mechanisms, generally present when short duration voltage pulses are the cause of dielectric failure (reducing thermal heating and mechanical stress effects), can be thought of in two means: microscopic and macroscopic. Microscopic causes of dielectric breakdown in which free charge carriers get injected into the insulating material through the electrodes, can lead to the formation of conductive channels within the dielectric matrix [18]. Macroscale causes of breakdown are generally related to volume related defects in a material, such as voids in the material, or grain boundaries between insulating matrices [19].

2.3.1 Electrical Breakdown Mechanisms of Polymers

Electrical breakdown in polymers can be caused by a number of issues, macroscopic or microscopic, but what is most commonly the cause of failure in high quality insulating polymer films is phenomena present on the microscale. The dielectric breakdown strength of most polymers is so high, often times approaching 1 GV/m (10,000 kV/cm), that the typical fast electron collision avalanche, similar to the Townsend discharge in gases, cannot begin without very high local field enhanced regions being

present. These internally very high local fields are caused by phenomena on the microscale [20]. The microscale processes include surface charge injection from the electrodes as in Schottky Injection, and/or, under very high field stresses, electron tunneling, such as Fowler-Nordheim Injection [20]. When charge carriers are injected into the insulating medium they can form conducting filaments [21] [22], and/or spark the formation of electrical trees [14]. The tips of these space charge formed filaments will be needle like, bringing about large local electric field enhancements, which will cause the filament to grow faster until it is an uncontrolled run away [23] [24] [25] [26].

Polymers, like all solid materials are known to lose dielectric strength according to an inverse power law as volume of the medium is increased, mentioned in detail in chapter 5 [27]. The processes mentioned above will consequently speed up with increasing dielectric volume because larger electrode areas will have higher possibilities for irregularities in the electrode-dielectric interface, speeding up the space charge injection rate [28]. Irregularities in the dielectric-electrode interface known to initiate charge injection are rough points of the electrode forming field enhancements in the dielectric, electrode adhesion issues caused by surface roughness, and current density hot spots due to non-uniform electrode thickness [29]. Also, as dielectric substrates become thicker, the electrical effects of the opposing electrode will become less predominant, allowing the injected charges more freedom to migrate through the matrix, as well as more freedom to clump together with other charge carriers, aiding in the formation of charge conducting filaments or trees [30].

Another factor effecting the breakdown strength levels of polymers, which is crucial to the fielding of pulsed power systems, is temperature. Most dielectric polymers

have a breakdown strength that is reasonably constant (+/- 20%) with temperature up to a critical point, generally near room temperature, but will vary for each polymer, at which breakdown strength decreases strongly [31]. The temperature relationship with breakdown strength can be seen in Figure 2.7, and lends support to the described breakdown initiation theory, as free carrier mobility increases with temperature [31].

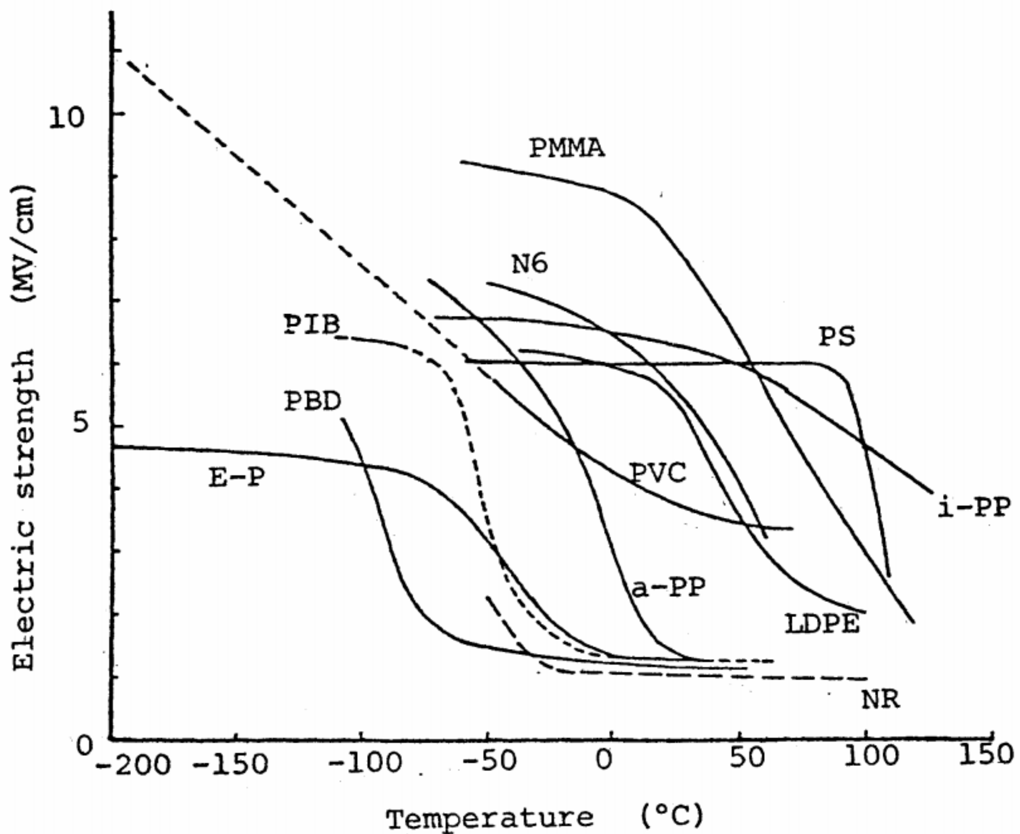

Figure 2.7: Temperature dependence of dielectric strength of many common polymers [31].

2.3.2 Electrical Breakdown Mechanisms of Ceramics

Like other materials, at any time, any breakdown mechanism can lead to failure in pure ceramics, but the predominant mechanism at work in ceramic are those at work in the macroscale. The physical make up of most ceramic materials makes these macroscale mechanical issues the leading cause of dielectric breakdown. Since bulk ceramic materials are generally fabricated using a pressing and sintering process of individual particles

varying in both size and shape, the possibility for substantial grain boundaries, occlusions, and/or voids in the ceramic matrix is high. Macroscopic material inconsistencies such as those will cause electric fields throughout the material to not be uniform. Having an air void within a high dielectric constant material, such as a perovskite ceramic, will cause the electric fields through the void to be several times higher than what is present in the higher dielectric constant material [32]. These enhanced fields, when brought near the surrounding material can then excite electrons. Once sufficient electron energy is reached, free electrons will begin to move through the material defects, colliding with static atoms, and if they attain high enough kinetic energy, knocking free additional electrons. This process is commonly referred to as a breakdown avalanche, as one high energy electron collides with and subsequently ionizes an atom, freeing additional electrons which free further electrons with successive collisions [33]. This process can grow at very large rates leading to an uncontrolled runaway of free high energy electrons, which will short out the insulating material [27]. Thus, increasing the physical size of insulating materials will increase dielectric breakdown susceptibility. Larger material volume increases the possibility for a material defect initiating a breakdown avalanche [34] [35] [28] [36].

2.3.3 Electrical Breakdown Mechanisms of Polymer-Ceramic Composites

It is known that polymer-ceramic composite materials are of interest because they can combine the large dielectric strength of polymers with the high dielectric constant of ceramics, however when composite materials fail electrically what is the primary cause? Since breakdown is statistical in nature it can be reasoned that both breakdown initiating processes, microscale and macroscale, have a closer to equal probability of contributing to failure, rather than a single dominating realm.

Further research into the physics behind breakdown in both ceramic and polymer insulators suggests the cause of breakdown to be both the microscale and macroscale factors mentioned above [14] [22] [37] [31]. It is theorized that a possible breakdown mechanism in highly packed, highly developed polymer-nanoceramics, such as MU100B is initiated on the microscopic level but finishes with a macroscopic process, for example, an avalanche breakdown. The pre breakdown conduction in an advanced nanocomposite material is initiated by a space charge limited conduction process where space charge is injected through the electrode into the nanocomposite matrix [38]. Once injected, charge carriers are trapped in the insulator and may form conducting filaments. The sharp tips of these conducting filaments coupled with the sharp tips of the ceramic filler particle, will have an inherently large field enhancement factor, making the peak electric field within the insulator several times larger than normal, which can then trigger the more well understood avalanche breakdown in a void in the material or a weakened fracture of the insulating matrix [14]. Thus, the breakdown process inherent to highly specialized dielectric polymer-nanoceramic composites is dependent on both microscopic effects (space charge injected in to the insulator from the electrodes) and macroscopic defects which can allow a breakdown avalanche to initiate and travel more readily.

Each of those process can contribute to a reduced dielectric strength as the dielectric size is increased. Space charge, once injected, is more free to move around the insulating matrix when the oppositely charged electrode is farther away, and as the dielectric material becomes more thick, the volume dependent defects e.g. voids and mechanical instabilities have a greater probability of appearing.

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Chapter 3. Material Synthesis and Testing Material Preparation

The preparation of MU100B nanocomposite capacitors is done entirely by the University of Missouri, except for the chemical production of the barium titanate (BaTiO3). Large crystals of barium titanate are received from an industrial manufacturer and then crushed into fine powders. From, this step the powders are wet-pressed into pellets and sintered under proprietary conditions intended to increase the density of the material as well as the uniformity of the crystal structure. Once sintered, the pellets are crushed again and then classified into sizes corresponding with the trimodal distribution discussed previously in section 2.2. For the capacitor applications, a high density of barium titanate is desired, a trimodal distribution can help increase the density of barium titanate within a prepared sample.

A binder solution is added to the mixture of the separated particles, where upon it is mixed thoroughly until all of the particles are wet. This nanocomposite mixture is then loaded into a die and pressed with a proprietary scheme. During this period, the binder solution begins to polymerize around individual nanoparticles of barium titanate. Once sufficiently pressed, the newly formed disk is removed from the die and placed in a vacuum oven where it is baked under vacuum for a length of time until out gassing of the nanocomposite material has been allowed to occur.

3.1 MU100B Disk Preparation

After test samples have been sufficiently out gassed and cooled, the raw MU100B disks are prepared for electrode application. This preparation process encompasses making sure the disk in question is the desired thickness and the faces of the puck are polished

sufficiently. Reaching the desired thickness is accomplished by careful hand sanding with a coarse grit sand paper (generally 220 grit). Sanding is done on certified flat granite surface plates to ensure the faces of the cylindrical disks remain entirely flat and parallel with one another. Once the desired thickness is attained the faces are polished to a uniform surface, free of any defects and glossy to the naked eye. The polishing process is done by stepping up the grit of sand paper from 400 grit sand paper to 12,000 grit optical polishing paper. The polishing process is also done on the granite surface plate to further ensure the faces remain parallel. Attaining a very uniform, smooth surface on the nanocomposite is crucial for good capacitor performance. If the surface of the dielectric is too rough, space charge injection can occur at increased levels from the jagged field enhancement points after the electrode is applied, leading to premature device failure by means described in section 2.3.3.

3.2 Electrode Deposition

When samples have been sanded and polished to the desired size the electrodes are then applied to the sample nanocomposite disk. Due to the evolution and adaptation of the electrode application process, several generations of electrode materials were evaluated and tested: generation 1, a non-masked 1.905 cm diameter silver (Ag) loaded epoxy; generation 2, a masked 1.905 cm diameter silver-loaded epoxy; generation 3, a full disk radius silver-loaded epoxy electrode and generation 4, electroplated copper (Cu). Electrode generations 2, 3 and 4 are pictured in Figure 3.1.

Figure 3.1: Comparison of samples from different electrode generations. From left to right: a USA quarter for size comparison, generation 4 sample with full radius electroplated copper electrode, generation 2 sample with inset silver loaded epoxy electrode, and generation 3 sample with full radius painted silver electrode [1].

Electrodes for all samples prepared and tested for this report are applied in the same manner, beginning with application of a highly conductive base layer electrode. The electrode base layer is silver deposited using a high voltage DC sputter coating process. For most samples tested in this program the electrode base layers were applied using a Denton Desk II, pictured in Figure 3.2, which has been modified to run at higher currents for extended periods of time.

Figure 3.2: Denton Desk II DC sputter coater developed by Denton Vacuum used to deposit conductive silver (Ag) as electrodes onto sample capacitors. Sputter coating allows for some surface penetration of the sample as well as surface deposition resulting in a greater metal-substrate interface [2].

High energy sputtering allows for a small amount of surface penetration when applying the metal allowing for good surface adhesion and uniform metal deposition. Sputter coating the seed electrode layer maintains a strong electrode/dielectric interface. For single capacitors fabricated during this effort, the final step in the electrode deposition process is to electroplate copper to the silver coated faces of the disk. Prior to the copper electroplating, the edges of the substrates are wrapped in conductive tape to mask the edges and to carry voltage to allow the electroplating process to occur.

When electroplating copper onto a MU100B disk, the disk is immersed in a copper sulfate electrolyte bath [3]. The faces of the disk are held at ground potential while a sacrificial copper anode is positively charged, as shown in Figure 3.3. The flow of copper ions from the anode to the disk (cathode in this process) deposits pure copper on the silver sputter coated faces. The rate of copper deposition is regulated by the anode voltage which governs the flow of current. By varying the current level and plating time the thickness of copper plating could be finely regulated. For samples prepared in this effort, the copper was plated by employing a current of 1.3 A for 60 minutes. This protocol resulted in a copper electrode approximately 50 µm thick. Once plated, the disks are removed from the bath and dried in a vacuum oven. After drying, any copper fingering down the disk edge is carefully removed by sanding.

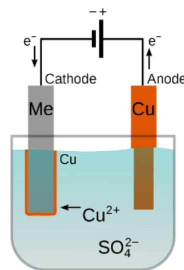

Figure 3.3: A depiction of a copper electroplating system. Flowing an electric current from the sacrificial copper anode to the cathode results in copper deposition on electrically conductive areas of the cathode [4].

3.3 Stacked Capacitor Assembly

To enhance the operational voltage of MU100B based capacitors, a greater substrate thickness was required than could be manufactured with a single disk. To increase the thickness of MU100B capacitors, multiple MU100B substrates were stacked together in series using a novel brazing process. When stacking disks, there are two objectives: one, to introduce an equipotential layer between each disk and two, to securely adhere the substrates together mechanically. To produce the stacked assemblies, each substrate was sputter coated only. A low temperature eutectic solder was bonded directly to the sputtered silver on the face of each MU100B substrate. A modified version of the protocol listed in reference [2] was used to develop the technique.

The procedure used to join the MU100B substrates in series involved solder preforms obtained from the Indium Corporation and were adhered to the sputtered substrate face following the manufacturer's suggested method [5]. To breakup oxides formed during the soldering process, a vibrating applicator was used to spread the liquidous solder across the substrate face [6]. The substrates were affixed in an alignment jig to aid concentric stacking. Additionally, this process was used for bonding field shaping electrodes to MU100B substrates.

3.4 Capacitor Encapsulation

As discussed in Section 1.1, bringing the electrodes to the edge of the disk allows for a minimization of the effects of triple points on the surface of the capacitor substrates. However, additional difficulties arose and were addressed with novel electrode topologies, which are discussed in detail later in this thesis. The use of field shaping electrodes in these capacitors concentrate the highest electric fields in the potting or encapsulation, as well as

on the wall of the capacitor. Depending on the electrode configuration, the peak electric field in the encapsulant was enhanced by various factors. The flat electrode configuration induces the largest peak electric fields in the encapsulant with a field enhancement factor of 5 times the average electric field. The subsequent generations of field shaping electrodes reduced the large field enhancement factor of the flat electrodes to 2.5 times the average field in the first generation and just 1.11 times in the final generation. Due to the field enhancement induced high peak electric fields in the encapsulant, several materials were explored as possible potting compounds. Candidate materials were evaluated to reduce the likelihood of surface flashover. In the early stages of this project, capacitors were potted in a two-part epoxy made by Laird [7]. The Laird material has been shown to have breakdown fields in excess of 430 kV/cm with a dielectric constant of 10; however, it does not flow well and its relatively high viscosity traps air, forming voids at the electrode nanodielectric interface. These voids are difficult to remove by application of vacuum due to the material's short working time.

The Laird material was used to encapsulate early 250 kV capacitors, but as the operational voltage of the capacitors increased, the Laird material did not have an adequate dielectric strength for continued use. A two-part epoxy specifically designed for potting high voltage electrical components made by Hexion was then employed [8]. The Hexion 815c epoxy has a measured dielectric constant of 3.2 and a quoted dielectric strength of over 1 MV/cm [9]. Both the Hexion 815c and the Laird material are castable; however, they are two-part epoxies and must be mixed manually, resulting in the introduction of air voids. As a potting compound, it can be out gassed in a chamber like that pictured in Figure

3.4; however, given the relatively fast cure times for these materials, complete removal of air is difficult.

Figure 3.4: Vacuum chamber used when encapsulating ultra-high voltage capacitors. Out gassing is used to reduce the prevalence of voids in potting compound. Vacuum is reached with a roughing pump capable of reaching 29 in. Hg.

The potting of ultra-high voltage capacitor assemblies is required due to the high electric fields present in the design. When a sample is potted in an encapsulant, the process is primarily the same for both the Laird material and the Hexion epoxy, the epoxies are mixed and then placed in several containers to increase surface area to aid in the outgassing process. Tall polypropylene cups served as the encapsulation mold. Capacitors to be potted are secured to the bottom of the cups through the screw termination of the device. Once outgassed, a portion of the epoxy was carefully poured into the polypropylene mold around the capacitor to be potted. Care is taken in this step to minimize the introduction of air and other contaminates. When fully covered with epoxy, the capacitor/epoxy assembly is outgassed again to ensure minimal to no air voids are present in the mold before breaking vacuum and allowing the epoxy to cure.

After the epoxy was cured in air for 16 hours, final curing was accomplished by heating the assemblies to 100 ºC for two hours [8]. After completing the curing process, the potted capacitors are removed manually from the polypropylene cups. The screws keeping the encapsulant epoxy out of electrode screw terminals are then removed and any excess epoxy in machined away before polishing of the completed assembly.

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Chapter 4. Test Sample Evaluation Equipment

4.1 Low Voltage Electrical Characterization Equipment

4.1.1 Low Voltage Permittivity Measurements

Characterization of MU100B substrates begins with low voltage measurements of capacitance and dissipation factor. These measurements were made with an Agilent 4285A Precision LCR Meter at frequencies ranging from 75 kHz to 30 MHz with most of the measurements recorded at 5-10 MHz [1]. The Agilent 4285A is shown in Figure 4.1. These low voltage permittivity and loss tangent measurements are made using a shielded probe housing shown in Figure 4.2. The shielded capacitance probe, made by Keysight, part number 16451B, is designed to mitigate the effects of stray and fringing capacitance on device measurements [2]. When measuring capacitance levels in the 100's of picofarads, stray capacitance can significantly affect recorded capacitance values [3].

Figure 4.1: Agilent 4285A Precision LCR Meter used to gather low voltage dielectric measurements over a range or frequencies, 75 kHz up to 30 MHz. Per the ringing nature of the ultimate application, most concern was put on frequencies between 5 and 15 MHz [1].

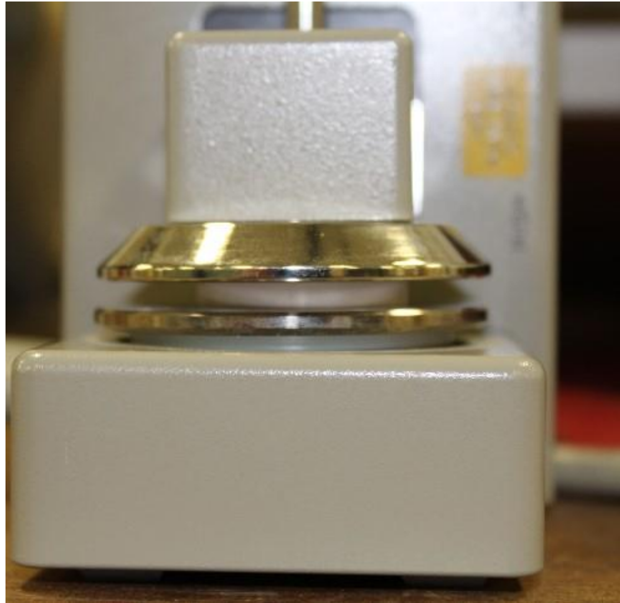

Figure 4.2: Thin test sample in shielded dielectric probe for minimizing the effects of stray capacitance on dielectric measurements. Substrates ranging in thickness from 0.1 cm to 2.4 cm can be characterized with this shielded probe [2].

4.1.2 Leakage Resistance and Current Measurements

The leakage current and resistance of sample capacitors was measured with a Sencore LC103 Inductor and Capacitor Analyzer, pictured in Figure 4.3, where a voltage of up to 1 kV can be applied. The LC103 is rated to measure currents as low as 0.01 µA [4]. Leakage currents too low to be accurately measured will return a leakage resistance of greater than 1 GΩ. Samples which did not return this value were not used for fabrication and testing. In addition to using the LC103's leakage resistance measurements as a "pre-screening" of MU100B substrates, the leakage resistance is measured after high voltage testing to confirm dielectric failure. Many times, in larger capacitor prototypes the device will fail at high voltage (>250 kV) but will still show a stable capacitance reading at low voltage, thus the leakage resistance is a method of confirming the failure at lower voltage. After failure, the leakage resistance with 1 kV across the device will be on the order of 1-5 kΩ as opposed to over 1 GΩ in pretesting assessments.

Figure 4.3: Sencore LC 103 Capacitor and Inductor Analyzer. The primary characterization function of this instrument is to take a high voltage leakage resistance measurement. If leakage resistance measures too low, samples are discarded [4].

4.2 PA-80 Based High Voltage Breakdown Test Stand

A PA-80 pulse generator, from L-3 Communications Pulse Sciences, was integrated with a resistive protection network and was utilized as the pulsed high voltage source for one of the breakdown test stands [5]. Diagnostics for the pulsed breakdown test consists of two PVM-6 high-voltage probes [6] [7] which monitor the voltage on each side of the test sample. Measurement of the breakdown voltage is obtained from the difference of the two voltage measurements and determines the maximum voltage of the difference signal. The maximum bandwidth of the PVM-6 is 80 MHz, which corresponds to a rise time resolution of 4.4 ns.

Table 4.1: Summary of the performance specifications of the PA-80 pulse generator used to evaluate thin substrates under a high-voltage pulsed condition. Specifications are from the PA-80 operation manual [5].

Charge Voltage	5 - 80 kV
Stored Energy (at 80 kV)	240 Joules
Output Voltage with a 50 Ω Matched Load	80 kV
Output Voltage with an Open Circuit	~160 kV
Output Rise Time (10-90 %)	~100 ns
Accessory Gas Required	SF_6 at 100 psig

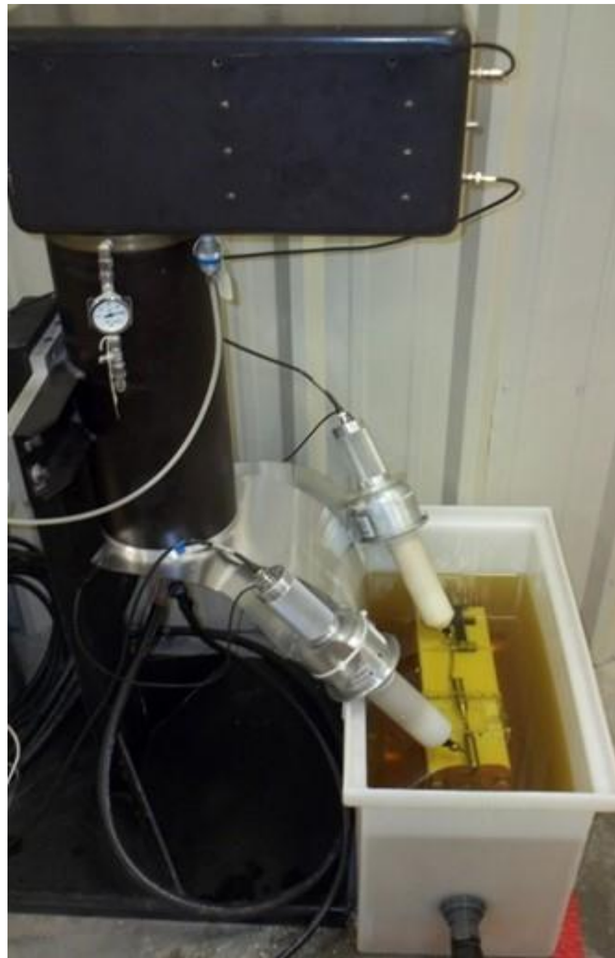

Figure 4.4: PA-80 trigger system used for delivering a high-voltage pulse to small-scale test capacitors. Test stand capable of delivering up to 100 kV with a 100 ns rise time to a capacitive load.

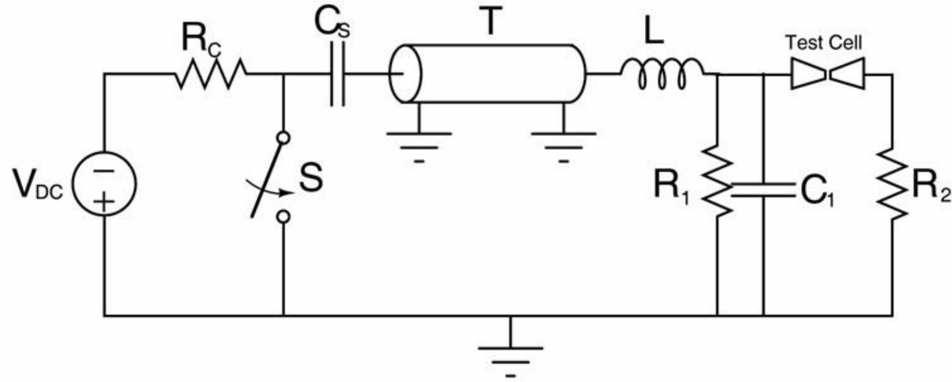

Figure 4.5: Schematic of the PA-80 high-voltage pulse test stand.

The schematic for the PA-80 pulse generator from L-3 Communications Pulse Sciences in Figure 4.5. A 75 nF capacitance, Cs, is resistively charged to the voltage range specified in Table 4.1 from a DC power supply. Once the proper charge voltage has been reached, a spark gap, S, is triggered by a PT-55 [8]. This allows for the capacitor to discharge into an RG-218/U transmission line, T, which has an impedance of 50 Ω. This transmission line is terminated into the load, which consists of a 0.54 nF capacitor, C1, in parallel with resistor, R1. This can be switched between 50 Ω and 100 Ω to limit the peak voltage experienced by the test cell to 100 kV reducing the likelihood of damaging the high-voltage diagnostics. Imbalance of capacitances between Cs and C1 allows for the voltage delivered to the test cell to ring up nearly 1.8 times the voltage of V_{DC} due to the design of the test fixture.

4.3 250 kV High-Voltage Test Stand

As the capabilities of MU100B base capacitors increased, higher voltages were needed to sufficiently test them. The PA-80 based test stand is typically used for testing small-scale samples up to 100 kV. As MU100B substrates became thicker and more refined, the PA-80 was no longer capable of breaking down the thicker (~2 cm) substrate capacitors. To adequately test capacitors of that size for dielectric breakdown strength, a

new test stand was developed. This design consists of a 150 kV capacitor bank that rings up the voltage across the capacitor under test. The capacitor is discharged through a single spark gap into a smaller capacitive load comprised of the device under test and a compensated voltage divider through a discrete series inductor and resistor to allow for voltage ring up, schematic shown in Figure 4.6.

The primary capacitance consists of a series connection of three Maxwell capacitors (Model 31165) [9]**.** The individual Maxwell capacitors are 40 nF at 100 kV. Three capacitors in series have an effective capacitance of 13.33 nF at a rated voltage of 300 kV for the stack. The series inductor of the network is a copper tubing wound inductor with an inductance of 5.5 μH. Also, there is a series resistance to damp the ringing discharge, as can be seen in the simple circuit diagram shown in Figure 4.6. With no test load in the circuit, the primary capacitance discharges into a resistive and capacitive load. The two voltage dividers, one resistive and one capacitive, are monitored with Tektronix high-voltage probes and a 500 MHz oscilloscope.

Through experimental analysis, the output voltage to charge voltage ratio was found to be 1.75:1, through the ring up nature of CLC (capacitor – inductor – capacitor) type circuits. In circuits of this configuration, when capacitor bank and load capacitance are mismatched, i.e. bank capacitance is much greater than the load capacitance, the theoretical maximum voltage on the load capacitance undergoing CLC resonant charging can approach two times the charge voltage. This phenomenon is governed by the following equation [10].

$$V_{C,load} = \frac{2V_o}{1+\frac{C_{load}}{C_{bank}}} \tag{4.1}$$

Where V_o is the capacitor bank charge voltage, and $V_{C,load}$ is the voltage across the load capacitance.

Studying the electrical energy flow through the circuit during the discharge can explain how the voltage across a much smaller load capacitance can be larger than the charge voltage of the primary. Upon charging, energy stored in the bank capacitance is given by the following equation.

$$E = \frac{1}{2}CV^2 \tag{4.2}$$

Where E is the energy stored in the capacitor in joules when the capacitance, C, and the charge voltage, V, are given in farads and volts, respectively. Thus, when the primary capacitance is switched into the CLC circuit, it discharges its stored energy and transfers it to the load capacitance. Therefore, all the energy from the primary capacitance must be transferred to the load capacitor, and if the load capacitance is much smaller than the primary capacitance, the only way to maintain the same energy level is to increase the voltage on the load cap.

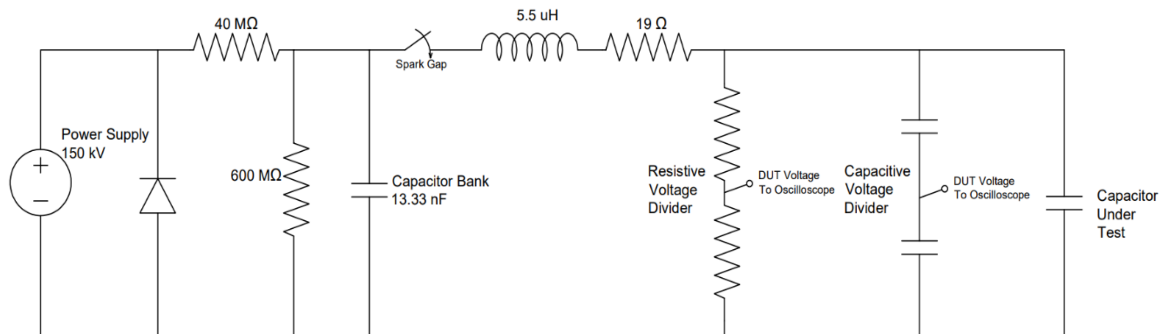

Figure 4.6: Schematic diagram of the 250 kV high-voltage test stand used for evaluating large scale substrates up to 265 kV.

Theoretically, all the energy from the capacitor bank will be transferred to the load. Thus, when the load capacitance is at least four times smaller than the bank capacitance, the load voltage will be twice as large as the charge voltage. However, in practice, energy

does not flow perfectly through electric circuits. Considerable amounts can be dissipated through lossy means, such as the resistance of conductors, and component connections. Due to that parasitic energy dissipation, voltage ring up across the load capacitor in circuits such as this is limited to about 1.7 – 1.8 X's the primary capacitance charge voltage, which is precisely what is seen in the 250 kV test stand.

Therefore, to achieve 250 kV across the test load, the primary capacitor bank is charged to approximately 145 kV. This test system was used to test encapsulated, or potted, ceramic capacitors to a voltage of 265 kV with a pulse rise time of approximately 110 ns, when the capacitor under test is placed in parallel with the two voltage dividers. Figure 4.7 shows a typical full charge voltage waveform from the described system. The first iteration of the test stand, which was only intended for single shot operation, is shown in Figure 4.8.

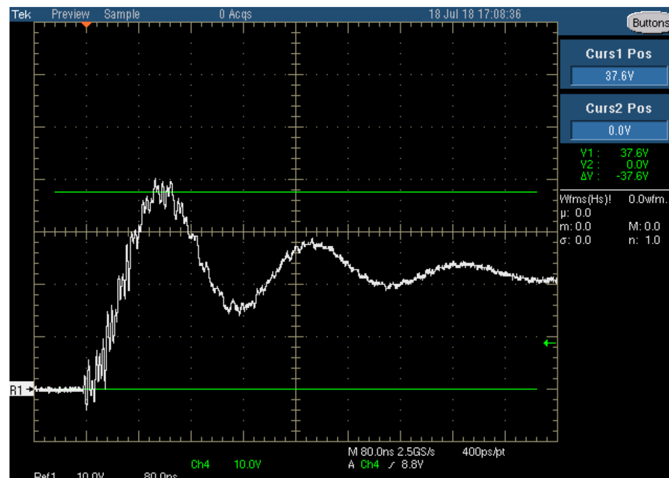

Figure 4.7: No load waveform of the 250 kV CLC test stand used to evaluate prototype dielectric strength and high voltage lifetime. Peak no-load voltage is equal to nearly 270 kV with 110 ns risetime.

Material and assembly advancements necessitated design of a system capable of achieving 250 kV at a slow rep-rate. Additionally, a more robust design was incorporated in this upgrade, enabling long duration operation at a shot repetition rate of about 1 Hz. The redesigned 250 kV test stand is shown in Figure 4.9. When operated in a repetative

mode, the improved 250 kV test stand can repetitively test devices at 1 pps with peak voltages ranging from 120 kV to approximately 270 kV. The redesigned system allows for thousands of shots to be applied to test devices per day, which is a substantial improvement of the 10's of shots that could be applied with the fist generation of the test stand.

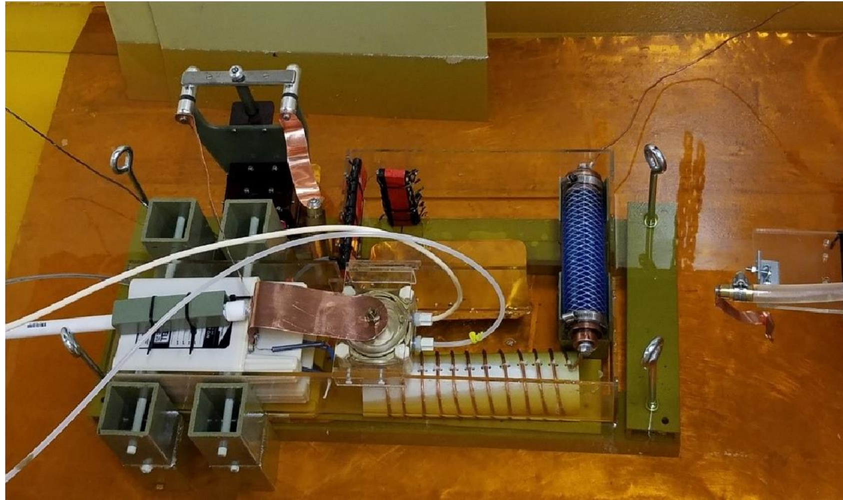

Figure 4.8: High-voltage test stand capable of pulse charging a capacitor to 250 kV with a pulse rise time of 110 ns.

Figure 4.9: Iteration two of the 250 kV Test Stand. Addition of copper pipe conductors and higher power components enabled test stand operation in repetitive mode at a pulse frequency of 1 Hz.

4.4 Ultra-High Voltage Marx Bank – Dahlgren, VA

The final requirement of this capacitor development effort was to deliver two fully functional 130 pF, 500 kV capacitors to the Joint Non-Lethal Weapons Directorate (JNLWD). The motivation for the delivery was to reduce one component in the system. The system is known as Pre-Emplaced Electric Vehicle Stopper (PEVS) and is designed to slow or arrest vehicle momentum to stop vehicles. The system is a pre-emplaced, non-intrusive device that provides an electrical pulse through deployed contacts to shut down power train electrical circuits or components per the Joint Non-Lethal Weapons Program website [11]. The component this program sought to reduce is known as the "Transfer Capacitor" and the specifics of the purpose it performs in the system is beyond the scope of this thesis. After improved material and capacitor developments at the University of Missouri, two smaller versions of the PEVS Transfer Capacitor were fabricated and shipped to the JNLWD in Dahlgren, VA for testing. The test and evaluation of the prototype transfer caps was carried out by Dr. J. Tom Camp.

The team at Dahlgren developed a test stand which closely emulated the electrical conditions a PEVS Transfer Cap are expected to operate under. The test stand consisted of a 15 stage Marx generator which pulse charged the transfer capacitor under test and a self-breakdown peaking spark gap. When the peaking switch closes, the transfer capacitor is shorted to ground through a known resistance and inductance, which generated a bipolar ringing discharge. A circuit diagram of the Dahlgren test stand is shown in Figure 4.10. The system was capable, under matched capacitance conditions, of pulse charging a test capacitor up to ~600 kV with a 50-60% voltage reversal during the ringing discharge. The risetime of the system, with full-scale test capacitor in place, was approximately 50 ns. As shown in the circuit diagram, the diagnostic method employed only recorded current

through the test capacitor. Capacitor voltage can be determined from the following equation:

$$V(t) = \frac{1}{C} \int I(t)\, dt \tag{4.3}$$

Voltage as a function of time can be obtained by integrating the current over time where I(t) is the current versus time waveform, and C is the capacitance of the test capacitor.

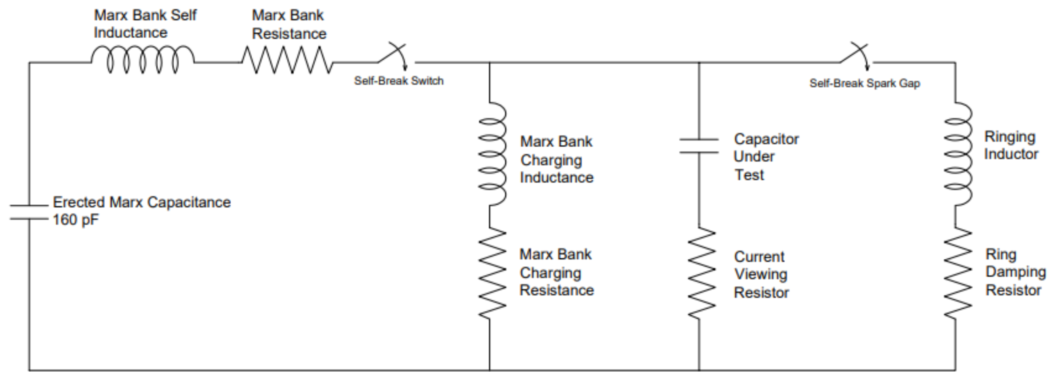

Figure 4.10: Simple Circuit diagram of the test stand set up at NSWCDD to emulate the PEVS module and test prototype transfer capacitors up to 600 kV with 55-60% voltage reversal, or test smaller capacitance sub-modules to greater than 1 MV.

The test stand was fully automated allowing it to run in a burst mode, where shots were fired at a repetition rate of 100 pps over a burst length of 2 seconds. A 10 second delay period was programed in before the burst mode began again to minimize component heating.

When the source capacitance (erected Marx bank capacitance) and the load capacitance are nearly equal, as they are when testing a full-scale transfer capacitor prototype, the erected Marx voltage is delivered to the load (limited to a max of about 600 kV due to Marx bank insulation and power supply limitations). A typical waveform from the tests is shown in Figure 4.11. However, if higher voltages were desired, decreasing the load capacitance allowed for ring up of the circuit, due to its CLC topology. Overvoltage testing of the MU100B transfer capacitor sub-modules was done in this way. Reducing the

load capacitance by approximately 9 times allowed ring up to occur, which enabled tests from 600 kV to upwards of 1.1 MV. A typical waveform from those tests are shown in Figure 4.12. Running the system in ring up mode changed the pulse characteristics of voltage peak and reversal. Rise time, pulse width and all other pulse parameters remained unchanged.

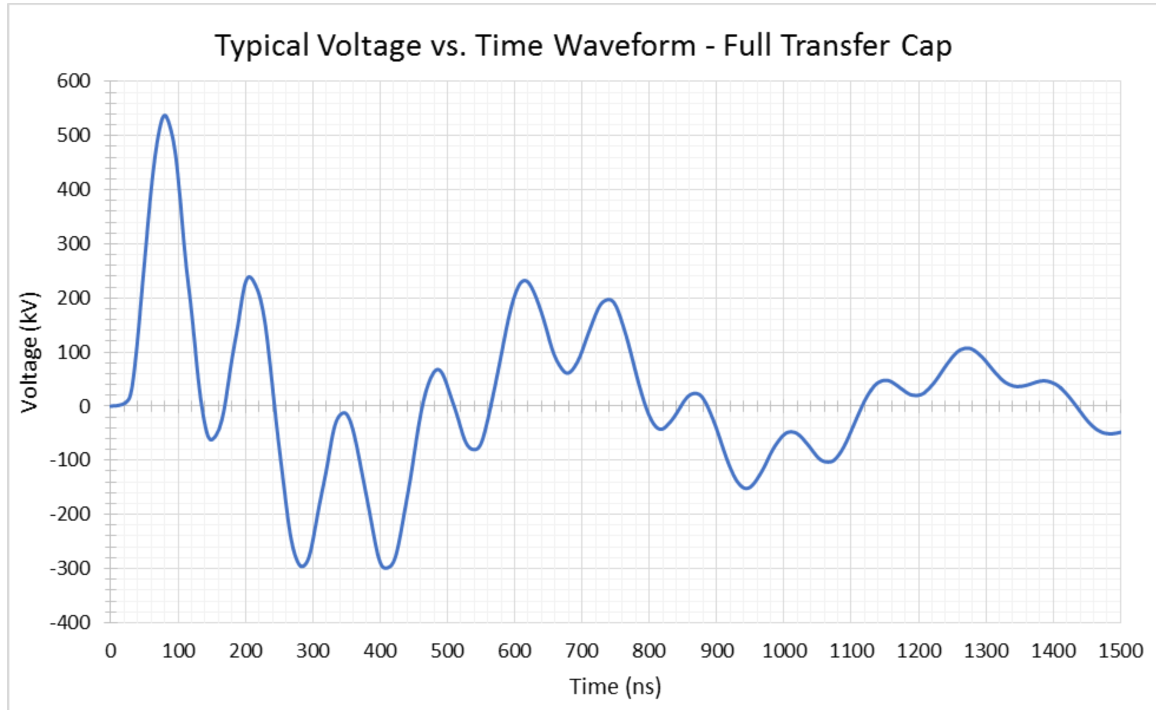

Figure 4.11: A typical voltage waveform from full-scale transfer capacitor testing. Matched load and erected Marx capacitances allowed max voltages of ~600 kV with 50 ns rise times. The voltage waveforms were obtained by integrating the measured current waveforms

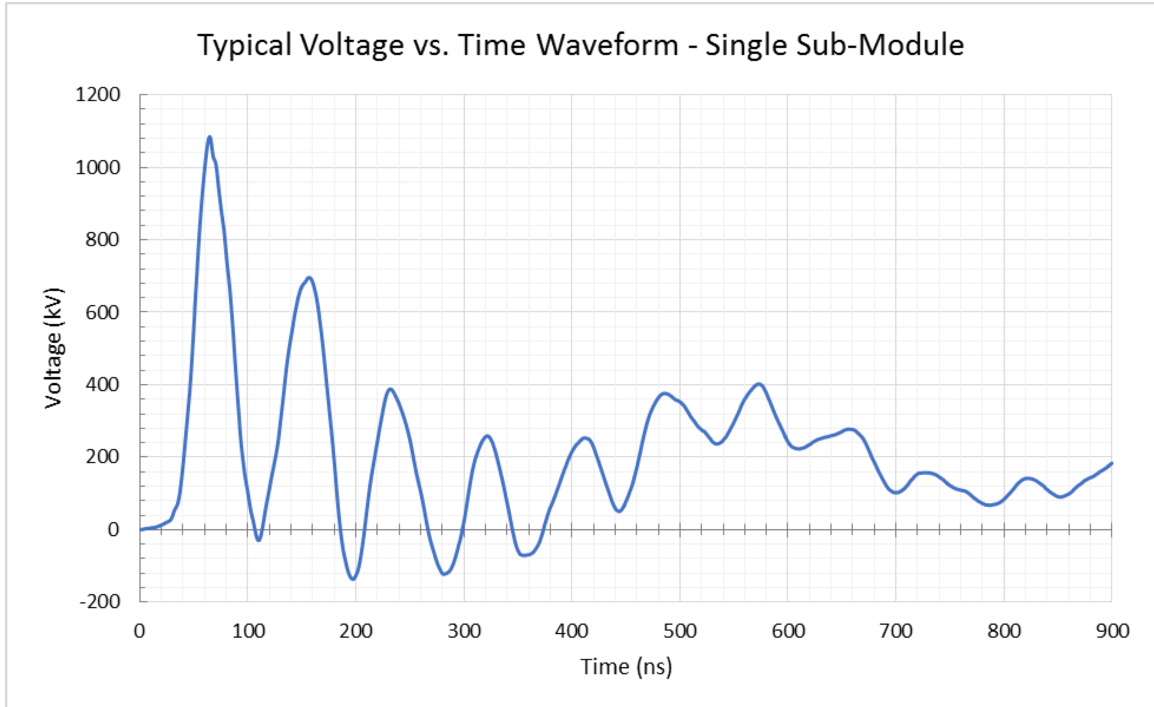

Figure 4.12: Typical voltage waveform from single sub-module testing. The mismatched capacitance allowed for voltage doubling of the Marx circuit. In this configuration the applied voltage reversal was 15%.

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Chapter 5. Material Scaling

Capacitor development on this project began with small-scale test samples [1]. The idea was to study what type of material or electrical assembly factors were most pertinent to MU100B based capacitor development. Small-scale samples were used in this phase to keep MU100B material demands low, enabling manufacture of a greater number of test samples, which helped build a statistical knowledge base of which capacitor parameters effected MU100B performance most.

It was determined through the early capacitor work that the dielectric-electrode interface and the capacitor edge effects were predominantly the factor which determine device performance [2]. A poor interface induces electric field enhancement factors, thus lowering the threshold field of the device. As described in section 1.1, an iterative electrode development process resulted in small scale capacitors with full dielectric radius electrodes which had acceptable adherence to the nanodielectric. Further improvements were attained with the small-scale samples by encapsulating the devices. The success of the small-scale development saw encapsulated devices demonstrate lifetimes in excess of 800,000 discharges. No failures were observed before testing was discontinued.

Understanding the physics of MU100B capacitor development was paramount in fabrication of successful small-scale capacitors. A strong small-scale foundation allowed for scaling the material to be capable of operation at much higher voltage levels. The small-scale capacitors operated at a voltage level varying between 20 and 40 kV. As was stated in the introduction, the final prototypes must be capable of long lifetime performance at a minimum of 500 kV with some devices approaching 1 MV. To achieve the operational voltage required, the thickness and volume of MU100B samples were increased to allow

ultra high voltage capacitors to be manufactured. The remainder of this chapter will describe how the MU100B material was scaled from 2.54 cm diameter, 0.15 cm thick small-scale test samples to 3.4 cm diameter, 2 cm thick dielectric substrates with a small dielectric strength decrease with increasing volume.

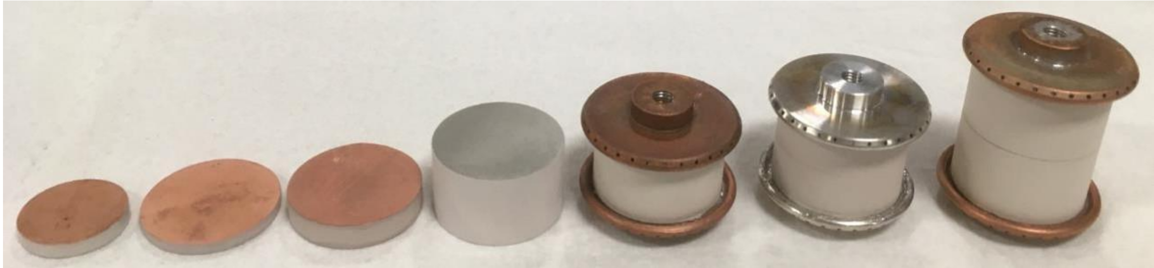

Figure 5.1: MU100B capacitors from the first small-scale test samples (left) up through near full-scale embodiments. This image shows the various size increments which made the scaling effort presented here possible.

5.1 Material Scale up Concerns

It is well documented that the dielectric strength in solid insulators drops according to an inverse power law as thickness and, as such, volume of the medium is increased [3].

$$E(d) = kd^{-n} \tag{5.1}$$

Where E is the applied electric field at breakdown, d is the dielectric thickness and k and n are constants associated with a specific material.

In order to scale up the nanodielectric, the material properties causing the volume dependent inverse power law decrease in breakdown field must be understood, and steps must be taken to mitigate those issues in the scaled nanodielectric material. As stated in section 2.3, the primary breakdown mechanisms in different solid materials can vary. Dielectric failure in polymers is generally initiated by phenomena on the microscale, whereas electric breakdown in pure ceramics is more commonly initiated through macroscopic means such as volume defects or grain boundaries in the material. With the polymer – ceramic composite nature of MU100B, each class of breakdown contributes to

dielectric failure in the MU100B material. Thus, both processes (microscale and macroscale) must be understood and accounted for as the typical size of usable MU100B disks are scaled up from 2.54 cm diameter by 0.1 – 0.5 cm thick small-scale test samples to 3.4 cm diameter by 1.8 – 2 cm thick ultra-high voltage substrates.

5.2 Material Refinements

To account for the volume effects induced and reduce the attribution of macroscale effects when scaling MU100B from 0.15 cm thick test samples to 2 cm thick capacitor substrates, the bulk manufacturing procedures of the MU100B nanodielectric were enhanced. These proprietary material manufacturing refinements resulted in more consistent and higher quality material.

The manufacturing refinements focused on increasing particle packing density as well as increasing the effectiveness of the particle-binder interactions. These improvements resulted in a more rigid material. Further, the manufacturing improvements saw led to less voids throughout the bulk material, while increasing particle wetting and mixing removed or concealed, internal jagged edges of particles within the matrix. The material improvements from this refinement are visible in the following scanning electron microscope images (SEM). The reduction of voids and grain boundaries makes it more difficult for a breakdown avalanche to propagate, while shielding of particle jagged edges makes it harder for a breakdown avalanche to be initiated, Figure 5.2.

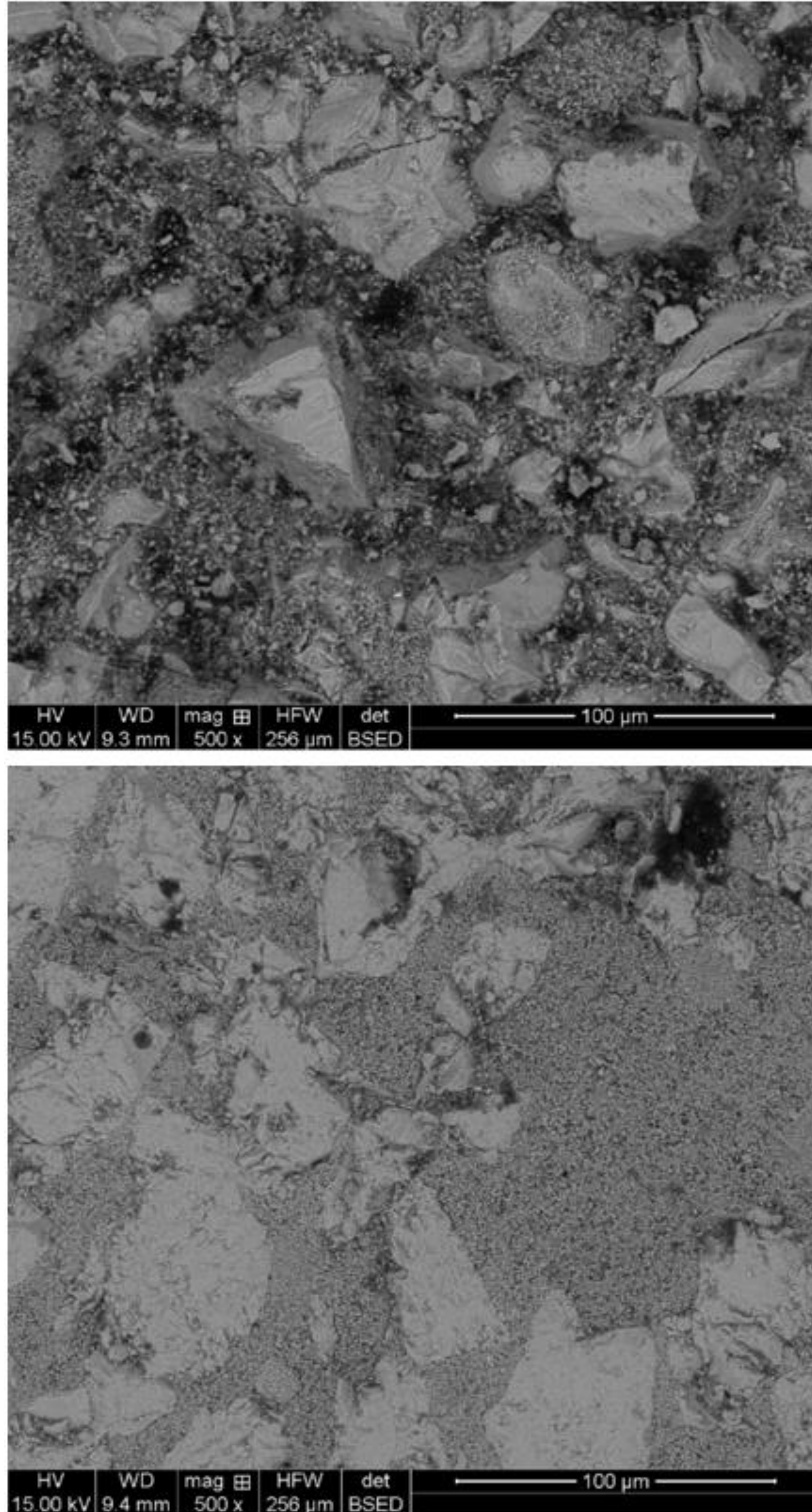

Figure 5.2: Side-by-side cross sectional SEM images of MU100B produced before the material scaling manufacturing refinements (top) and after the material manufacturing refinements (bottom). A larger presence of voids, grain boundaries, and particle jagged edges is evident in the small-scale material, where the larger scale substrate material is much more uniform.

To account for the volume effects induced on a microscale level, the electrode-dielectric interface was examined. Space charge is most commonly injected into dielectric materials through large field enhancements along that interface. The early, small-scale material had a rougher edge on the face of the MU100B material. When an electrode was applied the imperfections on the face of the material would result in field enhancements on the bottom side of the electrode. Sharp points into the MU100B would be locations of high space charge injection due to the field enhancement factors present at any sharp point.

To address the microscale space charge injection issues a method to apply a finer polish to the faces of full-scale MU100B ultra-high voltage substrates was developed. This finer polish resulted in a considerably smoother surface upon which to apply the electrode. Further, electrode application was also improved. Higher energy sputtering of the seed electrode allowed the electrode layer to lightly penetrate the dielectric material which improved adhesion and ensured a smooth, consistent interface. These microscale improvements can be visualized in the SEM images of Figure 5.3.

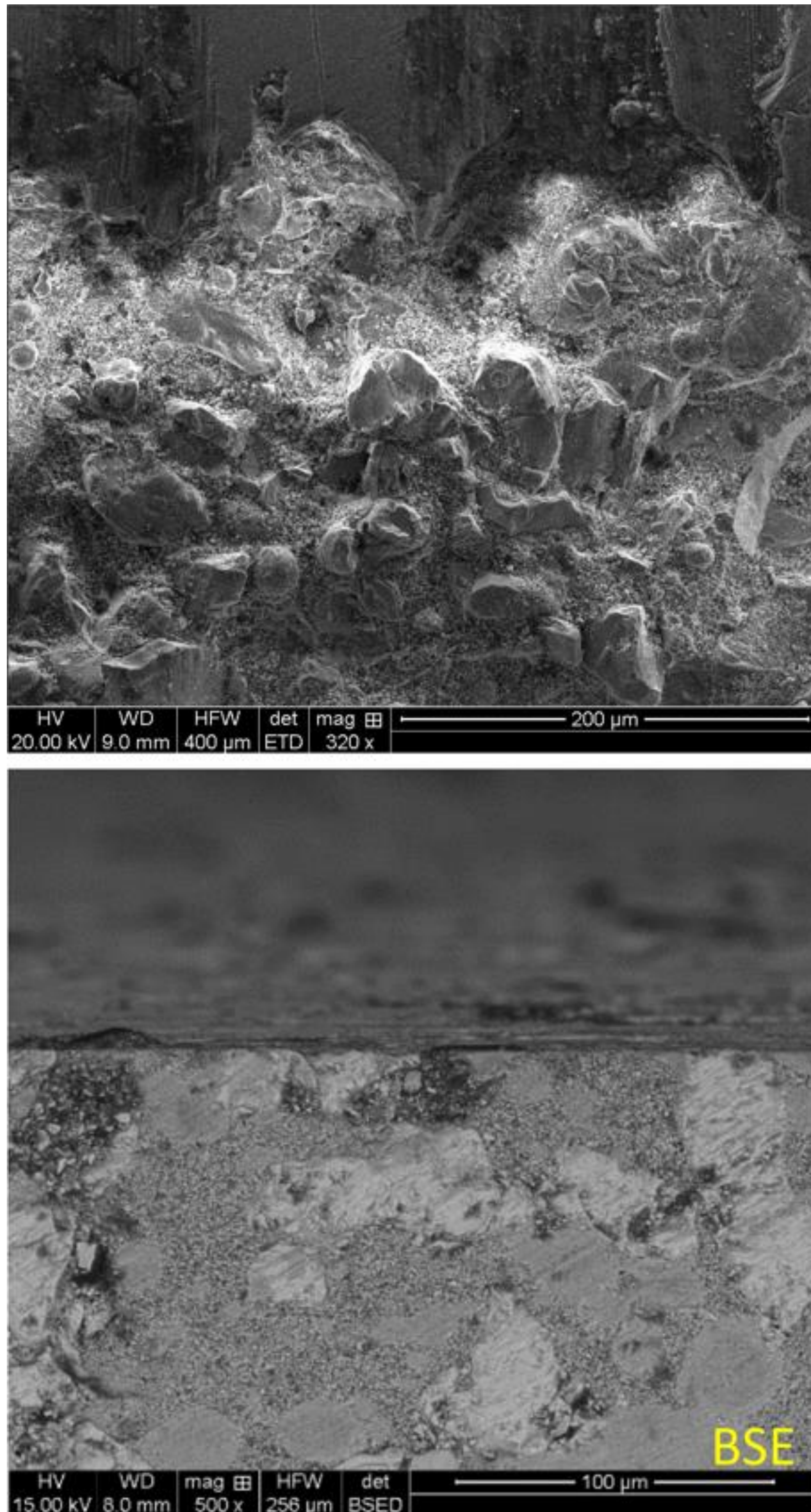

Figure 5.3: Side-by-side SEM images of the MU100B dielectric-electrode interface. The small-scale material is shown on top, where the rough, space charge injecting, electrode interface is visible toward the top of the image. The interface is visibly improved in the scaled material, as that edge appears smoother even at a higher image magnification (500x versus 320x).

5.3 Material Scaling Results

The refinements made to the MU100B manufacturing and electrode deposition procedures during the process of scaling the MU100B material were crucial in the development of ultra-high voltage capacitor substrates. The scaling effort resulted in increasing 2.54 cm diameter, 0.15 cm thick samples to 3.4 cm diameter, 2 cm thick substrates which resulted in a platform upon which ultra-high voltage capacitors could be developed. The scaling process resulted in full scale (3.4 cm diameter, 2 cm thick) MU100B with a dielectric constant 60%-80% higher than the initial small-scale embodiments.

The refinements to the manufacturing process were the predominant cause of the increase in dielectric constant, as the particle packing factor was increased which allows a higher level of ceramic to be incorporated into the composite material. The improved surface polishing, to reduce space charge injection, improved the dielectric-electrode interface, which showed great improvements to constituent device lifetimes at high voltages, as well as high breakdown voltages in substrates of similar thickness.

As stated previously, it is well known that solid dielectric materials generally follow an inverse power relationship between breakdown voltage and dielectric size (see equation 5.1). In many cases the n value (exponent) which fits best for typical materials is on the order of -0.5. Many nanocomposites have been shown to follow that trend [4]. However, due to the material scaling efforts described here, the dielectric strength of MU100B has a much smaller volume dependence than is typical. The breakdown strength with volume dependence goes to the power of -0.094 and is shown in Figure 5.4 where average breakdown fields of varying volumes of MU100B dielectric are plotted. All points on the graph are average breakdown fields which are averaged over 10 test samples at each

volume. The result is a similar scaling law to what was observed by Charlie Martin and Ian Smith for polymers [5] [6].

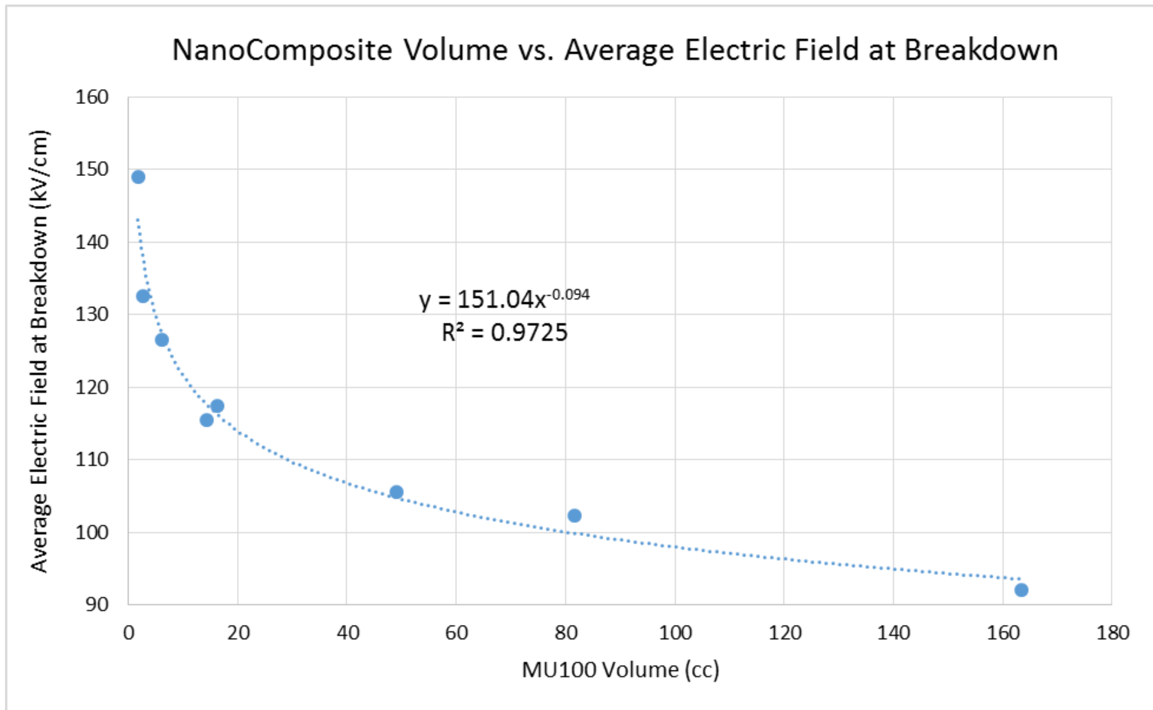

Figure 5.4: MU100B volume versus average breakdown strength. Each point on the graph is an average of 10 test samples at each individual volume.

References – Chapter 5

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Chapter 6. Field Shaping Electrode: Modeling, Development, and Evaluation

Nearly all of the dielectric breakdowns observed during the small-scale testing and initial scaled testing were edge breakdowns. Edge breakdowns are generally field enhancement factor induced failures and are not a true representation of the device's bulk dielectric strength. In order to realize the full potential of the MU100B dielectric, the field enhancement factors (FEF), which resulted in surface tracking or edge breakdown, had to be reduced.

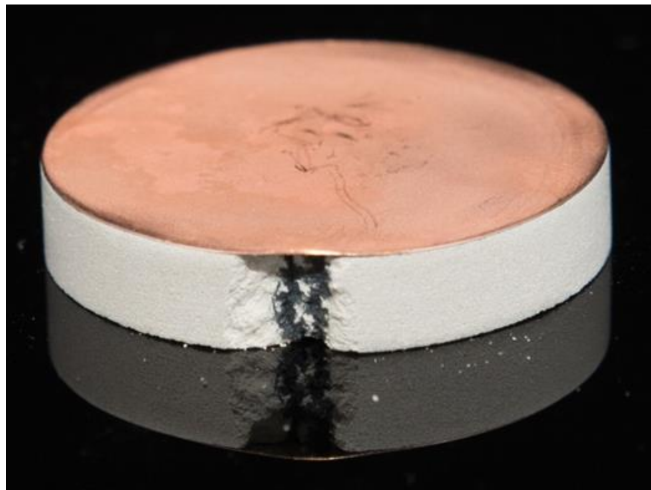

Figure 6.1: A small scale capacitor sample edge breakdown. Edge breakdowns are the result of large field enhancement factors at the dielectric, electrode, and surrounding material triple point.

The flat electrode tests were conducted at 40, 100, and 250 kV utilizing existing test stands and varying dielectric thicknesses from small scale (approximately 0.2 cm thick) up to the scaled embodiments at 2 cm thick. The electrode edge breakdowns suggested that field enhancement at the triple point was the primary cause of the premature device failure [1]. The breakdown due to the FEF would initiate at the interface between the surface of the MU100B disk and the encapsulant and then would move into the bulk of the MU100B substrate as the breakdown propagated as shown in Figure 6.1 for a small scale test sample

and in Figure 6.2 for a scaled, encapsulated flat electrode capacitor. Thus, to further improve the electrical performance of the full-scale nanodielectric material, a method for mitigating the electrical FEF's was developed and tested.

Figure 6.2: A scaled, flat electrode edge breakdown. The high field enhancements at the triple point lead to edge failure at ~80 kV/cm average field (400 kV/cm at enhanced points) [2].

6.1 Modeling Introduction

6.1.1 Modeling Motivation

To mitigate the effects of FEF on 2 cm thick MU100B capacitors, advanced electrode topologies were investigated. The advanced electrode was designed to shape the electric fields at the electrode edge, thus reducing the FEF. The goal of the design was to hide the triple point interface, at the edge of the disc where the MU100B nanodielectric, mating base electrode and potting material meet. As previously mentioned, that point has been the origin of breakdown in many of the prior capacitor samples. The proposed field-shaping electrode hides this point from high electric fields by employing a corona ring electrode topology mated to the base electrode. Investigation into this sort of field shaper

resulted from multiple theoretical and experimental iterations. The modeling allowed us to understand how the field shaper changes the way the field lines wrap around the triple point in an effort to shield that location from excess electric field levels, in a physically implementable configuration.

Electrostatic modeling was used to evaluate the design of the capacitor field shaping electrode designs and determine the effects of changes to component properties and geometries. Electrostatic modeling has advantages over a completely experimental approach in that it is significantly less expensive, faster and is not subject to experimental errors due to uncontrolled variables in the manufacturing, testing or evaluating process. However, models always include approximations of the physical system, hence the results of electrostatic modeling are only accurate and valuable when the approximations included in the model adequately represent the physical system. Some of the key approximations included in the electrostatic model are described in more detail later in this section.

Electrostatic modeling provides critical information in the design of the capacitor prototype in two important areas. First, the model provides a way to verify the capacitance of a chosen geometry and the average electric field in the composite material. Second, the model provides critical information in the analysis of FEF. While it is straightforward to calculate the average fields in the composite material based on the operating voltage and the thickness of the composite substrate, the FEF are often the critical points of failure in the capacitor. FEF are larger when one of the materials has a large dielectric constant as with the materials used in this effort. Therefore, the electrode-composite interface must be designed to limit FEF to enable operation at the largest possible average electric field. Electrostatic simulation allows a better understanding of the effects of geometry and

material changes along with enabling a means of rapid calculation of the peak electric fields.

6.1.2 Modeling Methods

The electromagnetic (EM) studio in the CST studio suite of programs is a software package that models electromagnetic, electrostatic, magnetostatic and low-frequency fields. The electrostatic solver is used in this program to calculate electric fields from specified geometry and applied voltage. The mesh geometry can be either hexahedral or tetrahedral, although some features are available with only one mesh geometry. In most cases, either mesh can give satisfactory results and comparison of results can provide a useful check on accuracy. After repetition of modeling runs of identical geometries, it was determined the hexahedral meshing algorithm was most applicable to the information important to this phase of MU100B based capacitor development. The tetrahedral mesh is a material volume-based approach to meshing a finite element model, whereas the hexahedral process places more emphasis on surfaces and component interactions. Thus, the hexahedral, surface-based approach gives more applicable insight into the FEF between various materials and adjacent components.

The field shaping electrode models presented here and every ultra-high voltage capacitor model in this report represents the environment in which the physical device is tested. Capacitors in all models have MU100B as the dielectric material, where the MU100B is simulated as a predominantly ceramic material with a dielectric constant equal to 160. Additionally, every capacitor simulated in this project is encapsulated in an epoxy material simulated with a relative permittivity (ε_r) of 3 which is consistent with the Hexion 815c epoxy used to encapsulate prototypes. Surrounding the potted capacitor, in the simulation, is 2.54 cm of Diala AX oil, with an isotropic ε_r of 2.3. The simulation

boundaries are set to be open as boundaries in an electrically large oil bath would be. Setting up the simulations in this manner was found to most closely emulate what was seen in physical testing.

6.2 Simulation Results/Iterative Field Shaping Electrode Design and Evaluation

Using scaled MU100B substrates with only flat electrodes, simulations in CST's EM studio showed a FEF within the MU100B of 4.96 times the average field as shown in Figure 6.3. Experimentally, the average dielectric strength at breakdown of the same size devices was found to be 80 kV/cm, much lower than what our the material scaling law would suggest [2]. The large FEF of the flat electrode topology were determined to be the cause of the premature nanodielectric failure. The FEF forced the peak field at failure of these devices to be approximately 400 kV/cm at areas around the triple point interface. This was evident in experimental testing as the FEF induced breakdowns would initiate at the capacitor triple point and track down the surface of the MU100B.

To mitigate the FEF's, a field shaping electrode was iteratively designed to shield the triple point and to spread the high electric fields present near the electrode, nanodielectric, and encapsulant triple point interface [3]. The field shaping electrode designs and constituent models began as rough estimations and progressed to all-encompassing models as designs and knowledge of parameters effecting performance improved. The iterations of field shaping electrode development, taking place after the flat electrode investigations, will be presented here. The field shaping electrode design and modeling began with the first iteration of field shaping electrode, which did not improve device performance when experimentally tested. The modeling concludes with the final field shaper iteration which improved the field enhancement factor in the MU100B to 1.11

times the average field, an improvement of 77.62% when compared to the flat electrode simulations. Furthermore, in experimental testing, the average electric field at breakdown was improved from 80 kV/cm in the flat electrode devices to 117 kV/cm when the final field shaping electrode was employed.

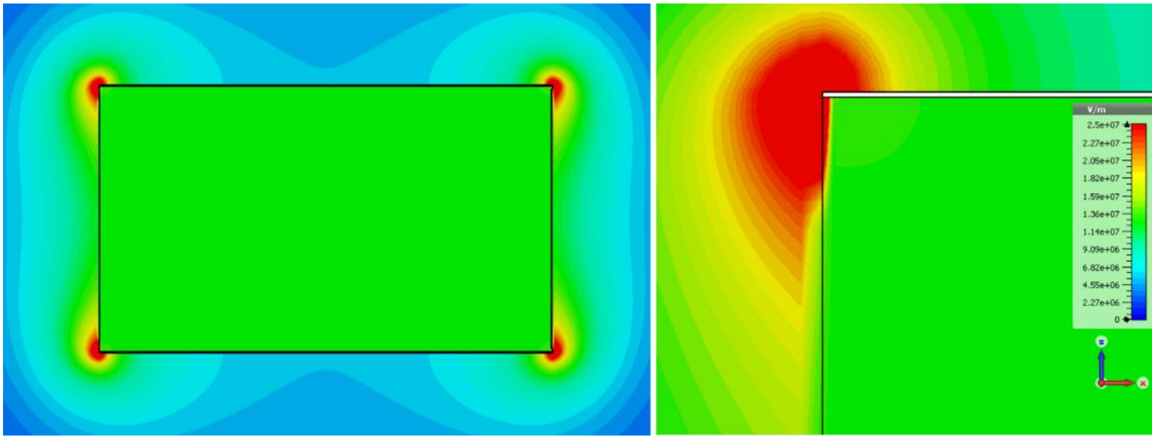

Figure 6.3: Electrostatic model of a scaled MU100B capacitor with flat electrodes. Left is the full device, right is a close up of the triple point. The average field of the model is 125 kV/cm (250 kV across the 2 cm thick dielectric). Peak field in the MU100B is 620 kV/cm, suggesting a FEF of 4.96 times the average field.

6.2.1 First Field Shaping Electrode Iteration

The first iteration of adding a corona ring based electrode to MU100B capacitors relied on various electrode design references, such as Hopkins, and Bouwers, respectively, to calculate the optimal cylindrical radius to apply to the corona ring in order to keep the fields as low as possible [1], [3]. Corona ring design, in this application, is a balancing act between radius of the corona ring and separation distance between the closest points of the two electrodes. The corona ring topology was mathematically modeled as what Hopkins calls "parallel or crossed cylinders" where the field enhancement factor, f* in Hopkins work, is shown in Figure 6.4 [1].

Due to the size limitations present in these devices, for the first corona ring modeling iteration, the ratio of separation distance (x in Hopkins work) to corona ring

diameter (d in Hopkins work) was designed to be approximately 7 [1]. The corona ring diameter, d, was first simulated at 0.25 cm with a separation distance, x, of 1.75 cm. Making the ring diameter any larger would begin to cancel out the FEF reducing effects of the corona ring as the separation distance between the two electrodes is reduced as the corona ring diameter is increased, forcing the average field between the two electrodes to increase accordingly. Reducing the separation distance a small amount cannot be avoided when employing corona ring electrodes, but reducing the separation distance too much runs the risk of inducing peak fields in the encapsulant that are greater than the encapsulant material's breakdown field (430 kV/cm for the Laird epoxy which was used in this iteration).

Per Figure 6.4, a separation distance to corona ring diameter ratio of 5 (1.75 : 0.25) implies a field enhancement factor, f*, of approximately 2.8. Thus the 0.25 cm corona ring diameter with a separation distance of 1.75 cm when applied to a 2 cm thick MU100B substrate was modeled and simulated in CST.

The results of the first iteration simulation, shown in Figure 6.5, suggested a FEF of 2.5 times the average field present in the MU100B material, showing the corona ring is capable of shielding the MU100B from the highest peak fields. This FEF reduction is a substantial improvement over what was seen in the flat electrode topology, a FEF of 4.96 times the average field. However, the FEF of 2.5 was still too large to be used as a viable field reducing electrode. The first iteration field shaper would subject the MU100B to peak electric fields on the order of 315 kV/cm when simulated with 250 kV across the 2 cm thick dielectric. Further design iterations were necessary to continue to reduce the FEF's.

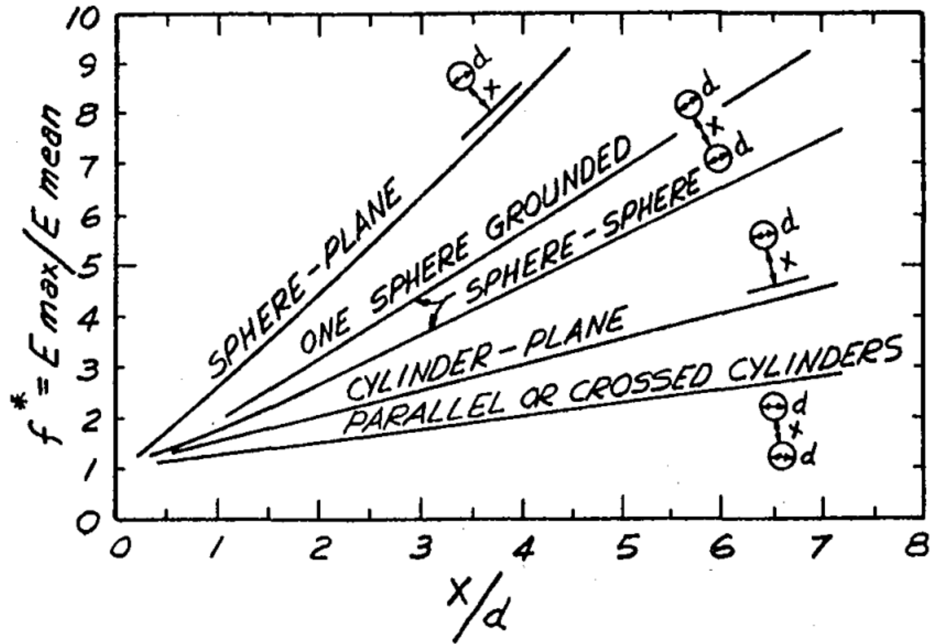

Figure 6.4: Graph of corona ring diameter (d) versus electrode separation distance (x). The case most relevant to opposing corona rings is the "parallel or crossed cylinders" case. The first iteration was sized to keep f* as low as possible considering size constraints of the device [1].

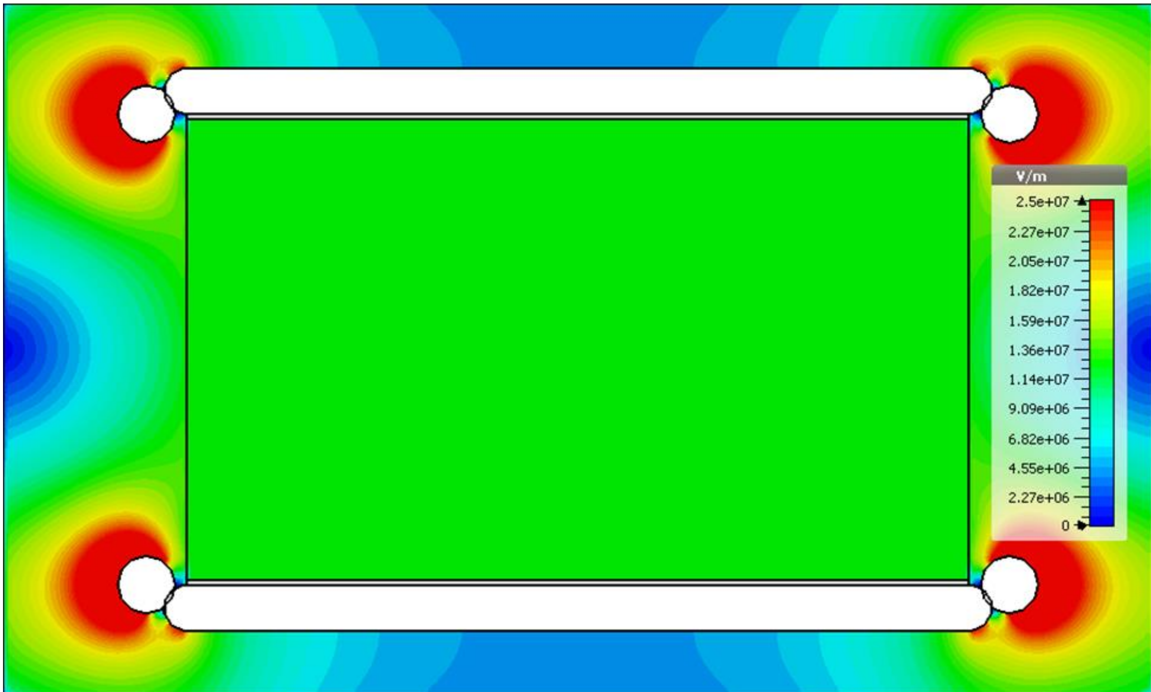

Figure 6.5: Electrostatic model of the first iteration field shaping electrode. The corona ring electrode shields the highest peak fields from the MU100B, but further design improvements remain necessary to achieve an electrode design capable of long lifetime high voltage operation.

6.2.2 Second Iteration Field Shaping Electrode

The second modeling iteration was conceived around exchanging the Laird encapsulant for the much higher dielectric strength of the Hexion 815c epoxy. Using the higher dielectric strength epoxy for the encapsulant material meant that higher peak field levels could be acceptably employed as long as they were pushed far enough away from the MU100B. Thus, the second field shaping electrode design iteration moved the corona ring away from the MU100B, while leaving all other field shaping ring parameters unchanged. The corona ring diameter remained 0.25 cm and electrode separation distance remained 1.75 cm when attached to a 2 cm thick dielectric substrate. The inside of the corona ring was extended from 0.058 cm from the edge of the MU100B in the first iteration to 0.1 cm from the MU100B. Moving the corona ring any farther from the MU100B was not desired in an effort to not increase the encapsulated diameter of the device. Increasing the corona ring diameter to more than 0.1 cm from the edge of the MU100B would require the encapsulant diameter to increase, which would increase the final size of the prototype, adversely effecting device energy density.

Moving the corona ring away from the MU100B proved to be a substantial improvement to the FEF present in the MU100B material. Moving the corona ring radially away from the nanodielectric allowed the electrodes immediately covering the top and bottom of the MU100B to more closely resemble the only electrode geometry with a FEF equal to 1, infinite parallel plates. Widening the corona ring electrode moved the field enhancing sharp geometry changes farther away from the MU100B, thus reducing field stress within the nanodielectric at the cost of an increase to the field stress in the encapsulation. The field increase to the encapsulation would be too great for the previously employed Laird epoxy, but the Hexion 815c, with its dielectric strength of 1 MV/cm could

acceptably with stand the 400 kV/cm peak fields present in close proximity to the corona ring. The electrostatic simulation results of the second iteration can be seen in Figure 6.6.

The second corona ring design iteration further reduced FEF present in the MU100B material to 1.36 times the average field. A substantial reduction when compared to the FEF of 2.5 X's the average field from the first design iteration. The low FEF of the second iteration field shaper suggest that the maximum fields present in devices employing that electrode would be around 170 kV/cm, 3.5 times smaller than the peak fields present in devices with flat electrodes. Such a substantial field reduction prompted physical testing of the second generation field shaper.

Figure 6.6: Electrostatic model of the second iteration field shaping electrode. The major inner radius of the corona ring was expanded to give 0.1 cm of separation between the field shaper and the MU100B, allowing the fields in the MU100B to be less distorted by geometry changes.

A 3D model of the second generation field shaper was completed and sent to a machine shop to be precision machined and polished. A conceptual cross section of a 2 cm capacitor employing the second iteration field shaping electrode can be seen in Figure 6.7.

The only difference between what was simulated and what was fabricated is the addition of a through hole in the center of the corona ring electrode to allow a press fit connection to be placed on the base electrode making a more secure connection with the dielectric and a very small in step on the bottom face of the electrode to allow for concentric assembly with a MU100B disk.

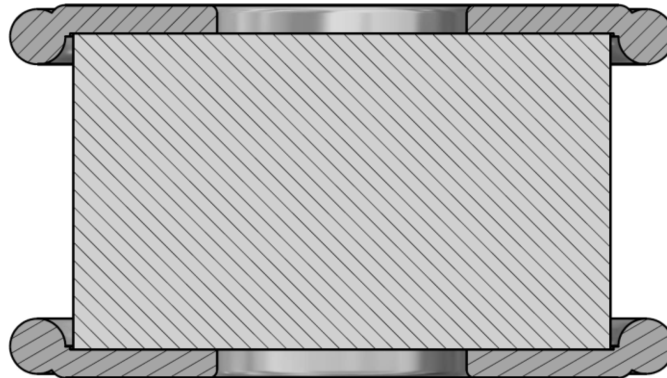

Figure 6.7: A conceptual cross section of a 2 cm thick capacitor prototype employing the machined version of the second iteration field shaper.

6.2.2.1 Second Iteration Field Shaping Electrode Physical Testing

Physical assembly of the second iteration proved to be the second iteration's shortcoming. The electrode was bonded to the MU100B substrate through the use of a conductive silver epoxy. As was found out in attempts to assemble the supposed 250 kV prototype, the second iteration field shaping electrode was not designed with physical implementation in mind. Uncontrollable and unrecoverable adhesive overflow from electrode-field shaper bonding, coupled with insufficient outgassing from under the corona ring diminished any gains the field shaping corona rings would have given. Physical devices fabricated with these parts under these conditions still broke down at an average field level of 80 kV/cm, similar to their flat electrode counterparts. Images of the silver epoxy overflow and insufficient air removal can be seen in Figure 6.8 and Figure 6.9,

respectively. The breakdown channel resulting from inadequate control of the capacitor-field shaper junction is visible in each image as well.

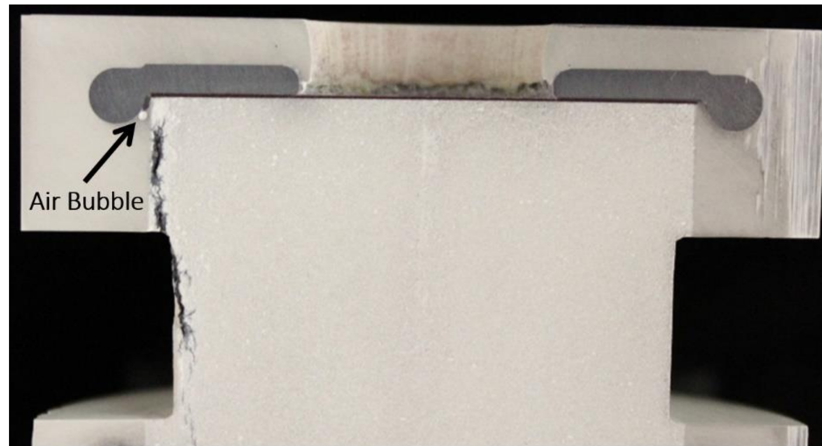

Figure 6.8: Physical shortcomings of the second iteration field shaping electrode trapped air bubbles under the corona ring and allowed for conductive adhesive overflow, resulting in no mitigation of edge breakdowns.

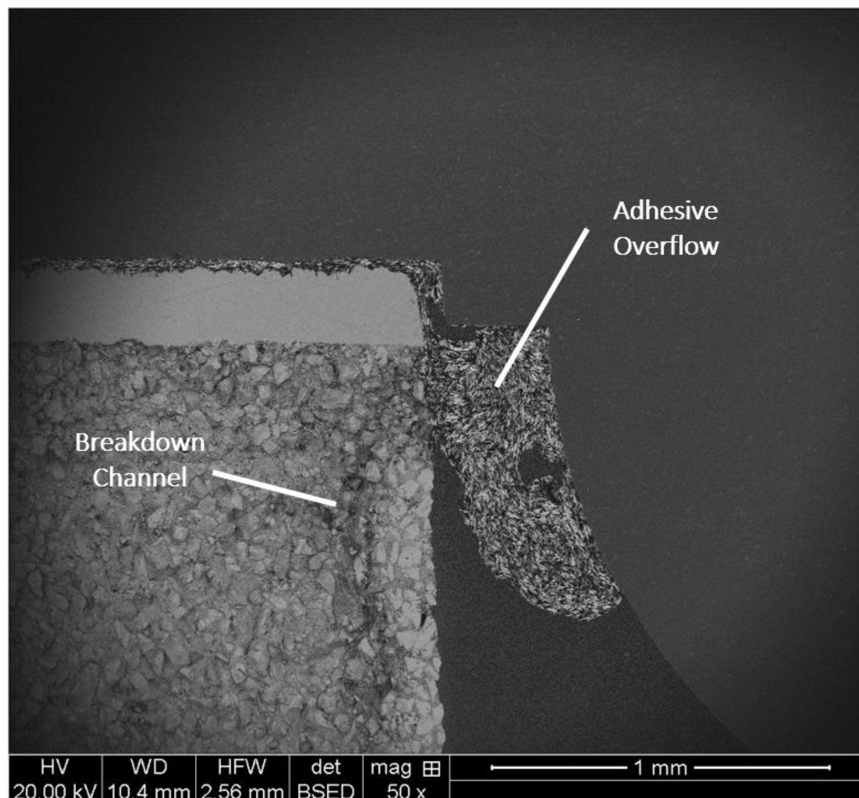

Figure 6.9: SEM image of the first application of a field shaping electrode. Insufficient control over the capacitor-field shaper junction allowed for adhesive overflow, which resulted in premature electric breakdown (arcing can be seen as the darker path originating at triple point and extending downward within the MU100B).

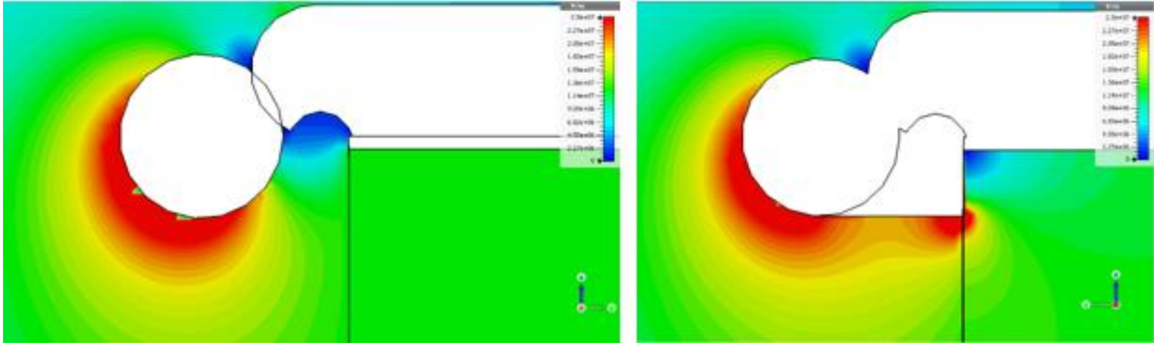

Figure 6.10: Side by side comparison of ideal assembly of a field shaping electrode (left) and an uncontrolled interface (right). It is visible that the overflowing adhesive induces a large field into the dielectric, which is similar in field magnitude to the flat electrode topology.

Further electrostatic modeling of a field shaping electrode which has experienced conductive adhesive overflow (Figure 6.10) shows why the physical implementation process of the second iteration field shaper is inadequate. The adhesive overflow imparts a FEF in the MU100B similar to that of a flat electrode, generating a triple point that is not shielded. This prompted a redesign of the field shaping electrode. The third design strove to maintain the electrical characteristics in the modeling environment but make controlling the physical field shaper-electrode junction possible.

6.2.3 Final Field Shaping Electrode Iteration

In addition to improving the field shaper design electrically, modifications in this iteration have been made to the method of attaching the field shaper to the metalized disk. In this iteration, a novel brazing process was developed, and has been employed ever since. The process is explained in section 3.3. The field shapers are bonded to the metalized MU100B disks through a eutectic solder, which is soft enough to allow for the coefficient of thermal expansion mismatch between the nanocomposite, base electrode, and field shaping electrode. The field shaper and disk are aligned during the brazing process using a jig which aids in concentric assembly. The advantage of using solder, opposed to an epoxy, to bond the field shaper to the capacitor is the fact that the solder can be reheated locally,

enabling removal from unwanted areas. Results suggest that a much cleaner field shaper-electrode interface is realizable, as shown in Figure 6.11.

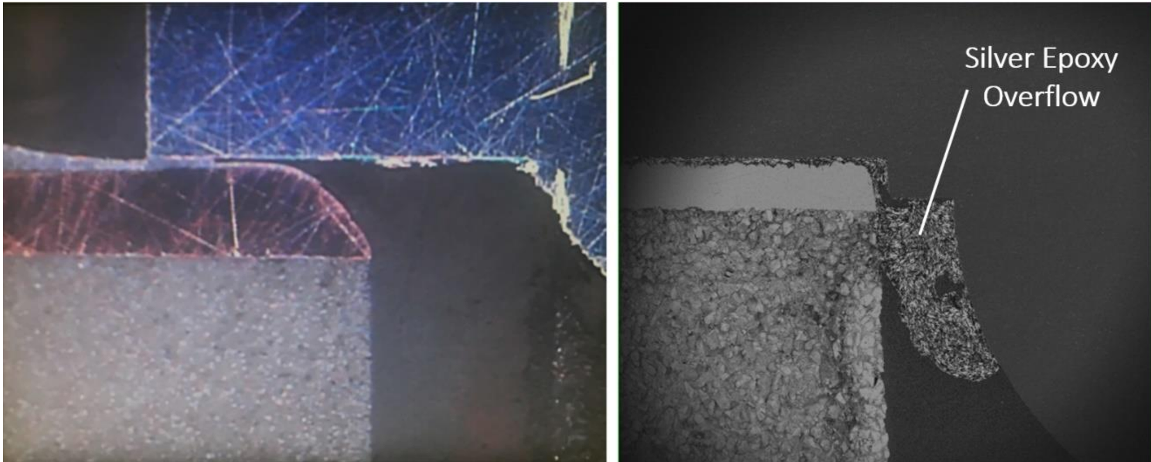

Figure 6.11: Two iterations of field shapers physically assembled. The second iteration field shaper (right) had problems being attached as seen by the large amount of epoxy overflow which lead to premature breakdown. It is evident the final iteration (left) has mitigated that issue, allowing a much cleaner edge to be manufactured.

Beyond a new field shaper application procedure, the final iteration field shaper was redesigned in CST. The design incorporated the machinists input to make it easier and cheaper to machine while not significantly altering the electric effects. The big addition to the final field shaping design is the addition of many small holes around the corona ring. The small holes are intended to allow air to escape from under the corona ring when encapsulating. This corrected another shortcoming of the second iteration.

Coupling the air release holes with a new epoxy hardener designed to do two things: double the work time of the potting material and to improve dielectric strength of the resulting material to >1 MV, the field shaper-capacitor interface should be very well maintained and remain viable under a wide range of electrical stresses. The longer epoxy work time allows vacuum to be pulled, as described in section 3.4, on assembled prototypes for about five hours enabling more complete void removal from the epoxy matrix.

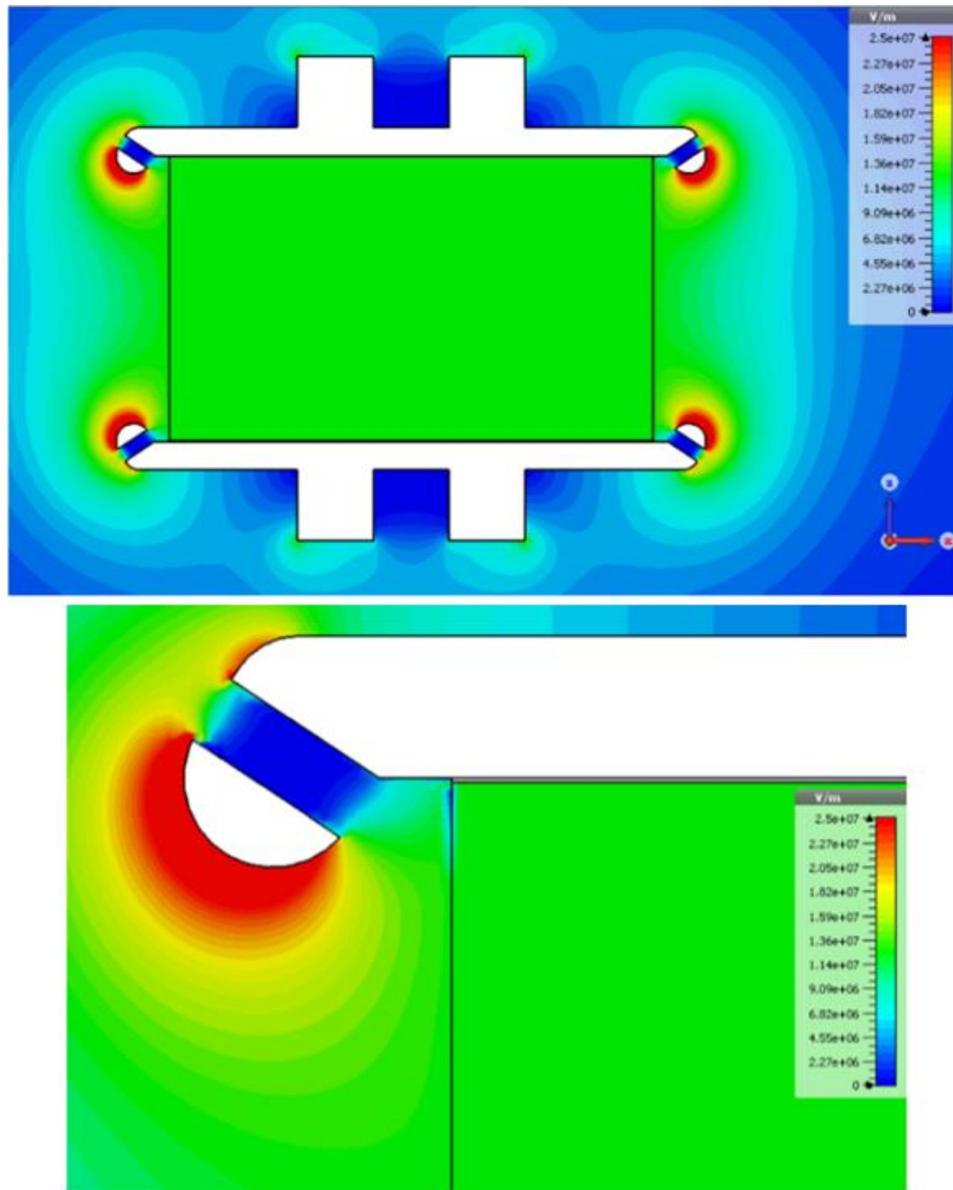

Figure 6.12: Electrostatic model of the final field shaper iteration. This design, coupled with an advanced method of attachment, improves device FEF and clean bonding improves dielectric strength.

The final iteration field shaper can be seen in the electrostatic model shown in Figure 6.12. The slight field shaper redesign further reduces the FEF in the MU100B from 1.36 (in the second iteration) to 1.11 times the average electric field. However, the redesign does place a larger field stress on the encapsulant epoxy, due to the radius of the corona ring not continuing all the way around to the top of the electrode. This change was made

in order to make the air release holes easier to precisely locate and drill. The FEF present in the epoxy is on the order of 3.87 times the average field, suggesting a peak field in the epoxy of 484 kV/cm which is approximately half of the literature value for on the Hexion 815c epoxy's dielectric strength [4].

After several implementations of scaled capacitor prototypes that employed the final iteration of field shaper, it was found that some trials had insufficient solder to fill the full gap between electrode and field shaper as shown in Figure 6.13.

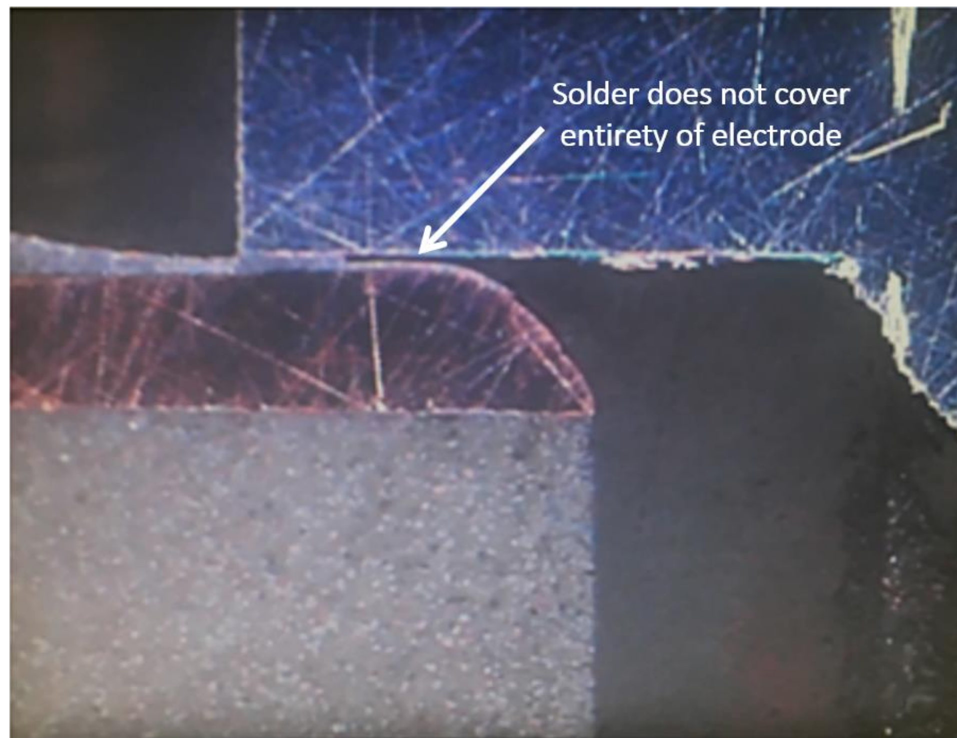

Figure 6.13: Small gap separating top hat and disk around the edge of a prototype, a phenomenon found in some full size capacitors resulting from insufficient solder when adhering the top hat to the disk electrode

In order to gain an understanding of this difference from the calculations before full scale tests were implemented, CST models were utilized in order to understand the effect on the triple point FEF. A gap between the disk electrode and the field shaper, which should be filled with solder, but is in this case filled with encapsulant, was modeled, simulated

and compared to unaltered models. It is evident from Figure 6.14 that the field values in and around the MU100B did not drastically change due to a lack of solder at the top hat-electrode edge.

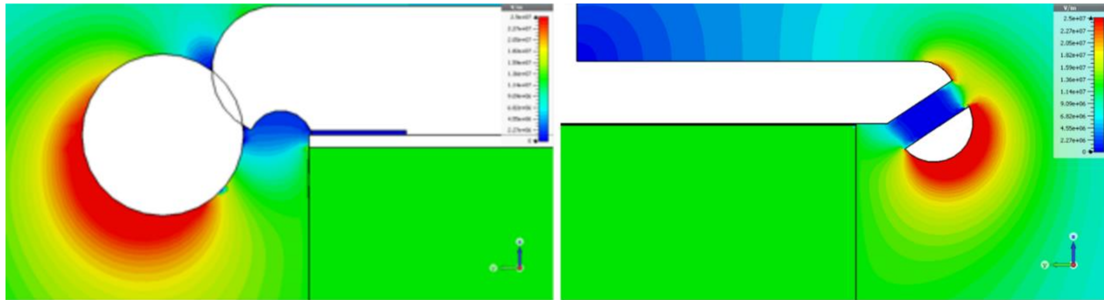

Figure 6.14: Model of how electric fields are affected when solder joining the field shaper to the electrode is incomplete at the edge. The results of the model suggest minimal changes in the resulting fields.

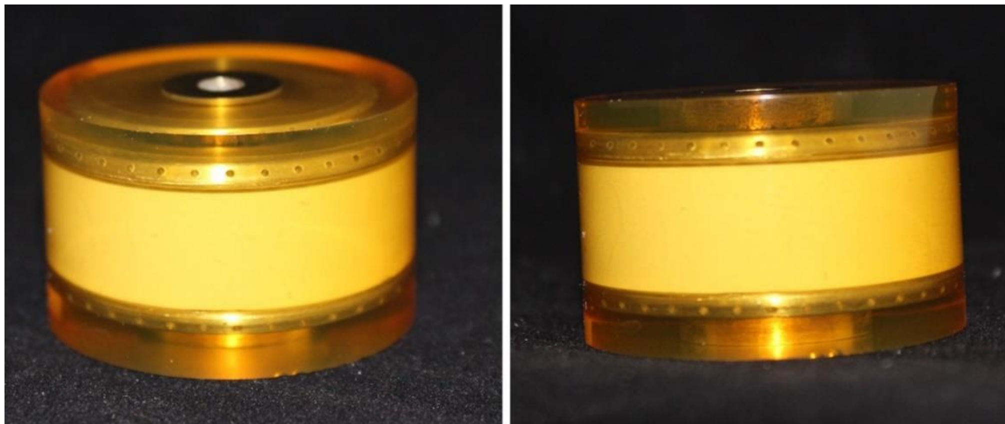

Figure 6.15: Scaled MU100B substrates coupled with the final field shaping electrode and encapsulation.

Further physical assembly and testing showed that the final iteration field shaping electrode allowed for clean, effective adhesion to the nanodielectric disks and allowed the field shaping electrode to work as intended. With the use of this field shaping electrode, the average breakdown of scaled MU100B prototypes has been improved from 80 kV/cm to 117 kV/cm on average for the 2 cm thick ultra-high voltage substrates. This increase in dielectric strength is approximately 46% higher than the scaled material with flat electrodes. Further confirmation of the field shaper's effectiveness was seen after analysis

of tested devices failure modes. All tested devices with field shaping electrodes of this type showed bulk dielectric failure in the MU100B substrate, suggesting that the field enhancements at the triple point were no longer the cause of device failure, Figure 6.16.

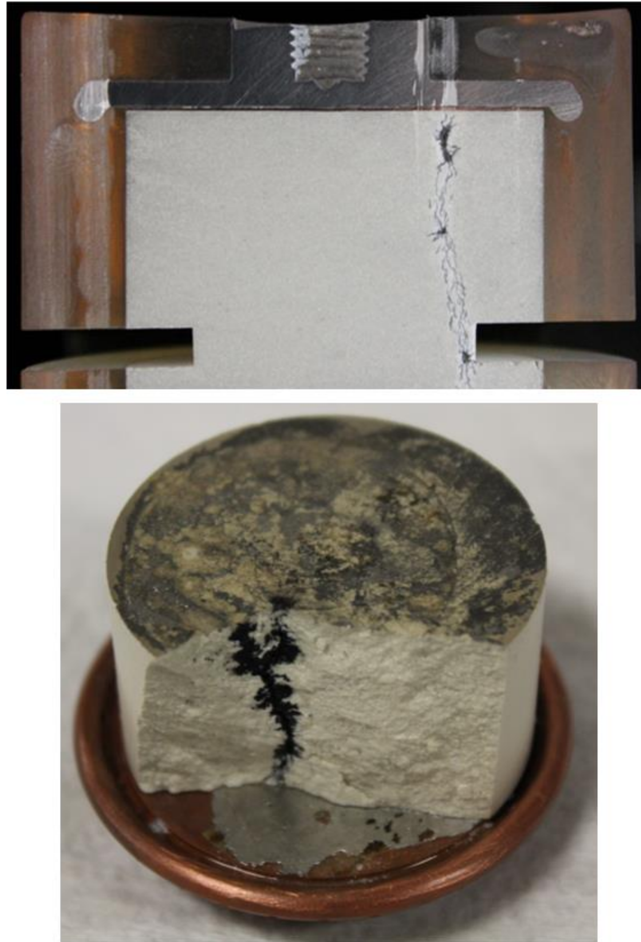

Figure 6.16: Images of two scaled MU100B ultra-high voltage substrates after undergoing breakdown testing. Testing of these devices proved the effectiveness of the field shaping electrode by a 46% increase in average breakdown field and moved the failure mode into the bulk of the MU100B, suggesting field enhancements are no longer the cause of device failure.

The usage of this field shaping electrode in the development of full-scale ultra-high voltage capacitors enables consistent high field operation and allows for 500 kV – 1 MV capacitors, several times smaller than commercially available counterparts, to be fabricated. The design, development and testing of full-scale MU100B ultra-high voltage capacitors will be discussed in the next chapter.

References – Chapter 6

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Chapter 7. Ultra-High Voltage MU100B Capacitors: Modeling, Development, and Evaluation

The requirements for the final deliverable in this ultra-high voltage capacitor development effort was required for the PEVS program. The Joint Non-Lethal Weapons Directorate (JNLWD) required two capacitors with specifications as follows: 130 pF with 500 kV hold off that could survive 50% - 80% voltage reversal with a shot lifetime in excess of 10^4 discharges. Instead of building these capacitors as single MU100B based devices, a modular capacitor was built which was assembled into the 130 pF capacitor. Each sub-module for the final modular capacitor is approximately 16 pF and is rated in unipolar mode for 750 kV and in bipolar mode (ringing operation) for 550 kV operation. The projected lifetime at full voltage for the full-scale assemblies is 10^5-10^6 shots. The subsequent sections of this chapter will detail how two, fully functional, 500 kV-plus capacitors were designed, modeled, developed and tested. The development resulted in the full-scale devices being 2.4 times smaller than anything available commercially with the same or similar specifications. Furthermore, after success of the full-scale devices, additional sub-modules (of the same size and smaller) were fabricated and tested with the performance of tested elements exceeding 1 MV at reduced lifetimes.

7.1 Ultra-High Voltage Capacitor Design and Modeling

In prior work with MU100B small scale capacitors, lifetime goes up dramatically when operated at field levels equal to 80% of the average breakdown field [1]. Thus, with full scale MU100B capacitors having an average breakdown field of 117 kV/cm, as detailed in section 6.2.3, a 20% derating for long lifetime operation makes the operational fields of scaled MU100B capacitors employing the developed field shaping electrode equal

to 94 kV/cm. Then, to account for the voltage reversal, or bipolar ringing, of the applications discharge an additional 35% derating was applied to the scaled MU100B capacitors [2]. The derating for voltage reversal made the operational field for long lifetime operation while undergoing greater than 50% voltage reversal equal to 62.5 kV/cm. Using the calculated long-life time and voltage reversal field level of 62.5 kV/cm, 8 cm of dielectric thickness are required to fabricate a 500 kV capacitor.

Therefore, to achieve a 500 kV, long lifetime capacitor capable of sustained operation under voltage reversal, the device must be able to continuously operate under maximum unipolar pulses of 750 kV and should have a short lifetime unipolar voltage rating of 940 kV [3].

Since MU100B substrates produced after the material scaling effort can be produced reliably at thicknesses up to 2 cm, four MU100B ultra-high voltage substrates must be bonded together to achieve the desired dielectric thickness of 8 cm. This device design was then modeled in CST's electromagnetic studio in the simulation environment described in section 6.1.2. The results of that simulation are presented in Figure 7.1. The model employed four 2 cm thick MU100B substrates with only sputtered silver electrodes (simulated with ε_r=160) stacked together serially with a thin layer of eutectic solder adhesive (thickness equal to 50 μm) between each disk and field shaping electrode.

Upon analysis of the four-stack electrostatic model, it was determined that the design was sufficient to meet the required specifications. According to the model, the peak field in any piece of MU100B is equal to 89 kV/cm, which is acceptably less than the experimentally determined breakdown field of devices of 117 kV/cm. The field enhancement factor in the MU100B in the thicker device was increased slightly from 1.11

times the average field in a 2 cm thick prototype to 1.424 times the average field in the 8 cm thick topology.

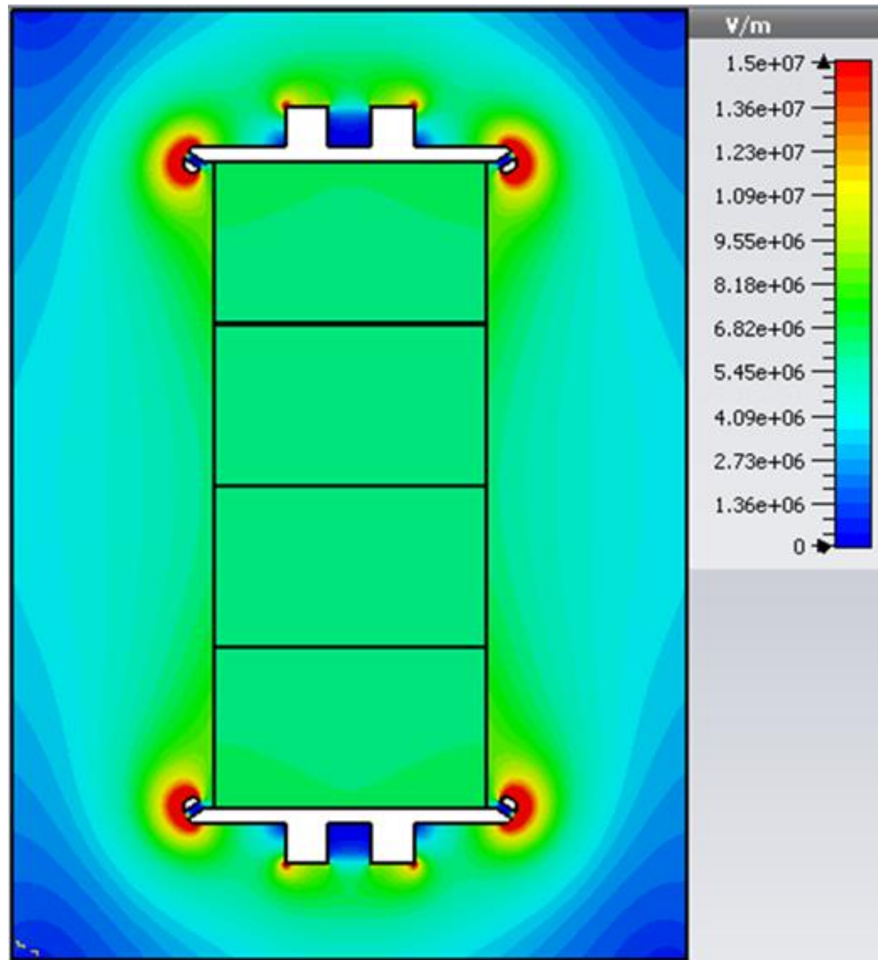

Figure 7.1: Electrostatic model of a single 500 kV capacitor sub-module. The peak field present in any of the four pieces of MU100B is 89 kV/cm, well below the average breakdown field of these devices, 117 kV/cm.

The model calculated the capacitance of the 3.4 cm diameter, 8 cm thick stack to be 15.5 pF. To meet the contract specification, a capacitor design with multiple 8 cm stacks connected in parallel was employed. If the individual 500 kV capacitor stacks, or sub-modules, have capacitance values near 15.5 pF, at least 9 must be joined in parallel to exceed the requirement of 130 pF. Thus, a simulation was run with nine stacks connected in parallel. The arrangement was kept as simple as possible with three rows of these sub-

capacitors to keep modeling and fabrication time of the full-scale development at a minimum. The results of the preliminary full-scale model can be seen in Figure 7.2. Only the cross section of one row is shown, the middle row, but analysis showed each row had nearly identical cross-sectional field patterns. Grouping the sub-modules as such did not change the peak fields present in the design. The peak field in any piece of MU100B was statistically determined to be 90 kV/cm which is about the same as the single element model. Arranging the sub-modules in this cubic formation subjects the sub-modules in the middle of the rows to considerably less high field area than the modules on the four corners. The capacitance of the full-assembly was calculated to be 139.9 pF, slightly over the target. Fabricating a prototype with higher capacitance than required at low voltage is necessary as the dielectric constant of MU100B has a 5-10% voltage coefficient. Meaning the dielectric constant of the nanodielectric will be reduced somewhat at high voltages.

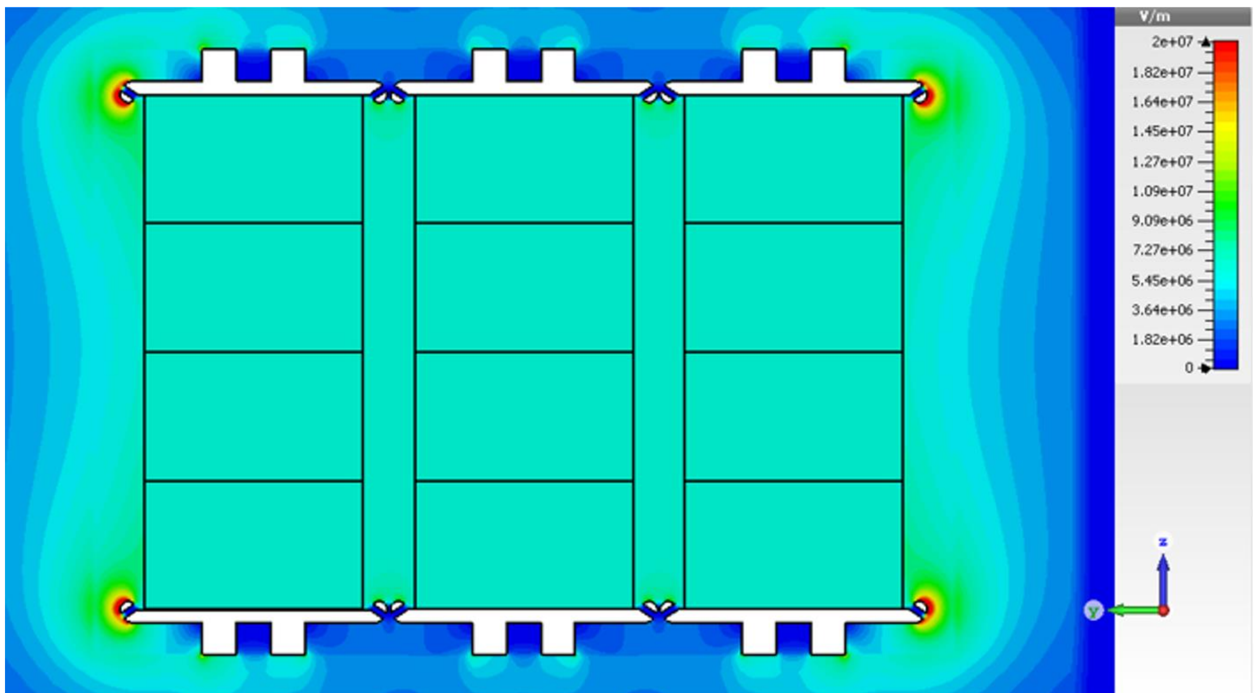

Figure 7.2: Initial model of a 130 pF capacitor assembly. The middle of three rows or three sub-capacitors is shown in this model. Joining the capacitors in this fashion did not change peak field magnitudes in the MU100B from the single sub module simulation.

7.2 Ultra-High Voltage Capacitor Element Fabrication and Assembly

When voltage hold off requirements force multiple substrates to be seriesed, it is crucial for the fabrication process to not induce any extra field enhancements or mechanical stresses in between the stacked substrates. Proper stacking of dielectric substrates demands all of the cylindrical disks be stacked concentrically. Further, there must be a solid equipotential layer joining each substrate to force the fields to grade evenly throughout the substrates. In assembly tests (as discussed in section 3.3 and section 6.2.2), it was found that conductive epoxy was too hard to contain and was not conductive enough throughout the bulk to be employed in this fashion. Thus, an advanced brazing technique was developed to join the substrates (section 3.3). A eutectic solder was employed as the brazing material which provided exceptional conductivity as well as remaining soft enough to account for variations in different materials' coefficients of thermal expansion.

When joining substrates to either a field shaping electrode or another substrate a simple jig was used to ensure concentric stacking, shown in Figure 7.3. The jig employs two vertical Teflon rods, which have been machined on the top and bottom to allow for the larger diameter field shaping electrodes to reside on the same center line as the MU100B disks. Simply pushing all components flush against the rods ensures concentric alignment. The result of using the stacking jig is capacitor sub-modules that are consistently assembled, allowing for better performance and a more consistent final product than hand stacking. An assembled ultra-high voltage stack can be seen in Figure 7.4.

After stacking, as a consequence of proper brazing, there will be excess solder adhered to the outside of the MU100B stack. This excess solder was removed by sanding. However, solder overrun from the field shaper is blocked by the corona ring and must be

locally heated and removed with a tool. Complete removal of solder in the field shaper-electrode junction was found to be crucial for voltage holdoff reasons.

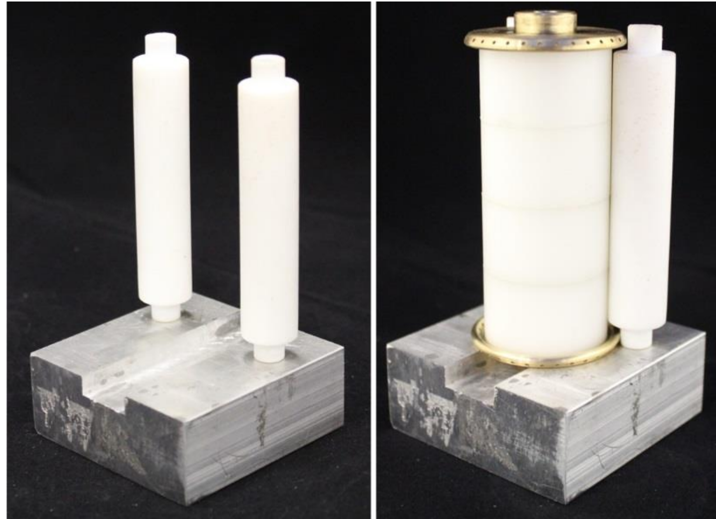

Figure 7.3: Stacking jig used to ensure concentric stacking of 500 kV capacitor elements (left). The jig is shown with a stacked element on right.

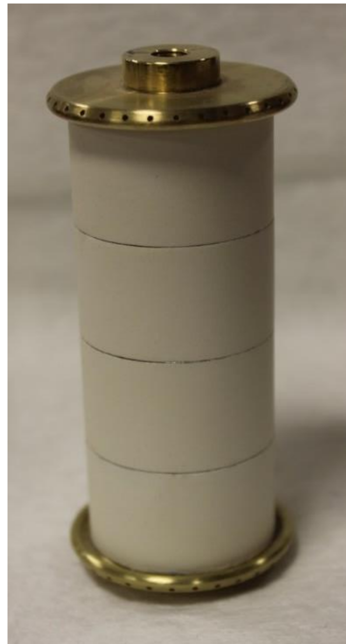

Figure 7.4: Advanced assembly methods allow for stacking of dielectric substrates, making assembly of ultra-high voltage capacitors possible.

After ultra-high voltage stack assembly and polishing, the capacitor sub-modules are encapsulated by the methods described in section 3.4. Encapsulation provided stability

to the assemblies, as well as reduction of the possibility for mechanical shock damaging a solder connection. The encapsulant used has previously been demonstrated to withstand sufficiently high electric fields while remaining mechanically robust. Thus, the encapsulant ensures no carbon build up occurs between electrodes over the course of tens of thousands of shots. Images of encapsulated sub-modules can be seen in Figure 7.5.

Figure 7.5: Ultra-high voltage capacitor elements are individually encapsulated to ensure long life time electrical performance and to add mechanical robustness to the assemblies.

Upon full cure of the potting epoxy, a fully functional 500 kV sub-capacitor was assembled. The dimensions of the sub-modules are very small compared to other devices capable of performance at such high voltages, Figure 7.6. To finish the full-scale assembly, fabricated capacitor sub-modules are joined together forming a full-scale prototype. Prior to joining, the assembled sub-modules are grouped together based upon total thickness and measured capacitance. This sorting step is done to keep the field variations at a minimum across the entire prototype. The measured substrate thickness and dielectric constant of each sub-module was used in CST simulations to optimize placement of each with in the

final assembly. Since the peak fields are lower at the middle position of each row, the shortest stacks are placed there, with the shortest of all being assembled in the center of the cube. The exact model developed for placing the sub-modules in the final prototype is shown in Figure 7.7. The most dramatic difference between the exact model and the generic models displayed earlier is the simulated capacitance value, which is several picofarads larger than the generic models because the manufactured MU100B substrates employed in this effort had dielectric constants ranging from 160 to 210, averaging considerably larger than the 160 which was used in the generic models.

Figure 7.6: An encapsulated 500 kV capacitor prototype (center) is shown next to a 500 kV assembly of TDK door knob capacitors (left) along with a ruler for size reference. The capacitor development effort resulted in 500 kV capacitors that fit in the palm of the hand.

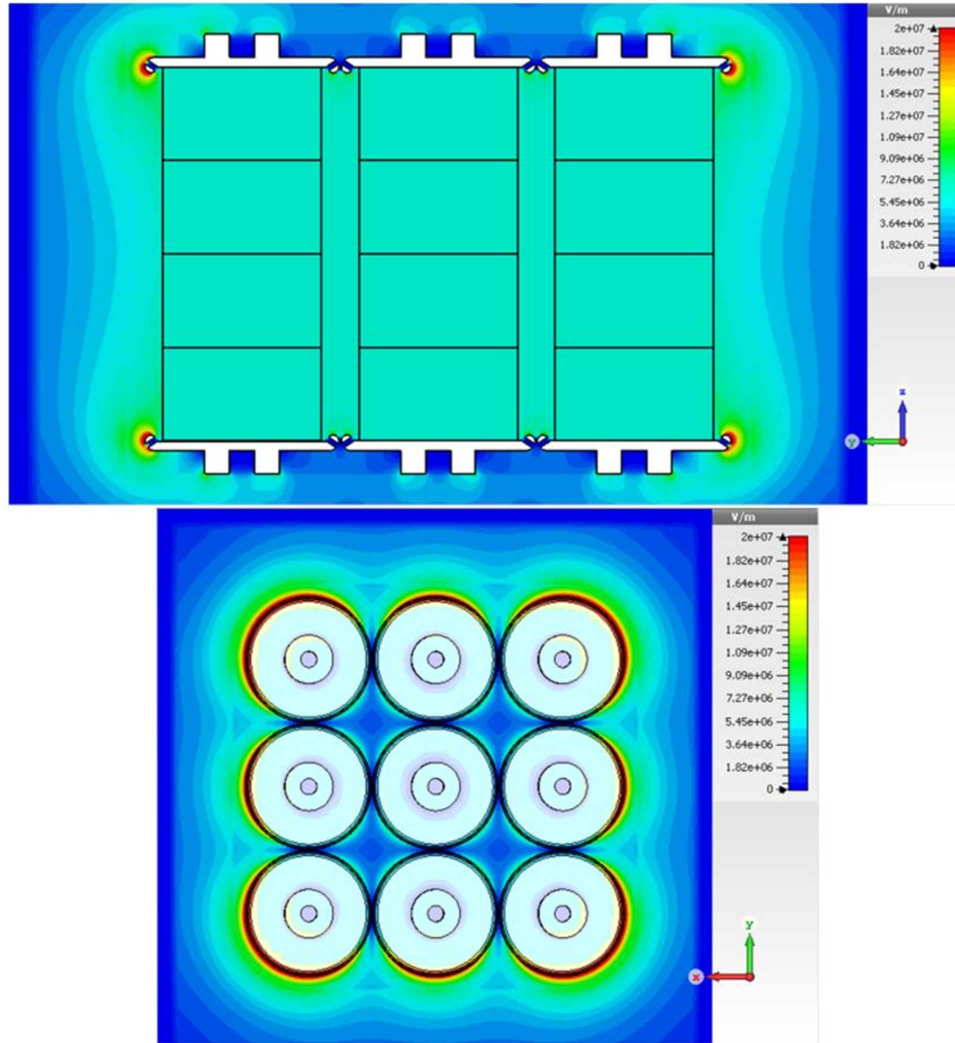

Figure 7.7: Electrostatic model of the cubical arrangement of the nine sub-module capacitors used to assemble the final 130 pF prototypes. Models at this stage were used to simulate the dielectric constant of the MU100B substrates employed to aid in placement of the individual sub-modules in the final assembly.

The nine sub-modules are joined in parallel by connecting each to a top and bottom plate electrode. One of the fully assembled transfer capacitors delivered to JNLWD is shown in Figure 7.8. A final transfer capacitor assembly has a capacitor volume of 1,767.15 cm^3, which is a substantial 2.43 X's volume reduction when compared to the commercial capacitor being used for the PEVS program currently (plastic case capacitor volume 4,301.60 cm^3). Transfer capacitor volume could likely be reduced further with a more sophisticated arrangement of capacitor sub-modules.

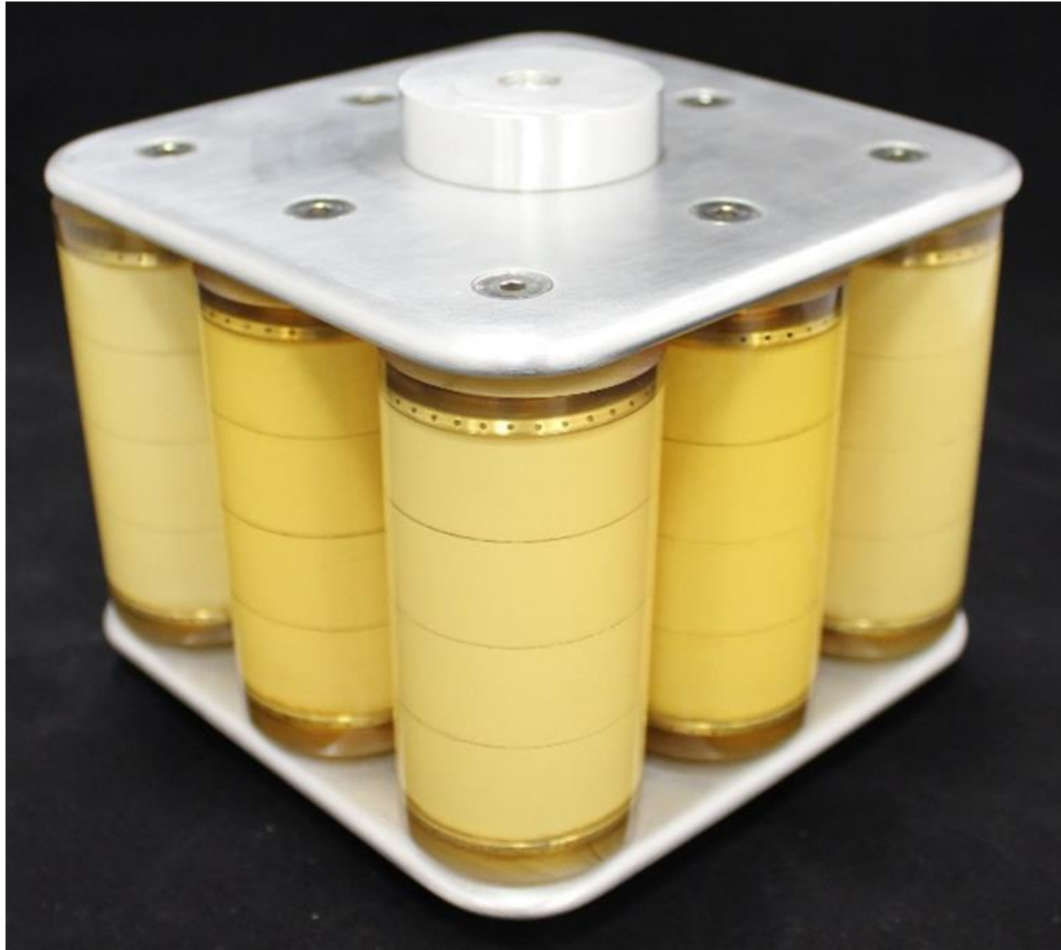

Figure 7.8: One of the final 130 pF, 500 kV prototype transfer capacitors. The prototypes weigh 5.5 kg (12 lbs.) and are essentially a 14 cm cube.

Table 7.1 and Table 7.2 show the MU100B substrate and sub-module information for transfer capacitor #1 and transfer capacitor #2, respectively. Spare sub-modules were included in the prototype shipments. The spare capacitor modules were intended to be used to characterize the PEVS based test stand and/or be used to gather overvoltage data if the full-scale devices met/exceeded specification.

Table 7.1: Individual sub-module information for Transfer Capacitor #1.

Transfer Capacitor #1 - Stack Information						
Stack Number	Disk Name	Disk Thickness (mm)	Permittivity		Stack Capacitance (pF)	Status
1	110917-4	19.90	205.22	Stack of 4	19.2	Assembled in Prototype
	110917-5	19.61	201.50			
	111717-1	20.37	206.01			
	113017-1	20.22	198.46			
2	112817-3	19.64	198.14	Stack of 4	17.8	
	112817-1	19.51	196.34			
	112917-1	19.84	199.42			
	111017-1	19.35	192.57			
3	112817-4	19.74	194.48	Stack of 4	17.2	
	111017-3	19.84	193.50			
	113017-2	19.94	193.73			
	110917-3	20.11	195.38			
4	110917-1	20.05	193.55	Stack of 4	13.5	
	110817-2	20.08	189.84			
	112917-2	19.81	188.52			
	113017-3	19.90	188.39			
5	111017-2	20.06	189.40	Stack of 4	16.7	
	113017-4	19.98	187.65			
	112817-2	19.67	185.48			
	110817-3	19.92	185.40			
6	110817-1	20.00	184.36	Stack of 4	16.8	
	111717-3	20.20	181.68			
	110917-2	19.94	179.09			
	112817-5	20.67	183.85			
7	012218-2	20.01	177.48	Stack of 4	15.3	
	012218-1	20.27	186.59			
	012218-5	19.67	186.04			
	012218-3	19.64	177.47			
8	113017-5	19.94	174.13	Stack of 4	16.9	
	112817-6	20.82	178.71			
	112917-3	20.24	167.43			
	120517-3	20.37	168.00			
9	113017-6	20.15	160.67	Stack of 4	17.5	
	120517-8	20.18	159.66			
	120517-7	20.78	157.94			
	120517-5	20.54	154.07			
10	012418-3	19.81	181.87	Stack of 4	19.5	Spare
	012318-5	19.70	186.79			
	012318-3	19.86	182.03			
	012318-2	19.74	181.72			
11	012518-3	19.56	177.02	Stack of 4	20.2	
	012518-2	19.65	180.42			
	012418-5	19.46	178.15			
	012518-1	19.36	175.01			

Table 7.2: Individual sub-module information for Transfer Capacitor #2.

Transfer Capacitor #2 - Stack Information					
Stack Number	**Disk Thickness (mm)**	**Permittivity**		**Stack Capacitance (pF)**	**Status**
12	19.63	183.49	Stack of 4	19.7	Assembled in Prototype
	19.87	184.07			
	19.57	182.02			
	19.84	184.36			
13	19.99	183.02	Stack of 4	18.5	
	20.16	184.75			
	20.16	184.05			
	20.00	182.74			
17	20.02	177.42	Stack of 4	17.3	
	19.94	173.49			
	19.96	172.15			
	20.01	171.13			
18	20.33	173.36	Stack of 4	18.3	
	20.18	177.56			
	20.15	176.79			
	20.20	167.05			
19	19.73	195.91	Stack of 4	19.0	
	19.96	191.69			
	19.83	197.22			
	19.80	199.80			
20	20.19	180.18	Stack of 4	19.2	
	19.71	181.27			
	19.83	180.77			
	20.09	176.19			
21	20.00	190.20	Stack of 4	18.7	
	19.80	195.22			
	20.05	187.94			
	19.95	192.68			
22	20.14	184.22	Stack of 4	18.9	
	20.14	180.51			
	20.12	185.51			
	20.13	181.95			
23	19.84	187.45	Stack of 4	19.3	
	19.83	188.76			
	20.02	188.60			
	19.69	186.72			
16	20.17	179.98	Stack of 4	17.9	Spare
	20.00	181.05			
	20.17	180.78			
	20.18	178.74			

7.3 Ultra-High Voltage Capacitor Testing and Evaluation

7.3.1 Preliminary Lifetime Testing

As discussed in chapter 4, the capacitor test and evaluation capabilities at the University of Missouri's Center for Physical and Power Electronics do not meet the requirement for full testing voltage. Thus, for the preliminary tests, two disks of the size utilized in the 500 kV sub-modules were stacked. The two-disk stack was meant to be tested at 250 kV (half of the final prototype thickness being tested at half the final voltage). Testing at this thickness and voltage level will be subjecting the specimen to the same electric field magnitudes as the final full-scale prototype as verified by the two-disk model in Figure 7.9.

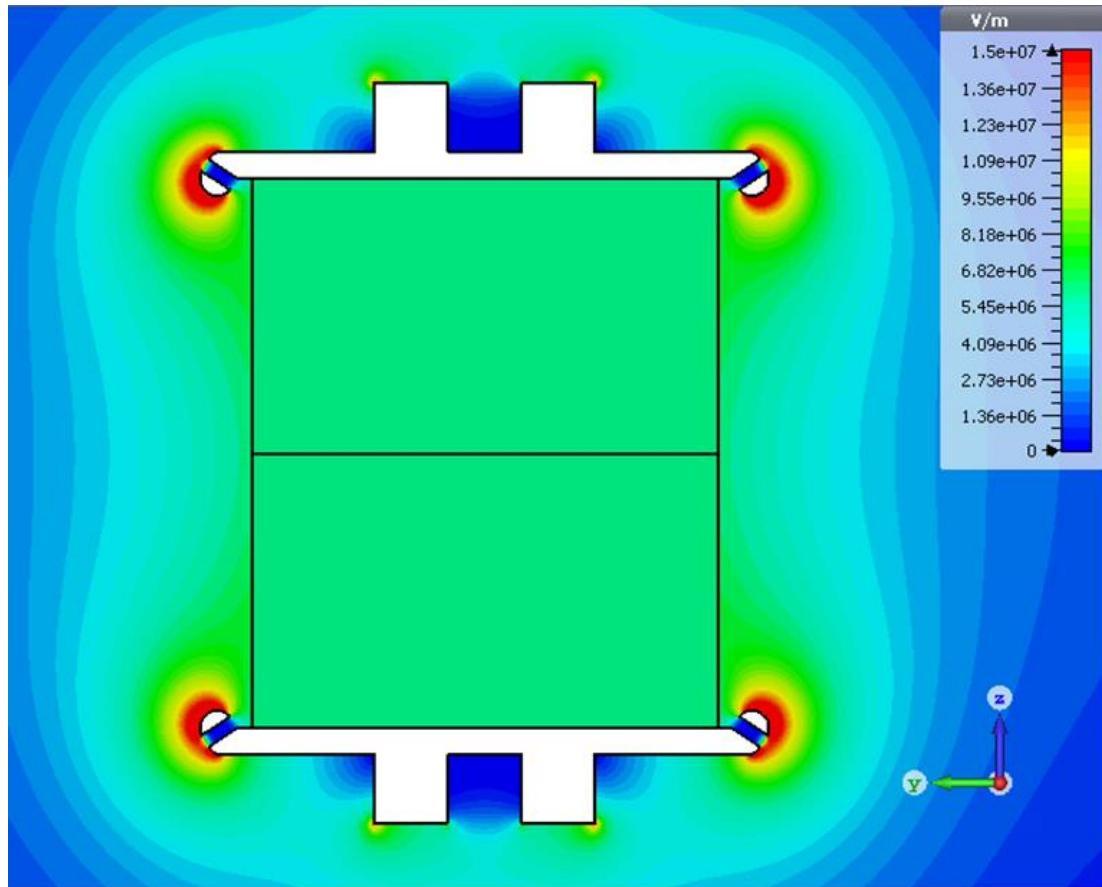

Figure 7.9: Electrostatic model of the half height device used for preliminary lifetime testing. The model confirmed the peak fields present in this configuration are similar in magnitude to a full thickness device when run at 500 kV.

Figure 7.10: The 3.4 cm diameter stacked capacitor that was tested for initial lifetime evaluation at 250 kV. The tests have been carried out on the capacitor as shown, unpotted, just submerged in oil, where it has withstood 10,000 shots from the 250 kV test stand. The image at the left is the capacitor before any testing. The image at the right is the same capacitor after surviving 10,000 shots. No signs of degradation have been observed.

Figure 7.10 shows the preliminary capacitor which has been tested in our 250 kV test stand and has withstood over 10,000 pulses without failure. The tests were carried out with the preliminary capacitor unpotted. The 250 kV test stand's pulse characteristics are substantially different than that of the final application as voltage reversal is not available and the high voltage is applied for a longer duration. The 1000th shot put on the preliminary 3.4 cm stacked capacitor waveform is shown in Figure 7.11 and is intended to illustrate the differences in our current test environment compared to the applications.

Figure 7.11: The 10,000th shot put on the preliminary stacked 3.4 cm capacitor. The voltage per division of the plot, including voltage divider attenuation, is 72.5 kV per division, giving a peak voltage of 256.7 kV. The time axis is 80 ns per division. Characterization of the test stand showed that voltage is left on the sample for ~10 μs.

7.3.2 Full-Scale Prototype (Transfer Capacitor) Testing and Evaluation

In July of 2018, I traveled to the Naval Surface Warfare Center in Dahlgren, VA to witness and assist in testing of two ultra-high voltage capacitors that were delivered to JNLWD. The delivered devices consisted of two full-scale Transfer Capacitors and several spare single sub-modules. The full-scale transfer capacitors fulfilled all of the specifications (500 kV operation, $> 50\%$ voltage reversal and 10^4 pulse lifetime or greater) for electrical performance. A photograph of one of the full scale prototype capacitors can be seen in Figure 7.12 along with the sub-module capacitors, nine of which comprise a full prototype, shown in Figure 7.13.

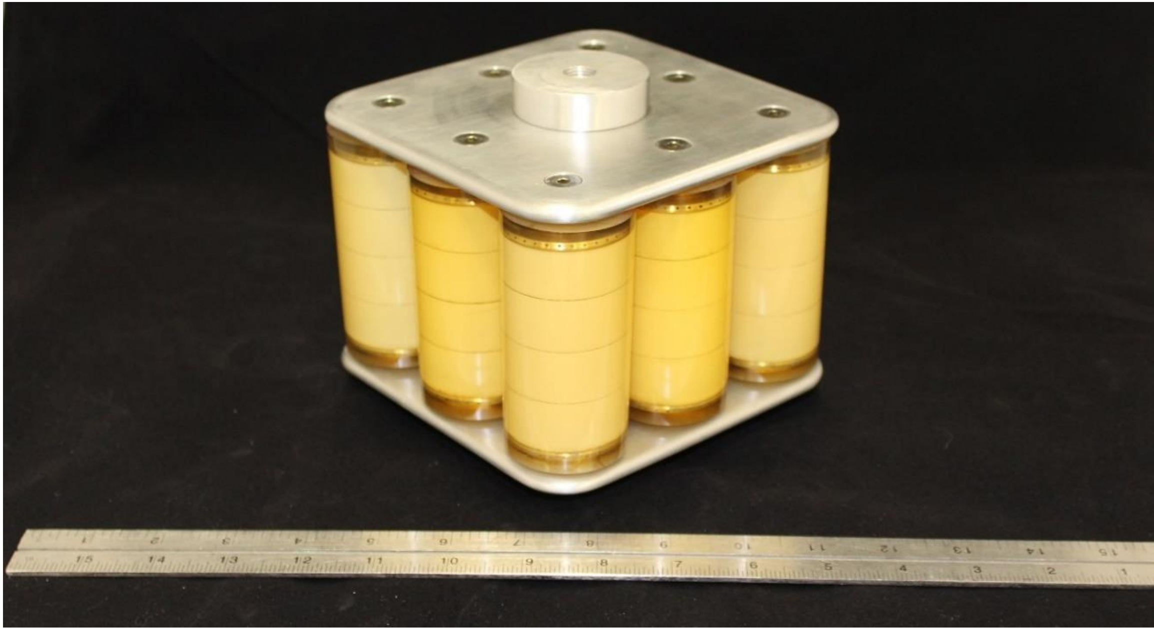

Figure 7.12: Photograph of an assembled 500 kV Transfer Capacitor with a ruler for size reference.

Figure 7.13: Photograph of various sub-modules which comprise the 500 kV capacitors. The sub-module capacitors are 9.5 cm in length with a diameter of 4.5 cm.

During the tests at NSWCDD, a test circuit was utilized to emulate the pulse characteristics of the PEVS module. The test stand was described in detail in section 4.4 and consists of a 15 stage Marx generator capable of pulse charging a matched capacitive load to nearly 600 kV and ringing it at a specific frequency with 55-60% voltage reversal, or, when subjected to an unbalanced load, could subject a small test capacitance to about 1

MV. The rise time of the system was approximately 50 ns with a pulse width on the order of a microsecond. The test stand was fully automated allowing it to run in a burst mode when shots were fired at a rep-rate of 100 Hz, with a burst length of 2 seconds. A 10 second delay period was programmed into the test stand to prevent overheating of the Marx generator.

7.3.2.1 Transfer Capacitor #2 Testing

The diagnostics on the test stand were calibrated prior to the test and evaluation of the 500 kV capacitors. To more closely emulate operation to that of the MU test stand, the test capacitor performance was verified with unipolar testing and minimal voltage reversal. The second transfer capacitor was incrementally tested to 500 kV with 10% reversal. A typical waveform is shown in Figure 7.14.

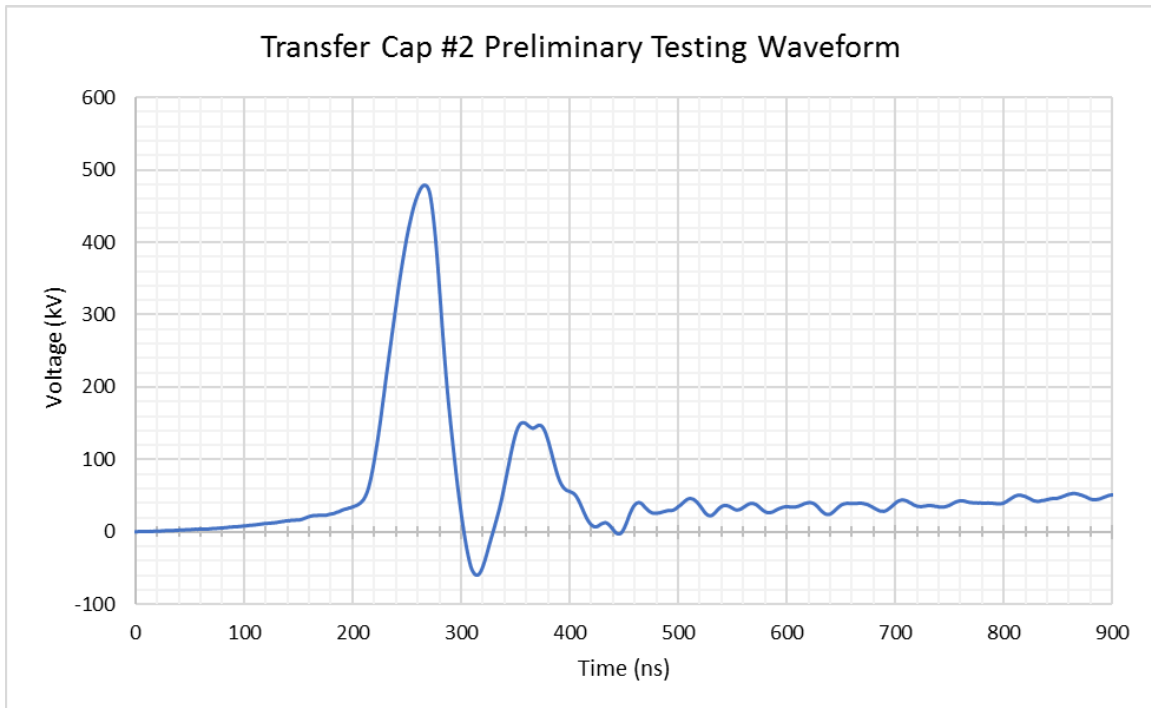

Figure 7.14: A typical unipolar waveform during the pulsed discharge tests. Initially Transfer Capacitor #2 was tested at low reversal, more closely emulating the test stands at UMC.

After successfully holding off 11,142 pulses with the test stand in the low reversal configuration, the test stand was modified to enable more reversal, about 35% reversal in this setup. The same transfer capacitor, Transfer Capacitor #2, was tested from ~300 kV with 35% reversal to nearly 500kV with 35% reversal. The capacitor under test withstood 5,681 pulses without failure. A typical waveform is shown in Figure 7.15.

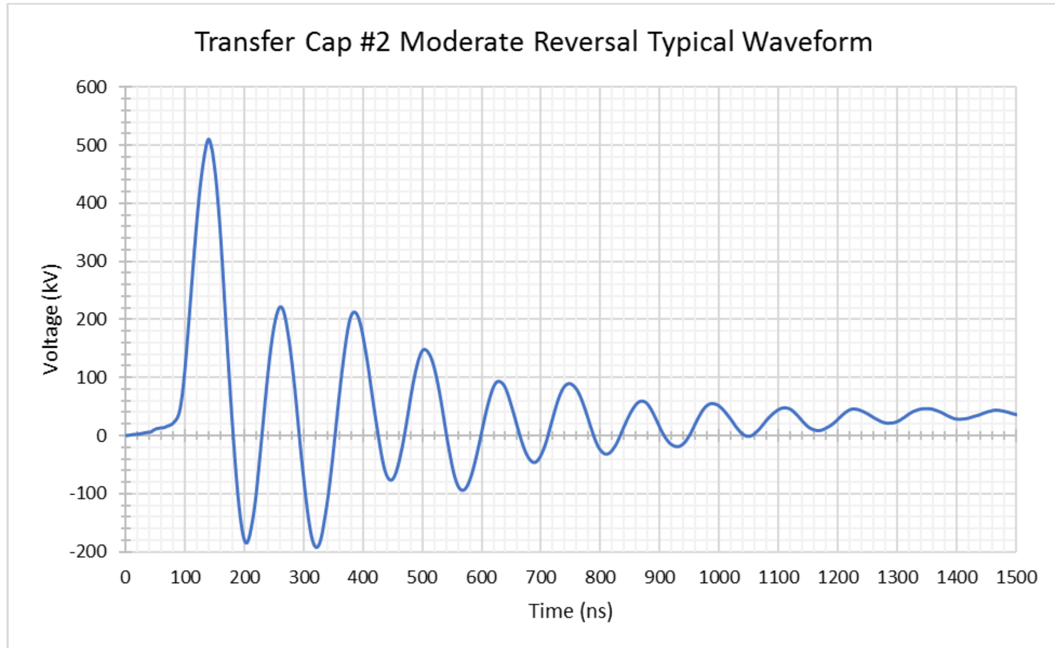

Figure 7.15: Typical waveform from the moderate reversal testing of Transfer Capacitor #2, reversal peak level equal to ~35% of positive peak voltage.

Upon successful completion of moderate reversal testing, the test stand was modified a final time to emulate the reversal magnitude of the transfer capacitors application, 55-60%. Trans Cap #2, which has been the subject of the low reversal and moderate reversal tests, was subjected to the full reversal tests. In total, the second transfer capacitor successfully withstood 18,828 pulses of near or greater than 500 kV with 55% reversal without any sign of degradation or failure. A typical waveform from one of those pulses is shown in Figure 7.16. During the tests the pulse charge voltage many times went above 550 kV.

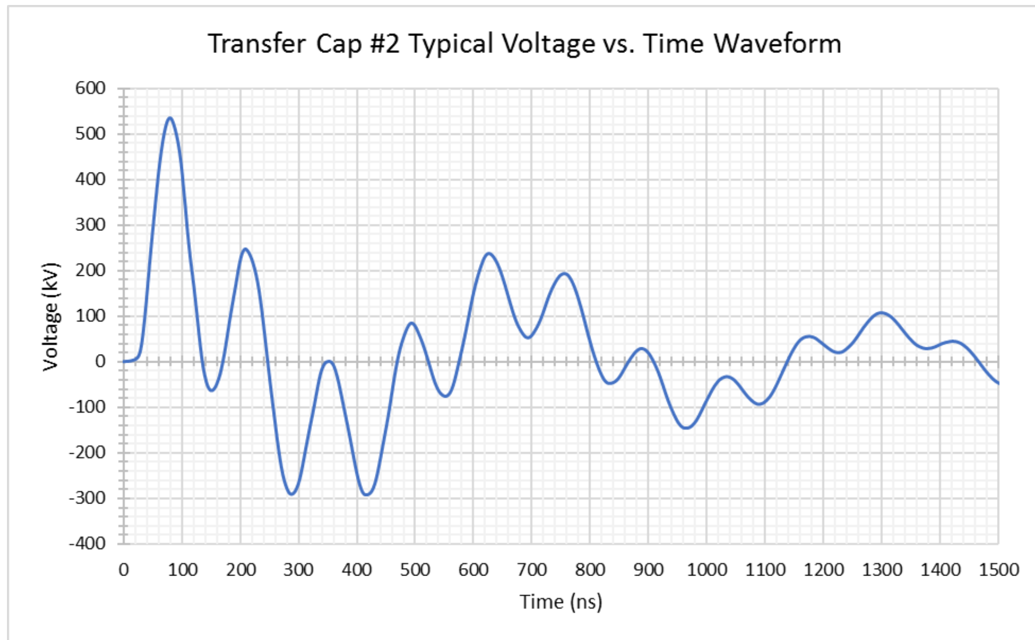

Figure 7.16: A typical waveform of the voltage pulses put on Transfer Capacitor #2. An average of 500 kV peak with 55% voltage reversal.

When the peaking switch in the test stand is closed, the capacitor under test rings as shown. Since the only capacitor in the RLC (resistor, inductor, capacitor) circuit in question is the capacitor under test, monitoring the ring frequency of the system yields a very precise indication of the health of the test capacitor. Any sustained changes in ring frequency will indicate if the capacitor has been degraded. A scatter plot of pulse ringing frequency versus time was used to monitor the health of the capacitor. If any substantial change in frequency was sustained, the device would be deemed degraded. Upon review of the ringing frequency versus time scatter plot for the full reversal test of Transfer Capacitor #2 (Figure 7.17), one can clearly see that the ring frequency remained constant throughout the entire test. The consistency of the ringing frequency from pulse to pulse suggests that the test capacitor performed reliably across all 18,828 pulses. Also visible in Figure 7.17 is the peak recorded voltage of the pulses. If the capacitor shorted out, the recorded voltage would be that of a short circuit, 0 V.

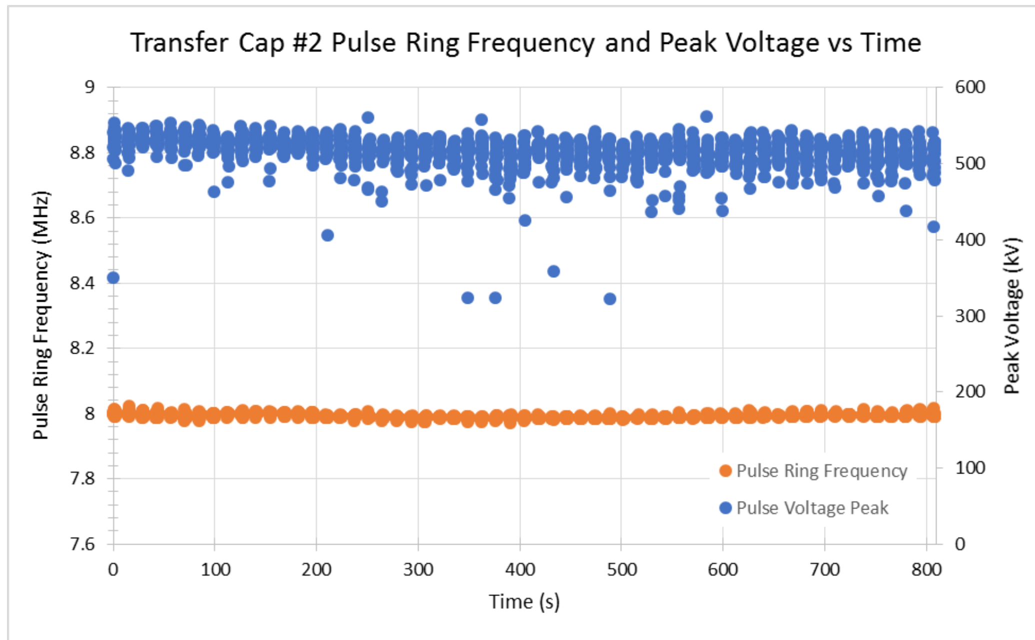

Figure 7.17: Ringing frequency and peak voltage of each full reversal pulse plotted against time. The consistency of the ringing frequency suggests the test capacitor performed remarkably consistently from pulse to pulse for the duration of the test. Further, the self-breakdown nature of the Marx bank is evident in the voltage peak scatter.

Due to the self-breakdown nature of the Marx generator and the peaking switch, the peak voltage of every shot is not identical. Further, during the full reversal tests, a 200 shot bursts were applied to the test capacitor at a frequency of 100 pps. The scatter is due to the deviation in the Marx discharge voltage. Since the capacitor development contract states the final prototype devices must be able to withstand 10^4 pulses with a peak voltage of 500 kV with 50% or greater reversal, it had to be verified that a minimum of 10,000 of the greater than 18,000 pulses applied to the second transfer cap were above 500 kV in voltage magnitude. Analysis of the voltage peak histogram, shown in Figure 7.18, suggests that approximately 9% of the recorded pulses had a voltage peak below 500 kV. Thus, of the 18,828 pulses applied, 1,698 of those had a voltage peak below 500 kV. Therefore, 17,130 pulses had voltage peaks of 500 kV or greater. Transfer Capacitor #2, having withstood 17,130 500 kV pulses with 55% reversal shows that it met full specification as

outlined by the contract with the funding agency. No further testing of that device was completed in this project.

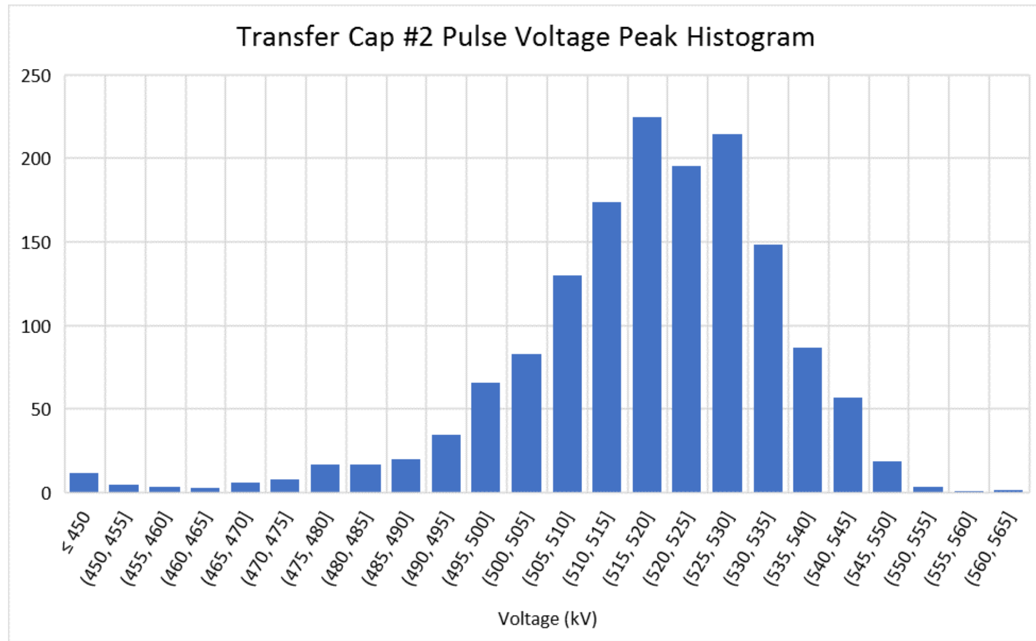

Figure 7.18: Histogram of the voltage peaks recorded throughout the entire full reversal testing of Transfer Capacitor #2. Analysis of the histogram shows ~90% of the 18,828 applied pulses were at or above the contract specification, confirming that the second transfer capacitor exceeded the specifications outlined in the program contract.

7.3.2.2 Transfer Capacitor #1 Testing

After Transfer Capacitor #2 performed so well, it was elected, when beginning testing of Transfer Capacitor #1, to not perform any ramp up of the voltage or reversal level. Transfer Capacitor #1 was tested only at 500 kV with 55% reversal – no preliminary lower voltage tests. Testing was ceased when Transfer Capacitor #1 held off the 18,032nd shot without any noticeable degradation. Figure 7.19 shows a typical waveform from the full reversal testing of the first transfer capacitor. The waveform shown is identical to that of Transfer Capacitor #2, confirming that the two devices are consistent with one another.

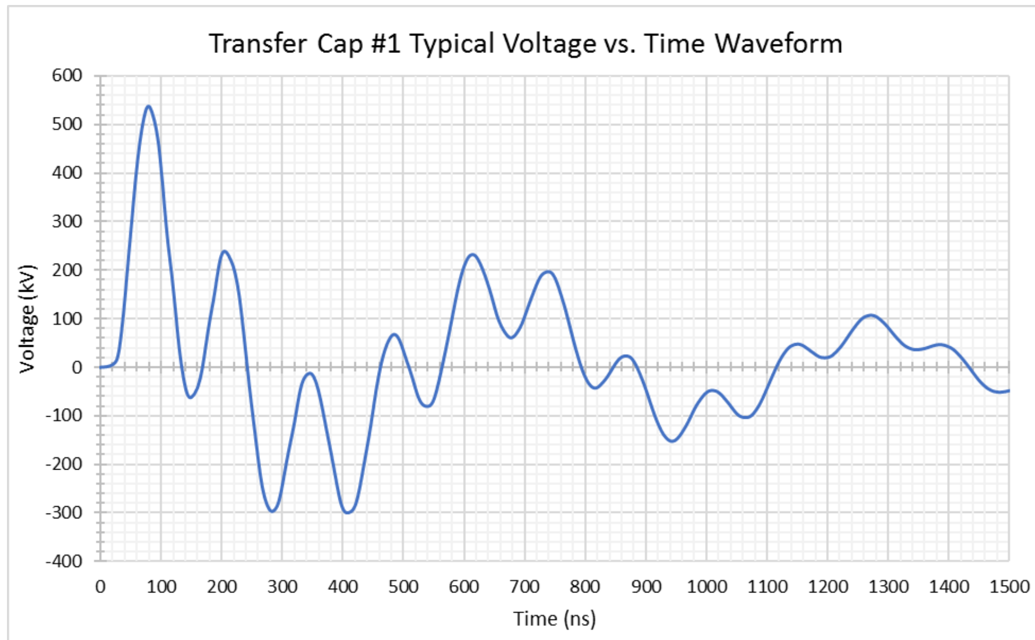

Figure 7.19: A typical waveform of the voltage pulses put on Transfer Capacitor #1. The device under test withstood over 18,000 pulses of the waveform shown here – 500 kV peak with 55% reversal.

Like the first capacitor tested, the ringing frequency of the discharge was monitored as an indication of capacitor health. Like Transfer Capacitor #2, Transfer Capacitor #1 proved to stay remarkably consistent throughout all 18,032 pulses, shown in Figure 7.20. The consistency in the ringing frequency suggests that after well over 10^4 pulses, there are no signs of degradation in the tested capacitor. Also, like the first test, this second test needed to confirm the self-breakdown Marx generator provided a minimum of 10,000 shots of sufficient magnitude (greater than 500 kV peak) to the test device. Again, analysis of the Transfer Capacitor #1 voltage peak histogram (Figure 7.21) can show that 29% of the total pulses were below the 500 kV threshold, meaning 71% of the pulses were above the contract specification threshold. Thus, Transfer Capacitor #1 withstood 12,805 shots of over 500 kV with 55% reversal, proving that it met full performance specification as specified by the program contract. No further testing of this device was performed.

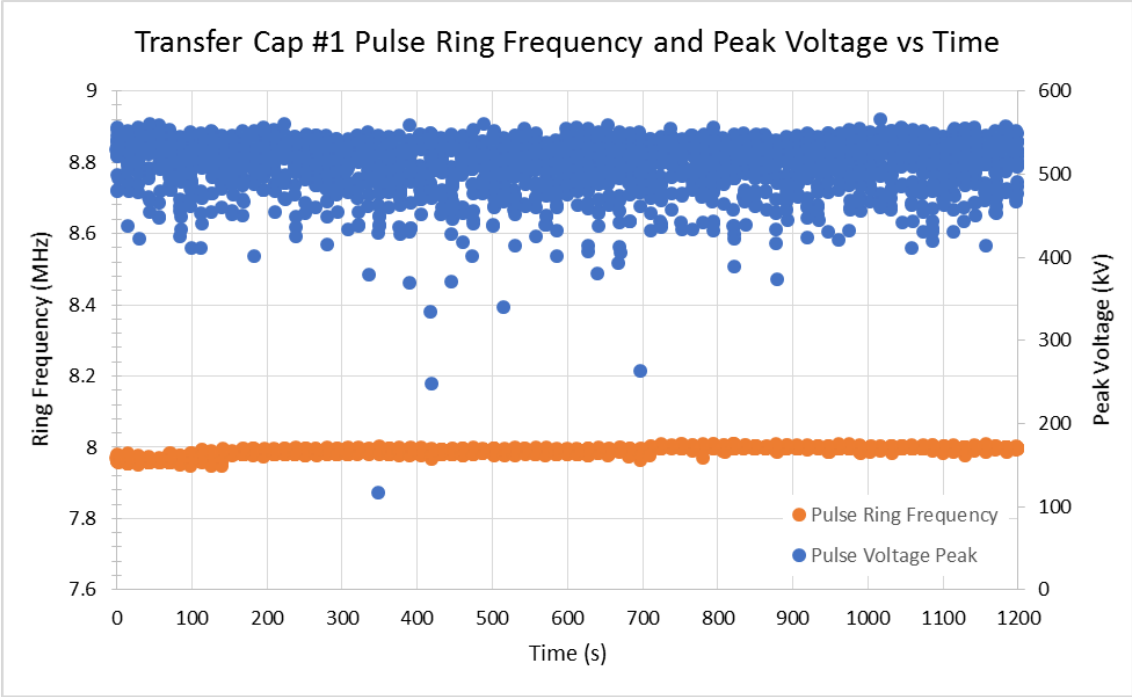

Figure 7.20: The ringing frequency and voltage peak of each pulse plotted against time. The consistency of the ringing frequency suggests the test capacitor performed remarkably consistently from pulse to pulse.

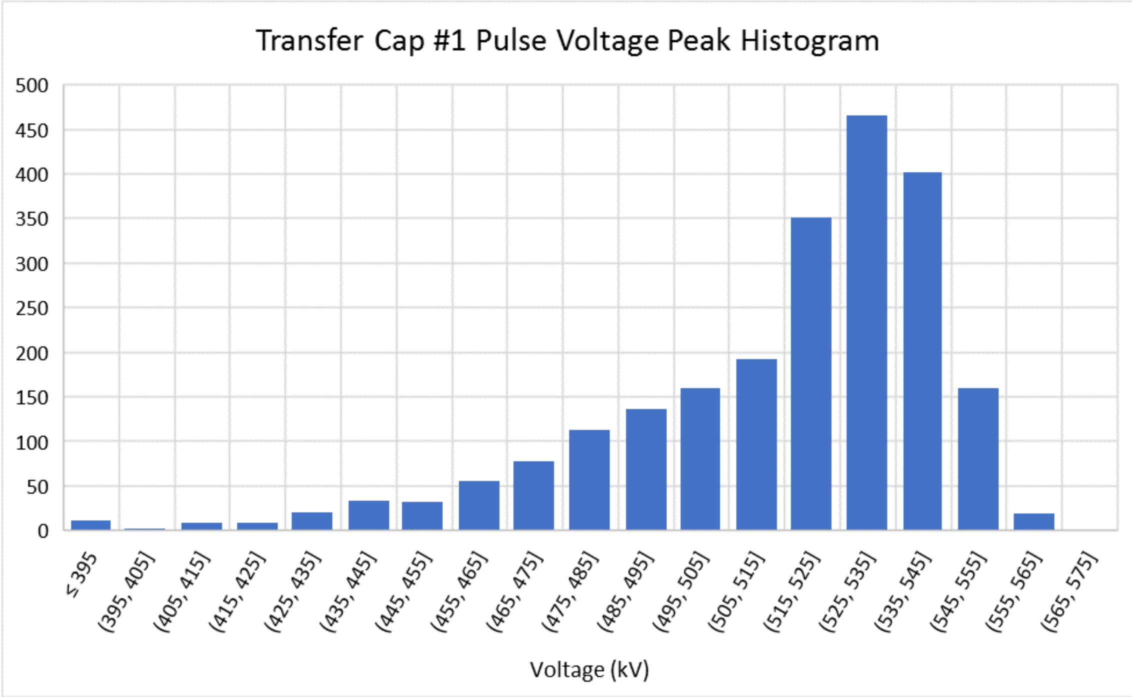

Figure 7.21: Histogram of the voltage peaks recorded throughout the entire full reversal testing of Transfer Capacitor #1. Analysis of the histogram shows ~71% of the 18,032 applied pulses were at or above the required peak voltage of 500 kV, confirming that the first delivered transfer capacitor exceeded the specifications outlined in the program contract.

7.3.2.3 Sub-Module Capacitor Overvoltage Testing

Upon successful testing of the full-scale transfer capacitors, two of the spare sub-elements were tested at higher voltage in an effort to see when and how these devices would breakdown. Having a much smaller capacitance on the output of the Marx bank allowed for voltage doubling to occur. The voltage doubling allowed for the ~600 kV test stand to be run at about 1.2 MV.

The tests showed that the single sub-module capacitors, nine of which make up a full transfer cap, were capable of withstanding ~1,000 shots of peak voltages ranging from 1-1.2 MV with ~10-15% reversal. A typical voltage waveform of the high voltage pulse used to test the sub capacitors is shown in Figure 7.22.

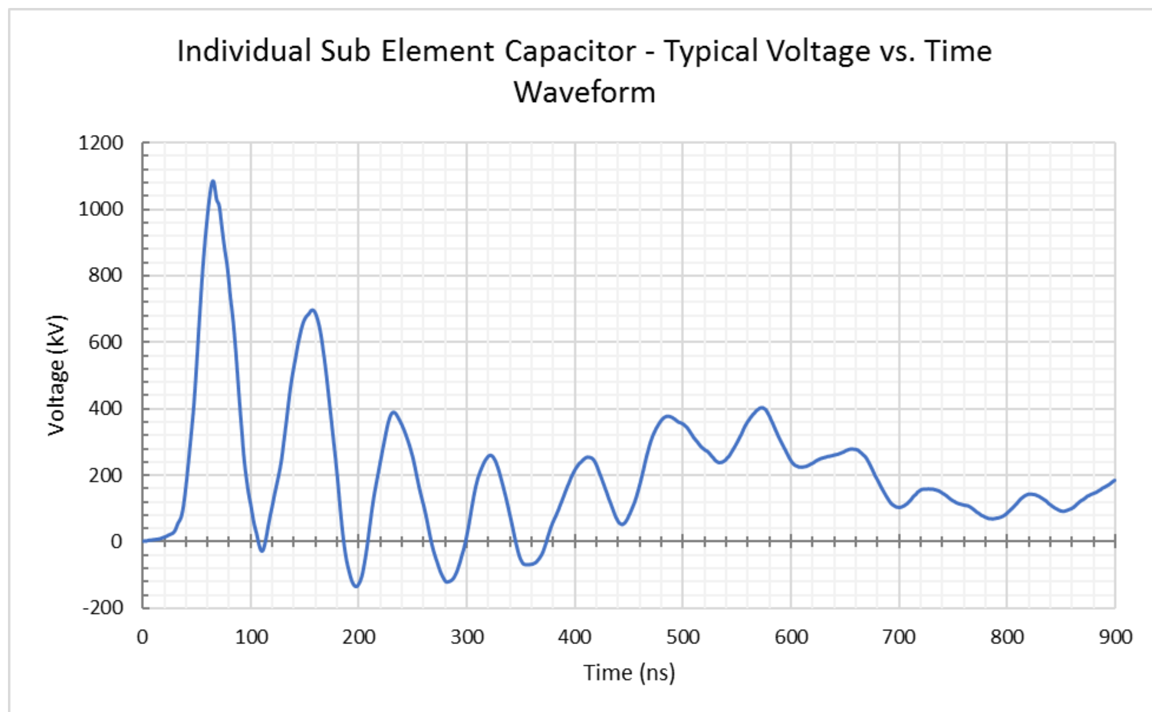

Figure 7.22: A typical waveform from the sub-module overvoltage testing. The smaller capacitance of the sub-module capacitor allowed for voltage doubling to occur, making testing at greater than 1 MV possible.

Running the test system at that high voltage level reduced the reliability and reproducibility of pulses. On a few pulses an arc would occur somewhere in the circuitry,

exposing the sub-element capacitors to 100% reversal, although these shots were minimal, no failure was noticed because of the increased reversal. Of the few times that happened, a waveform was captured showing the 100% reversal pulse, Figure 7.23.

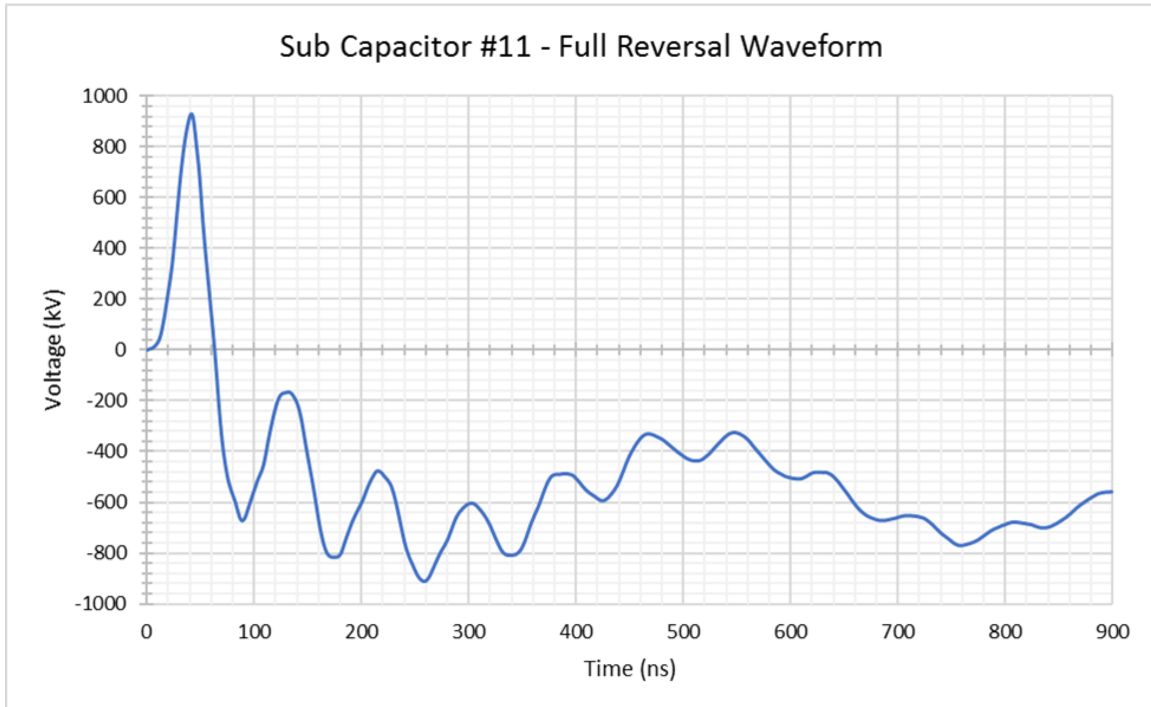

Figure 7.23: Initially, the test stand was not setup to reliably handle such a large increase in test voltage. The high testing voltages would sometimes cause arcing in and around the test circuit. Some of those arcs would short the test capacitor directly to ground, exposing the device under test to 100% voltage reversal. No adverse effects on the sub-module capacitor was seen as a result.

As was mentioned before, the health of the test capacitor can be monitored by the ringing frequency. During the tests of the sub capacitors, a substantial change in the ringing frequency was noticed at approximately 1,000 shots, or 160 seconds of testing time, on each sub-module that was tested. A scatter plot of each sub-module tested (#11 and #16) is shown in Figure 7.24 and Figure 7.25.

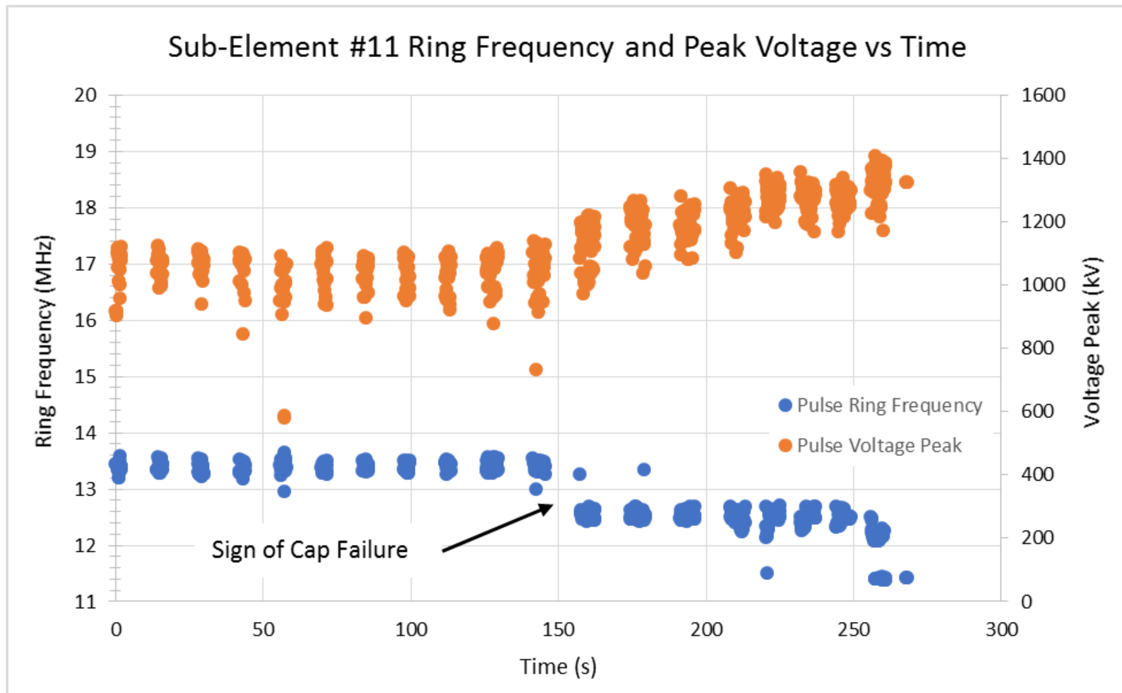

Figure 7.24: A plot of the ringing frequency and voltage peak of each recorded pulse plotted against time. First degradation, causing device failure, to the capacitor occurred near the 160 second mark of the testing cycle. The sharp change in ringing frequency, and sharp increase in voltage is characteristic of a capacitor failure.

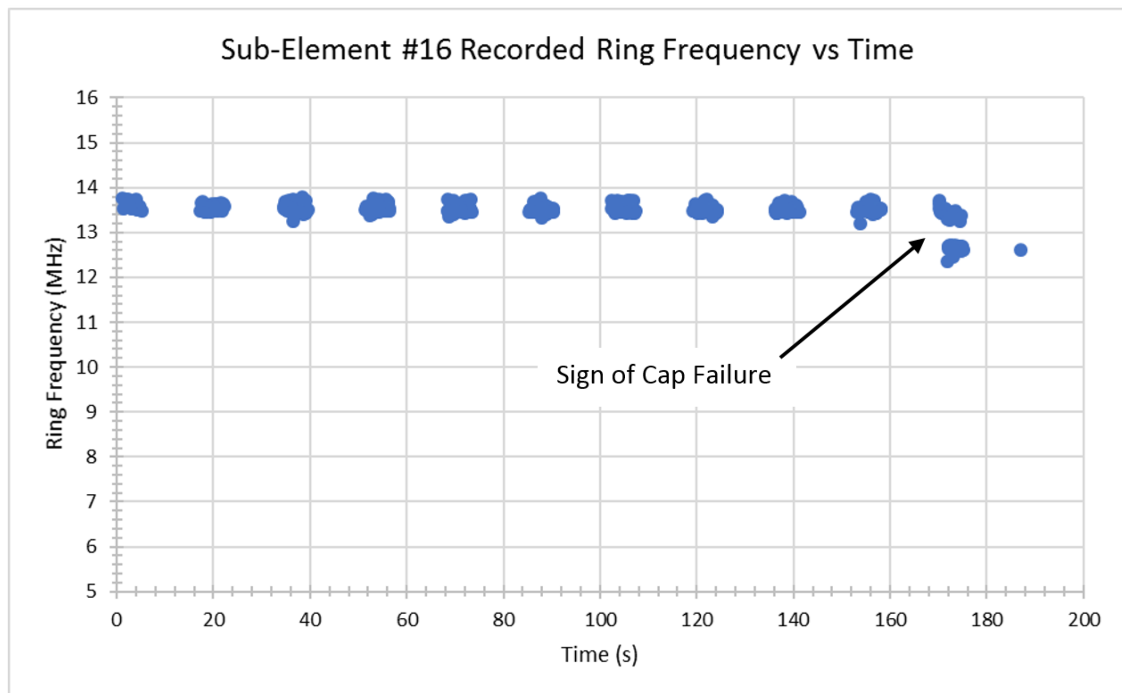

Figure 7.25: Similar to sub-module #11, the first ringing frequency changing degradation to the device occurred just after the 160 second mark of the testing cycle, showing the two devices have very similar lifetimes.

The failures of the two sub-modules were destructive and unrecoverable but were not catastrophic device failures. The sub-modules are made up of four MU100B substrates soldered together in series. In the case of these sub-module failures, only one of the four constituent MU100B disks broke down. This was first hypothesized when a post failure capacitance measurement still returned a stable capacitance value, nearly 25% higher than what was measured before testing began. Upon dissection of the failed devices, the hypothesis was confirmed. One of the failed devices is shown as it was immediately after testing in Figure 7.26. A buildup of carbon, indicative of an electrical breakdown is evident.

Figure 7.26: Sub-module #11 after failure. The carbon buildup is due to the breakdown tracking out of the MU100B material into the encapsulant.

After dissection of the failed devices, it became clear that only one of the four MU100B substrates broke down. This explains why the measured capacitance, after failure, was not typical of a failure, which usually results in the shorting out of the capacitor. A breakdown channel was found in one of the substrates after dissection and is shown in Figure 7.27. This explains why the sub-module continued to operate at 500 kV, albeit with a different ringing frequency.

Figure 7.27: After dissection, the breakdown channel through one MU100B substrate is partially visible. The breakdown began within the MU100B material, propagated out, into the encapsulant, then back into the MU100B material.

Further investigation into the failed sub-modules indicated some manufacturing short comings. SEM microscopy was employed to determine how off center the stacked disks were after the stacking process. SEM images were taken on spots called out in Figure 7.28. It is visible, without magnification that interface pairs 2-5 and 1-6 are off. As seen in Figure 7.29, the 2-5 interface is off center by 128.8 µm. The center junction, 1-6 is about 37 µm off center, Figure 7.30. Junction 10-7 is shown in Figure 7.31 and appears to be stacked concentrically. This analysis shows that further care is required in the area of disk placement when stacking. Conversely, the SEM's show that the solder is being applied evenly and being maintained in the disk junctions, Figure 7.31. However inconsistent the stacking was, the exceptionally high breakdown strength of the encapsulant epoxy kept those short comings from directly causing the failure in the sub-module, as the breakdown

initiates within the bulk of the MU100B, just inside of interface #1, before propagating to the edge of the material. The initiation of the breakdown being within the MU100B material suggests the performance limit of that particular substrate was reached in testing.

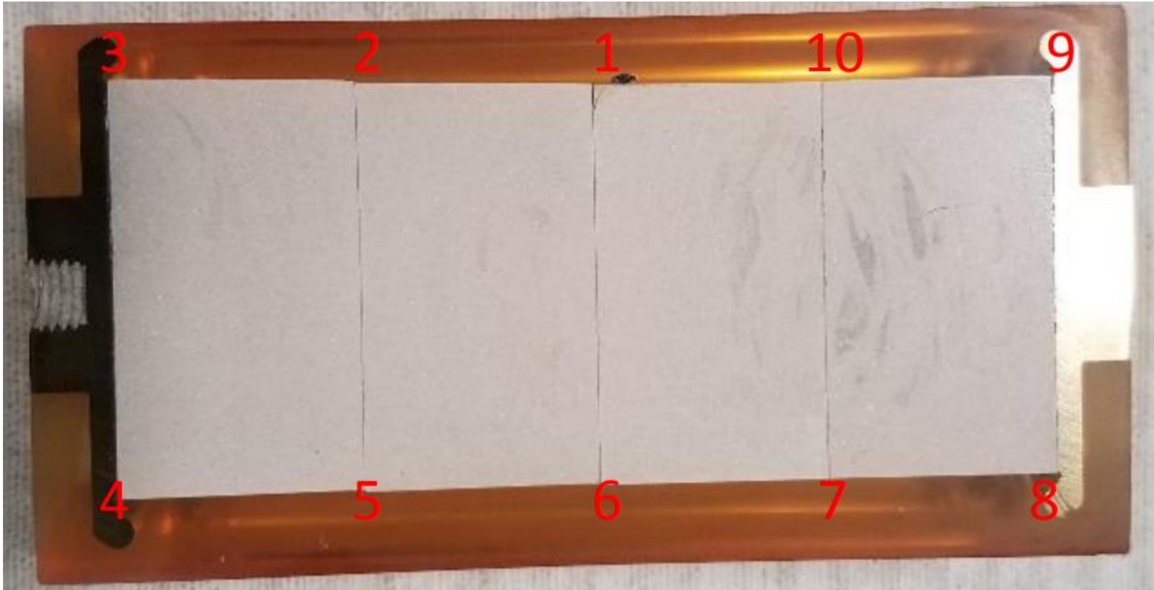

Figure 7.28: Failed sub-module cross section shown prepared for SEM imaging. Junction callouts are shown to measure the magnitude of off center substrate stacking.

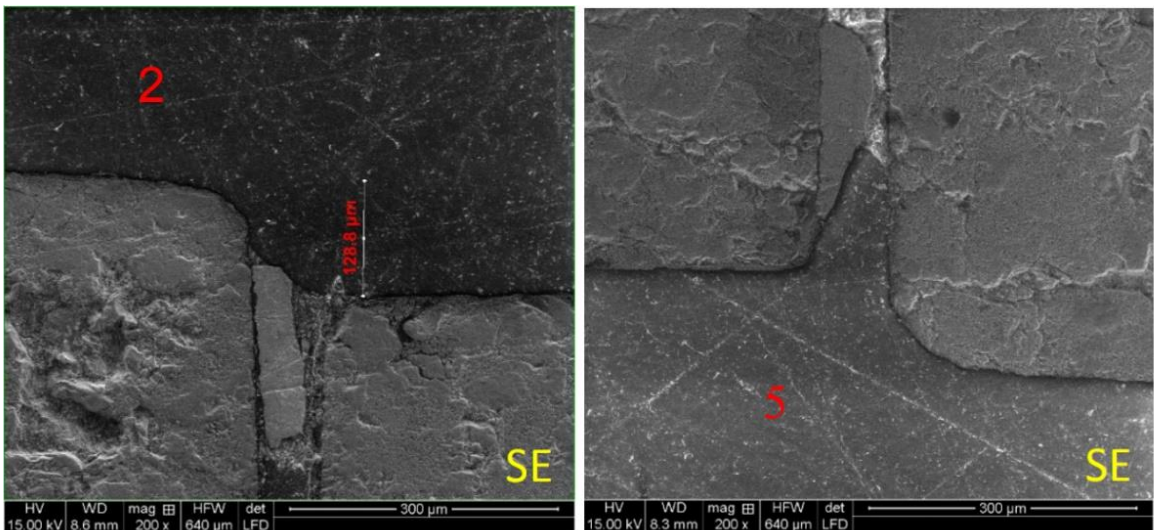

Figure 7.29: When stacking disks near the top of the stacking jig it is possible to force misalignment. In this case, 128.8 µm off center.

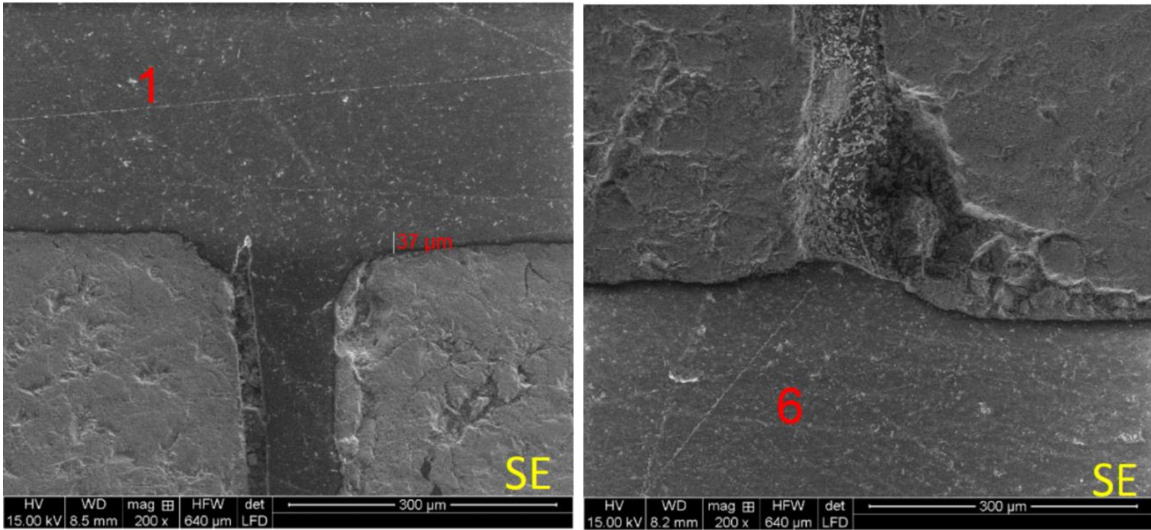

Figure 7.30: Stacking disk near the middle of the stacking jig are less susceptible for miss alignment, but the issue is not averted. Junction 1-6 is 37 μm off center.

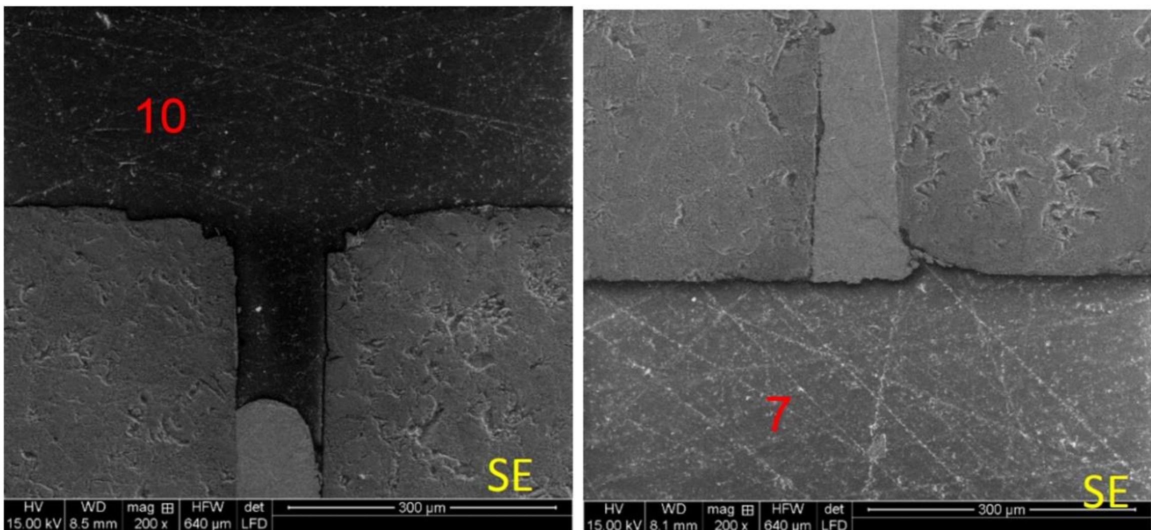

Figure 7.31: Junction 10-7 is aligned sufficiently as it is at the low point in the stacking jig. Solder fill is also of good quality here.

7.3.3 Smaller Sub-Module Design and Testing

From the information attained from the overvolting of the previously tested sub-module capacitors, new, smaller, sub-modules were fabricated with the intention of being shipped to NSWCDD for testing similar to the taller ones which were tested there. Since the sub-modules were found to have voltage handling capabilities much greater than required, the thickness of these smaller sub-modules will be reduced. Smaller sub-modules

fabricated for further testing are two each of a 6 cm thick sub-module capacitor (three 2 cm thick by 3.4 cm diameter MU100B substrates stacked together) and a 5.4 cm thick sub-module (three 1.8 cm thick by 3.4 cm diameter MU100B substrates stacked together). Fabrication of these devices underwent the same procedure as the original sub-modules.

During the tests at 500 kV, the transfer capacitor prototypes were exposed to an average field level of 62.5 kV/cm with peak fields approaching 90 kV/cm according to our models. Additionally, when testing the sub-modules at 1.1 MV, the average electric field across the previously tested samples was 137.5 kV/cm with peak field levels approaching 200 kV/cm in the MU100B. At those elevated electric field levels, the devices had lifetimes of less than 10^4 (for the transfer capacitor prototypes run at 500 kV – 60% reversal), approximately 10^3 pulses for the sub-modules tested at 1.1 MV. These numbers suggest the devices can be made smaller. Using those numbers, two designs were proposed for smaller sub-modules to be tested at 500 kV for a lifetime still greater than, but closer to 10^4 pulse lifetimes.

7.3.3.1 6.0 cm and 5.4 cm Sub-Module Modeling

Electrostatic models of the two designs are shown below. The 6 cm thick sub-module, when pulse charged to 500 kV has an average field in the MU100B of 83.3 kV/cm with peak fields of 108 kV/cm, Figure 7.32. The capacitance of these thinner devices is larger than the previously tested designs. Thus, fabrication of a new transfer capacitor would require seven of the 6 cm thick sub-modules in parallel compared to nine used in the 8 cm thick transfer capacitor described previously. Coupling the sub-module reduction with the total thickness reduction, the total volume of a transfer capacitor prototype was reduced by 38.6% compared to original design.

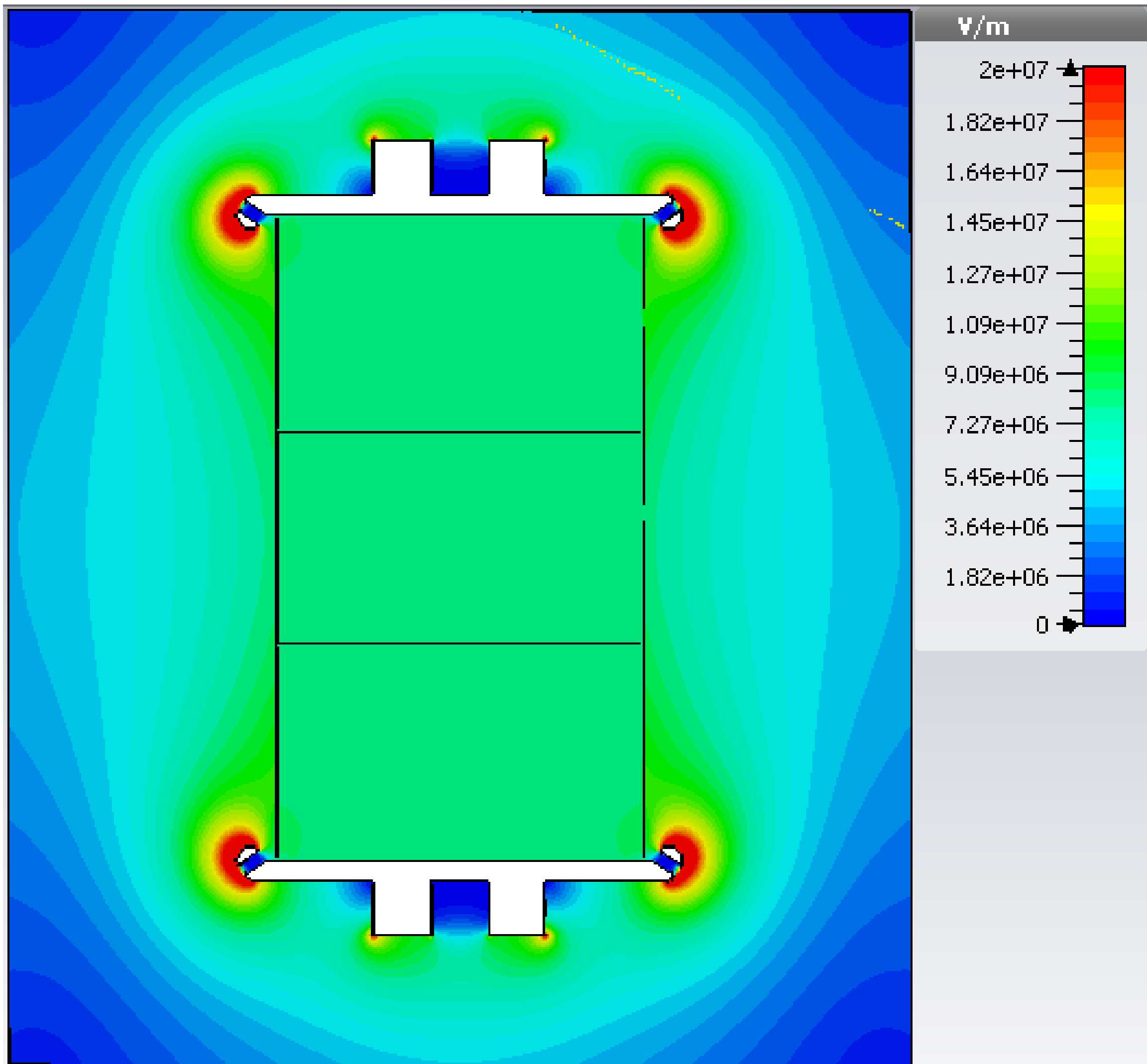

Figure 7.32: Electrostatic model of the 6 cm thick capacitor sub-module redesign. The device will be made up of three 2 cm thick by 3.4 cm diameter MU100B substrates. The average field in the MU100B of this embodiment will be raised to 83.3 kV/cm with a field enhancement factor equal to 1.296X.

The smaller 5.4 cm thick sub-module design will have an average field of 92.6 kV/cm in the MU100B with a peak field of 115.5 kV/cm, Figure 7.33. The capacitance of a single sub-module will be about 25 pF. With this design, six sub-modules in parallel are required to achieve a 130 pF Transfer Capacitor, resulting in a volume reduction of 51.6%.

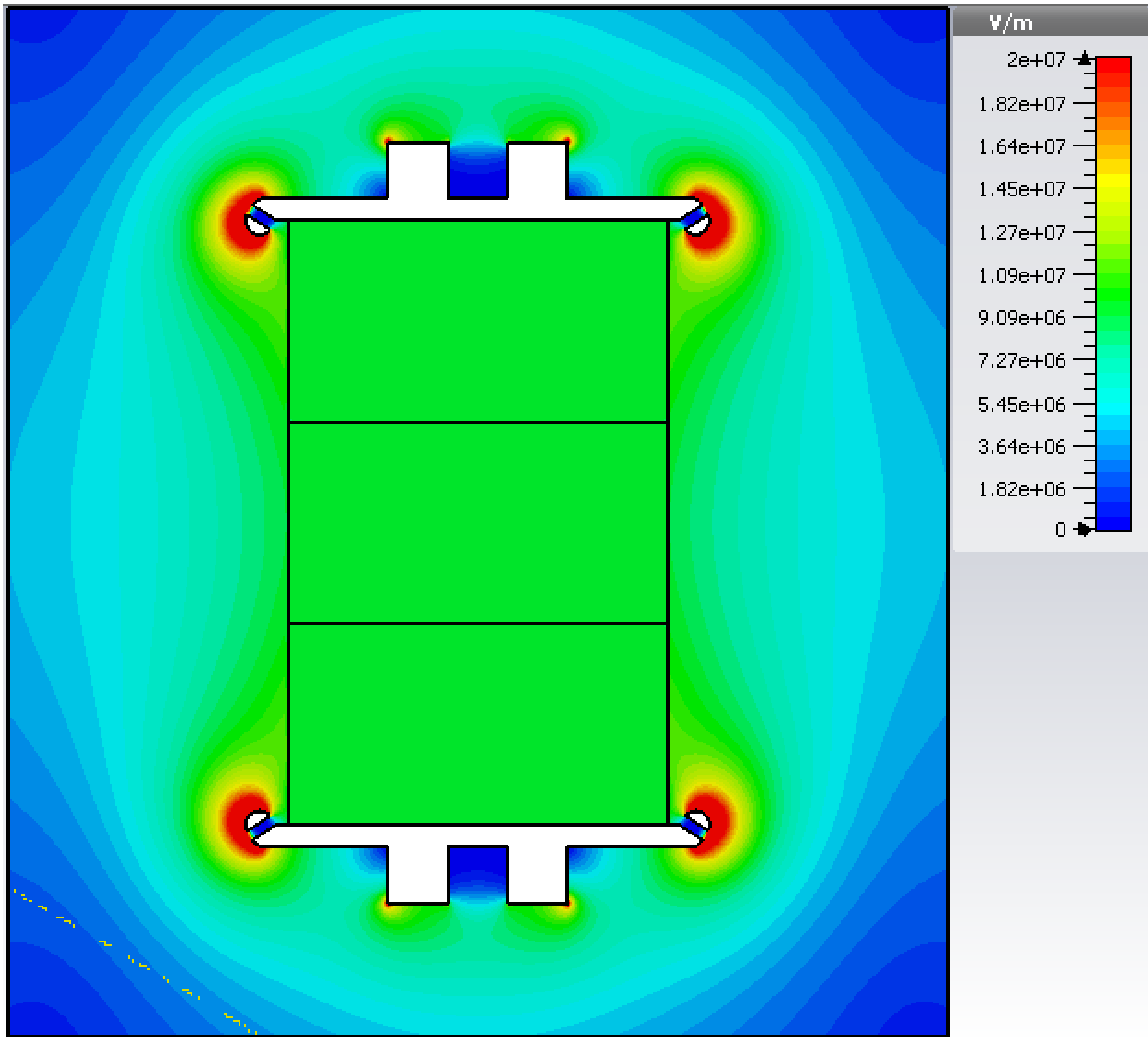

Figure 7.33: Model of the 5.4 cm thick capacitor sub-module redesign. The device will be made up of three 1.8 cm thick by 3.4 cm diameter MU100B substrates. The average field in the MU100B of this embodiment will be raised to 92.6 kV/cm with a field enhancement factor equal to 1.242X.

Fabrication of the smaller sub-modules resulted in operational capacitors considerably smaller than the 8 cm embodiments developed and tested, Figure 7.34.

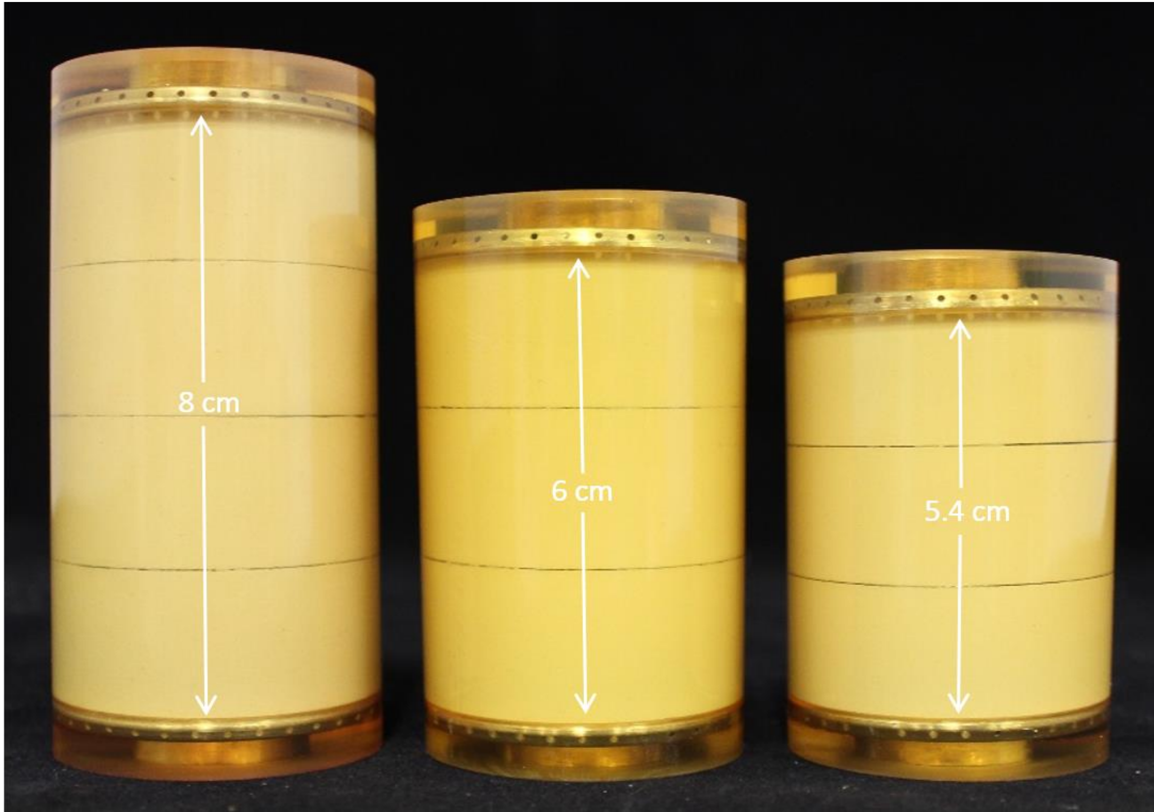

Figure 7.34: The smaller sub-capacitors shown with an 8 cm element previously tested at NSWCDD. One of the 5.4 cm devices is on the right with one of the 6 cm embodiments in the center.

The overvoltage testing of individual 8 cm thick sub-modules demonstrated a lifetime of 10^3 pulses at 1.1 MV. The 1.1 MV charge voltage gives an average field in the MU100B of 135 kV/cm. Thus, device lifetime is heavily dependent on applied electric field level. It was theorized, before testing at 500 kV, that the 6 cm thick sub-modules will experience an average electric field in the MU100B of 83 kV/cm. The increase in field level should reduce the expected lifetime of the devices to around 10^5 pulses. Similarly, when the 5.4 cm thick devices are evaluated at the required 500 kV voltage, the average field in the MU100B will be 92 kV/cm, which should reduce the device lifetime to between 10^4 and 10^5 pulses. Table 7.4 summarizes the smaller stacked devices.

Table 7.3: The individual stack information for each of the four tested smaller sub-modules.

Stack Number	Disk Name	Disk Thickness (mm)	Permittivity	Stack Capacitance (pF)
6.0-A	042318-1	20.93	194.83	22.21
	042318-3	20.87	196.87	
	042418-4	21.18	196.16	
6.0-B	042418-3	21.11	191.52	21.57
	042318-5	20.92	192.68	
	042418-6	20.97	189.36	
5.4-A	081718-4	18.47	171.98	23.35
	081718-3	18.37	172.37	
	081718-5	18.33	169.83	
5.4-B	032618-2	18.27	191.46	26.15
	032618-1	18.24	192.73	
	032618-3	18.27	192.18	

7.3.3.2 6.0 and 5.4 cm Sub-Module Testing

The four delivered smaller sub-module capacitors were tested under the same PEVS type conditions as their thicker counter parts. Each of the four delivered devices testing sequences will be discussed individually below.

7.3.3.2.1 5.4 cm Sub-Module Testing

Sub-module 5.4-A was tested first. This device was used in a sacrificial mode, as there was no similar dummy load to use to characterize the test stand. It withstood 10,000 pulses with peak voltages ranging from 100 kV – 500 kV with a majority of pulses in the 100 – 200 kV range.

After characterizing the test stand with sub-module 5.4-A, sub-module 5.4-B was evaluated. After an initial sequence of testing slightly below the contract specified levels in which sub-module 5.4-B withstood ~9,000 pulses of 430 kV with a 60% voltage reversal (79.6 kV/cm average field), device 5.4-B was tested to fully meet the contract performance specifications. Per the contract with JNLWD, the devices are required to withstand 10,000 or more pulses of 500 kV peak with greater than 50% voltage reversal. Sub-module 5.4-B in this sequence of testing withstood 10,000 shots with a peak voltage of 498 kV with a voltage reversal of ~60% on average. A characteristic waveform is shown in Figure 7.35.

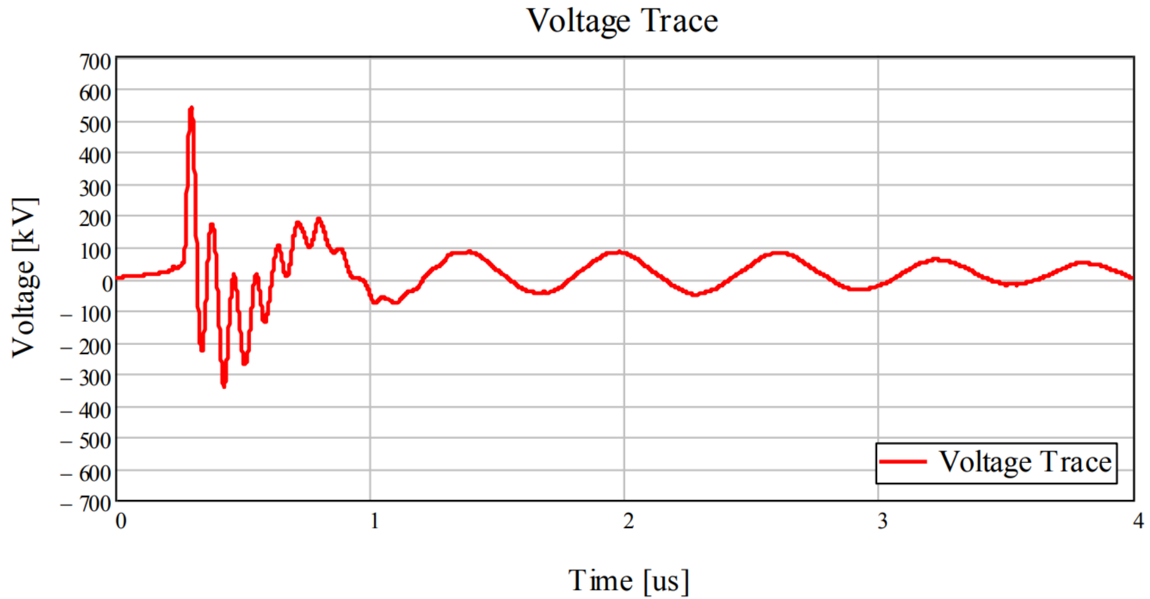

Figure 7.35: A typical waveform from sequence 2 of sub-module 5.4-B testing. The device withstood 10,000 pulses of this type with no signs of degradation, meeting contract specifications.

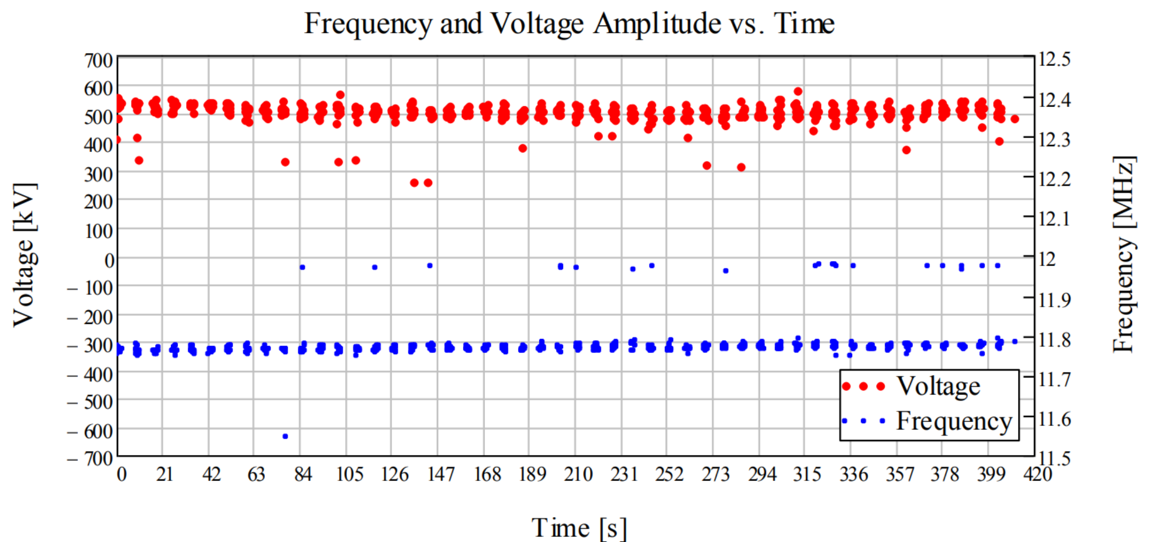

Figure 7.36: Single pulse plotting of peak voltage and ring frequency show that the capacitor under test performed very reliably over the 10,000 pulses, as shown by the consistency in ring frequency.

After meeting the contract specified performance specifications, the peak voltage applied to the device was gradually increased. During the third testing sequence, sub-module 5.4-B withstood 2,200 shots with an average peak voltage of 595 kV (110 kV/cm average field), during the fourth testing sequence the device withstood 1,200 pulses with

an average peak voltage of 646 kV (119.6 kV/cm average electric field) before the Marx bank failed to supply that voltage level. Through testing sequences five, six and seven, the device successfully withstood 2,000 pulses with an average peak level of 620 kV (114.8 kV/cm average electric field) and the characteristic 60% reversal, 2,000 720 kV (133.3 kV/cm average electric field) pulses with no signs of failure and withstood 2,000 shots of 813 kV (150.6 kV/cm average electric field) on average with no signs of degradation, respectively. A characteristic waveform from the sequence seven testing is shown Figure 7.37.

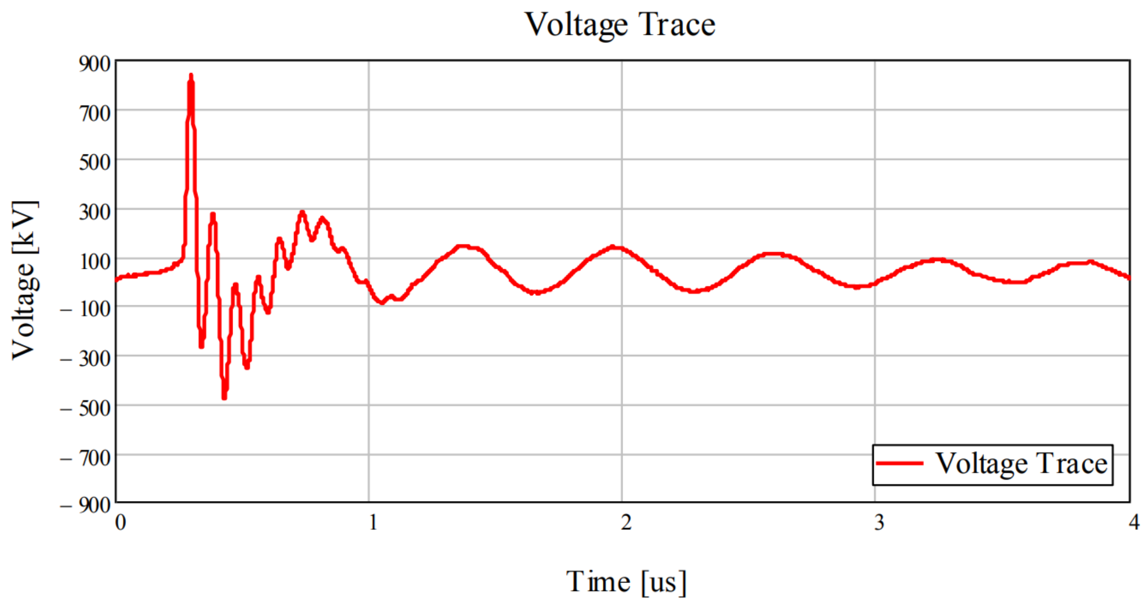

Figure 7.37: A characteristic waveform from the seventh sequence of testing sub-module 5.4-B. In sequence seven cap 5.4-B withstood 2,000 shots of 813 kV with no signs of degradation.

The eighth sequence of testing saw sub-module capacitor 5.4-B fail. The failure occurred after the 10th shot at 1 MV (185.2 kV/cm average electric field). The following figure shows the voltage trace preceding failure along with the voltage and frequency amplitudes. It is evident from the frequency amplitudes that a substantial change in the test capacitor occurred early in the test sequence.

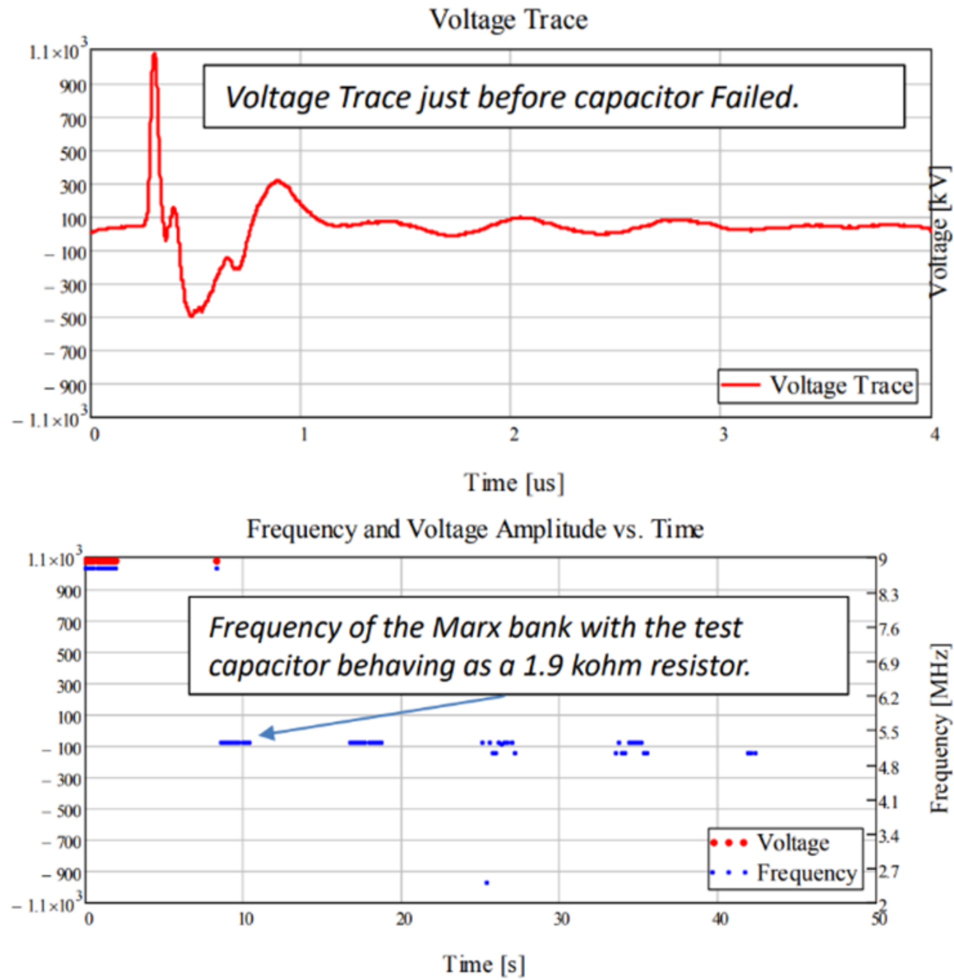

Figure 7.38: Sequence eight, waveform from just before capacitor failure (top) is shown along with the frequency and voltage amplitudes of the run (bottom). A drastic change in ringing frequency, typical of test capacitor failure is visible and is called out in the image.

A summary of the test sequences for sub-module 5.4-B is shown in the following table. Of note is the fact that the device successfully met and exceeded contract specifications for performance and eventually failed on the tenth shot of 1 MV.

After failure of the shorter device, an analysis was performed to determine the mode of breakdown. The device shorted entirely (all three substrates broke down), which is the only time that has been observed in a stacked device, Figure 7.39. The breakdowns in this device were all within the MU100B, although they are near the edge of the nanodielectric, which suggests the possibility of some manufacturing inconsistency causing the failure.

Table 7.4: A summary of the shots applied to sub-module 5.4-B. Sequence two confirmed specified performance, sequences three-seven exceeded specified performance in voltage magnitude and sequence eight saw failure of the device at 1 MV.

Cap 4: 5.4_B Value: 27.7 pF

Seqnce	1	2	3	4	5	6	7	8
Voltage [kV]	429 ± 61	497 ± 33	595 ± 21	646 ± 21	620 ± 52	723 ± 30	813 ± 31	~1,000
PRR	100				50			
Pulse Nmbr	9,200	10,000	2,200	1,200	2,000	2,000	2,000	~10
Burst	2s/6s							

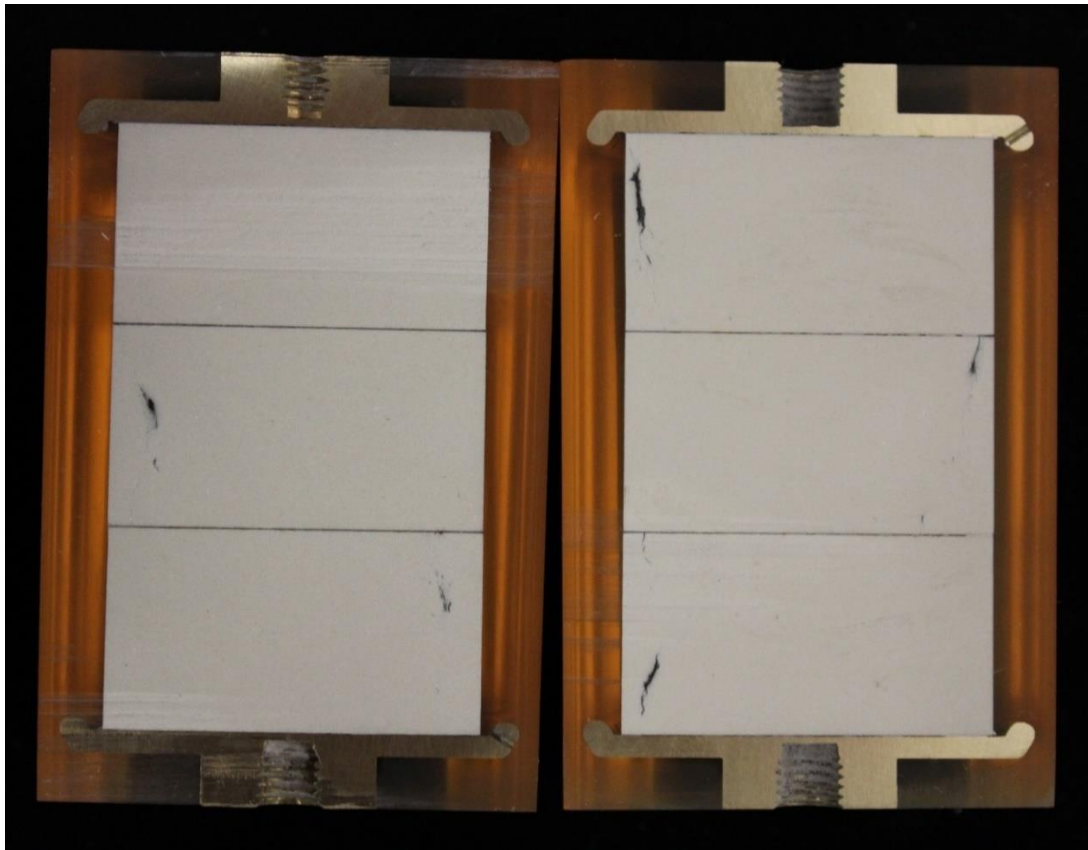

Figure 7.39: Breakdown channel cross section. The device was cut in half to obtain an image of the breakdown tracks. Breakdowns are within the MU100B.

7.3.3.2.2 6.0 cm Sub-Module Testing

Sub-module 6.0-A and B were assembled from three 2 cm thick MU100B substrates joined in series giving a total device thickness of approximately 6 cm. Tests with device 6.0-A began at the contract specified level of 500 kV (83.33 kV/cm average electric field) with 50-60% reversal. In the first sequence of testing 6.0-A, successfully withstood 4,400 shots before the Marx bank began misfiring due to a fault. The Marx was repaired and tests continued at the same levels with sequence two. In sequence two, the device successfully held off another 4,400 pulses before device failure. Thus, between both sequence 1 and 2 sub-module 6.0-A withstood 8,800, 500 kV pulses before one of the MU100B substrates failed. A characteristic waveform is shown, Figure 7.40, along with the graph of frequency and voltage amplitudes for sequence two (showing device failure), Figure 7.41. Figure 7.40 depicts a typical waveform having a peak of 500 kV and a reversal level of -300 kV. Device 6.0-A exhibited a partial failure in the one of the three substrates which comprised the sub-module. This type of failure resulted from having two of the three substrates acting as capacitors in seriese which caused the capacitance to increase in the device. The breakdown appears to be initiated at the triple point interface underneath the corona ring electrode suggesting solder over flow was not sufficiently removed before encapsulation as the cause of failure, Figure 7.42.

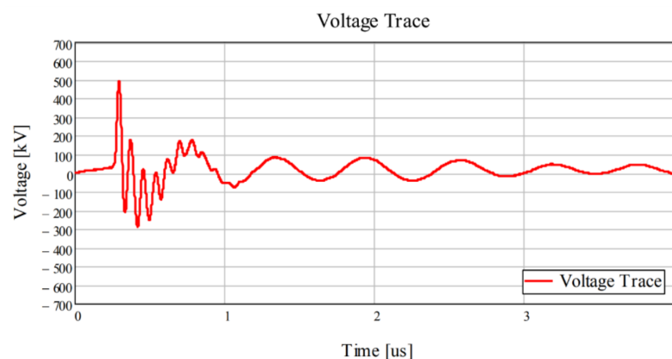

Figure 7.40: A characteristic waveform of the 8,800 pulses sub-module 6.0-A survived.

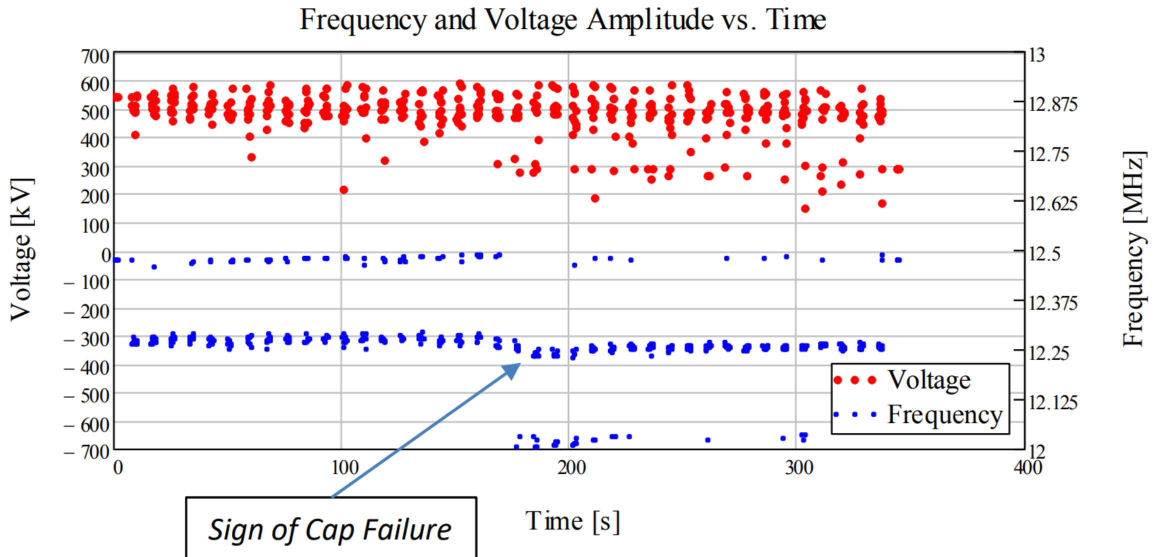

Figure 7.41: Frequency and voltage amplitudes of sub-module 6.0-A, test sequence 2. Failure is evident by the abrupt change in ringing frequency, which is shown above. Altogether sub-module 6.0-A withstood 8,800 500 kV pulses.

Figure 7.42: Autopsy of sub-module 6.0-A after failure occurred in the 6.0 cm tall, 22.2 pF device after 8,800 500 kV (83.33 kV/cm average electric field) pulses. The left image shows the breakdown initiated at the triple point, suggesting a small amount of solder overrun may not have gotten entirely removed as a possible cause of early failure.

Sub-module 6.0-B failed after 200 shots under the contract specified conditions. A characteristic waveform of the shots 6.0-B survived can be seen in Figure 7.43. The failure is evident from a large change in the ringing frequency and voltage amplitude plot, Figure

7.44. Dissection of the failure shows there may have been a problem with surface adhesion between the encapsulant and the nanodielectric as the breakdown traverses that interface for a measurable distance before entering the bulk MU100B, Figure 7.45.

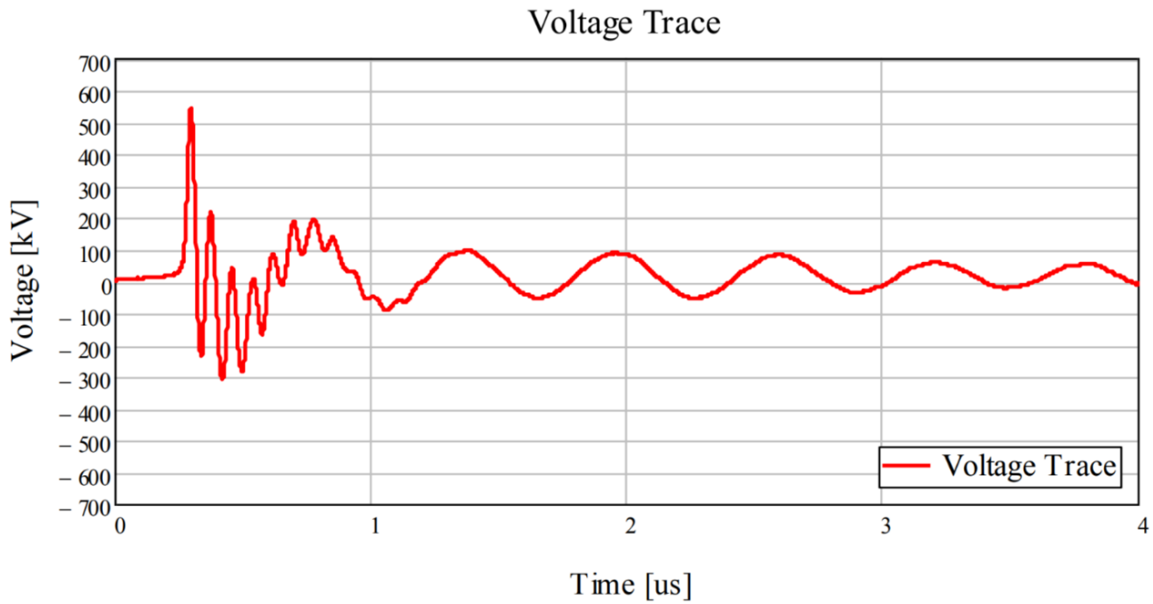

Figure 7.43: Characteristic waveform of the 200 pulses sub-module 6.0-B survived.

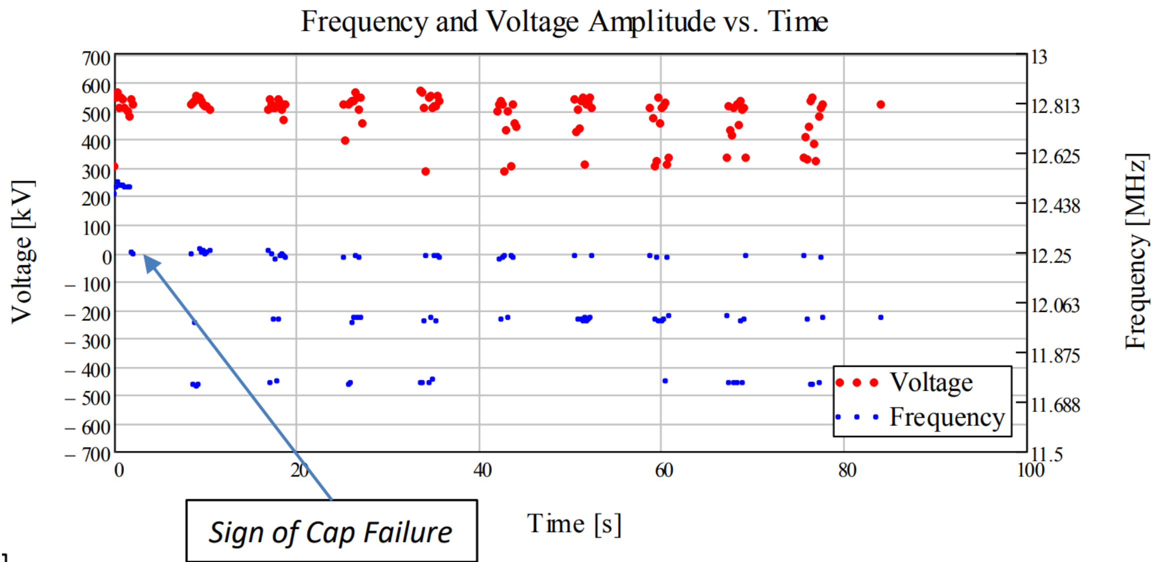

Figure 7.44: Frequency and voltage amplitudes of sub-module 6.0-B. Initial failure is shown on the figure by the stark change in the ringing frequency.

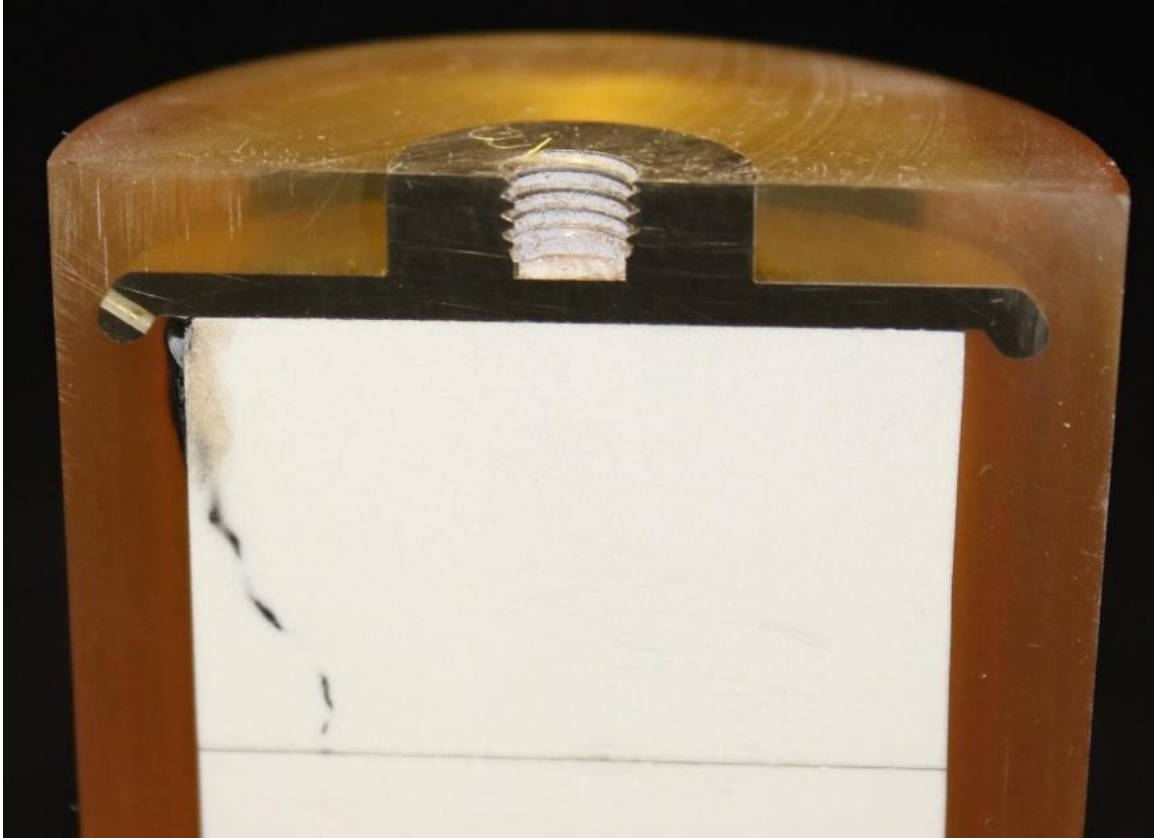

Figure 7.45: Breakdown of sub-module 6.0-B is shown to begin slightly within the MU100B, near the triple point, then traverses into and down the encapsulant-dielectric interface for a measurable distance before finishing well within the bulk of the nanodielectric.

Table 7.5: A tabular summary of the small sub-module testing.

Device	Dielectric Height (cm)	Measured Capacitance (pF)	#500 kV pulses withstood	Peak Voltage Withstood	Average Electric Field Withstood (kV/cm)	Met Performance Specification (Y/N)
5.4-A	5.4	23.4	200	500 kV	92.6	N
5.4-B	5.4	27.7	10,000	1 MV	185.2	Y
6.0-A	6.0	22.2	8800	500 kV	83.3	N
6.0-B	6.0	21.6	200	500 kV	83.3	N

Smaller sub-module testing showed that there are quality control issues in component fabrication that must be addressed to improve the consistency in device function. Most important in those is the interface between the nanodielectric and the field shaping electrode. All of the solder adhesive has to be removed from the edge of the MU100B after attaching the field shaping electrode, failure to do so can result in premature failure as seen with devices 5.4-A, 6.0-A, and 6.0-B. However, sub-module 5.4-B's test

performance indicates that with consistent assembly methods, a six sub-module Transfer Capacitor with a 50% volume decrease compared to the nine sub-module capacitor described earlier can be achieved.

References – Chapter 7

[1] R. D. Curry, S. A. Dickerson, A. Howard, B. Lamb and S. Mounter, "Scaled DC Lifetime, Test and Evaluation of Advanced Nanocomposite Materials for Compact High Voltage Capacitors," in *IEEE 21st International Conference on Pulsed Power (PPC)*, Brighton, UK, 2017.

[2] S. A. Dickerson, R. D. Curry, S. A. Mounter and L. J. Brown, "Compact Very High Voltage Capacitor Development Based on Advanced Machinable NanoDielectric Materials," in *IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, Jackson, WY, USA, 2018.

[3] S. A. Dickerson, R. D. Curry, S. A. Mounter and L. J. Brown, "Advanced NanoDielectric Material Development and Scaling for use in Compact Ultra-High Voltage Capacitor Prototypes," *IEEE Transactions on Dielectrics and Electrical Insulation,* 2019.

Chapter 8. Conclusions and Future Direction

The capacitor development effort described has successfully taken 20-40 kV small-scale test sample capacitors, scaled the technology, and designed, built, and tested ultra-high voltage capacitors rated in the 500 kV – 1 MV range. The MU100B material utilized in these devices is a game changer for the high voltage – pulsed power capacitor communities. In this report, reliable and reproducible manufacture of a scalable material was demonstrated. Using the MU100B material and advanced capacitor development processes, delivery of long-life time 500 kV capacitors was demonstrated. The delivered devices are 2.4 times smaller than the commercial devices currently being employed in the intended application. Moreover, the capacitor development effort described here showed possibility for even further size reductions when sufficient quality controls are placed on the ultra-high voltage capacitor assembly procedures. Tests of individual sub-module devices (full-voltage capacitors at a fraction of the capacitance of the full-scale prototypes) demonstrated that nanodielectric materials can be used to achieve compact 1 MV capacitors that are a substantial reduction in size and volume over commercial capacitors.

Although the scaling methods and capacitor development procedures outlined were focused on a point design, the same procedures can be used to manufacture high voltage capacitors over a much wider range of performance specifications. The flexibility is attainable from the way the 500 kV capacitor was designed. Various voltage ratings can be attained by varying the thickness of sub-module. Ranging from single kilovolt devices that are a fraction of a centimeter thick to the nearly megavolt prototypes presented here. The capacitance of future devices can also be varied by adjusting the number of modules in

parallel. Through these methods high voltage MU100 capacitors can be fabricated with specifications ranging from picofarads to nanofarads and 10's of kV up to the MV range.

The results described in this thesis lay a solid foundation for further work into reducing the size of high voltage pulsed power capacitors. The development of field shaping electrodes for novel geometries have been shown to increase the dielectric material performance by nearly 50%. The dielectric material performance increase was then leveraged into functional prototype devices which were tested with promising results. A general overview of devices fabricated and tested for this thesis are shown in Table 8.1.

Table 8.1: General summary of the testing results for the various MU100B capacitor types presented in this thesis.

Device Type	Dielectric Thickness	Capacitance Value	Voltage Rating	Lifetime Goal at Rated Voltage	Tested Lifetime at Rated Voltage
Small Scale Capacitors	0.2 cm	100-500 pF	40 kV	10^6 pulses	>800,000 pulses
2 cm UHV Substrate	2 cm	50-70 pF	250 kV	10^4 pulses	>10^3 pulses
5.4 cm Sub-Module	5.4 cm	25-30 pF	500 kV	10^4 pulses	10^4 pulses
8 cm Sub-Module	8 cm	15-20 pF	500 kV	10^5 - 10^6 pulses	>10^4 pulses
8 cm Sub-Module	8 cm	15-20 pF	1 MV	10^3 pulses	10^3 pulses
Transfer Capacitor	8 cm	130 pF	500 kV	10^5 - 10^6 pulses	>10^4 pulses

The work presented here was a result of scaling the nanodielectric material thickness, and enabled a substantial advance in capacitor technology when compared with what is available on the commercial market. The voltage handling improvements, compared to the commercial state of the art in ceramic capacitors, enabled by this MU100B development effort can be seen in Figure 8.1.

The next step in MU100B capacitor development is to scale the surface area of the nanodielectric, increasing the radius of dielectric substrates. Further, scaling the surface area of the material could enable other shapes for MU100B substrates, such as a square or rectangular substrate, to utilize the most surface area for a given footprint. Effectively

scaling up the surface area of MU100B capacitors would enable another substantial improvement in capacitor capability from the commercial state of the art. Increasing the surface area of MU100B capacitors would allow more capacitance to be packed into smaller packages, helping to enable the next generation of fieldable pulsed power/directed energy systems.

Figure 8.1: A 500 kV MU100B sub-module shown side by side with a 500 kV stack of commercially available ceramic capacitors and a standard ruler for size reference.

Improving the state of the art in such a manner can have profound effects on the pulsed power/directed energy industry. Capacitive energy storage is one of the leading contributors to directed energy size and weight. Reducing the size and weight of proposed systems will enable the next step in national security. Deploying high technology directed energy systems could enable non-lethal defense of our boarders and strategic assets. Thus, research and development efforts like the one presented here are crucial for the continued advancement of such systems.