IEEE Open Journal of Nanotechnology

Received 22 May 2020; revised 28 July 2020; accepted 26 August 2020. Date of publication 1 September 2020; date of current version 28 September 2020. The review of this article was arranged by Associate Editor Kazuhiko Endo.

Digital Object Identifier 10.1109/OJNANO.2020.3020567

Design of Ternary Logic and Arithmetic Circuits Using GNRFET

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This work was supported by the National Science Foundation under Grant NSF Award # 1629908.

ABSTRACT Multiple valued logic (MVL) can represent an exponentially higher number of data/information compared to the binary logic for the same number of logic bits. Compared to the conventional and other emerging device technologies, Graphene Nano Ribbon Field Effect Transistor (GNRFET) appears to be very promising for designing MVL logic gates and arithmetic circuits due to some exceptional electrical properties of the GNRFET, e.g., the ability to control the threshold voltage by changing the width of the GNR. Variation of the threshold voltage is one of the prescribed techniques to achieve multiple voltage levels to implement the MVL circuit. This paper introduces a design approach for ternary logic gates and circuits using MOS-type GNRFET. The designs of basic ternary logic gates like inverters, NAND, NOR, and ternary arithmetic circuits like the ternary decoder, 3:1 multiplexer, and ternary half-adder are demonstrated using GNRFET. A comparative analysis of the GNRFET based ternary logic gates and circuits and those based on the conventional CMOS and CNTFET technologies is performed using delay, total power, and power-delay-product (PDP) as the metrics. The simulation and analysis are performed using the H-SPICE tool with a GNRFET model available on the Nanohub website.

INDEX TERMS Decoder, graphene nano ribbon, half adder, multi-valued logic, multiplexer, ternary logic.

I. INTRODUCTION

Multiple Valued Logic (MVL) and its' applications have been studied extensively over the last couple of decades due to the ability of the MVL logic devices to provide an exponentially higher information density compared to the binary logic. In Binary or Boolean logic system (base 2), each logic bit can have two possible values: low (0) and high (1). Whereas, in the MVL system (base 3 or more), each digit can have three or more possible values leading to significantly higher information density with smaller logic gates and reduced circuit complexity. As a result, the energy consumption, area, and circuit overheads and other costs for each bit of information would decrease in the MVL system [1]. For example, in the ternary logic system, it takes only $\log_3 2^n$ bits to represent an n-bit binary number [2], which reduces the computational complexity to a large extent and thus enhances the power and area efficiency of the system.

Multiple valued logic can be ternary (radix 3), quaternary (radix 4), quinary (radix 5), etc. However, ternary and quaternary logic systems have drawn much attention from the research community. The ternary logic system appears to be the most feasible MVL system that can be adopted in the near future because of its simplicity and ease in distinguishing different logic levels as in the binary system. At smaller technology nodes, the supply voltage is limited to a value equal to or less than 1.2 V. Therefore, a higher number of discrete voltage levels needed to identify different logic values within this limited supply range (0 to 1.2 V) would be challenging and susceptible to noise and other signal integrity issues. As a consequence, most of the recent research work focuses on ternary logic and memory. The initial efforts to implement ternary logic are based on the prevailing CMOS and other technologies available since 1974 [3]– [5]. Due to short channel effects, scaling limitations, DIBL, energy consumption, and other signal integrity issues, conventional technologies are not appealing for the MVL system. New materials and new device technologies like carbon-based FETs, QDGFET, and Memristor [6]– [8] are being explored

to overcome these limitations and implement reliable MVL circuits.

Carbon-based Field Effect Transistors (FETs) are drawing widespread attention due to their outstanding electrical properties and integration capabilities. Carbon-Nano-Tube-Field-Effect-Transistor (CNTFET) and Graphene-Nano-Ribbon-Field-Effect-Transistor (GNRFET) are the two forms of carbon-based transistor that have become trendy research topics. Different pieces of literature are found which work in CNTFET and GNRFET based ternary logic design [1], [2], [5], [6], [9]– [11] which uses the threshold voltage control method for implementing different ternary logic circuits and arithmetic circuits. CNTFET experiences fabrication complexity like gate alignment challenge and incompatibility to planner technology. GNRFET, due to its planer structure, would be more suitable because it has the potential to use in the existing planner CMOS fabrication process [12]. As a consequence, GNRFET appears to be a promising technology for ternary logic and arithmetic circuits. In this paper, we present a design approach for GNRFET based ternary logic circuits.

One of the main issues with working with GNR is the effect of Line Edge Roughness (LER), which results from the unevenness in the edge of the ribbon during the fabrication process. LER affects the electrical properties of the ribbon as well as the transistor. The unevenness of the ribbon introduces unpredictability in the operating condition by changing the ribbon width. Studies show that the off currents of the transistor increases due to the gap states induced in the band-gap region that increases the leakage current at the OFF state. Simultaneously, the on-current of the device generally decreases due to the decreased quantum transport [13].

Different fabrication techniques have been tried for the fabrication of GNR like lithography, chemical synthetics, Extreme ultraviolet lithography, unzipping of carbon nanotubes [14]– [17], etc. Lithography can produce GNRs up to the width of 20 nm and produces uneven edges [14]. A combination of lithography and etching is presented in [15], in which lithography is used to pattern the ribbon, and etching is used to narrow it. In this method, GNR having a width of ∼4 nm has been produced. In [16], chemical synthesis has been used to produce GNRs up to ∼2 nm of width. There is another bottom-up chemical synthesis approach that can produce atomically precise graphene nanoribbon in different chirality and patterns in <2 nm of width [17]. The fabrication of ∼2 nm wide precise GNRs is reported in [18] and [19]. The approach in [19] displays the possibility of fabricating such narrow GNRs with perfect edges.

The following contributions are made in this paper:

- Explain the electrical properties of GNRFET.
- Design various basic ternary logic gates using GNRFET.
- Design more complex arithmetic circuits like a half adder, multiplexer using the basic gates.
- Compare different existing designs based on delay, power consumption, and Power Delay Product (PDP).

TABLE 1. Ternary Logic Values/Symbols And Voltage Levels

Voltage Level	Logic Symbol
0V	0 (False)
½ V_{DD} (0.45V)	1 (Intermediate)
V_{DD} (0.9V)	2 (True)

This paper is an extension of our recent conference paper [20], which introduces a GNRFET based ternary inverter design. This paper extends the basic concept presented in [20] and presents a general approach to implement GNRFET based logic and arithmetic circuits. The rest of the paper is organized as follows. Section II briefly illustrates the numerical explanation of the ternary logic system. Section III explains the operating principle of a GNRFET. Section IV presents the designs of a series of ternary logic gates and arithmetic circuits (NAND, NOR, Decoder, Half Adder, and Multiplexer) based on GNRFET. Section V provides a qualitative and quantitative comparison between the GNRFET based ternary circuits and those based on the prevailing technologies. The comparative analysis is performed in terms of delay and power consumption. Finally, Section VI concludes the paper with a brief discussion on our ongoing and future work.

II. TERNARY LOGIC SYSTEM

A binary number system is a number system that consists of two distinct logic levels: True (1) or False (0). This classical two-valued system can be further extended to a multiple-valued logic system that consists of "*R*" discrete logic levels, where $R > 2$. The different logic levels can be represented by some signal variables like voltage, current, or charge. The set of the discrete logic levels of an MVL device can be demonstrated by any of the two prevailing conventions: unbalanced and balanced. When the binary system is extended in such a way that the extension is constrained to only one direction, the system is called an unbalanced system. For instance, an *R*-bit unbalanced MVL system is represented by *0, 1, 2 … (R-2), (R-1).* And the balanced system is characterized by the set of the integer numbers with the help of an odd radix $R = 2K+1$ such as *(-K), (1-K) …-1, 0, 1 …. (K-1), K* [1].

The ternary logic system is one form of multi-valued logic (MVL) system, where the value of $R = 3$. Following the same convention of the MVL system, the unbalanced and balanced ternary logic system can be represented as *0, 1, 2,* and *-1, 0, 1*. In this paper, the unbalanced ternary logic system is implemented using a 0.9 V power supply (V_{DD}) and 0 V as the ground potential. The convention of the unbalanced ternary logic values and the corresponding voltage levels are illustrated in Table 1.

Based on the operating principle, a General Ternary Inverter (GTI) can be of three types: Negative, Positive, and Standard. A GTI is represented by (1), (2) and (3), where x is the input and y_0, y_1 and y_2 are the outputs that represent a Negative Ternary Inverter (NTI), a Positive Ternary Inverter (PTI) and a Standard Ternary Inverter (STI), respectively [21]. The truth table that represents the functions, y_0, y_1, and y_2, is shown in

TABLE 2. Truth Table That Represents Nti, Pti & Sti

Input (x)	NTI (y_0)	PTI (y_1)	STI (y_2)
0	2	2	2
1	0	2	1
2	0	0	0

TABLE 3. Truth Table For Ternary Nand, And, Nor & Or

Input 1	Input 2	NAND	AND	NOR	OR
0	0	2	0	2	0
0	1	2	0	1	1
0	2	2	0	0	2
1	0	2	0	1	1
1	1	1	1	1	1
1	2	1	1	0	2
2	0	2	0	0	2
2	1	1	1	0	2
2	2	0	2	0	2

Table 2.

$$y_0 = C_0(x) = \begin{cases} 2, x = 0 \\ 0, x \neq 0 \end{cases} \tag{1}$$

$$y_1 = C_1(x) = \begin{cases} 2, x \neq 2 \\ 0, x = 2 \end{cases} \tag{2}$$

$$y_2 = C_2(x) = \bar{x} = 2 - x \tag{3}$$

The elementary algebraic operations of ternary logic is given by (4), where, X, $Y = \{0, 1, 2\}$ [4]. Here, $+$ and $\bullet$ signs represent the NOR and NAND operations, respectively. Table 3 shows the truth tables of ternary NAND, AND, NOR, and OR.

$$\overline{X + Y} = \overline{\max(X, Y)} \tag{4a}$$

$$\overline{X \bullet Y} = \overline{\min(X, Y)} \tag{4b}$$

III. GRAPHENE NANORIBBON FIELD EFFECT TRANSISTOR

Graphene is an allotrope of carbon, which is a group 4 element like silicon and has four electrons in the valence band. Due to the presence of 4 electrons in the outermost band, carbon atoms form covalent bonds with the neighboring atoms and demonstrate mostly non-metallic behavior. In nature, carbon is found in many different non-metal forms. However, when carbon atoms are arranged in the crystalline structure of benzene-like rings of hexagonal shapes, several allotropes possessing extraordinary electrical properties are observed. Two of the most popular allotropes of carbon are carbon nanotube and graphene, which are widely explored as the replacement materials for silicon in the transistor channels [22]. Graphene is a two-dimensional, atomic-scale sheet of carbon atoms, which has a zero band-gap in normal state. If a narrow strip of graphene has a width of less than 50 nm, it is called Graphene Nano-Ribbon (GNR). GNR can be of two types depending on the edge structure: zigzag and armchair. While zigzag edged GNR always shows

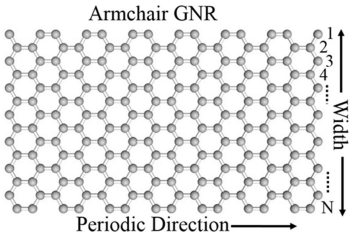

FIGURE 1. Width of an Armchair GNR with respect to Dimer lines.

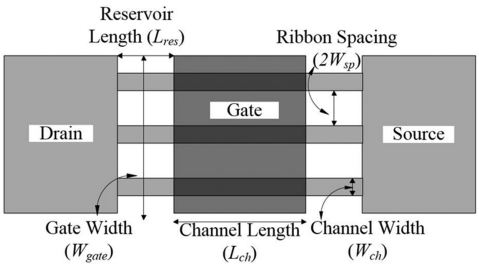

FIGURE 2. A multiple (three) ribbon Armchair GNRFET [24].

metallic characteristics, the armchair edged GNR can be either semiconducting or metallic in nature, depending on the ribbon width [23]. For the implemented MVL design in this paper, semiconducting GNR would be used.

Figure 1 exhibits the structure of an armchair Graphene Nanoribbon with N number of Dimer lines. The number of dimer lines (N) in a GNR strongly controls the semiconducting property of the GNR. The GNR shows semiconducting property mostly when $N = 3p$ *or* $3p + 1$, p being an integer [24]– [26]. Based on N, the width of a GNR can be expressed as in (5), where a_{c-c} signifies the lattice constant and the value is equal to 0.142 nm.

$$W_{GNR} = (N - 1)\frac{\sqrt{3}}{2}a_{c-c} \tag{5}$$

There are two types of GNRFETs: MOS-type and Schottky Barrier (SB) type. In the SB-GNRFET, the Schottky barrier is present at the interface of metal and graphene. Here, the charge transport is mainly due to the tunneling phenomenon through the barriers instead of the thermionic conduction as in the MOS-type FETs. Although the tunneling mechanism can overcome the fundamental thermionic limit of the MOS-type FETs (60 mV/decade), the MOS-type GNRFET is preferred here for designing the ternary logic circuits because of lots of advantages like higher I_{on}-I_{off} ratio due to absence of ambipolar transport, higher I_{on}, higher transconductance, better saturation behavior due to smaller output conductance, higher cutoff frequency, faster-switching speed, etc. [22]. In the MOS-type GNRFET structure, the *Si* channel is replaced by a parallel arrangement of multiple GNRs. Multiple parallel ribbons are provided to enhance the drive strength and create a wider contact. Figure 2 demonstrates the structure of

TABLE 4. Dependence Of Gnrfet Behavior On Dimer Lines (*N*)

Dimer Lines, N	Band Gap	I_{on}/I_{off}	Order of I_{on}/I_{off}	I_{on}
8, 11, 14, 17	Small	Lowest	$\sim 10^1$	Highest
6, 9, 12, 15, 18	Moderate	High	$\sim 10^6$	High
7, 10, 13, 16	Highest	Highest	$\sim 10^6$	Low

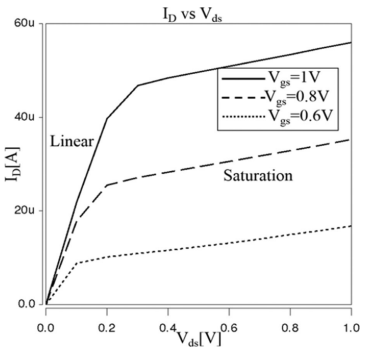

FIGURE 3. ID vs. Vds curve of an N-type GNRFET with respect to different values of Vgs.

a 3-ribbon MOS-type GNRFET. The portion of the ribbons, which is under the gate, is intrinsic in nature and called the channel. And the portion of the ribbon connecting the gate and the contact part is called the reservoirs, and they are heavily doped with a doping fraction of $f_{dop} = 0.001$ [27]. In Figure 2, L_{ch} = channel length, L_{res} = reservoir length, W_{ch} (W_{GNR}) = ribbon width, W_{gate} = gate width, and $2W_{sp}$ = spacing between the ribbons. The drain current in a GNRFET can be given by (6) [27].

$$I_D\ (\Psi_{CH}, V_D, V_S) = \frac{2qkT}{h} \sum_{\alpha} \left[\ln\left(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}\right) - \ln\left(1 + e^{\frac{q(\Psi_{CH} - V_D) - \varepsilon_\alpha}{kT}}\right)\right] \quad (6)$$

Here, Ψ_{CH} = Channel potential, V_D = Drain voltage, V_S = Source voltage, ε_α = Subband edge, α = Subband index ($1 \leq \alpha \leq N$), k = Boltzmann's constant, h = Plank's constant, and T = Temperature. As mentioned earlier in this section, if the width of the GNR is such that the number of dimer lines (N) is equal to $3p$ *or* $3p + 1$, that ribbon shows semiconducting behavior. If $N = 3p + 2$, that ribbon will exhibit more metallic nature [26]. Therefore, by controlling the value of N in the GNR channel, the threshold voltage and the I_{on}-I_{off} ratio of the GNRFET is modified here to achieve the desired multi-valued response. Table 4 summarizes the dependence of the electrical properties of the transistor on the number of dimer lines [27].

Figure 3 shows the I_D vs. V_{ds} curve with respect to a different level of V_{gs}. Initially, with the increase of V_{ds}, the drain current increases following a linear path, which represents the linear or triode region. After a certain $V_{ds,}$ the current follows the almost constant value, which denotes the saturation region. Figure 4 shows the I_D vs. V_{gs} curve for a drain to

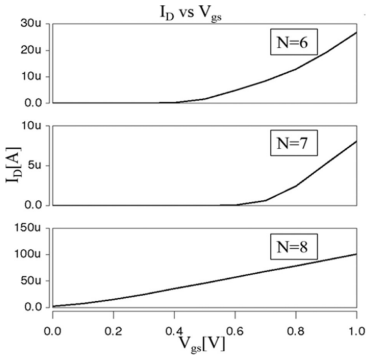

FIGURE 4. ID vs Vgs curve of an N-type GNRFET at Vds = 1 V for N = 3p, 3p+1 and 3p+2 (p = 2).

source voltage of 1.0 V. Like any other MOS-transistors, the I_D vs. V_{gs} curve gives a better understanding of the threshold voltage. For N-type GNRFET, increasing V_{gs} above a specific value turns the transistor ON. And as the gate voltage increases, the current also increases. In the Figure , the I_D *vs.* V_{gs} curve is given for $N = 3p$, $3p+1$, and $3p+2$ (where, $p = 2$). It is seen that for $N = 3p$ and $3p+1$, current switches from almost zero to a finite value, which results due to the semiconducting behavior of GNR. And for $N = 3p+2$, the I_{off} current is never zero, which results due to the metallic state of GNR. Upon close observation of the graph, the threshold voltage of the transistor for different values of N can also be measured.

IV. GNRFET BASED TERNARY LOGIC CIRCUITS

In this section, different basic ternary logic gates like inverter, NAND, and NOR are implemented utilizing the properties mentioned above of GNR. These logic gates are then used to design simple arithmetic circuits like decoder, half-adder, and multiplexer. For the implemented design and analysis, the GNRFET model files available on Nanohub [28] are used.

In the MOS-GNRFET model developed in [27], [28], the architecture is designed in such a way that there are multiple metal layers on the top of the single graphene layer. The metal gates of the GNRFET and most of the interconnects are comprised of those metal layers. The channels, drains, and sources of transistors are located on the graphene layer, and metal gates are located on the first metal layer. The width of the local GNR interconnects between transistors is 20 nm, which is much shorter than the mean free path of the graphene and, as a result, has negligible resistance. Due to this, the resistance of local interconnect within logic gates is neglected. The vias in the design is considered to be metal because the research on graphene vias is still on an underdeveloped level. Graphene-metal contact resistance is usually high [29]. For this reason, they are modeled with a 20-k resistor for a 50 nm wide via. In all the simulations in our paper, GNRFETs with three parallel armchair GNR as the channel is used (Figure 2). GNRFET with varied dimer length is used in the design to get appropriate threshold voltage. The channel length of each transistor is 16 nm.

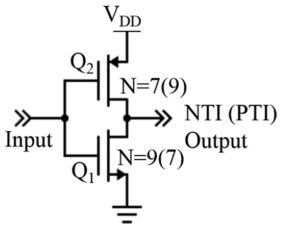

FIGURE 5. Schematic Diagram of Negative (Positive) Ternary Inverter.

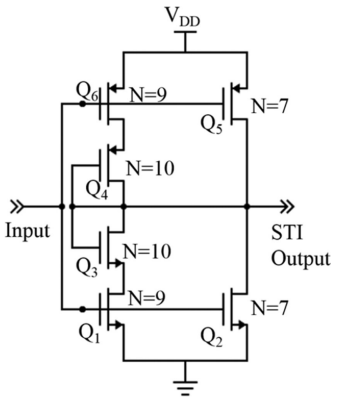

FIGURE 6. Schematic Diagram of Standard Ternary Inverter using GNRFET.

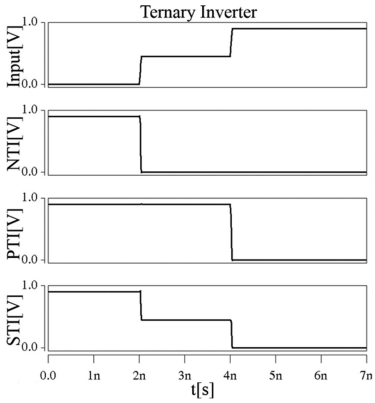

FIGURE 7. Transient response of NTI, PTI, and STI.

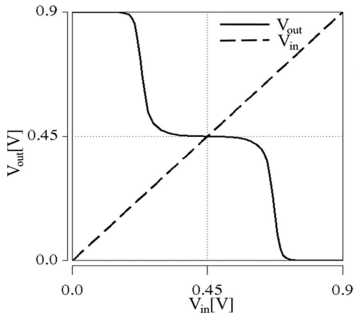

FIGURE 8. Transfer curve for GNTFET based STI.

A. INVERTER

Figure 5 shows the design for the negative ternary inverter (NTI) and the positive ternary inverter (PTI). For NTI, the numbers of dimmer lines (N) are 7 and 9 for the p-type and n-type GNRFET, respectively. For PTI, the values of N are 9 and 7 for the p-type and n-type GNRFET, respectively.

Figure 6 shows the standard ternary inverter (STI) design. The circuit topology for the inverter used here is similar to the CNTFET based inverter topology demonstrated in [2]. However, the operating principle and techniques to achieve multiple voltage levels are different in the proposed GNRFET based ternary inverter. For example, in CNTFET based ternary inverter, the chirality of the CNTs are varied to achieve different threshold voltages. On the other hand, in GNRFET, the width of the GNRs are varied to change the threshold voltage.

Here, Q_1, Q_2, and Q_3 are n-type transistors, and Q_4, Q_5, and Q_6 are p-type transistors. The threshold voltage of Q_1, Q_2, and Q_3 are 0.24 V, 0.6 V, and 0.4 V, respectively. The threshold voltage of Q_4, Q_5, and Q_6 are -0.4 V, -0.6 V, and -0.24 V, respectively. To obtain the specific threshold voltage, Q_1 and Q_6 are set to have $N = 9$, Q_2, and Q_5 to $N = 7$ and Q_3 and Q_4 to $N = 10$. If the input voltage is increased from low to high, when it is less than 0.3 V, Q_5 and Q_6 become ON, which makes the output voltage high. For an input voltage within the range 0.3 V and 0.6 V, Q_1 and Q_6 become on, and Q_3 and Q_4 perform as a diode-connected load. This maintains an intermediate voltage level at the output node. When the Input voltage reaches to a value higher than 0.6 V, Q_2 becomes ON, which brings the output voltage to a value equal to 0 V.

Figure 7 shows the transient response of three different types of ternary inverters. The voltage transfer curve for the STI is shown in Figure 8, which displays that the device is capable of holding three discrete output voltage levels for a wide range of input voltage. Four separate noise margins (NM) are relevant to the ternary logic circuit, and these are (i) noise margin low (NM_L), (ii) noise margin low-to-medium (NM_{ML}), (iii) noise margin medium-to-high (NM_{MH}), and (iv) noise margin high (NM_H) [30]. To estimate the robustness of the three discrete voltage levels (logic states) of the implemented STI, we performed the noise margin analysis using the butterfly curve method, as shown in Figure 9. Butterfly curve method is a well-known approach to determine the noise margins of logic and memory circuits. Figure 9 demonstrates that the GNRFET based STI has reasonably high noise margins to offer stable output voltages.

B. TERNARY NAND AND NOR GATES

Using the same convention used for the STI, we have designed both ternary NAND and NOR gates. The designs for these gates are presented in previous literature using different technologies [2]. Here, we have implemented the designs using GNRFET. Figure 10 shows the implemented design of a ternary NAND gate and its' logic symbol. Figure 11 shows the design of a ternary NOR gate and its' logic symbol. The

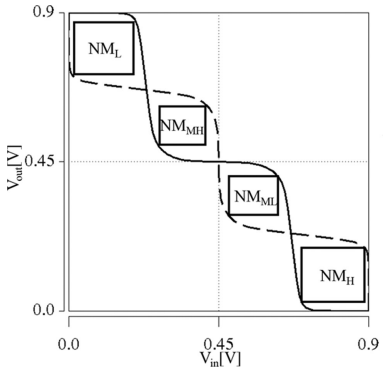

FIGURE 9. Butterfly curves for GNRFET based STI showing different Noise Margins (NM).

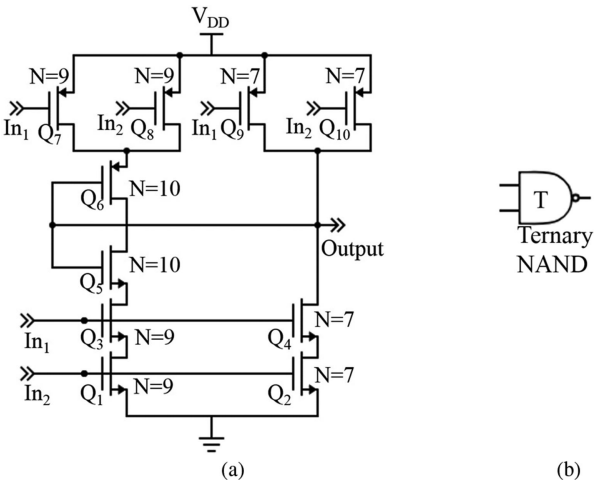

FIGURE 10. (a) Schematic Diagram (b) Logic symbol of GNRFET based 2-input NAND gate.

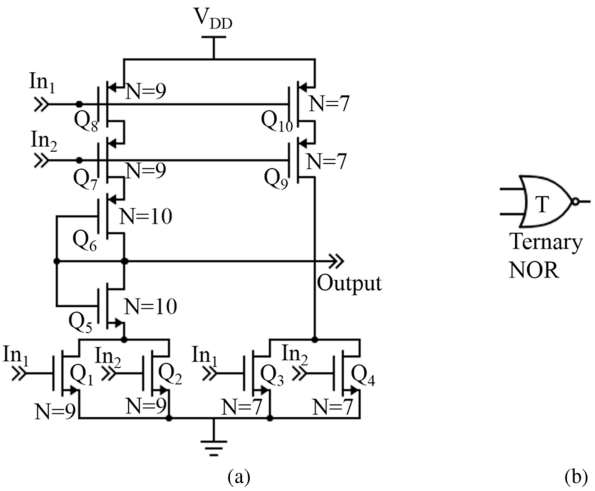

FIGURE 11. (a) Schematic Diagram (b) Logic symbol of GNRFET based 2-input NOR gate.

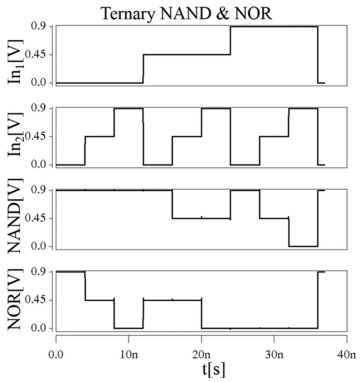

FIGURE 12. Transient response of a NAND and NOR gate.

TABLE 5. Truth Table For Ternary Half Adder

Input A	Input B	Carry	Sum
0	0	0	0
0	1	0	1
0	2	0	2
1	0	0	1
1	1	0	2
1	2	1	0
2	0	0	2
2	1	1	0
2	2	1	1

transient response for the ternary NAND and NOR gates are shown in Figure 12.

C. TERNARY DECODER

Using the logic gates mentioned above, a ternary decoder can be designed. The decoder is an essential part of a ternary half adder. It has one input port (X) and three output ports (X_0, X_1, and X_2). A ternary input voltage operates the decoder, and depending on the input voltage level, one of the three output ports gives a high output voltage. For example, if the input voltage is 0 V, the X_0 node will show a high voltage level (V_{dd}). The logical relation between the input and output ports of the decoder is represented by (7), and its schematic diagram and transient response are shown in Figure 13.

$$X_k = \begin{cases} 2, x = k \\ 0, x \neq k \end{cases} \tag{7}$$

D. TERNARY HALF-ADDER

The ternary half adder takes two 1-trit input voltage and produces a 1-trit sum and a 1-trit carry as the outputs. Table 5 shows the truth table of the ternary half adder.

From the truth table, the equations for the sum and carry outputs can be expressed in terms of input A and B as in (8).

$$Sum = 2 \bullet (A_0B_2 + A_1B_1 + A_2B_0) + 1 \bullet (A_0B_1 + A_1B_0 + A_2B_2) \tag{8a}$$

$$Carry = 1 \bullet (A_1B_2 + A_2B_1 + A_2B_2) \tag{8b}$$

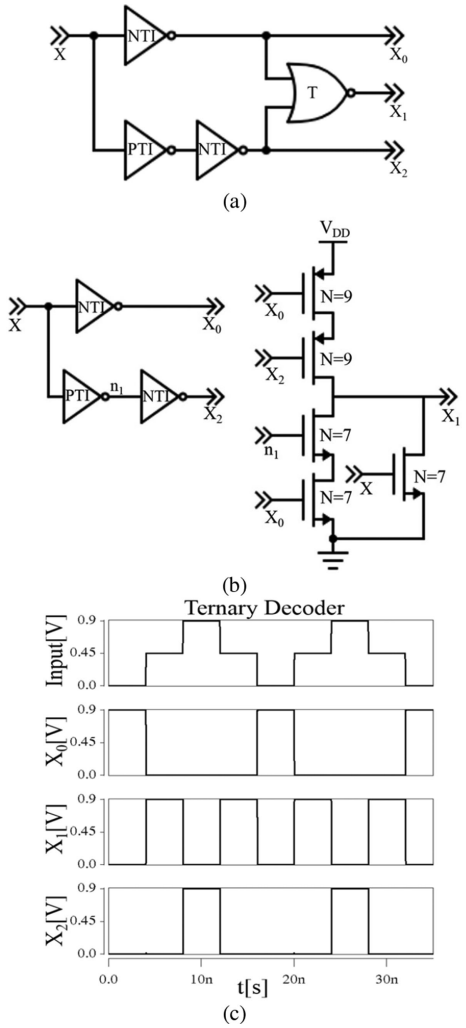

FIGURE 13. (a) Schematic Diagram of ternary decoder presented in [31] (b) Proposed diagram of the ternary decoder (c) Transient Response of proposed ternary decoder.

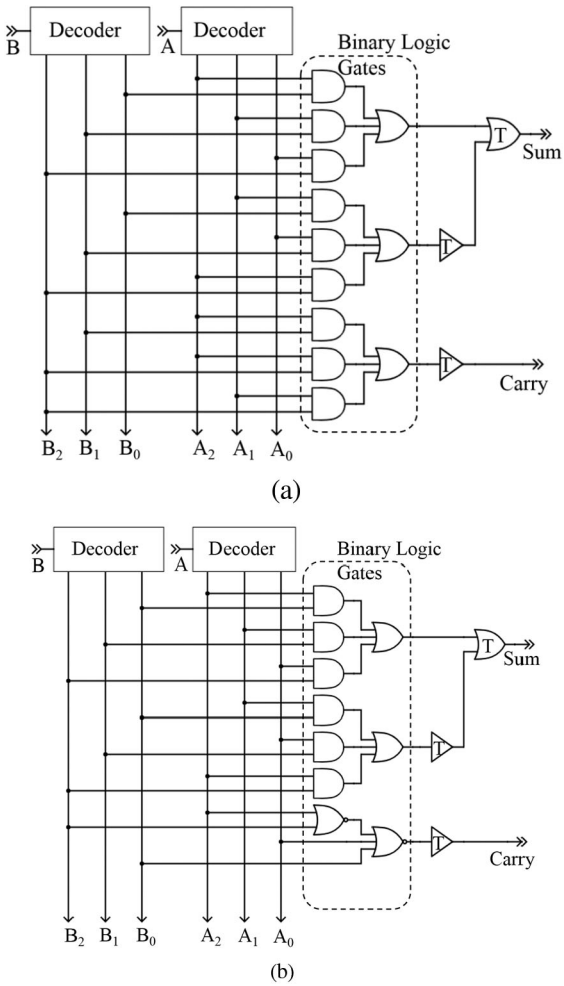

FIGURE 14. (a) Schematic diagram of ternary half adder [31] (b) Proposed design of ternary half-adder.

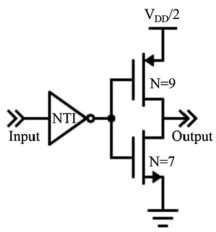

FIGURE 15. Proposed schematic diagram of T-buffer.

For the internal operation of the adder, different designs have been proposed in [4], [5], and [31]. Among them, the design in [31] uses the simplest and the most efficient topology using CNTFET. For the half adder, we have followed the topology of [31] and proposed a simpler carry circuitry which requires lesser transistor. Figure 14(b) demonstrates the proposed diagram of the ternary half adder using our proposed decoder. Here, the decoder is ternary, and it takes ternary input and produces high voltage levels at the respective output port, depending on the input voltage level. For example, for the input $A = 2$ and $B = 1$, it will give full rail-to-rail voltage on A_2 and B_1. The second stage of the ternary half-adder is made of binary logic gates, which receive the input signals from the ternary decoder output nodes to generate the half-adder outputs as in (8). And the outputs of these binary logic gates remain in binary form. The third stage of the half-adder circuit is comprised of a ternary OR and a T-buffer gate, which converts the binary signals from the second stage to ternary signals. T-buffer is a simple circuit that acts as a level shifter. The logical operation of the T-buffer is as shown in (9), and the proposed circuit diagram of the T-buffer is shown in Figure 15. The input-output voltage curves of the ternary half-adder of Figure 14 is shown in Figure 16. It is observed that the voltage curves match the truth table exactly.

$$\text{Out} = \begin{cases} 1, & Vin = 1, 2 \\ 0, & Vin = 0 \end{cases} \tag{9}$$

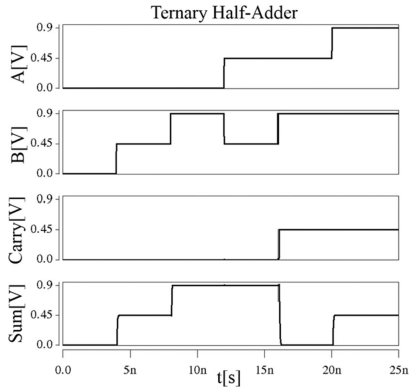

FIGURE 16. Transient Response of the ternary half-adder.

TABLE 6. Truth Table For 3:1 Ternary Mux

Selector (S)	Output
0	A
1	B
2	C

E. TERNARY MULTIPLEXER

The basic multiplexer is a device, which depending on the signal value in a particular select pin, can transmit one of several inputs to the output port. For example, in case of a 2:1 binary multiplexer (MUX), if the value on the select pin is 0, input-1 will be transmitted to the output, and if the value on the select pin is 1, input-2 will be transmitted. Here, we propose the design of a 3:1 ternary multiplexer, which can transmit any one of the 3 inputs to the output port depending on the select pin value. And it can transmit both binary and ternary data. Table 6 shows the truth table, and (10) represents the logical expression (input-output relation) of the 3:1 ternary MUX.

$$Out\,put = S_0\,A + S_1 B + S_2 C \tag{10}$$

Here, the values of S_0, S_1, and S_2 are obtained from a ternary decoder explained in the previous subsection. Depending on the input voltage value at the select (S) input terminal, it passes the corresponding input signals (A, B, or C) to the output port.

The logic and schematic diagrams of the ternary MUX are shown in Figure 17, where S denotes the select pin and A, B, and C are the three different inputs of the multiplexer. Figure 18 shows the simulated output of the multiplexer. The voltage range in those inputs is varied in such a manner that it can be observed that the circuit can transmit inputs of all voltage range. Here, input A is a signal within the range 0 to 2, input B is in the range of 0 to 1, and input C is in the range of 1 to 2. In all of the cases, the signal is passed accordingly without any significant distortion.

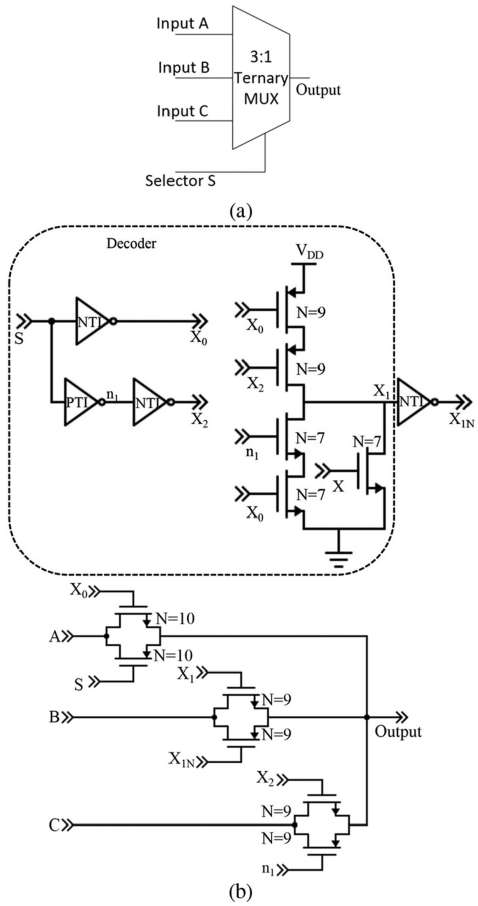

FIGURE 17. (a) Logic Diagram and (b) Schematic Diagram of 3:1 Ternary MUX.

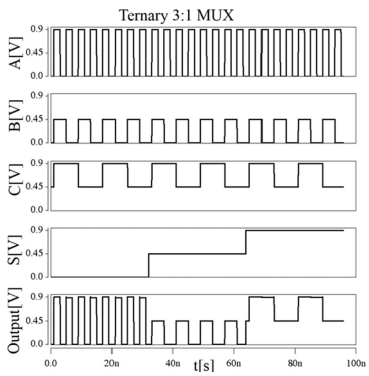

FIGURE 18. Transient Response of 3:1 Ternary MUX.

V. COMPARISON

In the literature, many CNTFET based ternary logic gate designs can be found. It is widely perceived that GNR would be a better choice for the transistor channel than CNT. Therefore, this paper focuses on GNRFET based ternary logic and arithmetic circuit implementation. Here, a comparative analysis between some of the existing CNTFET, GNRFET, CMOS, and the proposed GNRFET based basic ternary logic circuits

TABLE 7. Comparative analysis between existing cntfet and the proposed gnrfet based ternary logic gates

Logic Gates		Transistor count	Delay (ps)	Total power (nW)	Power Delay Product, PDP (e-18)
STI	CNTFET [31]	6	11	88.6	0.98
	CNTFET [34]	-	18.8	1170	33.2
	CNTFET [35]	6	8.9	263	2.34
	GNRFET [36]	6	30	8100	24
	GNRFET [37]	3	1.57	22200	34.9
	Proposed Work	6	13	23.22	0.302
NAND	CNTFET [31]	10	3	100.8	0.3
	CNTFET [34]	-	27.6	704.8	19.46
	GNRFET [36]	10	58	1580	92
	Proposed Work	10	5.2	27.5	0.14
NOR	CNTFET [31]	10	2	100	0.2
	CNTFET [34]	-	27.3	1054	28.79
	GNRFET [36]	10	47	1635	77
	Proposed Work	10	3.33	27.42	0.1
Decoder	CNTFET [31]	16	15	15.57	0.234
	Proposed Work	11	14	6.09	0.09
Mux	Proposed Work	19	1.5	1.548	0.002

are summarized in the latter portion of this section. All the simulations are done using an input slew of 50ps and an output load of 1pf. The doping fraction f_{dop} is selected to be 0.001 for all the transistors.

For the simulations, [6] uses the CNTFET model file derived in [36]. The transistors used in [31] are the 16 nm CNTFET model. The simulations are done in H-spice using model files from Stanford Nanoelectronics lab, which are derived in [32], [33].

The comparison between different basic gates in terms of delay, leakage power, total power, and power-delay-product (PDP) of CNTFET and GNRFET is presented in Table 7. From the Table, it can be observed that, in terms of delay, total power, and PDP, our proposed logic gates hold a lot of promise in the field of ternary devices.

Figure 19 shows the delay comparison of three different types of ternary half-adder circuits presented in [6], [21], and [31] with the proposed GNRFET based half-adder. Here,

T1 = 0-1 rise time delay of "Sum" with respect to "*B*"
T2 = 1-2 rise time delay of "Sum" with respect to "*B*"
T3 = 0-1 rise time delay of "Carry" with respect to "*B*"
T4 = 0-1 rise time delay of "Sum" with respect to "*A*"

It is observed that the delay in the proposed GNRFET based half-adder design is much lower than the other three designs.

The comparison of the transistor count and power-delay-product (PDP) of the proposed GNRFET based ternary half-adder with one MOSFET based and five other CNTFET based half-adder circuits is shown in Table 8. It shows clearly that in terms of PDP, the proposed GNRFET based ternary half-adder offers a significant improvement over other designs.

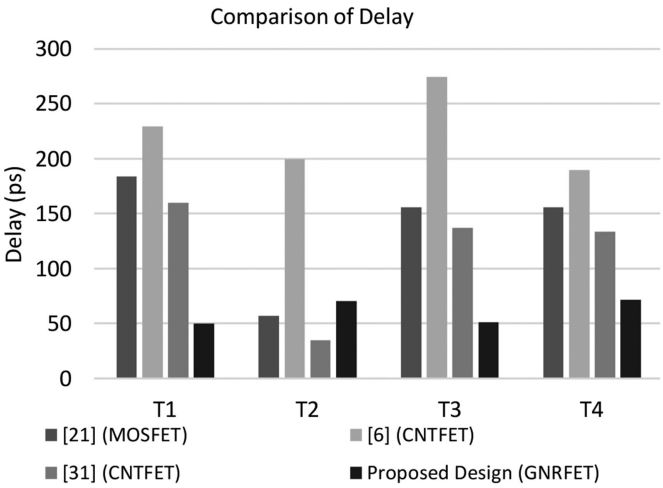

FIGURE 19. Comparative analysis of transient delay of half adder for different designs.

TABLE 8. Comparative Analysis Of Pdp (Power-Delay Product) Of The Proposed Gnrfet Based Half-Adder Design With Different Existing Designs

References	Technology	Transistor count	Power-Delay-Product (PDP) (e-15)
[21]	MOSFET	-	0.542
[38]	CNTFET	64	0.025
[6]	CNTFET	-	6.7
[39]	CNTFET	65	0.117
[31]	CNTFET	136	0.411
[40]	CNTFET	112	0.05
[41]	CNTFET	90	0.159
Proposed Design	GNRFET	108	0.01

There are a few designs available, which can significantly decrease the transistor count [38], [39]. These papers focus on the transistor-level designs of half-adder circuits. On the contrary, our proposed design focuses on the implementation of the half-adder circuit using basic logic gates (e.g., decoder, NAND, NOR, etc.). The logic-gate based implementation requires a higher number of transistors but enables more flexibility in the design. Compared to other similar logic gate based designs [31] and [40], our proposed design offers a lower transistor count.

VI. CONCLUSION AND FUTURE WORK

This paper presents the designs of a set of basic ternary logic gates (inverter, NAND, and NOR) and circuits (decoder, multiplexer, and half-adder) based on GNRFET. These particular set of basic gates and circuits are selected to establish the proposed design methodology. These basic gates and circuits can be utilized to implement any complex logic, arithmetic, and signal processing circuits. Here, the fundamental approach is to control the threshold voltage and other electrical properties of GNRFETs by changing the width of the GNRs to obtain different output levels. A comparative analysis between some

of the proposed GNRFET based ternary logic gates and circuits and existing designs is performed in terms of delay, leakage power, total power, and power-delay-product (PDP). It is observed that the proposed GNRFET based ternary gates and circuits offer significantly better results compared to similar gates and circuits based on CMOS and CNTFET technologies. The H-SPICE simulation and analysis are performed using a GNRFET model available on Nanohub, and the channel length for the device is selected to be 16 nm. The proposed design approach can be extended to implement quaternary logic.

However, it is essential to acknowledge that this paper is an attempt to establish the fundamental design concept of GNRFET based ternary logic gates and circuits. Some many issues and challenges need to be addressed before implementing more complex circuits like ternary full adders and complete ternary application systems. Implementing ternary memory with the proposed logic gates and circuits is another direction that can be pursued. As memory is the most critical part of any electronic system, increasing information and data storage capacity while decreasing delay and power consumption are the grand challenges for the memory designers. The ternary logic system is highly promising to resolve the grand challenges of the memory industry. It is also important to remember that the analysis techniques and design metrics for the MVL devices and circuits are still evolving. Our ongoing and future work is focused on addressing some of the issues and challenges mentioned above.

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