Sub-2 nm Size-Tunable High-Density Pt Nanoparticle Embedded Nonvolatile Memory

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***Abstract*—The charge-storage characteristics of a metal–oxide–semiconductor (MOS) structure containing size-tunable sub-2 nm Pt nanoparticles (NPs) between Al_2O_3 tunneling and capping oxide layers were studied. Significantly different amounts of memory window were obtained with the different sizes of Pt NP embedded MOS structures and reached a maximum of 4.3 V using a 1.14 nm Pt NP, which has the strongest charging capability caused by optimum size and the largest particle density obtained in our deposition method. Satisfactory long-term nonvolatility was attained in a low electric field due to the Coulomb blockade and quantum confinement effects in ∼1 nm Pt NP. These properties are very promising in view of device application.**

***Index Terms*—Nanoparticle (NP), nonvolatile memory (NVM), size-tunable platinum.**

I. Introduction

NONVOLATILE memory (NVM) devices using charge-storage mechanisms face serious obstacles due to the further downscaling of tunneling oxide thickness [1]. Metal nanoparticle (NP) embedded NVM devices have been attractive because metal has a larger work function and higher density of states than a semiconductor [2], [3] and it is easy to tune the barrier height for carrier injection due to numerous choices of metal [4]. In addition, metal NP embedded NVMs employing high-k dielectrics enable equivalent oxide thickness scaling and thus exhibit smaller operating voltage, faster program/erase (P/E) speeds, better data endurance, and long retention characteristics [5]. NPs smaller than 2 nm have the added benefit of the Coulomb blockade effect [6].

There are several ways to form metal NPs using physical vapor deposition. Specific to Pt NPs, two examples of NP formation processes include thermal dewetting technique [7], [8] and electron beam evaporation [9]. The first technique does not satisfy a low thermal budget and the particle distributions are broad, and the second technique shows inability to control uniform and spherically shaped NPs smaller than 5 nm.

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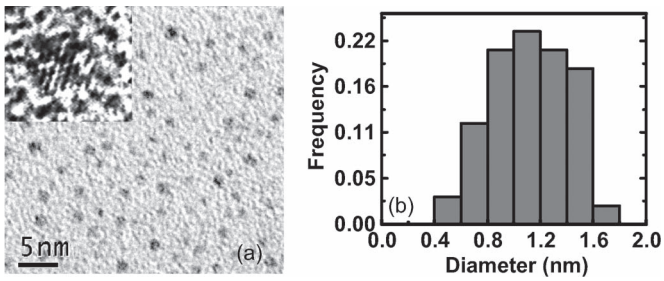

Fig. 1. (a) Plane-view TEM images of 20 s deposited Pt NPs. The inset of (a) shows monocrystallinity of Pt NPs. (b) Particle size distribution of 20 s deposited Pt NP samples over three images after statistical postimage analysis. The error in the analysis is caused by the lack of contrast between the NPs and the amorphous substrate material.

Recently, we have conducted research on metal NP formation using sputtering deposition without subsequent annealing. In this direct deposition, the average size of the NPs is simply controlled by varying deposition time with constant pressure, power, and gas flow rate at room temperature. This technique produces uniformly distributed spherical Pt NPs with mean diameters between 0.5 and 2 nm, having a high particle density $> 10^{12}$ cm^{-2}. In this method, we exploit the earliest stages of film growth where metal clusters arrive on the substrate surface and diffuse until encountering nucleation (trap) sites [10], [11]. Small clusters remain trapped at these sites and grow in size due to the continuous flux of atoms. The large surface energy difference between Al_2O_3 (40–50 mJ/m^2) and Pt (2190 mJ/m^2) dictates a Volmer–Weber type islanding growth mode with spherical particles. Our major motivation for a sub-2 nm size-tunable metal NP together with high particle density is for better controllability of the different memory capabilities of scaled NVM devices [12].

In this letter, we demonstrate size-tunable sub-2 nm Pt NP embedded metal–oxide–semiconductor (MOS) devices, utilizing thin Al_2O_3 tunneling and control oxide layers. Endurance and retention characteristics are also demonstrated.

II. Device Fabrication

Low-doped p (100) silicon was used to fabricate MOS capacitors. An e-beam system was utilized to deposit a 4.3 nm tunneling Al_2O_3 layer. Samples were immediately transferred to the sputtering system to deposit Pt NPs onto the tunneling oxide with the following deposition times: 5, 10, 20, 30, and 45 s. A power of 30 W RF was used with a working pressure of 4 mTorr and 10 sccm of Ar gas flown at room temperature

TABLE I
SUMMARY OF PLATINUM NPs AS A FUNCTION OF DEPOSITION TIME

Deposition time (s)	Nominal thickness (nm)	Average size (nm)	Average particle density ($\times 10^{12}$ cm^{-2})	Memory window (V)	Electron charge density ($\times 10^{12}$ cm^{-2})	Number of electrons per NP
5	~0.002	~0.5	~1-3	0.92	1.1	0.36-1.1
10	~0.011	0.8±0.1	3.95±1.08	2.03	2.3	0.58
20	~0.038	1.14±0.07	4.87±0.63	4.26	4.7	0.97
30	~0.094	1.54±0.05	4.9±0.85	3.78	4.3	0.77
45	~0.200	1.98±0.02	4.85±0.2	1.63	1.9	0.39

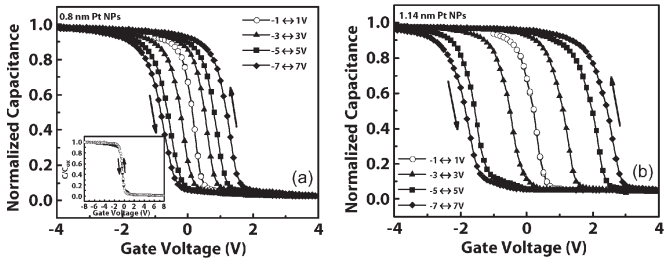

Fig. 2. High-frequency (1 MHz) bidirectional C–V curves of (a) 0.8 and (b) 1.14 nm Pt NP embedded memory device under different sweeping gate voltages. The C–V curve of the control sample is shown in the inset of (a). The control and active devices have negligible hysteresis when uncharged, as shown in (open circles) the initial voltage sweep. The $V_{\rm FB}$ of this range is the initial $V_{\rm FB}$ and used for $V_{\rm FB}$ shift calculation. The left three branches represent hole charging states while the right three branches represent electron charging states.

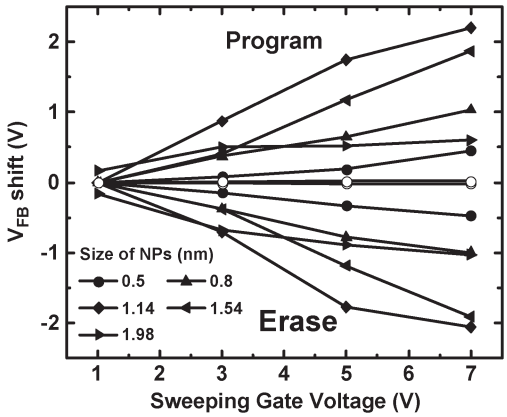

Fig. 3. $V_{\rm FB}$ shift as a function of P/E voltages from C–V curves according to the different sizes of Pt NPs. (Light open and labeled) Negligible $V_{\rm FB}$ shift in the control samples is shown.

[10]. Samples were again transferred to the e-beam for 14 nm Al_2O_3 capping oxide deposition and subsequent *in situ* H_2 gas annealing at 260 °C for 45 min. Finally, 250 nm Ti electrodes of 4.42×10^{-5} cm^2 were patterned using a shadow mask. A control sample without NPs was also prepared by the same process. Capacitance–voltage (C–V) measurements were performed using a Keithley 4200-SCS equipped with the 4200-CVU integrated C–V option. Data were taken with a voltage step of 0.1 V and a 30 mV ac signal at 1 MHz.

III. RESULTS AND DISCUSSION

Fig. 1 shows the plane-view transmission electron microscopy (TEM) image (a) and size-distribution analysis (b) of 20 s deposited Pt NPs, whose average size and density are estimated as 1.14 nm and 4.87×10^{12} cm^{-2}, respectively. The high-resolution TEM image in the inset of Fig. 1(a) shows the monocrystalline structure of the Pt NP. Table I summarizes the nominal layer thickness, size, and density of Pt NPs according to the different deposition times.

Fig. 2(a) and (b) shows the C–V curves of 0.8- and 1.14 nm Pt NP embedded memory devices under different sweeping voltages. The inset of Fig. 2(a) shows that there is a negligible hysteresis in control sample under the same applied voltage. Thus, the $V_{\rm FB}$ shift of the active device is attributed to electron charging in Pt NP or at the interface between NP and Al_2O_3, not from the defects in Al_2O_3 [13]. Counterclockwise hysteresis loops were observed, indicating electron injection from substrate to Pt NPs under positive voltage for the programming and hole injection under negative voltage for erasing by Fowler–Nordheim (F-N) tunneling [7]. It was also shown that $V_{\rm FB}$ shift under different sweeping voltages gradually increased with a uniform increase of F-N injection and finally saturated over a certain value within the measurement range.

Interestingly, there was a remarkable difference of memory window between 0.8- and 1.14 nm Pt NP embedded samples. The $V_{\rm FB}$ shift as a function of P/E voltages according to the different size of Pt NPs is shown in Fig. 3. Initially, there was no memory effect in the control sample, but the $V_{\rm FB}$ shift increased gradually with increased size and density of Pt NPs. The memory window reached its maximum value of 4.3 V with the 1.14 nm Pt NP sample which has optimum size and maximum density of NP, resulting in the strongest charging capability among the samples. As the particle size increased, the memory window decreased due to a reduction in Coulomb charging energy [6]. However, the exact nature of the decreasing memory window is still not clear, and we are striving to find the reason using further experiments such as different speeds of P/E characteristics and single electron tunneling effect. This will be presented as a follow-up paper. Since the C–V curve between ± 1 V with no memory window is located approximately in the middle of the hysteresis loop for each device, the amount of electron storage in Fig. 3 will be half of the area of the hysteresis loop. By using the relationship $N_t = (C_{\rm ox}\Delta_{\rm FB})/q$, where N_t is the trapped charge, $C_{\rm ox}$ is the oxide capacitance density, $\Delta_{\rm FB}$ is the $V_{\rm FB}$ shift, and q is the elementary charge, we find that, for 1.14 nm Pt NPs with particle density $(4.87 \times 10^{12}$ cm$^{-2})$ and electron charge density $(4.7 \times 10^{12}$ cm$^{-2})$ after programming, each Pt NP serves one electron storage node due to the small $\sim$1 nm size of NP, which is truly a single electron memory device.

As shown in Fig. 4(a), the endurance characteristics of the 1.14 nm Pt NP embedded memory devices were observed for up

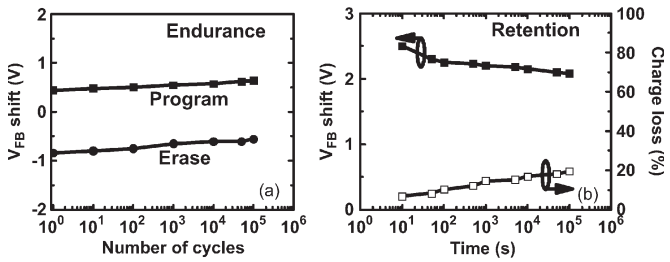

Fig. 4. (a) Endurance characteristic of 1.14 nm Pt NP embedded memory device. (b) Retention properties of the memory device at programming and its charge loss percentage versus time. The percentage of charge loss is calculated using the expression $(1 - V_{\rm FB}(t)/V_{\rm FB}(0)) \times 100$, where $V_{\rm FB}(0)$ is the $V_{\rm FB}$ after stressing and $V_{\rm FB}(t)$ is the $V_{\rm FB}$ at the time of interest.

to 10^5 cycles with 100 ms stress pulses of ± 6 V, demonstrating a stable memory window. No significant memory narrowing was observed up to 10^5 cycles. The memory device also showed good retention characteristics when applying a 5 s stress pulse of 7 V program voltage and sweeping C–V periodically, as shown in Fig. 4(b). Initial capacitance abruptly dropped by 10% within a short period of time due to the tunneling back of electrons and then maintained its $V_{\rm FB}$ up to 10^5 s because of the buildup of a high opposing electric field in the tunnel oxide.

IV. Conclusion

Pt NPs using room-temperature sputter deposition with a simple variation of deposition time were embedded into Al_2O_3 double layers to develop NVM devices. The memory devices showed different amounts of memory window from 1 to 4.3 V under low P/E voltages, good endurance, and long retention properties without narrowing. Our approach in developing metal NP embedded NVM devices is a good candidate for nonvolatile Flash memory and is compatible with low-temperature semiconductor processing.

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