DEVELOPMENT OF PULSED POWER SOURCES USING SELF-SUSTAINING NONLINEAR TRANSMISSION LINES AND HIGH-VOLTAGE SOLID-STATE SWITCHES

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ABSTRACT

The demand for short pulses capable of delivering high peak power is increasing by leaps and bounds over the last few decades. These pulses are garnering attraction from a wide variety of end-users associated with the military, medical, industry, etc. The diverse nature of the potential application spaces asks for agility and customization capability of the pulses in terms of frequency, voltage level, and current level to fit varying degrees of requirements. Several pulsed power approaches can generate high-power pulses including direct switch-based pulsers, pulse forming lines (PFLs), Marx generators, nonlinear transmission lines (NLTLs), pulse transformers, etc. Among these pulsed power approaches, NLTL showcases frequency-agility in output pulses that distinguishes it from the rest of the competition. NLTLs either sharpen the input pulse or break down the input pulse into a finite number of pulses with decaying amplitudes, known as solitons. This research work combines the uniqueness of the NLTL in terms of frequency agility and the robustness of the laterally-diffused metal-oxide-semiconductor (LDMOS) devices to produce self-sustaining oscillations from a single input pulse. To date, this research work is one-of-a-kind in the field of NLTLs used for generating medium-power RF signals. Multiple NLTLs have been fabricated to identify the best available

candidate showcasing excellent nonlinearity. The NLTL, coupled with a custom high voltage pulse generator, an LDMOS based amplifier, and RF matching networks constitute a closed-loop setup that produces solitons with a peak power close to 2.1 kW. The experimental results are verified by LTSpice simulations as well.

Direct high-voltage (HV) switch-based pulser is another intriguing option to produce pulsed power in a compact footprint. This approach can be easily streamlined compared to other pulsed power approaches thanks to the reduced number of required components. Traditionally, spark gap switches have been predominantly utilized in direct HV switch-based pulser. High voltage withstanding capability and high current carrying capability of the spark gap switches solidified their position during the early stages of pulsed power system development. That being said, the brilliance of the spark gap switches is overshadowed by the long jitter, limited lifetime, and inability to operate at higher switching frequencies which are some of the critical modern-day pulsed power requirements. To that end, the quest for an alternative switching candidate has led the researchers to solid-state semiconductor switches (e.g., MOSFETs, IGBTs, etc.) that can be employed in pulsed power systems. The solid-state semiconductor switches are inherently faster compared to the spark gap switches, thereby enabling operation at higher switching frequency as opposed to the spark gap switches. The lifetime of these switches is also much longer compared to the spark gap switches, and they offer mostly jitter-less operation. That being said, the voltage withstanding ability of the commercial-off-the-shelf (COTS) MOSFETs is limited to 3.3 kV which is inadequate for many pulsed power applications. Connecting multiple COTS MOSFETs in series is an intriguing way to increase the volage withstanding ability of the entire switch stack. However, ensuring

voltage balancing among the series-connected MOSFETs during the OFF state as well as the switching transition is a major design challenge for the researchers working in this field. The capacitive coupling method is one of the mechanisms that ensure voltage balancing among the series-connected switches while occupying a smaller area compared to other competing methods. However, literature pertaining to capacitive coupling-based series-connected switches illustrates experimental results using a HV switch with a maximum stage count of two. This research work outlines the design and development process of a capacitively coupled 6.8 kV rated four-stage SiC switch. Simulation results exhibit excellent voltage balancing traits which are reinforced by the experimental results. Modularity has been introduced in the HV switch design to facilitate the scalability of the switch in terms of voltage withstanding capability. This feature allows the user to tailor the switch in accordance with the voltage requirement of a potential pulsed power application by connecting multiple modules in series. A 10 kV rated modular SiC switch has been designed and fabricated based on the capacitive coupling method. At a high voltage level (>5.7 kV), custom gate drivers are required to provide adequate galvanic isolation. To drive the 10 kV rated switch, a 10 kV rated custom isolated gate driver has been designed and developed. The design procedure of this custom gate driver is detailed in this dissertation. The modular SiC switch coupled with the custom isolated gate driver has been tested up to a supply voltage of 6 kV exhibiting excellent voltage balancing, thereby validating the modularity concept of the HV switch.

APPROVAL PAGE

The faculty listed below, appointed by the Dean of the School of Graduate Studies have examined a dissertation titled " Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches" presented by A N M Wasekul Azad, candidate for the Doctor of Philosophy degree, and certify that in their opinion it is worthy of acceptance.

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DEDICATION

To my parents, Abul Kalam Azad and Shefali Begum, and my wife, Farhana Taher Sumya for their unconditional love and sacrifice have made me who I am today.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Pulsed power technology alludes to the technique that entails accumulating charge over a relatively long period (μs-min) and releasing that charge within a short period (ps-μs), thereby delivering a tremendous amount of power to the output load.

The origin of the pulsed power technology can be traced back to the 1960s when J.C. Martin and his colleagues of the British Atomic Energy Research Center (AI) combined a Blumlein line with a previously developed Marx generator to compress the width of an input pulse from microseconds to a few tens of nanoseconds [1]. During that era, the capabilities of the pulsed power sources were primarily leveraged in gigantic systems such as particle accelerators, fusion research, laser system, electromagnetic launchers, etc [2]–[7]. During its early age, the growth and development of pulsed power technology were primarily governed by the military or nuclear requirements, rendering it more of a specialized branch of research. United States, China, former Soviet Union, Japan, and many advanced countries in Europe were the pioneers in establishing pulsed power facilities leading to the development of pulsed power sources. For instance, AHrapa-5 was the first pulsed power source made in the Soviet Union in 1985 using a combination of Marx-Blumlein technologies with spectacular parameters of 2 MV, 40 MA, 90 ns. United States soon followed suit by developing its pulsed power source in the form of the PBFA-II (12MV, 8.4ma, 40ns) developed by Sandia laboratories in 1986 [8]. For historical and political reasons, Japan refrained from developing pulsed power sources for military purposes. Instead, pulsed power devices such as Etigo-II

were developed at the Nagaoka University of Technology in 1986 with a peak voltage of 3 MV, a peak current of 400 kA, and a pulse width of 60 ns for inertial confinement fusion research [9].

Over the last few decades, considerable development has taken place in the field of pulsed power technology embellishing this technology with promising features tailored for a wide range of applications with diverse backgrounds, biomedical, industry, environment, to name a few. Pulsed power sources are being used in environmental spaces, for instance, pulsed corona, and other ion purification methods of waste gas technology, high-pressure pulse discharge wastewater outlet, pulse electrostatic dust removal, microbial sterilization, and disinfection, production of ozone, etc [10]–[12]. In the biomedical field, pulsed power sources have been successfully employed to offer a potential non-intrusive treatment mechanism for cancer, malignant tumor, etc. Programmed cell death (apoptosis), electroporation are among some of the premeditated clinical phenomena induced by the application of pulsed power sources [13], [14]. Pulsed power sources have penetrated several other fields including but not limited to geophysical and underwater target detection, rock drilling, high-speed X-ray underwater photography, and rapid heating and quenching, etc [15], [16].

In light of the ever-increasing demand for pulsed power sources in a diverse array of applications, the research interest in this field has also heightened manyfold. In keeping with the widening application space of pulsed power, the importance of flexibility in the parameter space of the high-power pulses is growing. Long gone the days when a single long pulse with high peak power was primarily asked of a pulsed power source. Nowadays, frequency agility, waveform shape variation, high repetition frequency, compactness are some of the advanced

characteristics that end users yearn for from pulsed power sources. For example, the rise time of the output pulse waveform governs the efficacy of the pulsed power system in some of the applications where the impact of the pulse rise time is pronounced. Majority of the industrial applications that employ pulsed power sources as a key enabler require pulsing at a high repetition frequency. Therefore, researchers have delved deep into this field to devise unique schemes to meet the versatile demand stemming from a wide range of applications resulting in a number of pulsed power techniques, including pulse forming lines (PFLs), Marx generator, nonlinear transmission lines (NLTLs), semiconductor opening switch-based pulser, high-voltage switch-based pulser, etc.

The majority of the aforementioned pulsed power sources typically include a DC power supply, an energy storage unit, a pulse forming line, a switching device, and an output load. The simplest form of operation entails charging the energy storage unit up to the level of supply voltage over a relatively long period. The sored energy is then modulated into a pulse with a shorter width in the quasi-square or exponentially decayed wave shape. The output pulse waveform and repetition frequency are heavily influenced by the switching devices of these pulsed power sources. Unlike other methods of producing high-power pulse, NLTLs do not require a switching device to modulate an input pulse into a pulse with higher peak power with reduced rise time. On top of that, the constituting dielectric or magnetic material of an NLTL governs the center frequency of the output RF pulses and this frequency can be adjusted by changing the length of the NLTL as well. This frequency agility coupled with the absence of switching devices makes NLTL an intriguing pulsed power source. That being said, an NLTL can only generate a finite number of RF pulses from a single input pulse, therefore requiring a

continuous supply of input pulse stream to produce continuous output. Conversely, the HV switching devices are indispensable parts of the other pulsed power sources. Conventional switching devices used in these pulsed power sources typically come in the form of spark gap, vacuum tube, thyratron, etc. These magnetic and gas-based switches have high voltage withstanding capability and high current carrying capability that set them apart from other competing switches. However, these switches are plagued by high jitter, short life span, low operational frequency, etc. To make it worse, these switches are bulky and expensive as well, thereby compromising their compatibility in a high-speed application that emphasizes the portability and compactness of the overall pulsed power source as well.

Recent ongoing development in the fabrication process of semiconductor devices, especially wide bandgap (WBG) devices, have ushered in a new wave of fast, low-jitter, and reliable semiconductor switches (e.g., MOSFETs, IGBTs, etc.). These switches have paved the way for a new generation of pulsed power sources that are capable of switching at a higher rate with low jitter and extended lifetime. That being said, commercial solid-state semiconductor switches still trail the traditional magnetic and gas-based switches in terms of sheer voltage withstanding and current-carrying capability. To retain the high-speed advantage offered by the solid-state semiconductor switches while hitting the required voltage and current levels in pulsed power applications, researchers have come up with a technique where multiple semiconductor switches can be connected in series and parallel to increase the voltage withstanding ability and current-carrying capability. One of the most intriguing methods to accomplish this objective is the capacitive coupling method which entails driving series-connected switches using coupling capacitors, and a single gate driver is used for the entire

stack of the series-connected switches. The tangible advantages offered by the capacitive coupling method notwithstanding, experimental validation of the functionality of this method for multiple stages in terms of voltage balancing during steady-state and switching transients is lacking from the literature.

1.2 Research Objective

In this research, the lack of a working high-voltage switch prototype based on the capacitive coupling method has been addressed. A four-stage high-voltage switch using the capacitive coupling method based on SiC MOSFETs (WBG MOSFET) has been proposed and developed. The developed prototype has showcased excellent voltage balancing property during both steady-state and switching transients. Taking the capacitive coupling-based HV switch design one step further, modularity has been introduced in the HV switch design. This unique feature allows customization of the HV switch in terms of voltage rating by connecting multiple modules in series eliminating the need for a complete design overhaul. As the voltage rating of the modular custom HV switch is increased, a new design challenge springs in terms of the isolation rating of the gate driver. Commercial gate drivers with a high isolation rating (>5.7 kV) are not readily available till now. Therefore, a custom gate driver with sufficient isolation is needed to be designed to drive the modular HV switch. Within the scope of this research, a 10 kV rated isolated gate driver has been designed to drive a 10 kV rated modular HV switch.

As a pulsed power source, an NLTL separates itself from the rest of the class thanks to the absence of switching devices. However, the limited availability of nonlinear components in commercial space, and the requirement of continuous input supply, hinder the growth of this

pulsed power source in pulsed power applications. In this research, a novel design involving an NLTL, a power amplifier, and RF matching networks has been proposed that is capable of generating a continuous stream of solitons from a single input pulse. This unique feature can pave the way for the portability of the NLTL based pulsed power source.

1.3 Dissertation Outline

This dissertation is organized into eight (8) chapters. Chapter 2 gives a brief overview of the existing pulsed power techniques underscoring the relative advantages and disadvantages pertaining to each technique. Chapter 3 explains the broad categories of NLTLs as well as the fundamentals of soliton generation in a lumped element NLTL to set the stage for what comes in the next chapter. The detailed design procedure of a self-sustaining soliton generator is outlined in Chapter 4. The major components of the proposed self-sustaining soliton generator are discussed at length and simulation and experimental results are presented validating the proposed concept. Chapter 5 highlights the present need for a high-voltage solid-state switch in the field of pulsed power and challenges associated with the development of a high-voltage solid-state switch. Potential solutions to overcome the development challenges of HV switch are also elaborately discussed. Chapter 7 presents the design details of a series-connected four-stage HV SiC switch based on the capacitive coupling method along with ample simulation and experimental results. Chapter 8 highlights the introduction of modularity in the series-connected HV switch topology. The operating principle of the switch is articulated in detail in this chapter. The design concept is validated by simulation and experimental results and documented in this chapter. Finally, conclusions and future works are discussed in Chapter 8.

CHAPTER 2

LITERATURE REVIEW OF PULSED POWER TECHNOLOGIES

2.1 High-Voltage Switch Based Pulser

A high-voltage (HV) switch-based pulser represents one of the simplest ways to generate high voltage pulses. The basic configuration of an HV switch-based pulser includes a HV DC power supply, a capacitor bank to store charge, and a stack of switches to form a HV switch as shown in Fig. 1(a) [17], [18]. The primary design consideration in this approach is to ensure that the HV switch is able to withstand the entire DC supply voltage during the turn-OFF period. Spark gap switches are traditionally furnished with high voltage withstanding capability and high current carrying capabilities. However, limited lifetime and incompatibility with higher repetition frequency have driven the researchers towards solid-state switches (e.g., MOSFETs, IGBTs, etc.) that are capable of switching at a much faster rate as opposed to the spark gap switches. The tradeoff lies in the fact that these solid-state switches have limited capabilities with regards to voltage withstanding and current carrying. Therefore, an array of switches configured in series and parallel connections is required to satisfy the high-voltage and high-current requirements of pulsed power applications. The configuration shown in Fig. 1(a) includes a snubber circuit as well to limit the current in the case of an arcing phenomenon and facilitate abrupt interruption of circuit operation to avoid a destructive accumulation of arc energy. During high-power consumption, the output voltage across the load might experience considerable droop. A mitigation scheme is illustrated in Fig. 1(b) entailing a bouncer capacitor C_B, and an inductor forming a resonant circuit and termed as *L*-*C* bouncer [19]. The bouncer circuit is activated before the HV switch is triggered to compensate for the droop.

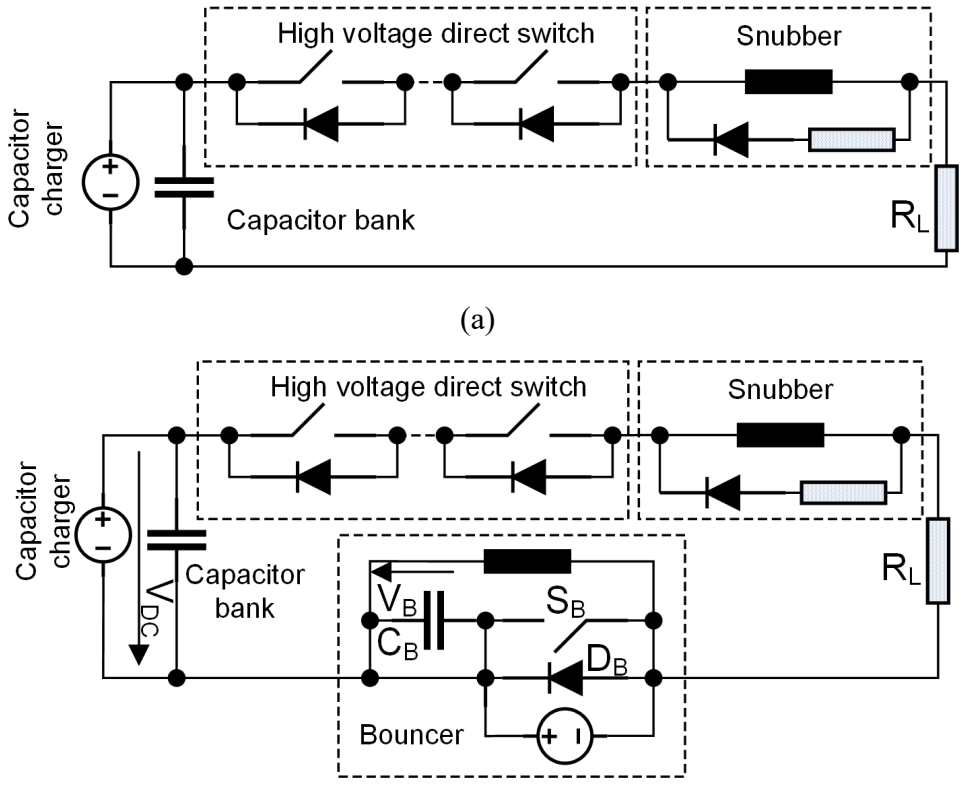


Fig. 1: Direct HV switch based pulser topology (b) Direct HV switch topology with active droop compensation, snubber circuit and voltage signals at different points of interest [17], [18]

The primary advantage of this pulse modulator topology is its simple construction, scalability that helps to discard pulse transformer from the design, thereby attaining a smaller footprint. That being said, series-connection of multiple switches requires a special scheme for voltage balancing during OFF state and during switching transitions which renders the approach sophisticated in case of very high voltage levels. On top of that, the capacitor charger, capacitor bank, and the HV switch is needed to be isolated from the output and therefore submerged in oil to reduce the modulator size.

2.2 Pulse Forming Line

A lot of pulsed power applications have exclusive requirements of short flat-top pulses with high peak power. One of the simplest yet most effective ways to generate short flat-top rectangular or square pulse at an extremely high-power level for numerous pulsed power applications is using pulse forming lines (PFLs) or their pulse forming network (PFN) analogs [20]–[24]. There exists a number of variants of pulse forming lines to cater to a variety of applications. The simplest form of PFL can be fabricated using a transmission line, a fast switch, and a DC supply [25]. This configuration can be coined as a single pulse forming line alluding to the use of a single transmission line in the configuration. The basic schematic of a single pulse forming line is shown in Fig. 2 [26].

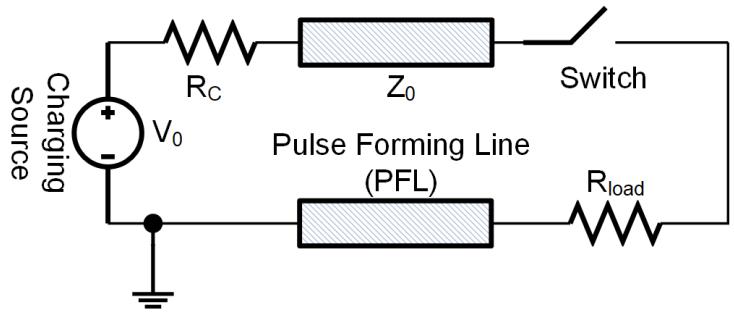


Fig. 2: Basic configuration of a single pulse forming line [26]

The transmission line is charged to the supply voltage level through a resistor with high impedance to minimize the level of the charging current to avoid overloading the DC power supply and/or to safeguard the switch from excessive current. The impedance of the charging resistor is required to be substantially larger than the characteristic impedance of the transmission line to ensure proper formation of the output voltage across the load. Once the transmission line is charged, the switch is closed, and the transmission line is discharged through the switch across the load. A rectangular-shaped output pulse is formed across the load

with a width twice the transit time that a voltage step would require to traverse the line from one end to the other end. If the load impedance is matched to the characteristic impedance of the transmission line, the theoretical value of the peak amplitude of the output pulse would be half of the peak amplitude of the input pulse. Coaxial cables or parallel-plate-type microstrip lines can be used as the transmission line depending on the impedance of the output load. Coaxial cables are typically manufactured with a fixed set of impedances (e.g., 50Ω, 75Ω, etc.), thereby suitable for use with output loads with similar values. However, for a diverse range of output impedances, parallel-plate transmission lines are more suitable as they can be fabricated to attain a dynamic range of impedances.

One of the major drawbacks associated with the single pulse forming line is that the maximum attainable output voltage is half of the input voltage provided by a DC power supply. At an extremely high power level requiring high peak voltages, the aforementioned issue can mount a serious practical challenge in terms of the availability of an extremely high-voltage power supply. Blumlein pulse forming line, invented by A. D. Blumlein offers a potential solution to this problem. The output voltage that can be obtained using the Blumlein line is equal to the input voltage if the impedance of the output load is twice the characteristic impedance of the transmission line. A basic Blumlein line can be constructed using two transmission lines of equal length and a closing switch as shown in Fig. 3 [24]. However, the width of the output pulse can only be varied by changing the length of the transmission line, or for PFNs, changing constituting components. This physical constraint makes it difficult to tune the parameter of the output pulse required by different applications. On top of that, the nonzero ON-resistance of the closing switch contributes to considerable distortion in the output

pulse. These aforementioned problems pertaining to the basic Blumlein line configuration can be mitigated using two independently controllable closing switches at either end of the transmission lines as shown by the dotted line in Fig. 3 [24]. This assembly allows for a modification of pulse polarity, pulse width without changing the physical dimensions of the transmission lines.

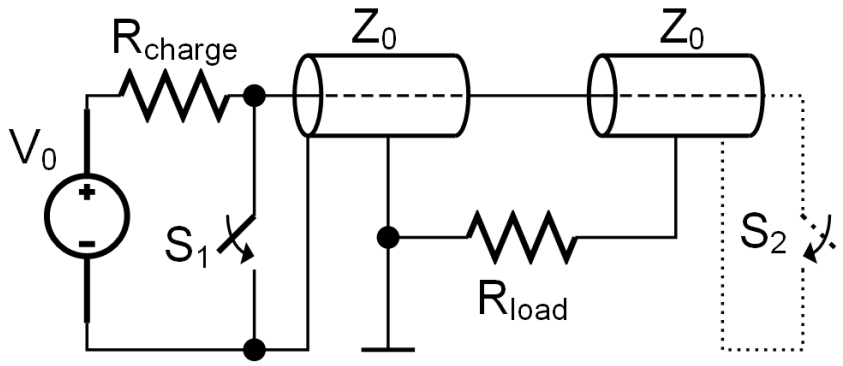


Fig. 3: Schematic of a basic Blumlein line configuration with one closing switch (solid line), and a modification involving a second closing switch at the end of the pulse forming line (dotted line) [24]

2.3 Nonlinear Transmission Lines

The width of a pulse generated from a single pulse forming line is typically proportionally related to the length of the transmission line. Coaxial cables and stripline type pulse forming lines are most commonly used to fabricate transmission lines pertaining to a pulse forming line. Coaxial cables, however, are manufactured with a limited number of impedance values (e.g., 50Ω, 75Ω, etc.), thereby rendering them incompatible in many pulsed power applications where output loads assume a wide range of impedance values. Fabrication of striplines can be customized to assume a wide range of impedance values. That being said, the dielectric constants of the dielectric materials (e.g., polymer plastic such as polypropylene) that are typically used to isolate the two constituting conductors of the stripline tend to be on

the lower side (ε_r = 2-3) [25]. The wave propagation velocity (v_p) through a stripline is related to the relative permittivity (ε_r) of the dielectric material through the following equation.

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} \quad (1)$$

Where c represents the velocity of light and ε_r represents the relative permittivity of the dielectric constant of the insulating material of the stripline. To produce a pulse having a width in the range of microseconds using stripline, long transmission lines are required which may be impractical in many cases. An alternative method tailored for pulsed power applications is using pulse-forming networks. Pulse forming networks features ladder networks constructed from inductors and capacitors. One of the prominent pulse forming networks used for generating high-power pulses is the nonlinear transmission line (NLTL). NLTLs have been successfully put into use in pulsed power applications over the last few decades thanks to their unique offerings in the form of frequency-agility, relatively high power, etc. The key contributing component in an NLTL is the nonlinear material either in the form of nonlinear dielectric material or magnetic material. This nonlinear material is periodically arranged in an NLTL, leading to pulse sharpening and/or a stream of high-frequency oscillation in the RF or microwave regime, known as solitons. The nonlinearity sharpens the input pulse and the dispersion pertaining to an NLTL leads to the breakup of the input pulse into a stream of high-frequency oscillations. A combination of nonlinear capacitors and nonlinear inductors can be used to fabricate an NLTL. Lumped element NLTL and gyromagnetic NLTLs are the two major NLTL types suitable for high power RF signal generation. Gyromagnetic transmission lines have demonstrated their capability of generating RF signals in the GHz range [27]. On top of that, as a compact RF source, NLTLs have showcased their capability to operate at a

repetition frequency greater than 1 kHz [28], [29]. That being said, sourcing a diverse array of materials with nonlinear dielectric or magnetic characteristics has been a field of interest for researchers.

2.4 Marx Generator

Marx generator is a kind of pulsed power modulator that relies on the charging of the capacitors in parallel and discharging in series into a load to obtain a high-voltage, high peak-power pulse. It is one of the most widely studied and used power modulator schemes thanks to its modularity and ease of design [30]–[37]. The Marx generator extends its versatility in the fields of high power systems such as kicker magnets [38], a critical component in particle accelerators; in plasm generation and control [39], and the medical field for tissue welding and cancer treatment [14]. Traditionally, spark gap switches have been used extensively in Marx generators to produce high-power pulses due to their high-voltage withstanding ability and high current carrying capability. That being said, compatibility issue at high repetition rate has inspired researchers to replace the bulky spark gap switches with more potent alternatives. With the recent advancement in semiconductor switch technologies, the spark gap switches are being replaced by all-solid-state semiconductor switches enabling a higher repetition rate and more compact footprint of the new-generation Marx generators. In an ideal Marx generator, the n number of capacitors are charged in parallel to produce a high-voltage pulse with a peak magnitude of nV_{DC}, where V_{DC} is the input voltage magnitude and n is the number of stages in a Marx generator circuit configuration as showcased in Fig. 4 [40].

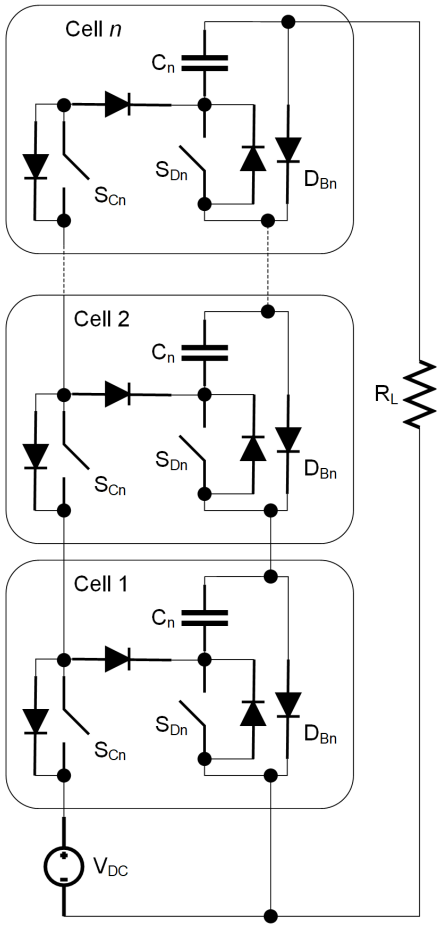


Fig. 4: Modular solid-state Marx modulator schematic [40]

A single module of a Marx generator consists of a charging switch S_C, a capacitor C, a discharging switch S_D, bypass diode D_B, and high-voltage switches, typically implemented using MOSFETs or IGBTs. During the charging phase, charging switches (S_{C1}----S_{Cn}) are triggered, thereby charging the capacitors (C_1, C_2----C_n) in parallel to a voltage level equaling to the level of the input voltage V_{DC} through the bypass diodes. The high-voltage output is delivered to the load during the discharging period. During this period, the charging switches (S_{C1}----S_{Cn}) remain turned-OFF, and the switches denoted by S_{D1}---S_{Dn} are triggered ON, thereby connecting the capacitors in series and discharging the high-voltage across the load.

The charging switches can be replaced by high-valued resistors to fulfill the requirements including but not limited to reduced complexity, more compact footprint, reduced cost, shorter pulse length [32]. However, owing to the large values of the charging resistors, the charging and the discharging paths remain decoupled from each other.

The advantage of the Marx generator is underscored by the ease of output voltage scalability by adding more modules, and the requirement of providing galvanic isolation up to the charging voltage level (V_{DC}). However, the output voltage level does not linearly scale up keeping in line with the increasing number of stages.

2.5 Pulse Transformer

Pulse modulators based on solid-state technology offer superior performance compared to the traditional spark-gap switch-based modulators in terms of switching frequency, lifetime, etc. That being said, solid-state technologies still lag behind the spark-gap switches from voltage withstanding ability and current-carrying capability standpoint. Pulse transformers are often combined with the solid-state switch-based pulse modulators to overcome this issue by facilitating the required voltage or current step up by virtue of flexible turns ratio [41]–[43]. The introduction of pulse transformers in a pulse modulator simplifies the design of the pulse modulator itself as a result of the lessened requirement of series or parallel connected switches to meet the application requirement. However, in practical pulsed power applications, such as radar systems, particle accelerators, and klystron modulators, a flat top pulse is required. Parasitic parameters (e.g., leakage inductance, distributed capacitance, etc.) pertaining to the pulse transformers influence the output pulse shape obtained from the pulse transformer to a great extent. Some crucial output pulse parameters such as rise time, overshoot, voltage droop

are significantly impacted by the parasitic parameters of the pulse transformers [42], [44]–[46]. Therefore, the meticulous design of pulsed transformers is of paramount importance to exert control over the parasitic parameters of the pulse transformers. Pulsed transformers are combined with pulse modulators in a number of ways as showcased in Fig. 5 [43].

The pulse transformer can be incorporated in a direct switch-based pulser as shown in Fig. 5(a). It can be coupled with a Marx generator circuit as well as illustrated in Fig. 5(b). The pulse transformer works in tandem with the direct-switch-based pulser and the Marx generator to reduce the number of solid-state switches connected in series and number of stages respectively. The addition of a pulse transformer also facilitates the use of a low-voltage input DC supply. To meet the requirement of higher output pulsed power, multiple switches can be connected in parallel at the input side of the pulse transformer as illustrated in Fig. 5(c). However, a current balancing scheme for the parallel connected switches is required in this scheme. An alternative approach to mitigate this issue can be splitting the single transformer into multiple transformers with a reduced turns ratio with the secondary windings connected in series as shown in Fig. 5(d).

Pulse transformers are associated with some level of leakage inductance depending on the quality of the design and geometric configuration. Leakage inductance adversely impacts the rise time (t_{rise}) of the output pulse as stated in the following equation.

$$t_{rise} \sim \sqrt{L_\sigma C_d} \tag{2}$$

Where C_{d} is the stray capacitance of the pulse transformer. The total leakage inductance associated with the configuration shown in Fig. 5(d) reduces as the number of split

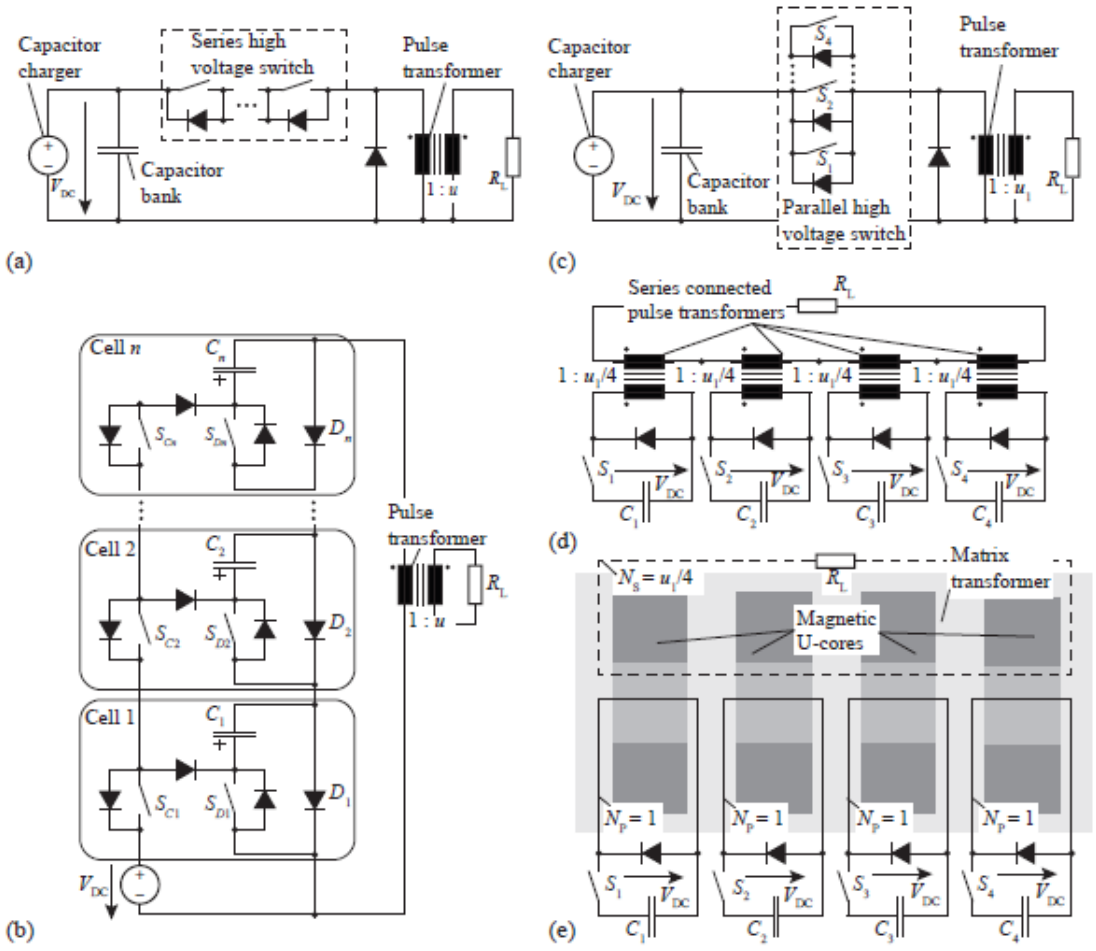


Fig. 5: Hybrid pulse transformer topologies: (a) Direct series HV switch + pulse transformer, (b) Marx generator + pulse transformer. (c) Direct parallel HV-switch + pulse transformer (d) Series connection of four single pulse transformers with the same output behavior as in (c). (e) Matrix transformer solution with the same output behavior as in (c) and (d), which results in lower transformer parasitic than in (c) and (d) [43]

transformers increases, and the total stray capacitance increases as this number increases. Fig. 5(e) showcases a matrix transformer that consists of four cores, enclosed by the secondary winding. The flux coupled to the secondary winding is the sum of the fluxes in the primary windings, thereby turns ratio is the same as the configuration shown in Fig. 5(d). The biggest advantage offered by this configuration is the reduction of leakage inductance and a smaller footprint.

Pulse transformer-based modulators typically occupy a significant amount of space, limiting their practical use in applications requiring portable and compact solutions. On top of that, the introduction of a pulse transformer in a Marx generator topology or a HV switch-based topology negates the advantage offered by the modularity of these topologies.

CHAPTER 3

FUNDAMENTALS OF NONLINEAR TRANSMISSION LINES (NLTLS) AND SOLITON GENERATION USING NLTL

Nonlinear transmission lines (NLTLs) are a class of pulse forming networks (PFN) for modulation of pulsed power to generate radiofrequency (RF) signals. Primarily, NLTL designs assume a two-port configuration, which requires one-to-tens of nanosecond input pulse rise time for each modulated pulse out. NLTL designs exploit the nonlinearity of the permittivity, and/or permeability to transform an input pulse into a shockwave or a series of oscillations with decaying amplitudes, known as solitons. The origin of these oscillations can be traced back to the precession of magnetic moments for nonlinear magnetic materials or the translations of the dipole in the crystalline structure for nonlinear dielectric materials. NLTLs are capable of operating at a repetition frequency greater than tens of kHz and capable of delivering high peak power in the range of MW, thereby rendering them an attractive candidate for high-power RF applications [47], [48]. On top of that, the use of NLTLs in high-power radio-frequency (RF) generation is gaining further momentum as their mode conversion efficiency and enabling components have improved [49]–[52]. NLTL utilization can be extended to applications in pulse compression, satellite communication, radar, electron beam drivers, defensive countermeasures, and battlefield communication disruption [53]–[56]. Robust and compact solid-state switching as the NLTL feed mechanism is, therefore, an enabling sub-technology, which when coupled in a closed-loop or positive feedback system as first described in [57], yields a potential leapfrog.

NLTLs used in high-power RF generator circuits can be classified into two major categories: (1) lumped element transmission lines assembled from a ladder network of identical

L-C sections, where a balance between the dispersion and nonlinearity gives rise to RF pulses; and, (2) gyromagnetic lines built from ferrimagnetic materials (ferrites), where damped precession of magnetic dipoles polarized by an external magnetic field yields RF pulses [58]. In an NLTL-based RF pulse generator, an input pulse can be decomposed into a stream of pulses with a narrower width, and heightened peak power (i.e., sharpening) compared to the input pulse, which propagates along the line while maintaining the shape and velocity throughout the line. This particular form of RF pulse(s) can be represented as a soliton(s). The balancing act between the dispersion and nonlinearity of the NLTL gives rise to the formation of solitons. The dispersion can be attributed to the periodic nature of the line, whereas the nonlinearity originates from the complex permittivity of the solids (e.g., the nonlinearity of ceramic capacitors, varactors, current dependent inductors, etc.).

Researchers have utilized NLTLs to deliver RF power into output loads in the form of solitons. Gyromagnetic lines typically generate RF signals with center frequency ranging from 500-MHz to a few GHz while achieving reported peak power as high as 100-MW [59]–[62]. As opposed to the gyromagnetic lines, lumped lines tend to be more compact with a caveat of generating RF signals with lower peak power and lower center frequency ranging from a few MHz to 1.2 GHz [63]. That being said, the compactness of the lumped NLTLs paves the way for the researchers to devise a portable high-power RF signal generator. Traditionally, NLTL designs assume a two-port configuration that is capable of generating a finite number of soliton bursts from an input pulse. The characteristics (e.g., frequency, peak amplitude, voltage modulation depth (VMD), oscillation count, etc.) of the soliton bursts are governed by at least the width, shape, and rise time of the input pulse, section count of the NLTL, level of

nonlinearity and dispersion of the NLTL. The nonlinearity of the commercial-of-the-shelf components (e.g., Schottky diodes, ceramic capacitors, varactor diodes, saturable inductors, etc.) are largely non-customizable, thereby imposing an upper threshold of frequency, and amplitude related to the solitons generated from the lumped NLTLs. However, by making changes to the configuration of the nonlinear components in the building block of the NLTL, the frequency of the solitons can be increased.

3.1 Lumped Element Nonlinear Transmission Lines

Lumped element transmission lines are typically constructed using identical *L*-*C* ladder blocks in series. The capacitor, and/or the inductor of a single block can be nonlinear, thereby contributing to the generation of solitons or a shockwave with higher amplitude. The nonlinear components can be either bought off-the-shelf or they can be custom-made. A typical lumped element NLTL can be illustrated as shown in Fig. 6 [64].

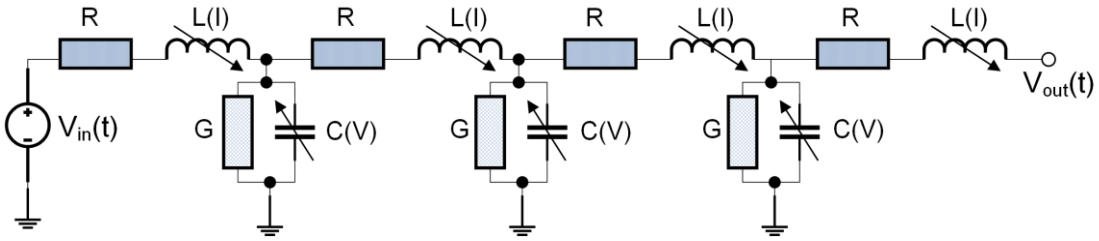


Fig. 6: Schematic of a lumped element nonlinear transmission line comprising of nonlinear inductor and nonlinear capacitor [64]

The general form of the wave equation for the NLTL shown in Fig. 6 can be expressed as:

$$\frac{\partial^2 V(x)}{\partial x^2} = (j\omega L(I) + R)(j\omega C(V) + G)V(x) \tag{3}$$

Where V represents the input voltage, x denotes the position along the line, $L(I)$ represents the nonlinear inductance as a function of current I, $C(V)$ represents the nonlinear capacitance as a function of voltage V and G is the conductance in parallel with $C(V)$.

Numerical techniques, such as the Bulirsch-Stoer or Runge-Kutta methods are some of the well-defined methods to solve the wave equation related to the generated solitons from the NLTL [65]–[67]. It is found out that the Runge-Kutta method is more efficient in solving wave equations for very steep rise time thanks to its simpler step calculation compared to the Bulirsch-Stoer method [66].

A lumped element transmission line can be represented by modeling transmission line capacitance and inductance as functions of voltage and current respectively. The resulting Korteweg-de Vries equations can be numerically solved for a number of NLTL configurations, namely, nonlinear inductors with linear capacitors [68], nonlinear capacitors with linear inductors [69], and hybrid lines composed of nonlinear inductors and nonlinear capacitors [70].

3.2 Gyromagnetic Nonlinear Transmission Lines

Gyromagnetic line alludes to a continuous ferrite-loaded nondispersive line biased by an axial magnetic field. Unlike lumped element NLTLs, the nonlinearity of a gyromagnetic line stems from the variation of the magnetic permeability with respect to current. The frequency of the output RF signal can be tuned by adjusting the external magnetic field bias and the peak voltage of the input pulse [71], [72]. The coaxial line used for a gyromagnetic line can be either azimuthally or axially biased for pulse compression and efficient RF signal generation from magnetic precession respectively. During azimuthal bias, the gyromagnetic

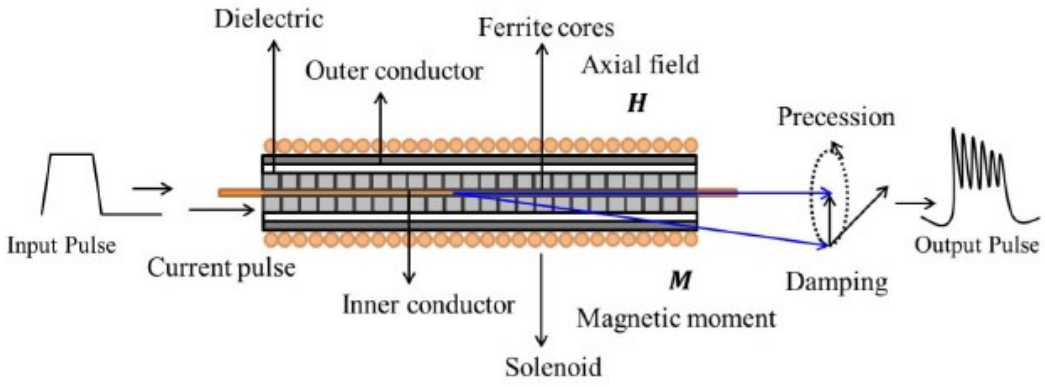


Fig. 7: Precession of magnetic moment *M* in gyromagnetic line [72]

line is biased by a DC current that flows through the inner conductor, and the ferrites encircling the line are saturated in the opposite direction at the application of this bias current. Conversely, as a result of the application of the axial bias, the entire effective field gets twisted as the azimuthal field generated by the current pulse injected onto the line is superimposed on the axial field.

As illustrated in Fig. 7, if the gyromagnetic line is subjected to an axial magnetic field H_z, upon injection of a current pulse with a magnitude of I, the magnetic moment M of the ferrites around the line changes their initial alignment along the longitudinal axis after their interaction with the azimuthal bias, leading to the pulse compression phenomenon [72]. The magnetic moment of the ferrite or ferroelectric material (e.g., barium titanate (BT), barium strontium titanate (BST)) stems from the positioning of the atoms in the polycrystalline structure. A high-frequency precession motion of the magnetic moment also initiates as soon as the current starts to propagate through the line leading to high-frequency oscillations with a shape similar to the input pulse, but with a reduced rise time.

3.3 Theory of Soliton Generation in Lumped Element Transmission Line

A lumped element nonlinear transmission line is a ladder network comprising identical sections of shunt capacitors and series inductors [63]. The shunt capacitor, the series inductor, or a combination of both can introduce nonlinearity in a lumped element NLTL. The potential capacitive elements exhibiting nonlinearity include Schottky diodes with nonlinear junction capacitance [73], nonlinear ceramic capacitors [74], and/or nonlinear ceramic dielectric slabs [75]. On the other hand, the potential inductive elements showing nonlinearity include nonlinear ferrite material [68], MEMS resonator [76]. The availability of multiple commercial-off-the-shelf (COTS) components exhibiting nonlinear capacitance has encouraged the design and fabrication of capacitive NLTL, which is one of the fundamental blocks of the proposed self-sustaining RF pulse generator. The voltage dependence of the capacitance $C(\mathrm{V})$ of the nonlinear capacitor is responsible for the nonlinear behavior exhibited by a capacitive transmission line. The propagation velocity (v_p) of an input pulse traveling across an NLTL is governed by the voltage dependence of the capacitance $C(\mathrm{V})$ of the nonlinear capacitor and can be stated by the following relationship [77].

$$v_\mathrm{p} = 1/\sqrt{LC(\mathrm{V})} \tag{4}$$

where L is the linear inductance, and $C(\mathrm{V})$ is the nonlinear capacitance. The capacitance of a nonlinear capacitor decreases as the voltage applied across it increases, thereby resulting in a faster propagation velocity of the traveling pulse. This phenomenon leads to points closer to the crest of the waveform, attaining faster propagation velocity compared to the rising edge of the waveform, thereby producing a steep shockwave front [57]. However, the ensuing reduction of the rise time of the output pulse is limited by the relaxation characteristics of the

dielectric material or dispersive properties of the lumped element transmission line [78]. Consequently, the output pulse propagates with a constant rise time irrespective of the number of sections once the minimum rise time is achieved. The reduction in pulse rise time (ΔT) caused by the *L*-*C* ladder sections can be stated by the following relationship [62].

$$\Delta T = t_{\mathrm{ri}} - t_{\mathrm{ro}} = \delta_1 - \delta_2 = n\left(\sqrt{LC}_{\mathrm{j0}} - \sqrt{LC(\mathrm{V_{max}})}\right) \tag{5}$$

where t_{ri} and t_{ro} represent the rise times of the input and output pulses respectively, n is the number of identical *L*-*C* sections in the NLTL, L is the linear inductance, δ_1 and δ_2 are the propagation delay times of the rising edge and peak of the input pulse respectively and C_{j0} and $C_{(\mathrm{Vmax})}$ represent the zero-bias capacitance, and the reduced saturated capacitance of the nonlinear capacitor respectively.

The rise time of the output pulse, t_{ro} can be expressed as $t_{\mathrm{ro}} = (t_{\mathrm{ri}} - \Delta T)$, where $t_{\mathrm{ri}} > \Delta T$. However, rise time reduction (ΔT) cannot be equal or greater than the rise time of the input pulse (t_{ri}) leading to an infinite steepness of the slope of the output pulse. Therefore, the rise time reduction of the output pulse is restricted by the rise time of the input pulse. The minimum rise time of an input pulse is defined by the cutoff frequency of the NLTL, which is an *L*-*C* ladder network that can be viewed as a cascaded low-pass filter arranged in π configuration. As with any other low pass filter, an NLTL has a cutoff frequency which is known as Bragg frequency. The Bragg frequency of an NLTL can be defined as follows [79]:

$$f_{\mathrm{c}} = 1/\pi\sqrt{LC(V_{\mathrm{max}})} \tag{6}$$

As the propagating pulse cannot be further sharpened by the remaining sections of the nonlinear transmission line, it breaks down into a stream of high-frequency oscillations with a narrow width, known as solitons. The frequency of the oscillation is close to Bragg frequency

[25] and the shape of the oscillation remains unaltered throughout the entire propagation path. To that end, equation (X) can be rearranged as follows [78].

$$\Delta T = n\left(1-\sqrt{k}\right)\left(\sqrt{LC}_{\mathrm{j0}}\right) \approx \pi\left(\sqrt{LC}(V_{max}\right) = \pi\sqrt{k}\left(\sqrt{LC}_{\mathrm{j0}}\right) \tag{7}$$

where k = $C_{(\mathrm{Vmax})}/C_{\mathrm{jo}}$ <1 and known as the nonlinearity factor. Manipulating equation (4), *K* can be isolated and expressed as follows [78].

$$K = \left(\frac{n}{n+\pi}\right)^2 \tag{8}$$

Equation (5) implies that for a large number of sections in the *L*-*C* ladder network ($n\rightarrow\infty$), the nonlinearity factor approaches unity, thereby capacitors with relatively weak nonlinearity can be used to generate solitons. In addition, for a fixed length of a nonlinear transmission line, dispersion tends to decrease with increasing section count [78], thereby the required delicate balance between dispersion and nonlinearity can be established using weak nonlinearity. Renowned mathematicians Diederik Korteweg and Gustav de Vries proposed the mathematical modeling of a discrete soliton wave in 1895 in the form of a third-order nonlinear partial differential equation, known as KDV equation, as follows [80].

$$\frac{\partial u}{\partial t} + 6u\frac{\partial u}{\partial x} + \frac{\partial^3 u}{\partial x^3} = 0 \tag{9}$$

For a waveform with a fixed shape like soliton and traveling at a speed *v* to the right side of the x-axis ($u=f(x-vt)$), this equation reduces to an ordinary differential equation (ODE) with a solution as given below [80]:

$$u(x,t) = \frac{v}{2}\mathrm{sech}^2\left[\frac{\sqrt{v}}{2}(x-vt-x_0)\right] = a\ \mathrm{sech}^2[b(x-vt-x_0)] \tag{10}$$

where v and x_0 denote wave propagation velocity and initial wave position respectively. The constants a and b represent the amplitude and the inverse of the width of the soliton wave as a function of the propagation velocity (v) [80]. Understandably, waves with faster propagation velocity are associated with higher amplitude and shorter width. Therefore, a stream of solitons tends to feature pulses with gradually decreasing amplitudes and greater widths. The pulse sharpening and soliton formation phenomenon are illustrated in Fig. 8.

The voltage modulation depth (VMD) indicates the level of the DC component present in the soliton waveform. It can be defined as the average peak-to-trough voltage of consecutive three pulses starting from the first pulse in a soliton stream [69].

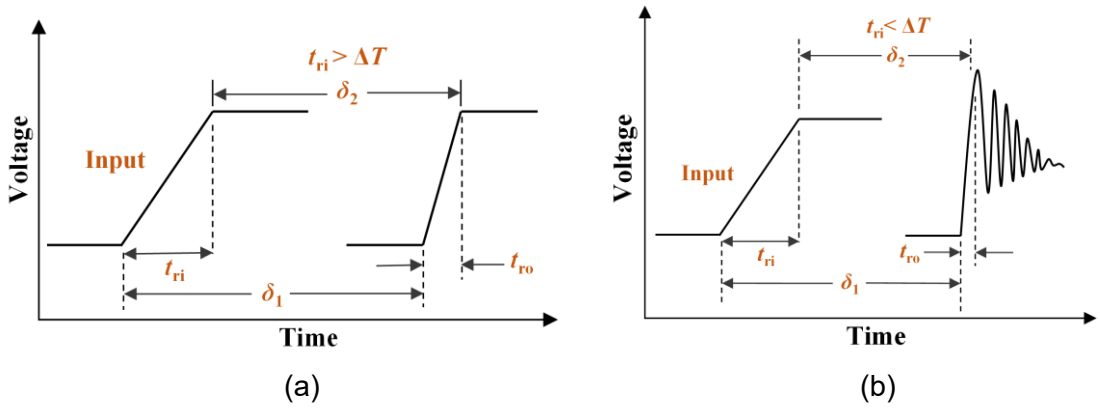


Fig. 8: (a) Pulse compression (b) Soliton formation

$$VMD = \frac{\sum_{j=1}^{3}(V_{\mathrm{pt}})_j}{3} \tag{11}$$

where j is the cycle number and V_{pt} is the voltage differential between the peak and trough of a pulse. VMD is taken into consideration to calculate the average RF power that can

be extracted from the generated soliton stream, and the expression of the average power is given by [69].

$$P_{\text{avg}} = \frac{\left(\frac{VMD}{2}\right)^2}{R_{\text{L}}} \tag{12}$$

where R_{L} is the output load and P_{avg} is the average RF power. The average RF power can be significantly lower than the peak instantaneous power related to solitons due to the underlying DC component and mismatched output load. Therefore, the characteristic impedance of an NLTL governs the selection of the output load or a matching network in between the NLTL and the load is needed to be designed for impedance matching. The characteristic impedance of an NLTL can be expressed as [62]:

$$Z_0 = \sqrt{\frac{L}{C(V)}} \tag{13}$$

CHAPTER 4

DESIGN OF A MEDIUM-POWER, SELF-SUSTAINING CONFIGURABLE SOLITON GENERATION CIRCUIT USING NLTL IN OPEN AND CLOSED LOOP CONFIGURATIONS

As opposed to the traditional method of generating continuous solitons, using an input pulse stream, a unique switching approach to generate continuous high-power solitons from a single input pulse is proposed and devised in this work. To this end, a Schottky diode-based sixteen-stage NLTL, an LDMOS based power amplifier with matching networks, and a custom GaNFET based high-voltage pulse generator has been combined to produce self-sustaining solitons from a single input pulse. The capability advantage of the closed-loop system is its stability and center frequency tunability; pragmatically, the solid-state-based design of this system enhances its probability of fielded use due to volume and mass savings compared to the prior-art. In [57], the authors have proposed a low-power soliton oscillator, which can amplify ambient noise and produce sustaining low-power solitons. However, the peak amplitude of the generated solitons was limited to 10 V, thereby limiting its practical use in most RF applications. In contrast, the solution demonstrated in this work can be a viable approach to generate self-sustaining solitons for medium-power RF applications in a compact package.

4.1 Design Procedure of the Self-Sustaining Soliton Generator

The validity of the design proposed in this work has been empirically shown by a 16-section NLTL coupled with a solid-state laterally-diffused metal-oxide-semiconductor (LDMOS) based power amplifier (PA), and a custom HV pulse generator. The closed-loop configuration constructed from these components demonstrated a peak power of 2.1 kW into

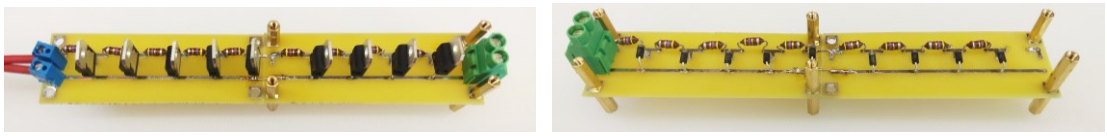
50 Ω at 90 MHz. This is the first report of a solid-state switch-based closed-loop NLTL configuration capable of producing a continuous pulse stream. The key design components of the implemented self-sustaining soliton generator are discussed at length below.

4.1.1 Capacitive NLTL

Nonlinearity in a capacitive NLTL can be introduced by nonlinear components that are predominantly made of ferroelectric dielectric [58]. Several commercially available ceramic capacitors are constructed from ferroelectric materials, thereby exhibiting capacitance nonlinearity when subjected to voltage variation. However, the performance of NLTLs assembled from this type of ceramic capacitors can considerably suffer from dielectric losses of ferroelectric materials. On top of that, the nonlinearity of the ceramic capacitors relies significantly on the Curie temperature of the ferroelectric material. Maximum nonlinearity can be achieved if the operating temperature is in the vicinity of the Curie temperature of the material. To compound the effects of the temperature dependence and dielectric loss of the ceramic capacitor on the performance of an NLTL, aging also has an adverse impact on the capacitance ratio which directly affects the performance of the NLTL [58]. Commercial semiconductor devices (e.g., Schottky diode, varactor, heterostructure barrier varactor, etc.) that exhibit nonlinear junction capacitance under the influence of reverse bias are reported in several studies as the nonlinear component in an NLTL [81]–[84]. The nonlinear junction capacitance is formed at the *p*-*n* junction at the depletion region of a diode when subjected to reverse bias voltage. The nonlinearity of the depletion layer junction capacitance can be expressed as follows [83].

$$C(V) = \frac{C_{j0}}{\left(1 + \frac{V}{V_J}\right)^n} \tag{14}$$

where V is the applied voltage, V_J is the junction voltage, n is a device doping-related coefficient, C_{jo} is the unbiased capacitance and C(V) is the nonlinear junction capacitance. The performance of an NLTL constructed using this type of nonlinear diodes is predominantly governed by their reverse breakdown voltage and capacitance ratio. As opposed to the ceramic capacitors, the operating temperature does not influence the nonlinear behavior of these diodes. Therefore, semiconductor diodes can be used to construct an NLTL whose performance is not affected by temperature variation. We have identified a wide range of commercial off-the-shelf (COTS) components displaying nonlinear capacitance including Schottky diodes, varactors, ceramic capacitors, etc. Through-hole Schottky diodes from STMicroelectronics (STPSC2H12D), varactors from ON Semiconductor (MBR1100RLG) were used to construct the initial NLTL prototypes, each containing nine sections. The preliminary NLTL prototypes are shown in Fig. 9.

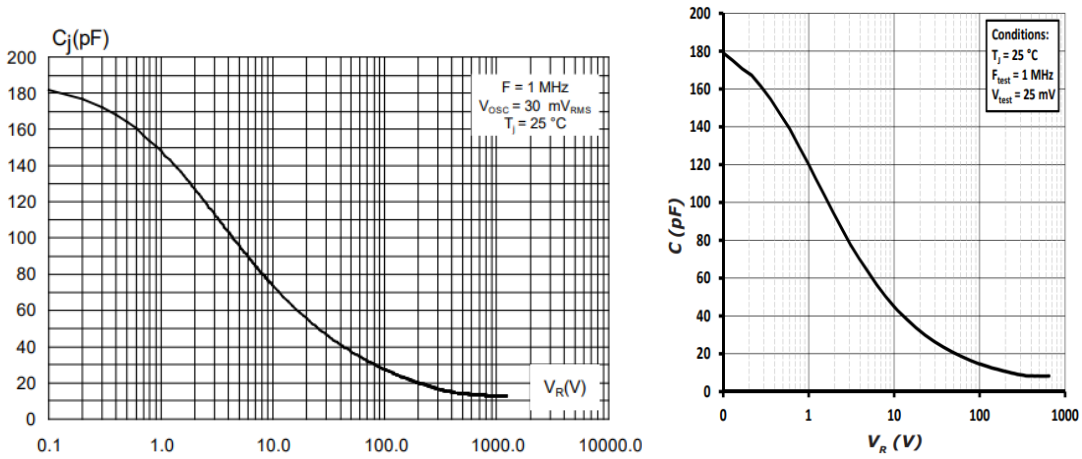


(a) (b)

Fig. 9: (a) Schottky diode based 9-section NLTL (b) Varactor based 9-section NLTL

Both these diodes were primarily selected because of their nonlinear *C*-*V* characteristics that are suitable for a capacitive NLTL. The capacitance of the 100V rated varactor undergoes a change from 150 pF to 20 pF with an applied reverse bias ranging from 0V to 100 V. The junction capacitance of a reverse-biased STPSC2H12D diode reduces to 10 pF at 1000 V from

a zero-bias capacitance of around 180 pF [85]. 600V rated Schottky diode from CREE (C3D02060F) is another potential candidate exhibiting nonlinear capacitance when subjected to reverse bias [86]. The junction capacitance of this diode undergoes a change from 180 pF to 10 pF over a voltage span of 0 V to 1000 V. The *C-V* characteristics curves of the aforementioned diodes are shown in Fig. 10 [85], [86].

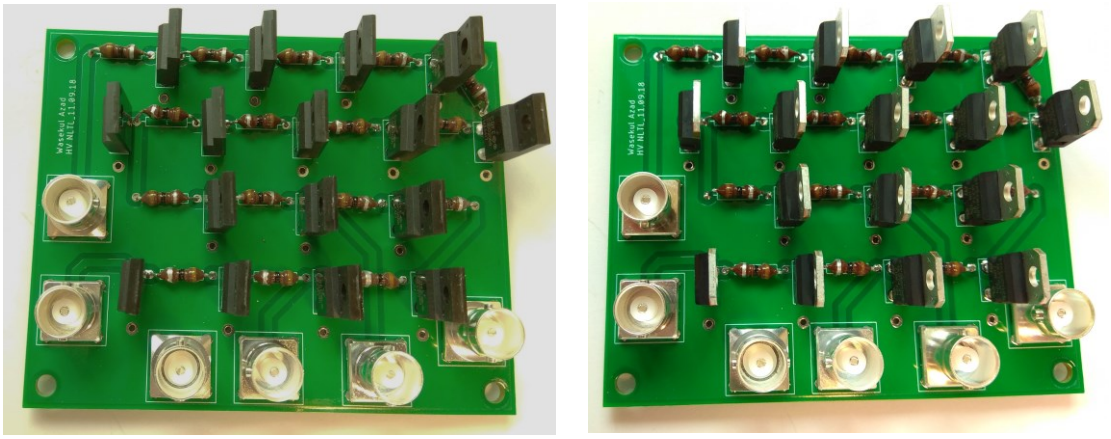


(a) (b)

Fig. 10: *C-V* characteristic curves obtained from datasheet of (a) STPSC2H12D [31] (b) C3D02060F [85], [86]

Two compact 16-section NLTLs were constructed from the chosen high-voltage Schottky diodes (STPSC2H12D, C3D02060F), and 50 nH fixed inductors [79]. BNC connectors were soldered to multiple sections of the NLTL to provide interconnection flexibility between the power amplifier (PA) and the NLTL. This arrangement facilitates the capability to apply an input RF signal from a pulse generator to different sections of an NLTL using the incorporated BNC interfaces between the pulse generator and the NLTL, thereby changing the effective length of the NLTL. This feature can influence the peak amplitude,

VMD, the center frequency of the generated RF signals, and the number of oscillations [74]. The fabricated capacitive NLTLs are shown in Fig. 11.



(a) (b)

Fig. 11: (a) 600 V rated Schottky diode based NLTL (b) 1200 V rated Schottky diode based NLTL

4.1.2 LDMOS Based RF Power Amplifier and RF Transformer Based Matching Networks

About 30 years ago, laterally diffused metal–oxide–semiconductor (LDMOS) transistors caught the attention of the research community as an alternative to bipolar transistors for base station applications [87]. Over time, LDMOS technology has been extended to a variety of RF applications, for instance, base station, broadcast, FM, VHF, UHF, industrial, scientific, medical (ISM), and radar to name a few [87]. The breakdown voltage of 200 V and higher, the capability to withstand a high voltage standing-wave ratio (VSWR) mismatch up to 65:1 at 65 V has enabled the LDMOS technology to excel in harsh in dustrial, scientific, and medical applications [88]. LDMOS is typically a three-terminal device whose *p*-type substrate accommodates *n*+ drain and source regions. The source region is connected to the *p*-type substrate and the source terminal by a laterally diffused, low resistance *p*+ sinker,

thereby allowing eutectic soldering to RF ground and minimizing wiring or lead parasitic. A thin layer of SiO_2 isolates the gate terminal of the LDMOS from its conducting channel. When an LDMOS is used as an amplifier, the gate signal is modulated with the input AC signal. A 1.4 kW rated LDMOS from AMPLEON (BLF188XR) was chosen to construct the power amplifier (PA) used in the proposed architecture. The LDMOS is rated for a maximum drain-source voltage of 135 V and a drain cut-off current of 77A with an operating frequency ranging from HF to 600 MHz [89]. Class-AB topology was adopted as the preferred LDMOS based amplifier topology as it combines the low distortion feature of Class-A and superior efficiency of Class-B type amplifiers. A 12 V power supply and a multi-turn potentiometer was used to bias the LDMOS at a voltage level close to 1.5 V. A zener diode was placed across the power supply for regulation purposes along with safeguarding the gate terminal of the LDMOS from unexpected transient voltages and EMI. The schematic of the PA with matching networks is illustrated in Fig. 12.

Matching networks placed in between the NLTL and the PA can maximize the power transfer from the amplifier and minimize back and forth reflections between the NLTL and the PA by matching the impedance of the NLTL to the impedance of the PA. That being said, the impedance of an NLTL varies with the voltage-dependent nonlinear capacitance as expressed in (10). In addition, solitons generated from different sections of the fabricated NLTLs may have different center frequencies. Therefore, a matching network placed between the NLTL and the PA featuring a combination of dynamic impedance and wide bandwidth can maximize power transfer and minimize reflections. Matching networks can be constructed from passive

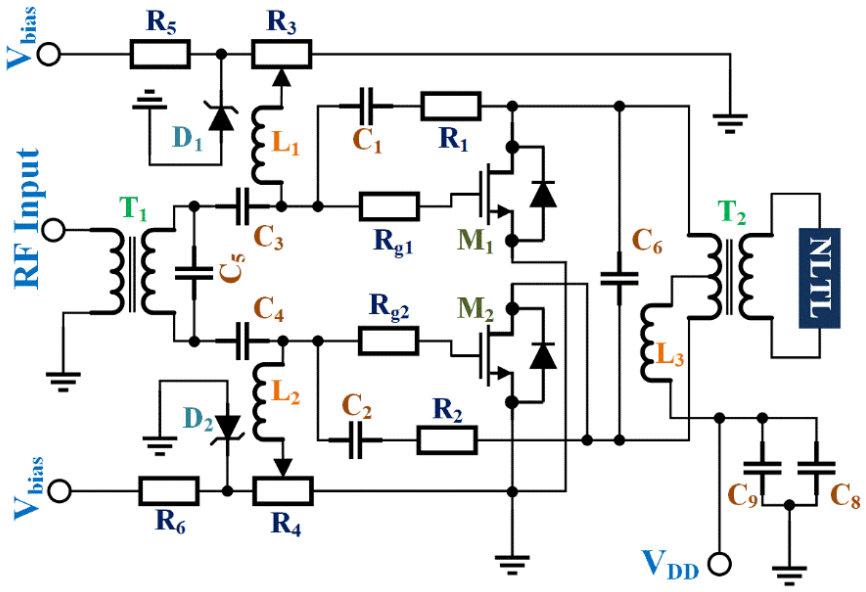


Fig. 12: Schematic of the power amplifier with matching networks

lumped elements, microstrip transmission lines, or RF transformers [90]. However, passive lumped element and microstrip transmission line-based matching networks typically offer narrower bandwidth compared to their RF transformer counterpart. Frequency dependency of some passive components (e.g., capacitors, inductors) and geometric limitation of transmission lines contribute to the narrowing of the bandwidth. Therefore, we have opted for RF transformer-based matching networks to achieve greater bandwidth. Type-61 (NiZn) ferrite core was chosen as the preferred core material to construct broadband RF transformers based matching networks thanks to its superior permeability compared to other ferrite core materials (e.g., MnZn ferrites) at the lower cutoff frequency. The high permeability of the selected type-61 core allows a lower number of required turns that minimizes leakage inductance and improves the bandwidth of the RF transformers [91]. An RF transformer (T_2) with a turn ratio of 1:4 was constructed for the output matching network of the PA using type-61 ferrite toroid cores which effectively transforms the output impedance of the LDMOS from 2.74 Ω [92] to

close to 43 Ω. At a reverse bias voltage of 100 V, the nonlinear capacitance of the 1200 V rated Schottky diode-based NLTL reduces close to 30 pF [85], thereby resulting in a characteristic impedance close to 41 Ω calculated using (4). Therefore, the output matching section of the PA closely matches the output impedance of the LDMOS to that of the NLTL. Another RF transformer (T_1) was used to form the input matching network of the PA. The turns ratio of the transformer was 4:1, which transforms the input impedance of the LDMOS (2.94 Ω) [92] to close to the impedance of the source of the RF input pulse. In closed-loop configuration, the last stage of the 16-stage NLTL is connected to the input of the PA, thereby acting as the RF input pulse trigger. Both the transformers of the PA have binocular type cores. Three RF transformers having binocular cores were constructed from Teflon insulated wire, co-axial cable, and semi-rigid coaxial cable respectively, and are shown in Fig. 13. Two metal tubes are connected by a piece of copper at one end to form a one-turn primary winding of these transformers. The secondary windings of thee three RF transformers were constructed by threading Teflon insulated wire, coaxial cable, and semi-rigid coaxial cable inside the metal tubes. To improve the bandwidth of the PA, the metal tubes of the RF transformers shown in Fig. 13(a) and 13(b) were surrounded by type-61 ferrite sleeves or toroids which are characterized by their low loss, high saturation flux density, and wide bandwidth [93]. The RF transformer depicted in Fig. 13(a) was used as the transformer denoted by T_1 in Fig. 12 as a part of the input matching network of the PA. Fig. 13(b) and 13(c) illustrate two in-house RF transformers either of which can be used as the transformer denoted by T_2 in Fig. 12 as a part of the output matching network. That said, the transformer shown in Fig. 13(b) exhibits better

(a) (b) (c)

Fig. 13: (a) Teflon insulated wire based RF transformer (T_1) (b) RG-328 coaxial cable based RF transformer (T_2) (c) Semi rigid coaxial cable based RF transformer (T_2)

performance in terms of bandwidth, thereby selected as the RF transformer (T_2) for the output matching network of the PA.

The matching networks of the PA minimize reflections from the NLTL and preserve the input signal fidelity. A 40-dB attenuator was used to safeguard the PA from overvoltage by connecting it before the input matching network of the PA. The LDMOS was mounted on a copper heat spreader which was at the ground potential for heat dissipation. Silicone paste (tye-120) was applied at the interface between the source pad and the copper heat spreader to lower the thermal resistance. The thermal management was further improved by attaching the heat spreader to a large Aluminum heatsink. The PA coupled with the matching networks incorporating the input (T_1) and output (T_2) RF transformers is shown in Fig. 14.

4.1.3 High-Voltage Pulse Generator

The amplitude and the frequency of solitons generated from an NLTL are substantially influenced by the peak amplitude and rise and fall times of the input pulse. The peak amplitude, thereby peak power of solitons proportionally increases with the amplitude of the input pulse. Pulse generators capable of producing pulses with peak amplitude in the range of kVs are commercially available. That being said, these commercial pulse generators are typically

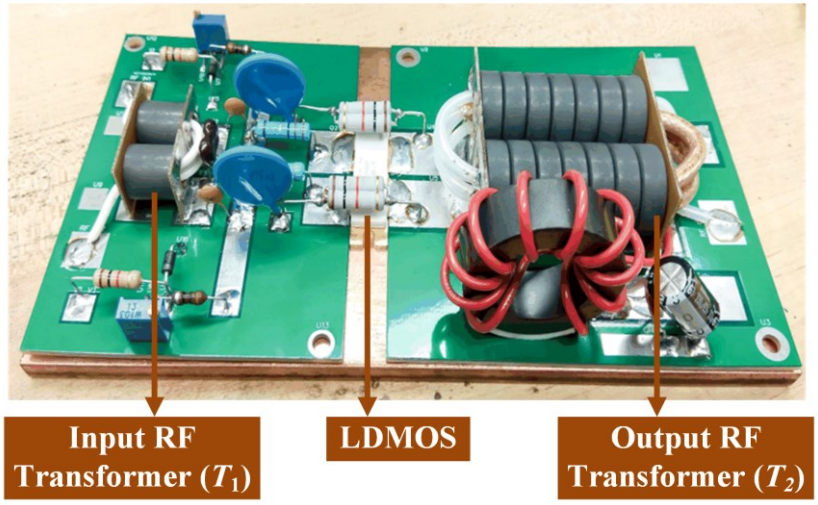


Fig. 14: LDMOS based power amplifier (PA) with matching networks

equipped with various thermal and safety management features to cater to a wide range of applications at the expense of being expensive and bulky. In this work, compact pulse generators, which are capable of providing HV pulses with adjustable pulse width, and fast rise and fall times to the NLTL have been designed and fabricated. The initial two prototypes of the HV pulse generator were constructed from 1000V rated Si MOSFET (FQA8N100C), half-bridge gate driver (IRS2104), and low-side gate driver (MIC4421). The prototypes were able to generate rectangular pulses with a width close to 750 ns at full width at half maximum (FWHM) and rise time close to 50 ns. The next iteration of the custom HV pulse generator was designed using GaN devices offering superior efficiency and performance compared to their Si counterparts in both hard-switched and soft-switched circuits in terms of lower gate charge, lower crossover loss, and smaller reverse recovery charge [94], [95]. A 650 V GaNFET (TPH3206PSB) made by Transphorm was used as the switching device in the third pulse generator prototype. The gate charge (Q_g) and the body-diode reverse recovery charge (Q_{rr}) of the selected GaNFET are 6.2 nC and 52 nC respectively which are relatively lower compared

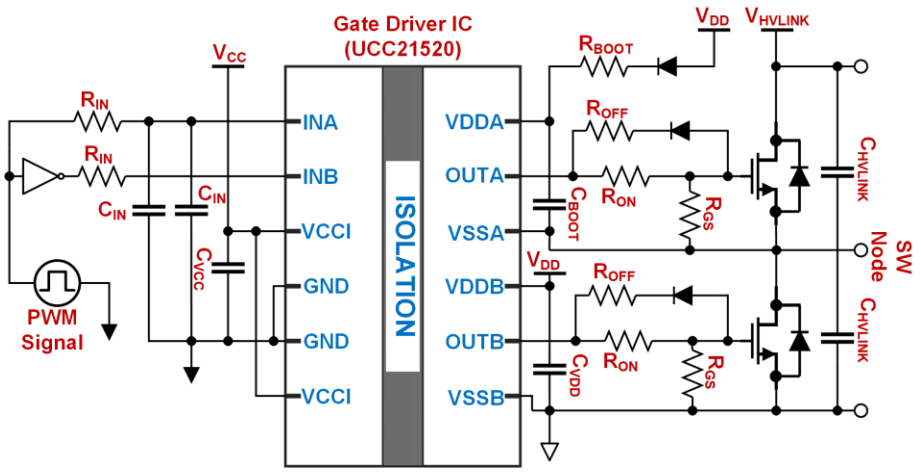


Fig. 15: Schematic of the GaNFET based in-house pulse generator

to the Si MOSFETs with similar voltage breakdown rating. This low gate charge requirement of the chosen GaNFET enables extremely fast switching speed and excellent reverse-recovery performance. That being said, the accompanying high di/dt transient during switching of a high-side GaNFET in a half-bridge configuration can lead to false turn-ON of the low-side GaNFET caused by the Miller effect leading to a shoot-through condition [96]. In addition, external parasitic inductance that can be attributed to non-optimal PCB layout can introduce sustained oscillations in the gate-drive signals. A large ground plane, gate ferrite beads (MMZ1608Q121BTA00), and switching node RC snubbers have been incorporated in the PCB prototype of the pulse generator to minimize the ringing in the gate-drive signals. An isolated half-bridge gate driver with reinforced isolation of 5.7 kV and capable of handling a switching frequency up to 5 MHz was selected to drive the GaNFETs in this custom HV pulse generator. The schematic and the prototype of this HV pulse generator are shown in Fig. 15 and Fig. 16 respectively. The pulse generator was able to generate pulses with rise and fall times close to

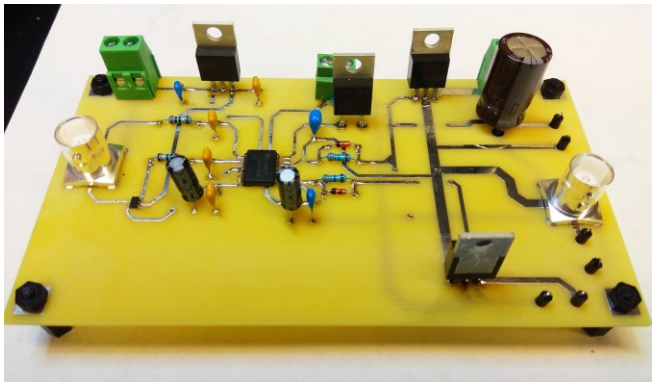


Fig. 16: Fabricated prototype of the UCC21520 based in-house pulse generator

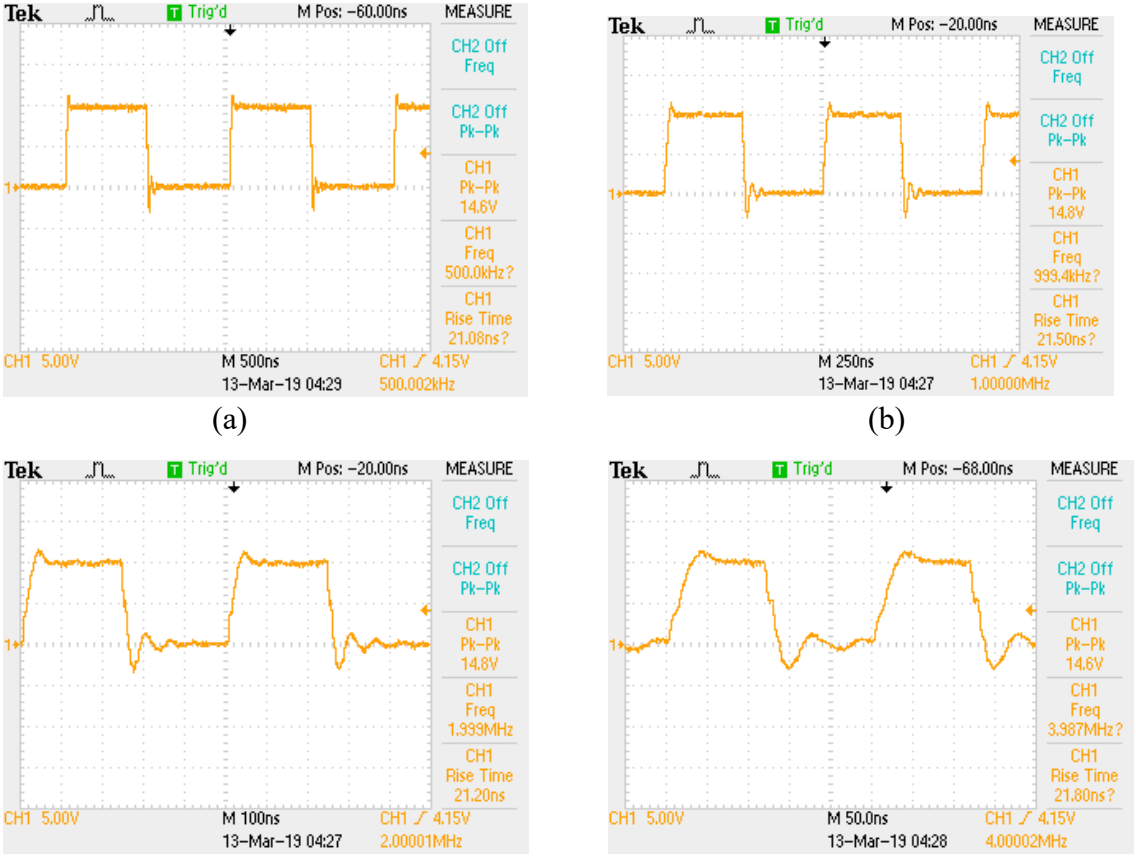


Fig. 17: Output pulses from the in-house pulse generator with (a) 1000 ns pulse width (b) 500 ns pulse width (c) 250 ns pulse width (d) 100 ns pulse width

20 ns and width close to 100 ns at FWHM. Fig. 17 shows the output pulses generated from this

GaNFET based pulse generator across a 50 Ω resistive load at different switching frequencies.

4.2 Simulation Results

This section presents results obtained from simulating a 32-section NLTL in LTSpice. The configuration of the building block (*L*-*C* section) of the simulated NLTL replicates the building block of the 16-section NLTL used in experiments. The higher number of sections is responsible for the heightened variation in frequency, VMD, and peak amplitude of soliton as it propagates along the line. The schematic of the NLTL with 32-sections is shown in Fig. 18.

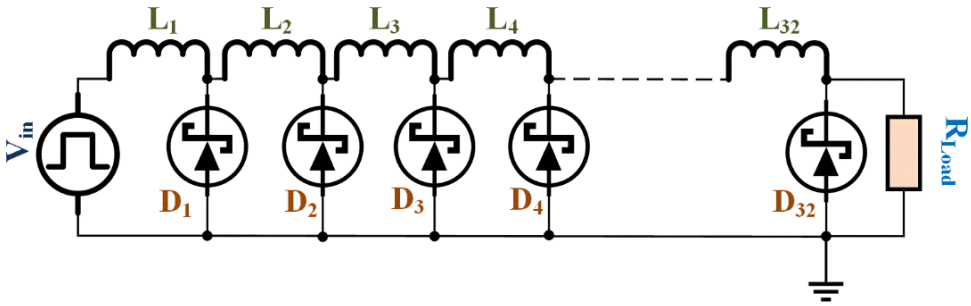


Fig. 18: Schematic of the 32-section NLTL

In this work, the spice model of the 1200V rated Schottky diode (STPSC2H12D) and a 400 nH fixed inductor in the NLTL model have been used in LTSpice simulations. A 2 kV rectangular 150 ns pulse with a rise time of 20 ns was applied as the input excitation of the NLTL. Fig. 19 highlights the increasing trend of the peak amplitude and VMD of the solitons as they propagate towards the end of the line. Therefore, increasing the section count of an NLTL can potentially increases the peak power of the solitons.

The 600 V and 1200 V rated Schottky diode-based open loop NLTL (16 section) configurations are simulated in LTSpice. The peak amplitude and the width of the applied input pulse were 250 mV (peak-peak) and 50 ns respectively. The simulated peak amplitude and

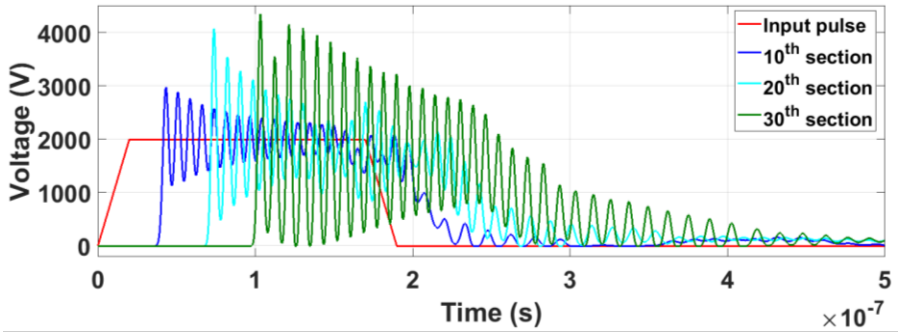
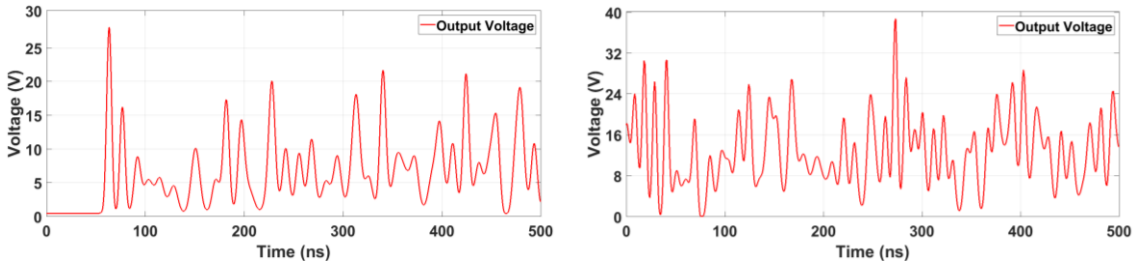


Fig. 19: Solitons generated at different sections of the single-diode NLTL

center frequency of the generated RF signal obtained from the 1200 V rated Schottky diode-based NLTL are 38 V and 100 MHz respectively. The peak amplitude and center frequency values of the simulated RF output signals associated with the 600 V rated Schottky diode-based NLTL are 28 V and 85 MHz respectively. The simulation results are shown in Fig. 20.

Followed by the simulation of the open-loop configuration, the 1200 V rated Schottky

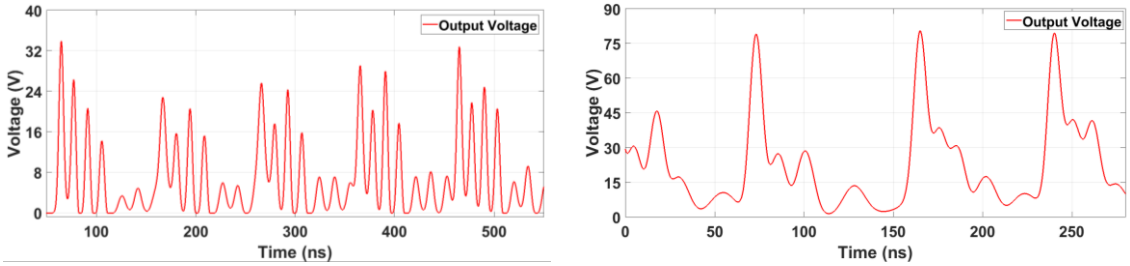


(a) (b)

Fig. 20: Simulated output from (a) 600 V rated Schottky diode based NLTL (V_{DD} = 10 V) (b) 1200 V rated Schottky diode based NLTL (V_{DD} = 10 V)

diode-based NLTL was simulated in a closed-loop configuration. The DC bias supply of the LDMOS was varied from 10 V to 30 V and the peak-peak voltage of the single input pulse was varied from 5 V to 7 V to measure the changes in the peak amplitude and center frequency of the generated solitons across the 50 Ω load connected to the 14th section of the NLTL. The

simulation results are shown in Fig. 21. The RF output signal shown in Fig. 21(b) demonstrates a peak amplitude close to 80 V and a center frequency close to 110 MHz.



(a) (b)

Fig. 21: Simulated output across (a) 14th section of the 1200 V rated Schottky diode based NLTL (V_{DD} = 10 V) (b) 14th section of the 1200 V Schottky diode based NLTL (V_{DD} = 30 V)

On top of that, this figure showcases the generation of continuous stream of output RF pulses, thereby validating the proposed concept of self-sustaining soliton generator using a closed-loop configuration. To increase the peak voltage of the output RF signals, the DC bias supply of the LDMOS of the PA was increased to 40 V and the custom pulse generator was incorporated in the closed-loop configuration to generate an input pulse with an increased peak amplitude of 40 V. The input pulse was applied to the 6th section of the NLTL in the closed-loop configuration while keeping the rest of the connections (e.g., NLTL-PA, NLTL-load, etc.) unchanged. Fig. 22 demonstrates the simulation result exhibiting the generation of continuous RF signal with a peak amplitude close to 210 V and center frequency close to 95 MHz.

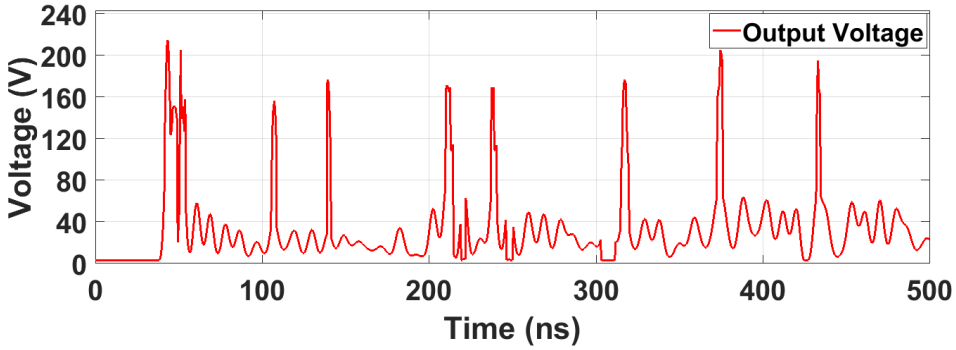


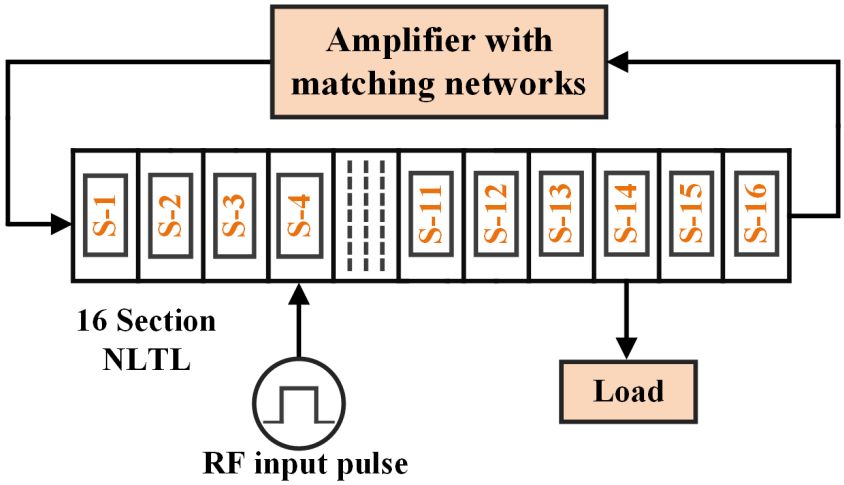
Fig. 22: Simulated output across the 11th section of the 1200 V rated Schottky diode based NLTL (fourth phase)

4.3 Experimental Setup and Results

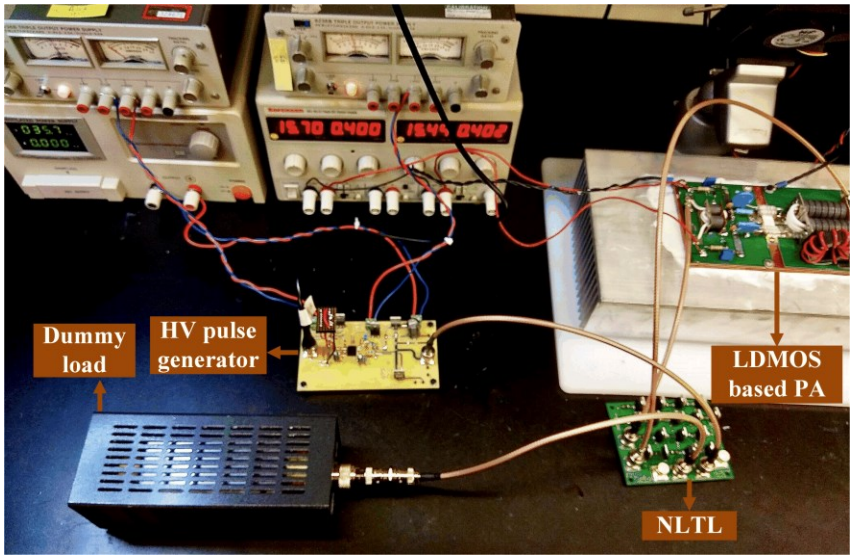
4.3.1 Experimental Setup

The research effort to generate self-sustaining solitons has four phases of design and test. The first phase is marked by the design and fabrication of the initial prototypes of multiple 9-section capacitive NLTLs. During the second phase, we have fabricated Schottky diode-based NLTLs comprised of 16-sectios and tested these NLTLs in open-loop configuration by connecting the 1st section of the fabricated NLTL to the output of the LDMOS based PA. A function generator was used to generate an external trapezoidal pulse with 250 mV amplitude (peak-peak), width of 50 ns, and rise and fall times of 8.9 ns. This pulse was applied to the input of the amplifier, and a resistive load of 50-Ω was connected to the 16th section of the NLTL. RG-328 coaxial cable was chosen for making connections between the NLTL, the PA and the load for its high voltage withstanding ability. An external cooling fan was used to aid the cooling of the LDMOS which was connected to a large Aluminum heatsink. A 50 V benchtop DC power supply was used as the DC bias source of the LDMOS.

The third phase featured experiments conducted in a closed-loop setup. The closed loop is formed by connecting the 1st and the 16th section of the NLTL to the output and the input of the PA, respectively. The input trapezoidal pulse with 250 mV amplitude (peak-peak), width of 50 ns, and rise and fall times of 8.9 ns from the function generator was applied to the 4th section of the NLTL. The 1.5 kW rated 50 Ω resistive load was connected either to the 11th section or the 14th section of the NLTL interchangeably to gauge the variation in peak output voltage and center frequency of the generated solitons. BNC connectors was used in the NLTL prototypes to form interfaces across six sections of the NLTL, and these interfaces facilitates applying input pulse or obtaining output pulse from multiple locations of the NLTL. This unique feature allows a user to change the effective length of the NLTL, thereby tune the peak amplitude, VMD and center frequency of the generated solitons that vary with the change of the length of the NLTL [43]. During the fourth phase, the custom in-house HV pulse generator was incorporated in the closed-loop configuration to increase the peak voltage and peak power of the generated RF signals. The pulse generator was biased to produce an input pulse with a peak amplitude of 40 V as opposed to the peak amplitude of 250 mV of the pulse generated from the function generator in the previous phases. The width and rise and fall times of the input pulse generated from the in-house pulse generator were close to 200 ns at FWHM and 20 ns respectively. The input pulse from the pulse generator was applied to the 6th section of the NLTL while the other connections (e.g., PA-NLTL, NLTL-load, etc.) remained unaltered. During all experiments, NLTLs with single-diode configuration have been used. Fig. 23(a), and Fig. 23(b) show the schematic diagram and the photograph of the NLTL-PA closed-loop setup respectively.



(a)

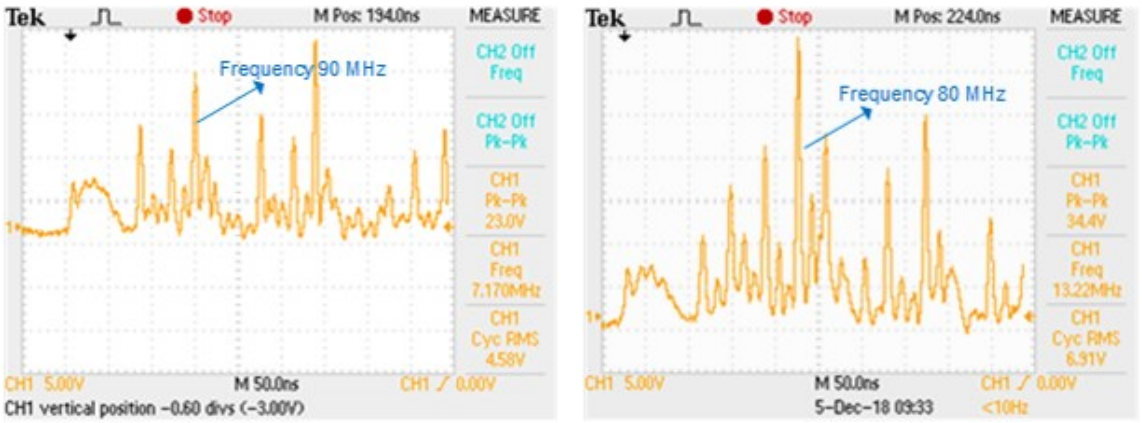


(b)

Fig. 23: (a) Simplified block diagram of the closed-loop setup of the NLTL and PA with excitation (b) Experimental setup of an NLTL-PA closed loop configuration

4.3.2 Experimental Results

The 600 V and 1200 V rated Schottky diode-based open-loop NLTL configurations produced solitons with center frequencies close to 80 MHz and 90 MHz as shown in Fig. 24. The 16-section NLTLs produced a stream of RF pulses with a peak amplitude close to 35 V, center frequency close to 90 MHz and a pulse width close to 10 ns at FWHM across the 50 Ω load connected to the 14th section of the NLTL. The peak amplitude and the width of the applied input pulse were 250 mV (peak-peak) and 50 ns respectively. The peak amplitude of the generated RF signal represents a 25 dB open-loop gain. The experimental results demonstrate good agreement with the simulation results in terms of peak amplitude and center frequency of the generated RF signal as showcased in Fig. 20.

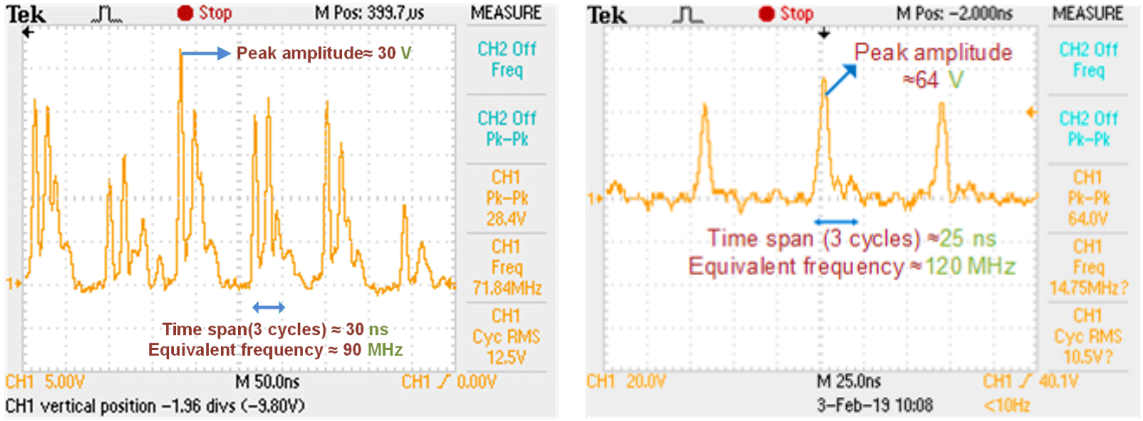


(a) (b)

Fig. 24: Output from (a) 600 V rated Schottky diode based NLTL (V_{DD} = 10 V) (b) 1200 V rated Schottky diode based NLTL (V_{DD} = 10 V)

Nonlinear characteristics of several commercial-off-the-shelf (COTS) components (e.g., Schottky diodes, varactors, X7R, Y5V type ceramic capacitor, etc.) have been exploited to fabricate NLTLs and empirically evaluate the performance of the nonlinear components. The 1200 V rated Schottky diode demonstrated maximum nonlinearity among the components

that had been identified as the potential nonlinear capacitive elements. Therefore, for the next stage of the experiment, a 16-section NLTL fabricated in-house from the 1200 V rated Schottky diodes has been utilized. During this phase of the experiment, the DC bias supply of the LDMOS was changed within a range of 10 V to 30 V to and the peak-peak voltage of the single input pulse was varied from 5 V to 7 V to measure the changes in the peak amplitude and center frequency of the generated solitons across the 50 Ω load connected to the 14th section of the NLTL. Fig. 25 shows the peak amplitude and the center frequency of the generated RF signals across the 50 Ω load connected to the 14th section of the 1200 V rated Schottky diode based NLTLs at different bias levels (V_{DD}=10V, 30 V). The output RF signal generated from the 1200 V rated Schottky diode based NLTL has a peak amplitude close to 64 V and a center frequency close to 120 MHz that corresponds to a voltage gain close to 19 dB. In addition, the RF signals generated from a single input are continuous which is the testament to the validity of the closed-loop configuration concept. The closed-loop configurations pertaining to the 1200 V rated Schottky diode have been simulated in LTSpice at identical



(a) (b)

Fig. 25: Output across (a) 14th section of the 1200 V rated Schottky diode based NLTL (V_{DD} = 10 V) (b) 14th section of the 1200 V Schottky diode based NLTL (V_{DD} = 30 V)

operating conditions and produced results that are quite similar to the experimental results as shown in Fig. 21.

During the fourth phase of the experiment, the DC bias supply of the LDMOS of the PA was increased to 40 V and the custom pulse generator was incorporated in the closed-loop configuration to generate an input pulse with an increased peak amplitude of 40 V. The input pulse was applied to the 6th section of the NLTL in the closed-loop configuration while keeping the rest of the connections (e.g., NLTL-PA, NLTL-load, etc.) unchanged. A continuous stream of RF pulses was recorded across the 50 Ω load connected to the 11th section of the NLTL with a peak amplitude and center frequency close to 178 V and 90 MHz, respectively as shown in Fig. 26 and similar to the simulation results shown in Fig. 22. The pulse width and the rise time of the generated output pulses were close to 6 ns at FWHM and 2 ns, respectively. The generated output RF pulse produces a peak power close to 2.1 kW across the 50 Ω resistive load.

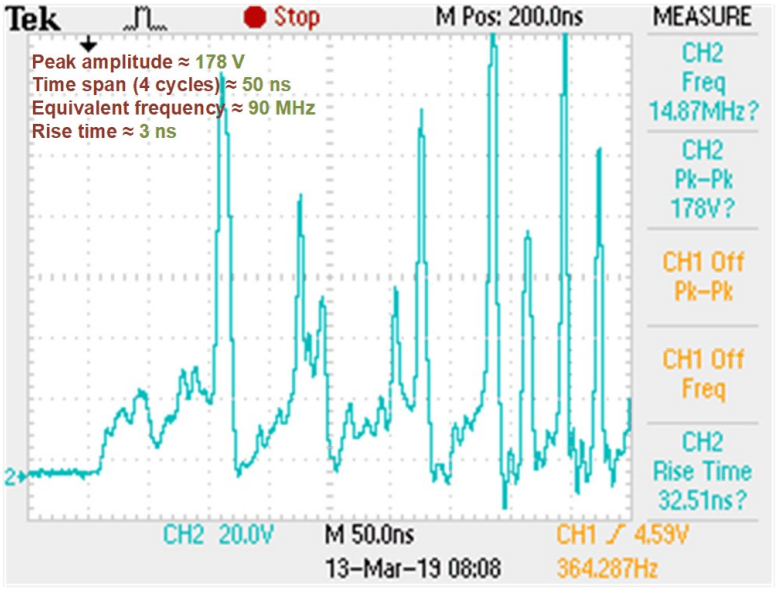


Fig. 26: Output across the 11th section of the 1200 V rated Schottky diode based NLTL coupled with UCC21520 based in-house pulse generator (V_{HVLINK}= 40 V, V_{DD} = 40 V, f = 2 MHz)

4.4 Discussion and Future Research Direction

4.4.1 Dual-diode NLTL Configuration

In this work, a dual-diode NLTL design has been proposed that can handle an input pulse with either positive or negative polarity and increase the center frequency of the solitons compared to the single-diode based NLTL with a similar number of sections. The schematic of the NLTL is illustrated in Fig. 27.

Each section of this NLTL features two series-connected diodes that are placed in such a way that one of them will be reverse-biased for input with any polarity and entire voltage stress will be equally shared between them. The simulation shows that this dual-diode NLTL generates solitons with higher center frequency (~180 MHz) compared to the single-diode NLTL (~120 MHz) under same operating condition and section count. However, the single-

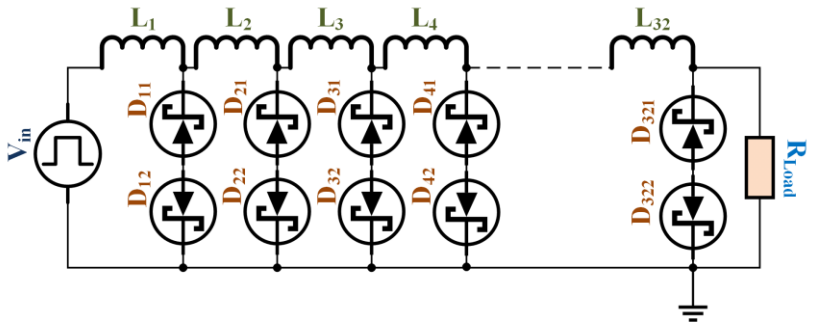
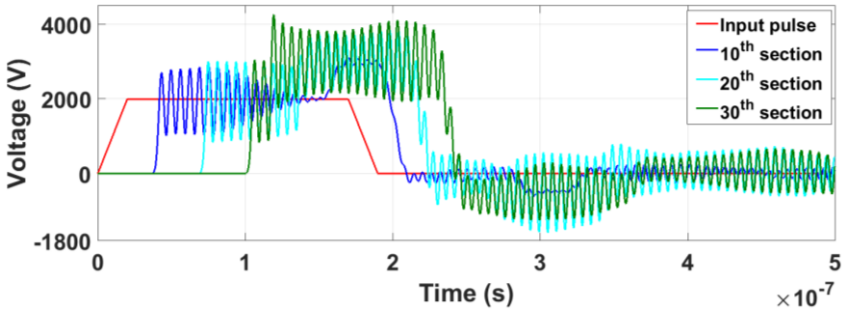


Fig. 27: Schematic of the 32-section dual-diode NLTL

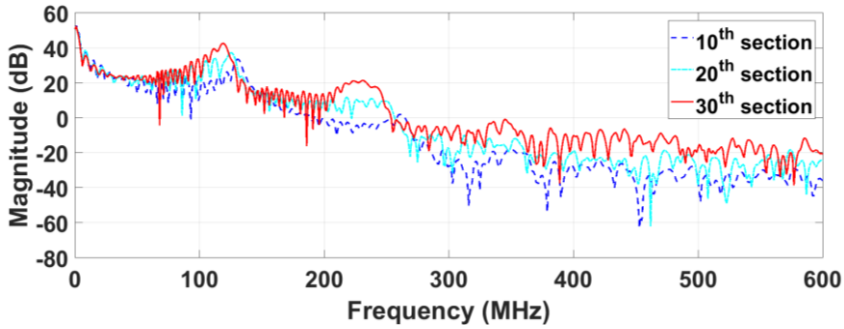
diode NLTL exhibits superior performance in terms of VMD and peak amplitude of the generated solitons. These findings from the simulations are shown in Fig. 28.

4.4.2 Increasing Peak Power and Center Frequency of Solitons

In addition to employing the dual-diode NLTL configuration, other feasible methods to increase the center frequency of the solitons include decreasing the rise time of the input pulse, decreasing the inductance, increasing the peak amplitude of the input pulse, etc [43]. The rise time of the input pulse can be reduced by incorporating faster SiC or GaN MOSFETs in the in-house pulse generator circuit. The peak amplitude of the input pulse generated by the in-house pulse generator can be increased by using MOSFETs with higher breakdown voltage rating and higher input DC supply voltage. To be compatible with the input pulse (solitons)



(a)



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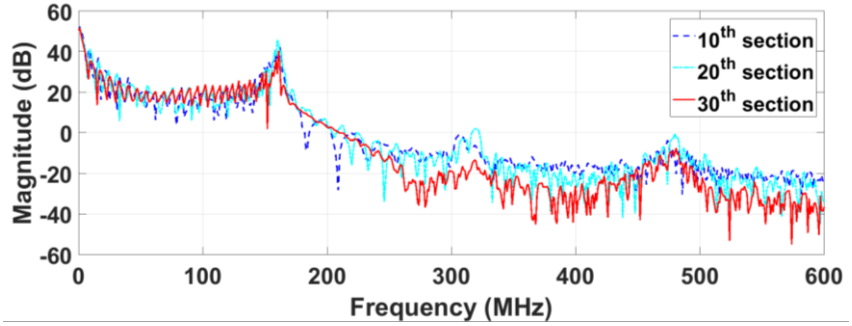


(c)

Fig. 28: (a) Solitons generated at different sections of the dual-diode NLTL (b) FFT of solitons generated from single-diode NLTL (c) FFT of solitons generated from dual-diode NLTL

with higher peak amplitude in addition to higher center frequency, the biasing voltage (V_{DD}) of the PA is required to be increased as well. Circuit inductance can be reduced by minimizing the trace length in the PCB.

4.5 Conclusion

This research presented a unique method of generating a continuous stream of medium-power RF signals from a closed-loop configuration made from of an NLTL, an LDMOS based PA with matching networks, and a custom HV pulse generator. A 1200 V rated Schottky diode with an impressive capacitance ratio close to 18:1 has been selected to build the NLTL for testing. An LDMOS based PA with suitable broadband matching networks was constructed to continue the propagation of RF signals generated from an NLTL while mitigating reflection at the NLTL-PA interface. Three custom HV pulse generators were designed and fabricated in smaller footprints compared to the commercial pulse generators. Multiple signal interfaces were formed by connecting the pulse generator and the PA at different locations of the NLTL, and this feature facilitates the necessary tuning capacity to control the peak amplitude, VMD, and center frequency of the RF signals. A dual-diode based NLTL design has been proposed and simulation results have been presented exhibiting an increase in the center frequency of the generated RF signal compared to a single-diode based NLTL. This research work also provides guidance for the future researchers to further improve the proposed design.

CHAPTER 5

SERIES-CONNECTED MOSFET BASED HIGH-VOLTAGE, HIGH-SPEED SOLID-STATE SWITCH

5.1 Motivation

High-voltage pulses associated with short duration exert a profound impact on a wide variety of applications including but not limited to military, medical, industrial, plasma deposition systems, food processing, etc. A widespread moniker pertaining to these short-duration pulses is pulsed power. This term alludes to a broader concept of accumulating charge over a relatively long period and dumping the stored charge over a shorter period, thus producing an extremely high instantaneous power. The energy is stored within an electrostatic field (capacitor), or electromagnetic field (inductor), or as chemical energy in the form of high-current lead-acid batteries. The energy or the stored charge can be discharged into a load using a simple closing switch or by exploiting a sophisticated periodically pulsed, relativistic magnetron. Pulsed power systems rose to prominence from relative obscurity and grabbed the attention of the whole world during World War II by empowering the radar system requiring short bursts of high-power pulses at that time. Henceforth, the application of pulsed power has been extended manifold encompassing a wide portion of the military, medical, industrial fields, such as electromagnetic launchers, cell membrane electroporation, cancer therapy, particle accelerators, food processing, waste water treatment, concrete recycling, to name a few.

The biomedical sector has experienced an uptick in the usage of the short high-power pulse over the past few decades. Longer pulses with moderate power have been traditionally used for the cellular membrane electropermeabilization effect to take place. Deposited energy in the cells during this effect is typically lower if nanosecond pulse is used compared to longer

pulses. The ramification is reduced tissue heating that mitigates potential health hazards. Further investigation of nanosecond pulses in the biomedical field revealed that the magnitude of the applied electric field plays a pivotal role in the programmed death of cancerous cells. This phenomenon implies that an intense localized field induced by high-power short nanosecond pulses can be effectively used to treat malignant tumors without significant tissue heating [97]. On top of that, the megavolt-per-meter electric strength associated with the high-power nanosecond pulses can set in motion a chain of intercellular events with positive outcomes, including but not limited to calcium bursts, the appearance of apoptotic indicators [97], [98]. Traditional method of electroporation involves applying a 100 V to 3500 V rated rectangular pulse with a width in the range of microseconds to a cellular suspension to porate the cellular membrane [99]. Recently, researchers have ventured forward with extremely short high-power pulses for electroporation with substantial success [100], [101].

Pulsed power techniques are extensively used in material processing in today's heavily semiconductor reliant world landscape. Plasma-based ion implantation, deposition, etching employ pulsed power techniques to devise cutting-edge technologies for surface treatment of complex shaped materials. Pulsed power leaves a profound impact on the fields of material ablation, annealing, new material synthesizing, etc. Pulsed power technology is also being used in recycling concrete scrap, ignition, and combustion of fuel-air mixture extensively.

One of the most critical components of a pulsed power system is a switch that transfers the stored energy to the load. Spark gap switches have been the stalwarts in this aspect of the pulsed power system. A Marx generator-based pulsed power system developed by the Physics International Company in 1964 employed a liquid spark gap to discharge a liquid dielectric

transmission line to the load. Spark gaps can switch a relatively high level of current and can withstand high voltage levels, both of which are quintessential features of the switching element of a pulsed power system. That being said, spark gap switches suffer from shot-to-shot timing instability (jitter), thereby elevating the level of difficulty to ensure accurate timing and synchronization for particular application requirements. The considerable jitter stems from the stochastic process that drives the actual breakdown procedure of a spark gap [102]. In addition, spark gap switches suffer from a short lifetime, and they are not compatible with high repetition frequency. On the flip side, solid-state semiconductor switches (e.g., MOSFETs, IGBTs, etc.) are devoid of these aforementioned drawbacks associated with the spark gap switches. With the rapid advancement of wide-bandgap (WBG) semiconductor devices, applications of power electronics have increased manifold. WBG material (e.g., SiC, GaN) based semiconductor devices (e.g., MOSFET, IGBT, etc.) undeniably edges the traditional Si-based semiconductor devices in some key performance metrics including but not limited to dielectric field strength, breakdown voltage, thermal reliability at high temperature, form factor [103]. Low conduction loss (due to low ON-resistance), low switching loss (due to low gate charge) of WBG devices enable higher switching speed, and lead to a diminished requirement of thermal management compared to Si devices, thereby increasing the power density of an entire system reliant on semiconductor devices. The typical junction temperature of SiC-based devices is close to 200 °C which is approximately 50 °C higher than the typical junction temperature of Si-based devices [104]. This property coupled with excellent thermal conductivity allows the SiC devices to reliably operate at a higher temperature without introducing significant performance de-rating as opposed to the Si devices.

MOSFETs, in general, are inherently faster compared to other types of semiconductor devices (e.g., IGBT, thyristor, etc.). Therefore, WBG MOSFETs are predominantly preferred in high-voltage and high-speed power electronics applications, such as high-voltage pulse generators, electric vehicle powertrain, industrial motor drives, X-ray machines, pulsed power systems, etc. Lower switching loss and lower ON-resistance of the GaN MOSFETs notwithstanding, the maximum breakdown voltage (900 V) of the commercial-off-the-shelf (COTS) GaNFETs is lower than that of the COTS SiC MOSFET (3300 V) [105], [106]. Therefore, SiC MOSFETs are preferable in high-voltage and high-speed power electronics applications as an alternative for Si devices.

Recent advancement in SiC technology is mirrored in the gradually increasing blocking voltage capability of COTS SiC MOSFETs as evidenced by the new generation of commercially available SiC MOSFETs with a voltage breakdown rating of 3.3 kV. Testing of some of the high-voltage (10-15 kV rated) SiC modules has been demonstrated in select research laboratories. [107], [108]. However, commercialization of these modules seemingly not forthcoming due to excessive manufacturing cost and design complexities. To date, a single manufactured based in Germany, named BEHLKE, is manufacturing high-voltage solid state switches commercially. However, the exorbitant price of the high-voltage switches manufactured by BEHLKE can put off a large section of potential customers. A 15 kV rated HV switch module from BEHLKE costs in the vicinity of $5000 which is too steep for widespread commercial use. On top of that, the switch itself is quite bulky, for instance a 15 kV rated HV switch made by BEHLKE occupies a footprint close to 4500 cm^3 that without

factoring in the liquid cooling pump required to facilitate the switch operation at a higher switching frequency (>10 kHz) [109]. A picture of a HV BEHLKE switch is shown in Fig. 29.

In addition, being a commodity made outside of the United States, the lead time of the

Fig. 29: A high-voltage solid-state switch from BEHLKE [109]

HV switches from BEHLKE is excruciatingly long, therefore hindering the production speed of any commercial products using these switches in the United States. To alleviate these aforementioned issues pertaining to the commercially available discrete MOSFETs and commercial HV products from BEHLKE, this research work courts alternate solution that can be viable from technical, financial, and commercial standpoint.

Series connection of multiple low-cost COTS SiC MOSFETs or multilevel converter topologies are two intriguing approaches to attain higher voltage blocking capability while taking the aforementioned issues related to commercial products into consideration. Notwithstanding the considerable advantages of the multilevel converter topologies in terms of low common-mode voltage, low dv/dt stress, and radiated electromagnetic interference to a lesser extent compared to the series-connected MOSFETs [110]–[112], features such as lesser

cost, relatively simpler construction, higher efficiency related to the series-connected MOSFET tip the scale in favor of this approach.

5.2 Fundamental Design Challenges of Series-Connected Solid-State Switch

Series connection of multiple low-cost COTS SiC MOSFETs is an intriguing cost-effective solution to the increasing demand for semiconductor devices with a high voltage blocking capability and high-speed compatibility. That being said, ensuring equal voltage stress across the MOSFETs in a series stack during the turn-OFF period (steady-state) and switching transients (dynamic state) is a major design challenge for researchers in this field.

Parameter variation of the switching devices, unsynchronized gate drive signals, non-optimized trace layout can lead to unequal voltage exposure across the series-connected MOSFETs in a stack. The unbalanced voltage distribution among the series-connected switches can subject single or multiple switches to overvoltage stress beyond their rated value resulting in the failure of these switches. This event can subsequently lead to cascaded failure of all the switches in the series stack, thereby leading to complete failure of the device which can be catastrophic. The failure mechanism is illustrated in Fig. 30. As shown in Fig. 30(a), ideally each series-connected MOSFET in a stack is anticipated to withstand equal voltage stress. However, in the absence of a well-designed voltage balancing scheme, one or multiple MOSFETs in the series stack can be subjected to a greater voltage stress compared to the rest of the MOSFETs in the stack. If this voltage stress exceeds the breakdown voltage rating of an individual MOSFET, it can inflict irreversible physical damage to the overstressed MOSFETs. As a cascading effect, the voltage distribution profile among the other healthy MOSFETs in the series stack is altered resulting in a voltage stress beyond the breakdown voltage rating of

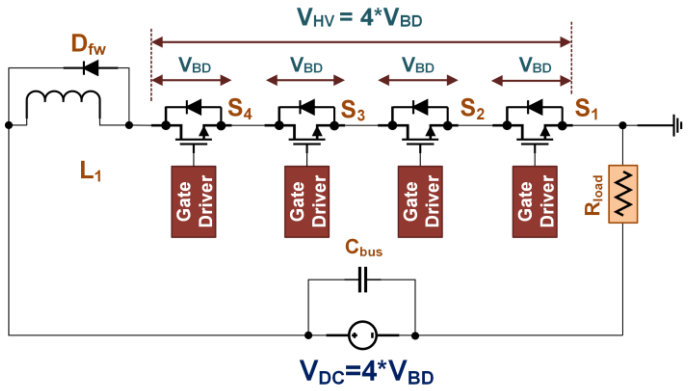
individual MOSFET, therefore causing a full-scale damage of the HV switch as illustrated in Fig. 30 (b) and (c).

To that end, mitigating the voltage imbalance issues pertaining to the series-connected switch is a major design consideration for the researchers working in this field.

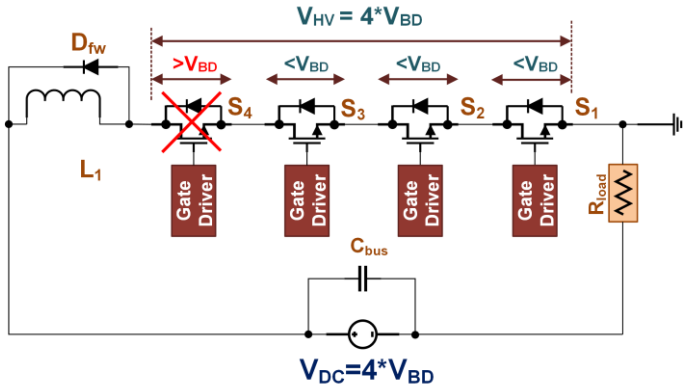
5.3 Existing Techniques to Mitigate Fundamental Design Challenges Associated with Series-Connected Solid-State Switch

Voltage balancing among series-connected switches entails design consideration for both steady-state and dynamic state voltage balancing. Steady state alludes to the phase when the series-connected switches remain in the cutoff region, thereby not allowing load current to pass through the HV switch. Conversely, dynamic state refers to the transients during the onset of the turn-ON and turn-OFF phases.

Steady-state voltage balancing can be attained by paralleling balancing resistors across each switch connected in series [103], [113]–[126]. However, there is a tradeoff between the level of voltage imbalance at steady-state and losses due to leakage current [123]. As opposed to the relatively simpler design process of voltage balancing during the steady-state, a more sophisticated approach is required to address the dynamic voltage balancing issues. Researchers, working in this field, have proposed a number of approaches as of now to address



(a)



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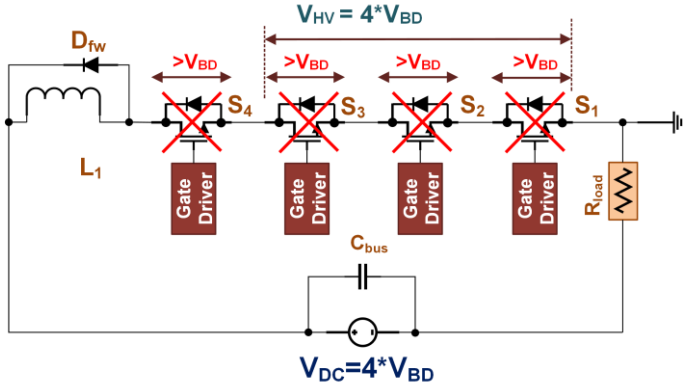


(c)

Fig. 30: Series-connected switch failure mechanism due to voltage imbalance (a) Ideal scenario (b) Beginning of the failure (c) Cascaded failure of the entire switch.

this issue with a certain amount of success. The techniques proposed to ensure voltage balancing during switching transients can be classified into two major categories, namely- load-side techniques [127]–[130], and gate-side techniques [131]–[135].

The load-side technique is largely reliant on the utilization of passive snubbers, which are among the simplest forms of voltage balancing schemes. In this scheme, snubber capacitors coupled with snubber resistors (*RC* snubber) and/or diodes (*RCD* snubber), are connected in parallel with individual power switches. The capacitances of the snubber capacitors are required to be at least five to ten times the output capacitances of the semiconductor switches [127] to effectively control the dynamic voltage imbalance at the expense of the increased amount of snubber power loss and extended commutation time of the switches. In [128], a *RCD* snubber was introduced in the dynamic voltage balancing scheme for a series-connected HV switch made from two 1.7 kV rated MOSFETs. A *RC* snubber was used in [130] to minimize the dynamic voltage imbalance of a developmental series-stacked HV switch. To address the fundamental problem of high snubber losses associated with a snubber scheme, a strategy has been proposed in [129] that involves the partial discharge of snubber capacitors during a switching cycle leading to reduced reset current surge and reduced power loss. However, one onboard power supply per switch is required in this proposed scheme, thereby increasing the footprint, and cost of the HV switch.

The active gate control method can be a feasible solution for the dynamic voltage balancing problems among the semiconductor switches in a series stack. This method involves manipulating the dynamic of operation of the switches in their active region and capitalizing on the relationship between the levels of the gate drive signal and the switching transient of

the devices. Active voltage clamping circuits proposed in [131], [136], and auxiliary circuits proposed in [132], [133] based on active gate control mechanism aim at controlling the dynamic voltage imbalance in a series stack of switches by feeding additional charges back to the gate terminal to marginally turn the switches ON at the onset of a voltage overshoot event. More sophisticated active gate control methods are demonstrated in [134], [135], [137], where feedback control is employed in the gate-drive loop to regulate the slew rate (*dv/dt*) of the devices connected in series with respect to carefully defined reference signals to control the voltage overshoot during switching transients. Another way to minimize voltage overshoot, thereby voltage imbalance in a series stack of switches caused by asynchronous gate signal delays during switching transients is to introduce controlled delays in the gate drive signals [115], [116]. The ingenuity of this approach lies in the fact that the switching speed of the HV switch remains the same while particular gate signals are slightly delayed by a precise amount to counteract the voltage overshoot pertaining to those switches. However, to ensure cycle-by-cycle control over the entire switch, feedback circuits and associated A/D conversion circuits are required in these methods [115], [121], [138], [139]. A considerable amount of time delay may incur on top of the feedback circuitry-controlled gate signal delays due to the delay in sensing and prolonged response time of the A/D conversion circuits. This may curb the high-speed switching capability of SiC MOSFETs, thereby nullifying the advantages associated with WBG devices, and leading to excessive voltage imbalance during initial switching cycles that put the entire switch at risk of a cascaded failure. A modified gate delay control method using a delay line IC to increase the resolution of the delay control step to 150 ps has been reported in [121]. This method allows the SiC MOSFETs to retain their switching capability

at the rated maximum operating frequency. However, this method does not account for the problem of voltage imbalance during the initial switching cycles encountered in similar aforementioned works. To solve this problem, a voltage balancing technique under steady-state and start-up conditions based on digital time delay circuit is proposed in [140]. This technique features the capability of updating the initial delay time to account for the voltage imbalance during the startup of the HV switch. However, parameter fluctuations of the switching devices due to process variation during the manufacturing process can lead to the variation of the initial delay time. In addition, the auxiliary circuits associated with generating the delays in gate signal compound the overall cost and complexity of the entire HV switch. In [141]–[143], authors introduced a new wrinkle to the dynamic voltage balancing schemes in the form of adaptive gate resistance for a specific period during the turn-ON or turn-OFF time of the switch. However, attaining the required amount of change in gate resistance with precision timing is of utmost importance to ensure optimal voltage balancing, which is relatively complex to accomplish, and costly to implement. In [117], a voltage balancing scheme incorporating a gate-balancing core is introduced to synchronize the gate drive signals for all the series-connected power devices. However, the magnetic core increases the footprint of the device, and the margin for error in core design is slim, thereby compromising its practical implementation feasibility. An active voltage control technique incorporating a current source at the gate control side of the low-side switch is proposed in [120]. However, this technique is capable of ensuring voltage balancing during switching transients for the low-side switch only.

Capacitive coupling-based series-connected switches employ a single gate driver to drive an entire switch stack aided by a few coupling components [103], [122]–[124], [144]. As

opposed to the active gate control-based voltage balancing methods, the switches in a series stack in the capacitive coupling method do not require individual gate drives, thereby resulting in a more compact footprint and reduced manufacturing/fabrication cost. In [103], the capacitive coupling method is used to control dynamic voltage balancing among series-connected MOSFETs. However, the design of the proposed HV switch is relevant for only two stages. A quasi-active gate control-based capacitive coupling method was proposed in [124] featuring a single gate driver. However, during the turn-OFF period, the gate-source voltage of the upper device of the series stack remains close to the threshold limit, thereby posing a risk of false turn-ON. Therefore, reliability and scalability issues plague this technique and compromise its implementation feasibility in practical applications. A two-stage GaN MOSFET-based HV switch featuring a capacitive coupling method is proposed in [144]. However, the scalability of this method in terms of a higher number of stages requires experimental validation. Some of these capacitive coupling based HV switch topologies are shown in Fig. 31 [103], [124], [145], [146]. One of the major drawbacks common to these topologies is the low number (2) of stages used in the design and experimental validation. The designs illustrated in Fig. 31(a) and (d) suffers from disproportionate charge distribution among the coupling capacitors, thereby resulting in considerable voltage balancing discrepancies during the switching transients among the series-connected MOSFETs. The HV switch designs shown in Fig. 31 (b) and (c) lacks the flexibility to expand the design to more than two stages, thereby not suitable for facilitating pulsed power applications with high voltage requirements.

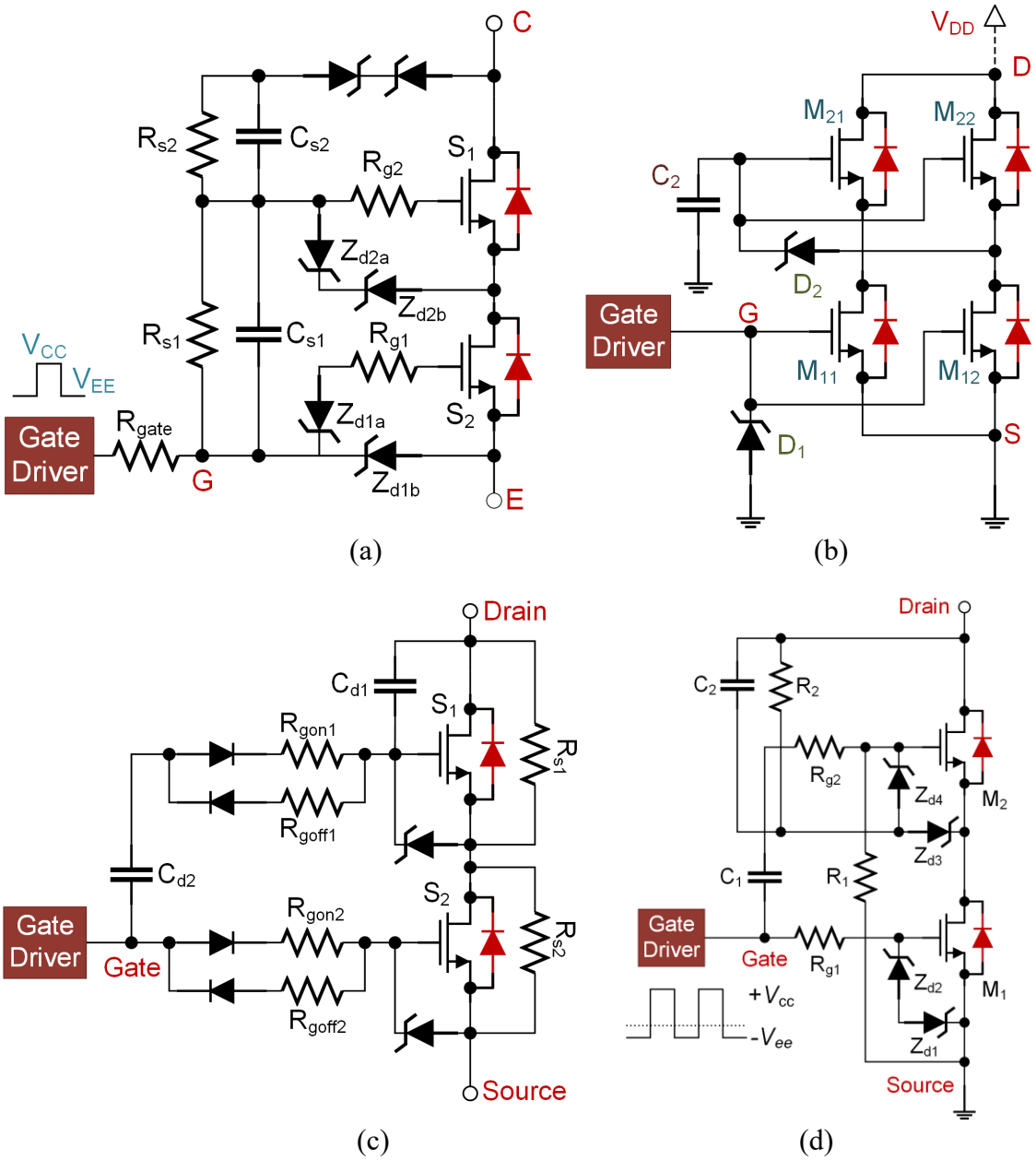


Fig. 31: Two-stage capacitive coupling based HV switch designs proposed in (a) [103] (b) [124] (c) [145] (d) [146]

In contrast with the passive snubber-based and active gate control-based dynamic voltage balancing techniques, the capacitive coupling-based technique in general offers superior response speed, simpler circuit operation, and reduced fabrication cost. However, ensuring steady voltage balancing with higher number of stages and higher operating voltage remains an area of continuous improvement in HV switch design as evidenced in Fig. 31.

The unavailability of standard isolated gate drivers at high-voltage levels (>5.7 kV) is another major design challenge in experimentally validating the efficiency of the designs of HV switches (as high-side switches) at high (>5.7 kV) voltage levels. Standard COTS isolated gate driver ICs along with standard isolated power supplies for the gate driver ICs lack adequate ruggedness to handle high *dv/dt* stress typically associated with SiC MOSFETs. To that end, developing a custom gate driver equipped with adequate voltage isolation for the power supplies and the control signal for the gate driver IC is of equal importance as designing a HV switch.

CHAPTER 6

A SINGLE GATE DRIVER BASED FOUR-STAGE HIGH-VOLTAGE SIC SWITCH

A Single gate driver-based capacitive coupling technique involving devices connected in series is a compact, low-cost solution to ensure voltage balancing in an HV switch [144]. In [103], [124], [125], [145], [147], the authors proposed single gate driver-based two-stage HV switch designs. These designs can suffer from compromised voltage balancing and insufficient gate-source threshold voltage when scaled up to a higher number of stages (>2). In order to address the needs for low-cost, high-voltage switches, a single gate driver-based compact four (4) stage HV switch with excellent voltage balancing has been proposed in this work. The proposed technique involves four series connected MOSFETs, and passive components such as diodes and capacitors are used for gate control. Therefore, it was possible to drive all four MOSFETs using a single gate driver circuit. Simulation in LTSpice and experimental results are in close agreement concerning voltage balancing across all four MOSFETs during both static and dynamic phases.

6.1 Proposed Series-Connected Four-Stage High-Voltage Switch Architecture

The schematic of the proposed four-stage series-connected switch using SiC MOSFETs and capacitive coupling is shown in Fig. 32. Aside from the SiC switches, the circuit contains coupling capacitors, C_{ci} (i=1,2,3), snubber capacitors, C_{si} (i=1,2,3,4), DC bus capacitor, C_{bus}, zener diodes, Z_{ia} and Z_{ib} (i=1,2,3,4), gate resistors, R_{gi} (i=1,2,3,4), ferrite bead, FB_i (i=1,2,3,4), balancing resistors, R_{si} (i=1,2,3,4), gate-loop diodes, D_{ci} (i=1,2,3), inductor L_1 and a freewheeling diode, D_{fw}. A gate driver is connected to the gate terminal of the bottom MOSFET

(S_1) of the series stack. The switch is connected to a resistor bank (R_{load}) configured as a low-side load.

6.2 Operating Principle of the Proposed Switch

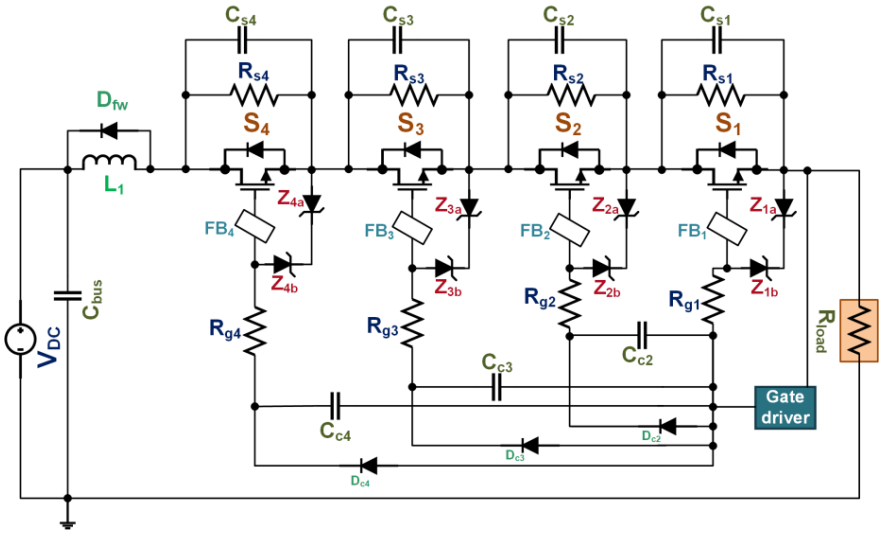


Fig. 32: Schematic of the four-stage 4.8 kV rated HV switch

6.2.1 Steady-State

The steady-state voltage imbalance among the MOSFETs in a series stack is primarily caused by the unequal leakage current. Balancing resistors (R_s) are connected in parallel to the drain-source terminals of the MOSFETs. The selection of resistors is a trade-off between power dissipation and level of voltage imbalance during the steady state. The value of the balancing resistors can be determined from the following equation [103].

$$R_s < \frac{V_{DC}}{10 I_{DSS(max)}} \tag{15}$$

Where I_{DSS} is the leakage current at $V_{GS} = 0$, and V_{DC} is the supply voltage. Lower R_s leads to a reduced level of voltage imbalance at the expense of higher static power dissipation. In

practice, resistors are chosen to have values that are one magnitude less than the equivalent OFF-state resistance of the MOSFETs to ensure leakage current passing through them.

6.2.2 Turn-ON Transition

A simplified schematic illustrating the current paths during the turn-ON transition of the HV switch is shown in Fig. 33.

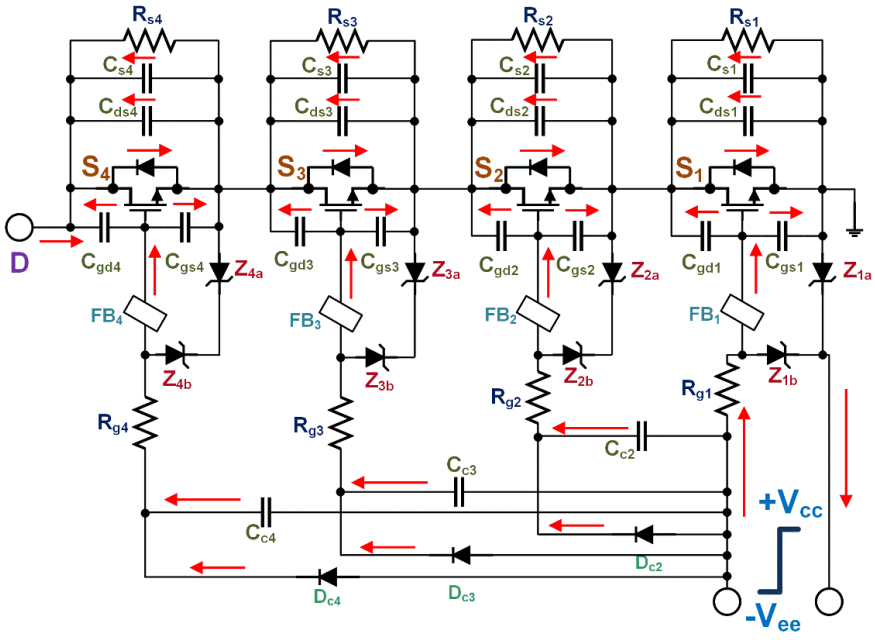


Fig. 33: Main current paths during turn-ON transition

Initially, we assume all of the series-connected switches are in the cut-off region. When the bottom MOSFET (S_1) receives the turn-ON signal ($+V_{cc}$) from the gate driver, the current starts to replenish C_{gs1} leading to the increase of V_{gs1}. S_1 enters the active region once V_{gs1} reaches $V_{gs1(th)}$, and current (i_D) starts flowing through the device, which can be expressed as follows.

$$i_D = g_m(V_{gs} - V_{gs(th)}) \tag{16}$$

Where g_m is the transconductance of the SiC MOSFET. Coupling capacitor C_{c2} starts to discharge through C_{gs2} through the newly formed conducting channel of S_1 resulting in the buildup of V_{gs2}. Meanwhile, C_{ds1} and C_{s1} start to discharge through S_1 and V_{ds1} start to fall to $V_{ds(sat)}$. However, the load current (i_D) does not increase rapidly as soon as S_1 starts conducting since the other switches are either in OFF (S_3, S_4) or partially OFF state (S_2), thereby emulating a large current limiting resistor connected in series with S_1. As soon as V_{gs2} is elevated above $V_{gs2(th)}$, discharging current from C_{c3} starts to charge C_{gs3} through S_2 and S_1, thereby increasing V_{gs3}. Meanwhile, C_{ds2} and C_{s2} start to discharge through S_1 and S_2 followed by C_{ds3} and C_{s3} resulting in a rapid decrease of V_{ds2} and V_{ds3}. Once $V_{gs3(th)}$ is reached, C_{c4} starts discharging through C_{gs4} through S_3, S_2, and S_1 followed by C_{ds4} and C_{s4} discharging through the path formed by the conducting channels of S_4, S_3, S_2, and S_1. At this stage, V_{ds} across all MOSFETs have collapsed to $V_{ds(sat)}$, and load current has been completely commutated to the switches.

6.2.3 Turn-OFF Transition

The current paths during the turn-OFF transition of the HV switch are shown in Fig. 34. The turn-OFF transition begins once the voltage level of the external gate driver shifts from $+V_{cc}$ to $-V_{ee}$. C_{gs1} starts to discharge leading to a rapid decrease of V_{gs1} followed by C_{ds1} and C_{s1} getting charged by the load current, thereby increasing V_{ds1}. In addition, the load current charges C_{c1} which in turn discharges C_{gs2}. This turn OFF event initiates the S_1 turn OFF and triggers

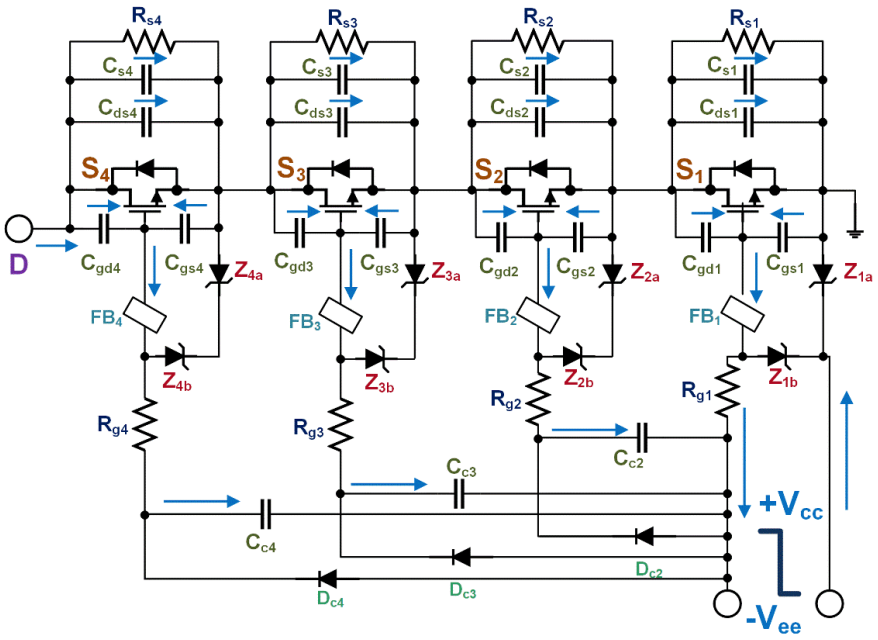


Fig. 34: Main current paths during turn-OFF transition

subsequent switching OFF procedures of the other switches in the stack. The load current charges C_{c3} and C_{c4} while discharging C_{gs3} and C_{gs4} respectively, thereby driving down V_{gs3} and V_{gs4}. Meanwhile, the load current charges C_{ds2}, C_{ds3}, C_{ds4} as well as C_{s2}, C_{s3}, C_{s4} leading to the increase of V_{ds2}, V_{ds3}, and V_{ds4} respectively. Once the gate-source voltages of all the MOSFETs fall below the threshold and drop closer to the level of $-V_{ee}$, the devices enter the cut-off region and the turn-OFF transition is complete.

6.3 Key Parameter Selection

6.3.1 Gate Resistor Selection

SiC MOSFETs have superior switching speed compared to their Si counterparts, with slew rates of 50V/ns and higher, thereby minimizing switching loss [148]. However, the extremely high slew rate in addition to the package and circuit stray inductances ($L*di/it$) can

lead to voltage overshoot and subsequent ringing [149]. Reducing stray inductance using a compactly designed PCB is a solution to the aforementioned problem pertaining to the SiC switches. That being said, minimum creepage and clearance requirements for safe high-voltage operation can inhibit the ability of the circuit designer to optimize the PCB footprint. To that end, slowing down the slew rate (di/dt) of the SiC devices by adding a sufficiently large gate resistor can be a solution to the overshoot and ringing problem at the expense of increased switching loss. In our proposed design, we have chosen 18 **Ω** resistors as gate resistors (R_{gi}, i=1, 2, 3, 4) as a tradeoff between the switching loss and the voltage overshoot.

6.3.2 Coupling Capacitor Selection

The coupling capacitors profoundly influence the switching transients of the proposed switch, which in turn impact the voltage distribution during the steady-state. Gate-source capacitances, C_{gsi} (i=2, 3, 4) of the slave MOSFETs (S_2, S_3, S_4) are charged and discharged by the discharging and charging of the coupling capacitors, C_{ci} (i= 2, 3, 4) respectively. The amount of gate charges required to turn the MOSFETs ON are entirely provided by the coupling capacitors. To that end, the stored charge in the coupling capacitors during the turn-OFF period should be greater than the total gate charges (Q_{gi}. i= 2, 3, 4) of the slave MOSFETs. Given an input voltage V_{DC}, the magnitudes of the voltage stress experienced by the coupling capacitors C_{c2}, C_{c3}, C_{c4} are $V_{DC}/4$, $2V_{DC}/4$, $3V_{DC}/4$ respectively. The required capacitance values should satisfy the following equation.

$$C_{ci} > \frac{Q_{gi}}{(i-1) * V_{DC}/4}, i = 2, 3, 4 \quad (17)$$

The typical value of the gate charge (Q_g) of the used MOSFET is 40 nC under a DC bus voltage of 800 V and a load current of 10 A. Using this value of Q_g in equation (3), the minimum

values of C_{c2}, C_{c3}, C_{c4} for a DC supply voltage of 2.5 kV are determined as 64 pF, 32 pF, and 21 pF respectively. The 4.8 kV rated HV switch prototype includes coupling capacitors with values of 68 pF, 39 pF, and 24 pF respectively.

6.3.3 Snubber Capacitor Selection

Snubber capacitors (C_{si}, i= 1, 2, 3, 4) connected across the drain-source terminals of the series-connected MOSFETs, minimizes the mismatch in slew rates (dV_{dsi}/dt, i= 1, 2, 3, 4) during switching transients. Snubber capacitors with large values incur an additional turn-OFF loss and induce a larger current spike during the turn-ON process. Notwithstanding the tangible benefit of having snubber capacitors with larger values that minimize slew rate mismatch among MOSFETs in a series stack, a tradeoff is required during the selection of the snubber capacitor values. In the fabricated HV switch prototype, 100 pF MLCC capacitors have been used as the coupling capacitors.

6.3.4 Ferrite Bead Selection

Mitigation of voltage overshoot, electromagnetic interference (EMI) associated with the ultrafast switching characteristic (i.e., high *di/dt*, high *dv/dt*) of the SiC devices is of paramount importance in any high-voltage application [76], [150]. Ferrite bead can assist gate resistors to further minimize the aforementioned issues related to ultrafast switching of the SiC devices [150]. Ferrite bead, in essence, mimics the performance of an RF choke, thereby incorporating high resistance (hundreds to thousands of ohms) in the gate loop at relatively high frequency (tens to hundreds of MHz). However, it barely impacts the circuit's operation at low frequency. Therefore, a carefully selected ferrite bead that offers high impedance at the frequency of interest (ringing frequency) can drastically elevate the performance of the SiC

switch. We have incorporated SMD ferrite beads with 2 kΩ resistance at 30 MHz in the gate loop circuits of the series-connected MOSFETs.

6.4 Simulation Results

The performance of the proposed four-stage HV switch was evaluated in LTSpice using the spice model provided by CREE for the 1.2 kV rated SiC MOSFETs. In the simulation, the switch was subjected to a 2.5 kV DC supply at a repetition frequency of 40 kHz with a 50% duty cycle. Fig. 35 shows that all gate-source signals are in good agreement with the recommended voltage swing (-5 V to 20 V) provided by the external gate driver.

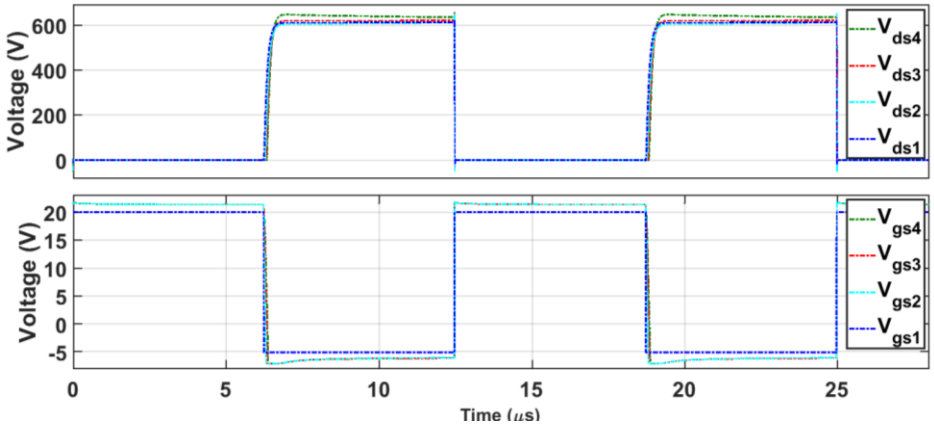


Fig. 35: Simulated (a) drain-source voltages (b) gate-source voltages across the four individual MOSFETs (V_{DC} = 2.5 kV, f_{sw} = 40 kHz, D = 50%)

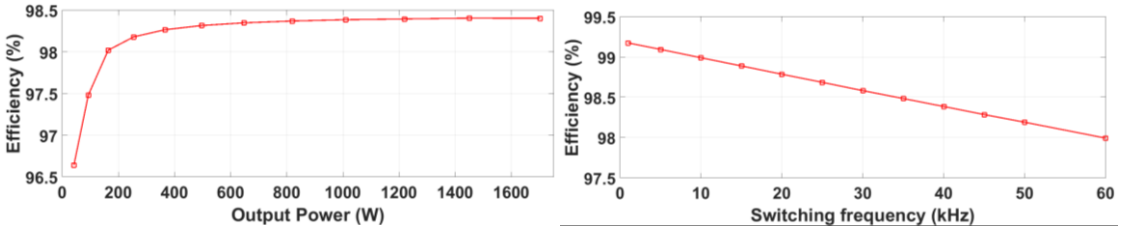
The drain-source voltages show negligible imbalance (~50V) during OFF-state. The efficiency of the proposed HV switch was evaluated in simulation at different operating conditions using a 3.2 kΩ resistive load to emulate the experimental setup. Fig. 36(a) shows the variation in efficiency during different loading conditions while keeping the switching frequency fixed at 40 kHz (Duty cycle=50%). The efficiency of the switch increases with loading as loss incurred due to the resistive load dominates the overall loss of the switch. Fig.

36(b) illustrates a steady decrease in efficiency, which is caused by increased switching loss although the load impedance remained unchanged. The switch operates at relatively high efficiency (~98%) at a switching frequency as high as 50 kHz highlighting the low-loss nature of the proposed architecture.

6.5 Experimental Setup and Results

6.5.1 Experimental Setup

To validate the proposed four-stage HV switch topology, we have fabricated two prototypes. The first one was a 4.8 kV rated HV switch, which used four 1.2 kV rated SiC



(a) (b)

Fig. 36: Effciency of the HV switch at (a) different power outputs (f_{sw}=40kHz, D=50%) (b) different switching frequency (D=50%)

MOSFETs. An isolated gate driver module (CGD15SG00D2) customized to drive SiC MOSFETs was used as the external gate driver. Two 51 kΩ, 6W rated resistors were connected in series as the balancing resistor. MLCC capacitors were used as the coupling capacitors and snubber capacitors in the fabricated switch. Gate resistors (18 Ω) followed by ferrite beads (2 kΩ @ 30 MHz) were connected to the gate terminals of each MOSFET. 20 V and 6.2 V rated Zener diodes were connected across the gate-source terminals of the MOSFETs to safeguard the gate from voltage overshoots. A 15µH rated inductor was connected in series with the switch to protect it from a sudden in-rush current, and a capacitor bank of 0.2 µF was connected

in parallel with the DC supply. A 3.2 kΩ load was fabricated using sixteen 100 W, 200 Ω thick-film resistors.

The second prototype was a 6.8 kV rated HV switch, which was constructed using four 1.7 kV rated surface-mount MOSFETs. Capacitors, gate resistors, zener diodes, gate-loop diodes, and an inductor used in this modified prototype are surface-mount types as well. Surface-mount heat sinks are soldered to the exposed drain tabs of the surface-mount MOSFETs for efficient heat dissipation. This HV switch prototype is shown in Fig. 37. The use of surface-mount components supposedly helps to reduce the stray inductances in the circuit layout, thereby minimizing oscillations caused by fast switching. All the experimental data were recorded on MSO64, which is a high-speed mixed-signal oscilloscope. The experimental setup to test the 4.8 kV rated HV switch including the load bank is shown in Fig. 38.

6.5.2 Experimental Results

The 4.8 kV rated HV switch with four stages was tested using a DC supply voltage of 2.5 kV and at a repetition frequency of 20 and 40 kHz with a 50% duty cycle. The measured drain-source voltages and the gate-source voltages across these four MOSFETs are shown in

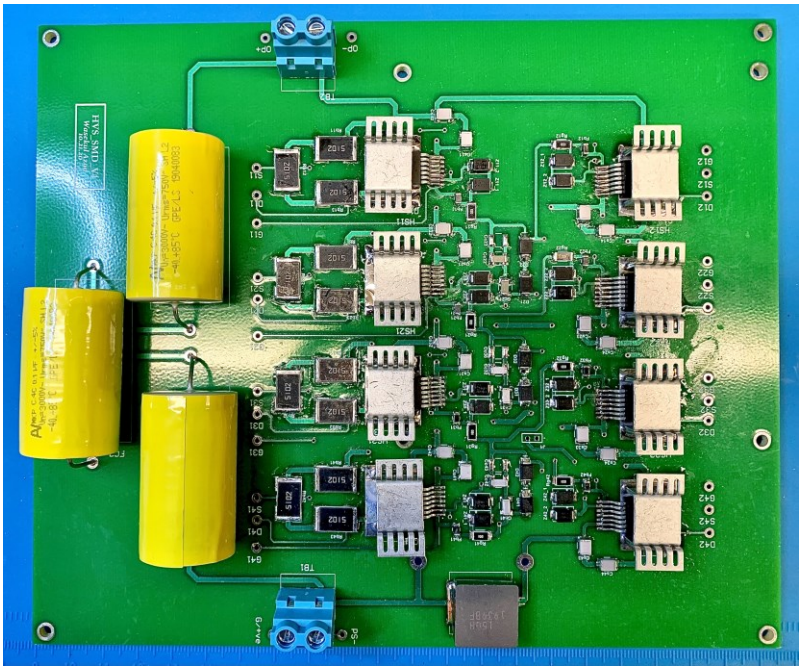


Fig. 37: The 6.8 kV rated HV switch prototype

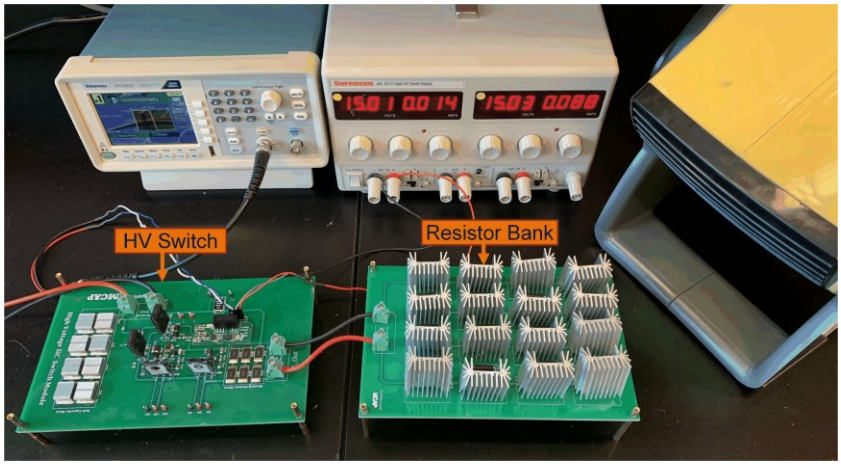
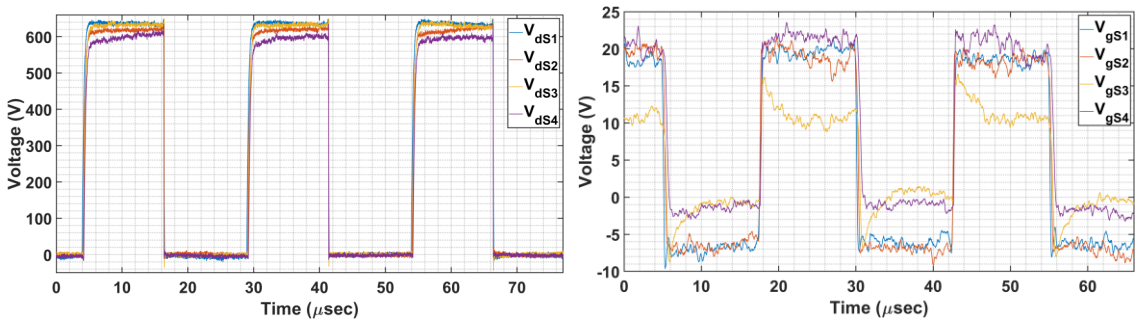


Fig. 38: Experimental setup of the HV switch with a 3.2 kΩ resistive load

Fig. 39. It is evident from this figure that all the switches in the series stack can turn ON and OFF successfully following the transitions of the external gate driver signal. A maximum voltage imbalance close to 40 V was recorded among the drain-source voltages of the four



(a) (b)

Fig. 39: (a) Experimental drain-source voltages across the four individual MOSFETs (V_{DC}= 2.5 kV) (b) experimental gate-source voltages across the four individual MOSFETs

series-connected MOSFETs during steady-state which is negligible compared to the voltage rating (1200 V) of the individual MOSFETs. The experimental results shown in Fig. 39 are in good agreement with the simulation results shown in Fig. 35. The measured gate-source signals exhibit some degree of oscillations that can be attributed to the inductance of the long ground lead of the probe (P5100), mutual EMI coupling of the probes, and parasitic inductance of the PCB layout. The voltage across the 3.2 kΩ load was measured and shown in Fig. 40. The rise and fall times of the load voltage are 40.2 ns and 550 ns respectively.

The four-stage 6.8 kV rated HV switch (prototype 2) was tested at a DC supply voltage up to 4 kV and at a switching frequency up to 20 kHz with the 3.2 kΩ resistive load. A custom gate driver was fabricated and used as the external gate driver to drive the entire stack of the series-connected switches. The test results are summarized in Fig. 41. The rise time of the load voltage was measured close to 101 ns.

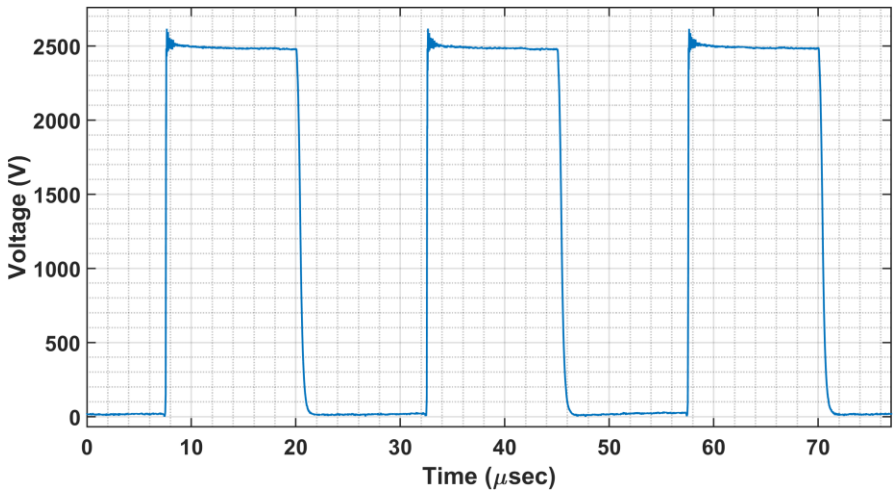


Fig. 40: Voltage measured across 3.2 kΩ resistive load at 2.5 kV (f_{sw} =40 kHz, D=50%)

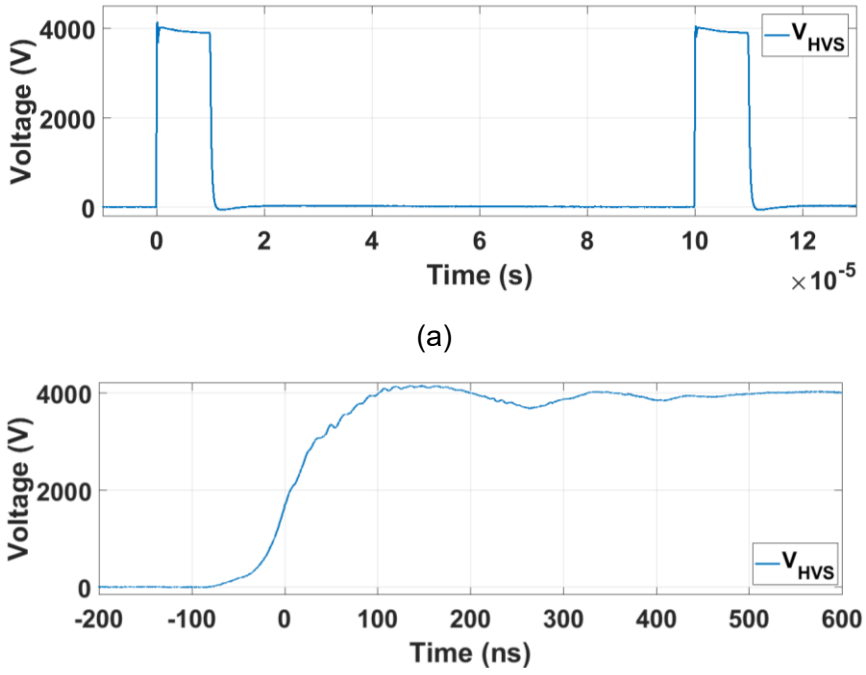


Fig. 41: (a) Voltage measured across 3.2 kΩ resistive load at 4 kV (f_{sw}=10 kHz) (b) zoomed-in version of the load voltage during turn-on transient

6.6 Conclusion

In this work, a single gate driver-based four-stage HV SiC switch topology has been proposed. Two HV SiC switch modules rated for 4.8 kV and 6.8 kV respectively have been designed and developed. A limited number of passive components, an intriguing voltage balancing scheme entailing a single gate driver, and four-stages makes this compact device an enticing option as a solid-state switch to use in high-voltage and high-speed applications. The performance of the switch is validated using results obtained from simulation and experiments, which are in good agreement.

CHAPTER 7

A MULTILEVEL-MODULAR HIGH-VOLTAGE SIC SWITCH MODULE USING CUSTOM HIGH-VOLTAGE ISOLATED GATE DRIVER

This work presents a multilevel-modular high-voltage (HV) switch architecture comprised of series-connected SiC MOSFETs and a voltage balancing method that achieves <1.1% voltage mismatch under steady-state and switching modes. An individual module consists of four series-connected 1.7-kV rated SiC MOSFETs, yielding a breakdown voltage of 6.8-kV, and driven by a single custom 10-kV isolated gate driver. One gate driver per module and 46 passive components (e.g., coupling capacitors, resistors, etc.) per module lead to low-cost fabrication and simpler operation of this HV switch. The unique modularity feature of the proposed switch enables voltage scalability to the limit of the weakest passive link. Any single or a combination of multiple passive components (e.g., capacitors, diodes, resistors, etc.) can form the weakest passive link in a module. The working principle of the HV switch during switching transients and steady-state are demonstrated and compared in simulation and from measurements. Simulation and experimental results demonstrate excellent voltage balancing as supported by a minimal voltage imbalance of <80-V among the individual MOSFETs in the HV switch at a supply voltage of 6-kV and a switching frequency of 15-kHz.

7.1 Proposed Modular Series-Connected Four-Stage High-Voltage Switch Architecture

The schematic of the proposed modular switch using series-connected SiC MOSFETs is shown in Fig. 42. Two identical modules comprise the HV switch, and each module consists

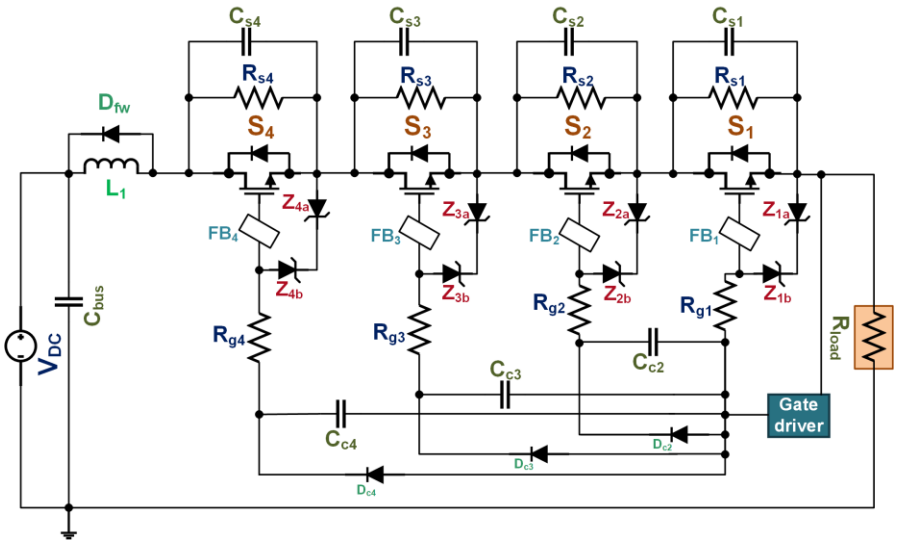


Fig. 43: Detailed schematic of a single module of the modular HV switch

of four series-connected MOSFETs. Aside from the SiC switches (S_i, i= 1, 2…..8), the circuit of the HV switch contains coupling capacitors, C_{ci} (i=2, 3, 4, 6, 7, 8), snubber capacitors, C_{si} (i=1, 2…8), zener diodes, Z_{ia} and Z_{ib} (i=1, 2….8), gate resistors, R_{gi} (i=1, 2….8), ferrite bead, FB_i (i=1, 2….8), balancing resistors, R_{si} (i=1, 2…..8), gate-loop diodes, D_{ci} (i=2, 3, 4, 6, 7, 8), inductor L_1 and a freewheeling diode, D_{fw}. A DC bus capacitor bank, C_{bus} is connected across the entire switch, and incorporated in the fabricated HV switch prototype to reduce parasitic inductance stemming from additional wire-board connections. Two custom HV gate drivers are connected across the gate-source terminals of the rightmost MOSFETs (S_1, S_5) in each module. These MOSFETs can be coined as the master MOSFETs for the ease of narration. The rest of the MOSFETs are termed as slave MOSFETs. A detailed schematic diagram of a single module is illustrated in Fig. 43.

7.2 Operating Principle of the Proposed Modular Switch

7.2.1 Turn-ON Transition

The turn-ON transition of the proposed HV switch can be segmented into four stages. The identical nature of the series-connected modules leads to a remarkable similarity in transition during the turn-ON period pertaining to each module. Therefore, the four stages associated with the turn-ON transition of a single module are shown in Fig. 44. The current paths critical to the analysis of the turn-ON transition are illustrated in Fig. 45.

Stage-1: At the onset of the turn-ON transition of the HV switch, the custom gate drivers supply recommended level of negative voltage ($-V_{ee}$) to the gate-source terminals of the master MOSFETs (S_1, S_5) of each module. At this point, the entire switch stays in a reliable OFF state; thereby no current is flowing through the MOSFETs. However, leakage current flow through

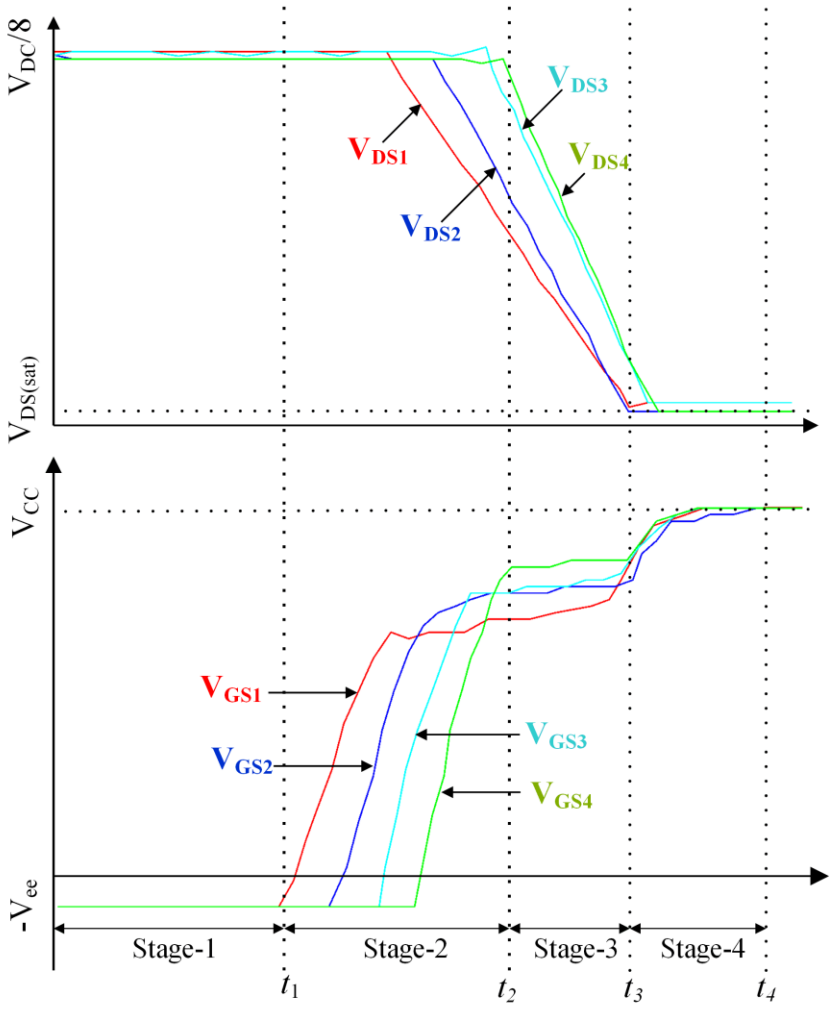


Fig. 44: Turn-ON transition of the four series-connected MOSFETs in a single module of the proposed HV switch

the path formed by the balancing resistors, R_{si} (i= 1, 2…8), and each MOSFET in the stack (S_1, S_2…..S_8) experiences equal voltage stress of $V_{DC}/8$. At t_1, the master MOSFETs (S_1, S_5) receive turn-ON signal ($+V_{cc}$) from the corresponding gate drivers.

Stage-2: At the advent of the turn-ON process at t_1, the charging currents from the gate drivers begin to charge the input capacitances (C_{iss1}, C_{iss5}) of S_1 and S_5 through corresponding gate

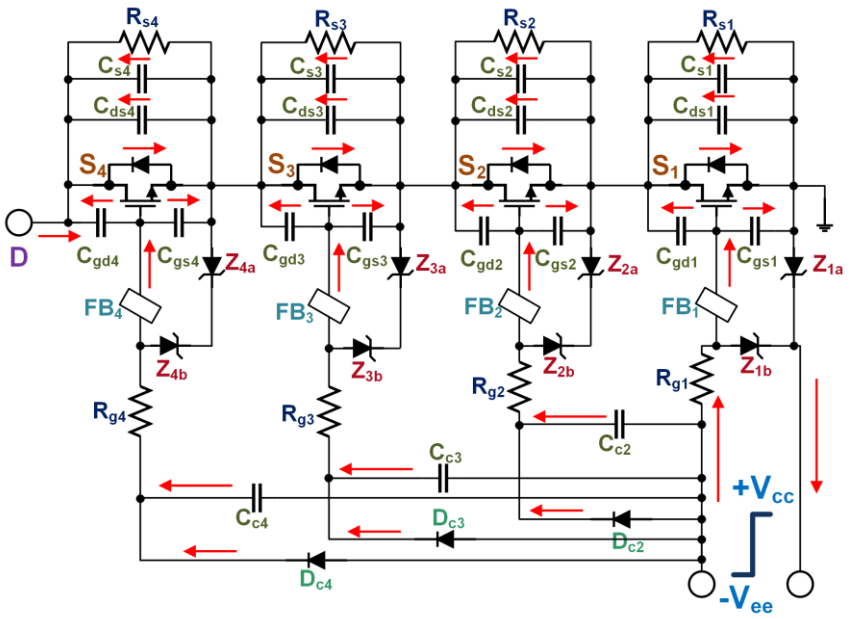


Fig. 45: Main current paths in a single module during turn-ON transition

resistors (R_{g1}, R_{g5}). The input capacitance (C_{iss}) of a MOSFET is the sum of the gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}). The initiation of the charging process causes V_{gs1} and V_{gs5} to increase exponentially from the voltage level of V_{ee}. During this stage spanning from t_1 to t_2, $V_{gs1(th)}$ and $V_{gs5(th)}$ are reached, thereby propelling S_1 and S_5 from the cutoff region to the active region. Once S_1 and S_5 are in the active region, they can be modeled as voltage-controlled current sources following the relationship stated as follows.

$$i_d = g_{mi} * (V_{gsi} - V_{gsi(th)}) \tag{18}$$

Where g_{mi} is the transconductance of the SiC MOSFET and i=1, 5. The rest of the MOSFETs (S_i, i = 2, 3, 4, 6, 7, 8) that belong to the HV switch remain in OFF state at this point. Therefore, it can be approximated that S_1 and S_5 are connected with a large valued resistor connected in series with them at this stage preventing current (i_D) from DC supply flowing through the switch. During this stage, V_{gs1}, V_{gs5} reach the Miller plateau followed by

the gradual discharge of C_{si} (i= 1, 5) and C_{dsi} (i = 1, 5) resulting in a gradual decrease of V_{ds1}, V_{ds5} from V_{DC}/8. The fall rate of the drain-source voltages across the MOSFETs in a series stack can be expressed by the following relationship.

$$\frac{dV_{dsi}}{dt} \approx -\frac{i_{gi}}{C_{gdi}}, i = 1, 2 \ldots\ldots 8 \tag{19}$$

Where i_{gi} is the current flowing in the gate loop of the MOSFET S_i. At this point, coupling capacitors, C_{ci} (i= 2, 3, 4, 6, 7, 8) starts to discharge through the gate-source capacitors, C_{gsi} (i = 2, 3, 4, 6, 7, 8) of the other MOSFETs, S_i (i= 2, 3, 4, 6, 7, 8) respectively through partially ON channels. The generalized flow direction of the discharge current can be denoted as $V_{cc} \rightarrow C_{ci} \rightarrow R_{gi} \rightarrow C_{gsi} \rightarrow \sum_1^{i-1} S_i$, where, i = 2, 3, 4 for the first module, and $V_{cc} \rightarrow C_{cj} \rightarrow R_{gj} \rightarrow C_{gsj} \rightarrow \sum_5^{j-1} S_j$, where, j = 6, 7, 8 in case of the second module. In the meantime, these discharge currents begin to charge C_{gsi} (i = 2, 3, 4, 6, 7, 8) and increase the gate-source voltages (V_{gsi}, i = 2, 3, 4, 6, 7, 8) of the rest of the MOSFETs in the series stack. The increased gate-source voltage (ΔV_{gs}) correlates with the reduced charge from the coupling capacitor as expressed in the following equation.

$$\Delta V_{gsi} = \frac{C_{ci} * \Delta V_{ci}}{C_{gsi}} \quad , i=2, 3, 4, 6, 7, 8 \tag{20}$$

Where ΔV_{ci} is the level of the voltage drop across the coupling capacitors. Evidently, larger coupling capacitors will lead to faster charging of the gate-source voltages of the MOSFETs in the series stack and accentuate the turn-ON transition of the switch. Conversely, larger coupling capacitors that are in parallel with the output capacitances of the MOSFETs will increase the transition time during the turn-OFF period. In addition, the following relationships pertain to this stage as well.

$$i_{gk}R_{gk} + V_{gsk} + \sum_{k=1}^{k-1} V_{dsk} = V_{cc} + V_{Ck} \quad , k = 1, 2, 3, 4 \quad (21)$$

$$i_{gl}R_{gl} + V_{gsl} + \sum_{l=5}^{l-5} V_{dsl} = V_{cc} + V_{Cl} \quad , l = 5, 6, 7, 8 \quad (22)$$

$$i_{gm} = -\frac{C_{cm}dV_{cm}}{dt} = \frac{C_{gsm}dV_{gsm}}{dt} \quad , m = 2, 3, 4, 6, 7, 8 \quad (23)$$

Where, V_{cl}, V_{cm} denote the voltages across the coupling capacitors in the HV switch. At the end of this stage, gate-source voltages (V_{gsi}, i = 2, 3, 4, 6, 7, 8) of the slave MOSFETs (S_i, i = 2, 3, 4, 6, 7, 8) reach Miller plateau.

Stage-3: During this stage, V_{dsi} (i = 2, 3, 4, 6, 7, 8) begins to fall rapidly from $V_{DC}/8$ as snubber capacitors (C_{si}, i = 2, 3, 4, 6, 7, 8) and drain-source capacitances, C_{dsi} (i = 2, 3, 4, 6, 7, 8) start to discharge through the partially ON channels of the series-connected devices. The drain-source voltages approach a saturated level ($V_{DS(sat)}$) which the MOSFETs hold throughout the ON-state. V_{gsi} (I = 1, 2…8) begins to rise above the Miller plateau and current (i_D) starts to increase, and within a short period assumes the value of the full-load current (i_L).

Stage-4: During this stage, voltages across the drain-source terminals (V_{dsi}, i= 1, 2…..8) of all the MOSFETs (S_1, S_2….S_8) reach the saturation level ($V_{DS(sat)}$), and stay at this level throughout the ON period. V_{gsi} (i= 1, 2…..8) exceed the Miller plateau and approach the positive voltage level (V_{cc}) pertaining to the gate driver signal. All the gate drive loops are completely formed at this point and can be defined as: $V_{cc} \rightarrow D_{ci} \rightarrow R_{gi} \rightarrow C_{gsi} \rightarrow \sum_1^{i-1} S_i$, where, i = 2, 3, 4 for the first module, and $V_{cc} \rightarrow D_{cj} \rightarrow R_{gj} \rightarrow C_{gsj} \rightarrow \sum_5^{j-1} S_j$, where, j = 6, 7, 8 for the second

module. The end of this stage is marked by V_{gsi} (i= 1, 2…..8) reaching V_{cc}, and load current (i_L) completely commutating to the series-connected MOSFETs.

7.2.2 Turn-OFF Transition

The turn-OFF transition of the proposed HV switch can be segmented into four stages as well. The identical nature of the series-connected modules leads to a remarkable similarity in transition during the turn-OFF period pertaining to each module. Therefore, the four stages associated with the turn-OFF transition of a single module are shown in Fig. 46. The current paths critical to the analysis of the turn-OFF transition are illustrated in Fig. 47.

Stage-1: During this stage, the gate-source voltage signals across the MOSFETs in each module maintain the voltage level (V_{cc}) recommended for sustaining the turn-ON state of the SiC MOSFETs. The custom gate drivers keep supplying this recommended level of voltage signal (V_{cc}) till t_1. Therefore, all the MOSFETs (S_1, S_2….S_8) in the series stack operate in the ohmic region characterized by low ON-state resistance during this stage. A sustained level of full load current (i_L) keeps flowing through the series-connected modules during this stage.

Stage-2: At t_1, the master MOSFETs (S_1, S_5) receive turn-OFF signals ($-V_{ee}$) from the connected custom HV gate drivers. Upon receiving the turn-OFF signals, C_{gs1}, C_{gs5} start to discharge through the following path: $C_{gsi} \rightarrow R_{gi} \rightarrow V_{ee}$, where, i= 1, 5. Secondary discharging loops for other gate-source capacitances (C_{gsi}, i = 2, 3, 4, 6, 7, 8) are created without further delay as opposed to the delay in secondary charging loop creation during the turn-ON phase.

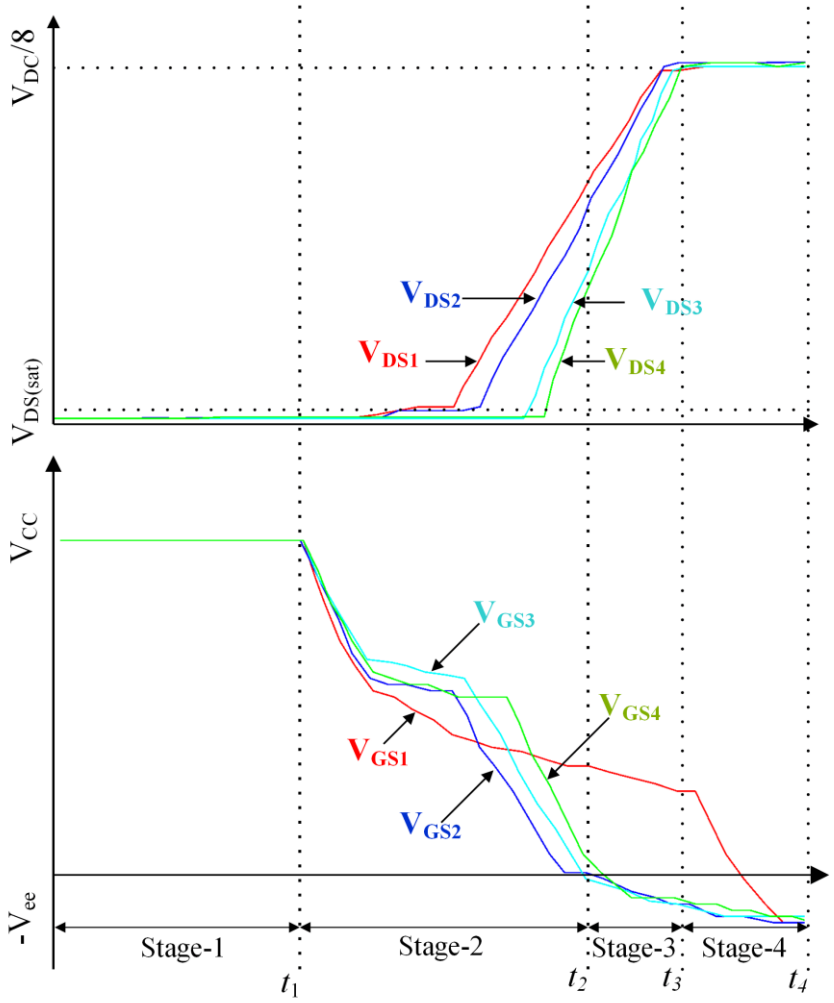


Fig. 46: Turn-OFF transition of the four series-connected MOSFETs in a single module of the proposed HV switch

The secondary discharging path can be expressed as follows: $\sum_1^{i-1} S_i \rightarrow C_{gsi} \rightarrow R_{gi} \rightarrow C_{ci} \rightarrow V_{ee}$, where, i = 2, 3, 4 for the first module, and $\sum_5^{j-1} S_i \rightarrow C_{gsi} \rightarrow R_{gi} \rightarrow C_{ci} \rightarrow V_{ee}$, where, j = 6, 7, 8 for the second module. However, charging of the coupling capacitors (C_{ci}, i = 2, 3, 4, 6, 7, 8) prolong the discharging period of gate-source capacitors of the slave MOSFETs (S_i, i = 2, 3, 4, 6, 7, 8) compared to the master MOSFETs (S_1, S_5). Consequently, the slopes of V_{gs1}, V_{gs5} are steeper compared to the initial gate-source voltage slopes of the slave MOSFETs

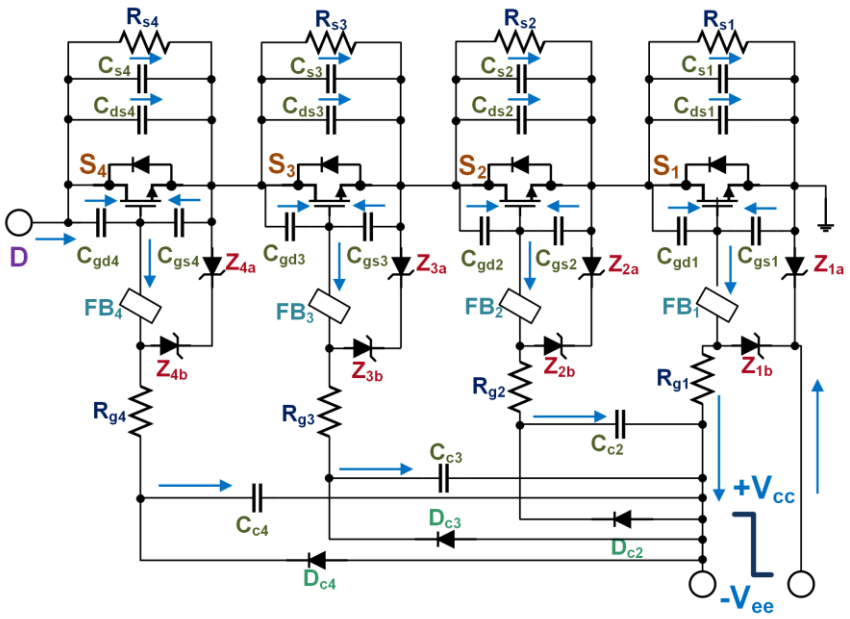


Fig. 47: Main current paths in a single module during turn-OFF transition

during this stage. Midway through this stage, V_{gsi} (i= 1, 2…..8) keeps falling toward the Miller plateau level. V_{gs1}, V_{gs5} plunge below the Miller plateau level earlier compared to the gate-source voltages of the slave MOSFETs. This event triggers the rising of V_{ds1}, V_{ds5}, and charging of the snubber capacitor C_{s1}, C_{s5} along with C_{ds1}, C_{ds5} by the load current. The rate of the voltage rise across the drain-source terminals of the MOSFETs can be stated as:

$$\frac{dV_{dsi}}{dt} \approx -\frac{i_{gi}}{C_{gdi}}, i = 1, 2 \ldots\ldots 8 \tag{24}$$

The rate of the fall of the gate-source voltages of the slave MOSFETs (V_{gsi}, i = 2, 3, 4, 6, 7, 8) begins to ramp up during the latter half of this stage and they fall below the Miller plateau level, and V_{dsi} (i = 2, 3, 4, 6, 7, 8) of these MOSFETs subsequently start increasing. Associated snubber capacitors (C_{si}, i = 2, 3, 4, 6, 7, 8) and C_{dsi} (i = 2, 3, 4, 6, 7, 8) begin to get charged by the load current as well.

Stage-3: During this stage, V_{dsi} (i = 1, 2…..8) of all the series-connected MOSFETs in the HV switch approaches the steady-state voltage level (V_{DC}/8). Near the end of this stage, the voltage across the MOSFETs in both of the modules stabilizes and attains the steady-state value of V_{DC}/8.

Stage-4: V_{gsi} (i = 1, 2…..8) continues to decline and approaches the negative voltage level (-V_{ee}) provided by the custom gate drivers. At the end of this stage, all the gate-source voltages attain the turn-OFF voltage level (-V_{ee}) and current (i_D) stops flowing through the switch altogether marking the end of the turn-OFF transition. All the series-connected MOSFETs hold the steady-state voltage level (V_{DC}/8) across their corresponding drain-source terminals during this stage.

7.3 Key Parameter Selection

7.3.1 Balancing Resistor

During the steady-state, the modular switch as a whole is subjected to the entire DC bus voltage. Two mechanisms primarily govern the degree of voltage imbalance among the series-connected MOSFETs in the series stack. Unequal leakage currents pertaining to the manufacturing process variations of the MOSFETs in the modular switch act as the salient instigator of the voltage imbalance during the steady-state. On top of that, probable voltage imbalance among the drain-source voltages of the series-connected MOSFETs at the end of the turn-OFF transition stage may carry over to the ensuing steady-state. Resistors can be connected in parallel to the drain-source terminals of the series-connected MOSFETs to minimize the aforementioned voltage imbalance issue associated with the steady-state. The selection of these resistors (R_{si}, i= 1, 2….8), termed as balancing resistors, is a trade-off between power dissipation

and the level of voltage imbalance during the steady-state. The value of the balancing resistors required to ensure a steady-state voltage imbalance ratio below 10% can be determined from the following equation [103].

$$R_{\mathrm{si}} < \frac{V_{\mathrm{DC}}}{10 I_{\mathrm{DSS(max)}}}, i = 1, 2 \ldots \ldots 8 \tag{25}$$

Where I_{DSS} is the leakage current at $V_{\mathrm{GS}} = 0$, and V_{DC} is the supply voltage. Lower R_{s} leads to a reduced level of voltage imbalance at the expense of higher static power dissipation. In practice, resistors are chosen to have values that are one magnitude less than the equivalent OFF-state resistance of the MOSFETs to direct the leakage current passing through them instead of the MOSFETs.

7.3.2 Coupling Capacitors

The influence of the coupling capacitors on the dynamics of the switching transient of the individual MOSFETs of the proposed modular switch is pronounced. The gate-source capacitances of the slave MOSFETs are charged and discharged by the discharging and charging of the coupling capacitors respectively. This implies that the amount of gate charge required to completely turn the slave MOSFETs ON and OFF are solely provided by these coupling capacitors. To that end, the stored charge in the coupling capacitors during the turn-OFF period should be greater than the total gate charges (Q_{gi}, i= 2, 3, 4, 6, 7, 8) of the slave MOSFETs.

In the proposed architecture, the coupling capacitor associated with the slave MOSFET located farthest from the master MOSFET in each module experiences the maximum voltage stress which does not exceed a level of $3V_{\mathrm{DC}}/8$ thanks to the modularity of the proposed switch.

The voltage level experienced by C_{c2}, C_{c6} is $V_{DC}/8$, and in the case of C_{c3}, C_{c7} it is $2V_{DC}/8$. The required capacitance values should satisfy the following equation.

$$C_{ci} > \frac{Q_{gi}}{(i-1) * V_{DC}/8}, i = 2, 3, 4 \quad (26)$$

$$C_{cj} > \frac{Q_{gj}}{(j-5) * V_{DC}/8}, j = 6, 7, 8 \quad (27)$$

The typical value of the gate charge (Q_g) of the used MOSFET is 13 nC under a DC bus voltage of 1.2 kV and a load current of 2 A. From equations (9) and (10), the minimum value required for the coupling capacitors at 6 kV can be determined as 5.7 pF, 8.7 pF, and 17.3 pF. The proposed modular switch includes coupling capacitors with values 7 pF, 10 pF, and 21 pF, thereby closely approximating the theoretical values.

7.3.3 Gate Resistors

SiC MOSFETs have superior switching speed compared to their Si counterparts, reaching a slew rate as high as 50V/ns [148]. However, the extremely high slew rate in addition to the package and circuit stray inductances can lead to voltage overshoot (*L*di/dt*) and subsequent ringing [76], [149]. A compactly designed PCB can contribute significantly to the reduction of stray inductance, thereby mitigating the aforementioned problem to a great extent. That said, minimum creepage and clearance requirements for safe high-voltage operation can inhibit the ability of the circuit designer to optimize the PCB footprint. An alternative solution can come in the form of sufficiently large gate resistors at the expense of increased loss. In our proposed design, we have incorporated 15 Ω gate resistors as a tradeoff between the level of gate ringing and additional loss.

7.3.4 Snubber Capacitors

Snubber capacitors (C_{si}, i= 1, 2…..8) connected across the drain-source terminals of the series-connected MOSFETs, minimizes the mismatch in slew rates (dV_{dsi}/dt, i= 1, 2,…..8) during switching transients. Unlike traditional snubber capacitors, small valued (in the range of picofarads) capacitors are connected across the drain-source terminals of individual MOSFETs. Snubber capacitors with large values prolong the turn-OFF transition of the individual MOSFETs, thereby increasing the switching loss. Conversely, the absence of snubber capacitors curtails the transition time during the turn-OFF period of the switch at the expense of too big of a mismatch between the slew rates of the individual MOSFETs that can potentially lead to voltage imbalance of excessive proportions. To that end, a tradeoff is required during the selection of the snubber capacitor values. In the fabricated HV switch prototype, 100 pF ceramic capacitors have been used as snubber capacitors.

7.3.5 Ferrite Beads

Mitigation of voltage overshoot, electromagnetic interference (EMI) associated with the ultrafast switching characteristic (i.e., high *di/dt*, high *dv/dt*) of the SiC devices is of paramount importance in any high-voltage application [76], [150]. Ferrite bead can assist gate resistors to further minimize the aforementioned issues related to ultrafast switching of the SiC devices [150]. Ferrite bead, in essence, mimics the performance of an RF choke, thereby incorporating high resistance (hundreds to thousands of ohms) in the gate loop at relatively high frequency (tens to hundreds of MHz). However, it barely impacts the circuit's operation at low frequency (tens to hundreds of kHz). Therefore, a carefully selected ferrite bead that offers high impedance at the frequency of interest (ringing frequency) can drastically elevate

the performance of the SiC switch. We have incorporated SMD ferrite beads with 2 kΩ resistance at 30 MHz in the gate loop circuits of the series-connected MOSFETs.

7.4 Design Details of a Custom High-Voltage Isolated Gate Driver

With the rapid advancement of wide bandgap semiconductor devices (e.g., SiC, GaN MOSFETs) over the last decade, the breakdown voltage rating of WBG MOSFETs has reached as high as 3.3 kV. This high-voltage (HV) WBG MOSFETs have contributed to the ongoing development of high-voltage switches with high breakdown voltages, such as 27.5 kV 4H-SiC n-IGBT [151], 15 kV SiC IGBT [152], etc. That being said, commercially available gate drivers have a maximum isolation rating of 5.7 kV, thereby not suitable to drive the aforementioned HV semiconductor devices. On top of that, the high switching speed capability of SiC devices can subject a gate driver to a *dv/dt* stress as high as 100kV/µs which imposes a low isolation capacitance requirement in the gate driver design [153], [154].

7.4.1 Design Criteria of a Custom High-Voltage Isolated Gate Driver

Two fundamental isolation requirements are needed to be addressed while designing a HV isolated gate driver. Isolation for the power supplies of the gate driver IC and isolation for

the control signal (e.g., PWM signal, protection, monitoring, etc.) are these two levels of isolation as shown in Fig. 48 [151].

Optocouplers [155], coreless transformers [156], classical transformers [157] are some

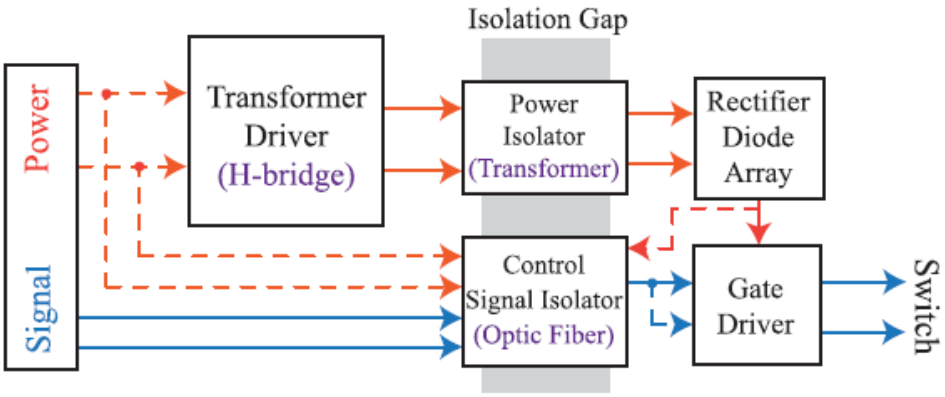


Fig. 48: Basic schematic of an isolated gate driver circuit. Power isolation stage and control signal isolation stage are incorporated in the gate driver [149]

of the isolation schemes employed for control signal isolation. That being said, owing to the superior noise immunity, isolation voltage capability it retains, optical fiber remains by far the most promising and practical method of control signal isolation technique. Ensuring adequate galvanic isolation for the power supplies of the gate driver IC is more sophisticated as opposed to control signal isolation. The sophistication stems from the simultaneous requirements of high galvanic isolation, low coupling capacitance, and compact footprint. However, keeping the footprint compact compromises the requirements of low coupling capacitance, high galvanic isolation, and vice versa. The small gate capacitance of the SiC devices allows fast switching speed leading to an extremely high *dv/dt*. The high *dv/dt* coupled with high isolation capacitance (C_{iso}) can introduce common-mode (CM) current (i_{CM}) that can perturb the normal

operation of the gate driver and pose health risks to the human operator at the control side. The CM current is related to the isolation capacitance and *dv/dt* through the following equation.

$$i_{CM} = C_{iso} \frac{dv}{dt} \tag{28}$$

A number of medium to high-voltage isolated gate drivers have been proposed in the literature [153], [154], [158]–[160]. Multiple isolation transformer topologies intended for use in HV isolated gate drivers have been proposed in [161]. Isolation capability up to a voltage rating of 20 kV has been claimed in this paper without experimental validation. A power over optical fiber (PoF) concept has been proposed in [162] to transfer power from a laser to a floating gate driver over optical fiber. A powerful laser feeds an optical fiber with the required amount of power which is subsequently converted to electrical energy by a laser transducer at the receiving end. The primary advantage of this approach is its inherent theoretical advantage of infinite *dv/dt* immunity along with minimal coupling capacitance. The aforementioned promising advantages notwithstanding, the bulky nature of the laser transmitter handicaps the feasibility of this approach in real-life applications. Isolated gate driver using conventional isolation transformer has been proposed in [154]. However, the conventional isolation transformer is typically associated with a larger footprint due to the low dielectric strength of air. The inductive power transfer (IPT) method has also been proposed in the literature to provide galvanic isolation to the gate driver [163]–[165]. That being said, large clearance and creepage due to the low dielectric breakdown strength of air contribute to a large isolated gate driver footprint in this method. In light of this discussion, it is evident that a custom HV isolated gate driver with sufficient isolation and low coupling capacitance in a small footprint is required to drive HV WBG switches.

7.4.2 Isolation Transformer Based High-Voltage Isolated Gate Driver

Traditionally, discrete winding-based or PCB winding-based air or tape insulated isolation transformers are employed in HV gate driver design to insulate the power supply of the gate driver IC from high voltage. However, to adhere to the minimum clearance and creepage requirement recommended by IEEE safety standards (40 mm for 10 kV according to the International Standard IEC 60950-1 [166]), the footprints of the aforementioned transformers get prohibitively big. Inductive power transfer (IPT) based galvanic isolation solution for the power supplies of the gate driver IC is another viable technique for high-voltage isolated gate driver design. That being said, the low dielectric strength of air (3 kV/mm) requires a large air gap to be incorporated in the isolation transformer design. Consequently, the overall footprint size of the IPT based gate driver will be large rendering it incompatible with a highly compact module. A galvanically isolated power supply based on an isolation transformer is expected to provide sufficient energy to the driver circuit of the HV MOSFET. If the MOSFET is in high-side configuration, the voltage levels (+20V/-5V) provided by the custom gate driver for switching operation, are referenced with respect to the switching node which could be as high as the supply voltage. In addition, the coupling capacitance of the isolation transformer should be as low as possible to minimize the common-mode (CM) currents coupled to the control side of the gate driver through the coupling capacitance of the isolation transformer. CM currents can perturb the normal operation of the gate driver and pose healths risk to the operator on the control side. That being said, traditional methods to minimize coupling capacitance ask for large distances between primary and secondary winding as well as the large distance between cores and windings, thereby increasing the footprint of the gate

driver. On the flip side, downsizing the gate driver footprint is critical to ensure physical implementation feasibly. Therefore, while designing a custom isolation transformer-based gate driver, it is of paramount importance to design a compact transformer with minimum coupling capacitance.

7.4.2.1 Design and Fabrication Procedures

The high isolation barrier requirement (10 kV) of our proposed gate driver enforces a large clearance and creepage requirement between the windings of the isolation transformer. Large clearance and creepage translate into a low magnetic coupling factor (K) and large leakage inductance which if not counteracted, can lead to a considerable load-dependent voltage drop. The output voltage (+20V/-5V) produced by the gate driver will also suffer from inconsistencies due to the load dependency. As a countermeasure, a feedback-control can be employed in the gate driver circuitry at the expense of increased complexity and heightened production cost.

Another method to address the problem is by adopting a topology with a load-independent voltage transfer ratio. Series-series resonant converter is one of the topologies that facilitates a load-independent output voltage. This topology consists of an H-bridge driver, an isolation transformer with single or multiple taps at the output, resonance capacitors, and a rectifier circuit to produce the required output DC voltage rails. The leakage inductance of the isolation transformer is compensated by the resonance capacitors incorporated in this topology. Therefore, this topology acts as an enabler for the gate driver to function in a unity gain operating point with a load-independent output voltage capability [167]. On top of that, the H-bridge driver used in the proposed design (MAX13256) has the soft-switching capability,

thereby enabling faster switching speed leading to a more compact design. A basic diagram of the proposed series-series resonant converter based DC-DC converter is shown in Fig. 49.

The series-series resonant converter is most efficient when the impedance of the primary winding is matched to the impedance of the secondary winding. For a maximum output power P_{max}, secondary side inductance L_s, the voltage at the secondary side V_s, the optimum frequency, f_0 for load matching at full load can be expressed as follows.

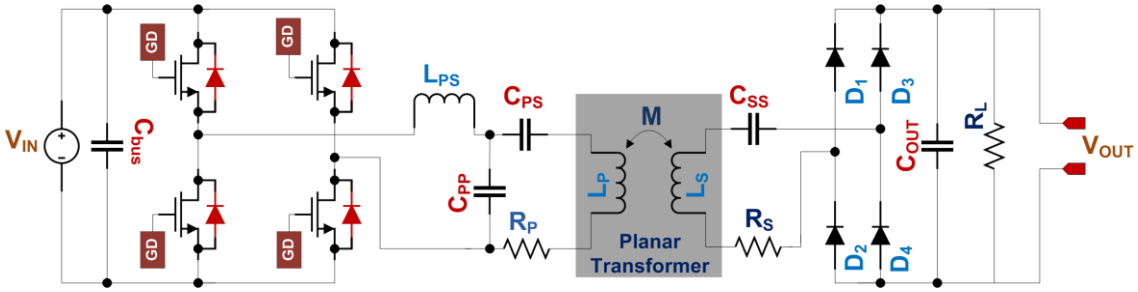


Fig. 49: Schematic of the resonant converter-based DC-DC converter for the isolated gate driver

$$f_0 = \frac{8V_s^2}{2\pi^3\sqrt{2L_s k P_{max}}} \tag{29}$$

Where k is the magnetic coupling coefficient between the primary and secondary windings of the transformer. The value of the resonance capacitors can be derived from the following equation [167].

$$C_{r1} = C_{r2} = \frac{1}{(2\pi f_0)^2 L_s (1-k)} \tag{30}$$

In traditional isolation transformers, the primary and the secondary windings are placed on the same magnetic core and galvanic isolation is ensured by insulating the primary and the secondary windings from the core and each other as well. However, to conform to a compact form factor, we can discard the insulating material between the primary winding and the core,

as both of them are at ground potential. As opposed to the primary side winding, the secondary side winding floats at a potential that can be as high as the supply voltage potential. Therefore, the secondary windings are needed to be isolated from the core as well from the primary winding and its associated core. Two separate cores have been used to wound the primary winding and the secondary winding separately and a gap close to 1.6mm has been introduced between the cores coupled with suitable potting material to provide sufficient galvanic isolation. To accommodate the secondary winding on a separate core, the window size of the chosen core should be adequately large. E30 core having N30 material has been chosen as the cores for the primary and secondary windings. To drive the selected gate driver IC ISO5852S, three isolated power supplies (+20V, ±5V) are required. Therefore, three secondary windings have been wrapped around the secondary-side core. The windings have been insulated from each other using Kapton tapes in between the three layers of secondary windings. The cores with the windings encircling them are mounted on a bobbin compatible with the E30 core. The entire arrangement has been encapsulated using a silicone potting material with a dielectric breakdown strength of 20 kV/mm. The fabricated prototype of the isolation transformer is shown in Fig. 50.

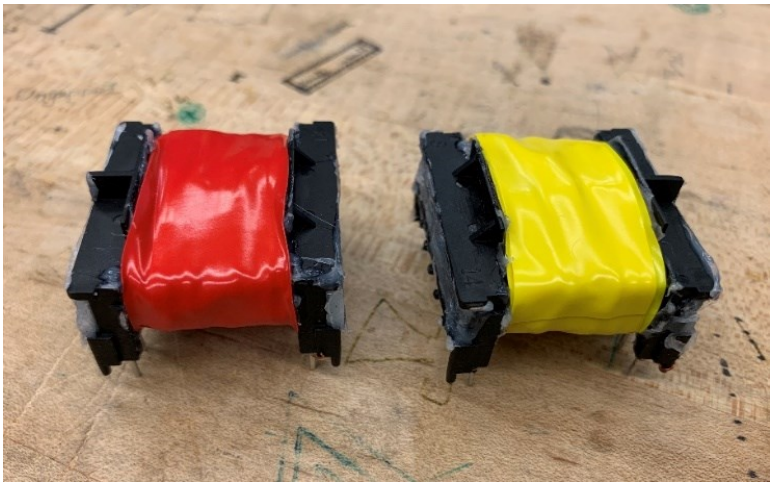


Fig. 50: Custom isolation transformers for the isolated gate driver

The primary and secondary side leakage inductances have been measured using a HIOKI LCR meter. The value of the primary side magnetizing inductance is close to 23.5 µH. The secondary side inductances associated with the coils generating the power supplies of the gate driver IC are measured as 24.6 µH, 6.8 µH, 7.1 µH respectively. The measured leakage inductance (L_σ) was close to 8.3 µH. The magnetic coupling factor pertaining to the isolation transformer can be calculated from the following equation.

$$k = \sqrt{1 - \frac{L_\sigma}{L_s}} = 0.41 \tag{31}$$

Using the value of k, the optimum operating frequency is determined as 50 kHz and the values of the resonance capacitors are determined as 4.5 nF. 20 turns of 30 AWG magnet wire have been wound on the primary side. At the secondary side, three separate coils of 30 AWG wire have been wound on the core having 24, 7, and 7 turns. Rectifier diodes and bulk capacitors are placed at the voltage output rails at the secondary side of the isolation transformer to convert the AC output signal to a DC signal. To produce steady levels of output

voltages (+20V, ±5V) for the gate driver IC, linear regulators have been incorporated in the design after the corresponding bulk capacitors. The fabricated prototype of the gate driver circuit using an isolation transformer is shown in Fig. 51.

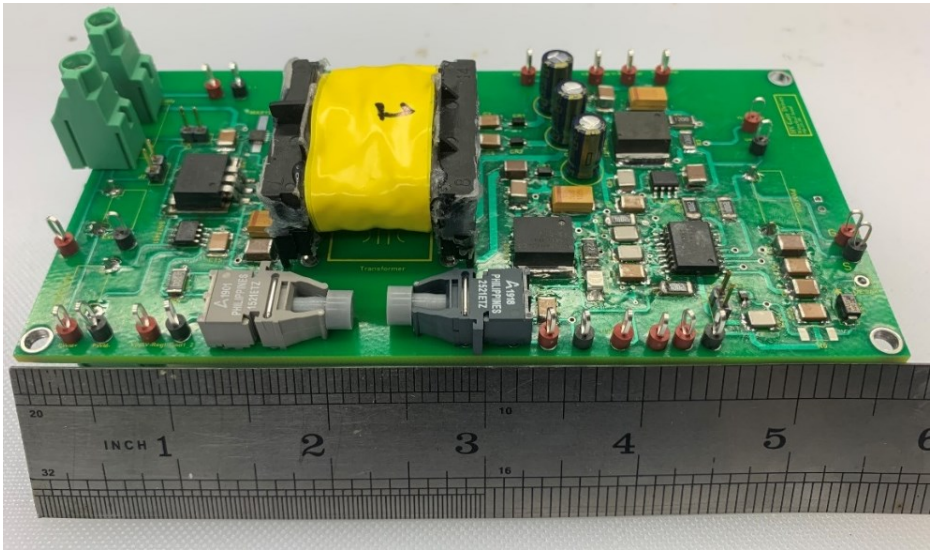


Fig. 51: Prototype of the custom isolation transformer based isolated gate driver

7.4.2.2 Experimental Results

At the primary side, a 20 V DC supply has been incorporated as the primary power source of the gate driver. The H-bridge driver (MAX13256) has been externally triggered using a function generator. After post-rectification and linear regulation, we have obtained three voltage rails with values of 18V, +5V, and -5V as shown in Fig. 52.

7.4.3 Commercial DC-DC Converter Based High-Voltage Isolated Gate driver

The modular 10 kV rated HV switch proposed by the authors in this work requires two isolated HV gate drivers, one for each module of the HV switch. The required isolation rating

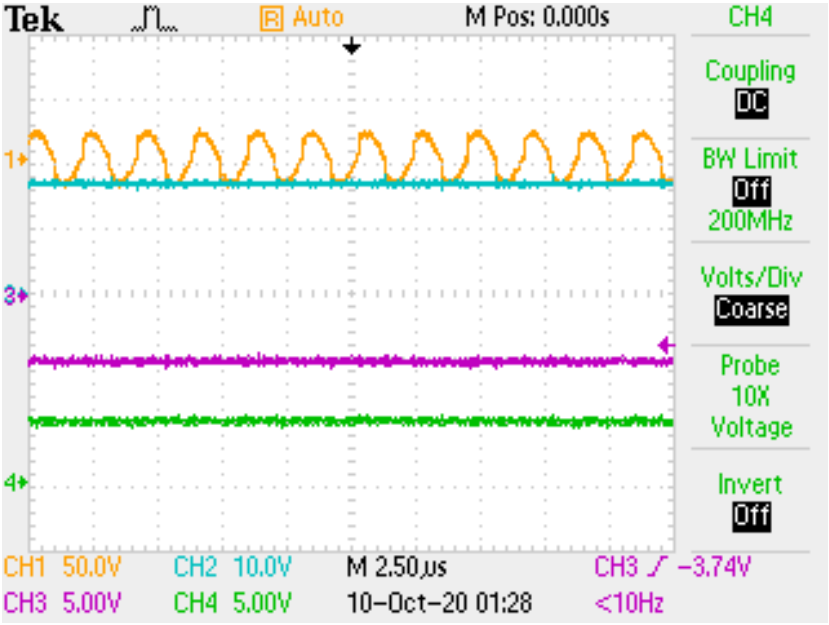


Fig. 52: Voltage waveforms (yellow-transformer primary side voltage, cyan-20V bus, green- +5V bus, purple- -5V bus)

of each gate driver is at least 10 kV to ensure the reliable operation of the HV switch. However, commercial-off-the-shelf (COTS) gate driver modules have isolation ratings as high as 5.7 kV [168], [169]. This rating implies that COTS gate driver modules are not equipped to drive a HV switch with a voltage rating greater than 5.7 kV. Prior studies on HV isolated gate drivers showcased designs based on some experimental switch modules (e.g., CPM3-10000-0350, XHV-9, XHV-7 developed by CREE) [151], [161], [162], [170]. However, none of the gate driver designs has been realized as a commercial high-voltage isolated gate driver solution as of now. Commercially available 10 kV rated DC-DC converters with 3 pF isolation capacitance have been incorporated in the second variation of the isolated gate driver design in this work.

7.4.3.1 Design and Fabrication Procedures

A single module of the proposed 10 kV rated gate driver features three compact (≈ 1 sq. inch) 10 kV rated isolated DC-DC converters to provide galvanic isolation for the power supplies of the gate driver IC [171]. These converters, having a power rating of 6 W, can operate at an input voltage ranging from 24 V to 36 V, and capable of producing a regulated output. A 5.7 kV_{RMS} rated reinforced isolated gate driver IC with 2.5 A sourcing and 5 A sinking current capability, has been selected for the proposed gate driver module. The selected gate driver IC has a dedicated pin (V_{EE2}) for ease of application of bipolar supply that facilitates the supply of recommended negative voltage required to ensure reliable turn OFF of SiC MOSFET. An optical fiber link has been designed and developed using transmitters, receivers, and plastic optical fiber that belong to the HFBR-0500Z series. The optical fiber link supports a data transmission rate of 5 MBd and can handle a breakdown voltage rating of 500 V/mm [172]. Therefore, a 20 mm length optical fiber cable can withstand a voltage level up to 10 kV with the added benefit of noise immunity offered by it. Therefore, the isolation mechanism for the control signal is insulated from noise coupling from any potential external source, thereby elevating the reliability of the isolated gate driver. A DC supply voltage of 24 V powers the gate driver board. Three isolated DC-DC converters yield three voltage rails of +24 V, +5 V, and -5V respectively. The +5 V rail powers the input side of the gate driver IC as well as the receiver of the optical fiber link. A linear regulator (LM1086) scales down the +24 V rail to a regulated +20 V rail. The +20 V rail and the -5 V rails are connected to the output side of the gate driver IC to generate the recommended voltage levels (+20 V, -5 V) required for reliable switching of the SiC MOSFETs. Another linear regulator (LM1086) is incorporated in the

design to generate a steady +5 V rail from the primary DC supply that is used to power the transmitter of the optical fiber link.

The modular gate driver has six isolated DC-DC converters, three for each module as in the single module. However, both modules share the same input DC supply and a single buffer IC (SN75451) with dual outputs feeding identical PWM signals to two transmitters equally distanced from the buffer IC. The rest of the circuit designs of the two gate driver modules are quite identical, thereby eliminating the possibility of performance variation of the gate driver modules as much as possible. One of the major design concerns of a multi-output gate driver is ensuring synchronization of the gate drive signals. To that end, two gate driver ICs, one for each module, are placed equally apart from the receivers of two fiber-optic links in the PCB design. Board-to-board connectors are used to connect the modular gate driver board to the modular HV switch to reduce parasitic inductance in the gate drive loop as well as providing mechanical rigidity to the assembly of the HV gate driver and the HV switch. The traces from the output signal pins of the gate driver ICs to the board-to-board connectors are kept short and of equal length to ensure synchronization of the gate signals as well as further minimization of parasitic inductances in the gate loop of the modules of the HV switch. The schematic of a single module of the modular HV gate driver and the fabricated modular HV gate driver board are shown in Fig. 53 and Fig. 54 respectively.

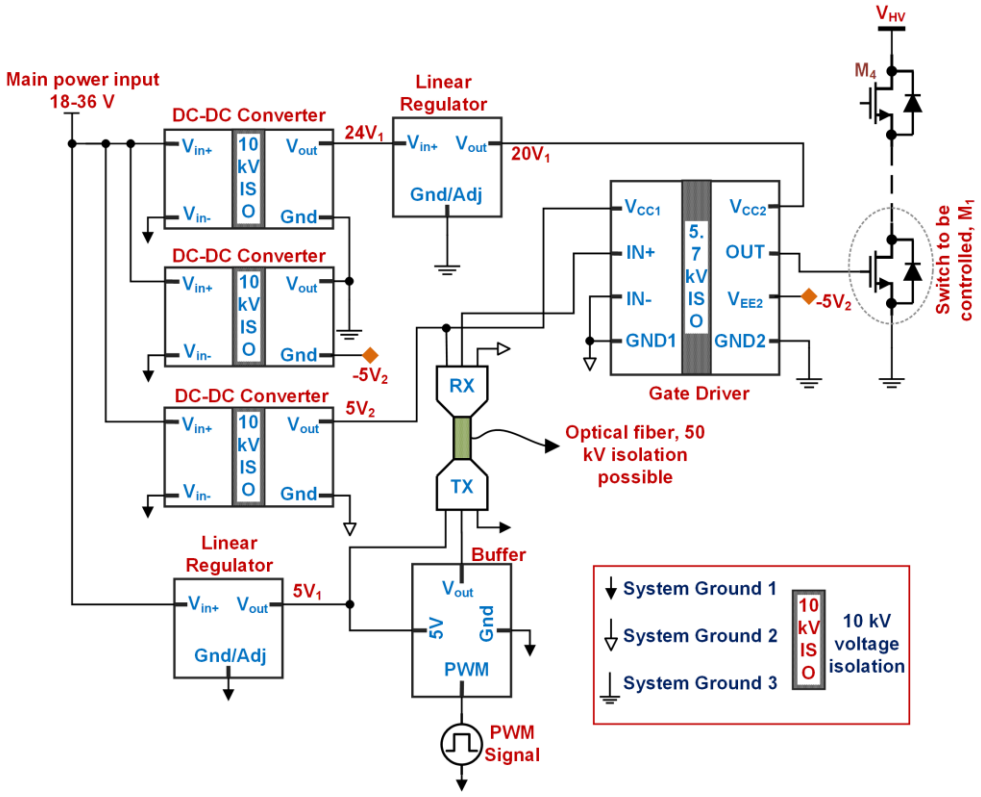


Fig. 53: Schematic of a single module of the proposed gate driver

7.4.3.2 Experimental Results

A 30V, 2A rated DC power supply has been used as the input of the 10 kV rated DC-DC converters. +24V, +5V and -5V voltage rails have been generated at the output of the DC-DC converters. Two sets of identical voltage rails have been generated for two gate driver modules. The gate driver outputs generated from the two gate driver modules have been well-synchronized and shown in Fig. 55.

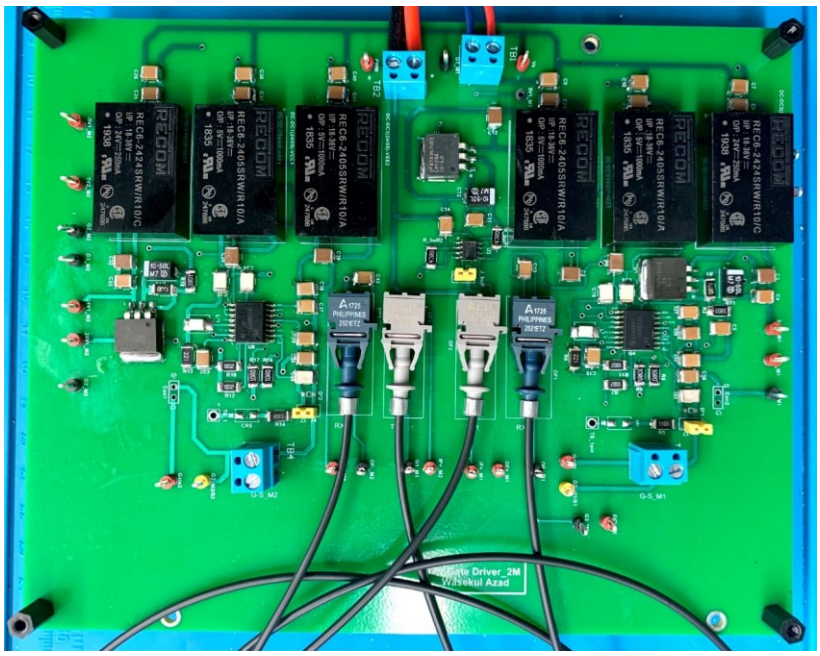


Fig. 54: Fabricated prototype of the in-house modular HV (10 kV rated) gate driver

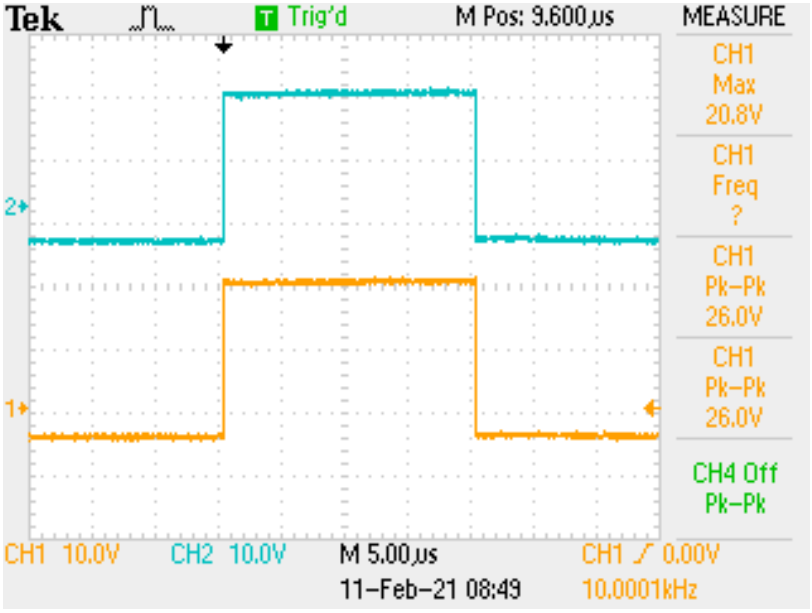


Fig. 55: Identical gate drive signals originated from the modular gate driver

7.5 Simulation Results of the Modular High-Voltage Switch

The modular HV switch comprising two modules has been simulated in LTSpice at a DC supply voltage of 12 kV and a switching frequency of 20 kHz with a 9.6 kΩ resistive load. Each module consists of four series-connected 1.7 kV rated SiC MOSFETs. Simulated voltages across the drain-source terminals of the series-connected MOSFETs in identical positions in each switch module showcase remarkable similarity.

The HV switch consists of four pairs of identically positioned MOSFETs. Each pair of MOSFETs are separated by three MOSFETs in between. Simulation results have demonstrated outstanding voltage balancing among all the series-connected MOSFETs. A maximum voltage imbalance of 60 V has been recorded among the series-connected MOSFETs of the HV switch. Fig. 56 shows the simulated voltages across the drain-source terminals of the series-connected MOSFETs in the modular HV switch.

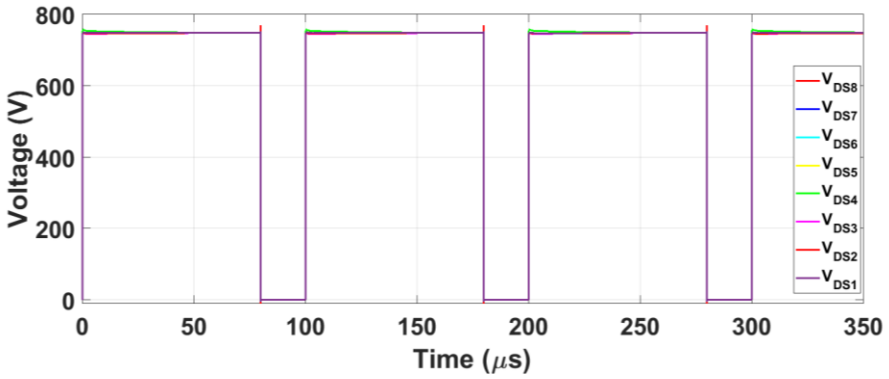


Fig. 56: Simulated drain-source voltages across the eight individual MOSFETs (V_{DC} = 6 kV, f_{sw} = 20 kHz)

The lowest rise time was measured across the switch farthest from the master switch in each module and was recorded close to 13.4 ns. The master MOSFET of each module exhibited

the highest rise time in simulation, close to 19 ns. The simulated rise time of the entire modular switch was recorded as 17.8 ns, markedly faster than the Si devices and SiC devices from earlier generations with a similar breakdown voltage rating.

Simulated gate-source voltage waveforms across the slave MOSFETs (S_2, S_3, S_4, S_6, S_7, S_8) bear excellent resemblance to the gate drive signals originated from the external gate drivers, thereby ensuring reliable turn-ON and turn-OFF of all the SiC MOSFETs in the series stack. In addition, voltages measured across the gate-source terminals of the identical MOSFETs in each module exhibit remarkable similarity as well, therefore validating the efficacy of the modular approach of the proposed switch.

During the ON-period, all the gate-source signals stick to a voltage level close to 20 V. Conversely, during the OFF-period, all the gate signals stay close to a voltage level of -5V, which is recommended to reliably turn a SiC MOSFET OFF. To that end, all the series-connected MOSFETs in the series stack undergo reliable switching transitions. The simulated voltages across the gate-source terminals of all the series-connected MOSFETs are shown in Fig. 57.

7.6 Experimental Setup and Results

7.6.1 Experimental Setup

Each switching module consists of four (4) 1.7 kV SiC switches, and the theoretical operating voltage of a single module is thus 6.8 kV. With a certain headroom, this module is

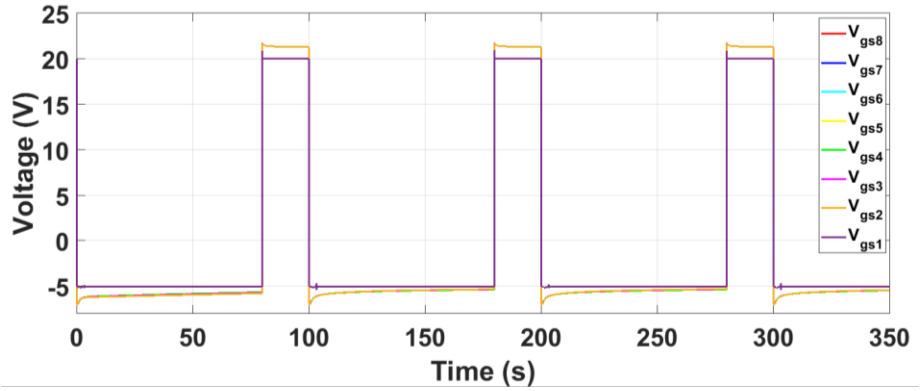


Fig. 57: Simulated gate-source voltages across the eight individual MOSFETs (V_{DC} = 6 kV, f_{sw} = 20 kHz)

tested up to 5 kV. Two of these modules are connected in series to build a 10 kV switch. This 10 kV switch has been tested up to a DC supply voltage of 6 kV.

The selected MOSFET features a separate driver pin to minimize stray inductance in the gate driver loop, thereby assisting to minimize voltage overshoot present in the gate drive signals stemming from the stray inductance of the gate drive loop. Top mount SMD heatsinks are soldered to the exposed drain pads of the SMD MOSFETs for efficient heat dissipation. Four 150 kΩ surface-mount resistors, each rated for 6 W and 600 V are connected in series to form a branch, and two of such branches are connected in parallel to form a resistor bank with increased power handling capability and used as the balancing resistors. Ceramic surface-mount capacitors are connected in series and parallel to form the coupling capacitors and snubber capacitors with required voltage withstanding capability. 3.3 kV rated surface-mount SiC diodes are connected in series to sustain the maximum possible voltage stress of $3V_{DC}/8$ (≈ 3.75 kV) across this block at a maximum supply voltage of 10 kV and this block is connected in parallel with the coupling capacitors to form the gate-loop diodes. A surface-mount gate

resistor (15 Ω) followed by a surface-mount ferrite bead (2 kΩ @ 30 MHz) is placed in the gate loop of each MOSFET pair. 20 V and 6.2 V rated zener diodes were connected across the gate-source terminals of the MOSFET pairs to safeguard the gate from voltage overshoots. A 15μH rated surface-mount inductor was connected in series with the switch to protect it from a sudden in-rush current. A 12 kV rated 0.2 μF capacitor bank was constructed using four series-connected film capacitors, each with a voltage rating of 3 kV. The capacitor bank was accommodated in the PCB of the HV switch for the ease of conducting HV testing, minimizing stray inductances, and was connected in parallel with the DC power supply. Two board-board connectors were incorporated in the PCB design of the HV switch to form low-inductance interfaces with the custom gate drivers. A separate PCB was designed and developed to accommodate a 9.6 kΩ resistor bank constructed using sixteen 100 W rated 600 Ω thick-film resistors. All of the resistors were tethered to an individual heatsink to facilitate effective heat dissipation. All of the measurements were recorded on a mixed-signal oscilloscope (MSO64) using differential IsoVu probes made by Tektronix. The probes are capable of delivering accurate differential measurements up to ±2.5 kV with a common-mode voltage range of ±60 kV. The fabricated prototype of the modular HV switch is shown in Fig. 58. The streamlined combination of the modular HV switch and the HV gate driver is shown in Fig. 59. Fig. 60 showcases the entire experimental setup consisting of the modular HV switch coupled with the custom HV isolated gate driver and a resistive load.

7.6.2 Experimental Results

The proposed modular HV switch coupled with the custom in-house HV isolated gate driver was tested using a DC supply voltage up to 6 kV and at a repetition frequency up to 15

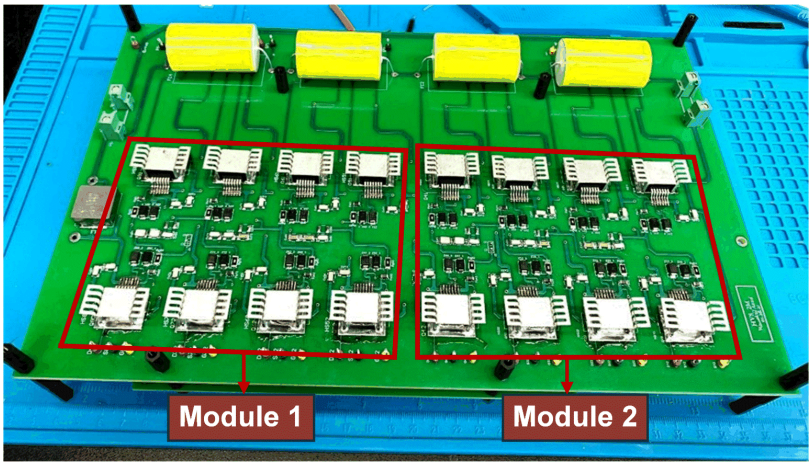


Fig. 58: Fabricated prototype of the proposed HV modular switch

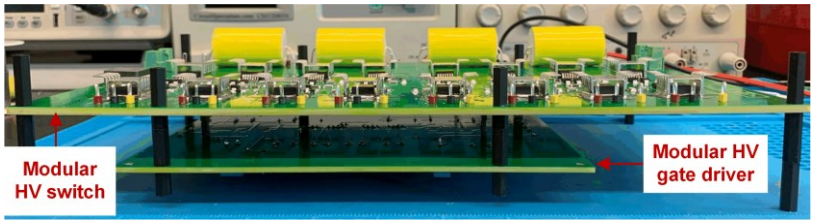


Fig. 59: Integrated prototype of the HV switch with the HV isolated gate driver

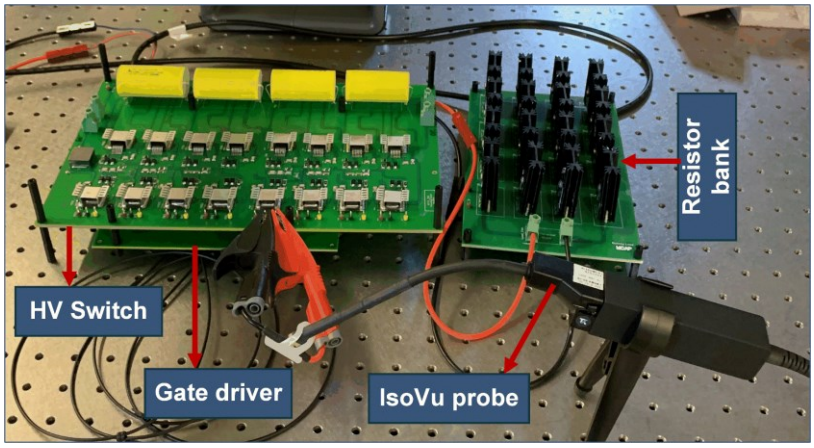


Fig. 60: Experimental setup including the HV switch, the HV isolated gate driver and the resistor bank

kHz using the 9.6 kΩ resistive load. Experimental results show reliable turn-ON and turn-OFF characteristics of the entire HV switch under the specified operating condition. The voltages measured across the drain-source terminals of the MOSFETs in a single module are shown in Fig. 61 (V_{DC} = 5 kV, f_{sw} = 40 kHz, duty cycle = 50%).

A maximum voltage imbalance close to 50 V was recorded among the drain-source

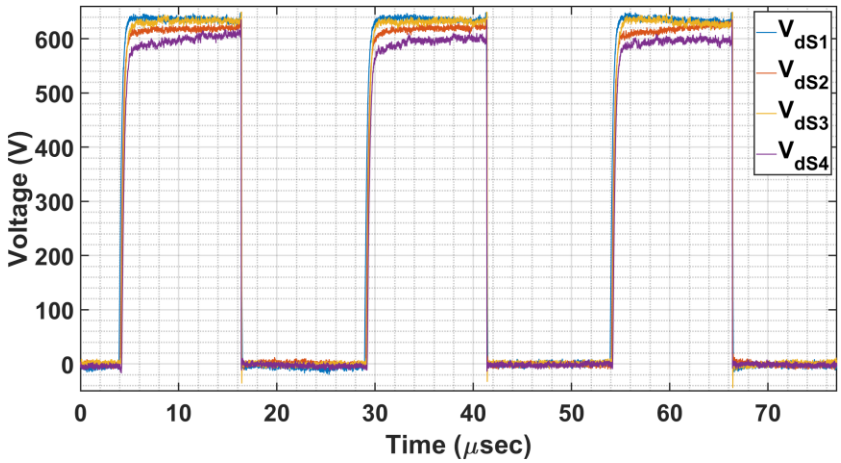


Fig. 61: Experimental drain-source voltages measured across the individual MOSFETs in a single module (V_{DC}= 5 kV)

voltages of the series-connected MOSFETs in a single module that experienced a DC voltage stress of 2.5 kV, thereby validating the effectiveness of the proposed voltage-balancing scheme. To test the entire switch at a higher voltage level, the voltage across the 9.6 kΩ load at a supply voltage of 6 kV and a repetition frequency of 10 kHz was measured and shown in Fig. 62. The measured voltages across the drain-source terminals of the series-connected MOSFETs from both of the modules are depicted in Fig. 63. In this configuration, each module experienced maximum voltage stress close to 3 kV. A maximum voltage imbalance close to

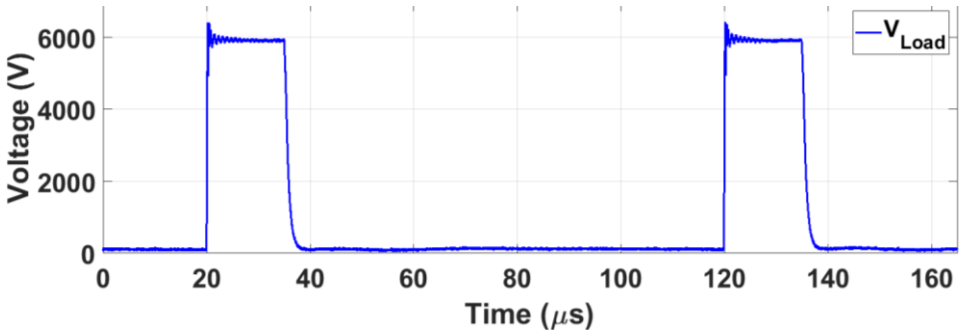


Fig. 62: Voltage measured across the 9.6 kΩ resistive load (V_{DC}= 6 kV) to test the 10 kV switch

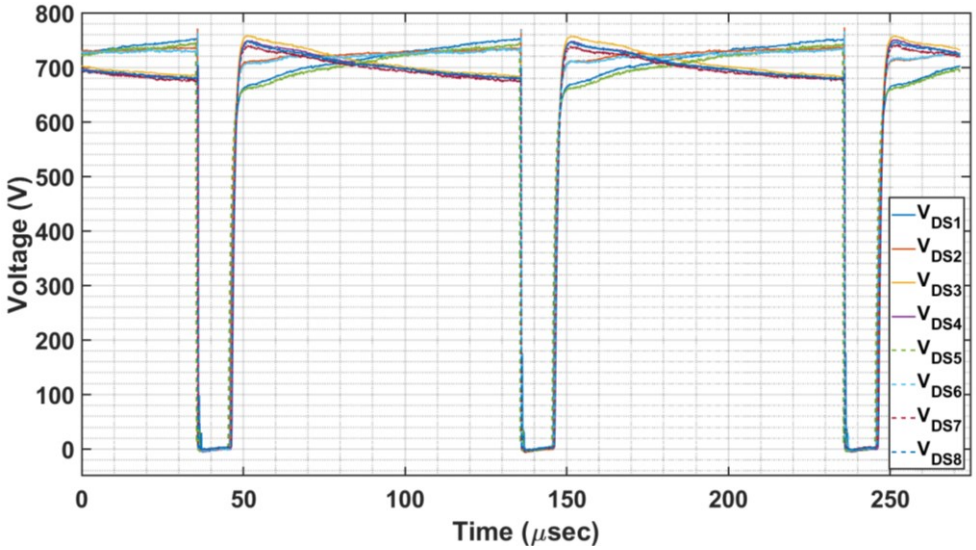


Fig. 63: Experimental drain-source voltages measured across the individual MOSFETs in the entire HV switch (V_{DC}= 5 kV)

80 V was recorded among the drain-source voltages, which is negligible compared to the breakdown voltage rating of an individual MOSFET.

The lowest rise time was measured as 41 ns associated with the slave MOSFETs (S_4, S_8) located farthest from the master MOSFET in each module. The highest rise time belonged to the master MOSFETs (S_1, S_5) in each module, and recorded as 52 ns. The rise time of the HV switch can be approximated by the highest rise time associated with the series-connected

MOSFETs. That being said, the recorded rise time of the proposed modular HV switch is still considerably lower compared to the COTS switches with similar voltage ratings.

The voltages measured across the gate-source terminals of the series-connected MOSFETs in a single module of the fabricated modular HV switch are shown in Fig. 64.

The time delay between the gate drive signals is not distinguishable, thereby

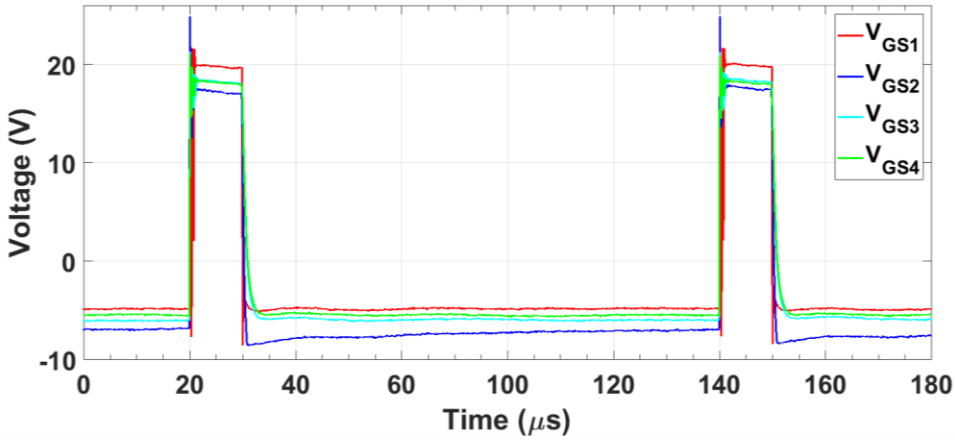


Fig. 64: Experimental gate-source voltages measured across the individual MOSFETs in a single module (V_{DC}= 6 kV)

minimizing the synchronization issue related to these signals. During the OFF state, the measured gate-source voltages of the slave MOSFETs are close to -6 V, governed by the Zener voltage of the Zener diodes connected across the gate-source terminals. Similarly, the measured gate-source voltages of the slave MOSFETs during the turn-ON period are close to 20 V, defined by the Zener voltage of the Zener diodes connected across the gate-source terminals of these MOSFETs. Therefore, all the series-connected MOSFETs demonstrate reliable turn-ON and turn-OFF in response to the corresponding gate-drive signals, which are within the recommended voltage levels related to the SiC MOSFETs.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Summary

Pulsed power sources are rapidly garnering interest from a diverse array of application fields. In stark contrast to their humble beginning, the applications of the pulsed power sources are not limited to military purposes only nowadays. The unique capability of pulsed power sources to deliver an enormous amount of power within a relatively short period is being leveraged in various sectors including industrial, biomedical, nuclear, etc. HV switches can be regarded as the centerpieces of a majority of the existing pulsed power sources. Traditional vacuum tube-based switches or spark gap switches can fulfill the high voltage and current requirement of the HV switches pertaining to the pulsed power applications. However, limited lifetime, long jitter, incompatibility with high switching frequency leave these switches trailing behind the new generation of solid-state switches showcasing superiority in these aforementioned performance metrics. That being said, solid-state switch options that can meet the high voltage requirements of the pulsed power applications are few and far between and confined within laboratory setup, therefore not available for off-the-rack use.

This dissertation presents a HV series-connected SiC switch with four stages that can address the lack of commercial HV switches with minimal footprint and complexity thanks to a relatively moderate number of passive components and a single gate driver. This design takes voltage balancing issues among series-connected devices into consideration and delivers excellent voltage balancing performance substantiated by simulation and experimental results. This dissertation also documents a unique wrinkle in the HV switch design in the form of

modularity in the HV switch design that can facilitate voltage withstanding scalability without redesigning the entire switch. Simulation and experimental results are presented in this dissertation to vindicate the claim and validate the modular design.

NLTL differs from other sources of pulsed power owing to its lack of switching elements, thereby deeming it an intriguing pulsed power solution. However, a continuous stream of input power supply is required to obtain a series of output pulses, thereby increasing the footprint and cost of the entire system due to the increased power requirement of the input power supply.

In this dissertation, a novel self-sustaining closed-loop configuration consisting of an NLTL, a power amplifier, HV pulse generator, and RF matching networks has been proposed that is capable of sustaining output RF pulses from a single input pulse. Simulation and experimental results have substantiated the efficacy of the proposed technique. This closed-loop NLTL configuration can usher in a new generation of portable and compact pulsed power sources and can be used in a variety of applications.

8.2 Future Work

NLTLs and HV solid-state switches are two cornerstones of the pulsed power technology moving forward. This dissertation lays out the groundwork for future researchers by narrating the present capabilities and the shortcomings of these technologies. The propositions pertaining to a self-sustaining soliton generator and a modular series-connected HV switch and the validation of these propositions through simulation and experimental results can stimulate new ideas in the future. Future works related to self-sustaining soliton generator can include the following tasks.

(i) Further exploration of dual-diode NLTL configuration to increase the center frequency of the generated output RF signal.

(ii) Identifying new nonlinear materials with superior capacitance ratios to increase the theoretical limit of the cutoff frequency of the NLTL.

(iii) Incorporating HV switches in the pulse generator circuit to increase the peak amplitude of the input pulse, and paralleling multiple power amplifiers to increase the power rating of the entire NLTL circuit.

The field of series-connected HV switch holds enormous potential, thereby options of innovations are aplenty in this field. As a continuation of the research work undertaken pertaining to this field, the following scopes can be further investigated.

(i) Incorporating new generation Sic MOSFETs with higher breakdown voltage rating to increase the overall voltage breakdown rating of the HV switch.

(ii) Designing a inductive power transfer (IPT) based custom gate driver to provide very high isolation for the power supplies and the control signal of the gate driver so that it can drive a modular HV switch with a voltage rating in the vicinity of 30 kV.

The aforementioned future work related to NLTL and HV switch can act as reference points for future works in this field to further improve the proposed designs of self-sustaining soliton generator and HV series-connected switch and embellish the pulsed power field.

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